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EQCO30R5.D 3G/HD-SDI Video Cable Equalizer

Features:

- Supports up to 140 Meters of Cable at 2.97 Gbps Using High-Quality Coax
- Supports up to 200 Meters of Cable at 1.485 Gbps Using High-Quality Coax
- Supports up to 450 Meters of Cable at 270 Mbps Using High-Quality Coax
- Compatible with all SMPTE3G SDI data rates:
  - SMPTE259M SDI, 143 to 360 Mbps
  - SMPTE344M, 540 Mbps
  - SMPTE292M HD-SDI, 1.485 Gbps
  - SMPTE372M Dual-Link HD-SDI, 2.97 Gbps
  - SMPTE424M Dual-Speed 3G-SDI, 2.97 Gbps
- Pin Compatible with Gennum and National Semiconductor Parts
- Also Operates with 8B/10B Coding
- Single 3.3V Supply.
- Low-Power Consumption (220 mW, 3.3V Supply; 80 mW, 1.2V Supply)
- Better Robustness Due to Transmit Amplitude Independent Operation
- 16-Pin, 0.65 mm Pin Pitch, 4 mm QFN Package
- -40°C to +85°C Industrial Temperature Range
- Pb-Free and RoHS Compliant

Applications:

- High Definition, High Frame Rate Pro-Video HD-SDI Frame Store
- Surveillance, Industrial/Inspection, Medical Video Inputs
- HDcctv Applications

Note: The EQCO30R5 video equalizer can be used in combination with the EQCO30T5 cable driver. This device is capable of receiving the uplink signal whilst other key parameters remain compliant to SMPTE specifications. Please refer to the Microchip web site (www.microchip.com) for the EQCO30T5 data sheet.

Introduction:

The EQCO30R5 is a video equalizer for 3G/HD/SD-SDI video, with speeds up to 2.97 Gbps. It is designed to be a direct replacement for competing video equalizers. In addition to downlink functionality from camera to frame grabber, it can also transmit a 5 Mbps uplink signal from the frame grabber to the camera. Additionally, power can be provided over the same cable using the same chip and a few external components. The device operates with 8B/10B coded signals up to 3.125 Gbps.

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Typical Link Performance

Table 1, Table 2, and Table 3 give an overview of video equalizer typical performance at room temperature without using the uplink and without providing power over the same coax. When providing power or using the uplink communication to the camera, a small length penalty may arise (in cable length, typically 10%) due to added parasitics and noise. The uplink operates to at least 400m at the 5 Mbps bit rate.

TABLE 1: BELDEN TYPICAL EQUALIZATION PERFORMANCE

	Name	Belden 7731A	Belden 1694A	Belden 1505A	Belden 1505F	Belden 1855A
	Type	Long Distance	Industry Standard	Compromise Coax	Flexible	Thinnest Cable
Diameter	(mm)	10.3	6.99	5.94	6.15	4.03
270 Mbps	(m)	718	469	384	302	270
1.485 Gbps	(m)	332	223	187	136	132
2.97 Gbps	(m)	219	149	128	89	91

TABLE 2: GEPCO TYPICAL EQUALIZATION PERFORMANCE

	Name	Gepco VHD1100	Gepco VSD2001	Gepco VPM2000	Gepco VHD2000M	Gepco VDM230
	Type	Long Distance	Industry Standard	Compromise Coax	Flexible	Thinnest Cable
Diameter	(mm)	10.3	6.91	6.15	6.15	4.16
270 Mbps	(m)	772	502	387	305	273
1.485 Gbps	(m)	372	241	187	138	133
2.97 Gbps	(m)	252	163	128	91	92

TABLE 3: CANARE TYPICAL EQUALIZATION PERFORMANCE

	Name	Canare L-7CFB	Canare L-5CFB	Canare L-4CFB	Canare L-3CFB	Canare L-2.5CFB
	Type	Long Distance	Industry Standard	Compromise Coax	Thin Cable	Thinnest Cable
Diameter	(mm)	10.3	6.99	5.94	6.15	4.03
270 Mbps	(m)	615	434	344	287	223
1.485 Gbps	(m)	281	201	161	135	109
2.97 Gbps	(m)	182	132	107	90	73

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EQCO30R5.D

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EQCO30R5.D

1.0 DEVICE OVERVIEW

The EQCO30R5 is a multi-rate adaptive cable equalizer, designed to restore signals received over coaxial cable. The EQCO30R5 chip is optimized for SMPTE HD/SDI signals, but works equally well with 8B/10B coded signals. The device operates from a single 3.3V power supply. A sister device operates from a single 1.2V power supply, which reduces power consumption at the cost of voltage compatibility with competitive parts. For more information on the 1.2V part, please contact Microchip.

The EQCO30T5 is a cable driver that matches to the EQCO30R5, since it can receive the uplink signal. Implementing the uplink requires very few additional components on both sides of the link and complies with SMPTE specifications. The EQCO30T5 data sheet is available separately from Microchip.

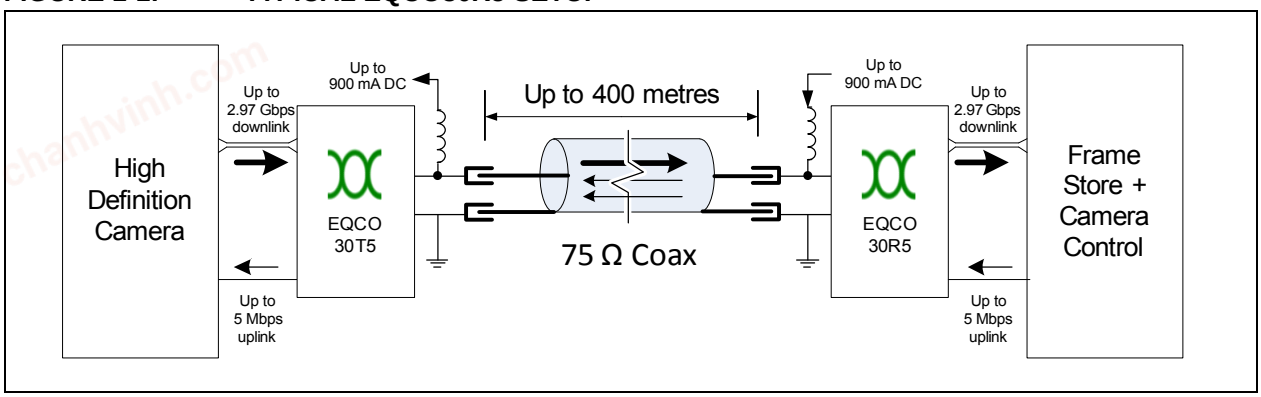
The EQCO30R5 has a DC restore circuit to recover SMPTE pathological patterns in the data stream. The EQCO30R5 has a variable gain to compensate for low-frequency attenuation through the coax and variations in transmit amplitude.

Figure 1-1 shows a typical communication link using the EQCO30T5 and EQCO30R5 chips

.

Note: Email address: eqcoproducts@microchip.com

FIGURE 1-1: TYPICAL EQCO30R5 SETUP



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1.1 Pinout and Pin Description

FIGURE 1-2: EQCO30R5.D PIN DIAGRAM (VIEWED FROM TOP)

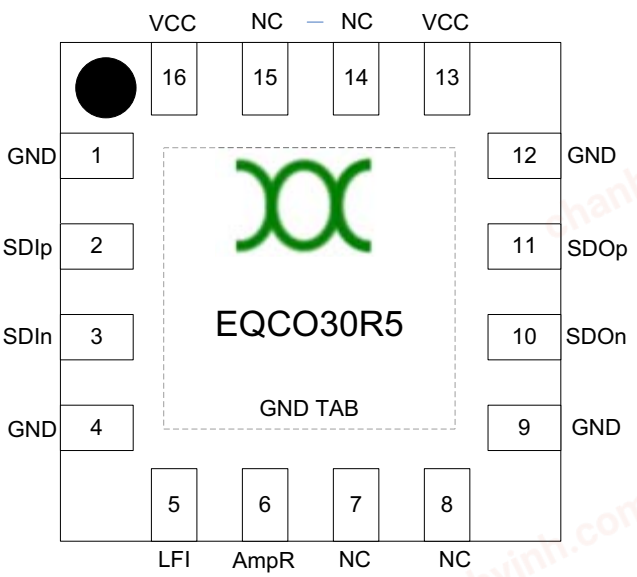


TABLE 1-1: EQCO30R5.D PIN DESCRIPTIONS

Pin Number	Pin Name	Signal Type	Description
(TAB)	GND	Power	Use as single-point ground.
13, 16	VCC	Power	+3.3V of power supply.
1, 4, 9, 12	GND	Power	Connect to ground of power supply.
2, 3	SDIp, SDIn	CML Input	Serial input positive/negative differential serial input. Connect SDIn to ground reference via termination network. External 75Ω resistors are required.
11, 10	SDOp/SDOn	CML Output	Serial output positive/negative differential serial output. Output has a swing of 2x370 mV and has 50Ω on-chip termination resistors to internal V_{DD} (1.2V).
5	LFI	Input	Uplink signal. (Low = 0V, High = 1.2V). When driving from 3.3V, an external series resistance of 6.2 kΩ is required.
6	AmpR	Input	Connect to ground with a 1 kΩ resistor, defining the uplink amplitude to 150 mV.
7	NC	Input	Do not connect. Used for internal testing.
8	NC	Input	Do not connect. Used for internal testing.
14	NC	Input	Do not connect. Used for internal testing.
15	NC	Input	Do not connect. Used for internal testing.

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1.1.1 SDIP/SDIN

SDIp/SDIn together form a differential input pair. The EQCO30R5 analyzes the differential voltage between these pins and adaptively equalizes for signal level and frequency response. The equalizer automatically detects and adapts to signals with different edge rates, different attenuation levels and different cable characteristics. Both SDIp and SDIn inputs need to be terminated by an external 75Ω resistor to GND.

1.1.2 SDOP/SDON

SDOp/SDOn together form a differential CML pair outputting the reconstructed far-end transmit signal. SDOp/SDOn are terminated on-chip with two 50Ω resistors to 1.2V. These outputs should be AC coupled to the deserializer (unless a 800 mV-1V common-mode voltage is acceptable). For SMPTE signals, it is best to use 4.7 µF AC coupling capacitors.

1.1.3 LFI

LFI is the uplink input signal that will be transmitted on the SDIp/SDIn pair. LFI must be a 0-1.2V signal. The pin has an internal resistor of 3.6 kΩ. When driving with a 3.3V (2.5V) signal, an external resistor of 6.2 kΩ (3.9 kΩ) should be placed in series close to the EQCO30R5 chip. When not using uplink communications, leave this pin floating.

1.1.4 AMPR

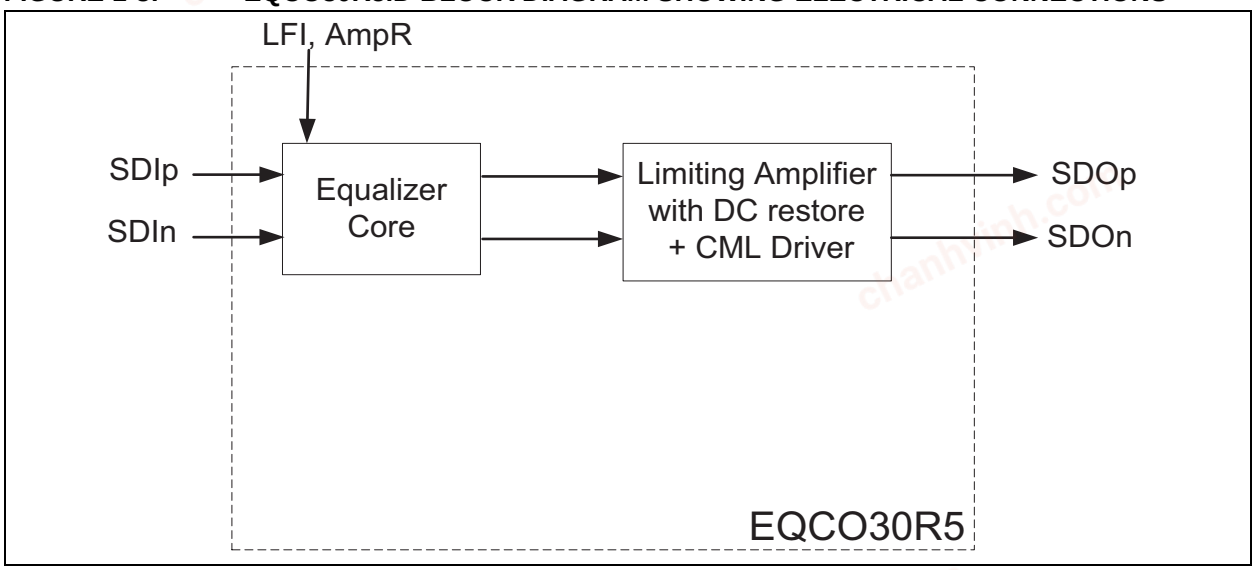
AmpR is a VCC resistor that sets the transmit amplitude of the uplink output driver. The typical value is R_{amp} = 1 kΩ for 150 mV transmit amplitude. When not using uplink communications, leave this pin floating.

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1.2 Circuit Operation

FIGURE 1-3: EQCO30R5.D BLOCK DIAGRAM SHOWING ELECTRICAL CONNECTIONS



1.2.1 EQUALIZER CORE

The EQCO30R5 has an embedded equalizer in the receive path with the following characteristics:

- Auto-Adaptive

The equalizer controls a multiple-pole analog filter which compensates for attenuation of the cable, as illustrated in Figure 1-4. The filter frequency response needed to restore the signal is automatically determined by the device using a time-continuous feedback loop that measures the frequency components in the signal. Upon the detection of a valid signal, the control loop converges within a few microseconds.

- Variable Gain

The EQCO30R5 equalizer has variable gain to compensate for low-frequency attenuation through the coax and variations in transmit amplitude; this makes the equalizer performance more robust, even at maximum cable lengths.

- Variable Coax

The equalizer can receive attenuated signals from other types of cables besides the Belden1694A.

- Multi-Speed

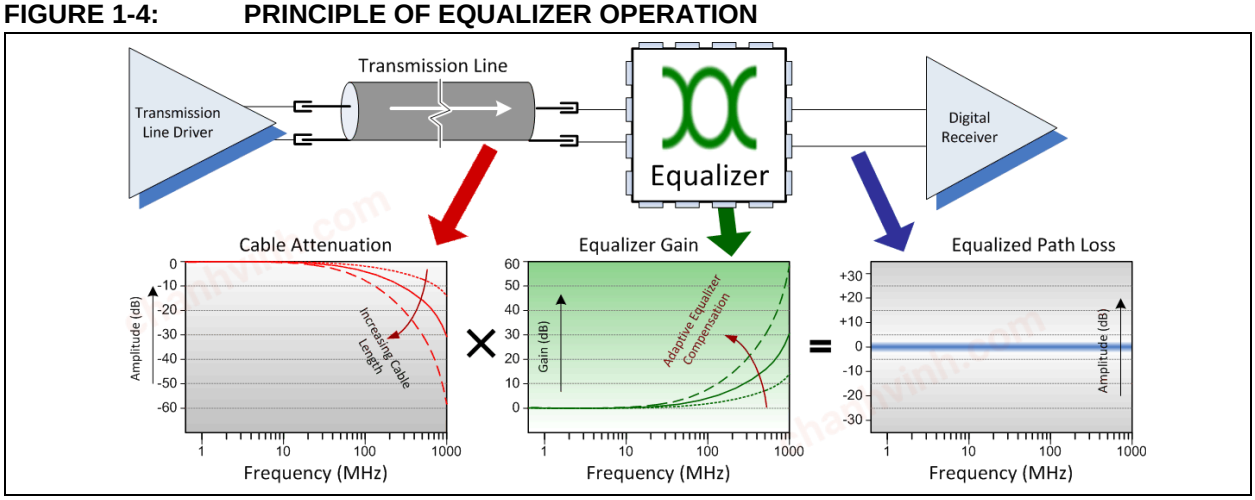
The EQCO30R5 works at data rates from 143 Mbps to 2.97 Gbps. With 8B/10B coding, the allowable bit rate is extended from 50 Mbps to 3.125 Gbps.

Example equalizer performance measurements can be found in Figure B-2.

1.2.2 RX OUTPUT DRIVER

The output driver converts the output of the equalizer core to an LVDS-like signal and sends it onto a 100Ω differential transmission line.

FIGURE 1-4: PRINCIPLE OF EQUALIZER OPERATION



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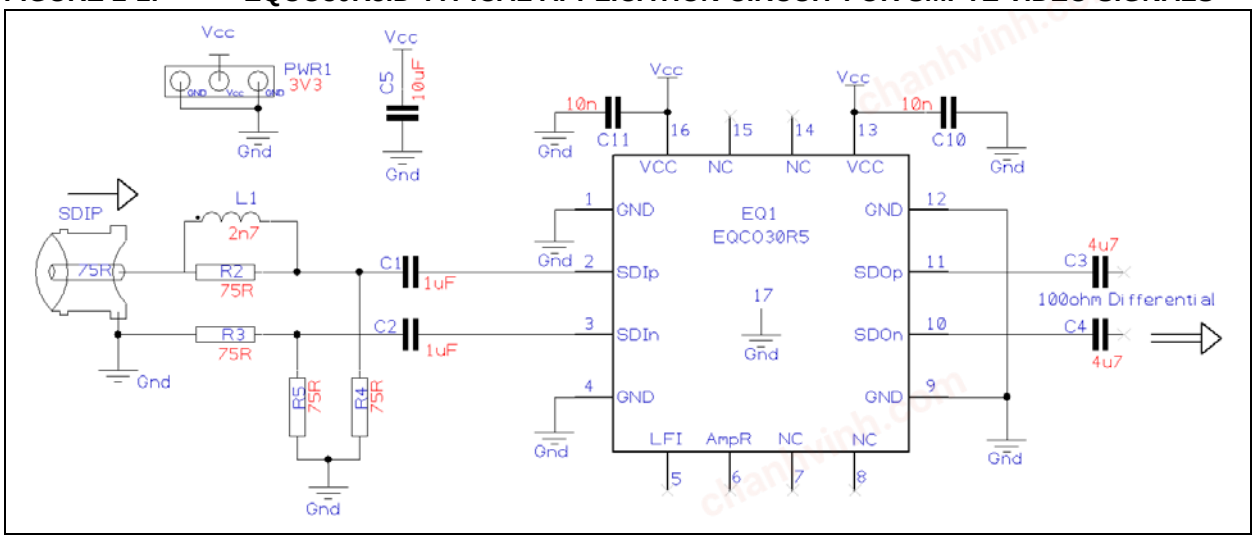
EQCO30R5.D

2.0 APPLICATION INFORMATION

2.1 Typical Application Circuit for SMPTE Video Signals

Figure 2-1 illustrates a typical schematic implementation of the EQCO30R5 used as an equalizer for SMPTE video signals.

FIGURE 2-1: EQCO30R5.D TYPICAL APPLICATION CIRCUIT FOR SMPTE VIDEO SIGNALS



2.1.1 RETURN-LOSS NETWORK

For optimal return-loss, an external return-loss network is needed. The value of R2 is 75Ω, and the value of L1 is 2.7 nH.

TABLE 2-1: COMPONENT RECOMMENDATION FOR THE EQCO30R5.D BOARD LAYOUT FOR SMPTE VIDEO SIGNALS

Element	Value	Size	Recommended Component
R2, R3, R4, R5	75Ω ±1%	0402	
L1	2.7 nH	0402	

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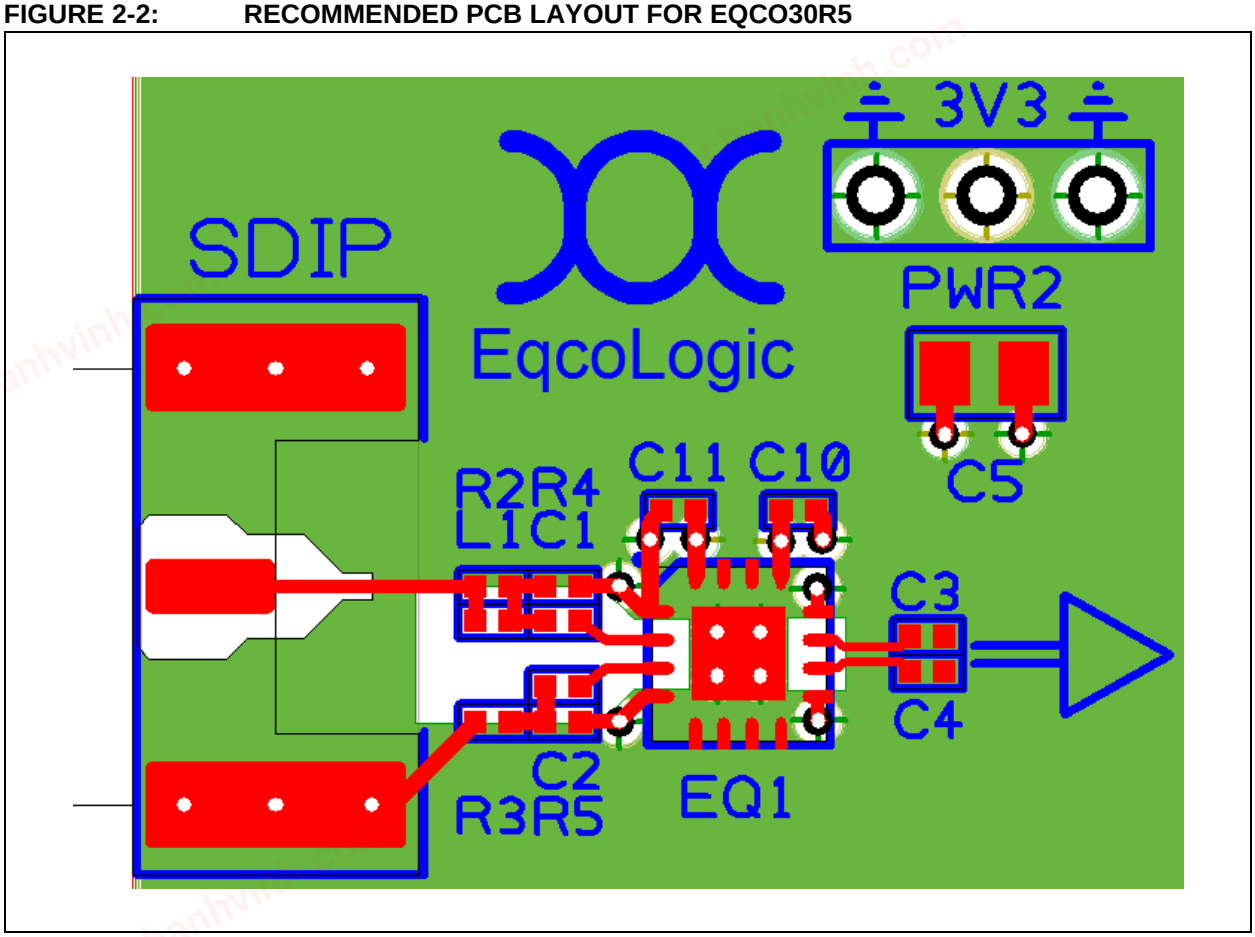
2.1.2 GUIDELINES FOR PCB LAYOUT

All components in the high-speed signal path should be 0402 size for minimal parasitic effects.

The transmission line between the BNC connector and the return-loss network (L1, R2) shall be a 75Ω single-ended transmission line. Components R2, R4 and R5 are 75Ω resistors, and component L1 is a 2.7 nH inductor. Component R3 is the 75Ω termination resistor to GND. Components C1 and C2 are AC coupling capacitors connected to the input of the chip. Two decoupling capacitors (C10, C11) are placed between VCC and GND, close to the chip. The output of the chip is connected to the deserializer or FPGA with a 100Ω differential transmission line. To minimize unwanted parasitic effects, a cutout of the ground and power plane is made underneath capacitor C6 and underneath the input pins of the EQCO30R5 chip.

Figure 2-2 shows a recommended layout for the EQCO30R5 implementation.

FIGURE 2-2: RECOMMENDED PCB LAYOUT FOR EQCO30R5



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2.2 Typical Application Circuit for Bidirectional Link with Power Over Coax

FIGURE 2-3: EQCO30R5.D TYPICAL APPLICATION CIRCUIT FOR BIDIRECTIONAL LINK WITH POWER OVER COAX

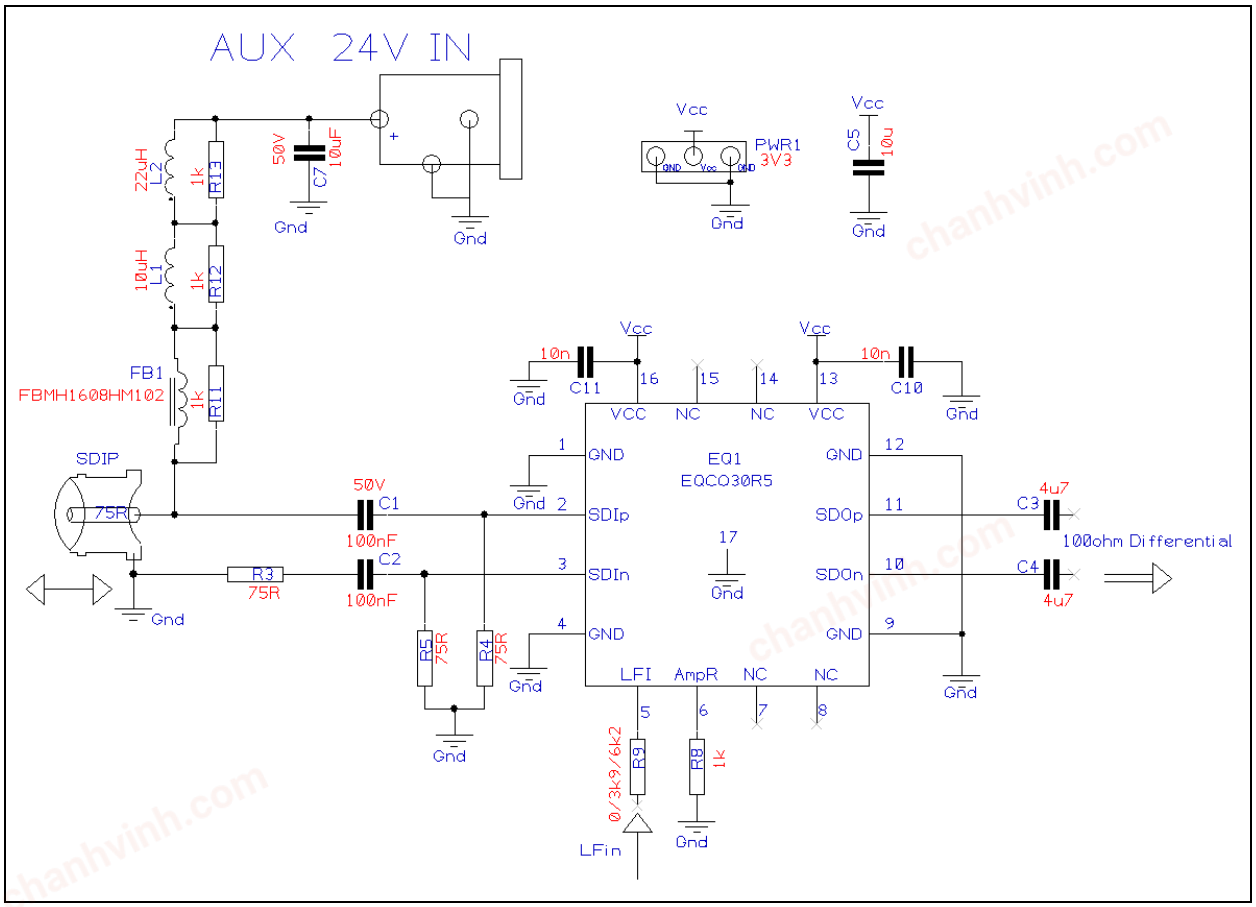


TABLE 2-2: COMPONENT RECOMMENDATION FOR THE EQCO30R5.D BOARD LAYOUT

Element	Value	Size	Recommended Component
Fb1, Fb2	1 kΩ @ 100 MHz Ferrite Bead	0603	FBMH1608HM102 from Taiyo Yuden
L1	10 µH	1812	1812PS_103 from Coilcraft

2.2.1 BIDIRECTIONAL LINK IN SMPTE APPLICATIONS

When using the bidirectional link with power supply transmission, the components (FB1, L1 and L2) and layout are very critical. Changes in the design or components may result in decreased performance.

2.2.2 PCB LAYOUT

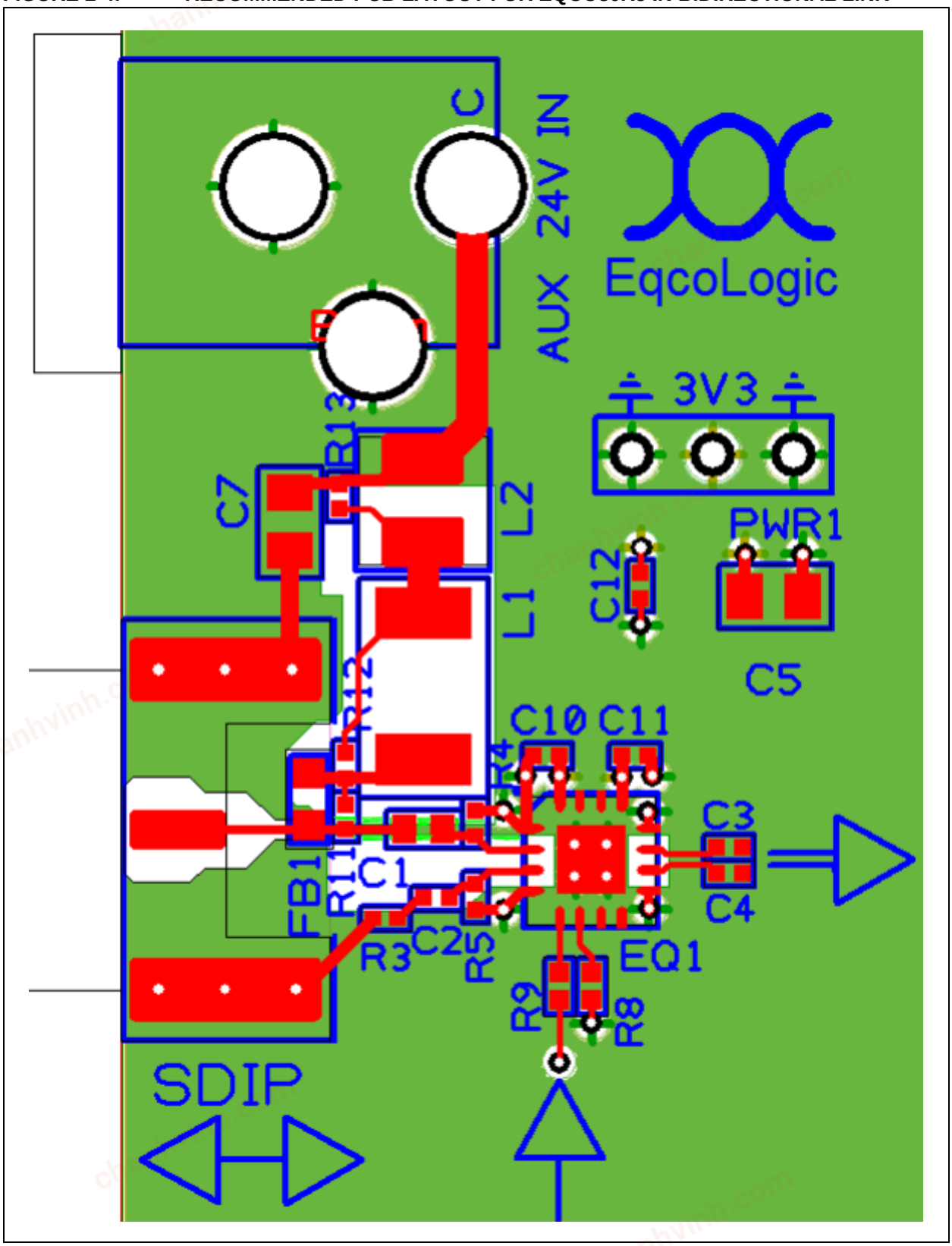
All components in the high-speed signal path should be 0402 size for minimal parasitic effects.

Figure 2-4 shows a recommended layout for the EQCO30R5 with uplink and power over coax.

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FIGURE 2-4: RECOMMENDED PCB LAYOUT FOR EQCO30R5 IN BIDIRECTIONAL LINK



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3.0 ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Ratings

Stresses beyond those listed under this section may cause permanent damage to the device. These are stress ratings only and are not tested. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 3-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Conditions	Min.	Typ.	Max.	Units
Storage Temperature	—	-65	—	+150	°C
Ambient Temperature	Power applied	-55	—	+125	°C
Operating Temperature	Normal operation (VCC = 3.3V ±5%)	-40	—	+85	°C
Supply Voltage to Ground	—	-0.8	—	+3.6	V
DC Input Voltage	—	-0.8	—	+3.6	V
DC Voltage to Outputs	—	-0.8	—	+3.6	V
Current into Outputs	Outputs low	—	—	90	mA
Electrostatic Discharge (ESD) HBM	JEDEC EIA/JESD-A114A	>2.2	—	—	kV
Electrostatic Discharge (ESD) Contact	IEC 61000-4-2	>4	—	—	kV
Latch-Up Current	—	>100	—	—	mA (DC)

TABLE 3-2: ELECTRICAL CHARACTERISTICS (OVER THE OPERATING VCC AND -40 TO +85°C RANGE)

Parameter	Description	Min.	Typ.	Max.	Unit
Power Supply					
V_{CC}	Supply voltage	3.15	3.3	3.45	V
I_S	Supply current, both transmitting and receiving	—	55	—	mA
Operational Bit Rate					
BR_{smpte}	Bit rate using SMPTE data	0.143	—	3.0	Gbps
BR_{8B10B}	Bit rate using 8B/10B coded data	0.05	—	3.125	Gbps
SDIp Connection to Coax					
Z_{coax}	Coax cable characteristic impedance	—	75	—	Ω
R_{loss}	Coax return-loss as seen on SDIp pin. Frequency range = 1 MHz-1.5 GHz	—	—	-15	dB
R_{loss}	Coax return-loss as seen on SDIp pin Frequency range = 1.5 GHz-3 GHz	—	—	-10	dB
$\triangle V_{TX}$	Transmit amplitude (at camera end into 75Ω)	500	800	1200	mV
SDOp/SDOn Outputs (CML to 1.2V)					
$\triangle V_o$	Output amplitude $V_{SDOp,n}$ (into 2x50Ω)	2x300	2x370	2x450	mV
V_{cmout}	Common-mode output voltage when AC coupled	—	0.83	—	V

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TABLE 3-2: ELECTRICAL CHARACTERISTICS (OVER THE OPERATING VCC AND -40 TO +85°C RANGE)

R_{output}	Termination on SDOp/SDOn to VCC	—	50	—	Ω
t_{rise_o}	Rise/Fall time 20% to 80% of $V_{SDOp,n}$	—	75	—	ps
Uplink Parameters					
V_{LF}	Uplink transmit amplitude for R_{amp} = 1 kΩ measured inside cable	110	150	190	mV
t_{rise_lf}	Rise/Fall time 20% to 80% of LF output on SDIp with R_{amp} = 1 kΩ	30	40	55	ns
V_{ih}	LFI input high voltage	0.8	—	1.3	V
V_{il}	LFI input low voltage	-0.5	—	0.4	V
R_{input}	Internal resistor to GND	—	3.6	—	kΩ

TABLE 3-3: JITTER NUMBERS(1)

Parameter	Conditions	Min.	Typ.	Max.	Units
Jitter in Equalizer Output	2.97 Gbps from 0-120m(2)	—	—	0.25	UI
Jitter in Equalizer Output	2.97 Gbps from 120-140m(2)	—	0.3	—	UI
Jitter in Equalizer Output	1.485 Gbps from 0-160m(2)	—	—	0.25	UI
Jitter in Equalizer Output	1.485 Gbps from 160-200m(2)	—	0.3	—	UI
Jitter in Equalizer Output	270 Mbps from 0-400m(2)	—	—	0.2	UI
Additive jitter on LF output	8B/10B coded signal at 5 Mbps over full VCC and temperature range.	—	—	10	ns
DCD in LF output	8B/10B coded signal at 5 Mbps over full VCC and temperature range.	—	—	10	ns

1: Jitter numbers (over operating VCC range at -40°C to +85°C and full $\triangle V_{TX}$ range with pathological patterns)

2: Measured with Belden 1694A

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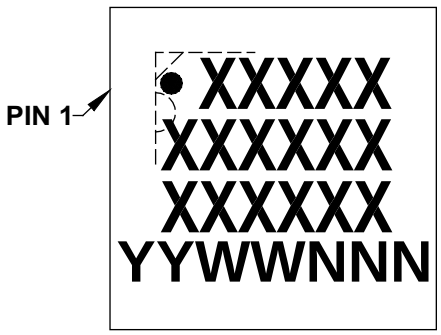
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4.0 PACKAGING INFORMATION

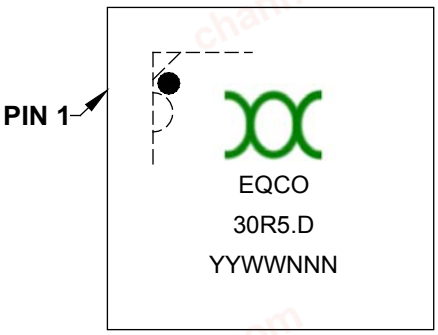
4.1 Package Marking Information

16-Lead Plastic Quad Flat, No Lead Package – 4x4x0.9 mm Body [QFN]

16-Lead QFN (4x4x0.9 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

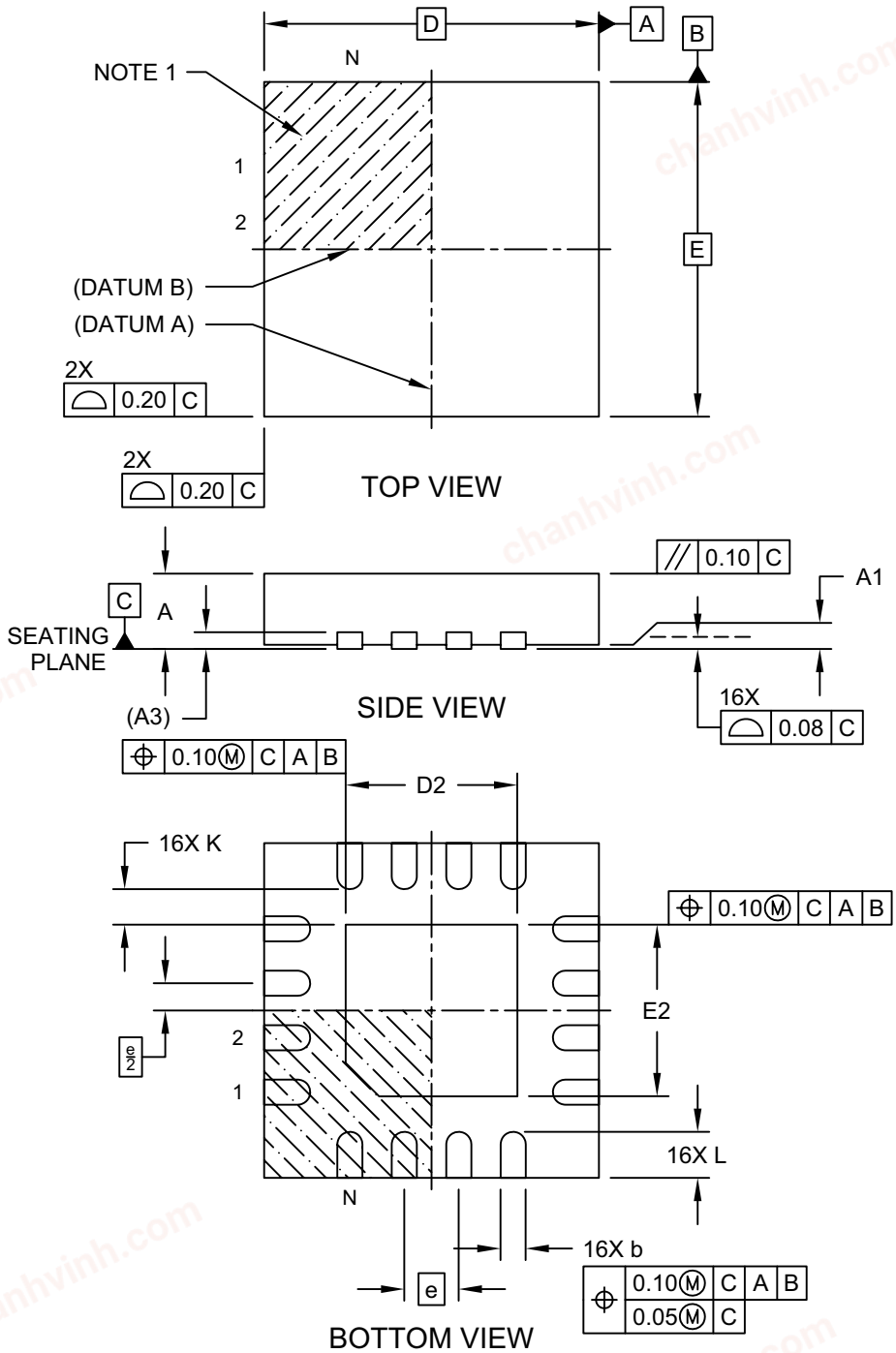
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



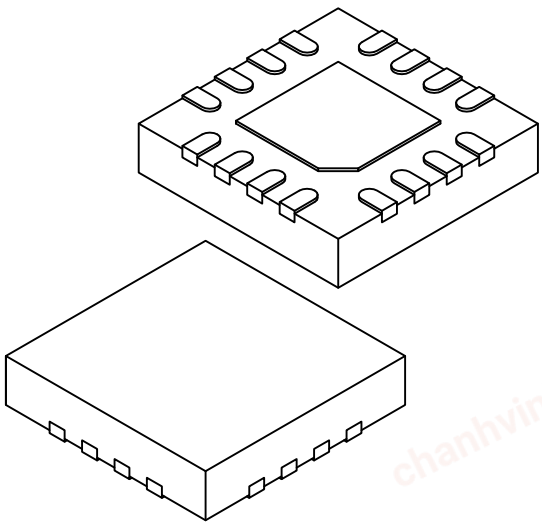
Microchip Technology Drawing C04-259A Sheet 1 of 2

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16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.85	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	1.95	2.05	2.15
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	1.95	2.05	2.15
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.45	0.55	0.65
Terminal-to-Exposed-Pad	K	0.20	—	—

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

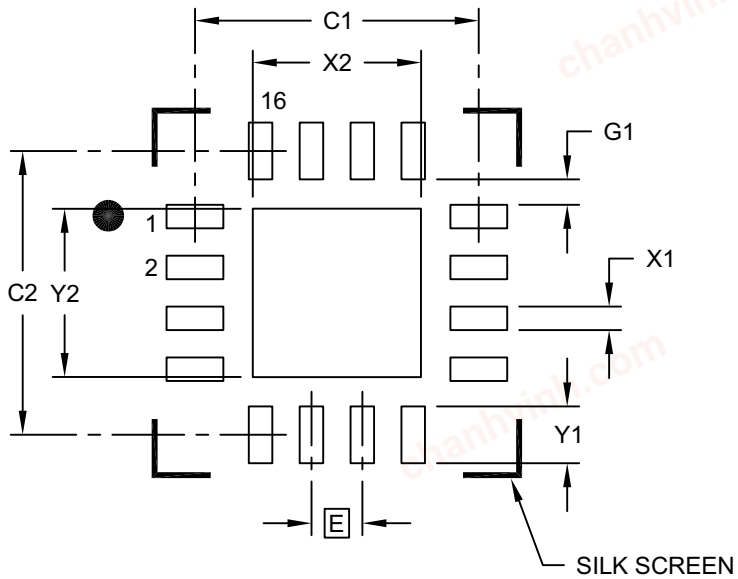
Microchip Technology Drawing C04-259A Sheet 2 of 2

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16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			2.15
Optional Center Pad Length	Y2			2.15
Contact Pad Spacing	C1		3.625	
Contact Pad Spacing	C2		3.625	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.725
Contact Pad to Center Pad (X16)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2259A

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APPENDIX A: REVISION HISTORY

Revision A (September 2014)

This is the initial release of the document in the Microchip format. This replaces EqcoLogic document version 1v0.

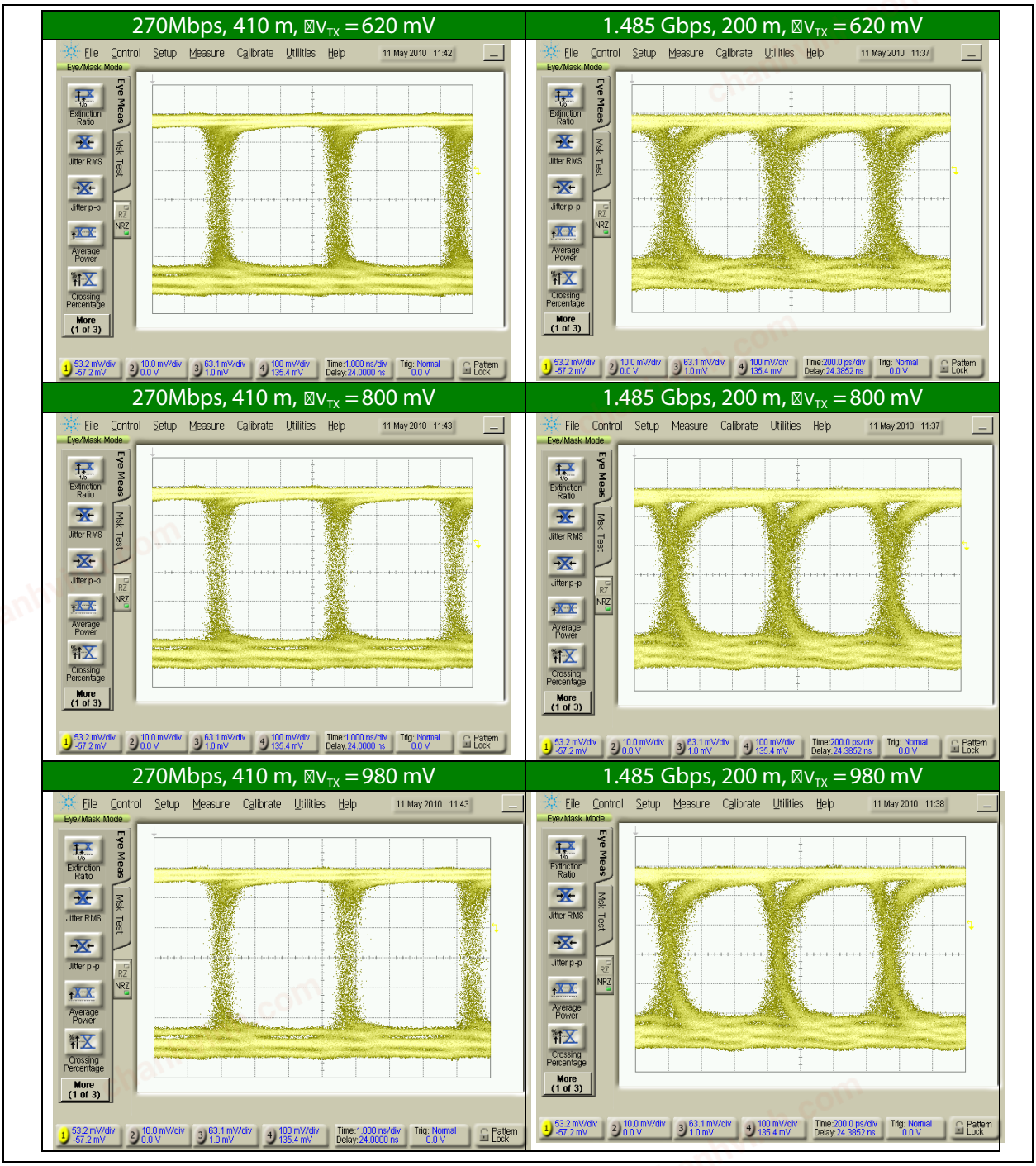
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APPENDIX B: TYPICAL EQUALIZER CHARACTERISTICS

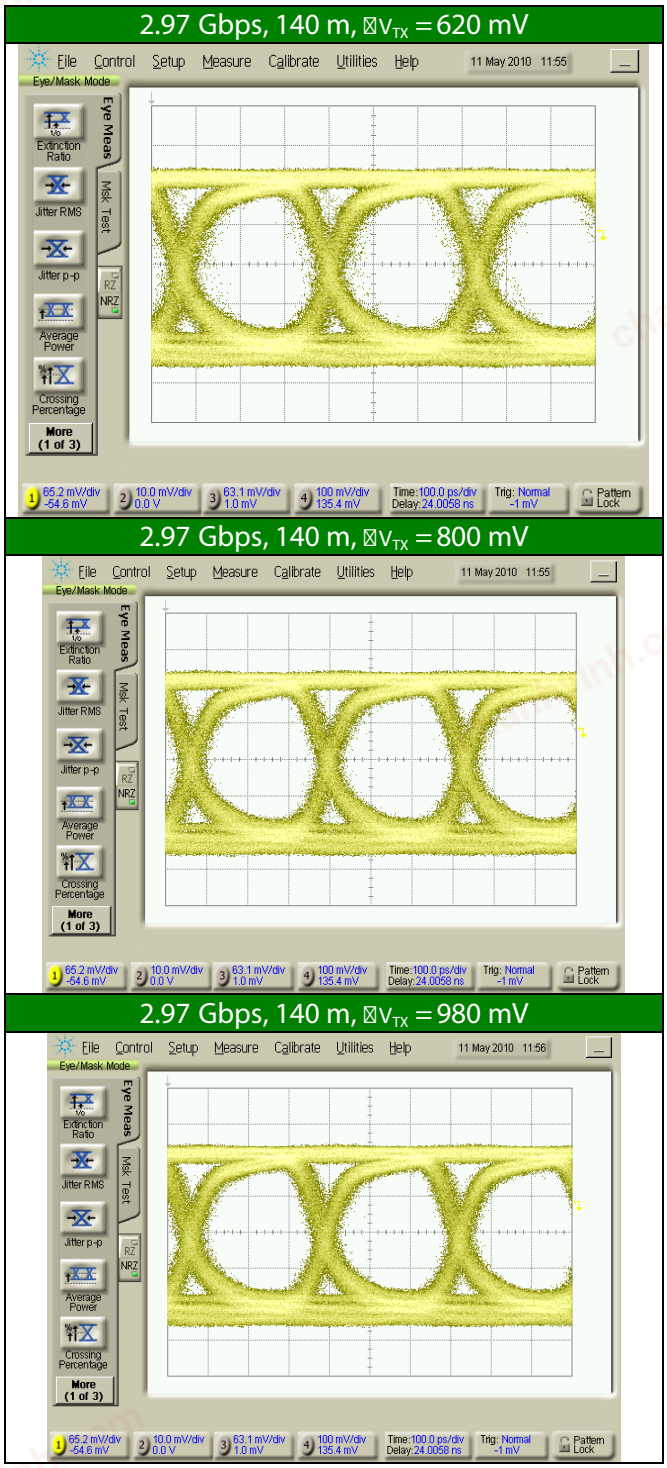
All measurements at VCC = 3.3V, Temp = +25ºC, data pattern = prbs15 (including 20 µs of each polarity of pathological pattern), measured with Belden 1694A cable.

FIGURE B-1: TYPICAL EQUALIZER PERFORMANCE AT ROOM TEMPERATURE FOR DIFFERENT SPEEDS



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FIGURE B-2: TYPICAL EQUALIZER PERFORMANCE AT ROOM TEMPERATURE AT 2.97 GBPS



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EQCO30R5.D

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To order parts, including industrial, or obtain information, for e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	I	RM	XXX
Device	Temp. Range	Radio Module	Firmware Revision Number

Device:	EQCO30R5.D	
Temperature Range:	I	= -40°C to +85°C (Industrial temperature)
Package:	TRAY	= Tray
	(Blank)	= Tube

Examples:

a) EQCO30R5.D = Industrial temperature, 16-Lead QFN Tube packaging

b) EQCO30R5.D-TRAY = Industrial temperature, 16-Lead QFN Tray packaging

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