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# dsPIC33CK64MC105

## dsPIC33CK64MC105 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CK64MC105 family devices that you have received conform functionally to the current Device Data Sheet (DS70005399**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CK64MC105 silicon.

| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**). |
|---|---|

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

| **Note:** | If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance. |
|---|---|

The DEVREV values for the various dsPIC33CK64MC105 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID(1) | Revision ID for Silicon Revision | | |
|---|---|---|---|---|
| | | A1 | A3 | A4 |
| dsPIC33CK32MC102 | 0x9900 | 0x0001 | 0x0003 | 0x0004 |
| dsPIC33CK32MC103 | 0x9901 | | | |
| dsPIC33CK32MC105 | 0x9902 | | | |
| dsPIC33CK64MC102 | 0x9910 | | | |
| dsPIC33CK64MC103 | 0x9911 | | | |
| dsPIC33CK64MC105 | 0x9912 | | | |

**Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

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**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item Number | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|---|
| | | | | A1 | A3 | A4 |
| CPU | `div.sd` Instruction | 1. | When using the signed 32-by-16-bit division instruction, `div.sd`, the Overflow bit is not set when an overflow occurs. | X | X | X |
| $I^2C$ | Interrupt | 2. | In Client mode, an incorrect interrupt is generated with DHEN = `1`. | X | X | X |
| $I^2C$ | Idle | 3. | SFRs are reset in Idle mode. | X | X | X |
| Oscillator | VCO Dividers | 4. | Main and auxiliary PLL external VCO dividers can fail to output the clock signal. | X | | |
| PWM | Time Base Capture | 5. | The PWM Capture Status (CAP) flag will not set again under certain conditions. | X | X | X |
| UART | Sleep | 6. | When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = `1`. | X | X | X |
| UART | IrDA® | 7. | IrDA is not functional. | X | X | X |
| Oscillator | POSC | 8. | POSCRDY sets early on the clock switch to POSC. | X | X | |


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## Silicon Errata Issues

| | |
|---|---|
| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**). |

### 1. Module: CPU

When using the Signed 32-by-16-Bit Division instruction, `div.sd`, the Overflow bit may not always get set when an overflow occurs. This erratum only affects operations in which at least one of the following conditions is true:

- Dividend and divisor differ in sign
- Dividend > 0x3FFFFFFF, or
- Dividend < 0xC0000000

**Work around**

The application software must perform both the following actions to handle possible undetected overflow conditions:

a) The value of the dividend must always be constrained to be in the following range: 0xC0000000 ≤ Dividend ≤ 0x3FFFFFFF.

b) If the dividend and divisor differ in sign (e.g., the dividend is negative and divisor is positive), then after executing the `div.sd` instruction or the compiler built-in function, `__builtin_divsd()`, inspect the sign of the resultant quotient. If the quotient is found to be a positive number, then treat it as an overflow condition.

**Affected Silicon Revisions**

| A1 | A3 | A4 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2. Module: I²C

In Client mode with DHEN = `1` (Data Hold Enable), if the software sends a NACK, a Client interrupt is asserted at the ninth falling edge of the clock.

**Work around**

Software should ignore the Client interrupt that is asserted after sending a NACK.

**Affected Silicon Revisions**

| A1 | A3 | A4 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 3. Module: I²C

In Client mode, the SFRs are reset when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL).

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | A4 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 4. Module: Oscillator

At PLL start-up, the main PLL VCO dividers may occasionally halt and not provide a clock output. The VCO dividers can be selected as clock sources for different peripheral modules, including the ADC, PWM, DAC, UART, etc. VCO divider outputs, FVCO/2, FVCO/3, FVCO/4 and FVCODIV, are affected.

**Work around**

1. Use another clock source, such as the FOSC or PLL Output (FPOLLO) instead of the VCO dividers.
2. If the application requires the VCO divider, test the clock source before using the peripheral in the end application. System resources, including a timer, I/O pin state or interrupts, can be used to detect and verify peripheral activity for presence of the VCO divider clock output. Any type of Reset may recover the VCO divider clock (Software Reset, WDT, MCLR or POR).

**Affected Silicon Revisions**

| A1 | A3 | A4 | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

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## 5. Module: PWM

When using a PWM Control Input (PCI) to trigger a time base capture, the Capture Status flag, CAP (PGxSTAT[5]), may not set again under certain conditions. When a subsequent PWM capture event occurs while, or just after, reading the current capture value from the PGxCAP register, the Capture Status Flag, CAP, will not set again.

**Work around**

Read the PWM Generator Capture (PGxCAP) register at a known time to avoid the condition. The timing of the PGxCAP read operation can be scheduled by using PWM Generator x interrupt or any of the PWM event interrupts corresponding to the PCI event that triggered the time base capture. Read the PGxCAP value after the CAP bit has set within the interrupt.

**Affected Silicon Revisions**

| A1 | A3 | A4 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 6. Module: UART

When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.

**Work around**

Set the SPLEN bit in addition to WAKE before entering Sleep.

**Affected Silicon Revisions**

| A1 | A3 | A4 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 7. Module: UART

The IrDA module is not functional.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | A4 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 8. Module: Oscillator

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

**Work around**

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral, such as REFO.
2. Provide a delay to stabilize the POSC.
3. Then, switch to the POSC source.

**Affected Silicon Revisions**

| A1 | A3 | A4 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |


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## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005399**D**):

| | |
|---|---|
| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |

None.

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## APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (8/2020)

Initial version of this document; issued for revision A1.

Rev B Document (9/2022)

Updated version issued for silicon revision A3.

Rev C Document (6/2026)

Updated version issued for silicon revision A4.


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