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DSA12X2/3/4

High Performance Differential MEMS Oscillators for Automotive

Features

- Automotive AEC-Q100 Qualified
- Any Frequency between 2.5 MHz and 450 MHz
- Supports LVPECL, LVDS, or HCSL Differential Outputs
- Very Low RMS Phase Jitter: <650 fs (typ.)
- PCIe Gen1-7 Compliant Output
- High Stability: ±20 ppm, ±25 ppm, ±50 ppm
- Wide Temperature Range:
  - Automotive Grade 1: –40°C to +125°C (DSA12x3 LVDS Output Only)
  - Automotive Grade 2: –40°C to +105°C
  - Automotive Grade 3: –40°C to +85°C
- Small Industry-Standard Footprints
  - 6-Lead 2.5 mm × 2.0 mm VDFN
  - 6-Lead 3.2 mm × 2.5 mm VDFN
  - 6-Lead 3.2 mm × 5.0 mm VDFN
  - 6-Lead 7.0 mm × 5.0 mm VDFN
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTF than Quartz Oscillators
- Supply Range of 2.25V to 3.63V
- Standby, Frequency Select, and Output Enable Functions
- Lead-Free and RoHS-Compliant

Applications

- Automotive Infotainment
- Automotive ADAS
- In-Vehicle Networking, CAN Bus, Ethernet
- PCI Express Gen 1/2/3/4/5/6/7

General Description

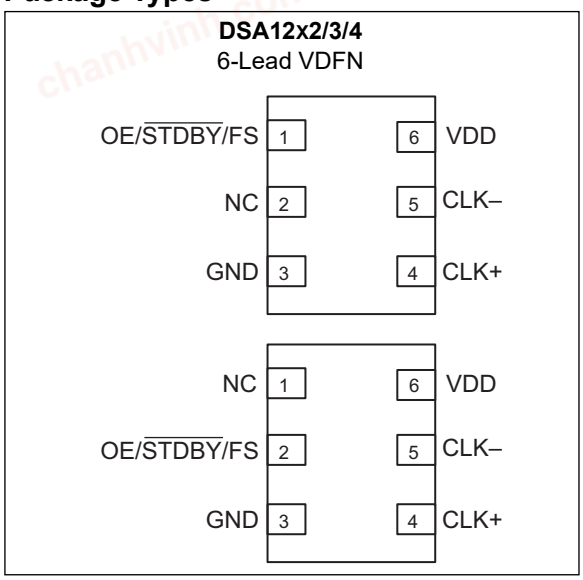
The DSA12x2/3/4 family of high performance oscillators utilizes the latest generation of silicon MEMS technology that reduces close-in noise and provides excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MES oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for automotive applications.

The DSA12x2/3/4 family features a control function on pin 1 or pin 2 that permits either a standby feature (complete power down when $\overline{\text{STDBY}}$ is low), output enable (output is tri-stated with OE low), or a frequency select (choice of two frequencies selected by FS high/low). See the Product Identification System section for detailed information.

All oscillators are available in industry-standard packages, including the small 2.5 mm x 2.0 mm, and are “drop-in” replacements for standard 6-pin LVPECL/LVDS/HCSL crystal oscillators.

Package Types

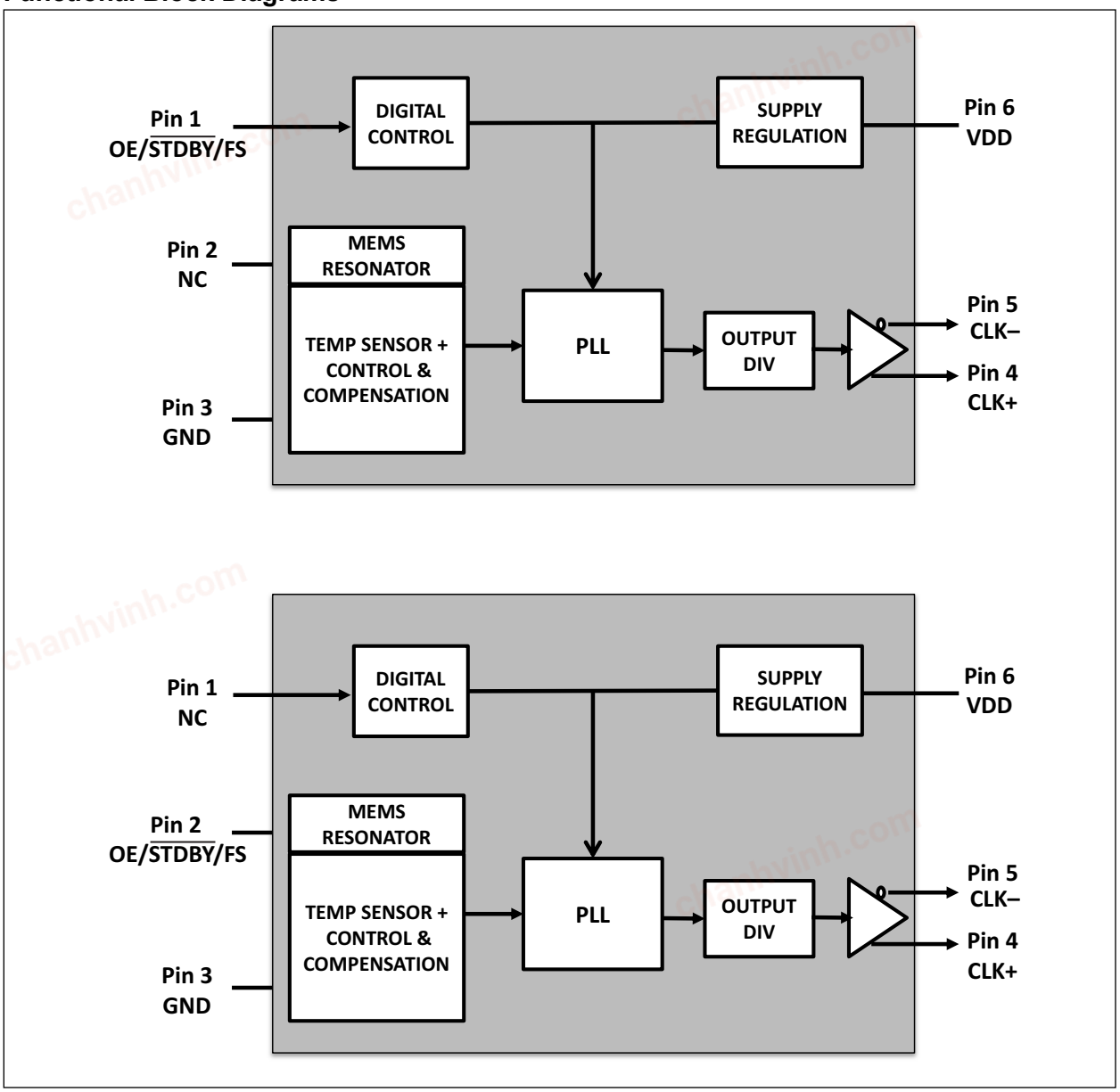
DSA12x2/3/4
6-Lead VDFN



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Functional Block Diagrams



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... –0.3V to +4.0V
Input Voltage ..... –0.3V to V_{DD} + 0.3V
ESD Protection (HBM) ..... 4 kV
ESD Protection (MM) 400V
ESD Protection (CDM) ..... 1.5 kV

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 2.5V ±10% or 3.3V±10%; T_A = –40°C to +105°C, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.25	—	3.63	V	Note 1
Supply Current	I_{DD}	—	50	—	mA	LVPECL, f_{OUT} = 100 MHz
		—	32	—		LVDS, f_{OUT} = 100 MHz
		—	40	—		HCSL, f_{OUT} = 100 MHz
		—	23	—		Output disabled (tri-state), f_{OUT} = 100 MHz
Standby Current	$I_{STDBY_}$	—	2.5	5	µA	Input pin = $\overline{\text{STDBY}}$ = Asserted (V_{DD} = 3.3V)
Frequency Stability	Δf	—	—	±20	ppm	Includes frequency variations due to initial tolerance, temp., and power supply voltage
		—	—	±25		
		—	—	±50		
Aging	Δf	—	—	±5	ppm	First year @ 25°C
		—	—	±1		Per year after first year
Startup Time	t_{SU}	—	5.5	6	ms	From 90% V_{DD} to valid clock output, T = +25°C, Note 2
Input Logic Levels	V_{IH}	0.75 x V_{DD}	—	—	V	Input logic high
	V_{IL}	—	—	0.25 x V_{DD}		Input logic low
Output Disable Time	t_{DA}	—	—	25	ns	Note 3
Output Enable Time	t_{EN}	—	—	6	ms	$\overline{\text{STDBY}}$
		—	—	350	ns	OE
Enable Pull-Up Resistor	—	—	1.5	—	MΩ	Pull-up resistor on pin 1, Note 4
LVPECL (DSA12x2)						
Frequency	f_0	2.5	—	450	MHz	—
Output Logic Levels	V_{OH}	V_{DD} – 1.145	—	—	V	R_L = 50Ω
	V_{OL}	—	—	V_{DD} – 1.695		
Peak-to-Peak Output Swing	V_{PP}	—	800	—	mV	Single-Ended
Output Transition Time	t_R	—	200	250	ps	20% to 80%, R_L = 50Ω
	t_F	—	250	300		

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = 2.5V ±10% or 3.3V±10%; T_A = –40°C to +105°C, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter RMS	J_{PER}	—	2.0	—	ps	f_0 = 156.25 MHz, 10k cycles
Period Jitter Peak-to-Peak	J_{PTP}	—	20	—	ps	f_0 = 156.25 MHz, 10k cycles
Integrated Phase Noise (Random)	J_{PH}	—	0.65	—	ps_{RMS}	12 kHz to 20 MHz @156.25 MHz
LVDS Integrated Phase Noise (DSA12x3)						
Frequency	f0	2.3	—	450	MHz	—
Output Offset Voltage	V_{OS}	1.15	1.25	1.35	V	R = 100Ω Differential
Peak-to-Peak Output Swing	V_{PP}	250	350	450	mV	Single-Ended
Output Transition Time	t_R	120	170	220	ps	20% to 80%, R_L = 100Ω
	t_F					
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter RMS	J_{PER}	—	2.5	—	ps	f_0 = 156.25 MHz, 10k cycles
Period Jitter Peak-to-Peak	J_{PTP}	—	20	—	ps	f_0 = 156.25 MHz, 10k cycles
Period Jitter RMS	J_{PER}	—	3	—	ps	f_0 = 156.25 MHz, T_A = –40°C to +125°C
Period Jitter Peak-to-Peak	J_{PTP}	—	25	—	ps	f_0 = 156.25 MHz, T_A = –40°C to +125°C
Integrated Phase Noise (Random)	J_{PH}	—	0.65	—	ps_{RMS}	12 kHz to 20 MHz @156.25 MHz T_A = –40°C to +105°C
		—	0.9	—		2 kHz to 20 MHz @156.25 MHz TA = –40°C to +125°C
Phase Jitter	J_{RMS-CC}	—	0.025	0.1	ps_{RMS}	PCIe Gen 6.0, 64 GT/s
HCSL (DSA12x4)						
Frequency	f_0	2.3	—	450	MHz	—
Output Logic Levels	V_{OH}	0.64	—	—	V	R_L = 50Ω
	V_{OL}	—	—	0.1		
Peak-to-Peak Output Swing	V_{PP}	—	750	—	mV	Single-Ended
Output Transition Time	t_R	200	260	400	ps	20% to 80%, R_L = 50Ω
	t_F	250	370	500		
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter RMS	J_{PER}	—	2	—	ps	f_0 = 100.00 MHz, 10k cycles
Period Jitter Peak-to-Peak	J_{PTP}	—	16	—	ps	f_0 = 100.00 MHz, 10k cycles
Integrated Phase Noise (Random)	J_{PH}	—	0.617	—	ps_{RMS}	12 kHz to 20 MHz @100 MHz
		—	0.460	—		100 kHz to 20 MHz @100 MHz
		—	0.212	—		1.875 MHz to 20 MHz @100 MHz

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = 2.5V ±10% or 3.3V±10%; T_A = –40°C to +105°C, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Phase Jitter	T_J	—	23	86	ps_{PP}	PCIe Gen 1.1, $T_J = D_J + 14.069 \times R_J$ (BER 10^{-12}), Note 5
	$J_{RMS-CCHF}$	—	2.230	3.1	ps_{RMS}	PCIe Gen 2.1, 1.5 MHz to Nyquist, Note 5
	$J_{RMS-CCLF}$	—	0.08	3.0	ps_{RMS}	PCIe Gen 2.1, 10 kHz to1.5 MHz, Note 5
	J_{RMS-CC}	—	0.107	1.0	ps_{RMS}	PCIe Gen 3.0, Note 5
		—	0.107	0.30		PCIe Gen 4.0, 16 GT/s
		—	0.043	0.12		PCIe Gen 5.0, 32 GT/s
		—	0.054	0.1		PCIe Gen 6.0, 64 GT/s
		—	0.038	0.067		PCIe Gen 7.0, 128 GT/s

Note 1: V_{DD} pin should be filtered with a 0.1 µF capacitor.

2: t_{SU} is the time to 100 ppm stable output frequency after V_{DD} is applied and outputs are enabled.

3: t_{DA}: See the Output Waveform and the Test Circuits sections for more information.

4: Output is enabled if pad is floated (not connected).

5: Jitter limits established by Gen1.1, Gen 2.1, and Gen 3.0 PCIe standards.

TEMPERATURE SPECIFICATIONS Note 1

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–55	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 40s

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: DSA120X/1X/2X PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	OE/$\overline{\text{STDBY}}$/FS	Control pin: Output enable/standby/frequency select. External 10 kΩ pull up recommended when not actively driven.
2	NC	No connect.
3	GND	Power supply ground.
4	CLK+	Clock output +.
5	CLK–	Clock output –.
6	VDD	Power supply.

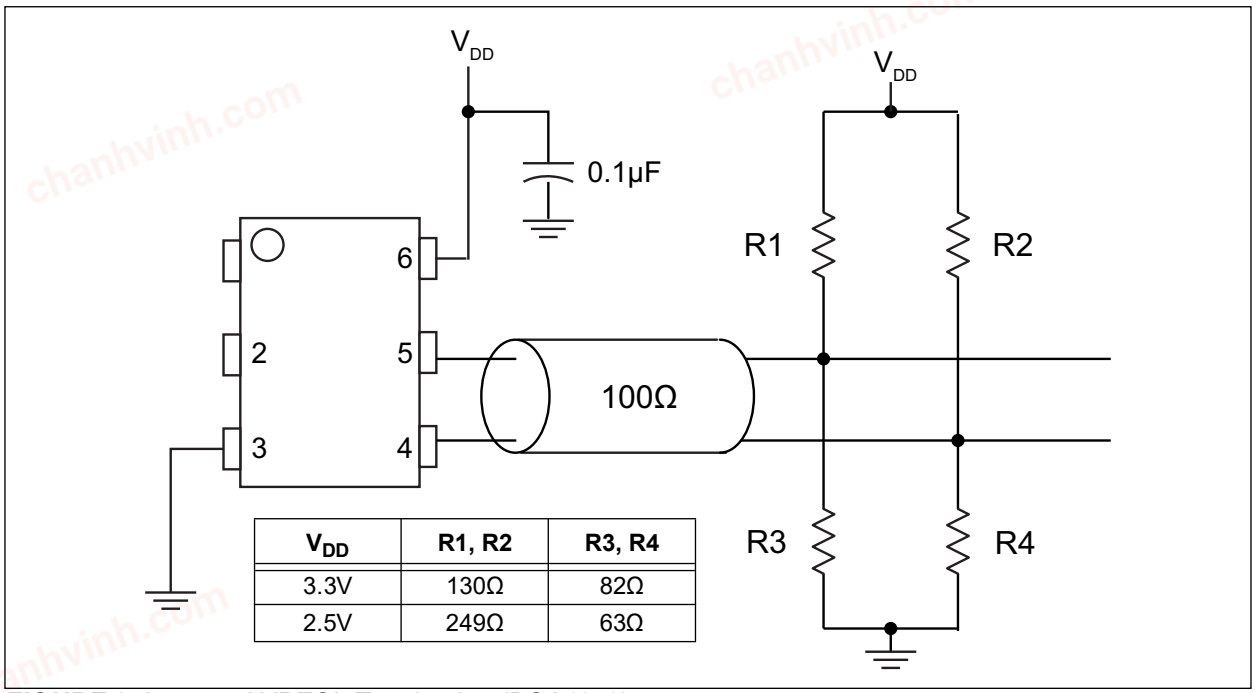
TABLE 2-2: DSA123X/4X/5X PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	NC	No connect.
2	OE/$\overline{\text{STDBY}}$/FS	Control pin: Output enable/standby/frequency select. External 10 kΩ pull up recommended when not actively driven.
3	GND	Power supply ground.
4	CLK+	Clock output +.
5	CLK–	Clock output –.
6	VDD	Power supply.

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3.0 TERMINATION SCHEME



V_{DD}	R1, R2	R3, R4
3.3V	130Ω	82Ω
2.5V	249Ω	63Ω

FIGURE 3-1: *LVPECL Termination (DSA12x2).*

In Figure 3-1, Thevenin termination for 3.3V operation. Values will differ for V_{DD} = 2.5V.

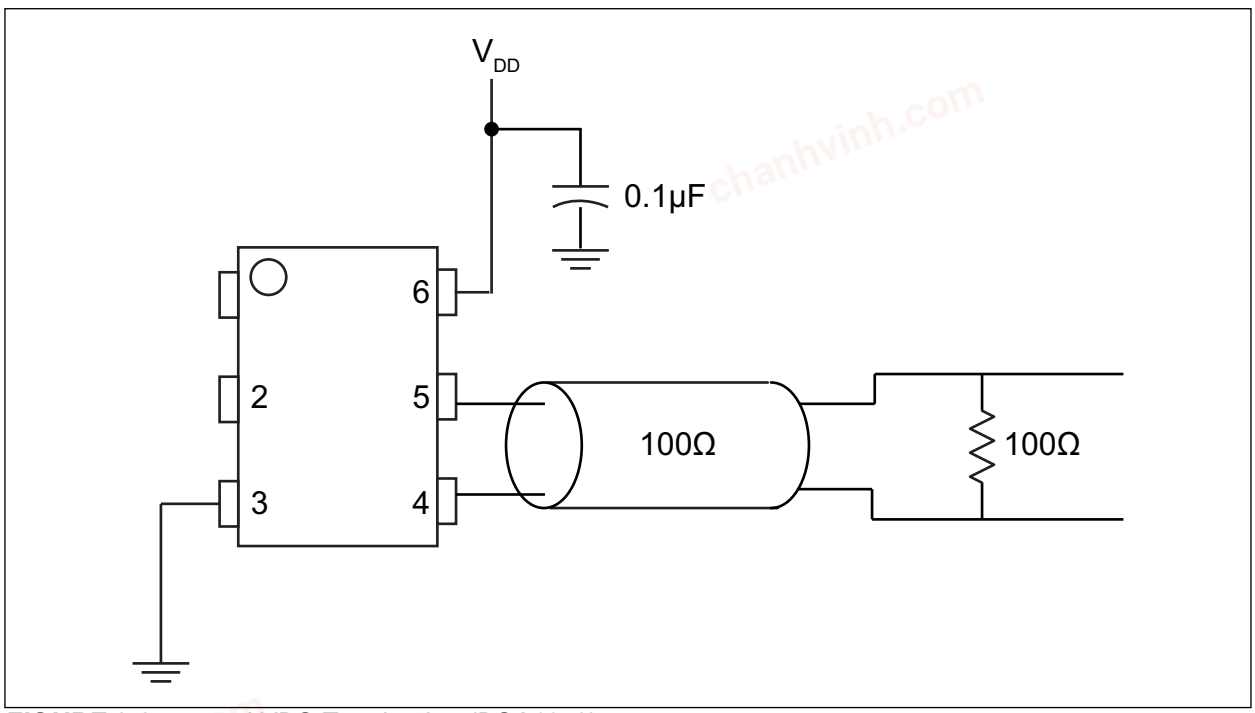


FIGURE 3-2: *LVDS Termination (DSA12x3).*

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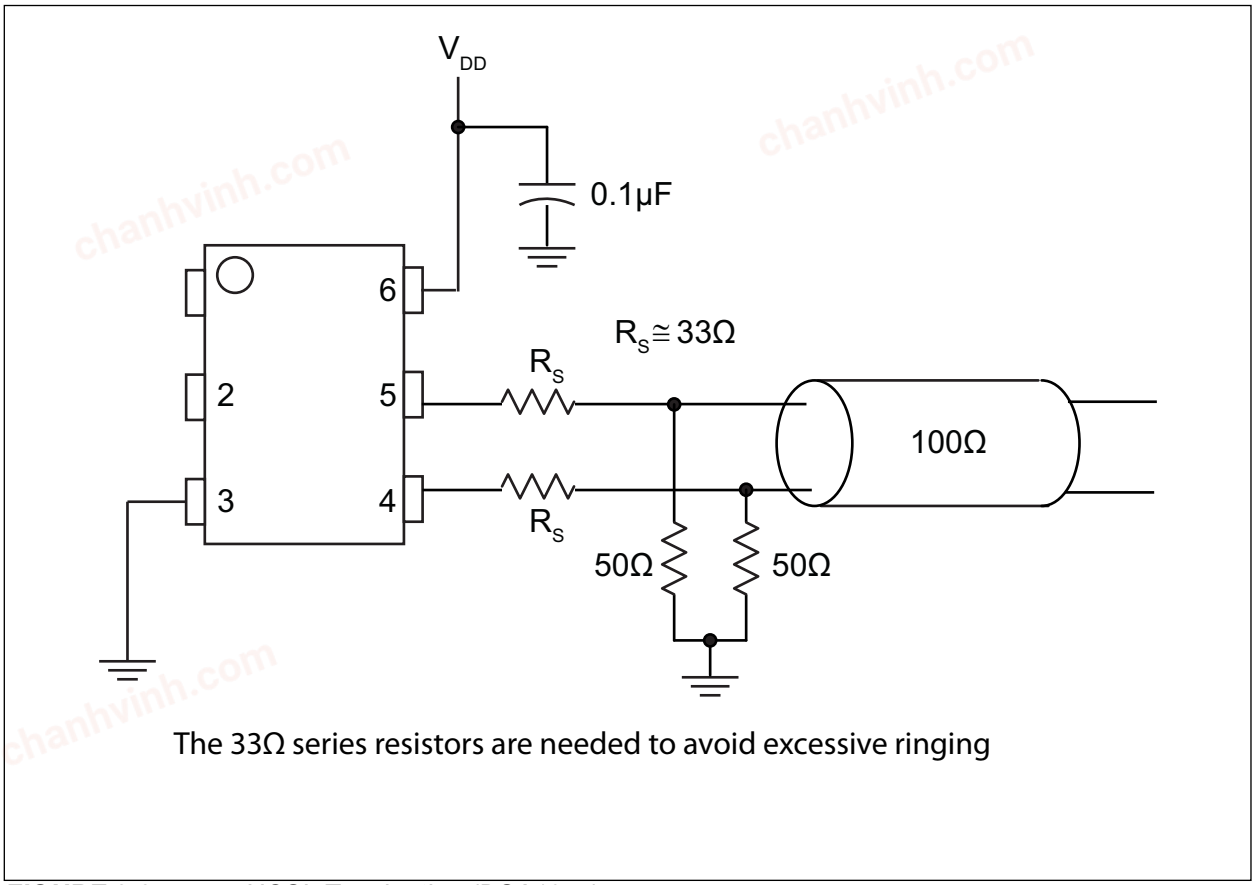


FIGURE 3-3: *HCSL Termination (DSA12x4).*

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4.0 OUTPUT WAVEFORM

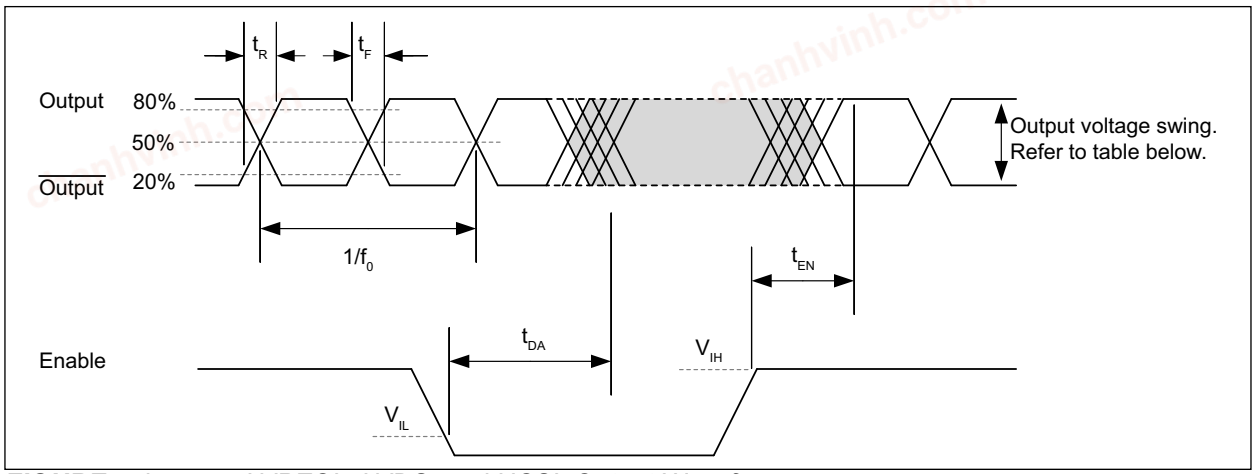


FIGURE 4-1: *LVPECL, LVDS, and HCSL Output Waveform.*

TABLE 4-1: OUTPUT VOLTAGE SWING BY LOGIC TYPE

Output Logic Protocol	Typical Peak-to-Peak Output Swing
LVPECL	830 mV
LVDS	350 mV
HCSL	675 mV

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5.0 TEST CIRCUITS

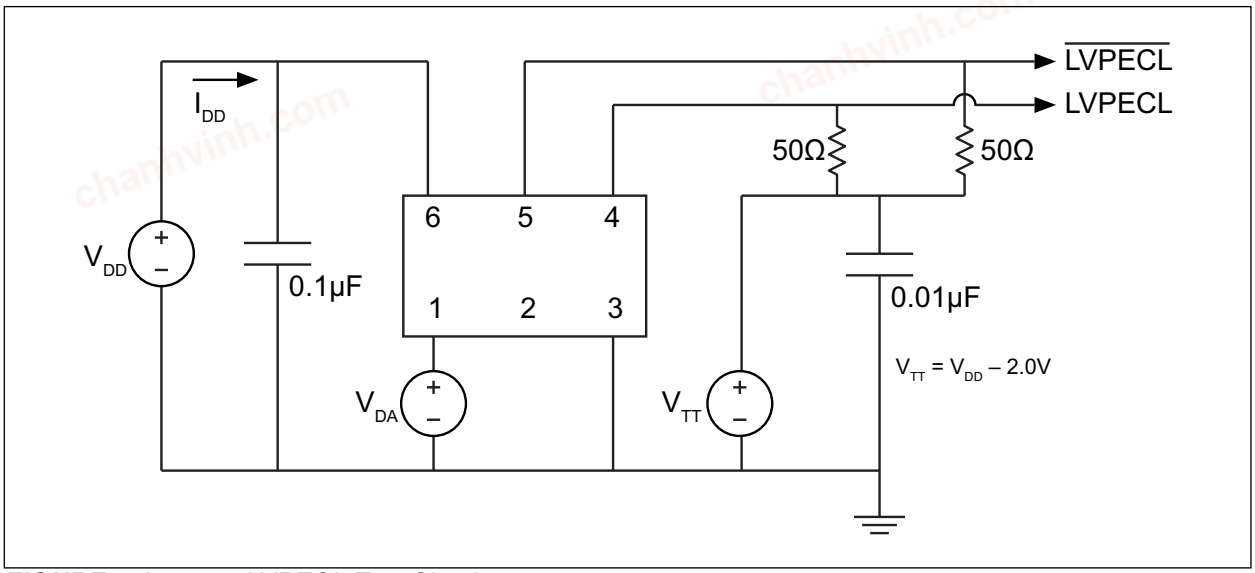


FIGURE 5-1: *LVPECL Test Circuit.*

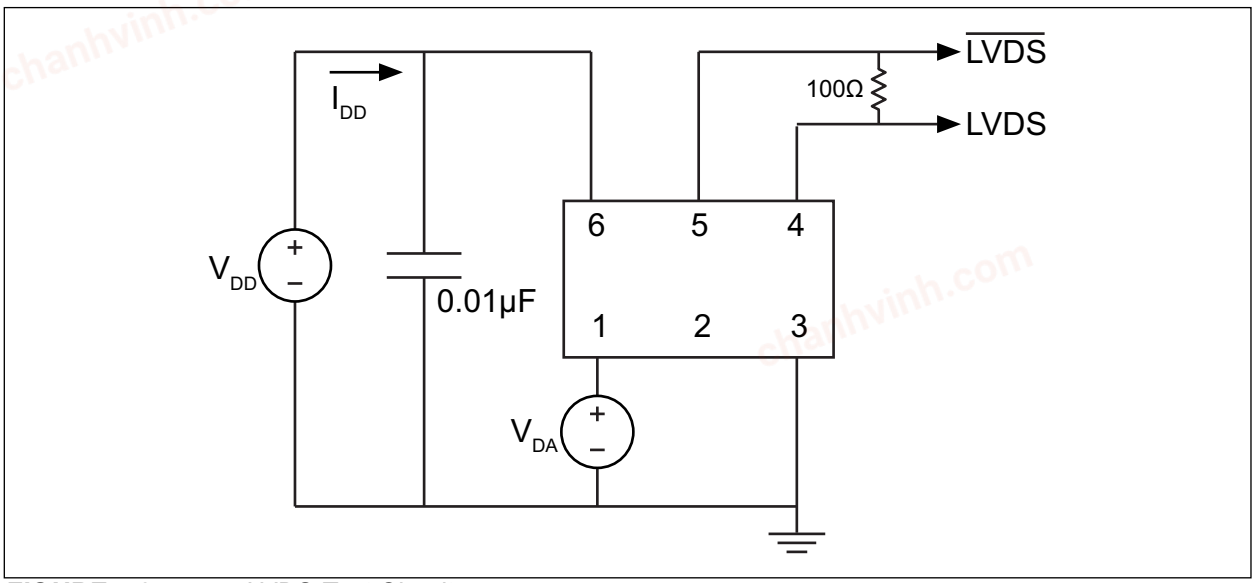


FIGURE 5-2: *LVDS Test Circuit.*

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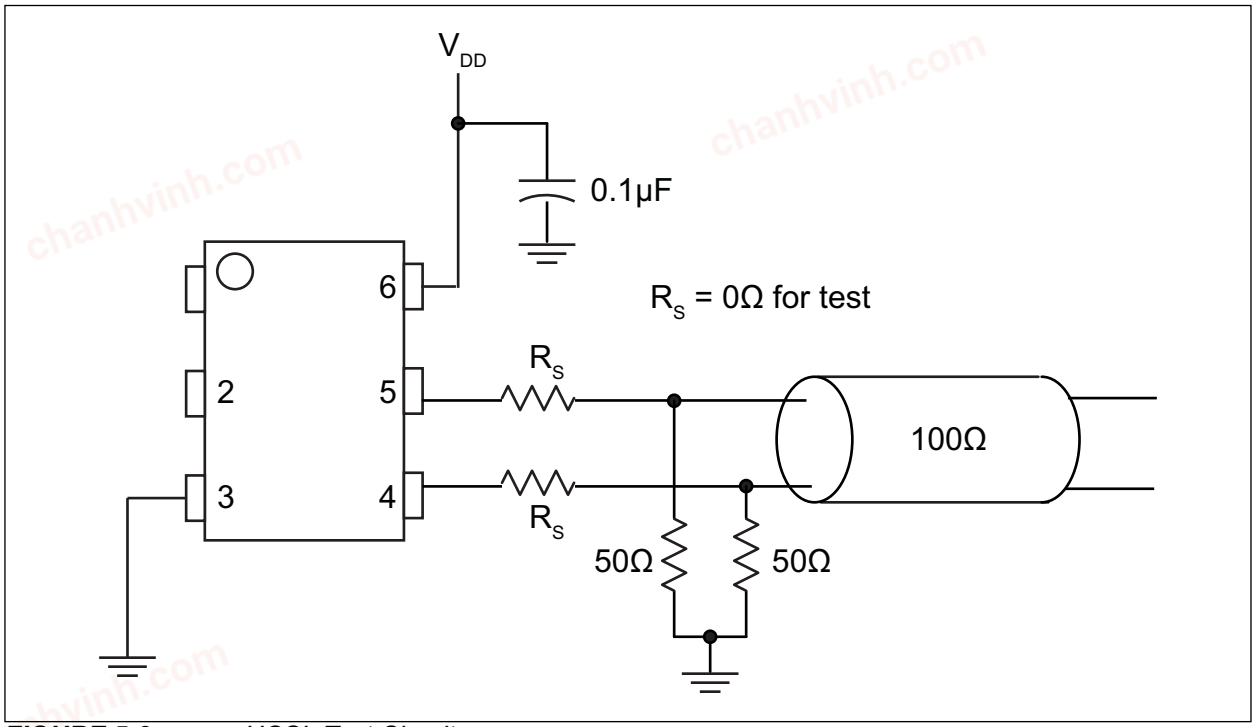


FIGURE 5-3: *HCSL Test Circuit.*

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6.0 SOLDER REFLOW PROFILE

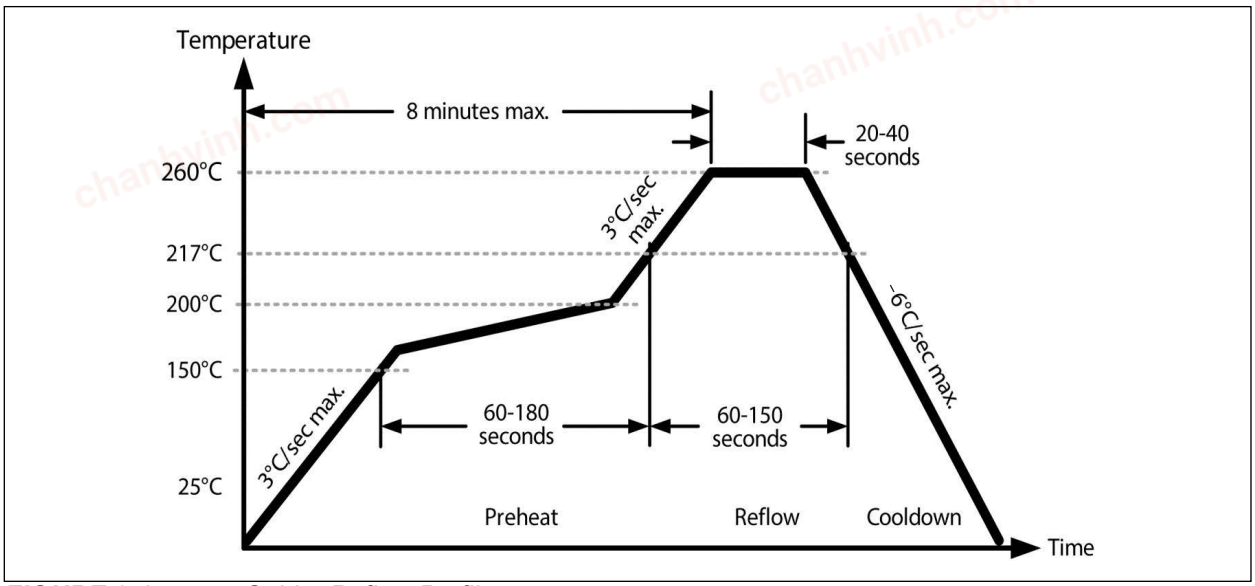


FIGURE 6-1: *Solder Reflow Profile.*

TABLE 6-1: SOLDER REFLOW

MSL 1 @ 260°C Refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp.)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time Maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	–6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

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7.0 BOARD LAYOUT (RECOMMENDED)

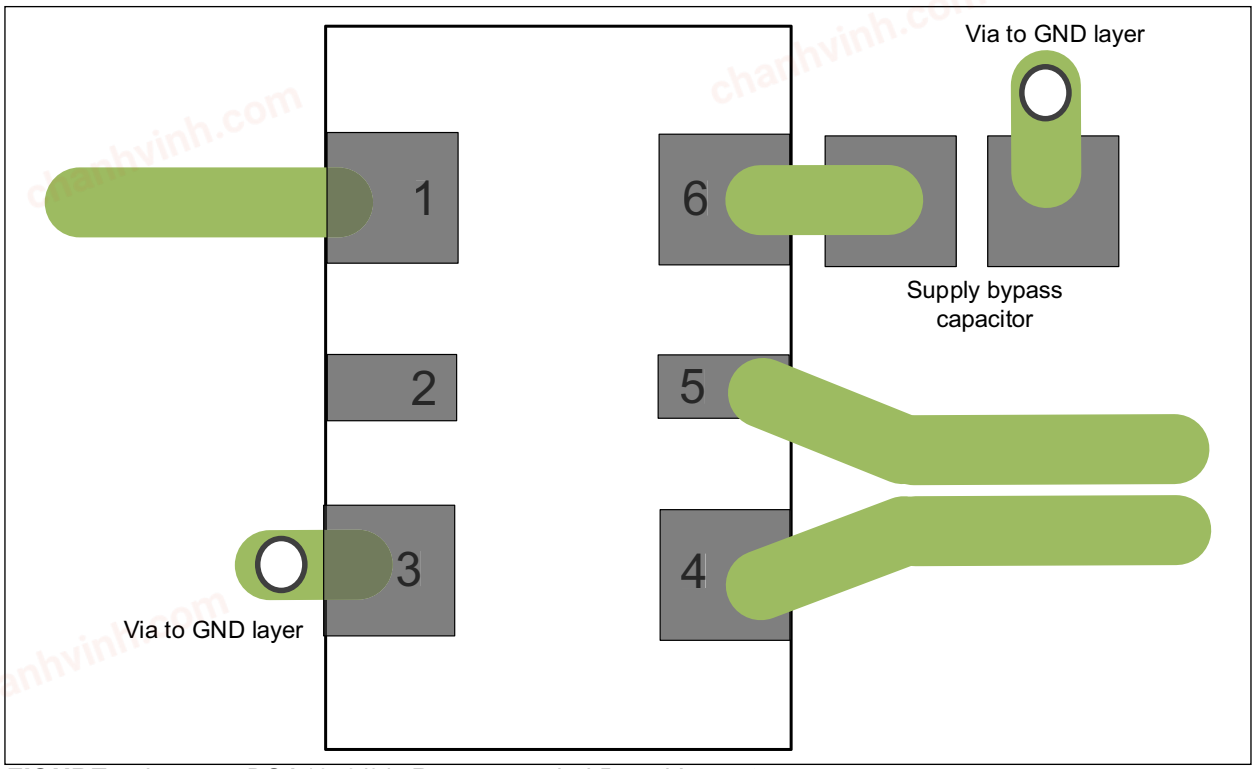


FIGURE 7-1: *DSA12x2/3/4 Recommended Board Layout.*

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8.0 PHASE NOISE

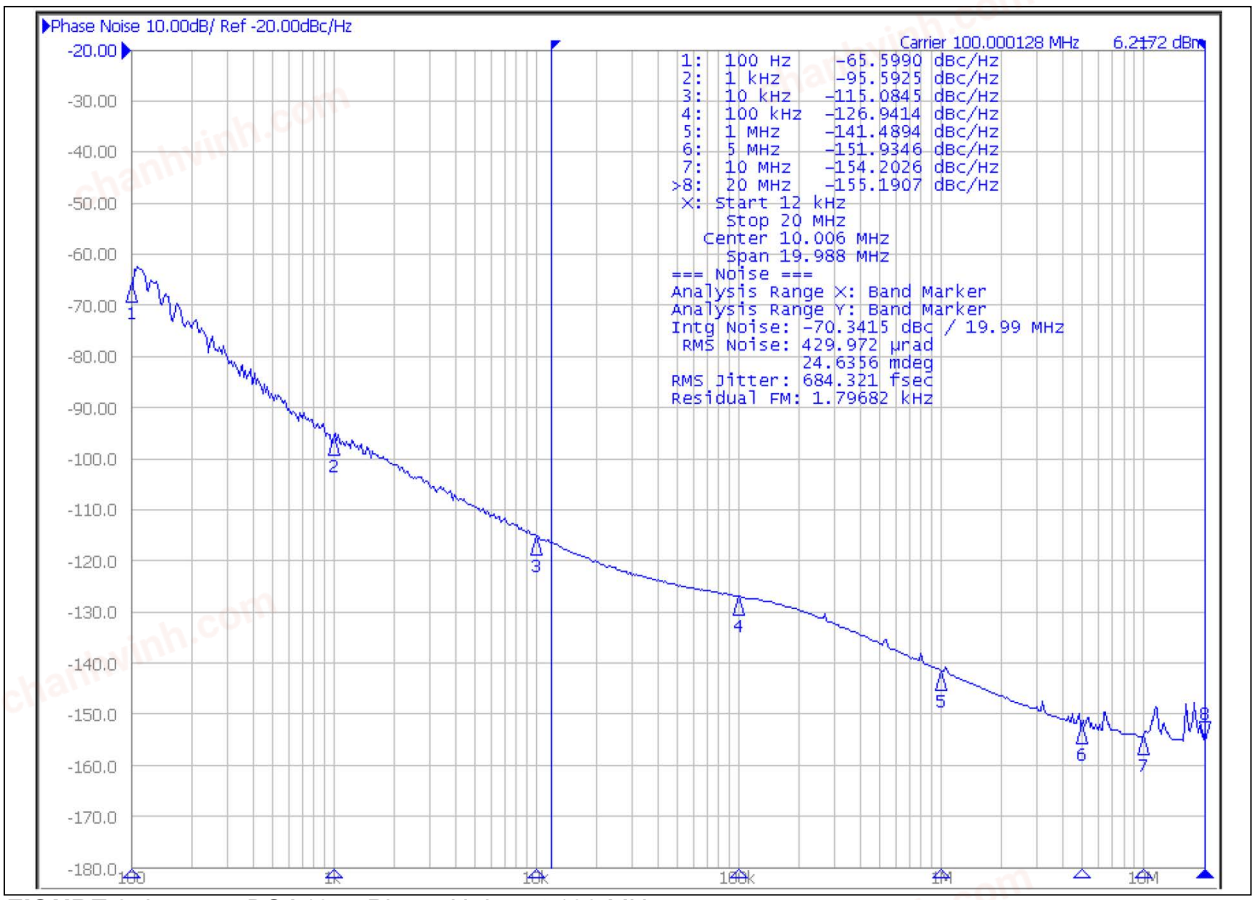


FIGURE 8-1: *DSA12x4 Phase Noise at 100 MHz.*

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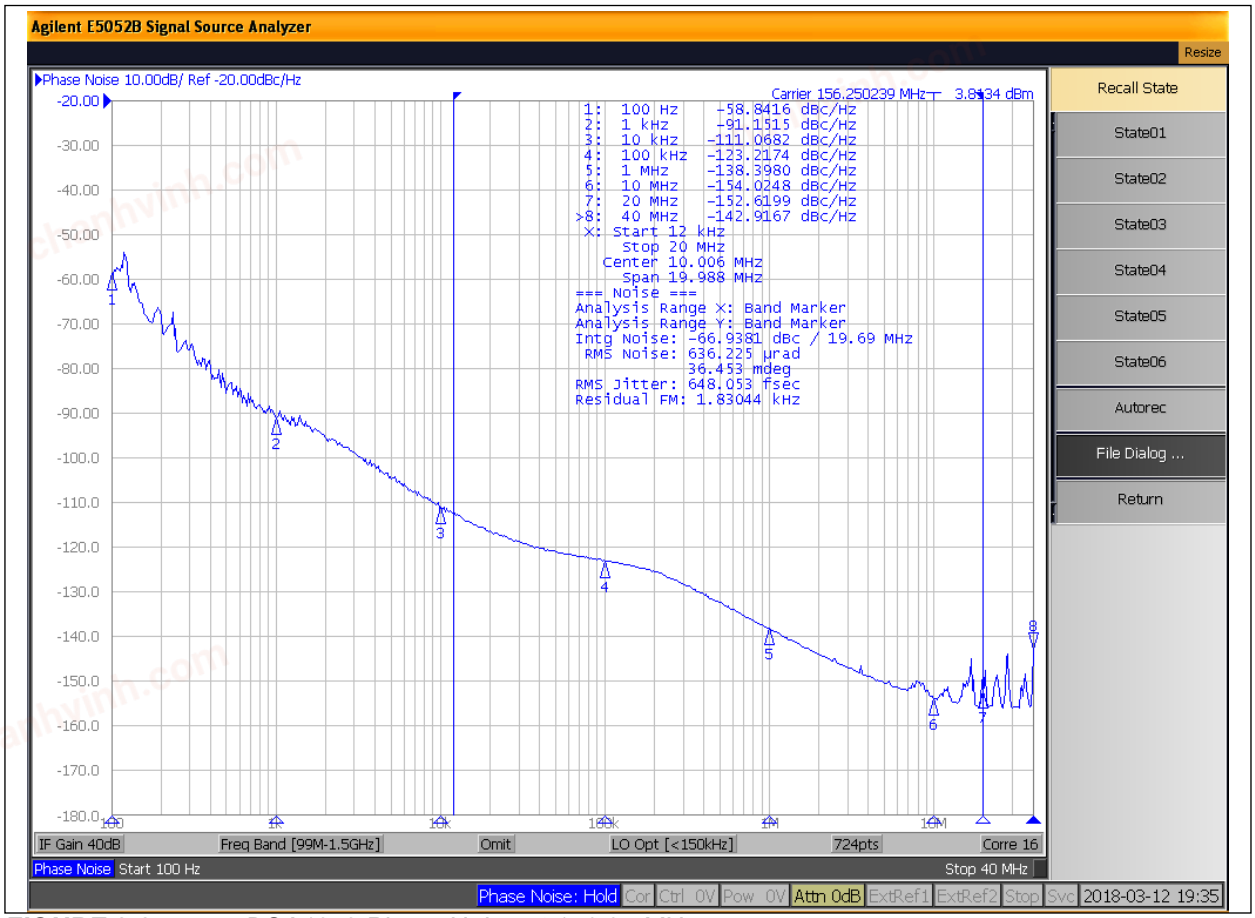


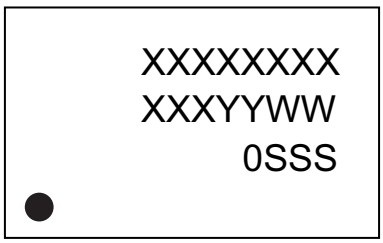
FIGURE 8-2: *DSA12x2 Phase Noise at 156.25 MHz.*

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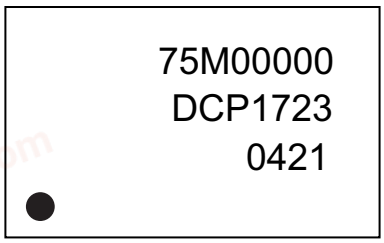
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

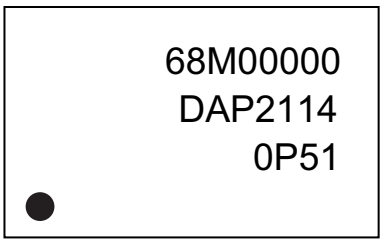
6-Lead VDFN*



Example 1*



Example 2*



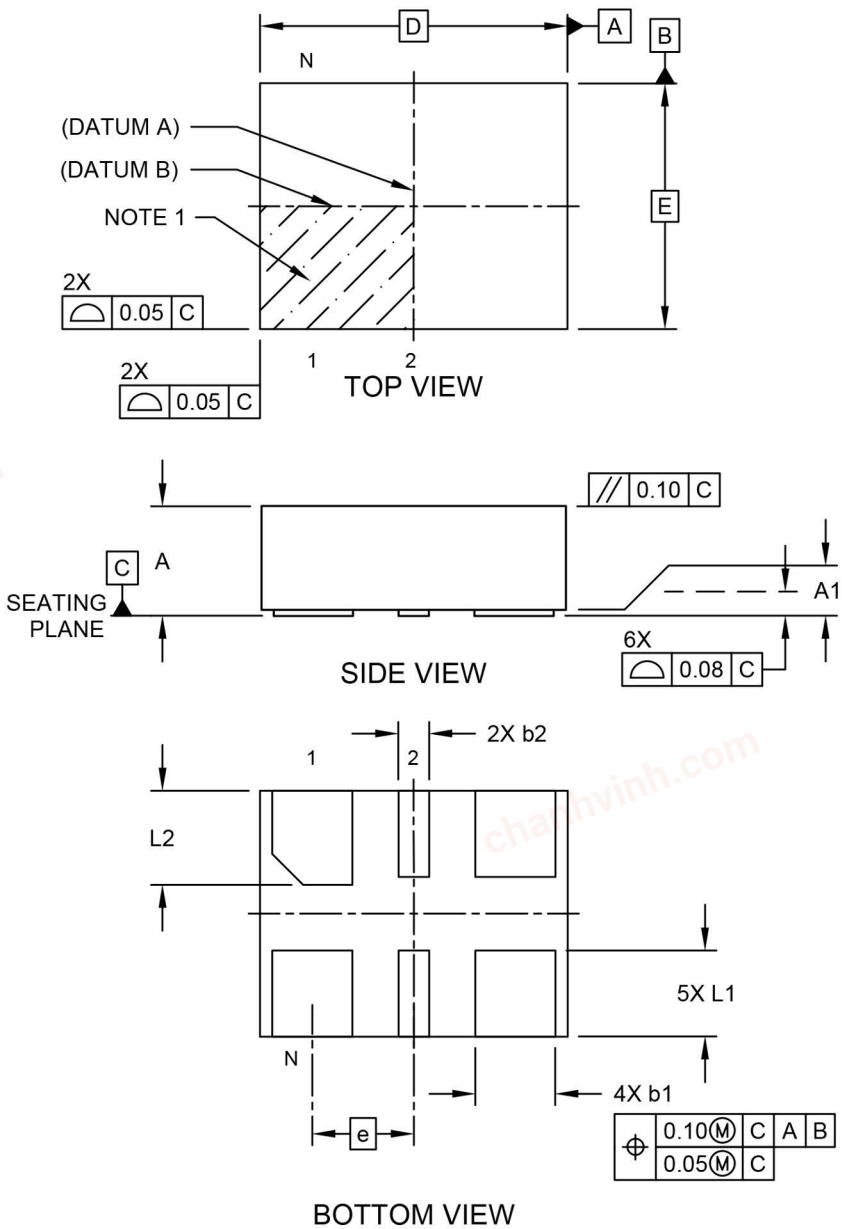
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	SSS	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
		Underbar (_) and/or Overbar (¯) symbol may not be to scale.

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6-Lead 2.5 mm × 2.0 mm VDFN (J7A) Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



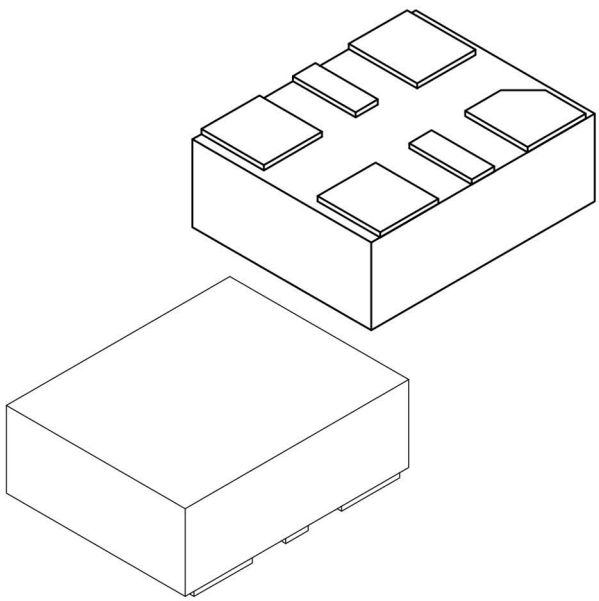
Microchip Technology Drawing C04-1005-J7A Rev E Sheet 1 of 2

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6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.825 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		2.50 BSC	
Overall Width	E		2.00 BSC	
Terminal Width	b1	0.60	0.65	0.70
Terminal Width	b2	0.20	0.25	0.30
Terminal Length	L1	0.60	0.70	0.80
Terminal Length	L2	0.665	0.765	0.865

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1005-J7A Rev E Sheet 2 of 2

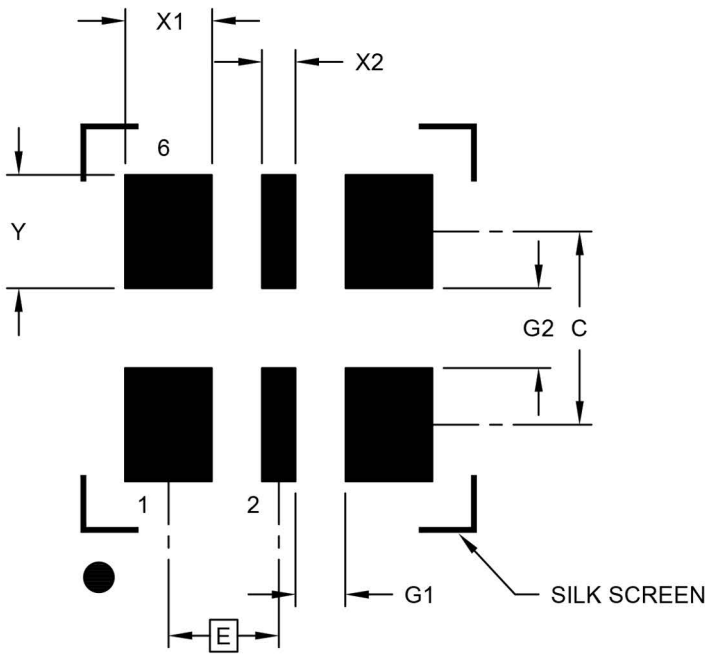
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6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.825 BSC	
Contact Pad Width (X4)	X1			0.65
Contact Pad Width (X2)	X2			0.25
Contact Pad Length (X6)	Y			0.85
Contact Pad Spacing	C		1.45	
Space Between Contacts (X4)	G1	0.38		
Space Between Contacts (X3)	G2	0.60		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

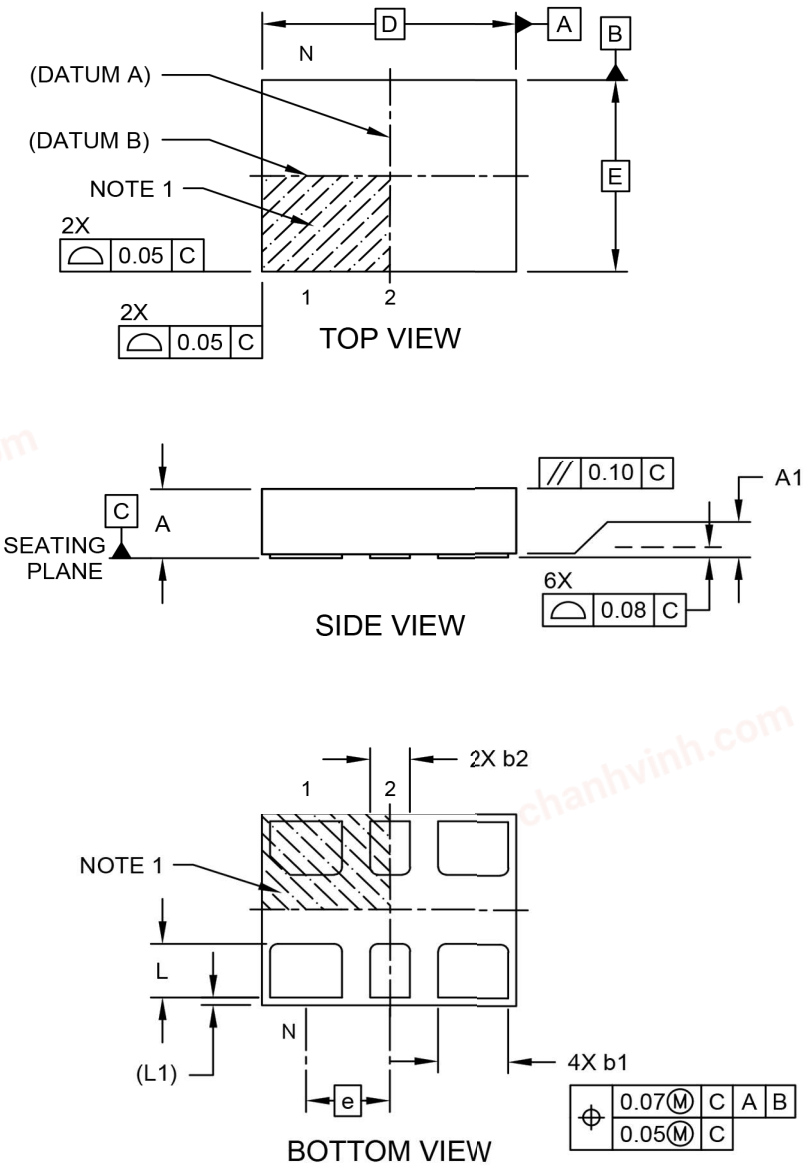
Microchip Technology Drawing C04-3005-J7A Rev E

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6-Lead 3.2 mm × 2.5 mm VDFN (H5A) Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1007-H5A Rev C Sheet 1 of 2

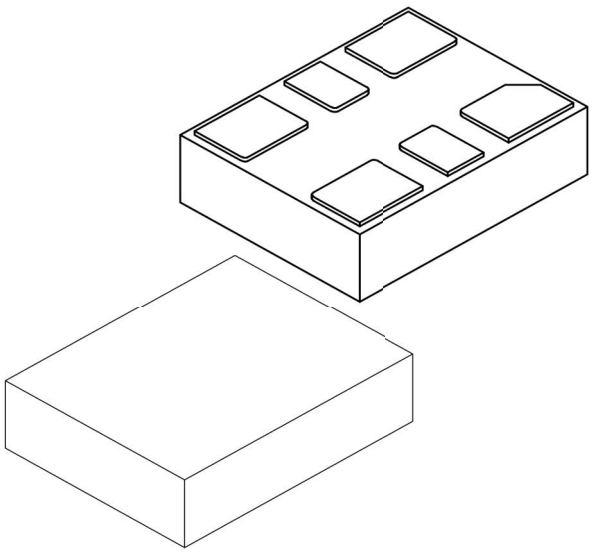
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6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		1.05 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		3.20 BSC	
Overall Width	E		2.50 BSC	
Terminal Width	b1	0.85	0.90	0.95
Terminal Width	b2	0.45	0.50	0.55
Terminal Length	L	0.65	0.70	0.75
Terminal Pullback	L1		0.10 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

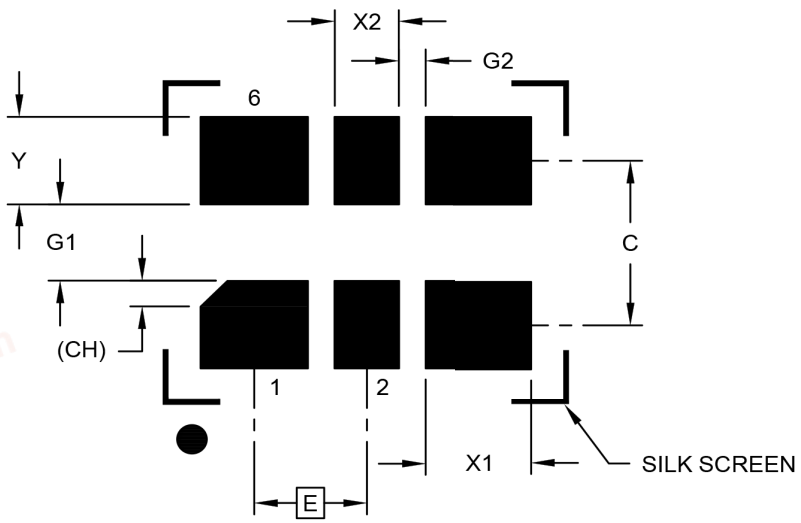
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6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.05 BSC	
Contact Pad Spacing	C		1.60	
Contact Pad Width (X4)	X1			1.00
Contact Pad Width (X2)	X2			0.60
Contact Pad Length (X6)	Y			0.85
Space Between Contacts (X4)	G1	0.75		
Space Between Contacts (X3)	G2	0.25		
Pin 1 Index Chamfer (X4)	CH		0.25	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3007-H5A Rev C

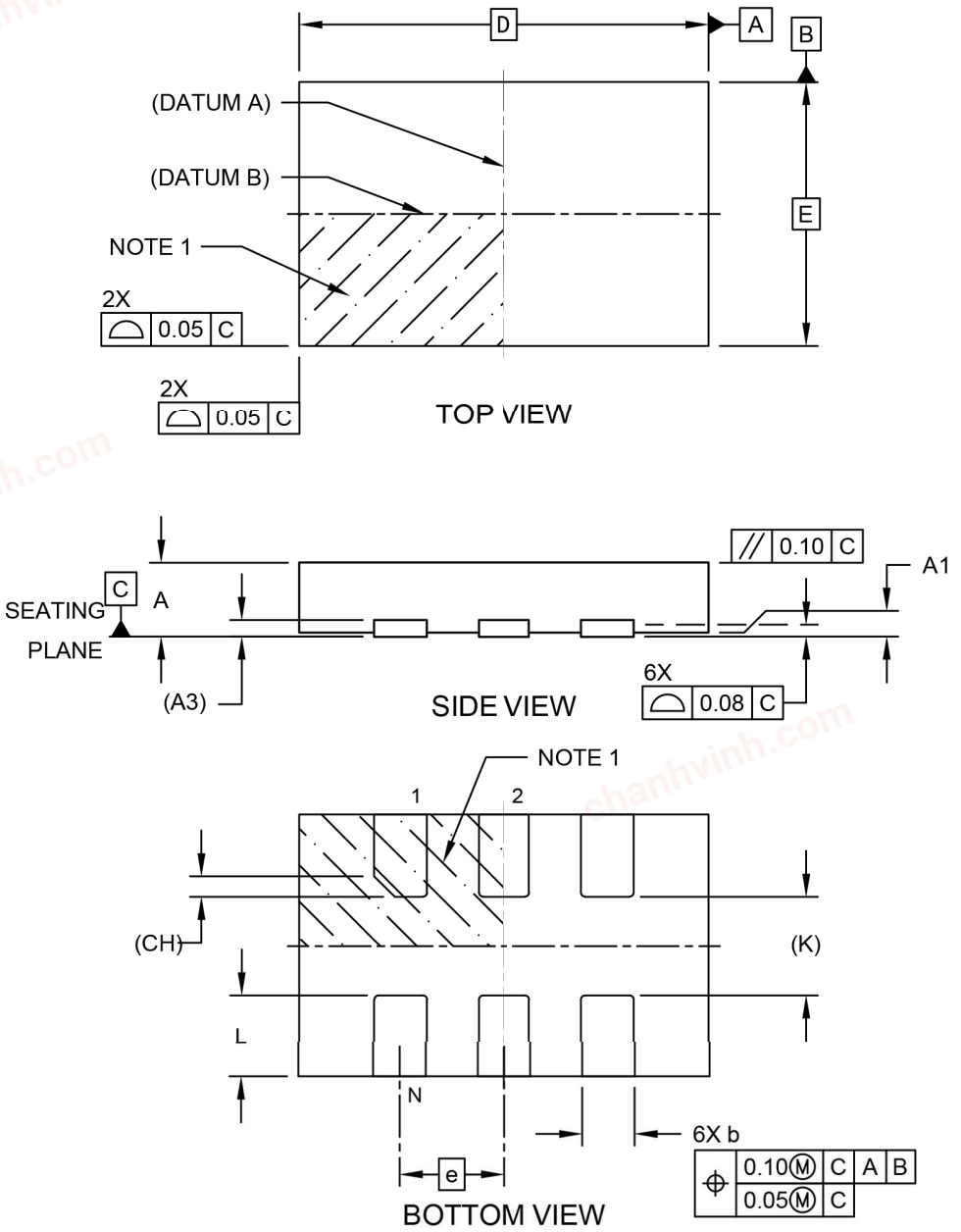
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6-Lead 3.2 mm × 5.0 mm VDFN (H7A) Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



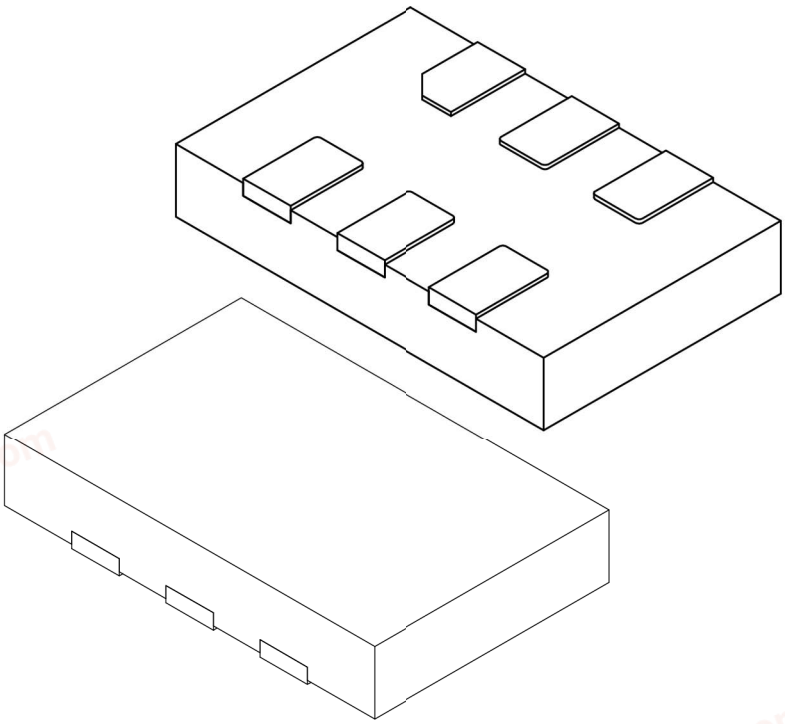
Microchip Technology Drawing C04-1009-H7A Rev B Sheet 1 of 2

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6-Lead Very Thin Plastic Dual Flat, No Lead Package (H7A) - 3.2x5.0 x0.9 Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Overall Width	E		3.20 BSC	
Terminal Width	b	0.59	0.64	0.69
Terminal Length	L	0.90	1.00	1.10
Terminal 1 Index Chamfer	CH		0.25 REF	
Terminal-to-Terminal	K		1.20 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1009-H7A Rev B Sheet 2 of 2

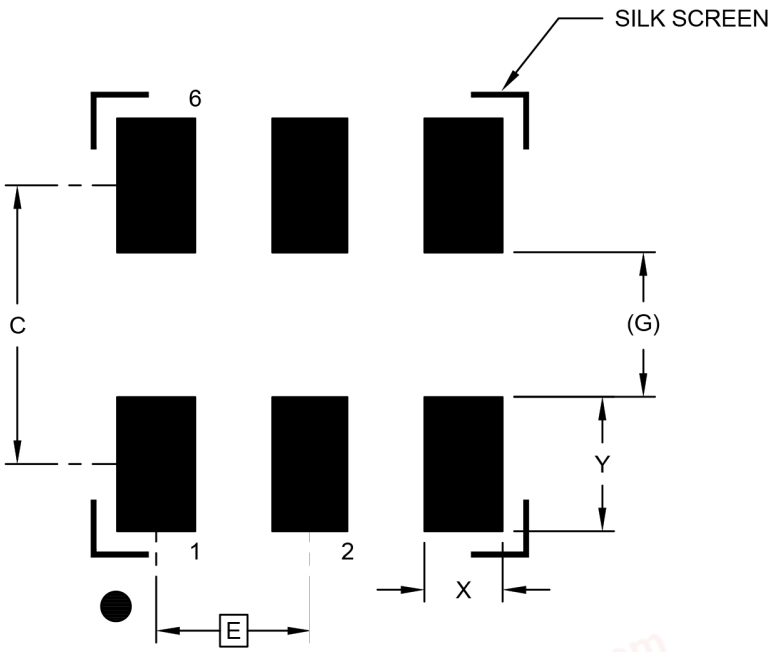
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6-Lead Very Thin Plastic Dual Flat, No Lead Package (H7A) - 3.2x5.0 x0.9 Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		2.30	
Contact Pad Width (X6)	X			0.64
Contact Pad Length (X6	Y			1.10
Contact Pad to Contact Pad (X4)	G	1.20 REF		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

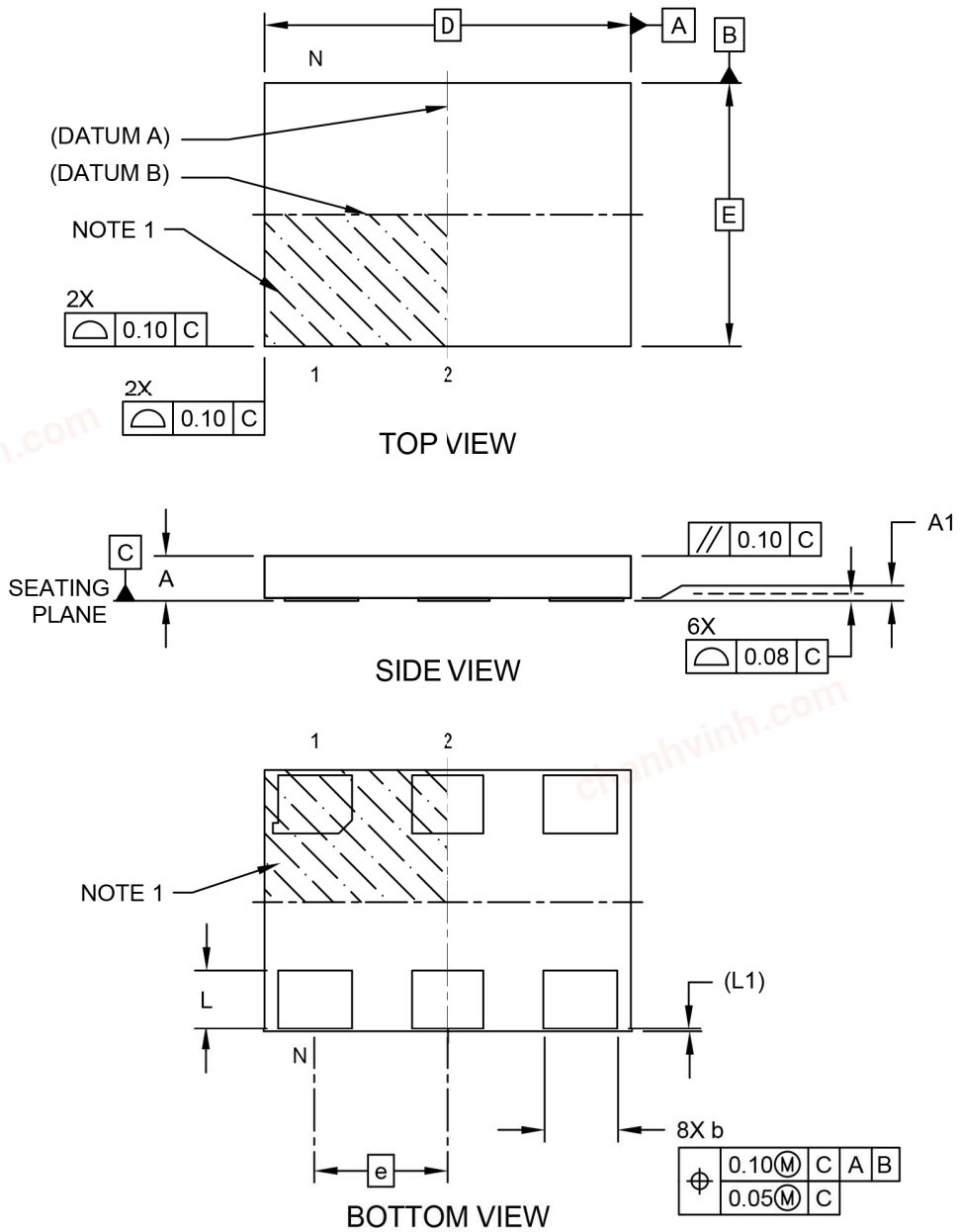
Microchip Technology Drawing C04-3009-H7A Rev B

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6-Lead 7.0 mm × 5.0 mm VDFN (HPA) Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1227-HPA Rev B Sheet 1of 2

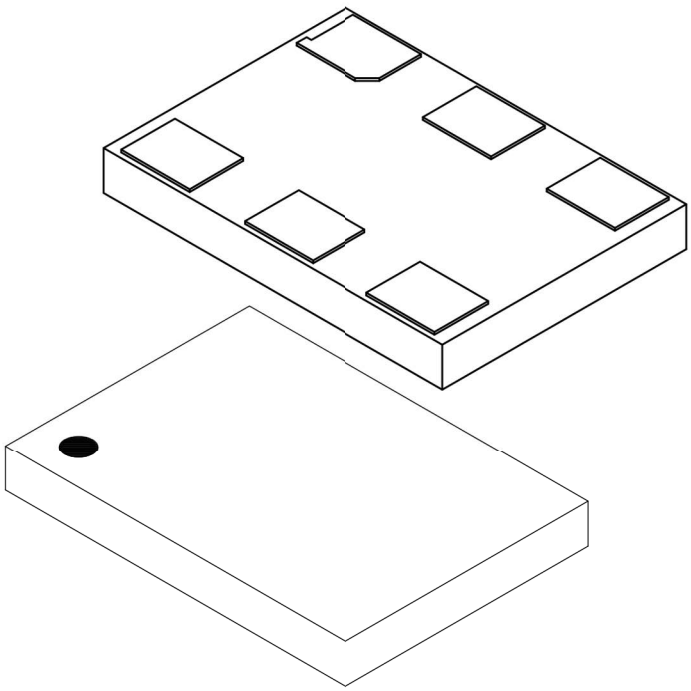
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6-Lead Very Thin Dual Flatpack, No Lead Package (HPA) - 7x5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		2.54 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		7.00 BSC	
Overall Width	E		5.00 BSC	
Terminal Width	b	1.30	1.40	1.50
Terminal Length	L	1.00	1.10	1.20
Pullback	L1		0.10 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

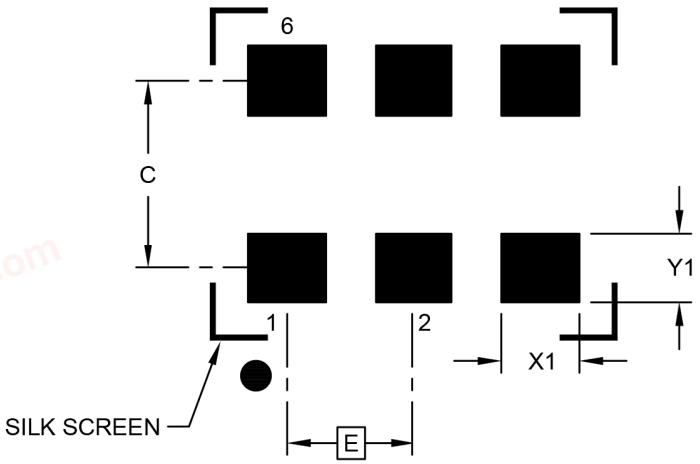
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6-Lead Very Thin Dual Flatpack, No Lead Package (HPA) - 7x5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		2.54 BSC	
Contact Pad Spacing	C		3.90	
Contact Pad Width (X6)	X1			1.55
Contact Pad Length (X6)	Y1			1.40

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3227-HPA Rev B

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APPENDIX A: REVISION HISTORY

Revision A (June 2020)

- Initial release of DSA12x2/3/4 as Microchip data sheet DS20006378A.

Revision B (March 2021)

- Updated Phase Jitter maximum values for J_{RMS-CC} in the Electrical Characteristics table and added a sixth note.
- Updated package drawing for 6-Lead 2.5 mm × 2.0 mm VDFN (J7A) Package Outline and Recommended Land Pattern.
- Updated Figure 3-1.

Revision C (March 2021)

- Removed Note 6 from the Electrical Characteristics table.

Revision D (May 2023)

- Updated the Features list to include PCIe Gen 6.
- Added Phase Jitter values for PCI Gen 6 to the LVDS and HCSL sections of the Electrical Characteristics table.

Revision E (October 2025)

- Added PCIe Gen 7 info to Features and Applications.
- Added PCIe Gen 7 phase jitter row in the Electrical Characteristics table.
- Updated Package Marking Information with additional DAP example.
- Replaced CDFN references throughout document text and images with current VDFN ones.
- Replaced old CDFN package outline drawing (POD) and recommended land pattern with Microchip package drawing for H7A 5032.
- Updated PODs to the latest revision for J7A 2520, H5A 3225, and HPA 7050.

Revision F (September 2026)

- Added “Unconfigured CPN” as an option to Output Format in the Product Identification System section.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	X	X	-XXXXXXXX	X	XXX
Device	Control Pin	Output Format	Package	Temperature	Freq. Stability	Output Frequency	Media Type	Automotive Suffix

Device:	DSA12:		High Performance Differential MEMS Oscillators for Automotive
Control Pin:	0	=	Pin 1 $\overline{\text{STDBY}}$ with Pull-up
	1	=	Pin 1 Frequency Select with Pull-up
	2	=	Pin 1 OE with Pull-up
	3	=	Pin 2 $\overline{\text{STDBY}}$ with Pull-up
	4	=	Pin 2 Frequency Select with Pull-up
	5	=	Pin 2 OE with Pull-up
Output Format:	0	=	Unconfigured CPN
	2	=	LVPECL
	3	=	LVDS
	4	=	HCSL
Package:	N	=	7 mm x 5 mm 6-Lead VDFN
	B	=	5 mm x 3.2 mm 6-Lead VDFN
	C	=	3.2 mm x 2.5 mm 6-Lead VDFN
	D	=	2.5 mm x 2 mm 6-Lead VDFN
Temperature:	A	=	–40°C to +125°C (Grade 1)
	L	=	–40°C to +105°C (Grade 2)
	I	=	–40°C to +85°C (Grade 3)
Frequency Stability:	1	=	±50 ppm
	2	=	±25 ppm
	3	=	±20 ppm
Output Frequency:	xMxxxxxx=		<10 MHz
	xxMxxxxx=		<100 MHz
	xxxMxxxx=		>100 MHz
	CCCCC=		with Frequency Select
	PROG =		TimeFlash
Media Type:	<blank>=		Bulk
	T	=	1,000/Reel
	B	=	3,000/Reel
Automotive Suffix:	VXX = Automotive Suffix in which “XX” is assigned by Microchip. Default value is “AO” for standard automotive part		

Please visit the Microchip ClockWorks Configurator® website to configure the part number for customized frequency select settings.

http://clockworks.microchip.com/timing

Examples:

a) DSA1202NI1-25M00000TVAO: Pin 1 $\overline{\text{STDBY}}$ with Pull-up, LVPECL Output, 7x5 VDFN, –20°C to +85°C, ±50 ppm, 25 MHz Output Frequency, 1,000/Reel, Standard Automotive

b) DSA1243CL3-C0013VAO: Pin 2 Frequency Select with Pull-up, LVDS Output, 3.2x2.5 VDFN, –40°C to +105°C, ±20 ppm, Multiple Output Frequency, Bulk, Standard Automotive

c) DSA124BI2-19M50000BVAO: Pin 1 OE with Pull-up, HCSL Output, 5x3.2 VDFN, –40°C to +85°C, ±25 ppm, 19.5 MHz Output Frequency, 3,000/Reel, Standard Automotive

d) DSA1232DL3-55M82000TVAO: Pin 2 $\overline{\text{STDBY}}$ with Pull-up, LVPECL Output, 2.5x2 VDFN, –40°C to +105°C, ±20 ppm, 55.82 MHz Output Frequency, 1,000/Reel, Standard Automotive

e) DSA1213NI1-C0014BVAO: Pin 1 Frequency Select with Pull-up, LVDS Output, 7x5 VDFN, –40°C to +85°C, ±50 ppm, Multiple Output Frequency, 3,000/Reel, Standard Automotive

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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