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DN3765

N-Channel Depletion-Mode Vertical DMOS FET

Features

- High Input Impedance
- Low Input Capacitance
- Fast Switching Speeds
- Low On-resistance
- Free from Secondary Breakdown
- Low Input and Output Leakage

Applications

- Normally-on Switches
- Solid-state Relays
- Converters
- Linear Amplifiers
- Constant Current Sources
- Telecommunications

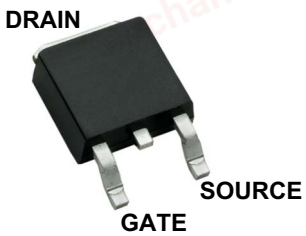
General Description

The DN3765 is a Depletion-mode (normally-on) transistor that uses an advanced vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type

TO-252 (D-PAK)
(Top view)



See Table 2-1 for pin information.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage ..... BV_{DSX}
Drain-to-Gate Voltage ..... BV_{DGX}
Gate-to-Source Voltage..... ±20V
Operating Ambient Temperature, T_A ..... –55°C to +150°C
Storage Temperature, T_S ..... –55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25°C$. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSX}	650	—	—	V	V_{GS} = –5V, I_D = 100 µA
Gate-to-Source Off Voltage	$V_{GS(OFF)}$	–1.5	—	–3.5	V	V_{DS} = 25V, I_D = 10 µA
Change in $V_{GS(OFF)}$ with Temperature	$\Delta V_{GS(OFF)}$	—	—	–4.5	mV/°C	V_{DS} = 25V, I_D = 10 µA (**Note 1**)
Gate Body Leakage Current	I_{GSS}	—	—	100	nA	V_{GS} = ± 20V, V_{DS} = 0V
Drain-to-Source Leakage Current	$I_{D(OFF)}$	—	—	10	µA	V_{GS} = –10V, V_{DS} = Maximum rating
		—	—	1	mA	V_{GS} = –10V, V_{DS} = 0.8 Maximum rating, T_A = 125°C (**Note 1**)
Saturated Drain-to-Source Current	I_{DSS}	200	—	—	mA	V_{GS} = 0V, V_{DS} = 25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	8	Ω	V_{GS} = 0V, I_D = 150 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1.1	%/°C	V_{GS} = 0V, I_D = 150 mA (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested

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AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25°C$. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	100	—	—	mmho	V_{DS} = 10V, I_D = 100 mA
Input Capacitance	C_{ISS}	—	—	825	pF	V_{GS} = –10V, V_{DS} = 25V, f = 1 MHz
Common-Source Output Capacitance	C_{OSS}	—	—	190	pF	
Reverse Transfer Capacitance	C_{RSS}	—	—	110	pF	
Turn-on Delay Time	$t_{d(ON)}$	—	—	50	ns	V_{DD} = 25V, I_D = 150 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	—	75	ns	
Turn-off Delay Time	$t_{d(OFF)}$	—	—	75	ns	
Fall Time	t_f	—	—	100	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	1.8	V	V_{GS} = –5V, I_{SD} = 200 mA (Note 1)
Reverse Recovery Time	t_{rr}	—	800	—	ns	V_{GS} = –5V, I_{SD} = 200 mA

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
TO-252 (D-PAK)	θ_{JA}	—	81	—	°C/W	

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (mA)	Power Dissipation at T_A = 25°C (W) (Note 2)	I_{DR} (Note 1) (mA)	I_{DRM} (mA)
TO-252 (D-PAK)	300	500	2.5	300	500

Note 1: I_D (continuous) is limited by maximum rated T_J of 150 °C.

2: Mounted on an FR4 board, 25 mm x 25 mm x 1.57 mm

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2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in DN3765. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2	Source	Source
3	Drain	Drain

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3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 illustrates the switching waveforms and test circuit for DN3765.

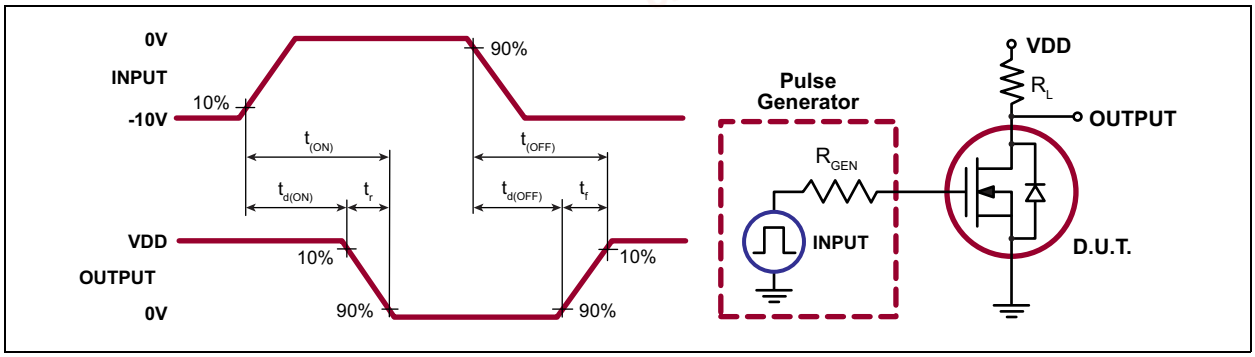


FIGURE 3-1: *Switching Waveforms and Test Circuit.*

TABLE 3-1: PRODUCT SUMMARY

BV_{DSX}/BV_{DGX} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	I_{DSS} (Minimum) (mA)
650	8	200

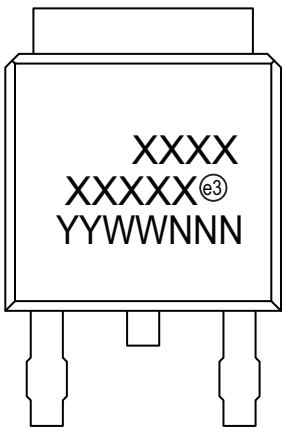
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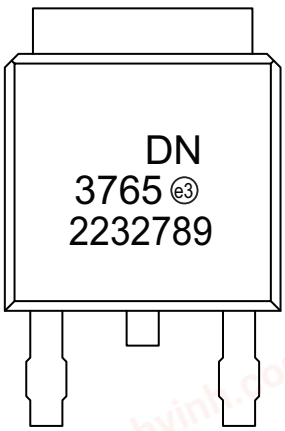
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

TO-252 (D-PAK)



Example



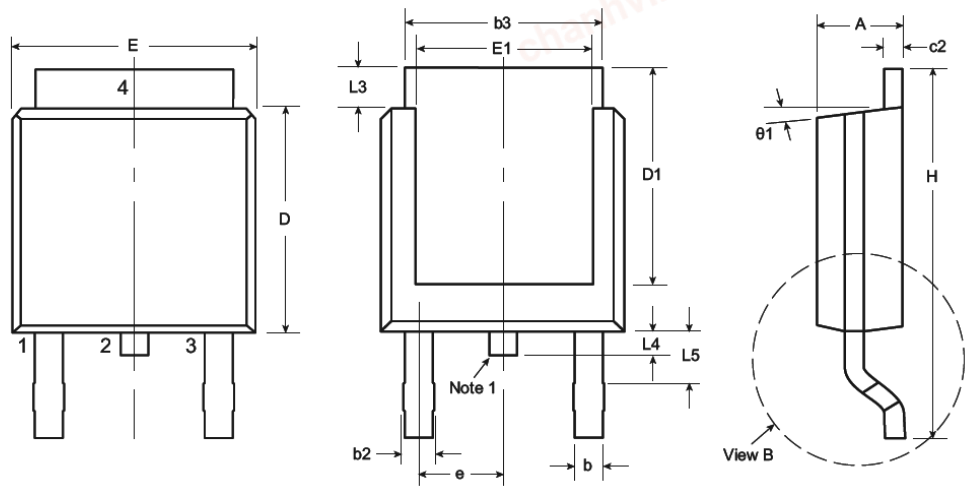
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

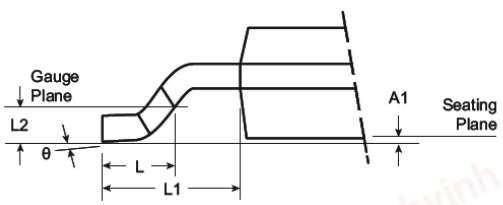
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3-Lead TO-252 (D-PAK) Package Outline (K4)



Front View **Rear View** **Side View**



View B

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

Symbol		A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimen-sion (inches)	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170	.090 BSC	.370	.055	.108 REF	.020 BSC	.035	.025*	.035†	0º	0º
	NOM	-	-	-	-	-	-	.240	-	-	-		-	.060			-	-	-	-	-
	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.200*		.410	.070			.050	.040	.060	10º	15º

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (August 2022)

- Converted Supertex Doc# DSFP-DN3765 to Microchip DS20005813A
- Changed the packaging format
- Made minor text changes throughout the document

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DN3765

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	DN3765	=	N-Channel Depletion-Mode Vertical DMOS FET
Package:	K4	=	3-lead TO-252 (D-PAK)
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	2000/Reel for a K4 Package

Example:

a) DN3765K4-G: N-Channel Depletion-Mode Vertical DMOS FET, 3-lead TO-252 (DPAK), 2000/Reel

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