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CL88030/31

Sequential Linear LED Driver with Four or Six Taps

Features

- Suitable for 120VAC/230VAC/277VAC Nominal Input Voltage
  - ± 15% input voltage tolerance recommended
- Targeted for 2W and Greater Output Power
- Programmable Overtemperature Protection
  - Provides gradual reduction in light output with increasing temperature
- Active Line Regulation
  - Provides fairly constant output power over variations in AC line voltage
  - Adjustable “knee” of regulation
- 4 Taps(CL88030) or 6 Taps(CL88031) with Two Current Set Resistors
  - Allows optimization of THD
- Optional Reduced Flicker Index
  - Provides near-continuous power to the LEDs
  - Reduces strobing
  - Uses an external capacitor
- Compatible with Phase-cut Dimming, both Leading-edge and Trailing-edge
- Uses a Thermally Enhanced DFN-10 Package with Bottom Heatslug
  - No high voltage Pins
  - Shunt regulator input
  - Power dissipation is in the external FETs and LEDs, not in the IC

Applications

- LED lamps
- LED lighting fixtures

Description

The CL88030T and CL88031T LED Driver Integrated Circuits (ICs) are intended offline sequential linear LED drivers designed to provide LED power from a utility voltage input.

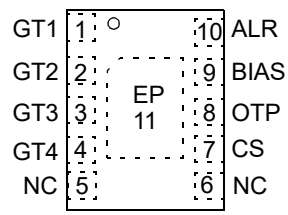
The CL88030/31 devices are designed to drive a long string of inexpensive, low-current LEDs directly from the AC mains. A basic driver circuit consists of Microchip’s CL88030/31 LED driver IC, four power FETs (six if using the CL88031), four resistors, two capacitors, and a bridge rectifier. Additional components are optional for various levels of transient protection. Adding an inexpensive NTC-thermistor assures over temperature protection (OTP). No EMI filters or power factor correction circuits are needed (unless the optional flicker-reduction feature is desired).

A string of series/parallel LEDs is tapped at four (or six) locations, called “taps”. Linear current regulators sink current at each tap through a single control point and are sequentially turned on and off. High efficiency is achieved by shutting off upstream regulators when downstream regulators achieve regulation. This makes controlling overall input current easier than trying to control multiple current paths by tracking the input sine wave voltage.

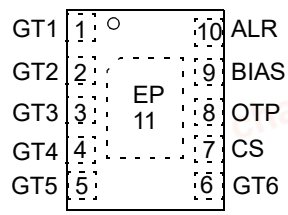
The CL88030/31 uses a self-commutation technique using only the tap currents themselves; this technique inherently provides smooth transitions from one regulator to the next, without relying on tap voltages or the rectified AC to coordinate the transitions.

Pin Diagram

CL88030T
3 x 3 DFN*



CL88031T
3 x 3 DFN*

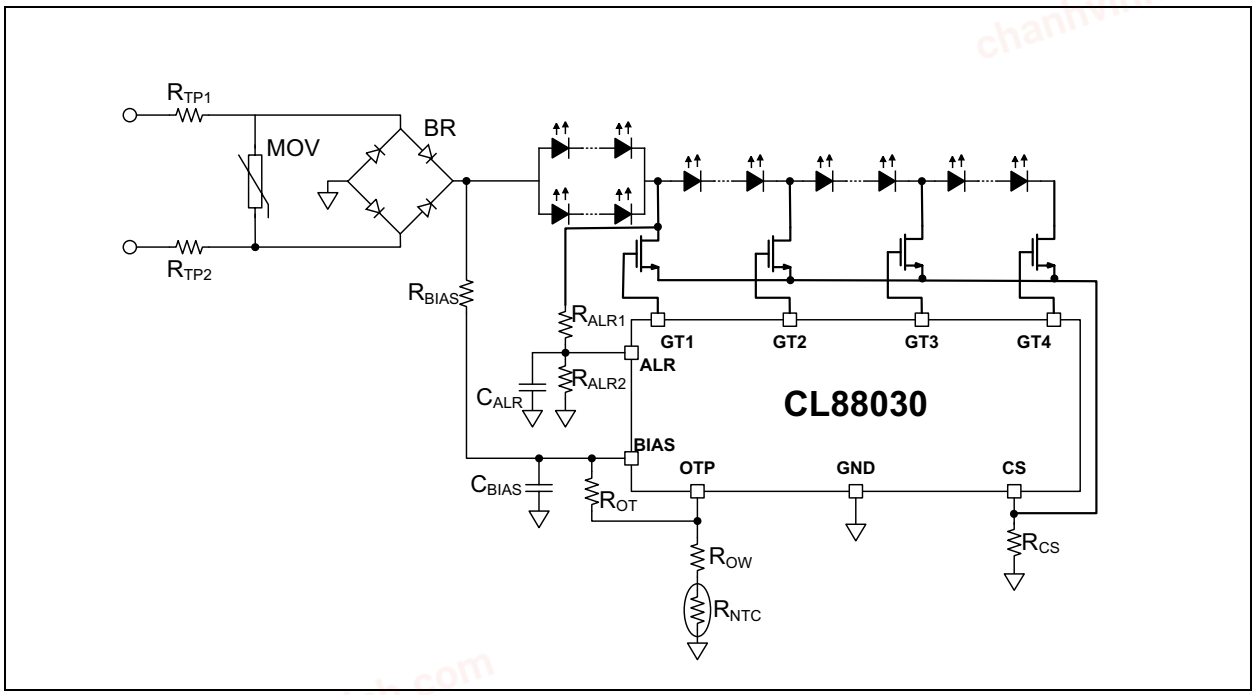


* Includes Exposed Thermal Pad (EP); see Table 2-1

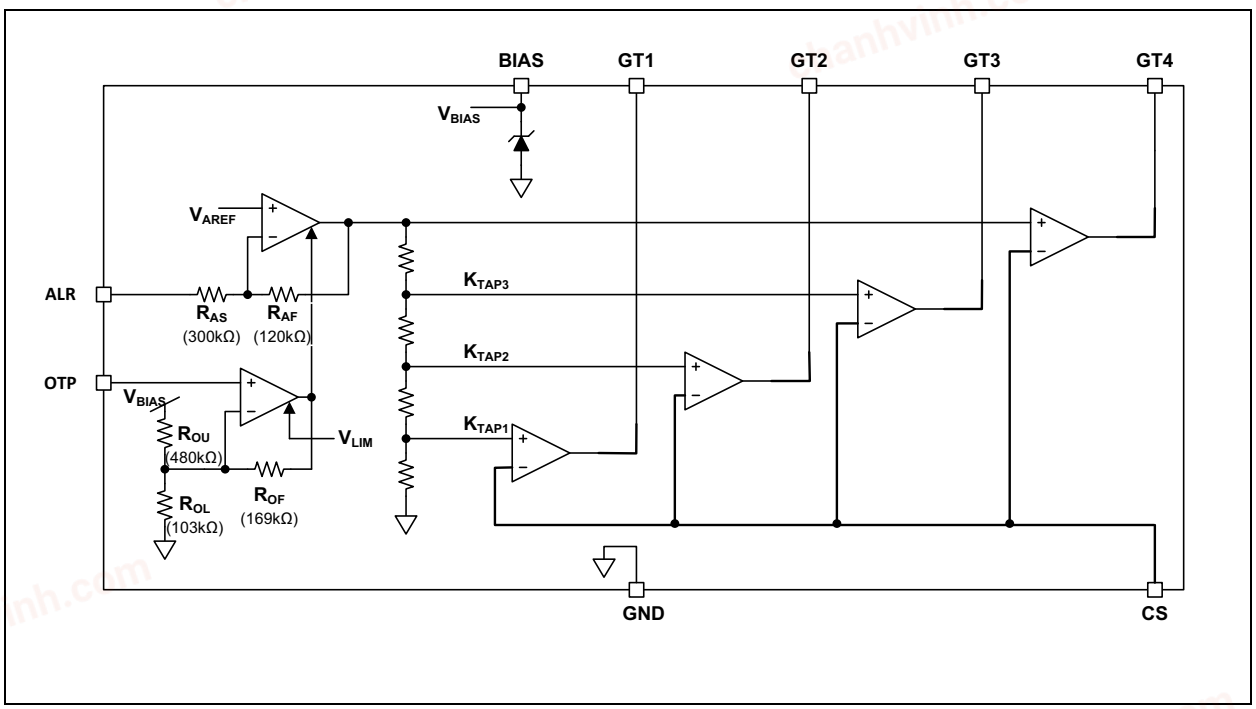
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TYPICAL CL88030T APPLICATION CIRCUIT



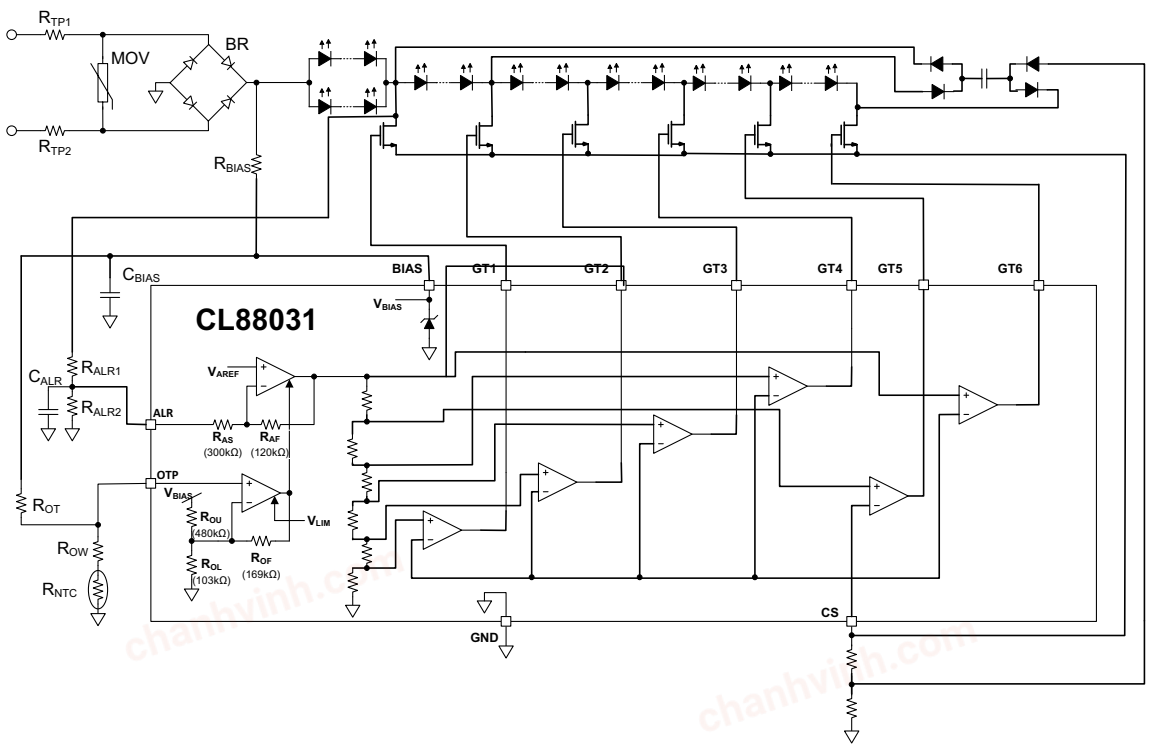
CL88030 INTERNAL BLOCK DIAGRAM



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TYPICAL CL88031T APPLICATION CIRCUIT AND BLOCK DIAGRAM (Note)



Note: With optional ripple reduction circuit.

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1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

GT1-4 (and GT5-6 on CL88031T).....–0.5V to (BIAS + 0.5V)

OTP, ALR, CS..... –0.3V to 5.5V

BIAS ..... –0.3V to 13V

Maximum Current into BIAS pin.....10 mA
Operating Junction Temperature.....–40°C to +125°C
Lead Soldering Temperature for 10s..... 300
Storage Temperature.....–65°C to +150°C
ESD Voltage in any pin ..... 2000V(HBM)

Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 ELECTRICAL SPECIFICATIONS

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all specifications are for $T_A = T_J = +25°C$. $I_{BIAS} = 1.5$ mA. ALR pin open, OTP = 5V unless otherwise noted. Boldface specifications apply over the full temperature range $T_A = T_J = –15°C$ to +95°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Gate Output Low (all GTx), V_{CS} = 2.0V	$V_{GT,low}$			0.100	V	
Gate Output High (all GTx), V_{CS} =0V	$V_{GT,high}$	V_{BIAS}- 1.0			V	
Voltage at BIAS pin I_{BIAS} = 0.8,5 mA,V_{CS}= 0V, CL88030	V_{BIAS}	**10**	**11**	**12**	V	
Voltage at BIAS pin I_{BIAS} = 1.0,5 mA,V_{CS}= 0V, CL88031						
Gate Output High Current (all GTx) 100k GTx to GND, V_{CS} = 0V	$I_{GT,high}$	10			µA	
Quiescent Current Consumption	$I_{BIAS,Q}$	—		900 1300	µA	Characterization Only, Note 1
Reference Voltage for Tap 4	V_{GT4}	**1.210**	**1.275**	**1.339**	V	CL88030, (Note 2)
GT3 to GT4 Current Ratio	K_{TAP3}	**0.883**	**0.929**	**0.975**	ratio	CL88030, (Note 2)
GT2 to GT4 Current Ratio	K_{TAP2}	**0.747**	**0.786**	**0.825**		CL88030, (Note 2)
GT1 to GT4 Current Ratio	K_{TAP1}	**0.542**	**0.571**	**0.600**		CL88030, (Note 2)
Reference Voltage for Tap 6	V_{GT6}	**1.210**	**1.275**	**1.339**	V	CL88031, (Note 2)
GT5 to GT6 Current Ratio	K_{TAP5}	**0.912**	**0.960**	**1.008**	ratio	CL88031, (Note 2)
GT4 to GT6 Current Ratio	K_{TAP4}	**0.893**	**0.940**	**0.987**		CL88031, (Note 2)
GT3 to GT6 Current Ratio	K_{TAP3}	**0.846**	**0.890**	**0.935**		CL88031, (Note 2)
GT2 to GT6 Current Ratio	K_{TAP2}	**0.741**	**0.780**	**0.819**		CL88031, (Note 2)
GT1 to GT6 Current Ratio	K_{TAP1}	**0.494**	**0.520**	**0.546**		CL88031, (Note 2)
Limiting Voltage from OTP, V_{ALR}= 0V,100 pF CS to GND, GT4/GT6 to CS	V_{LIM}	1.296	1.525	1.754	V	
Nominal ALR Voltage Reference, ALR pin open, GT4/GT6 to CS, 100 pF CS to GND	$V_{ALR,nom}$		1.275		V	
ALR Voltage Ratio at GT4/GT6	$K_{ALR,HI}$	**0.801**	**0.843**	**0.885**	ratio	Note 3
ALR Voltage Ratio at GT4/GT6	$K_{ALR,LO}$	**1.073**	**1.129**	**1.186**	ratio	Note 4
OTP Response Voltage	OTP	**0.90**	**1.10**	**1.32**	V	Note 5

Note 1: Does not include GATE current, or current into ALR or OTP divider. 900µA=CL88030, 1300µA=CL88031

2: GTx connected to CS, with 100pF from CS to GND.

3: V_{ALR} = 1.776V, GT4/GT6 to CS, 100 pf CS to GND.

4: V_{ALR} = 0.863V, GT4/GT6 to CS, 100 pf CS to GND.

5: GT4/GT6 to CS (unity gain), OTP=1.658V, 100pF CS to GND measure CS/GTx, see Equation 3-3.

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TABLE 1-2: TEMPERATURE SPECIFICATIONS

Parameters	Sym	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_J	-40°C	—	+125°C	°C	Note 1
Storage Temperature Range	T_A	-65°C	—	+150°C	°C	
Package Thermal Resistances						
Thermal Resistance, 10LD-DFN	θ_{JC}	—	+8°C	—	°C/W	Note 2

Note 1: The Operating Temperature Range is specified at the junction. The junction temperature must be computed using the thermal resistance (TR) from junction-to-case, and the case-to-ambient TR of the PCB design.

2: Thermal resistance is measured from junction to bottom metal slug.

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2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN DESCRIPTION

CL88030T	CL88031T	Pin Name	Description
1	1	GT1	Drives the FET for the most upstream LED string
2	2	GT2	Drives the FET for the top 2 LED strings
3	3	GT3	Drives the FET for the top 3 LED strings
4	4	GT4	Drives the FET for the top 4 LED strings
5	—	NC	Not Connected. To be left floating.
6	—	NC	Not Connected. To be left floating.
7	7	CS	Used to set the currents in the taps
8	8	OTP	Provides remote Overtemperature Protection.
9	9	BIAS	Provides power to the IC using an internal shunt regulator. It is recommended to be bypassed with a low ESR ceramic capacitor (at least 1 µF)
10	10	ALR	An external resistive voltage divider and capacitor provide line regulation for the tap currents
11	11	GND	Circuit common electrical connection (ground)
—	5	GT5	Drives the FET for the top 5 LED strings
—	6	GT6	Drives the FET for the top 6 LED strings

2.1 GT1 Pin

Gate drive voltage connection for external power FET for the first/top LED string.

2.2 GT2 Pin

Gate drive voltage connection for external power FET for the second LED string.

2.3 GT3 Pin

Gate drive voltage connection for external power FET for the third LED string.

2.4 GT4 Pin

Gate drive voltage connection for external power FET for the fourth LED string.

2.5 GT5 Pin

Gate drive voltage connection for external power FET for the fifth LED string.

2.6 GT6 Pin

Gate drive voltage connection for external power FET for the sixth LED string.

2.7 Current Set Pin (CS)

A resistor from this pin to ground sets the LED string current.

2.8 Overtemperature Protection Pin (OTP)

This input is connected to a resistor/NTC-thermistor combination to reduce the LED current when the temperature becomes too high.

2.9 BIAS Pin

An input pin to provide voltage to the chip. The BIAS pin is the input to a shunt regulator and must be fed by a current source, not a fixed voltage.

2.10 Active Line Regulation Pin (ALR)

This input pin is connected to an RC network to sense the input main voltage and regulate the LED string current against variations in AC input voltage.

2.11 Ground Terminal (GND)

Reference ground for all input voltages.

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3.0 FUNCTIONAL DESCRIPTION

3.1 Introduction

The CL88030/31 LED driver ICs are designed to drive a long string of inexpensive, low-current LEDs directly from the AC mains. A string of series/parallel LEDs is tapped at four (or six) locations. Linear current regulators sink current at each tap through a single control point and are sequentially turned on and off.

This IC is targeted to drive a string of LEDs from a nominal utility mains input voltage and provide >2W of output power. It has an internal line regulation circuit to regulate the output power as the line voltage changes from minimum to maximum. It also includes a remote Overtemperature Protection which allows thermal de-rating of the output power using a remote NTC to sense the LED or lamp temperature.

3.2 Principle of Operation

The CL88030 employs a very simple method of implementing single-point control and self-commutation, as shown in Figure 3-1. The single current sense resistor to ground (R_{CS}) comprises single-point control. Each tap's error amplifier shares this single control point, although only one err amp is active at any one time.

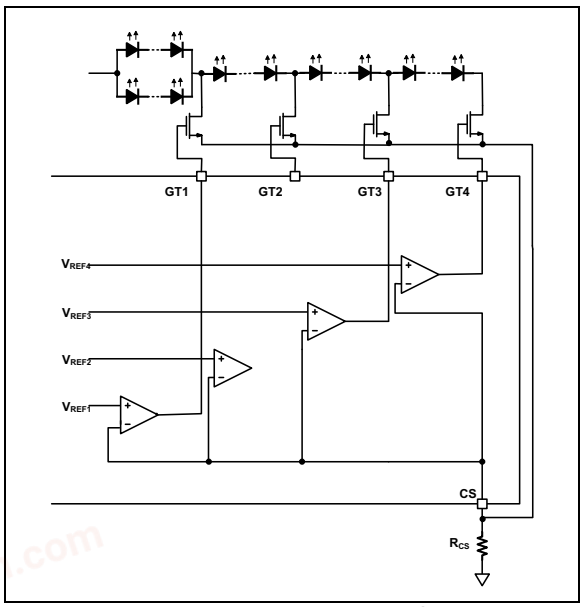


FIGURE 3-1: *Tap Commutation.*

Each current regulator has its own reference voltage, derived from a resistive voltage divider such that:

$$V_{REF4} > V_{REF3} > V_{REF2} > V_{REF1}$$

Initially, V_{CS} is at 0V, causing all the current regulators to be turned on but not conducting. Once the rectified AC rises high enough to forward bias the first LED string segment, the first current regulator begins conducting. Eventually it achieves regulation. At this point V_{REF1} and V_{CS} are in equilibrium. As the rectified AC continues to rise, the next LED segment becomes forward biased. Since the second regulator's reference voltage (V_{REF2}) is higher than V_{CS}, the second regulator is already on and begins conducting (although not regulating), injecting current (I_{TAP2}) into the single control point, raising the V_{CS} voltage. The first regulator responds to the increase in V_{CS} by reducing I_{TAP1} such that V_{CS} remains equal to V_{REF1}.

EQUATION 3-1:

$$I_{TAP1} = \frac{V_{REF1}}{R_{CS}} - I_{TAP2}$$

I_{TAP1} continues to decrease as I_{TAP2} increases. When the rectified AC rises sufficiently for the second regulator to achieve regulation, V_{CS} increases to be equal with V_{REF2}. With V_{CS} now greater than V_{REF1}, the first regulator is effectively shut off and the second regulator takes over. This repeats for the other taps and also works in reverse as the rectified AC passes the peak and begins decreasing.

This simple self-commutating mechanism and single-point control automatically sequences the current regulators and assures smooth tap-to-tap transitions.

3.2.1 ACTIVE LINE REGULATION (ALR)

Without compensating for line voltage variations, as the AC voltage increases, downstream LED segments become active. In addition, the dwell time at the higher tap currents increases as AC voltage goes up. This causes brightness to increase with AC voltage, resulting in poor line regulation.

The ALR circuit maintains fairly constant output power over variations in AC line voltage. It is not a closed loop system that directly monitors and corrects output power. Instead, it monitors the voltage applied to the LED string and uses it to adjust the reference voltage provided by the OTP circuit. The circuit used for achieving the active line regulation is shown in Figure 3-2.

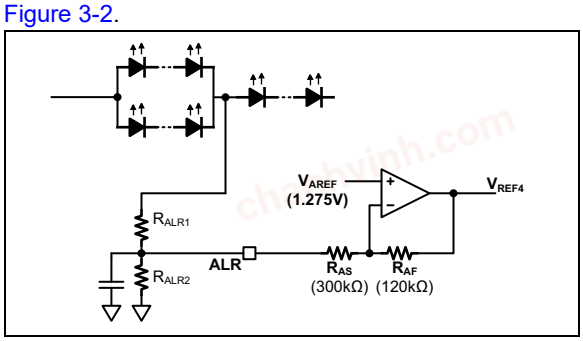


FIGURE 3-2: *ALR Circuit.*

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Under normal operation (OTP not activated) the OTP limiting voltage is essentially the reference voltage used to set the tap currents. The ALR circuit adjusts this voltage up or down to compensate for variations in the AC line voltage as represented by the voltage at the ALR pin.

EQUATION 3-2:

$$V_{REF4} = 1.275V - \left(\frac{V_{ALR} - 1.275V}{300k\Omega} \cdot 120k\Omega\right)$$

The external resistor divider at the ALR pin is usually chosen such that the average voltage at the pin is 1.275V at nominal 120 V_{AC} input. The ALR divider is connected after the first LED segment to increase its sensitivity to changes in the AC line voltage.

The function of the limiter circuit is three-fold. Except during OTP, the limiting voltage is fixed. First, during the initial application of power, the ALR filter capacitor (C_{ALR}) is at 0V. This would result in high LED current until C_{ALR} charges up. Without a limiter, this would cause a bright flash at turn-on. The second purpose of the limiter is during dimming, where the average ALR voltage will be low, causing the LED drive current to be high. This defeats the dimmer and could result in excessive currents. Lastly, during an overtemperature condition, the OTP circuit gradually lowers the limiting voltage from its fixed value. This reduces the power applied to the LEDs, lowering their temperature until an equilibrium is established.

3.2.2 OVERTEMPERATURE PROTECTION (OTP)

OTP uses an inexpensive, external NTC thermistor to remotely sense LED temperature. The thermistor can be located in close proximity to the LEDs, providing near-direct LED temperature monitoring. The OTP temperature is adjustable via selection of NTC resistance. It is essential that OTP operate linearly, gradually reducing output power as temperature increases. The thermistor is arranged in a full-bridge configuration with the active arm consisting of the NTC and a discrete resistor to V_{BIAS} (Figure 3-3). The passive arm consists of internal resistors. The thermistors' resistance versus temperature curve asymptotically approaches 0Ω as temperature rises. To provide a well-defined window between the threshold temperature and the extinguishing temperature, a small segment of the thermistors' resistance-temperature curve must be used.

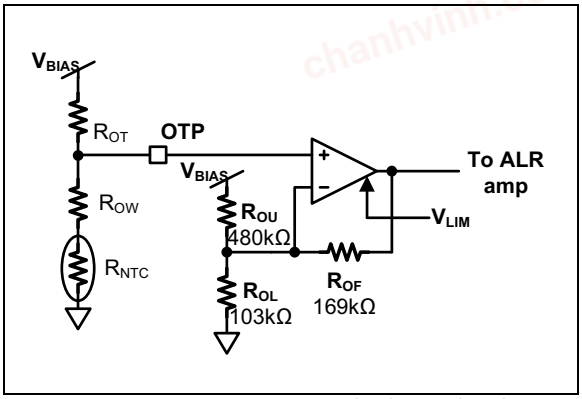


FIGURE 3-3: *OTP Equivalent Circuit.*

R_{OF} and the parallel combination of R_{OU} and R_{OL} determine OTP gain and set the width of the OTP window — the higher the gain, the narrower the window. Offset is determined by the passive arm of the bridge and sets the location of the OTP window along the temperature axis.

If OTP is unused, the OTP pin should be connected to 5V, by making a resistor divider through the BIAS pin.

The output of the OTP amplifier (which is used as a limit for the ALR amplifier) can be expressed as:

EQUATION 3-3:

$$V_{REF4} = R_{OF} \cdot \left[V_{OTP} \cdot \left(\frac{1}{R_{OF}} + \frac{1}{R_{OU}} + \frac{1}{R_{OL}}\right) - \frac{V_{BIAS}}{R_{OU}}\right]$$

$$= (2.993 \cdot V_{OTP} - (0.3521 \cdot V_{BIAS}))$$

Note that in the above equation, it is assumed that the input voltage is at nominal value and there is no adjustment to the reference due to the ALR circuit.

The output of the OTP amplifier is internally clamped to 1.575V, which corresponds to a voltage of 1.77V at the OTP pin. As the voltage at the OTP pin decreases to 1.686V, the output of the OTP amplifier falls to 1.275V. It is at this point, the OTP circuit starts modifying the tap currents and causes thermal derating.

Using two fixed resistors and one NTC, both the breakpoint and the slope of the derating curve can be set independently.

For example, consider a case with a breakpoint of 85°C with a derating curve such that the LED driver is at 20% of full power at 110°C. The NTC thermistor used is a 470 kΩ, with a Bvalue of 4500K. The NTC resistance at a given temperature (T_C, expressed in °C) can be expressed as:

EQUATION 3-4:

$$R_{NTC,\,Tc} = R_{NTC,\,25C} \cdot e^{-B \cdot \left(\frac{1}{298K} - \frac{1}{Tc + 273}\right)}$$

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Using Equation 3-4, the corresponding NTC resistances at 85°C and 110°C are 33.4 kΩ and 14.2 kΩ. Using these NTC resistance values, R_{OW} and R_{OT} can then be computed assuming 11 volts V_{BIAS}. The final set of values are provided in the Table 3-1.

TABLE 3-1: OVERTEMPERATURE PROTECTION

Parameter	25°C	85°C	110°C
R_{OT}	511 kΩ	511 kΩ	511 kΩ
R_{OW}	57.6 kΩ	57.6 kΩ	57.6 kΩ
R_{NTC}	470 kΩ	33.4 kΩ	14.2 kΩ
V_{OTP}	5.580V*	1.661V	1.135V
V_{OTPAMP}	1.575V	1.102V	0.183V

*Refer to Application Notes, Section 3.2.5

3.2.3 RIPPLE REDUCTION (OPTIONAL)

Low output ripple is achieved using a capacitor and four diodes. The capacitor may be one or more paralleled ceramic capacitors or a single electrolytic. Multiple ceramic capacitors may be needed due to their poor voltage coefficient. The four diodes may be obtained in a single small package.The LED and rectifier arrangement is shown in Figure 3-4.

With this method, all currents, including ripple capacitor charging and discharging currents, are controlled, passing through the same single control point. This allows the input current wave-shape to be maintained and avoids peak-charging the ripple-reduction capacitor.

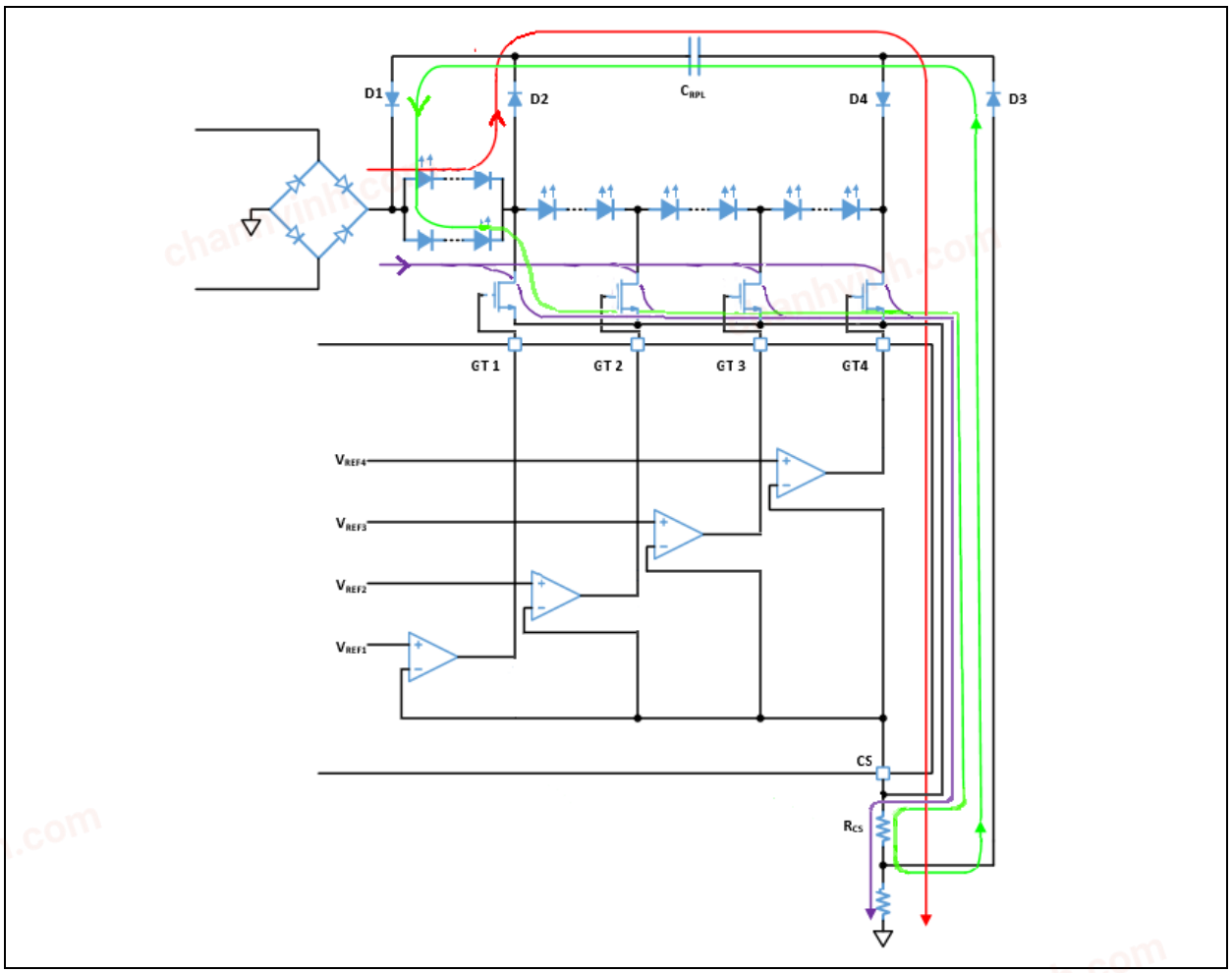


FIGURE 3-4: *Ripple Reduction Circuit.*

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The CL88030/31 with the ripple reduction circuit operates in four phases: recharge, hold-up, direct and under certain conditions, idle. Note that all active current paths include Segment 1, assuring uninterrupted light output during all phases of operation, excluding the idle phase.

Recharge (red path)

Recharging of the ripple capacitor (C_{RPL}) occurs when ($V_{RAC} – V_{SEG1}$) > V_{CRPL}. The maximum voltage that C_{RPL} can be charged to is:

$$V_{CRP(max)} = V_{SEG2} + V_{SEG3} + V_{SEG4}$$

The numbers of LEDs for each segment must be chosen carefully so as not to exceed C_{RPL}'s voltage rating while at the same time allowing C_{RPL} to charge up to a voltage sufficient to drive at least SEG1. To provide continuous light output, the recharge path must include LEDs.

Hold-Up (green path)

When the rectified AC falls below V_{CRPL}, the capacitor takes over, supplying the LEDs. The discharge path flows through R_{SET1} only. Since this is lesser sense resistance than for the other current paths, the current for the hold-up phase will be higher. This allows for normal currents to be drawn from the AC line to better track the input voltage sine wave while allowing a higher current during the hold-up interval.

Direct (purple paths)

When V_{CRPL}< V_{RAC} < (V_{CRPL} + V_{SEG1}), the LEDs are supplied directly from the AC line. The window when the direct phase is active is determined by V_{SEG1}.

Idle (no path)

At low AC line voltages, there is not enough voltage to charge C_{RPL} sufficiently to power SEG1 and strobing will occur. Also, strobing will occur if C_{RPL} is too small.

3.2.4 FET SELECTION

The advantage of external FETs is three-fold. First, external FETs allow the LED driver to be scaled in both power and voltage. This allows us to produce one chip that can meet the needs of many different markets. Secondly, the heat can be spread over multiple devices, allowing for cooler overall operation. Thirdly, without the high real estate used by integrated FETs, nor the high voltage requirements, the die can be made very small. The scalability plus small die results in a low cost chip that can address a multitude of high-brightness markets.

Common AC line voltages used in lighting are 90VAC, 120VAC, 208VAC, 230VAC, 277VAC, 347VAC, and 480VAC. A sequential linear driver can only be designed to handle one of these voltages – no multi-range, universal inputs can be realized.

Complicating the voltage requirements are lightning induced transients on the AC line. Depending on where the lamp is used, transient survivability requirements can range from 500V for protected indoor locations up to 10 kV for unprotected outdoor locations. Since high-brightness lamps will be mainly used outdoors, transient survivability requirements will be on the high end of the range. Transient protection can absorb the transients, but there is a rather large gap between the normal peak line voltage and the clamping voltage provided by the protection circuits, which can be hundreds of volts. The low-voltage controller will be powered by a shunt regulator. This avoids any high voltage on the controller, enabling it to be a strictly low voltage (~11V) chip. Due to the LED voltage drops, each tap has, theoretically, a different voltage requirement. And FET 1 sees higher current than FET 4. However, in practice one common FET is used to handle all taps. And from a BOM perspective, using a common FET can keep costs lower. For these be a strictly low voltage (~11V) chip. Due to the LED voltage drops, each tap has, theoretically, a different voltage requirement. And FET 1 sees higher current than FET 4. However, in practice one common FET is used to handle all taps. And from a BOM perspective, using a common FET can keep costs lower. For these reasons, a common FET is mentioned for every tap. Light output is estimated at 100 lm/watt.

3.2.5 APPLICATION NOTES

To prevent the OTP pin from going too high in voltage at cold temperatures, a 5.1 volt zener clamp to GND may be needed.

Because FET gate capacitance can vary considerably, it may be necessary to add a small GTx to GND capacitor for stability.

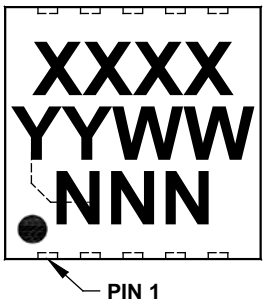
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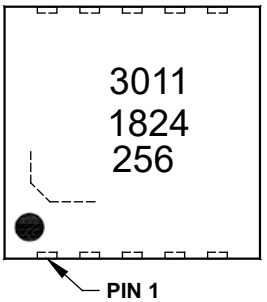
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

10-Lead DFN (3x3x0.9 mm)



Example



Part Number	Code
CL88030T-E/MF	3011
CL88031T-E/MF	3111

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

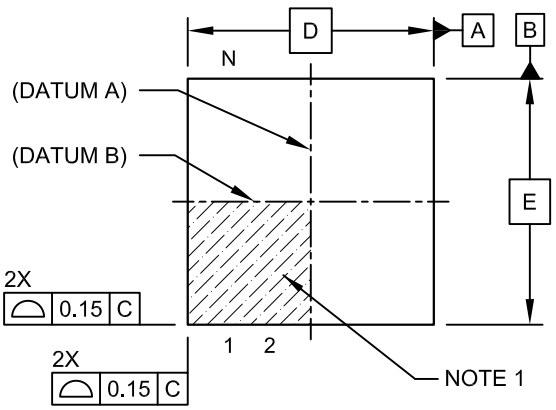
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or may not include the corporate logo.

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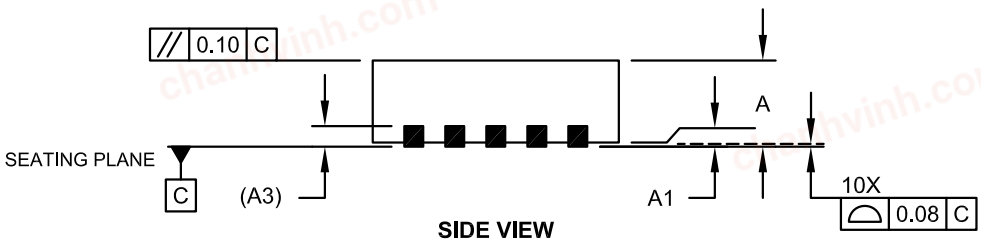
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10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

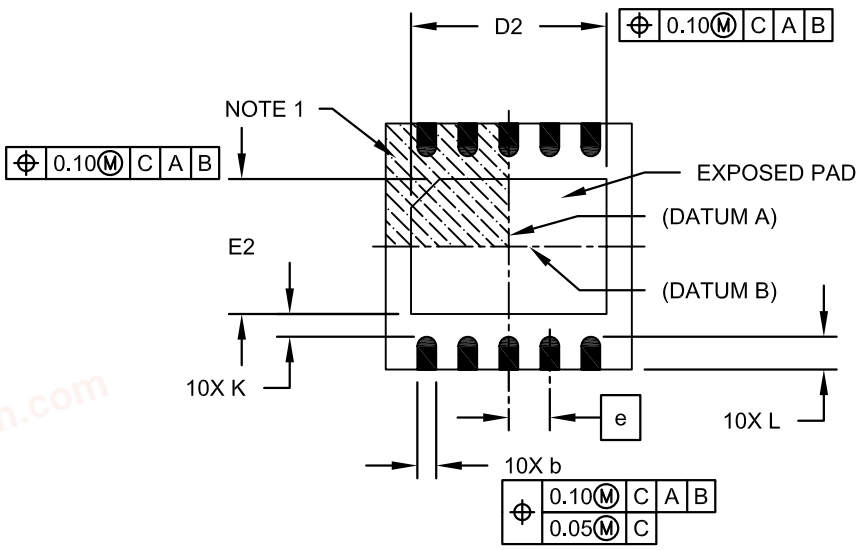
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



BOTTOM VIEW

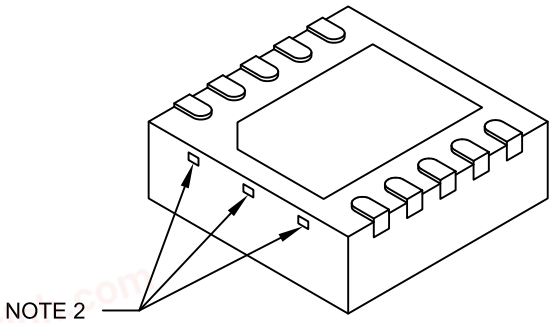
Microchip Technology Drawing No. C04-063C Sheet 1 of 2

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10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.15	2.35	2.45
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.40	1.50	1.75
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

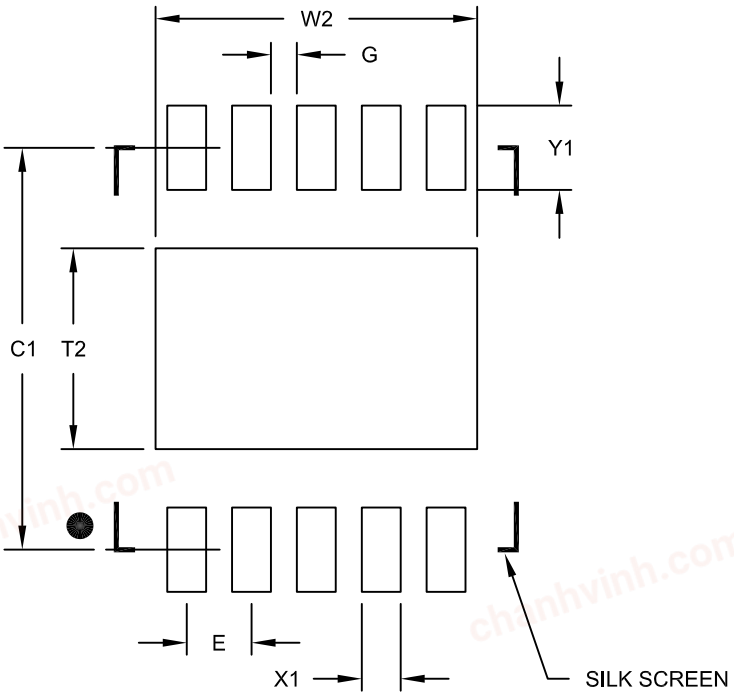
Microchip Technology Drawing No. C04-063C Sheet 2 of 2

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10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			2.48
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.65
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063B

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APPENDIX A: REVISION HISTORY

Revision A (July 2018)

- Original Release of this Document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X (1)	-	X	-	XX
	Device		Tape and Reel		Temperature Range		Package

Device:	CL88030	=	Sequential Linear LED Driver with 4 Taps
	CL88031	=	Sequential Linear LED Driver with 6 Taps
Tape and Reel Option	T	=	Tape and Reel
Temperature Range	E	=	-40°C to +125°C (Extended)
Package:	MF	=	Plastic Dual Flat, No Lead Package (DFN), 8-lead

Examples:

a) CL88030T-E/MF: Sequential Linear LED Driver with 4 Taps; Tape and Reel; 10LD DFN package

b) CL88031T-E/MF: Sequential Linear LED Driver with 6 Taps; Tape and Reel; 10LD DFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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