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AVR32SD20/28/32 Silicon Errata and Data Sheet Clarifications

AVR32SD20/28/32

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Introduction

The AVR32SD20/28/32 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002629), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR32SD20/28/32 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002629) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

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1. Silicon Issue Summary

Legend

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A1(1)	Rev. A2
ADC	False Overrun Detection	X	X
	Misleading Busy Status During Initialization Phase	X	X
TCD	Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used	X	X
USART	Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X	X

Note:

1. This revision is the initial release of the silicon.

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2. Silicon Errata Issues

2.1. Errata Details

- Erratum is not applicable.
X Erratum is applicable.

2.2. ADC - Analog-to-Digital Converter

2.2.1. False Overrun Detection

The first conversion after re-enabling the ADC can give a false overrun detection.

Work Around

Read the SAMPLE and RESULT registers before re-enabling the ADC.

Affected Silicon Revisions

Rev. A1	Rev. A2
X	X

2.2.2. Misleading Busy Status During Initialization Phase

When the ADC peripheral is enabled with LOWLAT = '0x1' in the CTRLA register, the initialization phase starts as expected, but the ADCBUSY bit in the STATUS register may be cleared too early. Any conversion started before the initialization phase is complete will be halted, regardless of the ADCBUSY bit. Once the initialization phase is completed, the ADCBUSY bit will operate correctly.

Work Around

Perform a dummy conversion and wait for the RESRDY or SAMPRDY flag in the INTFLAGS register to be set.

Affected Silicon Revisions

Rev. A1	Rev. A2
X	X

2.3. TCD - 12-Bit Timer/Counter Type D

2.3.1. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used

Halting TCD and waiting for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around

Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from 0 and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. A1	Rev. A2
X	X

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2.4. USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.4.1. Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. A1	Rev. A2
X	X

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3. Data Sheet Clarifications

Note the following typographical corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002629).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1. None

There are no known data sheet clarifications as of this publication date.

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4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1. Revision History

Doc. Rev.	Date	Comments
B	04/2026	• Added mask revision A2 • New errata: – ADC - False Overrun Detection – ADC - Misleading Busy Status During Initialization Phase
A	02/2025	Initial document release

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