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SAM D5x/E5x Family

SAM D5x/E5x Family Silicon Errata and Data Sheet Clarification

SAM D5x/E5x Family Errata

The SAM D5x/E5x family of devices that you have received conform functionally to the current Device Data Sheet (DS60001507A), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in **SAM D5x/E5x Family Silicon Device Identification**. The silicon issues are summarized in the Table of Contents following this section.

The errata described in this document will be addressed in future revisions of the SAM D5x/E5x family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. SAM D5x/E5x Family Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision (DID.REVISION[3:0])
		A
ATSAME54P19A	0x6184xx01	0x0
ATSAME54P20A	0x6184xx00	
ATSAME54N19A	0x6184xx03	
ATSAME54N20A	0x6184xx02	
ATSAME53N20A	0x6183xx02	
ATSAME53N19A	0x6183xx03	
ATSAME53J18A	0x6183xx06	
ATSAME53J19A	0x6183xx05	
ATSAME53J20A	0x6183xx04	
ATSAME51N19A	0x6181xx01	
ATSAME51N20A	0x6181xx00	
ATSAME51J18A	0x6181xx03	
ATSAME51J19A	0x6181xx02	
ATSAME51J20A	0x6181xx04	
ATSAMD51P20A	0x6006xx00	

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Part Number	Device Identification (DID[31:0])	Revision (DID.REVISION[3:0])
		A
ATSAMD51P19A	0x6006xx01	
ATSAMD51N19A	0x6006xx03	
ATSAMD51N20A	0x6006xx02	
ATSAMD51J18A	0x6006xx06	
ATSAMD51J19A	0x6006xx05	
ATSAMD51J20A	0x6006xx04	
ATSAMD51G18A	0x6006xx08	
ATSAMD51G19A	0x6006xx07	

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

Note: Refer to the **"Device Service Unit"** chapter in the current Device Data Sheet (DS60001507A) for a detailed information on Device Identification and Revision IDs for your specific device.

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1. Silicon Errata Issues

The following issues apply to the SAM D5x/E5x Family of devices.

1.1 Analog-to-Digital Converter (ADC)

1.1.1 ADC

The ADC SYNCBUSY.SWTRIG gets stuck to '1' after wake-up from Standby Sleep mode.

Workaround

Ignore the ADC SYNCBUSY.SWTRIG status when waking up from Sleep mode.

Affected Silicon Revisions

A							
X							

1.1.2 ADC

ADC TUE/INL/DNL performance is not guaranteed in the following scenarios:

- Sampling frequency is above 500 ksps
- ADC VREF is different from VDDANA

Workaround

None.

Affected Silicon Revisions

A							
X							

1.2 Analog Comparator (AC)

1.2.1 AC

Enabling Hysteresis (COMPCTRLn.HYSTEN = 0x1) changes the threshold voltage (VTH-), which may result in unexpected behavior of the Analog Comparator.

Workaround

None.

Affected Silicon Revisions

A							
X							

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1.3 Controller Area Network (CAN)

1.3.1 CAN

When edge filtering is activated (CCCR.EFBI = 1) and when the end of the integration phase coincides with a falling edge at the Rx input pin, it may occur that the CAN synchronizes itself incorrectly and does not correctly receive the first bit of the frame. In this case, the CRC will detect that the first bit was received incorrectly, it will rate the received FD frame as faulty, and an error frame will be send.

The issue only occurs when there is a falling edge at the Rx input pin (CAN_RX) within the last time quantum (tq) before the end of the integration phase. The last time quantum of the integration phase is at the sample point of the 11th recessive bit of the integration phase. When edge filtering is enabled, the bit timing logic of the CAN sees the Rx input signal delayed by the edge filtering. When the integration phase ends, edge filtering is automatically disabled. This affects the reset of the FD CRC registers at the beginning of the frame. The Classical CRC register is not affected, hence this issue does not affect the reception of Classical frames.

In CAN communication, the CAN module may enter an integrating state (either by resetting the CCCR.INIT or by protocol exception event) while a frame is active on the bus. In this case, the 11 recessive bits are counted between the acknowledge bit and the following start of frame. All nodes have synchronized at the beginning of the dominant acknowledge bit. This means that the edge of the following start of frame bit cannot fall on the sample point, hence the issue does not occur. The issue occurs only when the CAN is by local errors, mis-synchronized with regard to the other nodes.

Glitch filtering as specified in ISO 11898-1:2015 is fully functional.

Edge filtering was introduced for applications where the data bit time is at least 2-tq (of nominal bit time) long. In that case, edge filtering requires at least two consecutive dominant time quanta before the counter counting the 11 recessive bits for idle detection is restarted. This means edge filtering covers the theoretical case of occasional 1-tq long dominant spikes on the CAN bus that would delay idle detection. Repeated dominant spikes on the CAN bus would disturb all CAN communication, so the filtering to speed up idle detection would not help network performance.

When this rare event occurs, the CAN sends an error frame and the sender of the affected frame retransmits the frame. When the retransmitted frame is received, the CAN has left the integration phase and the frame will be received correctly. Edge filtering is only applied during the integration phase; it is never used during normal operation. Since the integration phase is very short with respect to "active communication time", the impact on total error frame rate is negligible. The issue has no impact on data integrity.

The CAN enters the integration phase under the following conditions:

- When CCCR.INIT is set to '0' after start-up
- After a protocol exception event (only when CCCR.PXHD = 0)

Scope:

The erratum is limited to FD frame reception when edge filtering is active (CCCR.EFBI = '1') and when the end of the integration phase coincides with a falling edge at the Rx input pin.

Effects:

The calculated CRC value does not match the CRC value of the received FD frame and the CAN module sends an error frame. After retransmission the frame is received correctly.

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Workaround
Disable edge filtering or wait on retransmission in the event that this rare event occurs.

Affected Silicon Revisions

A							
X							

1.3.2 CAN

When NBTP.NTSEG2 is configured to zero (Phase_Seg2(N) = 1), and when there is a pending transmission request, a dominant third bit of Intermission may cause the CAN to wrongly transmit the first identifier bit dominant instead of recessive, even if this bit was configured as '1' in the Tx Buffer Element of the CAN module.

Workaround
A phase buffer segment 2 of length '1' (Phase_Seg2(N) = 1) is not sufficient to switch to the first identifier bit after the sample point in Intermission where the dominant bit was detected.

The CAN protocol according to ISO 11898-1 defines that a dominant third bit of Intermission causes a pending transmission to be started immediately. The received dominant bit is handled as if the CAN has transmitted a Start-of-Frame (SoF) bit.

The ISO 11898-1 specifies the minimum configuration range for Phase_Seg2(N) to be 2..8 tq. Therefore, excluding a Phase_Seg2(N) of '1' will not affect CAN conformance.

Effects:

In case NBTP.NTSEG2 = 0, it may occur that the CAN transmits the first identifier bit dominant instead of recessive.

Update configuration range of NBTP.NTSEG2 from 0..127 tq to 1..127 tq in the CAN documentation.

Affected Silicon Revisions

A							
X							

1.4 Clock Failure Detector (CFD)

1.4.1 CFD

When the CFD is enabled for the XOSC/XOSC32K oscillator and the oscillator input signal is stuck at 1, the clock failure detection works correctly but the switch to the safe clock will fail.

Workaround
Two possible workarounds are:

1. If the main clock source itself comes from the XOSC/XOSC32K oscillator, the only workaround is indirect (i.e., using the WDT in firmware and switch to safe clock source in firmware at WDT reset).
2. Because the clock failure detection is functional, once the STATUS.CLKFAIL is set, and if the STATUS.CLKSW is not set, manually switch to safe clock from firmware by changing configurations of the generic clock generators that use the XOSC/XOSC32K oscillator as a clock source to use another source clock instead.

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Affected Silicon Revisions

A							
X							

1.5 Device

1.5.1 Device

The internal pull-up of the RESET pin is not functional.

Workaround

An external 100K pull-up must be added on the RESET pin.

Affected Silicon Revisions

A							
X							

1.5.2 Device

The detection of a debugger probe may fail if the "BOD33 Disable" fuse is cleared (i.e., BOD33 is enabled).

Workaround

To secure the detection of debugger probes, enable BOD33 using the SUPC.BOD33 register instead of the "BOD33 Disable" fuse. The "BOD33 Disable" fuse must be kept set.

Affected Silicon Revisions

A							
X							

1.5.3 Device

VBAT mode is not functional.

Workaround

None.

Affected Silicon Revisions

A							
X							

1.5.4 Device

When the internal reference is used with the DAC and ADC, their outputs become non-linear when the operating temperature is less than 0°C.

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Workaround
The internal reference must be used only for positive temperatures (i.e., above 0°C).

Affected Silicon Revisions

A							
X							

1.6 Device Service Unit (DSU)

1.6.1 DSU

DSU CRC32 may never complete when targeting NVM memory space while the NVM cache is disabled.

Workaround
Be sure to always enable the NVM cache when performing a DSU CRC32 request targeting the NVM memory space.

Affected Silicon Revisions

A							
X							

1.7 48 MHz Digital Frequency-Locked Loop (DFLL48M)

1.7.1 DFFL48M

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.

Workaround
Check that lockbits, DFLLLCKC and DFLLLCKF, in the OSCCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

Affected Silicon Revisions

A							
X							

1.7.2 DFFL48M

In Close Loop mode, the STATUS.DFLLRDY bit does not rise before lock fine occurs. Therefore, the information about DFLL ready to start Close Loop mode is not available.

Workaround
None.

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Affected Silicon Revisions

A							
X							

1.7.3 DFFL48M

If the DFLL is disabled and then re-enabled, the DFLLVAL.FINE value is ignored by the DFLL module, which will then start its lock fine process at another frequency.

Workaround

Before writing the final configuration in the DFLLCTRLB register, the DFLL module must be re-enabled in Open Loop mode to read and rewrite the DFLLVAL register.

1. `OSCCTRL->DFLLMUL.reg = X; // Write new DFLLMULL configuration`
2. `OSCCTRL.DFLLCTRLB.reg = 0; // Select Open loop configuration`
3. `OSCCTRL.DFLLCTRLA.bit.ENABLE = 1; // Enable DFLL`
4. `OSCCTRL.DFLLVAL.reg = OSCCTRL->DFLLVAL.reg; // Reload DFLLVAL register`
5. `OSCCTRL.DFLLCTRLB.reg = X; // Write final DFLL configuration`

Affected Silicon Revisions

A							
X							

1.8 Digital-to-Analog Converter (DAC)

1.8.1 DAC

In Differential mode the smoothing of the output signal is not fully functional. Smoothing works normally in Differential mode as long as the value of two consecutive data are both positive or negative. The behavior is incorrect when the data changes from positive to negative or vice versa.

Workaround

None.

Affected Silicon Revisions

A							
X							

1.8.2 DAC

The selection of VDDANA as the DAC reference in DAC.CTRLB.REFSEL is non-functional.

Workaround

The VDDANA must be connected externally to a VREF pin and DAC.CTRLB.VREFAU must be selected.

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Affected Silicon Revisions

A							
X							

1.8.3 DAC

No analog compare will be done on Comparator 0 (AC0) when using the DAC on negative input AIN1 and on Comparator 1 (AC1) when using the DAC on negative input AIN3.

Workaround

Use the internal VDD scaler.

Affected Silicon Revisions

A							
X							

1.8.4 DAC

If the Interpolation mode is enabled (with filter integrated to the DAC), the last data from the filter is missing, and therefore, the DAC final output value does not correspond to the DAC input value.

Although interrupt events are generated at the end of conversion (EOC), the EOC occurs before the final value from the filter and is of no use in the application.

Workaround

None.

Affected Silicon Revisions

A							
X							

1.9 Direct Memory Access Controller (DMAC)

1.9.1 DMAC

When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) may occur upon enabling a channel with no linked descriptor or the second descriptor (index 1) of the channel being enabled may be fetched by one of the already active channels using linked descriptors. These errors may occur when a channel is being enabled during the link request of another channel and if the channel number of the channel being enabled is lower than the channel already active.

Workaround

When enabling a channel while other channels using linked descriptors are already active, the channel number of the new channel to enable must be greater than the other channel numbers.

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Affected Silicon Revisions

A							
X							

1.10 Ethernet MAC (GMAC)

1.10.1 Ethernet Functionality in 64-pin Packages

Ethernet functionality in 64-pin packages is not available.

Workaround

None.

Affected Silicon Revisions

A							
X							

1.11 External Interrupt Controller (EIC)

1.11.1 EIC

When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K).

Workaround

None.

Affected Silicon Revisions

A							
X							

1.11.2 EIC

When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up.

Workaround

Use the asynchronous edge detection with debouncer enabled. It is recommended to set the DPRESCALER.PRESCALER and DPRESCALER.TICKON to have the lowest frequency possible. To reduce the power consumption, set the EIC GCLK frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL set).

Affected Silicon Revisions

A							
X							

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1.12 Fractional Digital Phase-Locked Loop (FDPLL)

1.12.1 FDPLL

When using a low frequency input clock on FDPLLn, several FDPLL unlocks may occur while the output frequency is stable.

Workaround

When using a low frequency input clock on FDPLLn, enable the lock bypass feature to avoid FDPLL unlocks.

Affected Silicon Revisions

A							
X							

1.12.2 FDPLL

When changing the FDPLL ratio in DPLLnRATIO register on-the-fly, STATUS.DPLLnLDRTO will not be set when the ratio update will be completed.

Workaround

Wait for the interruption flag INTFLAG.DPLLnLDRTO instead.

Affected Silicon Revisions

A							
X							

1.13 Non-Volatile Memory Controller (NVMCTRL)

1.13.1 NVMCTRL

NVM reads may be corrupted when mixing NVM reads with Page Buffer writes.

Workaround

Disable cache lines before writing to the Page Buffer when executing from NVM or reading data from NVM while writing to the Page Buffer. Cache lines are disabled by writing a one to CTRLA.CACHEDIS0 and CTRLA.CACHEDIS1.

Affected Silicon Revisions

A							
X							

1.13.2 NVMCTRL

The device does not start correctly under temperatures below -20°C.

Workaround

Reset the device (RESET pin) during power-up until VDDIO has reached 2V.

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A							
X							

1.13.3 NVMCTRL

Flash Write/Erase operations are not functional under temperatures below -20°C.

Workaround

VDDIO must be supplied at 2V minimum to guarantee Flash Write/Erase operations down to -40°C .

A							
X							

1.14 I/O Pin Controller (PORT)

1.14.1 PORT

PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB,...), do not generate a PAC protection error.

Workaround

None.

Affected Silicon Revisions

A							
X							

1.14.2 PORT Pull-Up/Pull-Down Resistor

The pull-down on PA24/PA25 are activated during power-up and when Sleep mode is OFF. On all other pins, except those in the VSWOUT cluster, the pull-up is activated during power-up and when Sleep mode is OFF.

Workaround

None.

Affected Silicon Revisions

A							
X							

1.15 Serial Communication Interface (SERCOM)

1.15.1 SERCOM

In USART Auto-baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

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Workaround
None.

Affected Silicon Revisions

A							
X							

1.15.2 SERCOM-I2C

SDAHOLD timing of the SERCOM-I2C does not match the value shown in the current device data sheet. The following table shows the specified and real values of SDA Hold timing.

Table -1. SDA Hold Timing

SDA Hold Time Value	Specified SDA Hold Time	Real SDA Hold Time
0x0	Disabled	Disabled
0x1	50 ns to 100 ns	20 ns to 40 ns
0x2	300 ns to 600 ns	100 ns to 250 ns
0x3	400 ns to 800 ns	150 ns to 350 ns

Workaround
None.

Affected Silicon Revisions

A							
X							

1.15.3 SERCOM

When 32-bit Extension mode is enabled and data to be sent is not in multiples of 4 bytes (which means the length counter must be enabled), additional bytes will be sent over the line.

Workarounds
Use any one of the following workarounds:

1. Write the Inter-Character Spacing bits (CTRLC.ICSPACE) to a non-zero-value.
2. Do not use length counter in firmware by keeping data to be sent is in multiples of 4 bytes.

Affected Silicon Revisions

A							
X							

1.15.4 SERCOM-UART

The TXINV and RXINV bits in the CTRLA register have inverted functionality.

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Workarounds
In software, interpret the TXINV bit as a functionality of RXINV, and conversely, interpret the RXINV bit as a functionality of TXINV.

Affected Silicon Revisions

A							
X							

1.16 Timer/Counter (TC)

1.16.1 TC

When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.

Workaround
Clear successively twice the STATUS.PERBUFV/STATUS.CCBUFx flag to ensure that the PERBUF/CCBUFx register value is restored before updating it.

Affected Silicon Revisions

A							
X							

1.17 Timer/Counter for Control Applications (TCC)

1.17.1 TCC

Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses, or shrink of left-aligned pulses.

Workaround
Do not use retrigger events or actions when the TCC module is configured in Dithering mode.

Affected Silicon Revisions

A							
X							

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2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001507A):

2.1 Analog-to-Digital (ADC) Characteristics

Operating Conditions

In *Table 54-23. Operating Conditions*, the following note pertaining to the V_{CMIN} parameter was omitted.

Note: Respect the input common mode voltage using the following equations (where VCM_IN is the input channel common mode voltage):
When CTRLC.R2R = 0:

- VCM_IN < 0.75*VREF
- VCM_IN > Maximum of (0, VREF-VDDANA-0.7, 1.25*VREF-VDDANA)

2.2 Ethernet MAC (GMAC)

IEEE 802.3AZ Energy Efficient Support

The Ethernet MAC supports IEEE 802.3AZ energy efficient standard. AF/PoE is an Ethernet PHY and application hardware dependent feature. The data sheet will be updated to cover this clarification.

2.3 SERCOM

Baud Rate Equations

In *Table 33-2. Baud Rate Equations*, the Asynchronous Fractional mode equation was omitted.

The following table shows the missing equation.

Table 1-1. Baud Rate Equations

Operating Mode	Condition	Baud Rate (Bits Per Second)	BAUD Register Value Calculation
Asynchronous Fractional	$f_{BAUD} \leq \frac{f_{ref}}{S}$	$f_{BAUD} = \frac{f_{ref}}{S(BAUD + (FP/8))}$	$BAUD = \frac{f_{REF}}{S \times f_{BAUD}} - \frac{FP}{8}$

SERCOM in SPI Mode Timing

In *Table 54-51. SPI Timing Characteristics and Requirements*, the maximum SPI clock frequency should be selected as the minimum of Reception and Transmission mode.

2.4 Packaging Information

TQFP 64-pin Package

The TQFP 64-pin package drawing was omitted from the data sheet.

A PDF of the TQFP 64-pin package, Microchip Drawing C04-085C, is available for download from the following URL:

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http://www.microchip.com/mymicrochip/filehandler.aspx?ddocname=en596496

2.5 Digital-to-Analog (DAC)

INL & DNL in Table 54-28

Table 54-28 has a note but it is omitted for INL and DNL symbols, this omitted note is shown below.

Note 1 : Specified in a restricted temperature range [0-85°C] when 1V internal reference is used.

INL & DNL in Table 54-29

Table 54-29 has a note but it is omitted for INL and DNL symbol, this omitted note is shown below

Note 1 : Specified only at Temp > 0°C when 1V internal reference is used.

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3. Appendix A: Revision History

Rev. A (7/2017)
Initial release of this document.

Rev. B (10/2017)
This revision includes the following additions:

Silicon Issues

- Ethernet Functionality in 64-pin Packages

Data Sheet Clarifications

- ADC Operating Conditions
- GMAC IEEE 802.3AZ Energy Efficient Support
- SERCOM Baud Rate Equations
- SERCOM in SPI Mode Timing
- TQFP 64-pin Package
- DAC Operating Conditions

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