chanhvinh.com

# ATSAMA5D27-WLSOM1

## SAMA5D27 Wireless SOM1 Data Sheet

Product Page Links

## Introduction

The Microchip SAMA5D27 Wireless System-On-Module 1 (ATSAMA5D27-WLSOM1) is a small single-sided SOM based on the high-performance System-in-Package (SiP) 32-bit Arm® Cortex®-A5 processor-based MPU SAMA5D27, 2 Gb LPDDR2-SDRAM running up to 500 MHz, and Wi-Fi® plus Bluetooth® (Wi-Fi/BT) Wireless module.

The ATSAMA5D27-WLSOM1 is built on a common set of proven Microchip components to reduce time to market by simplifying hardware design and software development.

The ATSAMA5D27-WLSOM1 also limits design rules of the main application board, reducing overall PCB complexity and cost. The ATSAMA5D27-WLSOM1 is delivered with a free Linux® distribution and bare metal C examples.

**Figure 1.** ATSAMA5D27-WLSOM1 Overview





© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 1. Features

- System-In-Package (ATSAMA5D27C-LD2G-CU) Including:
  - Arm Cortex-A5 processor-based SAMA5D27 MPU running up to 500 MHz
  - 2 Gbit LPDDR2-SDRAM
- On-Board Power Management Unit (MCP16502AC-E/S8B)
- 64 Mb Serial Quad I/O Flash Memory (SST26VF064BEUIT-104I/MF) with Embedded EUI-48™ and EUI-64™ MAC Addresses
- IEEE® 802.11 b/g/n Wi-Fi plus Bluetooth (Wi-Fi/BT) Module (ATWILC3000-MR110UA)
- 10Base-T/100Base-TX Ethernet PHY (KSZ8081RNAIA)
- ATECC608B-TNGTLS Secure Element
- MEMS Oscillators for Clock Generation
- 94 I/Os
- Up to 7 Tamper Pins
- One USB Device, one USB Host and one HSIC Interface
- Shutdown and Reset Control Pins
- Independent Power Supplies Available for Camera Sensor, for SD Card and for Backup Depending on Voltage Domains
- Operational Specifications:
  - Main operating voltage: 3.3V to 5.5V ± 5%
  - Temperature range: -40°C to 85°C
  - Integrated oscillators, internal voltage regulators
  - Multiple interfaces and I/Os for easy application development
- Package:
  - 40.8 x 40.8 mm module, pitch 0.8 mm, manually solderable for prototyping


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 2. Applications

- Industrial Control and Automation
- Smart Appliances
- Human Machine Interfaces (HMI)
- IoT Gateway
- Access Control Panels
- Security and Alarm Systems


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 3. Design Resources

## 3.1. Hardware Design Resources

As the SAMA5D27 System-in-Package (SiP) MPU embeds a DDR3L memory chip, most of the design complexity related to high-speed DDR interface routing is avoided when using the SAMA5D27-WLSOM1 System-On-Module.

For carrier board design, Microchip provides complete SAMA5D27-WLSOM1 System-On-Module schematics and PCB design files in Altium format (on request and under license agreement), enabling electrical simulations for high-speed interfaces such as MIPI, LVDS and USB, as well as mechanical evaluation/simulation. For signal integrity simulation, Microchip provides IBIS models of the SAMA5D27 SiP device.

## 3.2. Software Resources

Microchip Technology provides complete embedded Linux solutions for MPUs. For more information, refer to Linux® OS for MPUs.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 4. Reference Documents

**Table 4-1.** Reference Data Sheets

| Document Title | Available | Literature No. |
|---|---|---|
| KSZ8081RNA/RND | www.microchip.com/wwwproducts/en/KSZ8081 | DS00002199 |
| SAMA5D2 SIP | www.microchip.com/wwwproducts/en/ATSAMA5D27C-LD2G | DS60001484 |
| SST26VF064BEUI | www.microchip.com/wwwproducts/en/SST26VF064BEUI | DS20006138 |
| MCP16502 | www.microchip.com/wwwproducts/en/MCP16502 | DS20006275 |
| MIC841/2 | https://www.microchip.com/wwwproducts/en/MIC842 | DS20005758 |
| DSC60XXB | www.microchip.com/wwwproducts/en/DSC6000B | DS20006133 |
| DSC61XXB | www.microchip.com/wwwproducts/en/DSC6100B | DS20006155 |
| ATWILC3000-MR110UA | www.microchip.com/en-us/product/ATWILC3000 | DS70005327 |
| ATECC608B-TNGTLS | www.microchip.com/wwwproducts/en/ATECC608B-TNGTLS | DS40002250 |

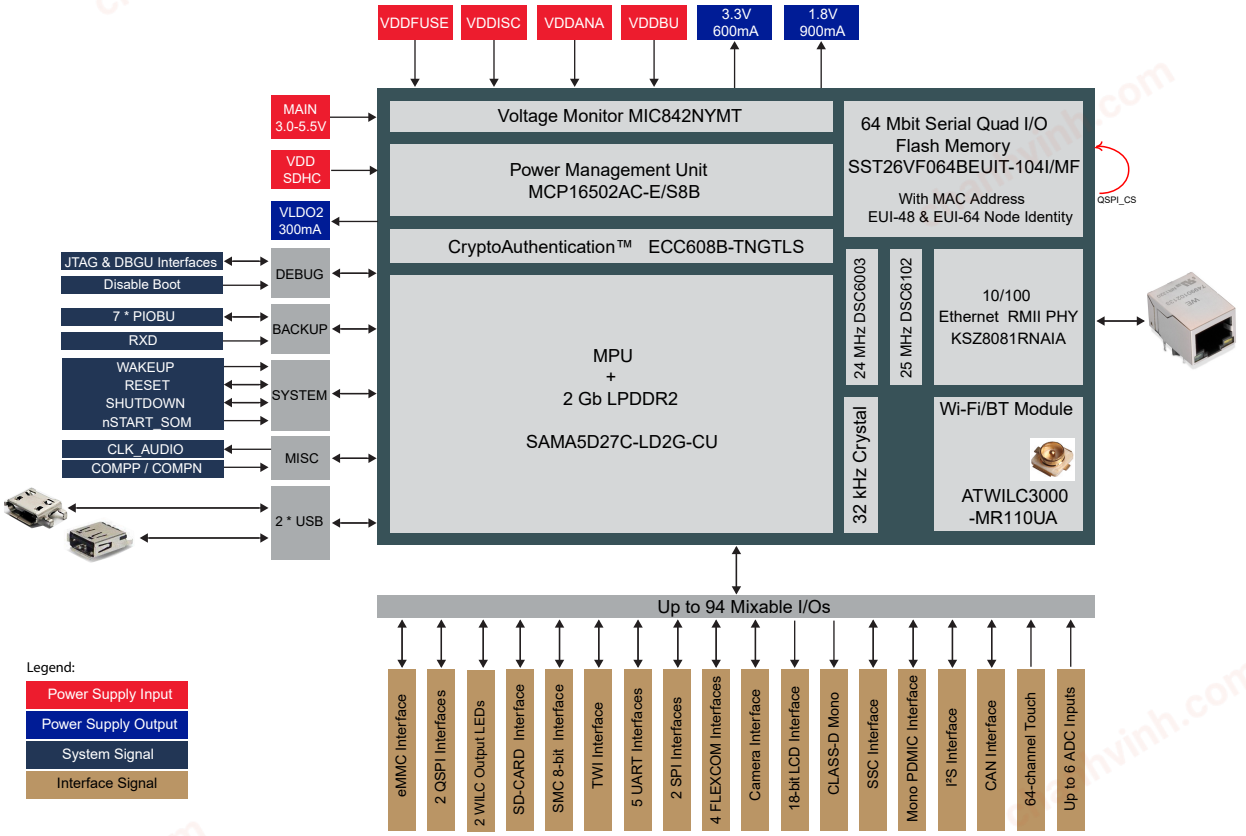

© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 5. Block Diagram

**Figure 5-1.** ATSAMA5D27-WLSOM1 Module Block Diagram





© 2026 Microchip Technology Inc. and its subsidiaries

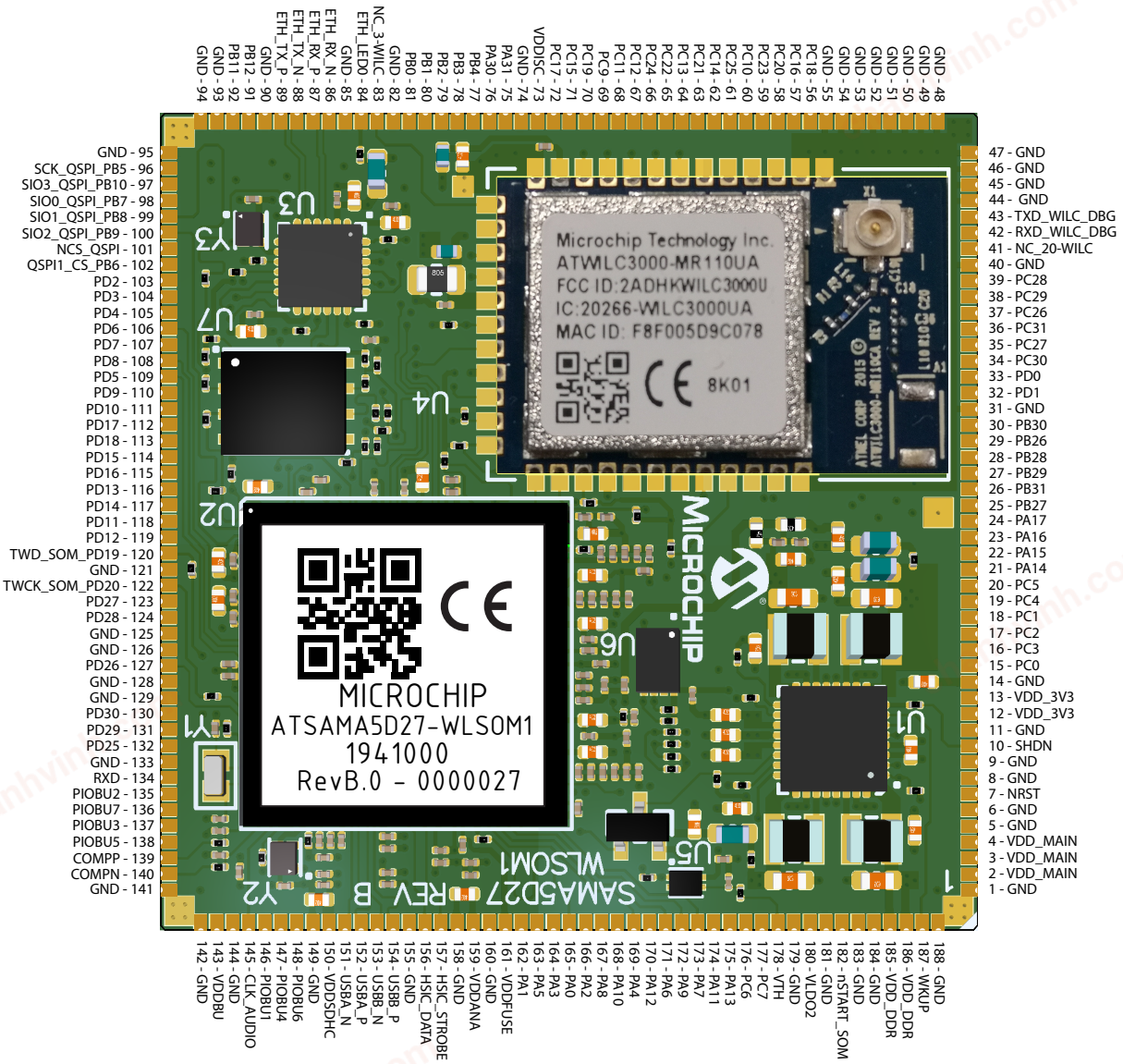
chanhvinh.com



# 6. Pinout

## 6.1. Pinout Overview

**Figure 6-1.** ATSAMA5D27-WLSOM1 Pin Assignment




## 6.2. Pin List

The following tables provide the ATSAMA5D27-WLSOM1 module pin description.

**Important:** Compared to SAMA5D2 Series devices, some PIO features are not listed. These features are used internally on the ATSAMA5D27-WLSOM1 and cannot be shared with other PIOs for use with features or for signal integrity.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



The device features several PIO controllers that multiplex the I/O lines of the peripheral set. The following PIOx Pin Description tables define how the I/O lines are multiplexed on the different PIO controllers. The "Reset State" column shows whether the PIO line resets in I/O mode or in Peripheral mode. If I/O is shown, the PIO line resets with the characteristics (input, output, pull-up or pull-down) indicated in this same column, so that the device is configured in a known state as soon as the reset is released. As a result, PIO_CFGR.FUNC resets to '0'. If a signal name is shown in the "Reset State" column, the PIO line is assigned to this function and PIO_CFGR.FUNC is not set to '0'. That is the case for pins controlling memories, in particular address lines, which require the pin to be driven as soon as the reset is released.

### 6.2.1. PIOA Pin Description

**Table 6-1.** PIOA Pin Description

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State[1] | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 165 | VDDSDHC | GPIO_EMMC | PA0 | I/O | – | – | A | SDMMC0_CK | I/O | 1 | PIO, I, PU, ST | |
| | | | | | | | B | QSPI0_SCK | O | 1 | | |
| | | | | | | | F | D0 | I/O | 2 | | |
| 162 | VDDSDHC | GPIO_EMMC | PA1 | I/O | – | – | A | SDMMC0_CMD | I/O | 1 | PIO, I, PU, ST | |
| | | | | | | | B | QSPI0_CS | O | 1 | | |
| | | | | | | | F | D1 | I/O | 2 | | |
| 166 | VDDSDHC | GPIO_EMMC | PA2 | I/O | – | – | A | SDMMC0_DAT0 | I/O | 1 | PIO, I, PU, ST | |
| | | | | | | | B | QSPI0_IO0 | I/O | 1 | | |
| | | | | | | | F | D2 | I/O | 2 | | |
| 164 | VDDSDHC | GPIO_EMMC | PA3 | I/O | – | – | A | SDMMC0_DAT1 | I/O | 1 | PIO, I, PU, ST | |
| | | | | | | | B | QSPI0_IO1 | I/O | 1 | | |
| | | | | | | | F | D3 | I/O | 2 | | |
| 169 | VDDSDHC | GPIO_EMMC | PA4 | I/O | – | – | A | SDMMC0_DAT2 | I/O | 1 | PIO, I, PU, ST | |
| | | | | | | | B | QSPI0_IO2 | I/O | 1 | | |
| | | | | | | | F | D4 | I/O | 2 | | |
| 163 | VDDSDHC | GPIO_EMMC | PA5 | I/O | – | – | A | SDMMC0_DAT3 | I/O | 1 | PIO, I, PU, ST | |
| | | | | | | | B | QSPI0_IO3 | I/O | 1 | | |
| | | | | | | | F | D5 | I/O | 2 | | |
| 171 | VDDSDHC | GPIO_EMMC | PA6 | I/O | – | – | A | SDMMC0_DAT4 | I/O | 1 | PIO, I, PU, ST | Note (3) |
| | | | | | | | B | QSPI1_SCK | O | 1 | | |
| | | | | | | | D | TIOA5 | I/O | 1 | | |
| | | | | | | | E | FLEXCOM2_IO0 | I/O | 1 | | |
| | | | | | | | F | D6 | I/O | 2 | | |
| 173 | VDDSDHC | GPIO_EMMC | PA7 | I/O | – | – | A | SDMMC0_DAT5 | I/O | 1 | PIO, I, PU, ST | Note (3) |
| | | | | | | | B | QSPI1_IO0 | I/O | 1 | | |
| | | | | | | | D | TIOB5 | I/O | 1 | | |
| | | | | | | | E | FLEXCOM2_IO1 | I/O | 1 | | |
| | | | | | | | F | D7 | I/O | 2 | | |
| 167 | VDDSDHC | GPIO_EMMC | PA8 | I/O | – | – | A | SDMMC0_DAT6 | I/O | 1 | PIO, I, PU, ST | Note (3) |
| | | | | | | | B | QSPI1_IO1 | I/O | 1 | | |
| | | | | | | | D | TCLK5 | I | 1 | | |
| | | | | | | | E | FLEXCOM2_IO2 | I/O | 1 | | |
| | | | | | | | F | NWE/NANDWE | O | 2 | | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Table 6-1.** PIOA Pin Description (continued)

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State(1) | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 172 | VDDSDHC | GPIO_EMMC | PA9 | I/O | – | – | A | SDMMC0_DAT7 | I/O | 1 | PIO, I, PU, ST | Note (3) |
| | | | | | | | B | QSPI1_IO2 | I/O | 1 | | |
| | | | | | | | D | TIOA4 | I/O | 1 | | |
| | | | | | | | E | FLEXCOM2_IO3 | O | 1 | | |
| | | | | | | | F | NCS3 | O | 2 | | |
| 168 | VDDSDHC | GPIO_EMMC | PA10 | I/O | – | – | A | SDMMC0_RSTN | O | 1 | PIO, I, PU, ST | Note (3) |
| | | | | | | | B | QSPI1_IO3 | I/O | 1 | | |
| | | | | | | | D | TIOB4 | I/O | 1 | | |
| | | | | | | | E | FLEXCOM2_IO4 | O | 1 | | |
| | | | | | | | F | A21/NANDALE | O | 2 | | |
| 174 | VDD_3V3 | GPIO | PA11 | I/O | – | – | A | SDMMC0_VDDSEL | O | 1 | PIO, I, PU, ST | |
| | | | | | | | B | QSPI1_CS | O | 1 | | |
| | | | | | | | D | TCLK4 | I | 1 | | |
| | | | | | | | F | A22/NANDCLE | O | 2 | | |
| 170 | VDD_3V3 | GPIO | PA12 | I/O | – | – | A | SDMMC0_WP | I | 1 | PIO, I, PU, ST | |
| | | | | | | | B | IRQ | I | 1 | | |
| | | | | | | | F | NRD/NANDOE | O | 2 | | |
| 175 | VDD_3V3 | GPIO | PA13 | I/O | – | – | A | SDMMC0_CD | I | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | E | FLEXCOM3_IO1 | I/O | 1 | | |
| 21 | VDD_3V3 | GPIO_QSPI | PA14 | I/O | – | – | A | SPI0_SPCK | I/O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | B | TK1 | I/O | 1 | | |
| | | | | | | | D | I2SMCK1 | O | 2 | | |
| | | | | | | | E | FLEXCOM3_IO2 | I/O | 1 | | |
| 22 | VDD_3V3 | GPIO | PA15 | I/O | – | – | A | SPI0_MOSI | I/O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | B | TF1 | I/O | 1 | | |
| | | | | | | | D | I2SCK1 | I/O | 2 | | |
| | | | | | | | E | FLEXCOM3_IO0 | I/O | 1 | | |
| 23 | VDD_3V3 | GPIO_IO | PA16 | I/O | – | – | A | SPI0_MISO | I/O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | B | TD1 | O | 1 | | |
| | | | | | | | D | I2SWS1 | I/O | 2 | | |
| | | | | | | | E | FLEXCOM3_IO3 | O | 1 | | |
| 24 | VDD_3V3 | GPIO_IO | PA17 | I/O | – | – | A | SPI0_NPCS0 | I/O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | I2SDI1 | I | 2 | | |
| | | | | | | | E | FLEXCOM3_IO4 | O | 1 | | |
| 76 | VDD_3V3 | GPIO | PA30 | I/O | – | – | C | SPI0_NPCS0 | I/O | 2 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | PWMH0 | O | 1 | | |
| 75 | VDD_3V3 | GPIO | PA31 | I/O | – | – | C | SPI0_MISO | I/O | 2 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | PWML0 | O | 1 | | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Notes:**

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. Fixed feature due to the WLSOM1 internal connection.
3. Limited feature compared to SAMA5D2 due to the WLSOM1 internal use of specific functionality, for example, QSPI, GMAC.
4. Limited feature compared to SAMA5D2 due to the use of a part of the functionality for other features in the WLSOM1, for example, GMAC, ISC, FLEXCOM, etc.

### 6.2.2. PIOB Pin Description

**Table 6-2.** PIOB Pin Description

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State(1) | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 81 | VDD_3V3 | GPIO | PB0 | I/O | – | – | C | SPI0_MOSI | I/O | 2 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | PWMH1 | O | 1 | | |
| 80 | VDD_3V3 | GPIO | PB1 | I/O | – | – | C | SPI0_SPCK | I/O | 2 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | PWML1 | O | 1 | | |
| | | | | | | | F | CLASSD_R0 | O | 1 | | |
| 79 | VDD_3V3 | GPIO | PB2 | I/O | – | – | D | PWMFI0 | I | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | F | CLASSD_R1 | O | 1 | | |
| 78 | VDD_3V3 | GPIO | PB3 | I/O | – | – | A | URXD4 | I | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | C | IRQ | I | 3 | | |
| | | | | | | | D | PWMEXTRG0 | I | 1 | | |
| | | | | | | | F | CLASSD_R2 | O | 1 | | |
| 77 | VDD_3V3 | GPIO | PB4 | I/O | – | – | A | UTXD4 | O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | C | FIQ | I | 4 | | |
| | | | | | | | F | CLASSD_R3 | O | 1 | | |
| 96 | VDD_3V3 | GPIO_QSPI | PB5 | I/O | – | – | A | TCLK2 | I | 1 | PIO, I, PU, ST | Note (3) Note (4) |
| | | | | | | | C | PWMH2 | O | 1 | | |
| | | | | | | | D | QSPI1_SCK | O | 2 | | |
| 102 | VDD_3V3 | GPIO | PB6 | I/O | – | – | A | TIOA2 | I/O | 1 | PIO, I, PU, ST | Note (3) Note (4) |
| | | | | | | | C | PWML2 | O | 1 | | |
| | | | | | | | D | QSPI1_CS | O | 2 | | |
| 98 | VDD_3V3 | GPIO_IO | PB7 | I/O | – | – | A | TIOB2 | I/O | 1 | PIO, I, PU, ST | Note (3) Note (4) |
| | | | | | | | C | PWMH3 | O | 1 | | |
| | | | | | | | D | QSPI1_IO0 | I/O | 2 | | |
| 99 | VDD_3V3 | GPIO_IO | PB8 | I/O | – | – | A | TCLK3 | I | 1 | PIO, I, PU, ST | Note (3) Note (4) |
| | | | | | | | C | PWML3 | O | 1 | | |
| | | | | | | | D | QSPI1_IO1 | I/O | 2 | | |
| 100 | VDD_3V3 | GPIO_IO | PB9 | I/O | – | – | A | TIOA3 | I/O | 1 | PIO, I, PU, ST | Note (3) Note (4) |
| | | | | | | | C | PWMFI1 | I | 1 | | |
| | | | | | | | D | QSPI1_IO2 | I/O | 2 | | |
| 97 | VDD_3V3 | GPIO_IO | PB10 | I/O | – | – | A | TIOB3 | I/O | 1 | PIO, I, PU, ST | Note (3) Note (4) |
| | | | | | | | C | PWMEXTRG1 | I | 1 | | |
| | | | | | | | D | QSPI1_IO3 | I/O | 2 | | |
| 92 | VDD_3V3 | GPIO | PB11 | I/O | – | – | C | URXD3 | I | 3 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | PDMIC_DAT0 | I/O | 2 | | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Table 6-2.** PIOB Pin Description (continued)

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State(1) | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 91 | VDD_3V3 | GPIO | PB12 | I/O | – | – | C | UTXD3 | O | 3 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | PDMIC_CLK0 | O | 2 | | |
| 29 | VDD_3V3 | GPIO | PB26 | I/O | – | – | C | URXD0 | I | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | PDMIC_DAT0 | I/O | 1 | | |
| | | | | | | | F | ISI_D0 | I | 3 | | |
| 25 | VDD_3V3 | GPIO | PB27 | I/O | – | – | C | UTXD0 | O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | PDMIC_CLK0 | O | 1 | | |
| | | | | | | | F | ISI_D1 | I | 3 | | |
| 28 | VDD_3V3 | GPIO | PB28 | I/O | – | – | C | FLEXCOM0_IO0 | I/O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | TIOA5 | I/O | 2 | | |
| | | | | | | | F | ISI_D2 | I | 3 | | |
| 27 | VDD_3V3 | GPIO | PB29 | I/O | – | – | C | FLEXCOM0_IO1 | I/O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | TIOB5 | I/O | 2 | | |
| | | | | | | | F | ISI_D3 | I | 3 | | |
| 30 | VDD_3V3 | GPIO | PB30 | I/O | – | – | C | FLEXCOM0_IO2 | I/O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | TCLK5 | I | 2 | | |
| | | | | | | | F | ISI_D4 | I | 3 | | |
| 26 | VDD_3V3 | GPIO | PB31 | I/O | – | – | C | FLEXCOM0_IO3 | O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | F | ISI_D5 | I | 3 | | |

**Notes:**

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. Fixed feature due to the WLSOM1 internal connection.
3. Limited feature compared to SAMA5D2 due to the WLSOM1 internal use of specific functionality, for example, QSPI, GMAC.
4. Limited feature compared to SAMA5D2 due to the use of a part of the functionality for other features in the WLSOM1, for example, GMAC, ISC, FLEXCOM, etc.

### 6.2.3. PIOC Pin Description

**Table 6-3.** PIOC Pin Description

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State (1) | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 15 | VDD_3V3 | GPIO | PC0 | I/O | – | – | C | FLEXCOM0_IO4 | O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | F | ISI_D6 | I | 3 | | |
| 18 | VDD_3V3 | GPIO | PC1 | I/O | – | – | C | CANTX0 | O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | SPI1_SPCK | I/O | 1 | | |
| | | | | | | | E | I2SCK0 | I/O | 1 | | |
| | | | | | | | F | ISI_D7 | I | 3 | | |
| 17 | VDD_3V3 | GPIO | PC2 | I/O | – | – | C | CANRX0 | I/O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | SPI1_MOSI | I/O | 1 | | |
| | | | | | | | E | I2SMCK0 | O | 1 | | |
| | | | | | | | F | ISI_D8 | I | 3 | | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Table 6-3.** PIOC Pin Description (continued)

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State [1] | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 16 | VDD_3V3 | GPIO | PC3 | I/O | – | – | C | TIOA1 | I/O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | SPI1_MISO | I/O | 1 | | |
| | | | | | | | E | I2SWS0 | I/O | 1 | | |
| | | | | | | | F | ISI_D9 | I | 3 | | |
| 19 | VDD_3V3 | GPIO | PC4 | I/O | – | – | C | TIOB1 | I/O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | SPI1_NPCS0 | I/O | 1 | | |
| | | | | | | | E | I2SDI0 | I | 1 | | |
| | | | | | | | F | ISI_PCK | I | 3 | | |
| 20 | VDD_3V3 | GPIO | PC5 | I/O | – | – | C | TCLK1 | I | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | SPI1_NPCS1 | O | 1 | | |
| | | | | | | | E | I2SDO0 | O | 1 | | |
| | | | | | | | F | ISI_VSYNC | I | 3 | | |
| 176 | VDD_3V3 | GPIO | PC6 | I/O | – | – | D | SPI1_NPCS2 | O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | F | ISI_HSYNC | I | 3 | | |
| 177 | VDD_3V3 | GPIO_CLK | PC7 | I/O | – | – | D | SPI1_NPCS3 | O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | F | ISI_MCK | O | 3 | | |
| 69 | VDDISC | GPIO | PC9 | I/O | – | – | A | FIQ | I | 3 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D0 | I | 1 | | |
| | | | | | | | D | TIOA4 | I/O | 2 | | |
| 60 | VDDISC | GPIO | PC10 | I/O | – | – | A | LCDDAT2 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D1 | I | 1 | | |
| | | | | | | | D | TIOB4 | I/O | 2 | | |
| | | | | | | | E | CANTX0 | O | 2 | | |
| 68 | VDDISC | GPIO | PC11 | I/O | – | – | A | LCDDAT3 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D2 | I | 1 | | |
| | | | | | | | D | TCLK4 | I | 2 | | |
| | | | | | | | E | CANRX0 | I | 2 | | |
| | | | | | | | F | A0/NBS0 | O | 2 | | |
| 67 | VDDISC | GPIO | PC12 | I/O | – | – | A | LCDDAT4 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D3 | I | 1 | | |
| | | | | | | | D | URXD3 | I | 1 | | |
| | | | | | | | E | TK0 | I/O | 2 | | |
| | | | | | | | F | A1 | O | 2 | | |
| 64 | VDDISC | GPIO | PC13 | I/O | – | – | A | LCDDAT5 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D4 | I | 1 | | |
| | | | | | | | D | UTXD3 | O | 1 | | |
| | | | | | | | E | TF0 | I/O | 2 | | |
| | | | | | | | F | A2 | O | 2 | | |
| 62 | VDDISC | GPIO | PC14 | I/O | – | – | A | LCDDAT6 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D5 | I | 1 | | |
| | | | | | | | E | TD0 | O | 2 | | |
| | | | | | | | F | A3 | O | 2 | | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Table 6-3.** PIOC Pin Description (continued)

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State [1] | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 71 | VDDISC | GPIO | PC15 | I/O | – | – | A | LCDDAT7 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D6 | I | 1 | | |
| | | | | | | | E | RD0 | I | 2 | | |
| | | | | | | | F | A4 | O | 2 | | |
| 57 | VDDISC | GPIO | PC16 | I/O | – | – | A | LCDDAT10 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D7 | I | 1 | | |
| | | | | | | | E | RK0 | I/O | 2 | | |
| | | | | | | | F | A5 | O | 2 | | |
| 72 | VDDISC | GPIO | PC17 | I/O | – | – | A | LCDDAT11 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D8 | I | 1 | | |
| | | | | | | | E | RF0 | I/O | 2 | | |
| | | | | | | | F | A6 | O | 2 | | |
| 56 | VDDISC | GPIO | PC18 | I/O | – | – | A | LCDDAT12 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D9 | I | 1 | | |
| | | | | | | | E | FLEXCOM3_IO2 | I/O | 2 | | |
| | | | | | | | F | A7 | O | 2 | | |
| 70 | VDDISC | GPIO | PC19 | I/O | – | – | A | LCDDAT13 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D10 | I | 1 | | |
| | | | | | | | E | FLEXCOM3_IO1 | I/O | 2 | | |
| | | | | | | | F | A8 | O | 2 | | |
| 58 | VDDISC | GPIO | PC20 | I/O | – | – | A | LCDDAT14 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_D11 | I | 1 | | |
| | | | | | | | E | FLEXCOM3_IO0 | I/O | 2 | | |
| | | | | | | | F | A9 | O | 2 | | |
| 63 | VDDISC | GPIO | PC21 | I/O | – | – | A | LCDDAT15 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_PCK | I | 1 | | |
| | | | | | | | E | FLEXCOM3_IO3 | O | 2 | | |
| | | | | | | | F | A10 | O | 2 | | |
| 65 | VDDISC | GPIO | PC22 | I/O | – | – | A | LCDDAT18 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_VSYNC | I | 1 | | |
| | | | | | | | E | FLEXCOM3_IO4 | O | 2 | | |
| | | | | | | | F | A11 | O | 2 | | |
| 59 | VDDISC | GPIO | PC23 | I/O | – | – | A | LCDDAT19 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_HSYNC | I | 1 | | |
| | | | | | | | F | A12 | O | 2 | | |
| 66 | VDDISC | GPIO_CLK | PC24 | I/O | – | – | A | LCDDAT20 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_MCK | O | 1 | | |
| | | | | | | | F | A13 | O | 2 | | |
| 61 | VDDISC | GPIO | PC25 | I/O | – | – | A | LCDDAT21 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | ISI_FIELD | I | 1 | | |
| | | | | | | | F | A14 | O | 2 | | |
| 37 | VDD_3V3 | GPIO | PC26 | I/O | – | – | A | LCDDAT22 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | D | CANTX1 | O | 1 | | |
| | | | | | | | F | A15 | O | 2 | | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Table 6-3.** PIOC Pin Description (continued)

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State (1) | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 35 | VDD_3V3 | GPIO | PC27 | I/O | – | – | A | LCDDAT23 | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | C | PCK1 | O | 2 | | |
| | | | | | | | D | CANRX1 | I/O | 1 | | |
| | | | | | | | F | A16 | O | 2 | | |
| 39 | VDD_3V3 | GPIO | PC28 | I/O | – | – | A | LCDPWM | O | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | B | FLEXCOM4_IO0 | I/O | 1 | | |
| | | | | | | | C | PCK2 | O | 1 | | |
| | | | | | | | F | A17 | O | 2 | | |
| 38 | VDD_3V3 | GPIO | PC29 | I/O | – | – | A | LCDDISP | O | 2 | PIO, I, PU, ST | |
| | | | | | | | B | FLEXCOM4_IO1 | I/O | 1 | | |
| | | | | | | | F | A18 | O | 2 | | |
| 34 | VDD_3V3 | GPIO | PC30 | I/O | – | – | A | LCDVSYNC | O | 2 | PIO, I, PU, ST | |
| | | | | | | | B | FLEXCOM4_IO2 | I/O | 1 | | |
| | | | | | | | F | A19 | O | 2 | | |
| 36 | VDD_3V3 | GPIO | PC31 | I/O | – | – | A | LCDHSYNC | O | 2 | PIO, I, PU, ST | |
| | | | | | | | B | FLEXCOM4_IO3 | O | 1 | | |
| | | | | | | | C | URXD3 | I | 2 | | |
| | | | | | | | F | A20 | O | 2 | | |

**Notes:**

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. Fixed feature due to the WLSOM1 internal connection.
3. Limited feature compared to SAMA5D2 due to the WLSOM1 internal use of specific functionality, for example, QSPI, GMAC.
4. Limited feature compared to SAMA5D2 due to the use of a part of the functionality for other features in the WLSOM1, for example, GMAC, ISC, FLEXCOM, etc.

### 6.2.4. PIOD Pin Description

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State(1) | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 33 | VDD_3V3 | GPIO_CLK | PD0 | I/O | – | – | A | LCDPCK | O | 2 | PIO, I, PU, ST | |
| | | | | | | | B | FLEXCOM4_IO4 | O | 1 | | |
| | | | | | | | C | UTXD3 | O | 2 | | |
| | | | | | | | D | GTSUCOMP | O | 2 | | |
| | | | | | | | F | A23 | O | 2 | | |
| 32 | VDD_3V3 | GPIO | PD1 | I/O | – | – | A | LCDDEN | O | 2 | PIO, I, PU, ST | |
| | | | | | | | D | GRXCK | I | 2 | | |
| | | | | | | | F | A24 | O | 2 | | |
| 103 | VDD_3V3 | GPIO_CLK | PD2 | I/O | – | – | A | URXD1 | I | 1 | PIO, I, PU, ST | |
| | | | | | | | D | GTXER | O | 2 | | |
| | | | | | | | E | ISI_MCK | O | 2 | | |
| | | | | | | | F | A25 | O | 2 | | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**PIOD Pin Description** (continued)

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State[1] | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 104 | VDDANA | GPIO_AD | PD3 | I/O | PTC_ROW0 | – | A | UTXD1 | O | 1 | PIO, I, PU, ST | |
| | | | | | | | B | FIQ | I | 2 | | |
| | | | | | | | D | GCRS | I | 2 | | |
| | | | | | | | E | ISI_D11 | I | 2 | | |
| | | | | | | | F | NWAIT | I | 2 | | |
| 105 | VDDANA | GPIO_AD | PD4 | I/O | PTC_ROW1 | – | B | URXD2 | I | 1 | PIO, I, PU, ST | Note (3) |
| | | | | | | | D | GCOL | I | 2 | | |
| | | | | | | | E | ISI_D10 | I | 2 | | |
| | | | | | | | F | NCS0 | O | 2 | | |
| 109 | VDDANA | GPIO_AD | PD5 | I/O | PTC_ROW2 | – | B | UTXD2 | O | 1 | PIO, I, PU, ST | Note (3) |
| | | | | | | | D | GRX2 | I | 2 | | |
| | | | | | | | E | ISI_D9 | I | 2 | | |
| | | | | | | | F | NCS1 | O | 2 | | |
| 106 | VDDANA | GPIO_AD | PD6 | I/O | PTC_ROW3 | – | A | TCK | I | 2 | PIO, I, PU, ST | Note (3) |
| | | | | | | | D | GRX3 | I | 2 | | |
| | | | | | | | E | ISI_D8 | I | 2 | | |
| | | | | | | | F | NCS2 | O | 2 | | |
| 107 | VDDANA | GPIO_AD | PD7 | I/O | PTC_ROW4 | – | A | TDI | I | 2 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | GTX2 | O | 2 | | |
| | | | | | | | E | ISI_D0 | I | 2 | | |
| | | | | | | | F | NWR1/NBS1 | O | 2 | | |
| 108 | VDDANA | GPIO_AD | PD8 | I/O | PTC_ROW5 | – | A | TDO | O | 2 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | GTX3 | O | 2 | | |
| | | | | | | | E | ISI_D1 | I | 2 | | |
| | | | | | | | F | NANDRDY | I | 2 | | |
| 110 | VDDANA | GPIO_AD | PD9 | I/O | PTC_ROW6 | – | A | TMS | I | 2 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | GTXCK | O | 2 | | |
| | | | | | | | E | ISI_D2 | I | 2 | | |
| 111 | VDDANA | GPIO_AD | PD10 | I/O | PTC_ROW7 | – | A | NTRST | I | 2 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | GTXEN | O | 2 | | |
| | | | | | | | E | ISI_D3 | I | 2 | | |
| 118 | VDDANA | GPIO_AD | PD11 | I/O | PTC_COL0 | – | A | TIOA1 | I/O | 3 | PIO, I, PU, ST | Note (4) |
| | | | | | | | B | PCK2 | O | 2 | | |
| | | | | | | | D | GRXDV | I | 2 | | |
| | | | | | | | E | ISI_D4 | I | 2 | | |
| 119 | VDDANA | GPIO_AD | PD12 | I/O | PTC_COL1 | – | A | TIOB1 | I/O | 3 | PIO, I, PU, ST | Note (4) |
| | | | | | | | B | FLEXCOM4_IO0 | I/O | 2 | | |
| | | | | | | | D | GRXER | I | 2 | | |
| | | | | | | | E | ISI_D5 | I | 2 | | |
| 116 | VDDANA | GPIO_AD | PD13 | I/O | PTC_COL2 | – | A | TCLK1 | I | 3 | PIO, I, PU, ST | Note (4) |
| | | | | | | | B | FLEXCOM4_IO1 | I/O | 2 | | |
| | | | | | | | D | GRX0 | I | 2 | | |
| | | | | | | | E | ISI_D6 | I | 2 | | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**PIOD Pin Description** (continued)

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State[1] | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | | |
| 117 | VDDANA | GPIO_AD | PD14 | I/O | PTC_COL3 | – | A | TCK | I | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | B | FLEXCOM4_IO2 | I/O | 2 | | |
| | | | | | | | D | GRX1 | I | 2 | | |
| | | | | | | | E | ISI_D7 | I | 2 | | |
| 114 | VDDANA | GPIO_AD | PD15 | I/O | PTC_COL4 | – | A | TDI | I | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | B | FLEXCOM4_IO3 | O | 2 | | |
| | | | | | | | D | GTX0 | O | 2 | | |
| | | | | | | | E | ISI_PCK | I | 2 | | |
| 115 | VDDANA | GPIO_AD | PD16 | I/O | PTC_COL5 | – | A | TDO | O | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | B | FLEXCOM4_IO4 | O | 2 | | |
| | | | | | | | D | GTX1 | O | 2 | | |
| | | | | | | | E | ISI_VSYNC | I | 2 | | |
| 112 | VDDANA | GPIO_AD | PD17 | I/O | PTC_COL6 | – | A | TMS | I | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | GMDC | O | 2 | | |
| | | | | | | | E | ISI_HSYNC | I | 2 | | |
| 113 | VDDANA | GPIO_AD | PD18 | I/O | PTC_COL7 | – | A | NTRST | I | 1 | PIO, I, PU, ST | Note (4) |
| | | | | | | | D | GMDIO | I/O | 2 | | |
| | | | | | | | E | ISI_FIELD | I | 2 | | |
| 120 | VDDANA | GPIO_AD | PD19 | I/O | – | – | B | TWD1 | I/O | 3 | PIO, I, PU, ST | Note (2) |
| 122 | VDDANA | GPIO_AD | PD20 | I/O | – | – | B | TWCK1 | I/O | 3 | PIO, I, PU, ST | Note (2) |
| 132 | VDDANA | GPIO_AD | PD25 | I/O | AD6 | – | A | SPI1_SPCK | O | 3 | PIO, I, PU, ST | |
| 127 | VDDANA | GPIO_AD | PD26 | I/O | AD7 | – | A | SPI1_MOSI | I/O | 3 | PIO, I, PU, ST | |
| | | | | | | | C | FLEXCOM2_IO0 | I/O | 2 | | |
| 123 | VDDANA | GPIO_AD | PD27 | I/O | AD8 | – | A | SPI1_MISO | I/O | 3 | PIO, I, PU, ST | |
| | | | | | | | B | TCK | I | 3 | | |
| | | | | | | | C | FLEXCOM2_IO1 | I/O | 2 | | |
| 124 | VDDANA | GPIO_AD | PD28 | I/O | AD9 | – | A | SPI1_NPCS0 | I/O | 3 | PIO, I, PU, ST | |
| | | | | | | | B | TDI | I | 3 | | |
| | | | | | | | C | FLEXCOM2_IO2 | I/O | 2 | | |
| 131 | VDDANA | GPIO_AD | PD29 | I/O | AD10 | – | A | SPI1_NPCS1 | O | 3 | PIO, I, PU, ST | Note (3) |
| | | | | | | | B | TDO | O | 3 | | |
| | | | | | | | C | FLEXCOM2_IO3 | O | 2 | | |
| | | | | | | | D | TIOA3 | I/O | 3 | | |
| 130 | VDDANA | GPIO_AD | PD30 | I/O | AD11 | – | A | SPI1_NPCS2 | O | 3 | PIO, I, PU, ST | Note (3) |
| | | | | | | | B | TMS | I | 3 | | |
| | | | | | | | C | FLEXCOM2_IO4 | O | 2 | | |
| | | | | | | | D | TIOB3 | I/O | 3 | | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Notes:**

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. Fixed feature due to the WLSOM1 internal connection.
3. Limited feature compared to SAMA5D2 due to the WLSOM1 internal use of specific functionality, for example, QSPI, GMAC.
4. Limited feature compared to SAMA5D2 due to the use of a part of the functionality for other features in the WLSOM1, for example, GMAC, ISC, FLEXCOM, etc.

### 6.2.5. System Pins Description

**Table 6-4.** System Pins Description

| Pin No. | Pin Name | Power Rail | Description |
|---|---|---|---|
| 145 | CLK_AUDIO | VDD_3V3 | Audio Main System Bus Clock Frequency Output |
| 151 | USBA_N | VDD_3V3 | USB Device High-Speed Data - |
| 152 | USBA_P | VDD_3V3 | USB Device High-Speed Data + |
| 157 | HSIC_STROBE | VDDHSIC (1.2V) | USB High-Speed Inter-Chip Strobe |
| 156 | HSIC_DATA | VDDHSIC (1.2V) | USB High-Speed Inter-Chip Data |
| 153 | USBB_N | VDD_3V3 | USB Host Port B High-Speed Data - |
| 154 | USBB_P | VDD_3V3 | USB Host Port B High-Speed Data + |
| 7 | NRST | VDDBU | Module Reset<br>A 100 kOhm pull-up must be provided by the host board |
| 140 | COMPN | VDDBU | External Analog Data Input |
| 139 | COMPP | VDDBU | External Analog Data Input |
| 146 | PIOBU1 | VDDBU | Tamper I/O #1 |
| 135 | PIOBU2 | VDDBU | Tamper I/O #2 |
| 137 | PIOBU3 | VDDBU | Tamper I/O #3 |
| 147 | PIOBU4 | VDDBU | Tamper I/O #4 |
| 138 | PIOBU5 | VDDBU | Tamper I/O #5 |
| 148 | PIOBU6 | VDDBU | Tamper I/O #6 |
| 136 | PIOBU7 | VDDBU | Tamper I/O #7 |
| 134 | RXD | VDDBU | RXLP Receive Data Input |
| 10 | SHDN | VDDBU | Shutdown Control |
| 187 | WKUP | VDDBU | Module Wake-Up<br>A 100 kOhm pull-up to VDDBU must be provided by the host board |
| 178 | VTH | VDD_MAIN | Low Voltage Threshold Detection Input |
| 101 | NCS_QSPI | VDD_3V3 | Embedded QSPI Chip Select Input |
| 83 | NC | – | Not connected |
| 41 | NC | – | Not connected |
| 89 | ETH_TX_P | – | Physical Transmit Signal (+ differential) |
| 88 | ETH_TX_N | – | Physical Transmit Signal (– differential) |
| 87 | ETH_RX_P | – | Physical Receive Signal (+ differential) |
| 86 | ETH_RX_N | – | Physical Receive Signal (– differential) |
| 84 | ETH_LED0 | VDD_3V3 | Programmable LED0 Output |
| 182 | nSTART_SOM | VDD_MAIN | Module Start-Up Control Input |
| 42 | RXD_WILC_DBG | VDD_3V3 | Used for Radio Debug. UART RXD |
| 43 | TXD_WILC_DBG | VDD_3V3 | Used for Radio Debug. UART TXD |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



### 6.2.6. Power Pins Description

**Table 6-5.** Power Pins Description

| Pin No. | Pin Name | Power Rail | Type | Description |
|---|---|---|---|---|
| 1, 5, 6, 8, 9, 11, 14, 31, 40, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 74, 82, 85, 90, 93, 94, 95, 121, 125, 126, 129, 133, 141, 142, 144, 128, 149, 155, 158, 160, 179, 181, 183, 184, 188 | GND | GND | GND | Ground |
| 159 | VDDANA | VDDANA | I | Analog Voltage Input |
| 143 | VDDBU | VDDBU | I | Backup Voltage Input |
| 161 | VDDFUSE | VDDFUSE | I | VDDFUSE Voltage Input |
| 73 | VDDISC | VDDISC | I | VDDISC Voltage Input |
| 2, 3, 4 | VDD_MAIN | VDD_MAIN | I | Main Input Voltage |
| 12, 13 | VDD_3V3 | VDD_3V3 | O | 3.3V Voltage Output |
| 180 | VLDO2 | VLDO2 | O | VLDO2 Output Voltage |
| 150 | VDDSDHC | VDDSDHC | I | VDDSDHC Input Voltage |
| 185, 186 | VDD_DDR | VDD_DDR | O | 1.8V Output Voltage |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 7. Functional Description

## 7.1. MPU and Memory Subsystem

### 7.1.1. SAMA5D27 System-In-Package

The SAMA5D27 System-In-Package (SiP) (ATSAMA5D27C-LD2G-CU) integrates the ARM Cortex-A5 processor-based SAMA5D2 MPU with 2 Gbit LPDDR2-SDRAM in a single package.

By combining the high-performance, ultra-low power SAMA5D2 with LPDDR2-SDRAM in a single package, PCB routing complexity, area and number of layers is reduced. This makes board design easier and lowers the overall cost of the bill of materials. Board design is more robust by facilitating design for EMI, ESD and signal integrity.

For more information about the SiP, see Reference Documents. The sole reference documents for product information on the SAMA5D2 and the LPDDR2-SDRAM memory are provided in this section.

The ATSAMA5D27C-LD2G-CU is available in a 361-ball TFBGA package.

The Microchip SAMA5D27 System-On-Module (SOM) provides global system Reset (NRST) and Shutdown (SHDN) pins to the application board.

- The NRST signal is an input/output pin generated by the internal Power Management Unit (MCP16502) in conjunction with power sequence timing. It is used to reset the internal microcontroller, the Ethernet transceiver and the rest of the customer application board. It can then be forced externally in case of a system crash.
- The SHDN pin is an output pin managed by the software application. In an application case, the pin switches on/off the external main supply VDD_MAIN.

### 7.1.2. MPU Clocks

Two clock sources are necessary for the module microcontroller:

- 24-MHz main oscillator for the SAMA5D27 MPU
- 32.768-kHz oscillator for slow clock oscillator input and embedded RTC of the SAMA5D27 MPU

The 24-MHz clock is generated by a Microchip ultra-low power MEMS oscillator DSC6003HI2B-024.0000T. It delivers a 24-MHz clock to the SAMA5D27 with an ultra-low power consumption of about 1.3 mA in Active mode.

For more information about the MEMS DSC60XXB, see Reference Documents. This section lists the sole reference documents for product information on the clock generation of the Microchip SAMA5D27 SOM.

The 24-MHz clock can be enabled/disabled as required by the application through the SAMA5D27 PD23 GPIO.

- By default, as the GPIO is in Input Pull-Up at reset, the clock is enable.
- To disable the clock, the GPIO must be forced to "0" logic.

The 32-kHz clock is generated by a small size crystal. It delivers an accurate 32-kHz clock to the SAMA5D27 MPU for its embedded RTC.

### 7.1.3. Power Management Unit

The MCP16502 is a full-featured Power Management Integrated Circuit (PMIC), cost- and size-optimized for Microchip MPU devices.

The Microchip SAMA5D27 SOM is supplied by an external 5V supply (VDD_MAIN) and generates its own internal supplies by interfacing with the Microchip MCP16502 Power Management Unit.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



The MCP16502 integrates four DC-DC buck regulators used for system supplying and two auxiliary LDOs for customer purposes.

- All buck channels can support loads up to 1A. All bucks are 100% duty cycle capable.
  - DCDC1 set @ 3.3 V supplies all pads of the embedded devices. This power rail offers a 600-mA load to customer applications through pins 12 and 13 (VDD_3V3).
  - DCDC2 set @ 1.2V supplies the LPDDR2 I/O memory. It is used internally only.
  - DCDC3 set @ 1.2V supplies the core of the microcontroller. It is used internally only.
  - DCDC4 set @ 1.8V supplies the LPDDR2 Core memory. It is used internally only.
- One 300 mA LDO set @ 3.3V internally is provided to supply Radio Power Amplifier of the ATWILC3000 module.
- One 300 mA LDO is provided so that sensitive analog loads can be supported. The LDO output voltage, named VLDO2 (accessible through pin 180), is disabled by default at power-up. Output voltage values are set through an I²C interface access after system initialization.

The default power channel sequencing is built-in, according to the requirements of the Microchip MPU device.

The MCP16502 features a low no-load operational quiescent current, and draws less than 10 uA in full shutdown.

Active discharge resistors are provided on each output. All buck channels support safe start-up into pre-biased outputs.

The MCP16502 is available in a 32-pin 5 mm x 5 mm VQFN package with an operating junction temperature range from –40°C to +125°C. It is AEC-Q100 Grade 2 ($T_{AMB}$=105°C) qualified.

The LPM pin of the Microchip SAMA5D27 System-On-Module, combined with HPM and PWRHLD (also named SHDN) pin status of the MCP16502 PMIC, define different power states which are illustrated in the table below.
**Note:** HPM is forced to “0” by hardware, since the high-performance feature of the MCP16502 PMIC is not supported by the SAMA5D27 SIP MPU device. For more information, refer to the MCP16502 data sheet (see Reference Documents).

**Table 7-1.** MCP16502 Default Power States

| PWRHLD | LPM | HPM | Buck1 | Buck2 | Buck3 | Buck4 | LDO1 | LDO2 | nRST | Power State (1) |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Off | Off | Off | Off | Off | Off | Low | Off |
| 0 | 1 | 0 | Off | On(2) | Off | On(2) | Off | Off | Low | Hibernate mode |
| 1 | 1 | 0 | On(2) | On(2) | On(2) | On(2) | On | Off | HiZ | Low-Power mode |
| 1 | 0 | 0 | On(3) | On(3) | On(3) | On(3) | On | Off | HiZ | Active mode |

**Notes:**

1. Only allowed modes are listed. If the PWRHLD/LPM/HPM combination is not listed, then the mode is not allowed.
2. In this mode, the DCDC is configured in Automatic Pulse-Frequency Modulation (Auto-PFM) mode.
3. In this mode, the DCDC is configured in Force Pulse-Width Modulation (FPWM) mode.

For more information about the use of the MCP16502 PMIC LPM feature, refer to the MCP16502 data sheet (see Reference Documents).

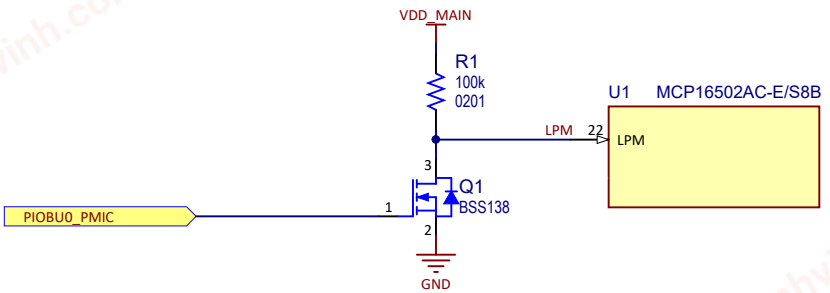
The LPM pin is controlled internally by PIOBU0 pin, as shown in the figure below.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-1.** PIOBU0 PMIC




### 7.1.4. SQI Memory

#### 7.1.4.1. Description and Schematic

The ATSAMA5D27-WLSOM1 embeds the SST26VF064BEUIT-104I/MF, a 64 Mb Serial Quad I/O Flash memory.

The SST26VF064BEUIT-104I/MF SQI features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package.

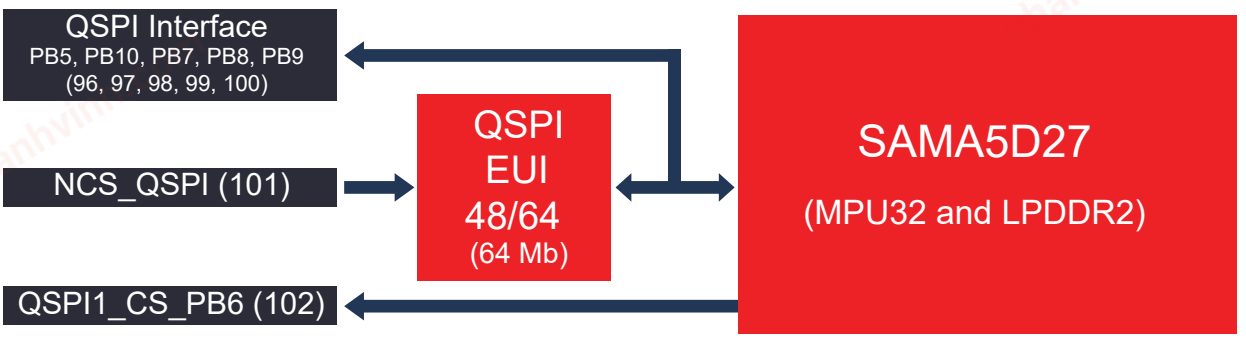
The SST26VF064BEUIT-104I/MF also embeds EUI-48 and EUI-64 MAC addresses.

The SST26VF064BEUIT-104I/MF is available in 8-lead WDFN package with 6 mm × 5 mm dimensions.

For more information, refer to the product web page.

It is possible to deselect the Chip Enable of the embedded QSPI to use an external one. In this case, the NCS_QSPI pin must be left floating and the signal QSPI1_CS_PB6 must be connected to an external QSPI Chip Select.

**Figure 7-2.** QSPI Memory Block Diagram




#### 7.1.4.2. MAC Address

The SST26VF064BEUI is pre-programmed at the factory with globally unique EUI-48 and EUI-64 node identifiers. The addresses are located in the Serial Flash Discoverable Parameters (SFDP) table and accessible via the SFDP read instruction.

The 6-byte EUI-48 address value of the SST26VF064BEUI is stored in the SFDP table at address locations 0x261 through 0x266.

The 8-byte EUI-64 address value of the SST26VF064BEUI is stored in the SFDP table at address locations 0x268 through 0x26F.

For more information, refer to the product web page.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

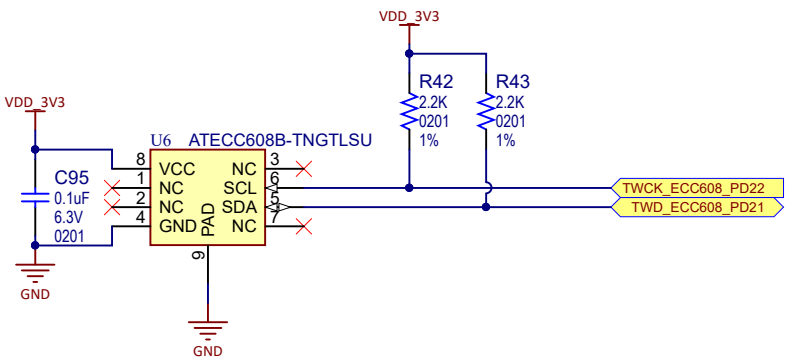


### 7.1.5. Secure Element

The Microchip ATECC608B-TNGTLS is the Trust&GO secure element part of the Trust Platform for the CryptoAuthentication family. The device comes pre-configured and pre-provisioned with default thumbprint certificates and key. The cloud infrastructure, whether it is a public or private network, must accommodate device authentication relying only on the thumbprint certificate from the ATECC608B-TNGTLS. This secure element integrates ECDH (Elliptic Curve Diffie Hellman) security protocol - an ultra-secure method to provide key agreement for encryption/decryption - along with ECDSA (Elliptic Curve Digital Signature Algorithm) sign-verify authentication for the Internet of Things (IoT) market, including home automation, industrial networking, medical, retail or any TLS connected networks.

For more information, refer to the product web page.

**Figure 7-3.** ECC608B Secure Element Schematic




## 7.2. Power Management

### 7.2.1. Power Architecture

Basic operation of the ATSAMA5D27-WLSOM1 requires a +5.0V input voltage supply and a VDDBU (+1.65V to +3.6V) input voltage supply, generally ensured by a backup battery. +5.0V power is supplied to the VDD_MAIN domain.

**CAUTION** As a general design rule, it is recommended to connect all input supply pins, except VDDFUSE which must be connected to GND by a 100 Ohms resistor if not used, to your power supply and at least a matching number of ground (GND) pins. For the best EMI performance, it is recommended to connect ALL ground pins of the ATSAMA5D27-WLSOM1 module to a solid ground plane.

Power-on is controlled through the nSTART_SOM signal. This signal must be provided by the host board; for example, via an automated reset controller or a push-button.

The ATSAMA5D27-WLSOM1 module can operate from a single voltage supply (VDD_MAIN) with a value comprised between +3.0V and +5.5V and, with the MCP16502 PMIC device, internally generates the voltage supplies required by the SAMA5D2 processor and on-board components.

The PMIC on-board switching regulators generate the 3.3V, 1.20V, 1.25V and 1.8V voltage supplies required by the SAMA5D27 processor and on-board components.

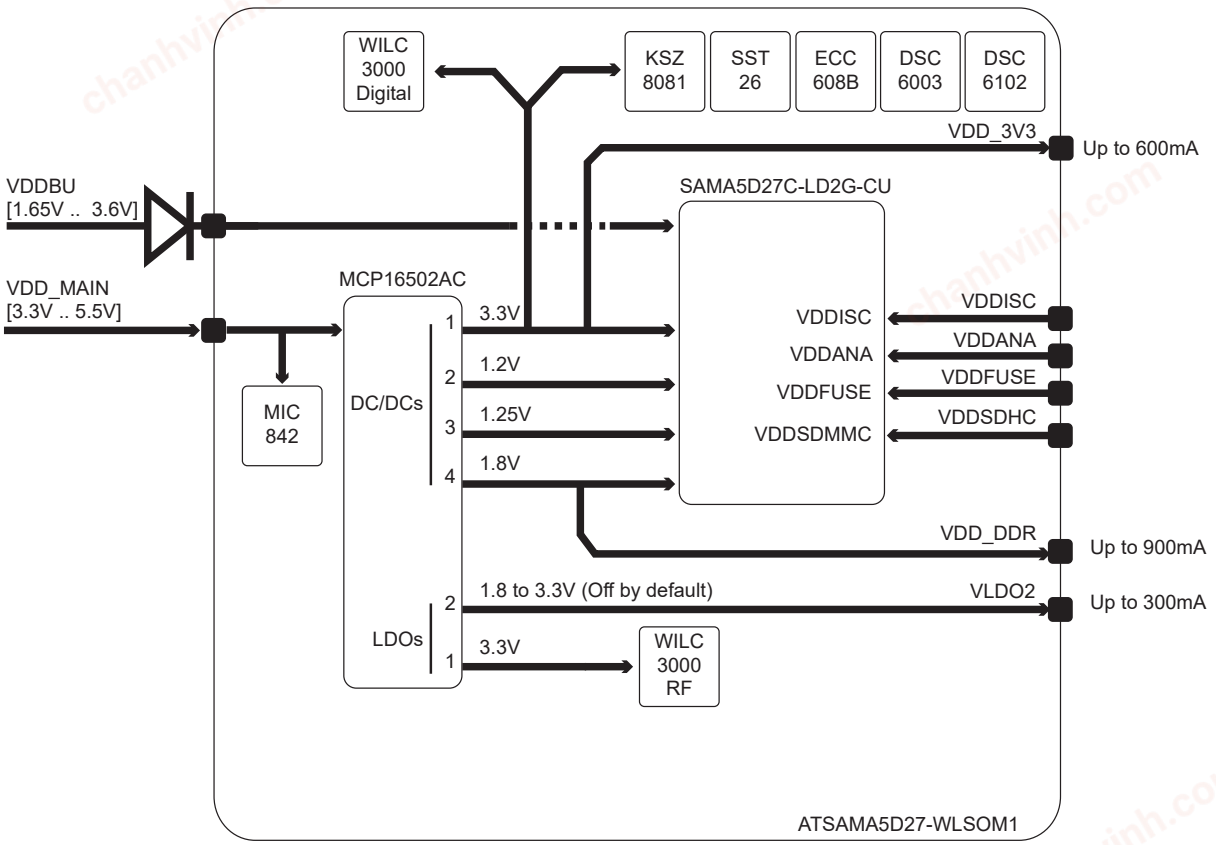
The ATSAMA5D27-WLSOM1 delivers external power supplies to the main board application, such as VDD_DDR (1.8V with 900 mA current capability), VDD_3V3 (3.3V with 600mA output current capability) and VLDO2 output (1.8V to 3.3V with 300 mA output current capability).


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-4.** ATSAMA5D27-WLSOM1 Power Architecture




### 7.2.2. Various Power Configurations

Two different configurations are described below, depending on customer use.

- Single Supply—ATSAMA5D27-WLSOM1 can be supplied by only one input supply (for example, a 5V AC/DC wall adapter) and other input supplies can be connected to the internal 3.3V regulator VDD_3V3. All the PIO lines are supplied at 3.3V.
- Multiple Supplies—ATSAMA5D27-WLSOM1 can be supplied by 5V and by a backup battery. Some PIO lines are supplied by different LDOs for specific applications, such as an ISC camera or a high-speed SD card.

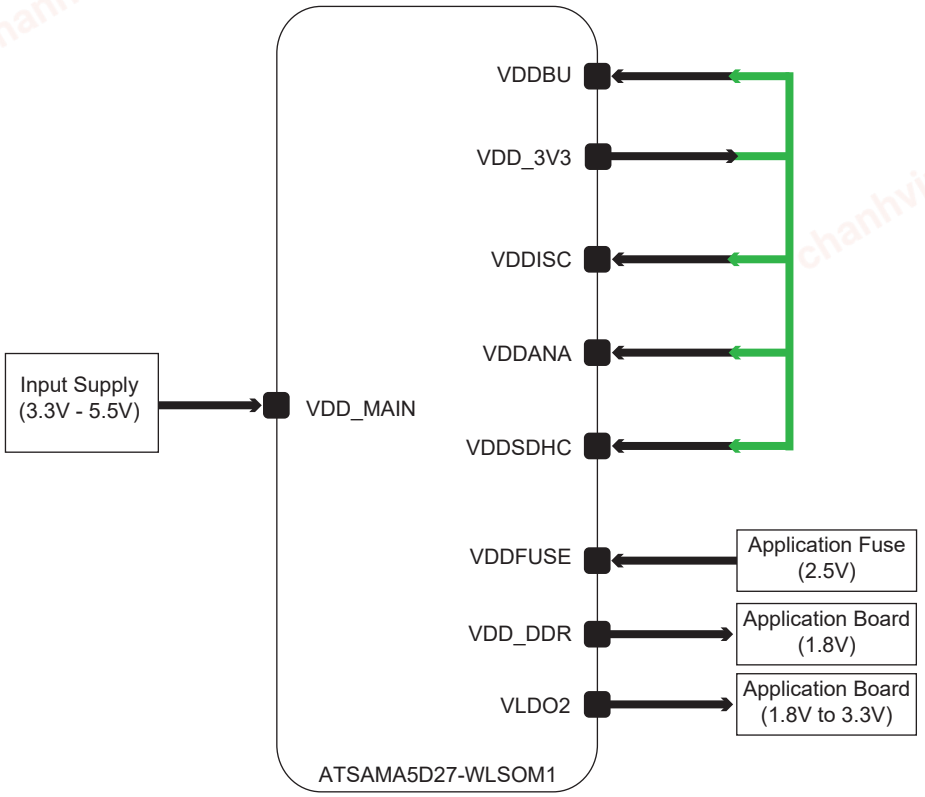

© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



### 7.2.2.1. Power Configurations: Single Supply

**Figure 7-5.** ATSAMA5D27-WLSOM1 Single Supply Connection Example





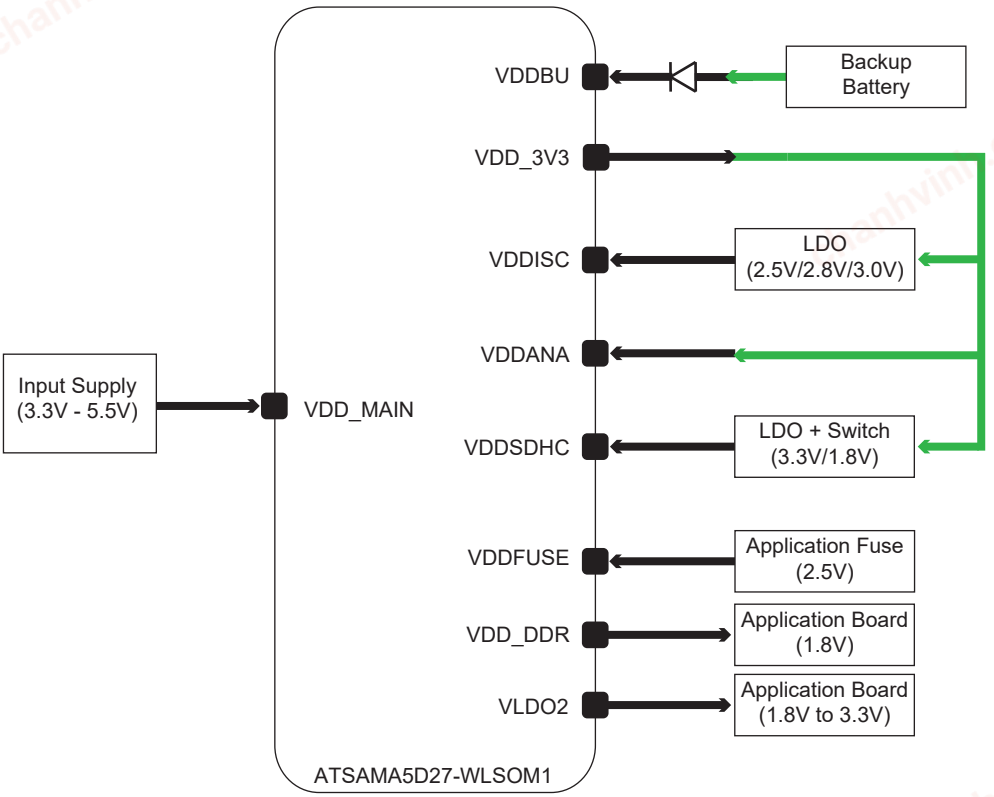
© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



#### 7.2.2.2. Power Configurations: Multiple Supplies

**Figure 7-6.** ATSAMA5D27-WLSOM1 Multiple Supplies Connection Example




### 7.2.3. Power On/Off Sequences

#### 7.2.3.1. LPDDR2 Power-Off Sequence

The LPDDR2 power-off sequence must be controlled by software to preserve the LPDDR2 device.

In this sequence, the CKE signal should be low during the full period the power rails are powering down.

The power failure can be controlled by the embedded Voltage Supervisor (MIC842) and handled at system level (IRQ on PD31). The LPDDR2 power-off sequence is applied using the bit LPDDR2_LPDDR3_PWOFF in the MPDDRC Low-Power register (MPDDRC_LPR).

For more information, refer to the following documents:

- SAMA5D2 Series Data sheet available on www.microchip.com/, sections *LPDDR2 Power Fail Management* and *MPDDRC Low-Power Register*
- Jedec Standard *Low Power Double Data Rate 2 (LPDDR2)*, JESD209-2B

**Note:** An uncontrolled power-off sequence can be applied only up to 400 times in the life of an LPDDR2 device.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



### 7.2.3.2. Power ON/OFF Sequences for Single Supply

**Figure 7-7.** ATSAMA5D27-WLSOM1 Single Supply Connection: Power-On Sequence

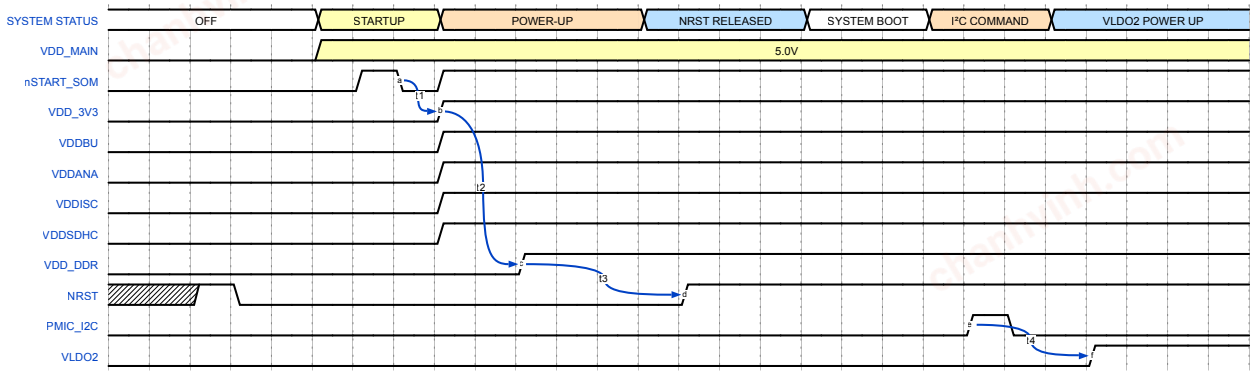



**Figure 7-8.** ATSAMA5D27-WLSOM1 Single Supply Connection: Power-Off Sequence

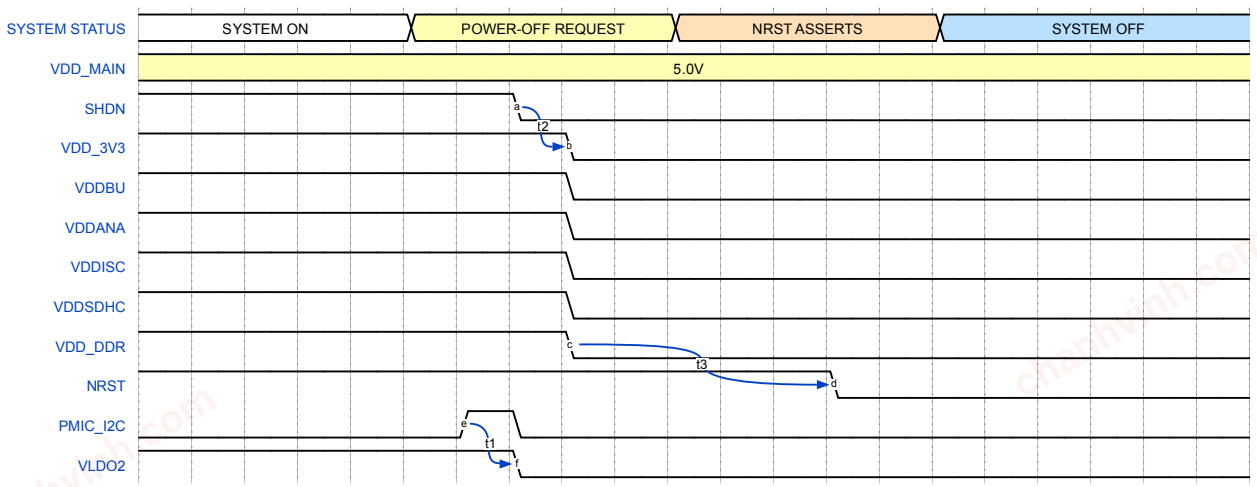



**Table 7-2.** ATSAMA5D27-WLSOM1 Simple Supply Timing Table

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| t1 | Power-Up Request Timing | 0.5 | – | 2000 | ms |
| t2 | VDD_DDR Power-Up Timing | – | 8 | – | ms |
| t3 | NRST Timing for Release | – | 16 | – | ms |
| t4 | VLDO2 Power-Up Timing after I²C Request | – | 0.5 | 1 | ms |
| t5 | VLDO2 Power-Down Timing after I²C Request | – | – | 1 | ms |
| t6 | VDD_3V3 Power-Down Timing | – | 10 | – | µs |
| t7 | NRST Forced to Low Timing | – | – | 10 | µs |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



### 7.2.3.3. Power ON/OFF Sequences for Multiple Supplies

**Figure 7-9.** ATSAMA5D27-WLSOM1 Multiple Supplies Connections: Power-On Sequence

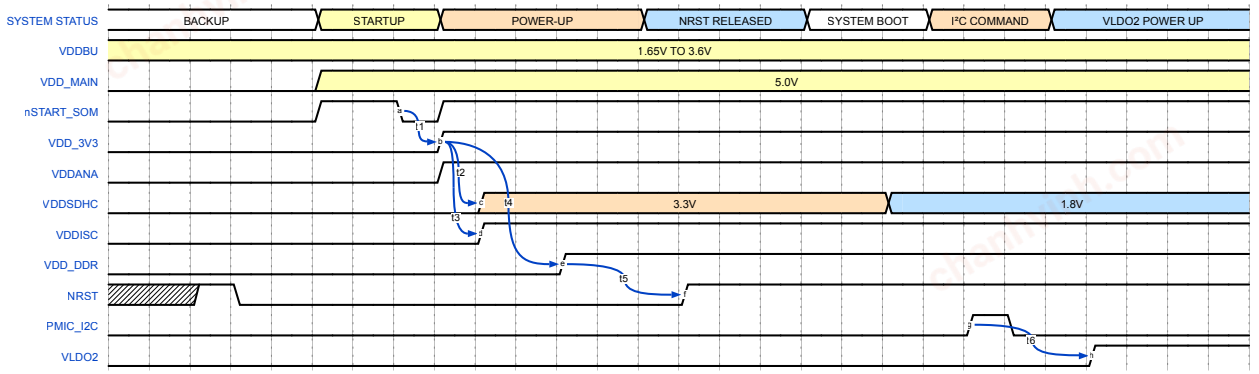



**Figure 7-10.** ATSAMA5D27-WLSOM1 Multiple Supplies Connections: Power-Off Sequence

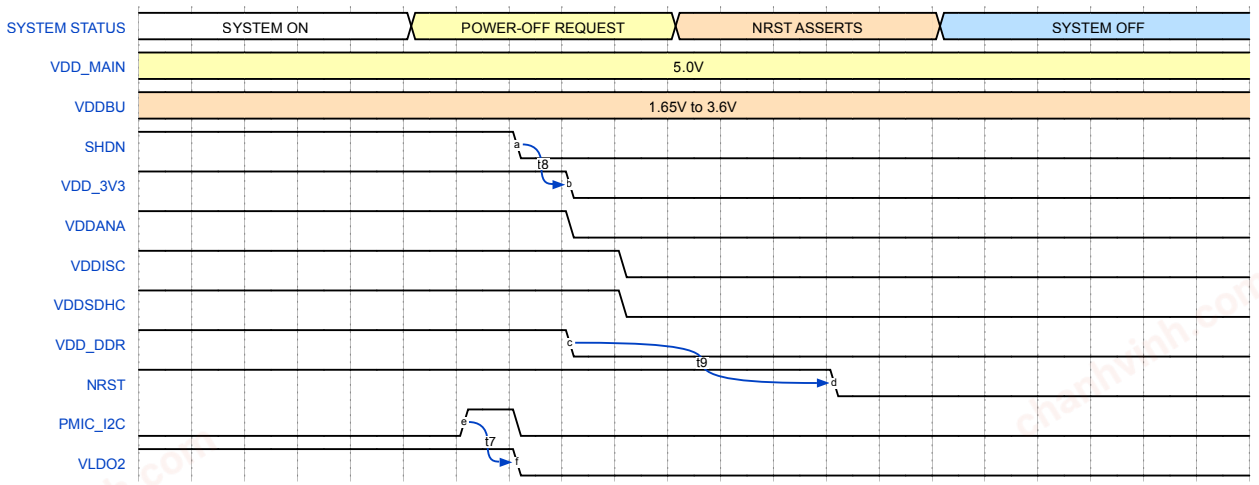



**Table 7-3.** ATSAMA5D27-WLSOM1 Multiple Supplies Timing Table

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| t1 | Power-Up Request Timing | 0.5 | – | 2000 | ms |
| t2 | VDDSDHC Power-Up Timing | – | 35 | 100 | µs |
| t3 | VDDISC Power-Up Timing | – | 40 | 100 | µs |
| t4 | VDD_DDR Power-Up Timing | – | 8 | – | ms |
| t5 | NRST Timing for Release | – | 16 | – | ms |
| t6 | VLDO2 Power-Up Timing after I²C Request | – | 0.5 | 1 | ms |
| t7 | VLDO2 Power-Down Timing after I²C Request | – | – | 1 | ms |
| t8 | VDD_3V3 Power-Down Timing | – | 10 | – | µs |
| t9 | NRST Forced to Low Timing | – | – | 10 | µs |

## 7.2.4. Baseboard Power Delivery Application Diagram Example

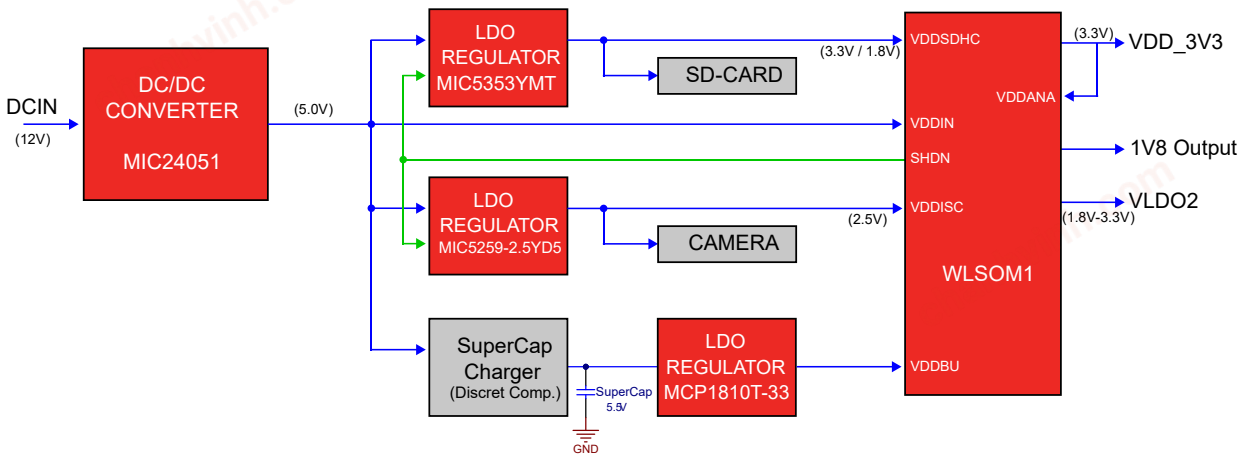
The following figure is an example of power architecture at the baseboard level, input to the SOM and output from the SOM.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-11.** Baseboard Power Delivery Application Diagram Example




## 7.3. LAN Subsystem

### 7.3.1. Ethernet Phy

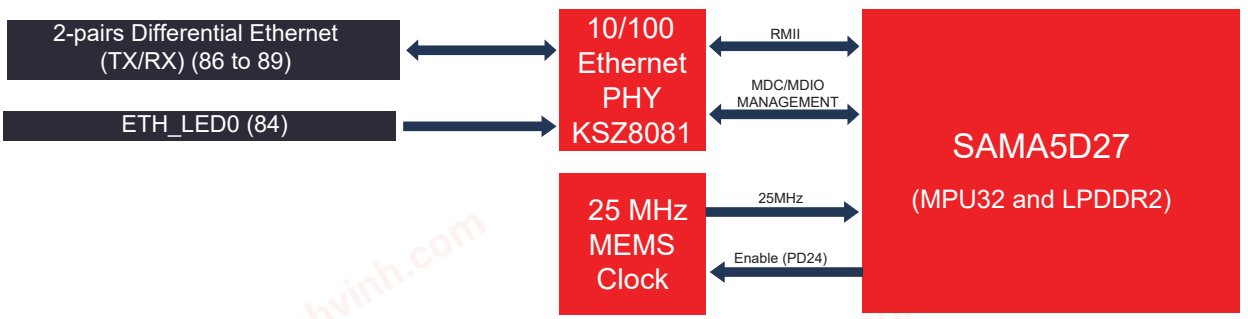
The Microchip ATSAMA5D27-WLSOM1 embeds a single-supply 10Base-T/100Base-TX Ethernet physical layer transceiver for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081RNAIA is a highly-integrated PHY solution. The KSZ8081RNAIA offers the Reduced Media Independent Interface (RMII) for direct connection to RMII-compliant MACs in Ethernet processors.

A small size MEMS Oscillator (DSC6102HI2B-025.0000) of 25-MHz is used to generate the clock source of the Ethernet functionalities of the SAMA5D27 MPU. This functionality is controlled internally by the MPU GPIO, PD24.

The KSZ8081RNAIA is available in 24-pin, lead-free QFN packages. For more information, refer to the product web page.

**Figure 7-12.** Ethernet Phy Block Diagram





© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



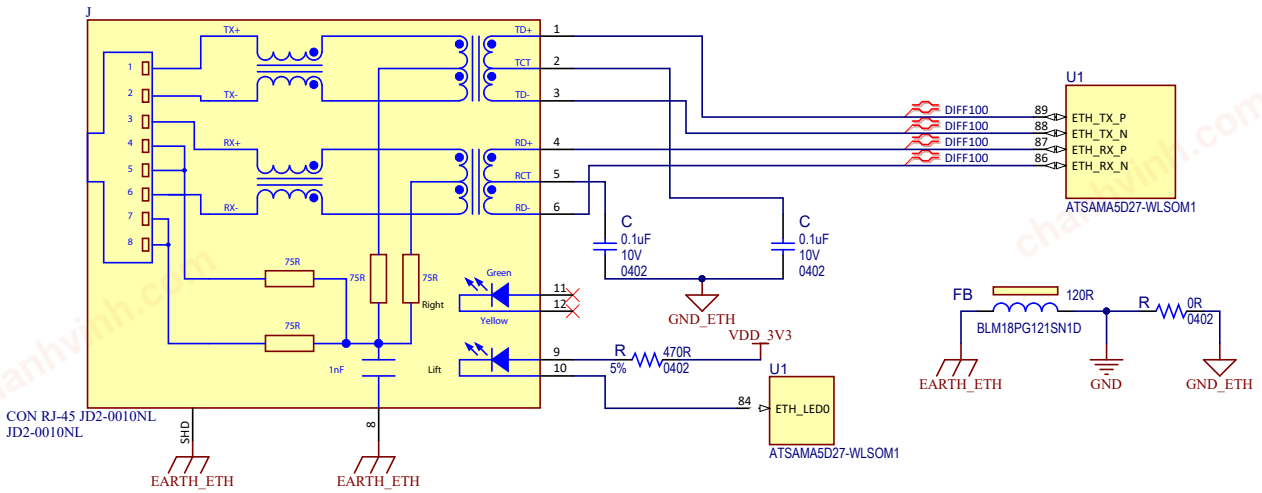
| Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Signal | Type | Signal | Dir | Func | Signal | Dir | IO Set | Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER | |
| VDD_3V3 | GPIO | PB14 | I/O | – | – | F | GTXCK | O | 3 | PIO, I, PU, ST | Used for RMII Interface |
| VDD_3V3 | GPIO | PB15 | I/O | – | – | F | GTXEN | O | 3 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PB16 | I/O | – | – | F | GRXDV | I | 3 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PB17 | I/O | – | – | F | GRXER | I | 3 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PB18 | I/O | – | – | F | GRX0 | I | 3 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PB19 | I/O | – | – | F | GRX1 | I | 3 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PB20 | I/O | – | – | F | GTX0 | O | 3 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PB21 | I/O | – | – | F | GTX1 | O | 3 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PB22 | I/O | – | – | F | GMDC | O | 3 | PIO, I, PU, ST | PIO, I, PU, ST |
| VDD_3V3 | GPIO | PB23 | I/O | – | – | F | GMDIO | I/O | 3 | PIO, I, PU, ST | PIO, I, PU, ST |
| VDD_3V3 | GPIO | PB24 | I/O | – | – | – | PB24 | | | PIO, I, PU, ST | Interrupt Line |

## 7.3.2. Interfacing with the Ethernet Phy

### 7.3.2.1. Design Schematic Example

The figure below is a schematic example at main board level.

**Figure 7-13.** Ethernet Phy Schematic Example




### 7.3.2.2. Design Layout Recommendations

When designing the Ethernet interface, consider the following recommendations:

- ETH_TX_P, ETH_TX_N, ETH_RX_P and ETH_RX_N should be routed on the top layer without any vias. Traces must be straight.
- ETH_TX_P and ETH_TX_N should be matched in length to within 120 mils.
- ETH_RX_P and ETH_RX_N should be matched in length to within 120 mils.
- ETH_TX_x and ETH_RX_x must be symmetric.
- Place the TX_P and TX_N signals at least 2 times the trace width away from other signals for noise immunity.
- Place signals at least 2 times the trace width away from any copper plan.
- Place the TX and RX signals at least 5 times the trace width away from other signals for noise immunity.

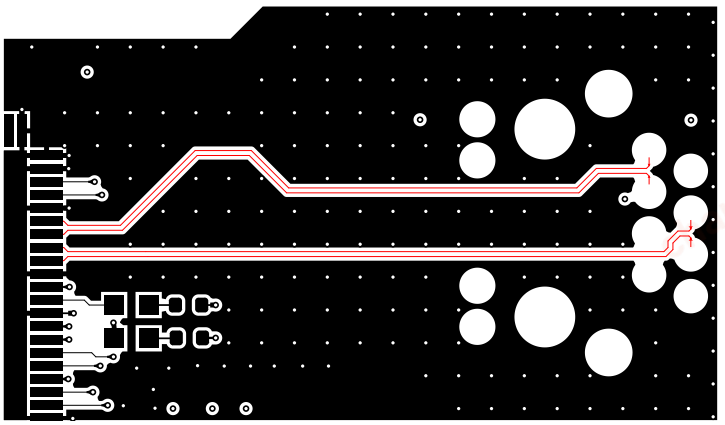

© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



- Check that the ETH_TX_x and ETH_RX_x line impedance is the same for all signal layers. Recommended differential impedance for net: 100Ω ± 5%.

#### 7.3.2.3. Design Layout Example



## 7.4. Voltage Threshold Detector

The Microchip ATSAMA5D27-WLSOM1 embeds a MIC842 micro-power, precision-voltage comparator with an on-chip voltage reference.

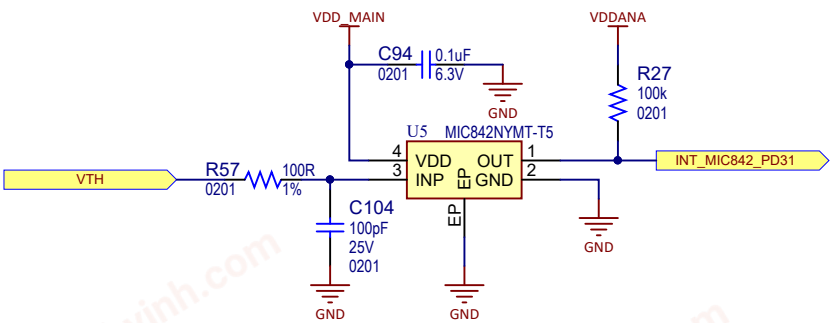
The device is intended for voltage monitoring applications. External resistors are used to set the voltage monitor threshold. When the threshold is crossed, the outputs switch polarity. Refer to the figures below.

The MIC842 incorporates a voltage reference and comparator with fixed internal hysteresis; two external resistors are used to set the switching threshold voltage.

Supply current is extremely low (1.5 µA, typical), making it ideal for portable applications.

The MIC842 is supplied in 4-pin 1.2 mm × 1.6 mm Thin DFN package. For more information, refer to the product web page.

**Figure 7-14.** Voltage Threshold Detector Schematic





© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-15.** Voltage Threshold Detector Implementation Example

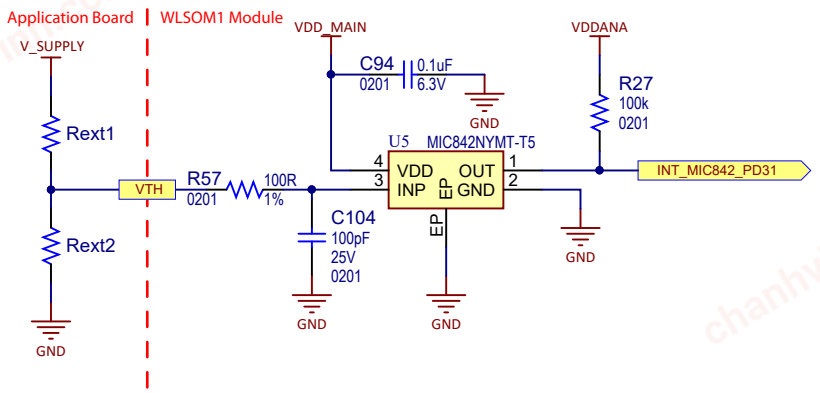



**Table 7-4.** Output Resistor Ladder Values and Input System Supply Example

| System Supply Voltage | Threshold Detection Value | Rext1 Value | Rext2 Value |
|---|---|---|---|
| 5V | 4.64V | 787 kΩ | 287 kΩ |
| 12V | 11V | 787 kΩ | 100 kΩ |
| 24V | 21.78V | 787 kΩ | 47.5 kΩ |
| 48V | 39.51V | 787 kΩ | 25.5 kΩ |

## 7.5. Radio Subsystem

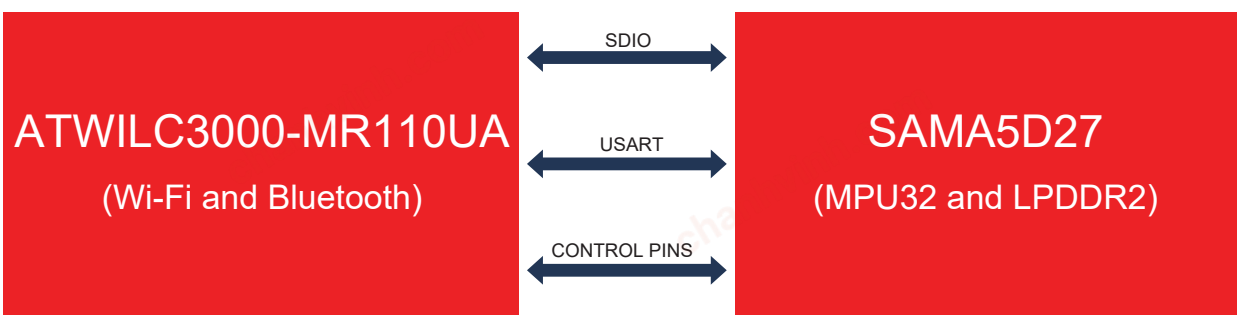
The ATSAMA5D27-WLSOM1 embeds an ATWILC3000-MR110UA module, which uses a single chip IEEE 802.11 b/g/n RF/Baseband/MAC link controller and Bluetooth 5. The ATWILC3000 connects to Microchip MPUs, with minimal resource requirements with simple SDIO-to-Wi-Fi and UART-to-Bluetooth interfaces.

The ATWILC3000-MR110UA supports single stream 1x1 802.11n mode, providing tested throughput of up to 46 Mbps UDP & 28 Mbps TCP/IP. The ATWILC3000-MR110UA features fully integrated power amplifier, LNA, switch and power management. Implemented in low-power CMOS technology, the ATWILC3000-MR110UA offers very low power consumption while simultaneously providing high performance and minimal bill of materials.

The ATWILC3000-MR110UA utilizes highly -optimized 802.11 Bluetooth coexistence protocols. The only external clock sources needed are a high-speed crystal or oscillator and a 32.768 kHz clock for sleep operation. In the ATSAMA5D27-WLSOM1, the 32.768 kHz clock is provided by the ATSAMA5D27 through PB13.

For more information, refer to the product web page.

**Figure 7-16.** Wi-Fi/BT Radio Subsystem Block Diagram





© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Table 7-5.** WILC Pin Description

| Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Signal | Type | Signal | Dir | Func | Signal | Dir | IO Set | Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER | |
| VDD_3V3 | GPIO | PA18 | I/O | – | – | E | SDMMC1_DAT0 | I/O | 1 | PIO, I, PU, ST | Used for SDIO Interface |
| VDD_3V3 | GPIO | PA19 | I/O | – | – | E | SDMMC1_DAT1 | I/O | 1 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PA20 | I/O | – | – | E | SDMMC1_DAT2 | I/O | 1 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PA21 | I/O | – | – | E | SDMMC1_DAT3 | I/O | 1 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PA22 | I/O | – | – | E | SDMMC1_CK | I/O | 1 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PA28 | I/O | – | – | E | SDMMC1_CMD | I/O | 1 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PA23 | I/O | – | – | A | FLEXCOM1_IO1 | I/O | 1 | PIO, I, PU, ST | Used for USART Interface |
| VDD_3V3 | GPIO | PA24 | I/O | – | – | A | FLEXCOM1_IO0 | I/O | 1 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PA25 | I/O | – | – | A | FLEXCOM1_IO3 | O | 1 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PA26 | I/O | – | – | A | FLEXCOM1_IO4 | O | 1 | PIO, I, PU, ST | |
| VDD_3V3 | GPIO | PA27 | I/O | – | – | – | PA27 | O | – | PIO, I, PU, ST | WILC Reset Line |
| VDD_3V3 | GPIO | PA29 | I/O | – | – | – | PA29 | O | – | PIO, I, PU, ST | WILC Chip Select |
| VDD_3V3 | GPIO | PB13 | I/O | – | – | – | PCK1 | O | 3 | PIO, I, PU, ST | WILC 32 kHz |
| VDD_3V3 | GPIO | PB25 | I/O | – | – | – | PB25 | I | – | PIO, I, PU, ST | WILC Interrupt |

## 7.6. External Interfaces

### 7.6.1. Interfacing with an SD Card

The SD (Secure Digital) Card is a nonvolatile memory card format used as mass storage memory in mobile devices.

Secure Digital Multimedia Card (SDMMC) Controller

The ATSAMA5D27-WLSOM1 has one Secure Digital Multimedia Card (SDMMC) interface that supports the MultiMedia Card (e.MMC) Specification V4.41, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 specification.

The SDMMC0 interface can be connected to a standard SD card interface.

SDMMC0 Card Connector

The board features a standard MMC/SD card connector, connected to SDMMC0. The SDMMC0 communication is based on a 4- or 8-pin interface (clock, command, four or eight data and power lines). It may include a card detection switch.

#### 7.6.1.1. Design Schematic Examples

The figures below illustrate the implementation for the SDMMC0 interface for a 4-bit interface and for an 8-bit interface with a power switch for the supply of the digital interface for high-speed interface management.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-17.** 4-bit/8-bit SD Card Power Switch Example Schematic

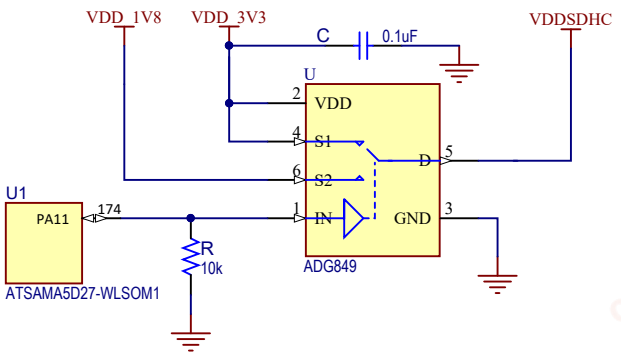
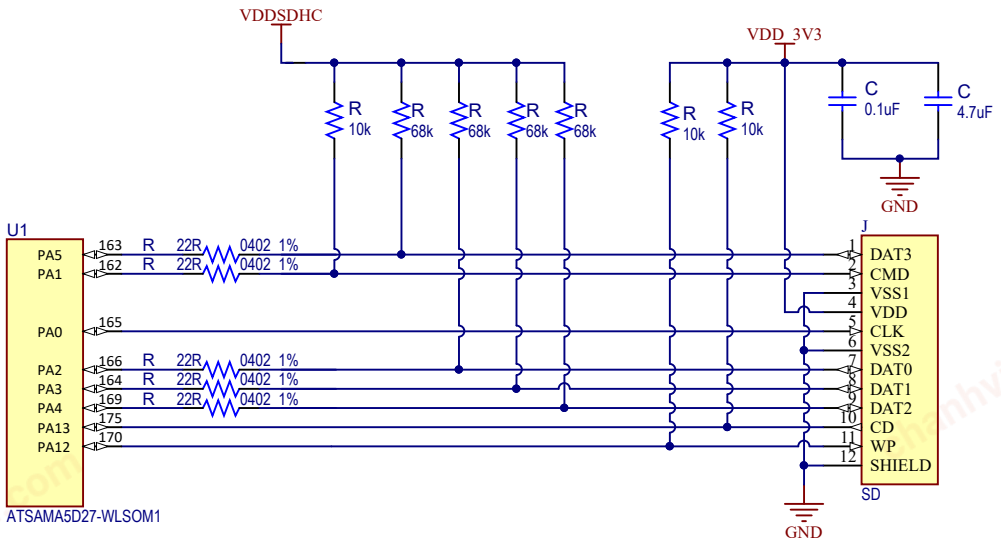



**Figure 7-18.** 4-bit SD Card Interface Example Schematic



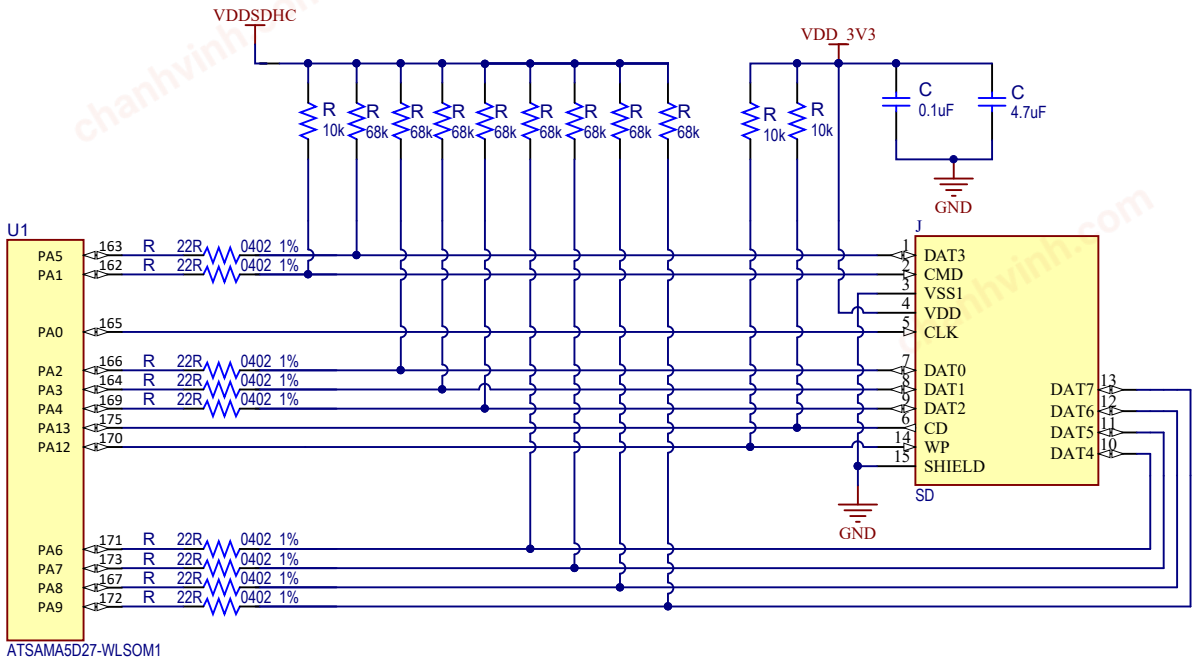


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-19.** 8-bit SD Card Interface Example Schematic

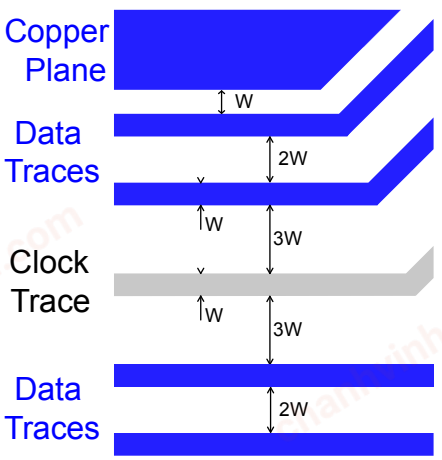



### 7.6.1.2. Design Layout Recommendations

When designing the SD Card interface, consider the following recommendations:

- Match signal lengths to within 50 mils. Affected PIOs in the example above are PA0 to PA5.
- Place the clock line (PA0) at least 3 times the trace width away from other signals for noise immunity.
- Apply impedance control of 50 Ohms on the clock and data interfaces.
- Place data signals at least 2 times the trace width away from any other data traces.
- Place data signals at least 1 trace width away from any copper plan.

**Figure 7-20.** SD Card Layout Example




### 7.6.1.3. EMI Improvement Recommendations

To reduce radiation emission, consider the following recommendations:

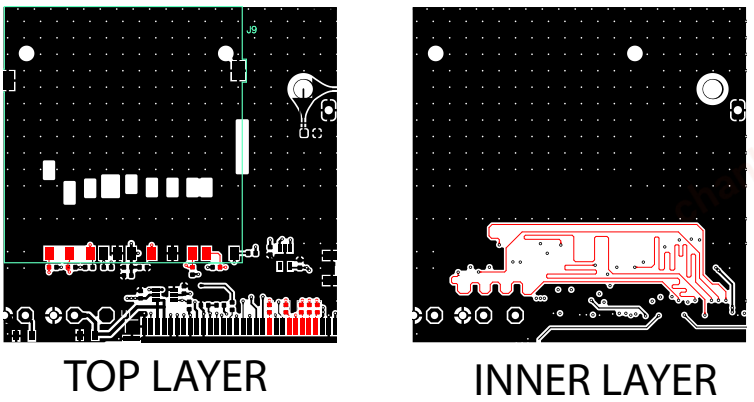

© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



- Position all the signals of the SD Card interface in inner layers of the PCB.
- Place the resistors as close as possible to the WLSOM1 module.

**Figure 7-21.** EMI Improvement Layout Example




### 7.6.2. Interfacing with e-MMC

The Secure Digital Multimedia Card (SDMMC) Controller supports the Embedded MultiMedia Card (e-MMC) Specification V4.41, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 specification.

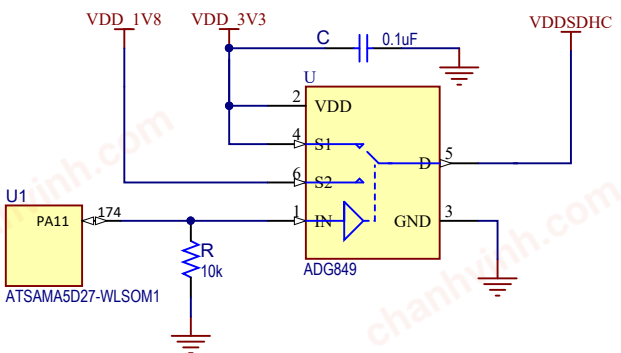
**Table 7-6.** SDMMC Reference Documents

| Name | Link |
|---|---|
| SD Host Controller Simplified Specification V3.00 | www.sdcard.org |
| SDIO Simplified Specification V3.00 | www.sdcard.org |
| Physical Layer Simplified Specification V3.01 | www.sdcard.org |
| Embedded MultiMedia Card (e-MMC) Electrical Standard 4.51 | www.jedec.org |

#### 7.6.2.1. Design Schematic Example

In the example below, one MTFC4GLDEA 4 GB e-MMC is connected to the processor through the SDMMC0 port.

**Figure 7-22.** e-MMC Power Switch Example Schematic



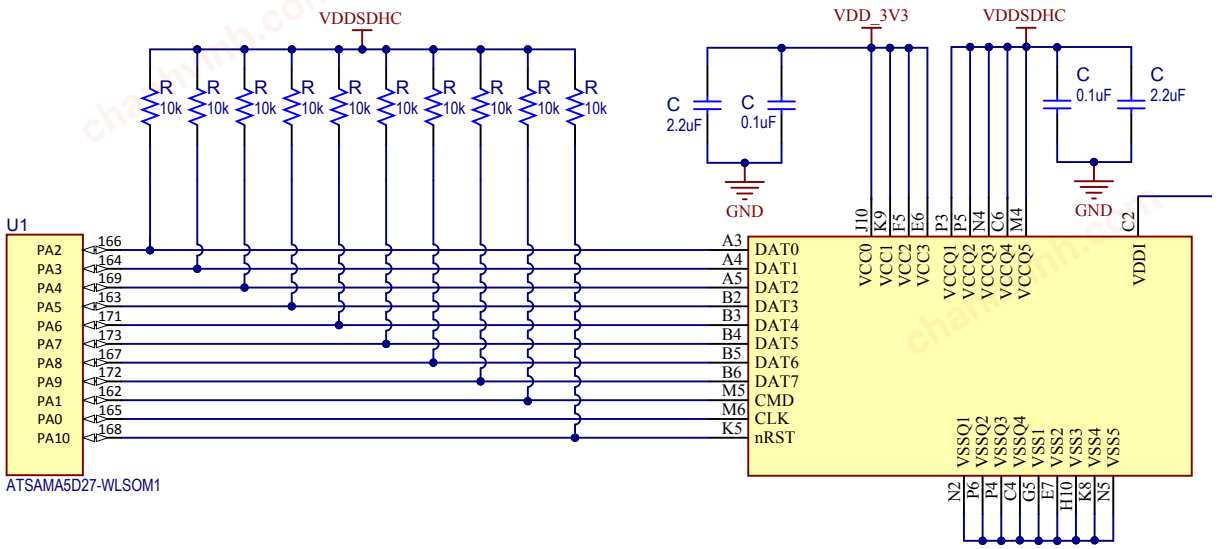


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-23.** e-MMC Interface Example Schematic

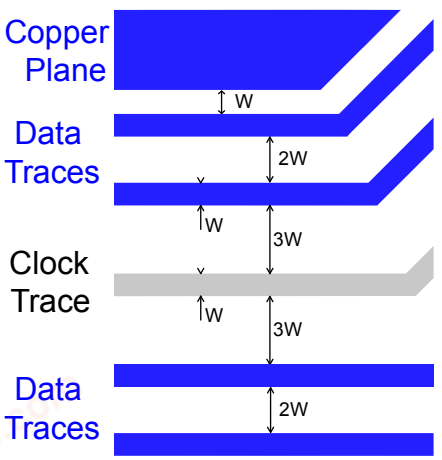



### 7.6.2.2. Design Layout Recommendations

When designing the e-MMC interface, consider the following recommendations:

- Match signal lengths to within 50 mils. Affected PIOs in the example above are PA0 to PA9.
- Place the clock line (PA0) at least 3 times the trace width away from other signals for noise immunity.
- Place data signals at least 2 times the trace width away from any other data trace.
- Place data signals at least 1 trace width away from any copper plan.

**Figure 7-24.** e-MMC Layout Example




## 7.6.3. Interfacing with NAND Flash

This Static Memory Controller (SMC) is capable of handling several types of external memory and peripheral devices, such as SRAM, PSRAM, PROM, EPROM, EEPROM, LCD module, NOR Flash and NAND Flash.

The SMC generates the signals that control the access to external memory devices or peripheral devices.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



The SMC embeds a NAND Flash Controller (NFC). The NFC can handle automatic transfers, sending the commands and address cycles to the NAND Flash and transferring the contents of the page (for read and write) to the NFC SRAM. It minimizes the CPU overhead.

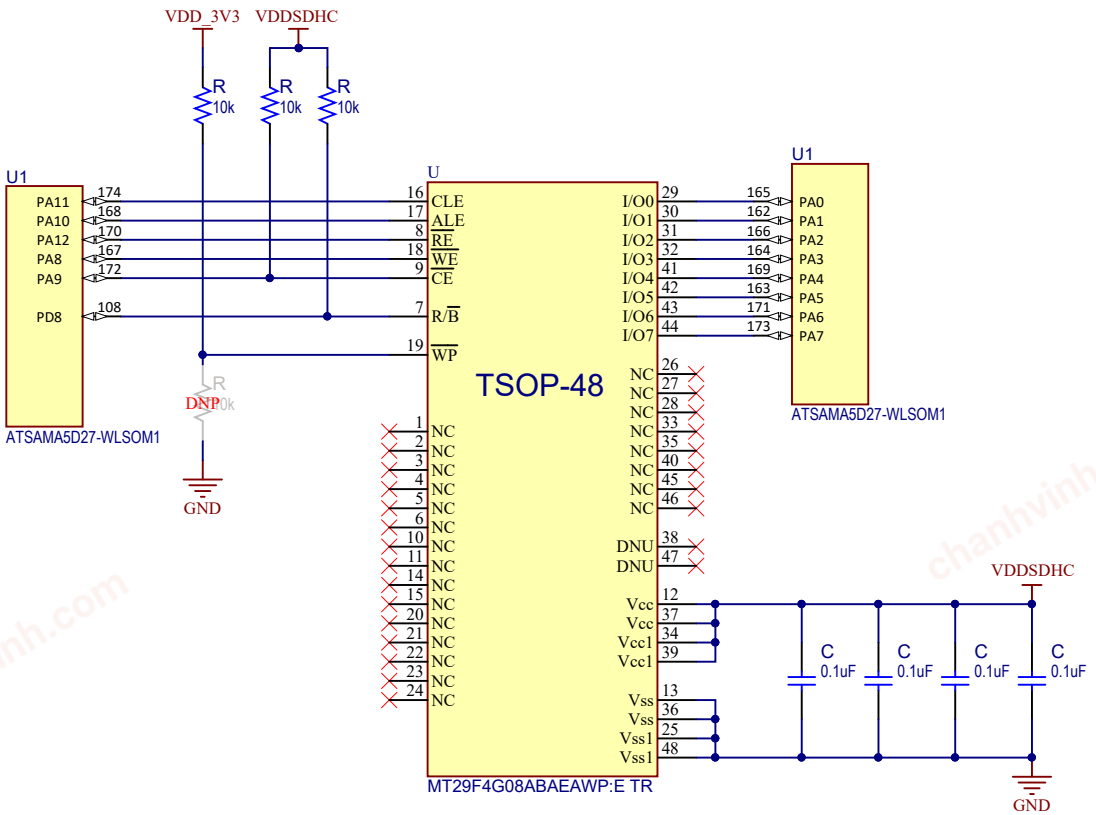
The SMC includes programmable hardware error correcting code with one-bit error correction capability and supports two-bit error detection.

In order to improve the overall system performance, the DATA phase of the transfer can be DMA-assisted.

### 7.6.3.1. Design Schematic Example

The example below is given with an 8-bit NAND Flash memory from Micron.

**Figure 7-25.** NAND Flash Interface Example Schematic




### 7.6.3.2. Design Layout Recommendations

When designing the NAND Flash interface, consider the following recommendations:

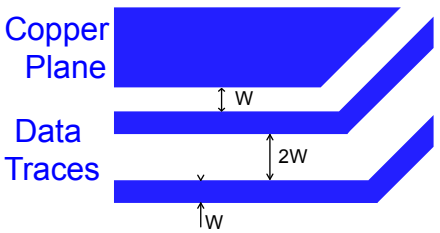
- Match signal lengths to within 50 mils. Affected PIOs in the example schematic above are PA0 to PA7. For EMI improvement, all these nets should be placed in inner layers.
- Place data signals at least 2 times the trace width away from any other data trace.
- Place data signals at least 1 trace width away from any copper plan.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-26.** NAND Flash Layout Example



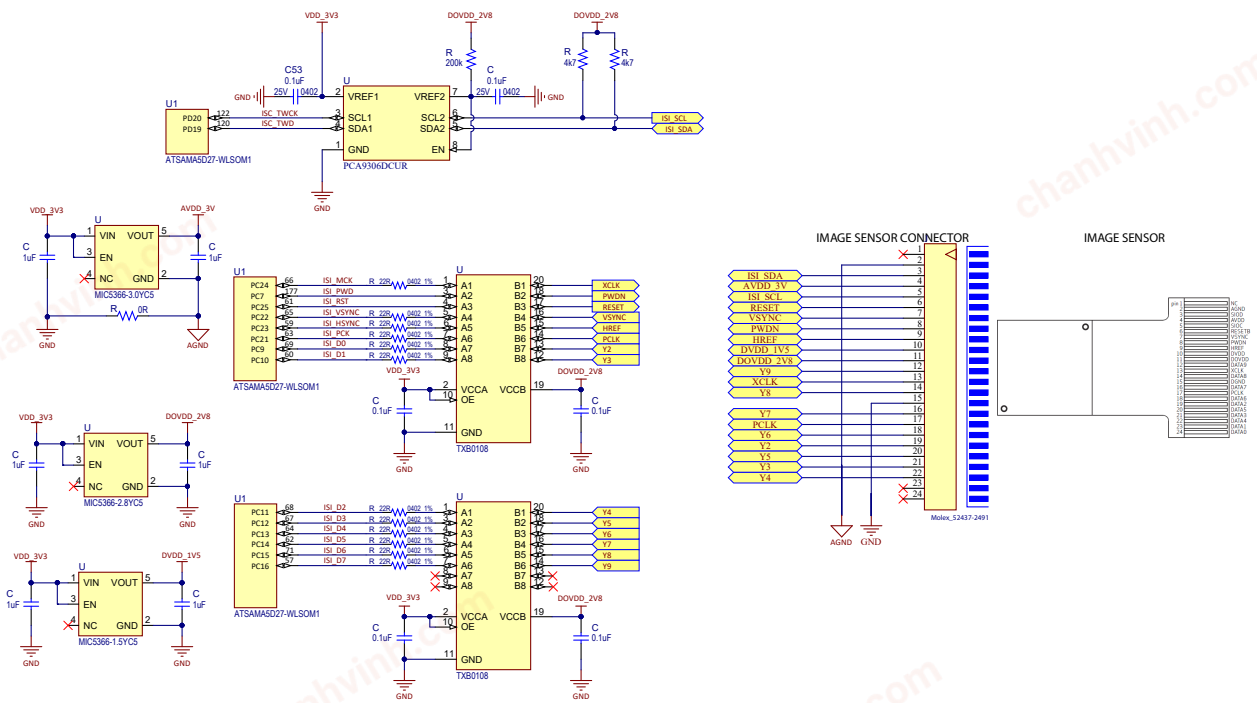

### 7.6.4. Interfacing with an Image Sensor Controller (ISC)

The Image Sensor Controller (ISC) system manages incoming data from a parallel sensor. It supports a single active interface. The parallel interface protocol can use a free-running clock or a gated clock strategy. It supports the ITU-R BT 656/1120 422 protocol with a data width of 8 bits or 10 bits and raw Bayer format. The internal image processor includes adjustable white balance, color filter array interpolation, color correction, gamma correction, 12-bit to 10-bit compression, programmable color space conversion and horizontal and vertical chrominance subsampling module. The module also integrates a triple channel Direct Memory Access Controller host interface.

#### 7.6.4.1. Design Schematic Example

The example schematics shown below are for different Image Sensor supply voltages.

**Figure 7-27.** Camera Interface Example Schematic with VDDISC Set at 3.3V



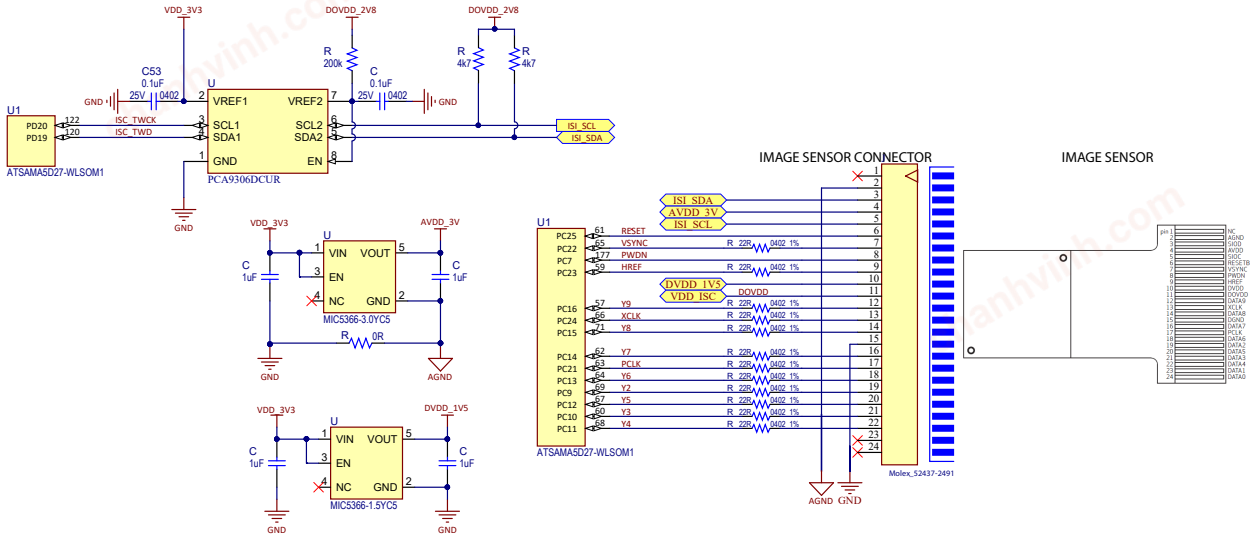


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-28.** Camera Interface Example Schematic with VDDISC Set at Specific Voltage

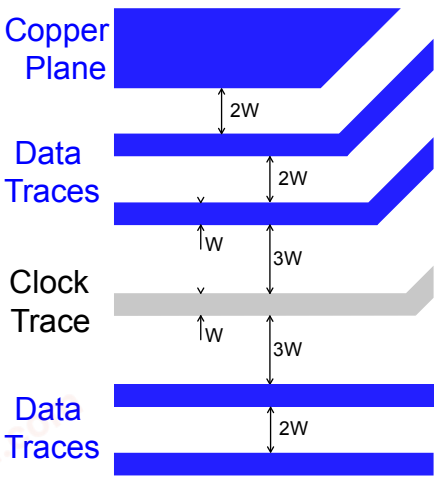



### 7.6.4.2. Design Layout Recommendations

When designing the ISC interface, consider the following recommendations:

- Match signal lengths to within 50 mils. Affected PIOs in the example above are PC9 to PC24.
- Place the clock lines (PC21 and PC24) at least 3 times the trace width away from other signals for noise immunity.
- Place data signals at least 2 times the trace width away from any other data traces.
- Place data signals at least 2 times the trace width away from any copper plan.

**Figure 7-29.** ISC Layout Example




### 7.6.4.3. EMI Improvement Recommendations

To reduce radiation emission, consider the following recommendations:

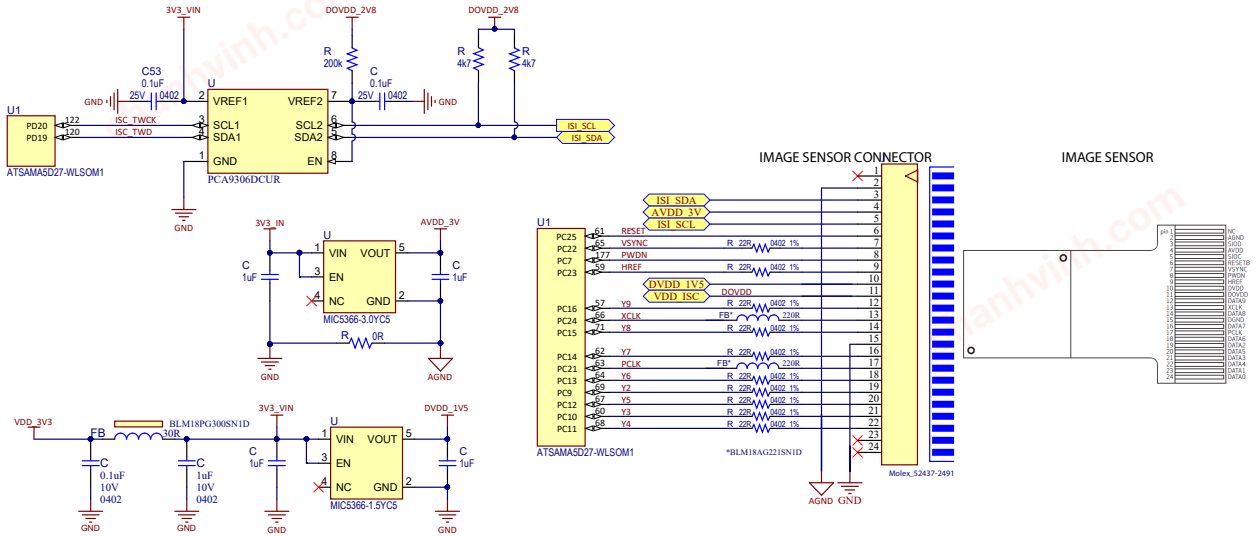
- Position the ISC bus interface in inner layers of the PCB.
- Add a ferrite bead on PCLK and on XCLK clocks lines.
- Add a ferrite bead on the camera power supply.
- Select a shielded camera connector.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-30.** EMI Improvement Example




## 7.6.5. Connecting to the SPI Interface

Four different FLEXCOM interfaces, with seven possible configurations (configured in SPI mode), and two pure SPI Interfaces, with four possible configurations, are available on the ATSAMA5D27-WLSOM1 module.

The Flexible Serial Communication Controller (FLEXCOM) offers several serial communication protocols that are managed by the three submodules USART, SPI, and TWI.

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Host or Client mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPI devices. During a data transfer, one SPI system acts as the “host”' which controls the data flow, while the other devices act as “clients'' which have data shifted into and out by the host. Different CPUs can take turn being hosts (multiple host protocol, contrary to single host protocol where one CPU is always the host while all of the others are always clients). One host can simultaneously shift data into multiple clients. However, only one client can drive its output to write data back to the host at any given time.

A client device is selected when the host asserts its NSS signal. If multiple client devices exist, the host generates a separate client select signal for each client (NPCS).

The SPI system consists of two data lines and two control lines:

- Host Out Client In (MOSI)—This data line supplies the output data from the host shifted into the input(s) of the client(s).
- Host In Client Out (MISO)—This data line supplies the output data from a client to the input of the host. There may be no more than one client transmitting data during any particular transfer.
- Serial Clock (SPCK)—This control line is driven by the host and regulates the flow of the data bits. The host can transmit data at a variety of baud rates; there is one SPCK pulse for each bit that is transmitted.
- Client Select (NSS)—This control line allows clients to be turned on and off by hardware.

**Table 7-7.** SPI Interface Configurations

| Interface Instance | IO set | Pin # | PIO | Pin Name | Comments |
|---|---|---|---|---|---|
| SPI0 | 1 | 21 | PA14 | SPI0_SPCK | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Table 7-7.** SPI Interface Configurations (continued)

| Interface Instance | IO set | Pin # | PIO | Pin Name | Comments |
|---|---|---|---|---|---|
| SPI0 | 1 | 22 | PA15 | SPI0_MOSI | |
| SPI0 | 1 | 23 | PA16 | SPI0_MISO | |
| SPI0 | 1 | 24 | PA17 | SPI0_NPCS0 | |
| SPI0 | 2 | 76 | PA30 | SPI0_NPCS0 | |
| SPI0 | 2 | 75 | PA31 | SPI0_MISO | |
| SPI0 | 2 | 81 | PB00 | SPI0_MOSI | |
| SPI0 | 2 | 80 | PB01 | SPI0_SPCK | |
| SPI0 | 1 | 18 | PC01 | SPI1_SPCK | |
| SPI1 | 1 | 17 | PC02 | SPI1_MOSI | |
| SPI1 | 1 | 16 | PC03 | SPI1_MISO | |
| SPI1 | 1 | 19 | PC04 | SPI1_NPCS0 | |
| SPI1 | 1 | 20 | PC05 | SPI1_NPCS1 | |
| SPI1 | 1 | 176 | PC06 | SPI1_NPCS2 | |
| SPI1 | 1 | 177 | PC07 | SPI1_NPCS3 | |
| SPI1 | 3 | 132 | PD25 | SPI1_SPCK | |
| SPI1 | 3 | 127 | PD26 | SPI1_MOSI | |
| SPI1 | 3 | 123 | PD27 | SPI1_MISO | |
| SPI1 | 3 | 124 | PD28 | SPI1_NPCS0 | |
| SPI1 | 3 | 131 | PD29 | SPI1_NPCS1 | |
| SPI1 | 3 | 130 | PD30 | SPI1_NPCS2 | |

**Table 7-8.** FLEXCOM Interfaces Configurations in SPI Mode

| Interface Instance | IO set | Pin # | PIO | Pin Name | Comments |
|---|---|---|---|---|---|
| FLEXCOM0 | 1 | 28 | PB28 | FLEXCOM0_IO0 | MOSI Signal |
| FLEXCOM0 | 1 | 27 | PB29 | FLEXCOM0_IO1 | MISO Signal |
| FLEXCOM0 | 1 | 30 | PB30 | FLEXCOM0_IO2 | SPCK Signal |
| FLEXCOM0 | 1 | 26 | PB31 | FLEXCOM0_IO3 | NPCS0 Signal |
| FLEXCOM0 | 1 | 15 | PC00 | FLEXCOM0_IO4 | NPCS1 Signal |
| FLEXCOM2 | 1 | 171 | PA06 | FLEXCOM2_IO0 | MOSI Signal |
| FLEXCOM2 | 1 | 173 | PA07 | FLEXCOM2_IO1 | MISO Signal |
| FLEXCOM2 | 1 | 167 | PA08 | FLEXCOM2_IO2 | SPCK Signal |
| FLEXCOM2 | 1 | 172 | PA09 | FLEXCOM2_IO3 | NPCS0 Signal |
| FLEXCOM2 | 1 | 168 | PA10 | FLEXCOM2_IO4 | NPCS1 Signal |
| FLEXCOM2 | 2 | 127 | PD26 | FLEXCOM2_IO0 | MOSI Signal |
| FLEXCOM2 | 2 | 123 | PD27 | FLEXCOM2_IO1 | MISO Signal |
| FLEXCOM2 | 2 | 124 | PD28 | FLEXCOM2_IO2 | SPCK Signal |
| FLEXCOM2 | 2 | 131 | PD29 | FLEXCOM2_IO3 | NPCS0 Signal |
| FLEXCOM2 | 2 | 130 | PD30 | FLEXCOM2_IO4 | NPCS1 Signal |
| FLEXCOM3 | 2 | 56 | PC18 | FLEXCOM3_IO2 | SPCK Signal |
| FLEXCOM3 | 2 | 70 | PC19 | FLEXCOM3_IO1 | MISO Signal |
| FLEXCOM3 | 2 | 58 | PC20 | FLEXCOM3_IO0 | MOSI Signal |
| FLEXCOM3 | 2 | 63 | PC21 | FLEXCOM3_IO3 | NPCS0 Signal |
| FLEXCOM3 | 2 | 65 | PC22 | FLEXCOM3_IO4 | NPCS1 Signal |
| FLEXCOM4 | 1 | 39 | PC28 | FLEXCOM4_IO0 | MOSI Signal |
| FLEXCOM4 | 1 | 38 | PC29 | FLEXCOM4_IO1 | MISO Signal |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Table 7-8.** FLEXCOM Interfaces Configurations in SPI Mode (continued)

| Interface Instance | IO set | Pin # | PIO | Pin Name | Comments |
|---|---|---|---|---|---|
| FLEXCOM4 | 1 | 34 | PC30 | FLEXCOM4_IO2 | SPCK Signal |
| FLEXCOM4 | 1 | 36 | PC31 | FLEXCOM4_IO3 | NPCS0 Signal |
| FLEXCOM4 | 1 | 33 | PD00 | FLEXCOM4_IO4 | NPCS1 Signal |
| FLEXCOM4 | 2 | 119 | PD12 | FLEXCOM4_IO0 | MOSI Signal |
| FLEXCOM4 | 2 | 116 | PD13 | FLEXCOM4_IO1 | MISO Signal |
| FLEXCOM4 | 2 | 117 | PD14 | FLEXCOM4_IO2 | SPCK Signal |
| FLEXCOM4 | 2 | 114 | PD15 | FLEXCOM4_IO3 | NPCS0 Signal |
| FLEXCOM4 | 2 | 115 | PD16 | FLEXCOM4_IO4 | NPCS1 Signal |

### 7.6.6. Connecting to the I²C Interface

Four different FLEXCOM interfaces, with seven possible configurations (configured in TWI mode), and one pure TWI Interface are available on the ATSAMA5D27-WLSOM1 module.

The Flexible Serial Communication Controller (FLEXCOM) offers several serial communication protocols that are managed by the three submodules USART, SPI, and TWI.

The Two-wire Interface (TWI) interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 kbit/s in Fast mode and up to 3.4 Mbit/s in High-Speed Client mode only, based on a byte-oriented transfer format.

It can be used with any Two-wire Interface bus Serial EEPROM and I²C-compatible devices, such as a Real-Time Clock (RTC), Dot Matrix/Graphic LCD Controller and temperature sensor. The TWI is programmable as a host or a client with sequential or single-byte access. Multiple host capability is supported.

**Table 7-9.** I²C Interface Configurations

| Interface Instance | IO Set | Pin # | PIO | Pin Name | Comment |
|---|---|---|---|---|---|
| TWI1 | 3 | 120 | PD19 | TWD1 | No need of external pull-up. Already integrated in ATSAMA5D27-WLSOM1 module |
| TWI1 | 3 | 122 | PD20 | TWCK1 | |
| FLEXCOM0 | 1 | 28 | PB28 | FLEXCOM0_IO0 | Need external pull-up in case the FLEXCOM interface is used as an I²C/TWI interface. |
| FLEXCOM0 | 1 | 27 | PB29 | FLEXCOM0_IO1 | |
| FLEXCOM2 | 1 | 171 | PA6 | FLEXCOM2_IO0 | |
| FLEXCOM2 | 1 | 173 | PA7 | FLEXCOM2_IO1 | |
| FLEXCOM2 | 2 | 127 | PD26 | FLEXCOM2_IO0 | |
| FLEXCOM2 | 2 | 123 | PD27 | FLEXCOM2_IO1 | |
| FLEXCOM3 | 1 | 22 | PA15 | FLEXCOM3_IO0 | |
| FLEXCOM3 | 1 | 175 | PA13 | FLEXCOM3_IO1 | |
| FLEXCOM3 | 2 | 58 | PC20 | FLEXCOM3_IO0 | |
| FLEXCOM3 | 2 | 63 | PC21 | FLEXCOM3_IO1 | |
| FLEXCOM4 | 1 | 39 | PC28 | FLEXCOM4_IO0 | |
| FLEXCOM4 | 1 | 38 | PC29 | FLEXCOM4_IO1 | |
| FLEXCOM4 | 2 | 119 | PD12 | FLEXCOM4_IO0 | |
| FLEXCOM4 | 2 | 116 | PD13 | FLEXCOM4_IO1 | |

### 7.6.7. Interfacing with CLASS-D Audio Output

The Audio Class D Amplifier (CLASSD) is a digital input, pulse width modulated (PWM) output mono Class D amplifier. It features a high-quality interpolation filter embedding a digitally controlled gain, an equalizer and a de-emphasis filter.


© 2026 Microchip Technology Inc. and its subsidiaries

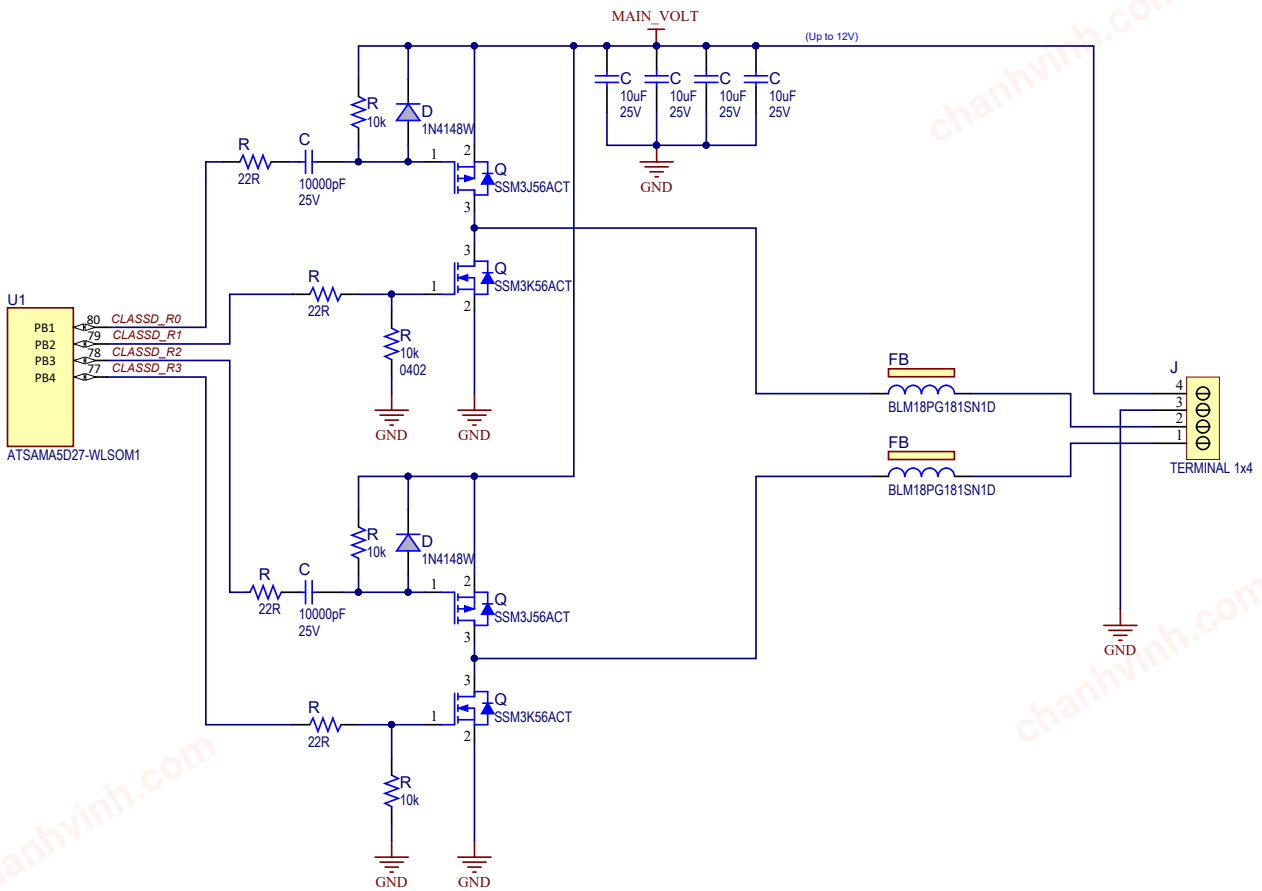
chanhvinh.com



On its input side, the CLASSD is compatible with most common audio data rates. On the output side, its PWM output can drive either:

- high-impedance single-ended or differential output loads (Audio DAC application) or,
- external MOSFETs through an integrated nonoverlapping circuit (Class D power amplifier application).

**Figure 7-31.** CLASS-D Interface Example Schematic




## 7.6.8. QTouch® Peripheral Touch Controller (PTC)

For details on implementing the PTC, refer to the documents listed below:

| Title | Document Type | Literature Number |
|---|---|---|
| QTAN0079 – Buttons, Sliders and Wheels Sensor Design Guide | Design Guide | 10752 |
| AN_2585: Implementing a QTouch PTC Subsystem on SAMA5D2 MPU | Application Note | DS000002585 |
| AN_2472: QTouch on SAMA5D2 MPU | Application Note | DS000002472 |

## 7.6.9. Interfacing with an LCD

### 7.6.9.1. Design Schematic Example

The ATSAMA5D27-WLSOM1 features an 18-bit RGB LCD interface.

The figure below is a schematic example at main board level illustrating the interface with the AC32005 Microchip display module (WVGA LCD display module with maXTouch® technology).

In this example, several interfaces are used:

- LCD _xxx signals for display

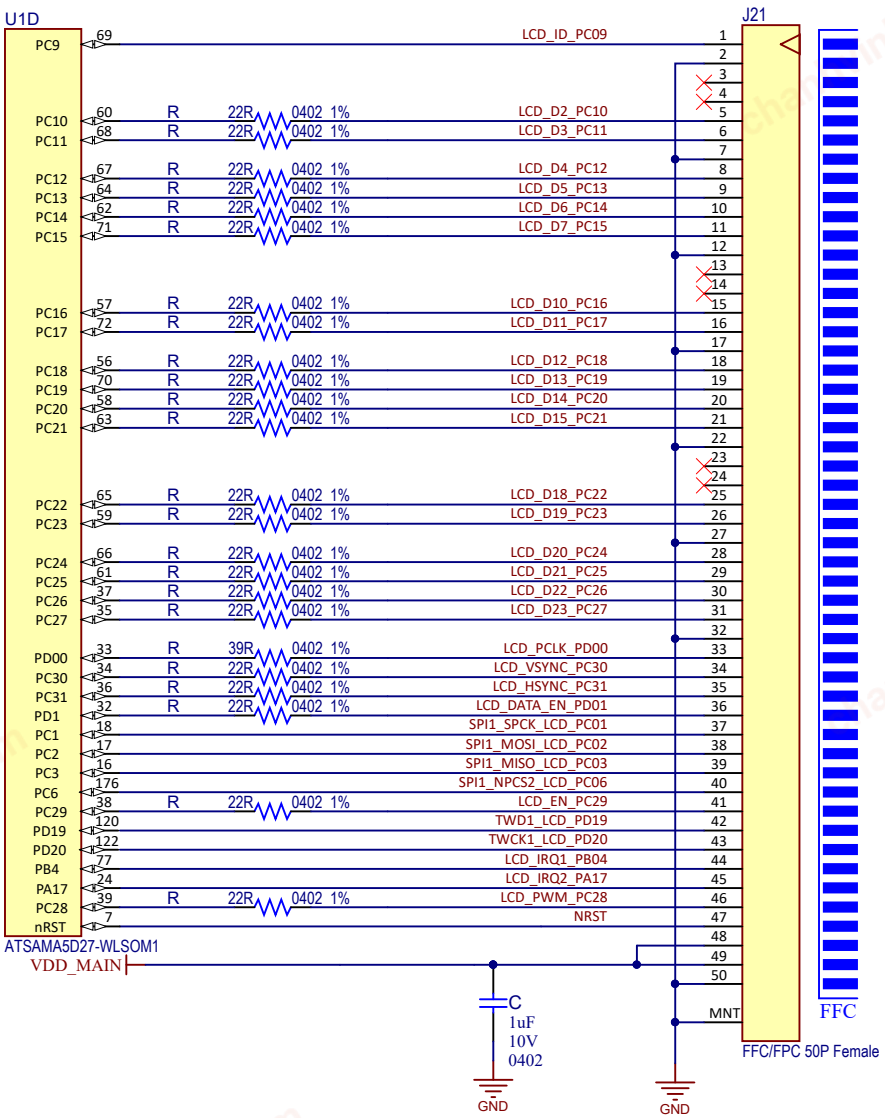

© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



- one SPI interface for display configuration
- one TWI interface for maXTouch and QTouch device control
- two IRQ I/Os for capacitive touch and buttons interruption

**Figure 7-32.** LCD Schematic Example




### 7.6.9.2. Design Layout Recommendations

When designing the LCD interface, consider the following recommendations:

- Match the LCD signal lengths to within 50 mils. Affected PIOs in the example above are PC10 to PC27, PC30, PC31, PD0 and PD1.
- Place the clock line (PD0) at least 3 times the trace width away from other signals for noise immunity.
- Place data signals at least 2 times the trace width away from any other data trace.

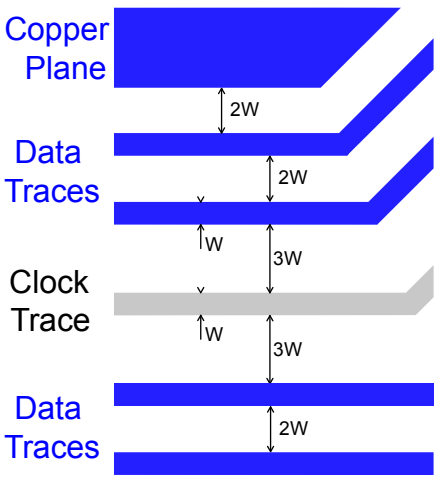

© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



- Design data signals at least 2 times the trace width away from any copper plan.

**Figure 7-33.** LCD Layout Example




### 7.6.9.3. EMI Improvement Recommendations

To reduce radiation emission, consider the following recommendations:

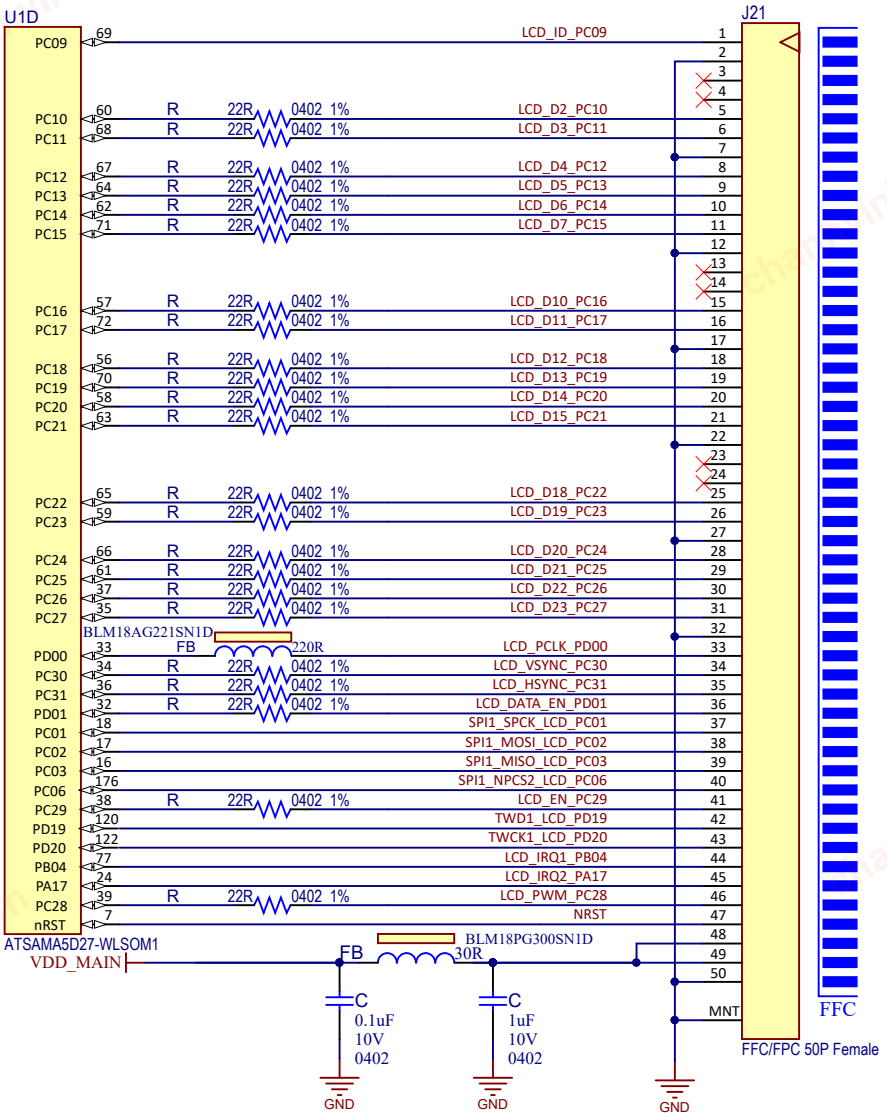
- Position the LCD bus interface in inner layers of the PCB.
- Add a ferrite bead on the CLK line.
- Add a ferrite bead on the LCD power supply.
- Select a shielded LCD connector.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 7-34.** EMI Improvement Layout Example





© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 8. Electrical Characteristics

## 8.1. Absolute Maximum Ratings

**Important:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. **Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

**Table 8-1.** Absolute Maximum Ratings

| Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| I/O Supply Voltage | VDDANA, VDDISC, VDDSDHC | -0.3 | 4.0 | V |
| Fuse Supply Voltage | VDDFUSE | -0.3 | 3.0 | V |
| Main Supply Voltage | VDD_MAIN | -0.3 | 6.0 | V |
| Backup Supply Voltage | VDDBU | -0.3 | 4.0 | V |
| Storage Temperature | $T_{STORAGE}$ | -55 | 150 | °C |
| RF Input Power Maximum | – | – | 23 | dBm |
| Maximum Input Current | VDD_MAIN | – | 2 | A |

## 8.2. Recommended Operating Conditions

The following table provides the operating ratings for the ATSAMA5D27-WLSOM1 module.

**Table 8-2.** Recommended Operating Ratings

| Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| I/O Supply Voltage | VDDANA, VDDISC, VDDSDHC | 1.6 | 3.6 | V |
| Fuse Supply Voltage | VDDFUSE | 2.25 | 2.75 | V |
| Main Supply Voltage | VDD_MAIN | 3.3 | 5.5 | V |
| Backup Supply Voltage | VDDBU | 1.65 | 3.6 | V |
| Module Operating Ambient Temperature | $T_A$ | -40 | +85 | °C |

## 8.3. Radio Performance

For more details about radio performance, refer to the ATWILC3000-MR110xA data sheet.

## 8.4. Other Characteristics

**Table 8-3.** ATSAMA5D27-WLSOM1 Other Characteristics

| Parameter | Measurement | |
|---|---|---|
| | Value | Unit |
| Weight | 7.91 | g |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 9. Mechanical Characteristics

## 9.1. Module Outline Drawings

**Figure 9-1.** ATSAMA5D27-WLSOM1 Module Drawing

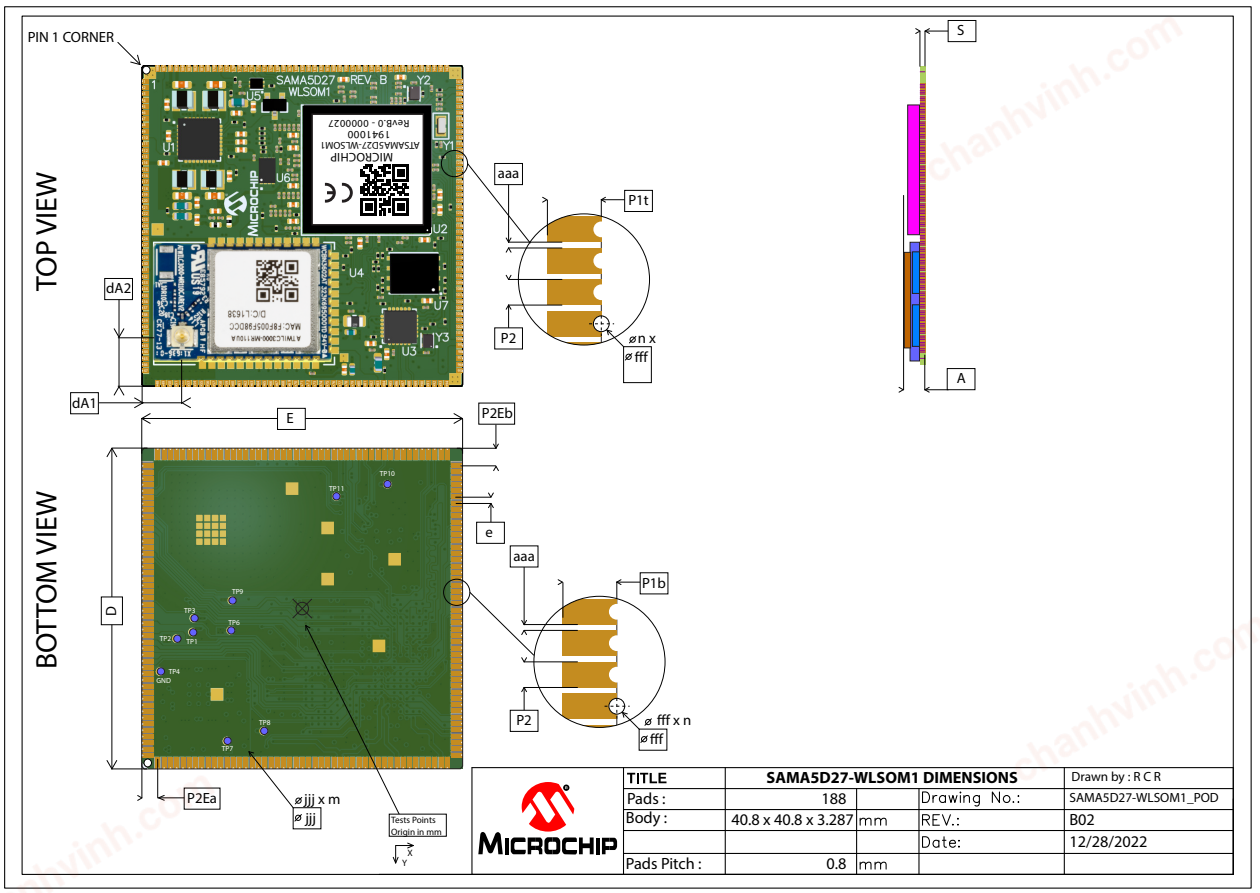



**Table 9-1.** ATSAMA5D27-WLSOM1 Module Dimensions (in mm)

| | | Symbol | Common Dimensions | | | Comments |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Body Size | X | E | 40.600 | 40.800 | 41.000 | |
| | Y | D | 40.600 | 40.800 | 41.000 | |
| Pad Pitch | | e | – | 0.800 | – | |
| PCB Thickness | | S | 1.150 | 1.200 | 1.250 | |
| Total Thickness | | A | – | 3.287 | 3.387 | |
| Pad Length | Top Side | P1t | – | 0.800 | – | |
| | Bottom Side | P1b | – | 1.500 | – | |
| Pad Width | | P2 | – | 0.600 | – | Solder Mask Defined 0.550 |
| Pad Space | | aaa | – | 0.200 | – | |
| Opening Drill Diameter | | fff | – | 0.400 | – | |
| Pad Count | | n | – | 188 | – | |
| Test Point Diameter | | jjj | – | 1.000 | – | |
| Test Point Count | | m | – | 10 | – | |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Table 9-1.** ATSAMA5D27-WLSOM1 Module Dimensions (in mm) (continued)

| | | Symbol | Common Dimensions | | | Comments |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Pad Axis to Edge | X | P2Ea | – | 2.000 | – | |
| | Y | P2Eb | – | 2.000 | – | |
| U.FL Antenna Axis to Edge | X | dA1 | – | 5.011 | – | |
| | Y | dA2 | – | 6.161 | – | |

**Note:**

1. Test points placed under the module are for production purposes only. No connection on these points is allowed. They are listed to avoid any contact with the main board vias or copper areas.

**Table 9-2.** Test Point Position Compared to Center Origin

| Test Point Number | X | Y | Voltage Point |
|---|---|---|---|
| TP1 | -13.875 | 3.000 | VDDUTMII |
| TP2 | -15.900 | 3.825 | VDD_3V3 |
| TP3 | -13.700 | 1.225 | VDDOSC_PLL |
| TP4 | -17.975 | 8.000 | GND |
| TP6 | -9.025 | 2.775 | VDDIODDR |
| TP7 | -9.500 | 16.825 | VDDCORE |
| TP8 | -4.850 | 15.550 | VDDPLLA |
| TP9 | -8.875 | -1.025 | VLDO1 |
| TP10 | 10.825 | -15.800 | VDDA_3V3 |
| TP11 | 4.350 | -14.250 | VBAT |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 10. Regulatory Approval

The ATSAMA5D27-WLSOM1 is the implementation of the ATWILC3000-MR110UA module in a particular host, in this case the PCB of the ATSAMA5D27-WLSOM1.

The ATWILC3000-MR110UA module has received regulatory approval for the following countries:

- United States/FCC ID: 2ADHKWILC3000U
- Canada/ISED:
  - IC: 20266-WILC3000UA
  - HVIN: ATWILC3000-MR110UA
  - PMN: ATWILC3000-MR110UA
- Europe/CE

## 10.1. United States

ATWILC3000-MR110UA module has received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C “Intentional Radiators” single-modular approval in accordance with Part 15.212 Modular Transmitter approval. Single-modular transmitter approval is defined as a complete RF transmission sub-assembly, designed to be incorporated into another device, that must demonstrate compliance with FCC rules and policies independent of any host. A transmitter with a modular grant can be installed in different end-use products (referred to as a host, host product, or host device) by the grantee or other equipment manufacturer, then the host product may not require additional testing or equipment authorization for the transmitter function provided by that specific module or limited module device.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

A host product itself is required to comply with all other applicable FCC equipment authorization regulations, requirements, and equipment functions that are not associated with the transmitter module portion. For example, compliance must be demonstrated: to regulations for other transmitter components within a host product; to requirements for unintentional radiators (Part 15 Subpart B), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Suppliers Declaration of Conformity (SDoC) or certification) as appropriate (e.g., Bluetooth and Wi-Fi transmitter modules may also contain digital logic functions).

### 10.1.1. Labeling and User Information Requirements

The ATWILC3000-MR110UA module has been labeled with its own FCC ID number, and if the FCC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label should use the following wording:

| |
|---|
| Contains Transmitter Module FCC ID: 2ADHKWILC3000U<br>or<br>Contains FCC ID: 2ADHKWILC3000U<br>**This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.** |


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) https://apps.fcc.gov/oetcf/kdb/index.cfm

### 10.1.2. RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power listed is conducted. This transmitter is restricted for use with the specific antenna(s) tested in this application for Certification.

The antenna(s) used with this transmitter must be installed to provide a separation distance of at least 8.0 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

### 10.1.3. Approved External Antennas

To maintain modular approval in the United States, only the antenna types that have been tested shall be used. It is permissible to use different antenna, provided they are of the same antenna type, antenna gain (equal to or less than), similar in band and out-of band characteristics (consult specification sheet for cutoff frequencies).

Testing of the ATWILC3000-MR110UA module was performed with the antenna types listed in the table List of External Antennas.

### 10.1.4. Module Integration in the Host Product

Host products are to ensure continued compliance as per KDB 996369 Module Integration Guide.

## 10.2. Canada

The ATSAMA5D27-WLSOM1 module contains the ATWILC3000-MR110UA which has been certified for use in Canada under Innovation, Science, and Economic Development (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

### 10.2.1. Labeling and User Information Requirements

Labeling Requirements (from RSP-100 - Issue 11, Section 3): The host product shall be properly labeled to identify the module within the host device.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host device; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



of the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows:

Contains IC: 20266-WILC3000UA

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 5, April 2018): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

> This device contains license-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada’s license-exempt RSS(s). Operation is subject to the following two conditions:
>
> 1. This device may not cause interference;
> 2. This device must accept any interference, including interference that may cause undesired operation of the device.
>
> L’émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d’Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L’exploitation est autorisée aux deux conditions suivantes:
>
> 1. L’appareil ne doit pas produire de brouillage;
> 2. L’appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d’en compromettre le fonctionnement.

Transmitter Antenna (From Section 6.8 RSS-GEN, Issue 5, April 2018): User manuals, for transmitters shall display the following notice in a conspicuous location:

> **This radio transmitter [IC: 20266-WILC3000UA] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.**
>
> **Le présent émetteur radio [IC: 20266-WILC3000UA] a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés cidessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué pour tout type figurant sur la liste, sont strictement interdits pour l'exploitation de l'émetteur.**

Immediately following the above notice, the manufacturer shall provide a list of all antenna types which can be used with the transmitter, indicating the maximum permissible antenna gain (in dBi) and the required impedance for each antenna type.

Testing of the ATWILC3000-MR110UA module was performed with the antenna types listed in the table List of External Antennas.

### 10.2.2. RF Exposure

All transmitters regulated by Innovation, Science and Economic Development Canada (ISED) must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radio communication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

The installation of the transmitter must ensure compliance is demonstrated according to the ISED SAR procedures.

### 10.2.3. Helpful Web Sites

Innovation, Science and Economic Development Canada (ISED): http://www.ic.gc.ca/.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



## 10.3. Europe

The ATSAMA5D27-WLSOM1 module is a Radio Equipment Directive (RED) assessed radio module that is CE marked and has been manufactured and tested with the intention of being integrated into a final product.

The ATSAMA5D27-WLSOM1 module has been tested to RED 2014/53/EU Essential Requirements for Health and Safety (Article (3.1(a)), Electromagnetic Compatibility (EMC) (Article 3.1(b)), and Radio (Article 3.2) and are summarized in European Compliance Testing.

The ETSI provides guidance on modular devices in “Guide to the application of harmonized standards covering articles 3.1b and 3.2 of the Directive 2014/53/EU (RED) to multi-radio and combined radio and non-radio equipment” document available for download from the following location: http://www.etsi.org/deliver/etsi_eg/203300_203399/203367/01.01.01_60/eg_203367v010101p.pdf

To maintain conformance to the testing listed in European Compliance Testing, the module shall be installed in accordance with the installation instructions in this data sheet and shall not be modified.

When integrating a radio module into a completed product the integrator becomes the manufacturer of the final product and is therefore responsible for demonstrating compliance of the final product with the essential requirements against the RED.

### 10.3.1. Labeling and User Information Requirements

The label on the final product which contains the ATSAMA5D27-WLSOM1 module must follow CE marking requirements.

### 10.3.2. Conformity Assessment

From ETSI Guidance Note EG 203367, section 6.1 Non-radio products are combined with a radio product:

If the manufacturer of the combined equipment installs the radio product in a host non-radio product in equivalent assessment conditions (i.e. host equivalent to the one used for the assessment of the radio product) and according to the installation instructions for the radio product, then no additional assessment of the combined equipment against article 3.2 of the RED is required.

The European Compliance Testing listed in the table below was performed using the antennas listed in the table List of External Antennas.

**Table 10-1.** European Compliance Testing

| Certification | Standards | Article |
|---|---|---|
| Safety | EN 62368 | 3.1(a) |
| Health | EN 300 328 / EN 62311 / EN 62479 | |
| EMC | EN 301 489-1 / EN 55032 / EN 55024 | 3.1(b) |
| Radio | EN 300 328 | 3.2 |

### 10.3.3. Simplified EU Declaration of Conformity

Hereby, Microchip Technology Inc. declares that the radio equipment type [ATSAMA5D27-WLSOM1] is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following internet address : https://www.microchip.com/wwwproducts/en/ATSAMA5D27-WLSOM1

### 10.3.4. Helpful Web Sites

A document that can be used as a starting point in understanding the use of Short Range Devices (SRD) in Europe is the European Radio Communications Committee (ERC) Recommendation 70-03 E, which can be downloaded from the European Communications Committee (ECC) at: http://www.ecodocdb.dk/


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



Additional helpful web sites are:

- Radio Equipment Directive (2014/53/EU):
  - https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/rtte_de
- European Conference of Postal and Telecommunications Administrations (CEPT):
  - http://www.cept.org
- European Telecommunications Standards Institute (ETSI):
  - http://www.etsi.org
- European Communications Committee (ECC):
  - http://www.ecodocdb.dk
- The Radio Equipment Directive Compliance Association (REDCA):
  - http://www.redca.eu/

## 10.4. Approved Antenna Types

ATWILC3000-MR110UA was tested and approved for use with the antennas listed in the table below.

Different antenna may be used, provided they are of the identical antenna type and antenna gain (equal to or less than) and have similar in-band and out-of-band characteristics (consult specification sheet for cutoff frequencies).

If other antenna types are used, the OEM installer must authorize the antenna with respective regulatory agencies and ensure its compliance.

**Table 10-2.** List of External Antennas[1]

| P/N | Vendor | Antenna Gain @ 2.4 GHz Band | Antenna Type | ATWILC3000-MR110UA | | Cable Length/ Remarks |
|---|---|---|---|---|---|---|
| | | | | FCC[2] [3] ISED | CE | |
| W3525B039 | Pulse Electronics Corporation | 2 dBi | PCB | X | X | 100 mm |
| RFDPA870920IMLB301 | WALSIN | 1.84 dBi | Dipole | X | X | 200 mm |
| RFA-02-P33 | Aristotle | 2 dBi | PCB | X | X | 150 mm |
| RN-SMA-S | Microchip | 0.56 dBi | Dipole | X | X | SMA to u.FL cable length of 100 mm [2] [3] |
| RFA-02-D3 | Aristotle | 2 dBi | Dipole | X | X | 150 mm |
| RFA-02-G03 | Aristotle | 2 dBi | Metal Stamp | X | X | 150 mm |
| RFA-02-L2H1 | Aristotle | 2 dBi | Dipole | X | X | 150 mm |
| RFA-02-P05 | Aristotle | 2 dBi | PCB | X | X | 150 mm |
| RFA-02-C2M2 | Aristotle | 2 dBi | Dipole | X | X | SMA to u.FL cable length of 100 mm [2] [3] |
| 86254 | Delock | 2 dBi | PCB | – | X | 50 mm |

**Notes:**

1. X = Covered under the certification.
2. If the end product using the module is designed to have an antenna port that is accessible to the end user, then a unique (nonstandard) antenna connector (refer to FCC KDB 353028) must be used; for example, Reverse Polarity - SMA.
3. If an RF coaxial cable is used between the module RF output and the enclosure, then a unique (nonstandard) antenna connector must be used in the enclosure wall for interface with antenna.

### 10.4.1. Antenna Placement Recommendations

Particular attention must be given to the placement of the antenna and its cable. The following recommendations must be applied:


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



- Ensure that the antenna cable is not expected to be routed over circuits generating electrical noise on the Host board.
- Antenna should not be placed in direct contact or in close proximity of the plastic casing/objects.
- Do not enclose the antenna within a metal shield.
- Keep any components which may radiate noise, signals or harmonics within the 2.4 GHz to 2.5 GHz frequency band away from the antenna and, if possible, shield those components. Any noise radiated from the host board in this frequency band degrades the sensitivity of the module.
- It is highly recommended not to run the antenna cable alongside or underneath the module. It is preferred that the cable is routed straight out of the module.
- The antenna should preferably be placed at a distance greater than 5 cm away from the module. The figure below indicates the area where the antenna should not be placed.

This recommendation is based on an open air measurement and does not take into account by any metal shielding of the customer end product. When a metal enclosure is used, the antenna can be located closer to the ATSAMA5D27-WLSOM1 module.

The drawing below indicates how the antenna cable should be routed depending on the location of the antenna with respect to the ATSAMA5D27-WLSOM1 PCB. Two possible options for the optimum routing of the cable are described.

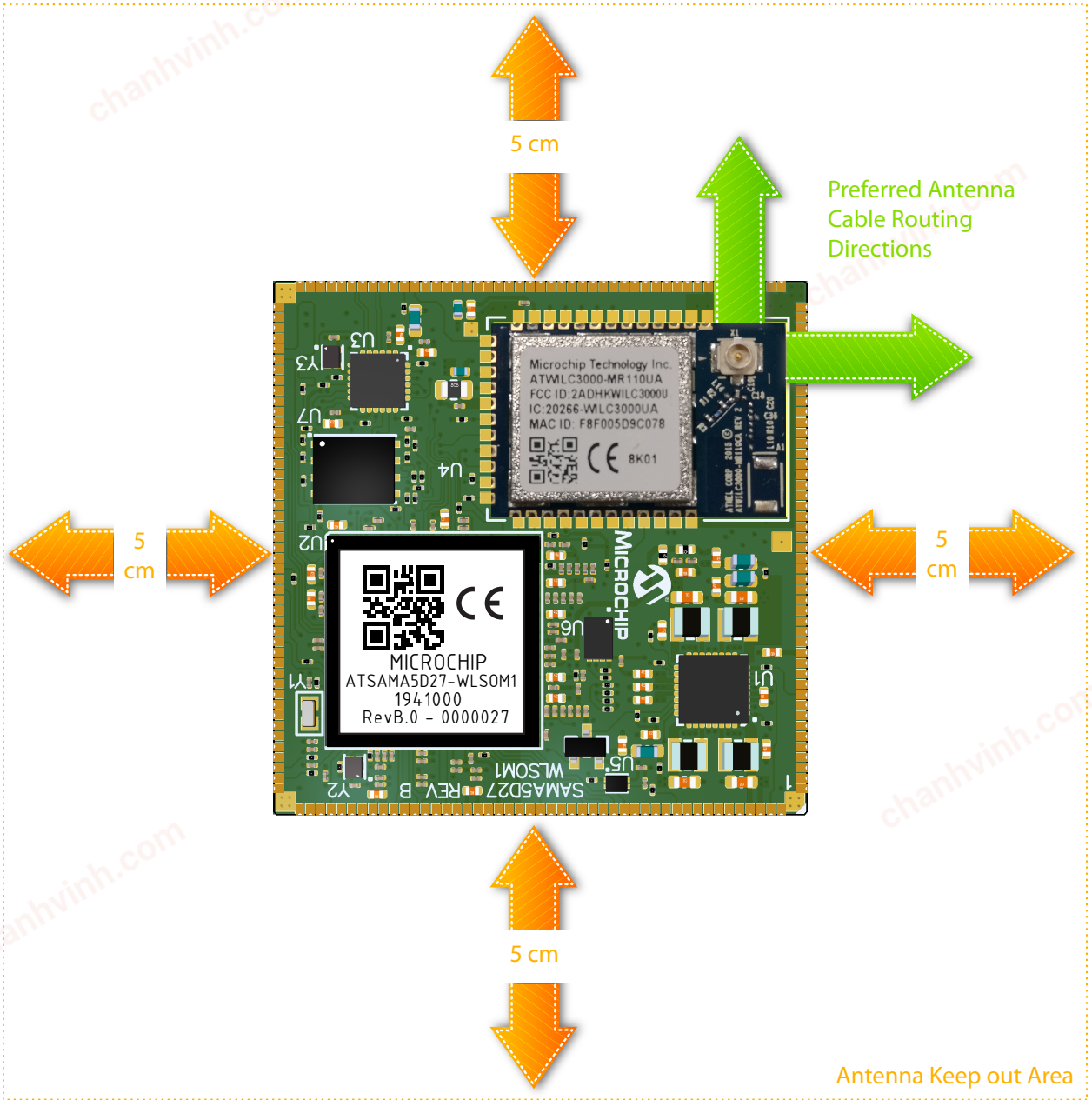
These guidelines are generic only; customers need to check and fine tune the antenna positioning in the final host product.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



**Figure 10-1.** ATSAMA5D27-WLSOM1 Antenna Placement





© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 11. Ordering Information

| Ordering Code[1] | Package | Description | Regulatory Information | Carrier Type | Module Ambient Temperature Range |
|---|---|---|---|---|---|
| ATSAMA5D27-WLSOM1 | 40.8 x 40.8 x 3.287 mm | Certified Microchip MPU Wireless module with ATSAMA5D27C-LD2G-CU, WILC3000 and U.FL connector | FCC, ISED, CE | Tray | -40°C to +85°C |

**Note:**

1. For details on the ordering code, see Product Identification System.

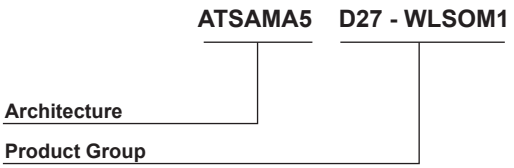

© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 12. Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.




| | | |
|---|---|---|
| Architecture: | ATSAMA5 | = Arm Cortex-A5 CPU |
| Product Group: | D27-WLSOM1 | Certified MPU Wireless module with SAMA5D27, WILC3000 and U.FL connector |

Example:

- ATSAMA5D27-WLSOM1 = System-On-Module (SOM) based on the SAMA5D27, with 2 Gb LPDDR2-SDRAM running up to 500 MHz, and a Wi-Fi/BT Wireless module


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# 13. Revision History

## 13.1. Rev. F - 01/2026

Updated body size minimum and maximum values in Table 9-1.
Added Design Resources section.
Updated Pin List introduction.
Updated Ordering Information.
Updated Table 10-1 in Conformity Assessment.

## 13.2. Rev. E - 01/2024

Updated Pad No. columns in PIOA Pin Description, PIOB Pin Description, PIOC Pin Description, PIOD Pin Description.
Updated pins NRST (7) and WKUP (187) descriptions in System Pins Description.
Updated Figure 7-25.
Updated text and figures in SAMA5D27 System-In-Package.
Added MPU Clocks.
Updated text and figures in Power Management Unit.
Updated Figure 7-2.
Updated figure in Power Architecture.
Updated figure in Power Configurations: Single Supply and Power Configurations: Multiple Supplies.
Updated text and figure in Ethernet Phy.
Updated figure in Radio Subsystem.
Updated Recommended Operating Conditions.
Updated ATSAMA5D27-WLSOM1 Module Drawing.
Deleted 6.2 Module Land Pattern (Host Board PCB Footprint) and 7. Assembly and Storage Information. This information is now available in the Microchip application note *SAMA5D27-WLSOM Power Consumption*.

## 13.3. Rev. D - 08/2021

Updated Table 10-1.

## 13.4. Rev. C - 03/2021

**Note:** Microchip is in the process of implementing inclusive language in our documentation. During this update, you may see the old terms and the new terms in our documentation text. We apologize for any confusion.

Throughout: Updated all secure element references to ATECC608B (was ATECC608A).
Updated Pin List and PIOA, PIOB, PIOC and PIOD pin description tables.
Updated Secure Element.
Updated figure in Power Architecture.
Updated figure in Power Configurations: Multiple Supplies.
Updated figure in Baseboard Power Delivery Application Diagram Example.
PIO muxing tables moved from External Interfaces to Pin List.
Updated schematic and EMI example in Interfacing with an LCD.
Added Power Consumption.
Updated link to ATWILC3000 data sheet in Radio Performance.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



## 13.5. Rev. B - 12/2019

Updated Figure 6-1.
Updated pins 151, 152 in Pin Description: System.
Updated figure in Secure Element.
Updated figure in Power Architecture.
Updated Ethernet Phy.
Modified component reference in Radio Subsystem.
Updated Interfacing with an SD Card.
Updated Interfacing with e-MMC.
Updated Interfacing with NAND Flash.
Updated Interfacing with an Image Sensor Controller (ISC).
Updated Interfacing with CLASS-D Audio Output.
Added QTouch® Peripheral Touch Controller (PTC).
Added Interfacing with an LCD.
Section 4.7 content moved to Regulatory Approval.
Updated Radio Performance.
Updated Figure 9-1.
Updated ATSAMA5D27-WLSOM1 Land Pattern Drawing.
Added new section Regulatory Approval.
Updated Regulatory Information in Ordering Information.

## 13.6. Rev. A - 10/2019

First issue.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



# Microchip Information

## Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-2584-8

## Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

## Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.


© 2026 Microchip Technology Inc. and its subsidiaries

chanhvinh.com



## Product Page Links

ATSAMA5D27-WLSOM1

chanhvinh.com


© 2026 Microchip Technology Inc. and its subsidiaries