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Features

- Number of Keys:
  - Comms Mode: 1 to 12 keys (1 to 9 if wheel or slider option enabled)
  - Standalone Mode: 1 to 5 keys
- Technology:
  - Patented spread-spectrum QTouchADC charge-transfer
- Number of Output Lines:
  - Comms Mode: Up to 10 channels can be configured as outputs (but they will replace the keys)
  - Standalone Mode: 1 to 5 channels can be configured as outputs
- Key Outline Sizes:
  - 5 mm x 5 mm or larger (panel thickness dependent)
- Key Spacings:
  - 6 mm or wider, center to center (panel thickness, human factors dependent)
- Key Design:
  - Single solid or ring shaped electrodes; widely different sizes and shapes possible
- Proximity Electrode Design:
  - Single solid electrodes; Key Design, Loop, PCB Trace - different sizes and shapes possible
- Wheel Size:
  - Typically 30 mm – 50 mm diameter
- Wheel Electrode Design:
  - Spatially interpolated wheel up to 80 mm diameter
  - Typical width of segments 12 mm
- Slider Electrode Design:
  - Spatially interpolated, resistorless design
  - Typical length 50 mm – 100 mm, typical width 12 mm
  - Can be an arc or other irregular shape
- Substrates:
  - FR-4, low cost CEM-1 or FR-2 PCB materials; polyamide FPCB; PET films, glass
- Adjacent Metal:
  - Compatible with grounded metal immediately next to keys
- Layers Required:
  - One; electrodes and components can be on same side
- Electrode Materials:
  - Etched copper, silver, carbon, indium tin oxide (ITO), PEDOT
- Panel Materials:
  - Plastic, glass, composites, painted surfaces (nonconductive paints)
- Key Panel Thickness:
  - Up to 15 mm glass (key size dependent)
  - Up to 10 mm plastic (key size dependent)
- Wheel/slider Panel Thickness:
  - Up to 4 mm glass
  - Up to 3 mm plastic
- Key Sensitivity:
  - Comms Mode – individually settable via simple commands over I^2C interface
  - Standalone mode – settings are fixed
- Interface:
  - I^2C slave mode (400 kHz)
  - CHANGE status indication pin
- Signal Processing:
  - Self-calibration, Auto drift compensation, Noise filtering, Adjacent Key Suppression® (AKS®)
- Power:
  - 1.8 V to 5.5 V
- Packages:
  - 20-pin SOIC/TSSOP RoHS compliant IC
  - 20-pad VQFN RoHS compliant IC

Atmel®

QTouch 12-channel Touch Sensor IC

AT42QT2120

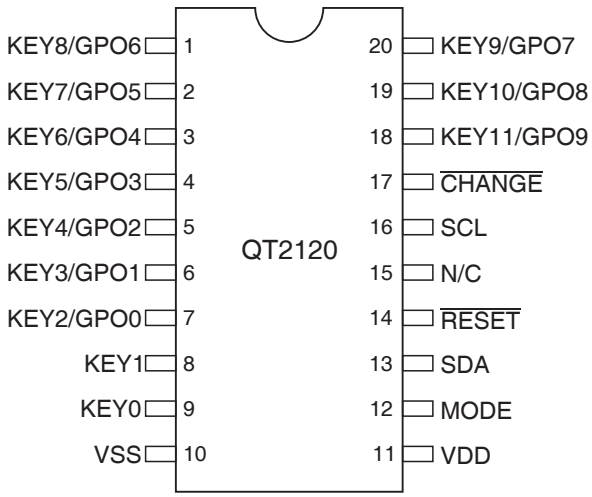
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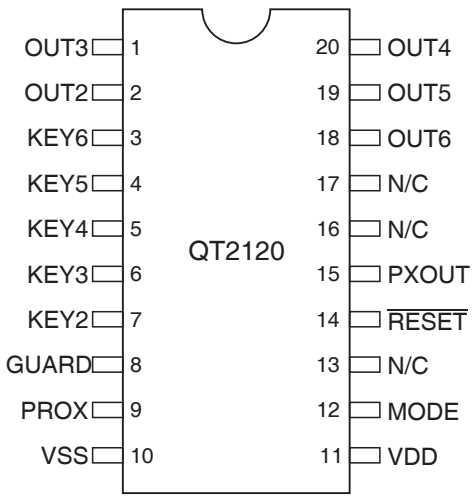
1. Pinouts and Schematics

1.1 Pinouts

1.1.1 20-pin SOIC/TSSOP – Comms Mode

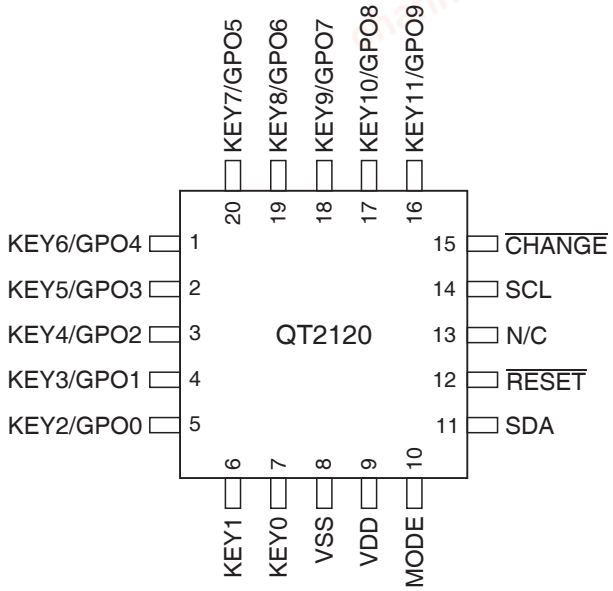


1.1.2 20-pin SOIC/TSSOP – Standalone Mode

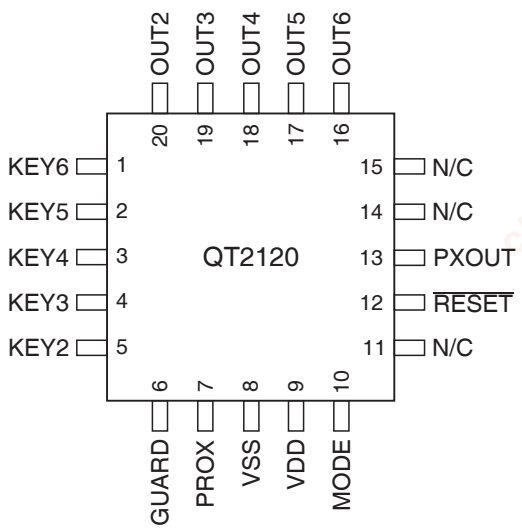


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1.1.3 20-pin VQFN – Comms Mode



1.1.4 20-pin VQFN – Standalone Mode



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1.2 Pin Descriptions

1.2.1 20-pin SOIC/TSSOP

Table 1-1. Pin Listings (20-pin SOIC/TSSOP)

Pin	Name (Comms)	Name (Standalone)	Type	Description	If Unused...
1	KEY8/ GPO6	OUT3	I/O	Comms mode: Key 8 / General-purpose output Standalone mode: push-pull output for key 3	Leave open
2	KEY7/ GPO5	OUT2	I/O	Comms mode: Key 7 / General-purpose output Standalone mode: push-pull output for key 2	Leave open
3	KEY6/ GPO4	KEY6	I/O	Comms mode: Key 6 / General-purpose output Standalone mode: Key 6	Leave open
4	KEY5/ GPO3	KEY5	I/O	Comms mode: Key 5 / General-purpose output Standalone mode: Key 5	Leave open
5	KEY4/ GPO2	KEY4	I/O	Comms mode: Key 4 / General-purpose output Standalone mode: Key 4	Leave open
6	KEY3/ GPO1	KEY3	I/O	Comms mode: Key 3 / General-purpose output Standalone mode: Key 3	Leave open
7	KEY2/ GPO0	KEY2	I/O	Comms mode: Key/slider/wheel 2 / General-purpose output Standalone mode: Key 2	Leave open
8	KEY1	GUARD	I/O	Comms mode: Key/slider/wheel 1 Standalone mode: Guard channel	Leave open
9	KEY0	PROX	I/O	Comms mode: Key/slider/wheel 0 Standalone mode: Proximity channel	Leave open
10	VSS	VSS	P	Ground	–
11	VDD	VDD	P	Power	–
12	MODE	MODE	I	Mode selection pin Comms mode: connect to Vss Standalone mode: connect to Vdd	–
13	SDA	N/C	OD	Comms mode: Serial Interface Data Standalone mode: Unused	Pull up to Vdd
14	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	I	Active low reset; has internal pull-up 60 kΩ resistor	Tie to Vdd
15	N/C	PXOUT	O	Comms mode: no connection Standalone mode: open drain output for proximity channel	Leave open
16	SCL	N/C	OD	Comms mode: Serial Interface Clock Standalone mode: Unused	Pull up to Vdd
17	$\overline{\text{CHANGE}}$	N/C	OD	Comms mode: Active low state change interrupt (external pull-up resistor needed) Standalone mode: Unused	Pull up to Vdd
18	KEY11/ GPO9	OUT6	I/O	Comms mode: Key 11 / General-purpose output Standalone mode: push-pull output for key 6	Leave open
19	KEY10/ GPO8	OUT5	I/O	Comms mode: Key 10 / General-purpose output Standalone mode: push-pull output for key 5	Leave open
20	KEY9/ GPO7	OUT4	I/O	Comms mode: Key 9 / General-purpose output Standalone mode: push-pull output for key 4	Leave open

I Input only I/O Input and output OD Open drain output P Ground or power

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1.2.2 20-pin VQFN

Table 1-2. Pin Listings (20-pin VQFN)

Pin	Name (Comms)	Name (Standalone)	Type	Description	If Unused...
1	KEY6/ GPO4	KEY6	I/O	Comms mode: Key 6 / General-purpose output Standalone mode: Key 6	Leave open
2	KEY5/ GPO3	KEY5	I/O	Comms mode: Key 5 / General-purpose output Standalone mode: Key 5	Leave open
3	KEY4/ GPO2	KEY4	I/O	Comms mode: Key 4 / General-purpose output Standalone mode: Key 4	Leave open
4	KEY3/ GPO1	KEY3	I/O	Comms mode: Key 3 / General-purpose output Standalone mode: Key 3	Leave open
5	KEY2/ GPO0	KEY2	I/O	Comms mode: Key/slider/wheel 2 / General-purpose output Standalone mode: Key 2	Leave open
6	KEY1	GUARD	I/O	Comms mode: Key/slider/wheel 1 Standalone mode: Guard channel	Leave open
7	KEY0	PROX	I/O	Comms mode: Key/slider/wheel 0 Standalone mode: Proximity channel	Leave open
8	VSS	VSS	P	Ground	–
9	VDD	VDD	P	Power	–
10	MODE	MODE	I	Mode selection pin Comms mode: connect to Vss Standalone mode: connect to Vdd	–
11	SDA	N/C	OD	Comms mode: Serial Interface Data Standalone mode: Unused	Pull up to Vdd
12	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	I	Active low reset; has internal pull-up 60 kΩ resistor	Tie to Vdd
13	N/C	PXOUT	OD	Comms mode: no connection Standalone mode: open drain output for proximity channel	Leave open
14	SCL	N/C	OD	Comms mode: Serial Interface Clock Standalone mode: Unused	Pull up to Vdd
15	$\overline{\text{CHANGE}}$	N/C	OD	Comms mode: Active low state change interrupt (external pull-up resistor needed) Standalone mode: Unused	Pull up to Vdd
16	KEY11/ GPO9	OUT6	I/O	Comms mode: Key 11 / General-purpose output Standalone mode: push-pull output for key 6	Leave open
17	KEY10/ GPO8	OUT5	I/O	Comms mode: Key 10 / General-purpose output Standalone mode: push-pull output for key 5	Leave open
18	KEY9/ GPO7	OUT4	I/O	Comms mode: Key 9 / General-purpose output Standalone mode: push-pull output for key 4	Leave open
19	KEY8/ GPO6	OUT3	I/O	Comms mode: Key 8 / General-purpose output Standalone mode: push-pull output for key 3	Leave open
20	KEY7/ GPO5	OUT2	I/O	Comms mode: Key 7 / General-purpose output Standalone mode: push-pull output for key 2	Leave open

I Input only I/O Input and output OD Open drain output P Ground or power O Output only

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1.3 Schematics

Figure 1-1. 20-pin SOIC/TSSOP – Comms Mode

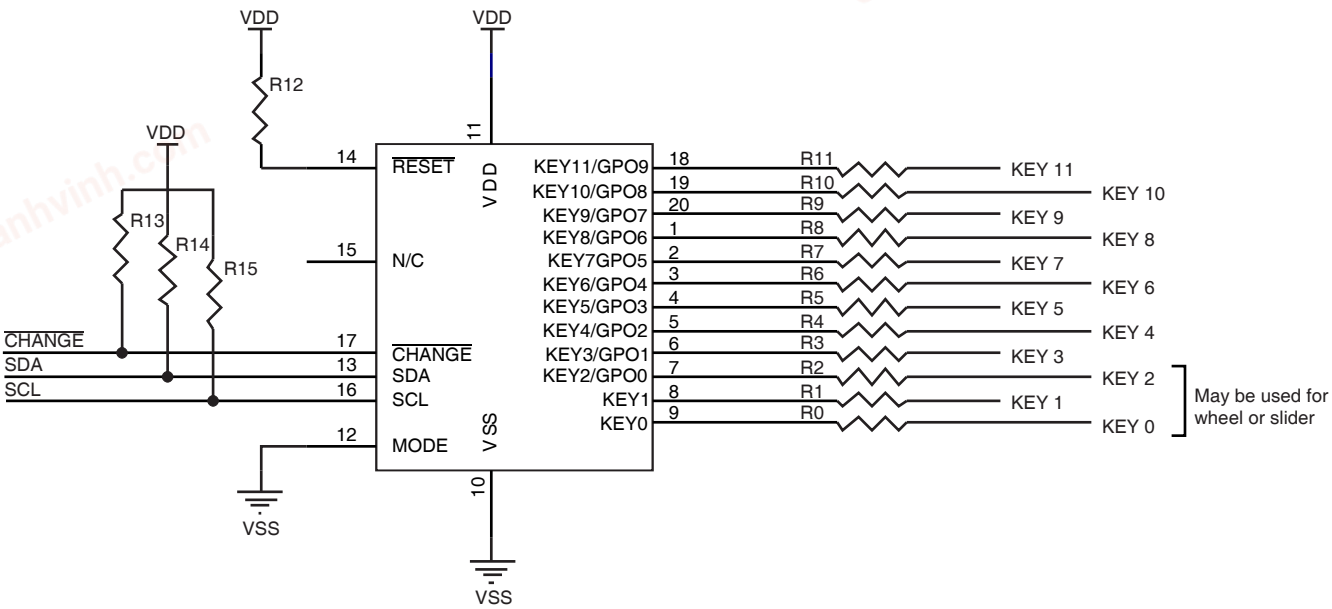
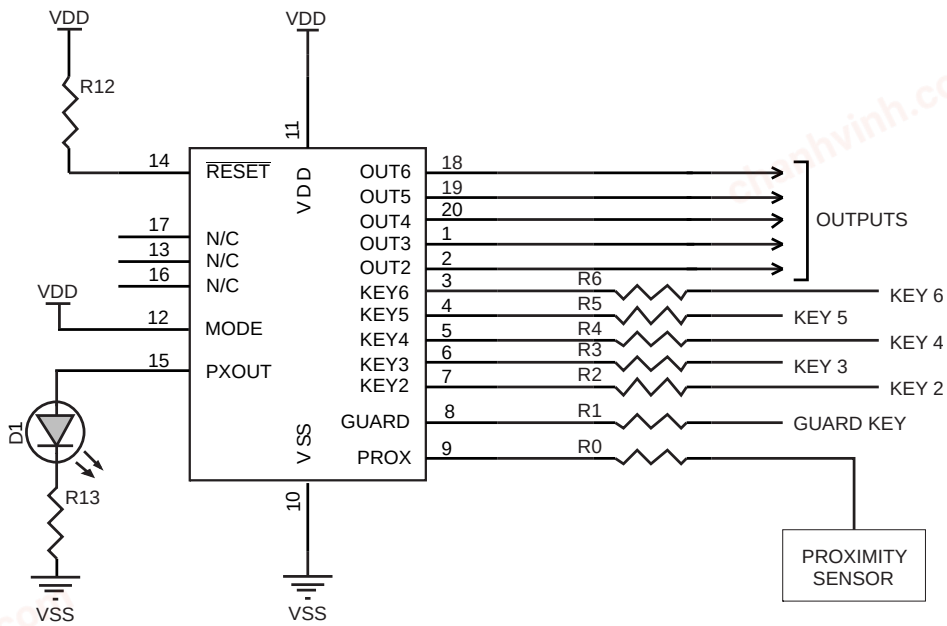


Figure 1-2. 20-pin SOIC/TSSOP – Standalone Mode



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Figure 1-3. 20-pin VQFN – Comms Mode

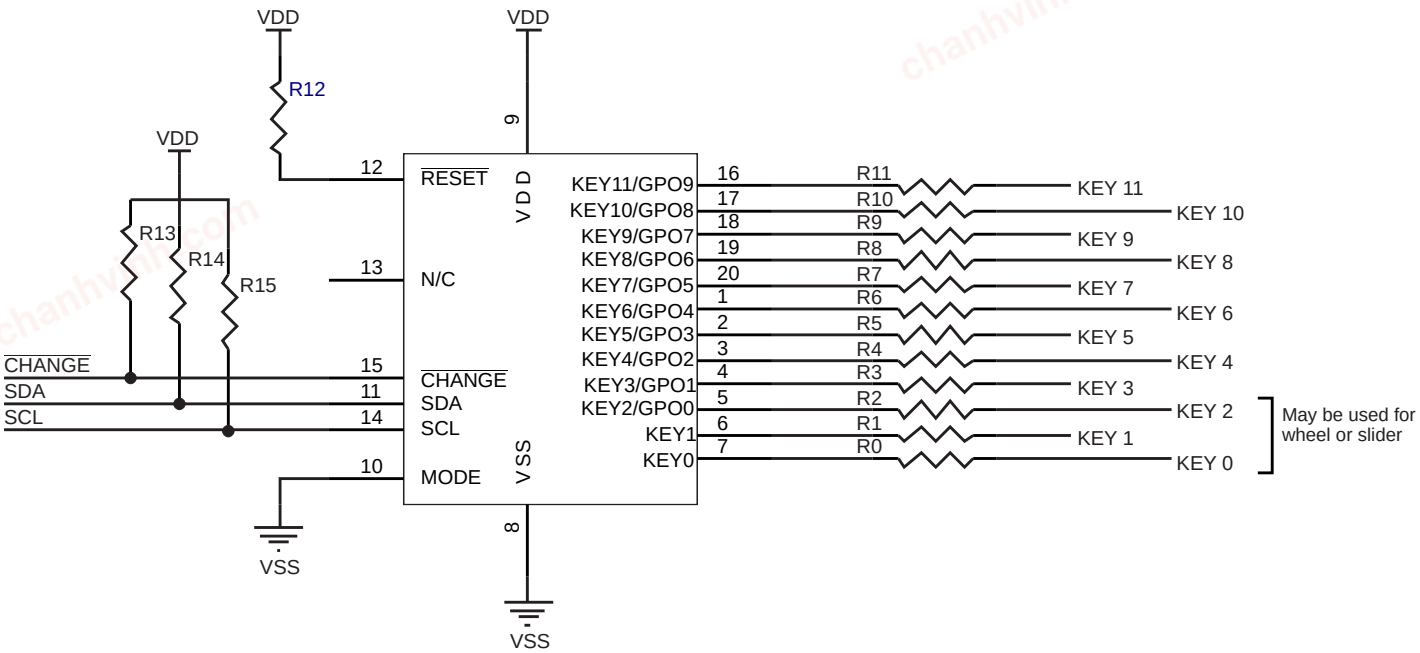
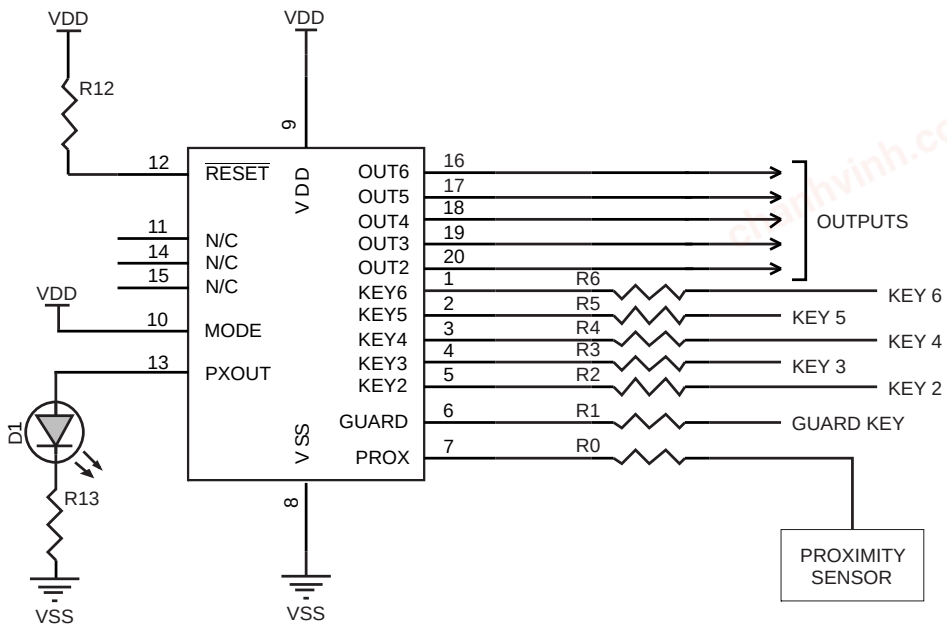


Figure 1-4. 20-pin VQFN – Standalone Mode



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2. Overview

2.1 Introduction

The AT42QT2120 (QT2120) is a QTouchADC sensor driver. The device can sense from one to 12 keys, dependent on mode. Three of the keys can be used as sense channels for a slider or wheel, leaving a maximum of nine standard touch keys. The device also supports the use of proximity sensors and a guard channel.

The QT2120 includes all signal processing functions necessary to provide stable sensing under a wide variety of changing conditions, and the outputs are fully debounced. Only a few external parts are required for operation and no external Cs capacitors are required.

The QT2120 modulates its bursts in a spread-spectrum fashion in order to heavily suppress the effects of external noise, and to suppress RF emissions. The QT2120 uses a QTouchADC method of acquisition. This provides greater noise immunity and eliminates the need for external sampling capacitors, allowing touch sensing using a single pin.

The QT2120 can operate in two ways; comms and standalone.

2.2 Modes

2.2.1 Comms Mode

The QT2120 can operate in comms mode where a host can communicate with the device via an I^2C bus. This allows the user to configure settings such as Threshold, Adjacent Key Suppression (AKS), Detect Integrator, Low Power (LP) Mode, Guard Channel and Max Time On for keys.

2.2.2 Standalone Mode

The QT2120 can operate in a standalone mode where an I^2C-compatible interface is not required. To enter standalone mode, connect the Mode pin to Vdd before powering up the QT2120.

In standalone mode, the start-up values are hard coded in firmware and cannot be changed. The default start-up values are used. This means that key detection is reported via its respective input/output.

The Guard channel feature is automatically implemented on key 1 in standalone mode. This means that this channel has a higher sensitivity and is used to protect against false triggering, perhaps by a hand covering all keys.

A proximity sensor is also available on channel (key) 0 in standalone mode.

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2.3 Keys

Dependent on mode, the QT2120 can have a minimum of one key and a maximum of 12 keys. These can be constructed in different shapes and sizes. See "Features" on page 1 for the recommended dimensions.

The possible combinations of keys are:

Comms mode:

- 1 to 12 keys

  or

- 1 to 9 keys plus 1 slider/wheel
- Key channels 2 to 11 can be reassigned as general outputs, if required

Note: Any number of keys can be configured as proximity channels.

Standalone mode:

- 1 to 5 keys plus corresponding discrete outputs
- 1 Guard Channel
- 1 Proximity sensor

Unused keys should be disabled by setting bit 0 of their control bytes to 1 (see Section 5.17 on page 26).

The Key Status register (see Section 5.5 on page 21) can be read to determine the touch status of the corresponding key. It is recommended using the open-drain $\overline{\text{CHANGE}}$ line to detect when a change of status has occurred.

2.4 Output Lines

In comms mode some pins, normally used for touch keys, can be used as output pins. If the Key Control bit 0 (EN) is set to 1, the pin can be used as an output. The state of the pin is then controlled by Key Control bit 1 (GPO).

In Standalone mode pins OUT2 to OUT6 are driven by KEY2 to KEY6 respectively. The OUT pins drive high during touch and can be used to drive, for example, LEDs.

2.5 Acquisition/Low Power Mode (LP)

There are 255 different acquisition times possible. These are controlled via the LP Mode byte (see Section 5.9 on page 22) which can be written to via I^2C-compatible communication.

LP mode controls the intervals between acquisition measurements. Longer intervals consume lower power but have an increased response time. During calibration, touch and during the detect integrator (DI) period, the LP mode is temporarily set to LP mode 1 for a faster response.

The QT2120 operation is based on a fixed cycle time of approximately 16 ms. The LP mode setting indicates how many of these periods exist per measurement cycle. For example, If LP mode = 1, there is an acquisition every cycle (16 ms). If LP mode = 3, there is an acquisition every 3 cycles (48 ms). If a high PULSE setting is selected then the acquisition time may exceed 16 ms.

An LP setting of 0 will send the device into Power-down mode. To wake the device from this mode a nonzero LP setting should be written to the LP address at location 8.

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2.6 Adjacent Key Suppression (AKS) Technology

The device includes the Atmel patented Adjacent Key Suppression (AKS) technology, to allow the use of tightly spaced keys on a keypad with no loss of selectability by the user.

There can be up to three AKS groups, implemented so that only one key in the group may be reported as being touched at any one time. Once a key in a particular AKS group is in detect no other key in that group can go into detect. Only when the key in detect goes out of detection can another key go into detect state.

Keys which are members of the AKS groups can be set in the Key Control register (see Section 5.17 on page 26). Keys outside the group may be in detect simultaneously.

Note: To use a key as a guard channel, its AKS group should be set to be the same as that of the keys it is to protect.

2.7 $\overline{\text{CHANGE}}$ Line (Comms Mode Only)

The $\overline{\text{CHANGE}}$ line is active low and signals when there is a change of state in the Detection Status and/or Key Status bytes. It is cleared (allowed to float high) when the host reads the status bytes.

If the status bytes change back to their original state before the host has read the status bytes (for example, a touch followed by a release), the $\overline{\text{CHANGE}}$ line will be held low. In this case, a read to any memory location will clear the $\overline{\text{CHANGE}}$ line.

The $\overline{\text{CHANGE}}$ line is open-drain and should be connected via a 47 kΩ resistor to Vdd. It is necessary for minimum power operation as it ensures that the QT2120 can sleep for as long as possible. Communications wake up the QT2120 from sleep causing a higher power consumption if the part is randomly polled.

Note that the $\overline{\text{CHANGE}}$ line is pulled low 85 ms after power-up or reset. The $\overline{\text{CHANGE}}$ line is pulled low approximately for another 16 ms before any bursting on the touch pins will occur. If any of the pins are required to be outputs then the relevant Key Control settings should be written within this 16 ms time to prevent bursting on pins required as outputs. Also note that the $\overline{\text{CHANGE}}$ line is cleared during a read of the Detection Status bytes when all bytes differing from the previous read have been read.

2.8 Types of Reset

2.8.1 External Reset

An external reset logic line can be used if desired, fed into the $\overline{\text{RESET}}$ pin. However, under most conditions it is acceptable to tie $\overline{\text{RESET}}$ to Vdd. The minimum reset pulse width is 2 µs.

2.8.2 Soft Reset

The host can cause a device reset by writing a nonzero value to the Reset byte. This soft reset triggers the internal watchdog timer on a 125 ms interval. After 125 ms the device executes a full reset.

The device NACKs any attempts to communicate with it for approximately 200 ms after the soft reset command. Communication can begin as soon the $\overline{\text{CHANGE}}$ line is first asserted.

Note: The device can process a Soft Reset command while in Power Down (LPM = 0) mode, causing a chip reset.

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2.9 Calibration

Writing a nonzero value to the calibration byte can force a recalibration at any time. This can be useful to clear out a stuck key condition after a prolonged period of uninterrupted detection. A calibration command executes 15 burst cycles at LPM 1 and sets the CALIBRATE bit of the Detection Status register during the calibration sequence.

Note: A calibration command should be sent whenever Key Control bit 0 (EN) is changed. This changes the use of the key from a standard touch key to an output pin and vice-versa.

2.10 Guard Channel

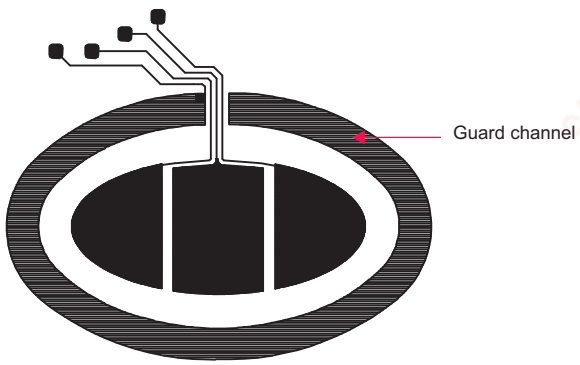
A guard channel to help prevent false detection is available in both modes. This is fixed on key 1 for standalone mode and programmable for comms mode by setting Key Control bit 4 (GUARD) (see Section 5.17 on page 26).

Guard channel keys should be more sensitive than the other keys and physically bigger. Because the guard channel key is physically bigger it becomes more susceptible to noise so it should have a higher Oversampling (see Section 5.18 on page 27) than the other keys. In standalone mode it is assigned to key 1 and cannot be changed.

In comms mode any key can be selected to be a guard key by setting Key Control bit 4 (GUARD).

The guard channel is connected to a sensor pad which detects the presence of touch. Because of its larger size and sensitivity it goes into touch before the keys it surrounds (if, for example, a hand covers all the keys).

Figure 2-1. Guard Channel Example



2.11 Signal Processing

2.11.1 Detect Threshold

The device detects a touch when the signal has crossed a threshold level and remained there for a specified number of counts (see Section 5.11 on page 24). This can be altered on a key-by-key basis using the key Detect Threshold I^2C-compatible commands.

This detect threshold is based on the reference value of the particular key. The delta of the key is obtained by subtracting the reference value from the signal value (the signal value rises when touch is present).

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In standalone mode the detect threshold is set to a fixed value of 10 counts of change with respect to the internal reference level for the guard channel and 10 counts for the other six keys (including proximity channel). The reference level has the ability to adjust itself slowly in accordance with the drift compensation mechanism.

The drift mechanism will drift toward touch at a rate of 160 ms x 20 = 3.2 seconds (Towards Touch Drift (TTD) register) and away from touch at a rate of 160 ms x 5 = 0.8 seconds (Away from Touch Drift (ATD) register). These values are fixed in standalone mode but can be configured in comms mode see Section 5.10 on page 22.

2.11.2 Detect Integrator

The device features a fast detection integrator counter (DI filter), which acts to filter out noise at the small expense of a slower response time. The DI filter requires a programmable number of consecutive samples confirmed in detection before the key is declared to be touched. The minimum number for the DI filter is 1. A setting of 0 for the DI also defaults to 1. The DI has a maximum usable value of 32. Values above this will prevent a key from entering touch.

The DI is also implemented when a touch is removed.

2.11.3 Cx Limitations

The recommended range for key capacitance Cx is 1 pF – 30 pF. Larger values of Cx will give reduced sensitivity.

2.11.4 Touch Recalibration Delay

If an object or material obstructs the sense pad the signal may rise enough to create a detection, preventing further operation. To prevent this, the sensor includes a timer which monitors detections. If a detection exceeds the timer setting the sensor performs a key recalibration. This is known as the Touch Recalibration Delay (TRD) and is set to approximately 30 s in standalone mode.

In comms mode this feature can be changed by setting a value in the range 1 – 255 (160 ms – 40,800 ms) in steps of 160 ms. A setting of 0 disables the TRD.

TRD is a global setting and applies to all keys.

2.11.5 Away from Touch Recalibration

If a keys signal jumps in the negative direction (with respect to its reference) by more than the Away from Touch Recalibration setting (25% of detect threshold), then a recalibration of that key takes place.

Note: The minimum Away from Touch Recalibration is hard limited to 4 counts.

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2.11.6 Drift Hold Time

Drift Hold Time (DHT) is used to restrict drift on all keys while one or more keys are activated. DHT restricts the drifting on all keys until approximately four seconds after all touches have been removed.

This feature is particularly useful in cases of high-density keypads where touching a key or hovering a finger over the keypad would cause untouched keys to drift, and therefore create a sensitivity shift, and ultimately inhibit touch detection. In Comms mode this value is settable, see Section 5.13 on page 24.

The QT2120 will remain in fast mode (LP = 1) for the duration of the DHT counter. The total DHT time is 160 ms × DHT value. The default setting for DHT is 25, so 160 ms × 25 = ~4 seconds. The QT2120 will not drift or re-enter slow LP mode during this time.

2.11.7 Hysteresis

Hysteresis is fixed at 12.5% of the Detect Threshold. When a key enters a detect state once the DI count has been reached, the Detect threshold (DTHR) value is changed by a small amount (12.5% of DTHR) in the direction away from touch. This is done to effect hysteresis and so makes it less likely a key will dither in and out of detect. DTHR is restored once the key drops out of detect.

Note: The minimum value for hysteresis is 2 counts.

3. Wiring and Parts

3.1 Rs Resistors

Series resistors Rs (Rs0 – Rs11 for comms mode and Rs0 – Rs6 for standalone mode) are in line with the electrode connections and should be used to limit electrostatic discharge (ESD) currents and to suppress radio frequency interference (RFI). Series resistors are recommended for noise reduction. They should be approximately 4.7 kΩ to 20 kΩ each. For maximum noise rejection the value may be up to 100 kΩ. Care should be taken in this case that the sensor keys are fully charged. The Charge Time may need to be increased (see Section 5.15 on page 26). Each count increase will extend the charge pulse by approximately 1 µs.

3.2 LED Traces and Other Switching Signals

Digital switching signals near the sense lines induce transients into the acquired signals, deteriorating the signal-to-noise (SNR) performance of the device. Such signals should be routed away from the sensing traces and electrodes, or the design should be such that these lines are not switched during the course of signal acquisition (bursts).

LED terminals which are multiplexed or switched into a floating state, and which are within, or physically very near, a key (even if on another nearby PCB) should be bypassed to either Vss or Vdd with at least a 10 nF capacitor. This is to suppress capacitive coupling effects which can induce false signal shifts. The bypass capacitor does not need to be next to the LED, in fact it can be quite distant. The bypass capacitor is noncritical and can be of any type.

LED terminals which are constantly connected to Vss or Vdd do not need further bypassing.

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3.3 PCB Cleanliness

Modern no-clean flux is generally compatible with capacitive sensing circuits.

> CAUTION: If a PCB is reworked to correct soldering faults relating to the device, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

If a PCB is reworked in any way, clean it thoroughly to remove all traces of the flux residue around the capacitive sensor components. Dry it thoroughly before any further testing is conducted.

3.4 Power Supply

See Section 6.2 on page 30 for the power supply range. If the power supply fluctuates slowly with temperature, the device tracks and compensates for these changes automatically with only minor changes in sensitivity. If the supply voltage drifts or shifts quickly, the drift compensation mechanism is not able to keep up, causing sensitivity anomalies or false detections.

The power should be clean and come from a separate regulator if possible. However, this device is designed to minimize the effects of unstable power, and except in extreme conditions should not require a separate Low Dropout (LDO) regulator.

> **CAUTION:** A regulator IC shared with other logic can result in erratic operation and is **not** advised.
>
> A single ceramic 0.1 µF bypass capacitor, with short traces, should be placed very close to the power pins of the IC. Failure to do so can result in device oscillation, high current consumption and erratic operation.

It is assumed that a larger bypass capacitor (like 1 µF) is somewhere else in the power circuit; for example, near the regulator.

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4. I²C-compatible Communications (Comms Mode Only)

4.1 I²C-compatible Protocol

4.1.1 Protocol

The I²C-compatible protocol is based around access to an address table (see Table 5-1 on page 18) and supports multibyte reads and writes. The maximum clock rate is 400 kHz.

See Section A on page 41 for an overview of I²C bus operation.

4.1.2 Signals

The I²C-compatible interface requires two signals to operate:

- **SDA** – Serial Data
- **SCL** – Serial Clock

A third line, $\overline{\text{CHANGE}}$, is used to signal when the device has seen a change in the status byte:

- **$\overline{\text{CHANGE}}$:** Open-drain, active low when the device status has changed since the last I²C read. After reading the four status bytes (1) (or all the status bytes which have changed since the previous read), this pin floats (high) again if it is pulled up with an external resistor. If the status bytes change back to their original state before the host has read the status bytes (for example, a touch followed by a release), the $\overline{\text{CHANGE}}$ line is held low. In this case, a read to any memory location clears the $\overline{\text{CHANGE}}$ line.

4.2 I²C-compatible Address

There is one preset I²C-compatible address of 0x1C (28). This is not changeable.

4.3 Data Read/Write

4.3.1 Address Pointer

The internal address pointer is initialized to address 0.

4.3.2 Writing Data to the Device

The sequence of events required to write data to the device is shown next.



Table 4-1. Description of Write Data Bits

Key	Description
S	START condition
SLA+W	Slave address plus write bit
A	Acknowledge bit
MemAddress	Target memory address within device
Data	Data to be written
P	Stop condition

1. Detection Status Byte, Key Status Byte[0], Key Status Byte[1], Slider Position

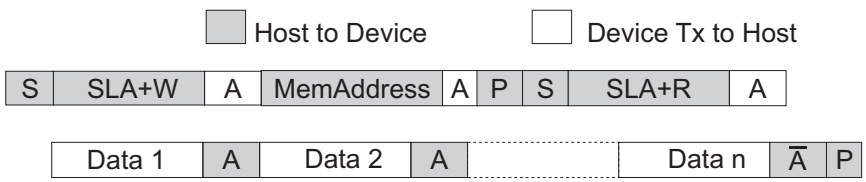
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1. The host initiates the transfer by sending the START condition
2. The host follows this by sending the slave address of the device together with the WRITE bit.
3. The device sends an ACK.
4. The host then sends the memory address within the device it wishes to write to.
5. The device sends an ACK.
6. The host transmits one or more data bytes; each is acknowledged by the device (unless trying to write to an invalid address). Valid write address are 5 – 51.
7. If the host sends more than one data byte, they are written to consecutive memory addresses.
8. The device automatically increments the target memory address after writing each data byte.
9. After writing the last data byte, the host should send the STOP condition.

Note: the host should not try to write to addresses outside the range 0x06 to 0x33 (6 – 51) because this is the limit of the device's internal memory address.

4.3.3 Reading Data From the Device

The sequence of events required to read data from the device is shown next.



1. The host initiates the transfer by sending the START condition
2. The host follows this by sending the slave address of the device together with the WRITE bit.
3. The device sends an ACK.
4. The host then sends the memory address within the device it wishes to read from.
5. The device sends an ACK if the address to be read from is less than 0x63 otherwise it sends a NACK).
6. The host must then send a STOP and a START condition followed by the slave address again but this time accompanied by the READ bit.

Note: Alternatively, instead of step 6, a repeated START can be sent so the host does not need to relinquish control of the bus.

7. The device returns an ACK, followed by a data byte.
8. The host must return either an ACK or NACK.
   a. If the host returns an ACK, the device subsequently transmits the data byte from the next address. Each time a data byte is transmitted, the device automatically increments the internal address. The device continues to return data bytes until the host responds with a NACK.
   b. If the host returns a NACK, it should then terminate the transfer by issuing the STOP condition.
9. The device resets the internal address to the location indicated by the memory address sent to it previously. Therefore, there is no need to send the memory address again when reading from the same location.

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Note: Reading the 16-bit reference and signal values is not an automatic operation; reading the first byte of a 16-bit value does not lock the other byte. As a result glitches in the reported value may be seen as values increase from 255 to 256, or decrease from 256 to 255. This device also supports the use of a repeated START condition as an alternative to the Stop condition.

4.4 SDA, SCL

The I^2C-compatible bus transmits data and clock with SDA and SCL respectively. They are open-drain; that is I^2C-compatible master and slave devices can only drive these lines low or leave them open. The termination resistors pull the line up to Vdd if no I^2C-compatible device is pulling it down.

The termination resistors commonly range from 1 kΩ to 10 kΩ and should be chosen so that the rise times on SDA and SCL meet the I^2C-compatible specifications (300 ns maximum for 400 kHz operation).

4.5 Standalone Mode

If I^2C-compatible communications are not required, then standalone mode can be enabled by connecting the MODE pin to Vdd. See Section 2.4 on page 9 for more information.

In Standalone mode (Mode pin connected to Vdd at start-up) the chip is configured to specific settings:

- Key0 is configured as a proximity channel. If this key goes into detect then PXOUT is asserted high.
- Key1 is configured as a guard channel and should have a PCB layout which reflects this.
- Keys 2 – 6 are standard QTouchADC keys and have pins OUT 2 – 6 configured to reflect their respective touch status.
- Keys1 – 6 are configured to have the same AKS group setting.

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5. Setups

5.1 Introduction

The device calibrates and processes signals using a number of algorithms specifically designed to provide for high survivability in the face of adverse environmental challenges. User-defined Setups are employed to alter these algorithms to suit each application. These Setups are loaded into the device over the I^2C-compatible serial interfaces. In standalone mode these settings are fixed to predetermined values.

Table 5-1. Internal Register Address Allocation

Address	Use	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
0	Chip ID	Chip Id = 0x3E (62)								R
1	Firmware Version	Major version				Minor version				R
2	Detection Status	CALIBRATE	OVERFLOW	–	–	–	–	SDET	TDET	R
3	Key Status	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0	R
4		Reserved				KEY11	KEY10	KEY9	KEY8	R
5	Slider Position	Slider position								R
6	Calibrate	Calibrate Command								R/W
7	$\overline{\text{Reset}}$	Reset Command								R/W
8	LP	Low Power (LP) Mode								R/W
9	TTD	0	Towards Touch Drift compensation							R/W
10	ATD	0	Away from Touch Drift compensation							R/W
11	DI	Detection integrator								R/W
12	TRD	Touch Recal Delay								R/W
13	DHT	Drift Hold Time								R/W
14	Slider Options	EN	WHEEL	Reserved						R/W
15	Charge Time	Reserved				Charge Time				–
16	Key 0 Detect Threshold	Detect Threshold level for key 0								R/W
17	Key 1 Detect Threshold	Detect Threshold level for key 1								R/W
18	Key 2 Detect Threshold	Detect Threshold level for key 2								R/W
19	Key 3 Detect Threshold	Detect Threshold level for key 3								R/W
20	Key 4 Detect Threshold	Detect Threshold level for key 4								R/W
21	Key 5 Detect Threshold	Detect Threshold level for key 5								R/W
22	Key 6 Detect Threshold	Detect Threshold level for key 6								R/W
23	Key 7 Detect Threshold	Detect Threshold level for key 7								R/W
24	Key 8 Detect Threshold	Detect Threshold level for key 8								R/W
25	Key 9 Detect Threshold	Detect Threshold level for key 9								R/W
26	Key 10 Detect Threshold	Detect Threshold level for key 10								R/W
27	Key 11 Detect Threshold	Detect Threshold level for key 11								R/W
28	Key 0 Control	Reserved			GUARD	AKS		GPO	EN	R/W
29	Key 1 Control	Reserved			GUARD	AKS		GPO	EN	R/W
30	Key 2 Control	Reserved			GUARD	AKS		GPO	EN	R/W

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Table 5-1. Internal Register Address Allocation (Continued)

Address	Use	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
31	Key 3 Control	Reserved			GUARD	AKS		GPO	EN	R/W
32	Key 4 Control	Reserved			GUARD	AKS		GPO	EN	R/W
33	Key 5 Control	Reserved			GUARD	AKS		GPO	EN	R/W
34	Key 6 Control	Reserved			GUARD	AKS		GPO	EN	R/W
35	Key 7 Control	Reserved			GUARD	AKS		GPO	EN	R/W
36	Key 8 Control	Reserved			GUARD	AKS		GPO	EN	R/W
37	Key 9 Control	Reserved			GUARD	AKS		GPO	EN	R/W
38	Key 10 Control	Reserved			GUARD	AKS		GPO	EN	R/W
39	Key 11 Control	Reserved			GUARD	AKS		GPO	EN	R/W
40	Key 0 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
41	Key 1 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
42	Key 2 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
43	Key 3 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
44	Key 4 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
45	Key 5 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
46	Key 6 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
47	Key 7 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
48	Key 8 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
49	Key 9 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
50	Key 10 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
51	Key 11 Pulse Scale	PULSE3	PULSE2	PULSE1	PULSE0	SCALE3	SCALE2	SCALE1	SCALE0	R/W
52–53	Key Signal 0	Key signal 0 (MSByte) – Key signal 0 (LSByte)								R
54–55	Key Signal 1	Key signal 1 (MSByte) – Key signal 1 (LSByte)								R
56–57	Key Signal 2	Key signal 2 (MSByte) – Key signal 2 (LSByte)								R
58–59	Key Signal 3	Key signal 3 (MSByte) – Key signal 3 (LSByte)								R
60–61	Key Signal 4	Key signal 4 (MSByte) – Key signal 4 (LSByte)								R
62–63	Key Signal 5	Key signal 5 (MSByte) – Key signal 5 (LSByte)								R
64–65	Key Signal 6	Key signal 6 (MSByte) – Key signal 6 (LSByte)								R
66–67	Key Signal 7	Key signal 7 (MSByte) – Key signal 7 (LSByte)								R
68–69	Key Signal 8	Key signal 8 (MSByte) – Key signal 8 (LSByte)								R
70–71	Key Signal 9	Key signal 9 (MSByte) – Key signal 9 (LSByte)								R
72–73	Key Signal 10	Key signal 10 (MSByte) – Key signal 10 (LSByte)								R
74–75	Key Signal 11	Key signal 11 (MSByte) – Key signal 11 (LSByte)								R
76–77	Reference Data 0	Reference data 0 (MSByte) – Reference data 0 (LSByte)								R
78–79	Reference Data 1	Reference data 1 (MSByte) – Reference data 1 (LSByte)								R
80–81	Reference Data 2	Reference data 2 (MSByte) – Reference data 2 (LSByte)								R
82–83	Reference Data 3	Reference data 3 (MSByte) – Reference data 3 (LSByte)								R
84–85	Reference Data 4	Reference data 4 (MSByte) – Reference data 4 (LSByte)								R

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Table 5-1. Internal Register Address Allocation (Continued)

Address	Use	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
86–87	Reference Data 5	Reference data 5 (MSByte) – Reference data 5 (LSByte)								R
88–89	Reference Data 6	Reference data 6 (MSByte) – Reference data 6 (LSByte)								R
90–91	Reference Data 7	Reference data 7 (MSByte) – Reference data 7 (LSByte)								R
92–93	Reference Data 8	Reference data 8 (MSByte) – Reference data 8 (LSByte)								R
94–95	Reference Data 9	Reference data 9 (MSByte) – Reference data 9 (LSByte)								R
96–97	Reference Data 10	Reference data 10 (MSByte) – Reference data 10 (LSByte)								R
98–99	Reference Data 11	Reference data 11 (MSByte) – Reference data 11 (LSByte)								R

5.2 Address 0: Chip ID

Table 5-2. Chip ID

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	CHIP ID							

CHIP ID: Holds the chip ID; always 0x3E.

5.3 Address 1: Firmware Version

Table 5-3. Firmware Version

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	MAJOR VERSION				MINOR VERSION			

MAJOR VERSION: Holds the major firmware version (for example revision 1.5).

MINOR VERSION: Holds the minor firmware version (for example revision 1.5).

5.4 Address 2: Detection Status

Table 5-4. Detection Status

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2	CALIBRATE	OVERFLOW	–	–	–	–	SDET	TDET

CALIBRATE: This bit is set during a calibration sequence.

OVERFLOW: This bit is set if the time to acquire all key signals exceeds 16 ms.

SDET: This bit is set if any of the slider/wheel channels are in detect.

TDET: This bit is set if any of the keys are in detect.

Note: If the slider or wheel is enabled then the SDET bit will be set when it is in detect. Also the relevant Key Status bit (0 – 2) and TDET will be set. These bits can be ignored if the SDET bit is set as the slider/wheel takes priority.

A change in these bytes will cause the $\overline{\text{CHANGE}}$ line to trigger.

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5.5 Addresses 3 – 4: Key Status

Table 5-5. Key Status

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
4	Reserved				KEY11	KEY10	KEY9	KEY8

KEY0 – KEY11: These bits indicate which keys are in detection, if any. Touched keys report as 1, untouched or disabled keys report as 0. A change in these bytes will cause the $\overline{\text{CHANGE}}$ line to trigger.

5.6 Address 5: Slider Position

Table 5-6. Slider Position

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5	SLIDER POSITION							

SLIDER POSITION: Reports the slider/wheel position. This value is only valid when the SDET bit in the Detection Status byte is set. A change in this value will cause the $\overline{\text{CHANGE}}$ line to assert low.

5.7 Address 6: Calibrate

Table 5-7. Calibrate

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6	CALIBRATE COMMAND							

CALIBRATE COMMAND: Writing any nonzero value into this address triggers the device to start a calibration cycle. The CALIBRATE flag in the detection status register is set when the calibration begins and clears when the calibration has finished.

5.8 Address 7: Reset

Table 5-8. Reset

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7	RESET COMMAND							

RESET COMMAND: Writing any nonzero value to this address triggers the device to reset.

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5.9 Address 8: Low Power (LP) Mode

Table 5-9. LP Mode

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8	LP MODE							

LP MODE: This 8-bit value determines the number of 16 ms intervals between key measurements. Longer intervals between measurements yield a lower power consumption but at the expense of a slower response to touch.

Setting	Time
0	Power Down
1	16 ms
2	32 ms
3	48 ms
4	64 ms
...254	4.064 s
255	4.08 s

Default: 1 (16 ms between key acquisitions)

To wake the device from Power-down mode a nonzero LP setting should be written to this address. The QT2120 can also be reset during power-down mode by writing a nonzero value to the reset register (address 7).

5.10 Address 9 – 10: Toward Touch and Away from Touch Drift (TTD, ATD)

Table 5-10. Toward Touch and Away from Touch Drift

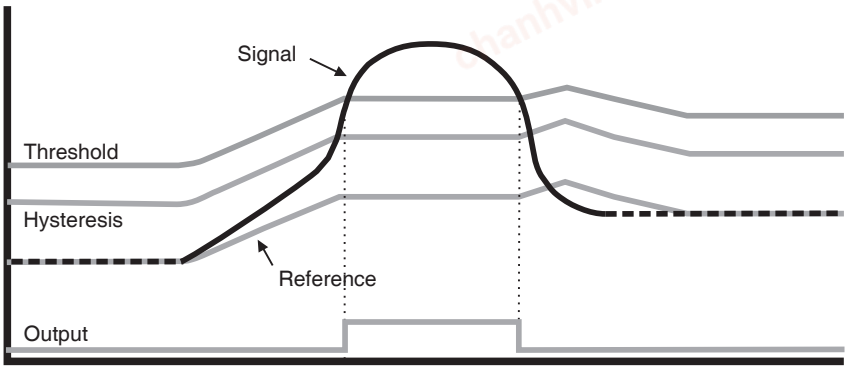
Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9	0	TOWARD TOUCH DRIFT						
10	0	AWAY FROM TOUCH DRIFT						

TOWARD TOUCH DRIFT and **AWAY FROM TOUCH DRIFT**: Signals can drift because of changes in Cx and Cs over time and temperature. It is crucial that such drift be compensated for, else false detections and sensitivity shifts can occur.

Drift compensation (see Figure 5-1) is performed by making the reference level track the raw signal at a slow rate, but only while there is no detection in effect. The rate of adjustment must be performed slowly, otherwise legitimate detections could be ignored. The parameters can be configured in increments of 0.16s.

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Figure 5-1. Thresholds and Away From Touch Drift



The device drift compensates using a slew-rate limited change to the reference level; the threshold and hysteresis values are slaved to this reference.

When a finger is sensed, the signal increases due to capacitance being added to Cx. An isolated, untouched foreign object (a coin, or a water film) will cause the signal to drop very slightly due to an enhancement of coupling.

Once a finger is sensed, the drift compensation mechanism ceases since the signal is legitimately detecting an object. Drift compensation only works when the signal in question has not crossed the negative threshold level.

The drift compensation mechanism can be asymmetric; the drift-compensation can be made to occur in one direction faster than it does in the other simply by changing the TTD and ATD Setup parameters. This is a global configuration.

Specifically, drift compensation should be set to compensate faster for decreasing signals than for increasing signals. Increasing signals should not be compensated quickly, since an approaching finger could be compensated for partially or entirely before even touching the touchpad (Toward Touch Drift (TTD)).

However, an obstruction over the sense pad, for which the sensor has already made full allowance, could suddenly be removed leaving the sensor with an artificially suppressed reference level and thus become insensitive to touch. In this latter case, the sensor should compensate for the object's removal by lowering the reference level relatively quickly (Away from Touch Drift (ATD)).

Drift compensation and the detection time-outs work together to provide for robust, adaptive sensing. The time-outs provide abrupt changes in reference calibration depending on the duration of the signal 'event'.

If ATD or TTD is set to 0 then the drift compensation in the respective direction is disabled.

Note: it is recommended that the drift compensation rate be more than four times the LP mode period. This is to prevent undersampling, which decreases the algorithm's efficiency.

Default TTD: 20 (3.2 s / reference level)

Default ATD: 5 (0.8 s / reference level)

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5.11 Address 11: Detection Integrator (DI)

Table 5-11. Detection Integrator

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11	DI							

DI: Allows the DI level to be set for each key. This 8-bit value controls the number of consecutive measurements that must be confirmed as having passed the key threshold before that key is registered as being in detect. The minimum value for the DI filter is 1. A settings of 0 for the DI also defaults to 1.

Default: 4 (maximum = 32)

5.12 Address 12: Touch Recal Delay (TRD)

Table 5-12. Touch Recal Delay

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12	TRD							

If an object unintentionally contacts a key resulting in a detection for a prolonged interval it is usually desirable to recalibrate the key in order to restore its function, perhaps after a time delay of some seconds.

The Touch Recal Delay timer monitors such detections; if a detection event exceeds the timer's setting, the key will be automatically recalibrated. After a recalibration has taken place, the affected key will once again function normally even if it is still being contacted by the foreign object. This feature is set globally.

TRD can be disabled by setting it to zero (infinite timeout) in which case the key will never autorecalibrate during a continuous detection (but the host could still command it).

TRD is set globally, which can range in value from 1 – 255. TRD above 0 is expressed in 0.16 s increments.

Default: 255 (Comms) 255 (Standalone)

5.13 Address 13: Drift Hold Time (DHT)

Table 5-13. Drift Hold Time

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
13	DHT							

This is used to restrict drift on all keys while one or more keys are activated. DHT defines the length of time the drift is halted after a key detection. When DHT = 0, drifting is never suspended, even during a valid touch of another key.

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This feature is particularly useful in cases of high-density keypads where touching a key or hovering a finger over the keypad would cause untouched keys to drift, and therefore create a sensitivity shift, and ultimately inhibit any touch detection. It is expressed in 0.16 s increments.

DHT default value: 25

DHT range: 0 – 255

5.14 Address 14: Slider Options

Table 5-14. Slider Options

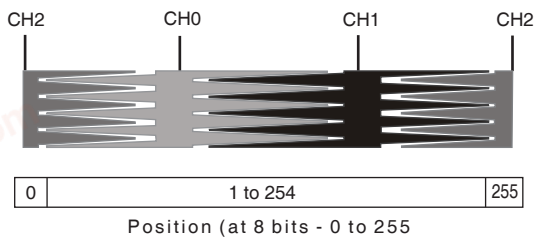
Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14	EN	WHEEL	Reserved					

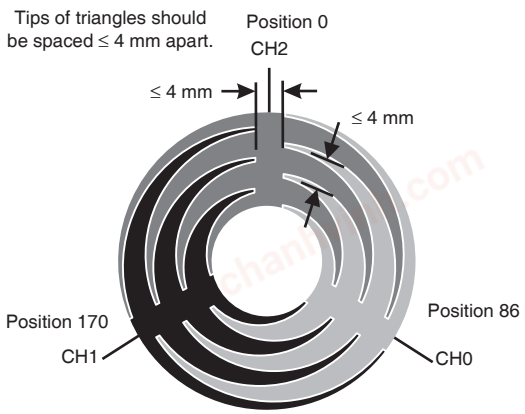
EN: Setting this bit enables a Slider or Wheel to be configured. Only the first three channels (0, 1 and 2) can be used.

WHEEL: Setting this bit allows a wheel to be configured. If not set, and EN is enabled, it defaults to a slider.

The range of both is from 0 – 255.

Figure 5-2. Slider/Wheel Settings





EN default value: 0

WHEEL default value: 0

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5.15 Address 15: Charge Time

Table 5-15. Charge Time

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
15	CHARGE TIME							

Prolongs the charge-transfer period of signal acquisition by 1 µs per count.

Allows full charge-transfer for keys with heavy Rs / Cx loading.

Range: 0 – 255

Default: 0

5.16 Address 16 – 27: Detect Threshold (DTHR)

Table 5-16. Detect Threshold

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16	DTHR KEY 0							
:	:							
27	DTHR KEY 11							

DTHR KEY 0 – DTHR KEY 11: these 8-bit values set the threshold value for each key to register a detection.

Default: 10 counts

Note: Do not use a setting of 0 as this causes a key to go into detection when its signal is equal to its reference.

5.17 Addresses 28 – 39: Key Control

Table 5-17. Key Control

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
28	Reserved			GUARD	AKS		GPO	EN
:	:							
39	Reserved			GUARD	AKS		GPO	EN

GUARD: If set to 1, this key will act as a guard channel. A key set as a guard key does not affect the Detection Status or Key Status register and the $\overline{\text{CHANGE}}$ line is not asserted if this key goes into detect.

AKS: These bits control which keys are included in an AKS group. There can be up to three groups, each containing any number of keys (up to the maximum allowed for the mode). A setting of 0 disables AKS for that key.

Each key can have a value between 0 and 3, which assigns it to an AKS group of that number. A key may only go into detect when it has the largest signal change of any key in its group. A value of 0 means the key is not in any AKS group.

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GPO: If set to 0, this key is a driven-low output. If set to 1 then the output is driven high. Setting this bit only has an effect if the EN bit is set to 1.

EN: If set to 0, indicates that this key is to be used as a touch channel. Setting this bit to 1 will disable the key for touch use and make the channel pin an output.

Note: It is not possible to enable Channel 0 or Channel 1 as an output. Setting the GPO bit on these channels will only have the effect of disabling the key. When a change is made to the EN bit a calibration cycle may occur because of the change in the signal values. It is recommended to manually initiate a calibration cycle after a change is made to the EN bit regardless of this.

Comms Defaults: All Key Control bytes set to 0x00

Standalone Defaults: Key 0 Control byte = 0x00

Key 1 Control byte = 0x14

Key 2 – 11 Control bytes = 0x04

5.18 Addresses 40 – 51: Pulse/Scale for Keys

Table 5-18. Controls for Keys

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40	PULSE				SCALE			
:					:			
51	PULSE				SCALE			

PULSE/SCALE: The PULSE/SCALE settings are used to set up a proximity key. In comms mode the proximity key is set up by configuring a key's PULSE/SCALE settings via an I^2C bus. In standalone mode, default settings make key 0 a proximity key. This cannot be changed.

These bits represent two numbers; the low nibble is SCALE, high nibble is PULSE.

Each acquisition cycle consists signal accumulation and signal averaging. PULSE determines the number of measurements accumulated, SCALE the averaging factor.

The SCALE factor (averaging factor) for the accumulated signal is an exponent of 2.

PULSE is the number of measurements accumulated and is an exponent of 2.

For example:

Oversampling is used to enhance the resolution of the Analog-to-Digital-Converter (ADC). Oversampling theory says that for each additional bit of resolution, n, the signal must be oversampled four times (or $2^2 \times n$.) If two bits of addition resolution are required then the pulse setting would be 4 ($4^2 = 2^4$). If 3-bits of additional resolution are required the Pulse setting would be 6 ($4^3 = 2^6$). Here the result of each ADC pulse measurement is taken and added to the last.

The oversampling theory also states that this accumulated result must be scaled back by a factor of 2^n. The will be the Scale value.

Table 5-19 on page 28 shows some of the recommended oversampling settings [1].

1.Other settings are possible but the Pulse value should never be more than six higher than the Scale setting as the signal result is stored in a 16-bit variable.

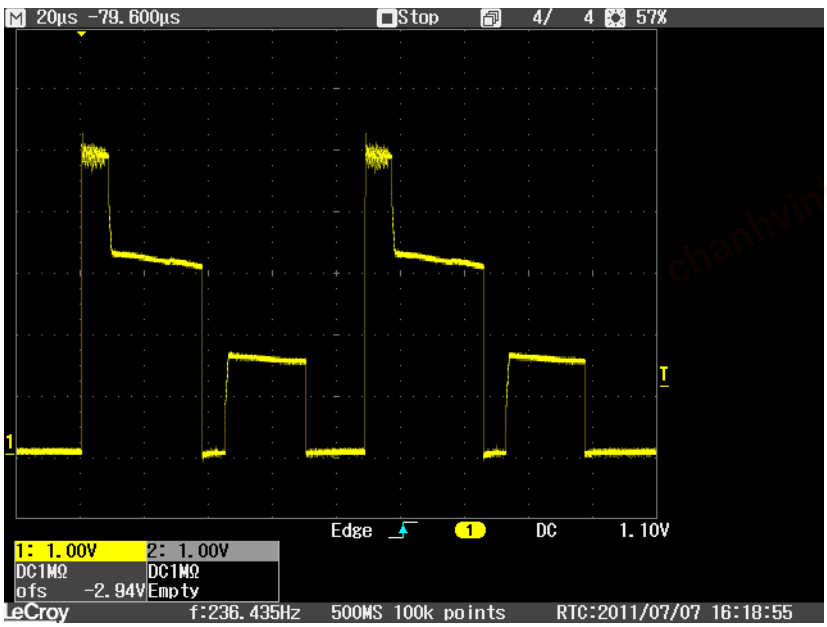
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Table 5-19. Oversample for “n” Bits

Sample	Scaling	Bits Gained (n)
4^n	2^n	n
…	…	…
1	1	0 (Pulse = 0x0 / Scale = 0x00)
4	2	1 (Pulse = 0x2 / Scale = 0x01)
16	4	2 (Pulse = 0x4 / Scale = 0x02)
64	8	3 (Pulse = 0x6 / Scale = 0x03)
256	16	4 (Pulse = 0x8 / Scale = 0x04)
1024	32	5 (Pulse = 0x0A / Scale = 0x05)
4096	64	6 (Pulse = 0x0C / Scale = 0x06)
16384	128	7 (Pulse = 0x0E / Scale = 0x07)

Consideration should be taken on the overall effect on timing when setting Pulse values. A single pulse takes approximately 90 µs to complete. As all keys are acquired sequentially a high-bit gain setting will add considerably to the time taken to acquire all channels.

Figure 5-3. Pulse and Scale Settings



Standalone Mode Defaults:

Key 0 Pulse Scale = 0x84

Key 1 Pulse Scale = 0x42

Key 2 – 6 Pulse Scale = 0x00

Comms Mode Defaults: PULSE0 – PULSE3 = 0

SCALE0 – SCALE3 = 0

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5.19 Address 52 – 75: Key Signal

Table 5-20. Key Signal

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
52	MSByte OF KEY SIGNAL FOR KEY 0							
53	LSByte OF KEY SIGNAL FOR KEY 0							
:	:							
74	MSByte OF KEY SIGNAL FOR KEY 11							
75	LSByte OF KEY SIGNAL FOR KEY 11							

KEY SIGNAL: addresses 52 – 75 allow key signals to be read for each key, starting with key 0. There are two bytes of data for each key. These are the key's 16-bit key signals which are accessed as two 8-bit bytes, stored MSByte first. These addresses are read-only.

5.20 Address 76 – 99: Reference Data

Table 5-21. Reference Data

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
76	MSByte OF REFERENCE DATA FOR KEY 0							
77	LSByte OF REFERENCE DATA FOR KEY 0							
:	:							
98	MSByte OF REFERENCE DATA FOR KEY 11							
99	LSByte OF REFERENCE DATA FOR KEY 11							

REFERENCE DATA: addresses 76 – 99 allow reference data to be read for each key, starting with key 0. There are two bytes of data for each key. These are the key's 16-bit reference data which is accessed as two 8-bit bytes, stored MSByte first. These addresses are read-only.

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6. Specifications

6.1 Absolute Maximum Specifications

Vdd	–0.5 to +6 V
Max continuous pin current, any control or drive pin	±10 mA
Short circuit duration to ground, any pin	infinite
Short circuit duration to Vdd, any pin	infinite
Voltage forced onto any pin	–0.5 V to (Vdd + 0.5) V
CAUTION: Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.	

6.2 Recommended Operating Conditions

Operating temperature	–40°C to +85°C
Storage temperature	–55°C to +125°C
Vdd	+1.8 V to 5.5 V
Supply ripple+noise	±25 mV
Cx load capacitance per key	1 to 30 pF

6.3 DC Specifications

Vdd = 3.3 V, Cs = 10 nF, load = 5 pF, 32 ms default sleep, Ta = recommended range, unless otherwise noted

Parameter	Description	Minimum	Typical	Maximum	Units	Notes
Vil	Low input logic level	–	–	0.2 × Vdd	V	
Vih	High input logic level	0.7 × Vdd	–	Vdd + 0.5	V	
Vol	Low output voltage	–	–	0.6	V	
Voh	High output voltage	Vdd – 0.7 V	–	–	V	
Iil	Input leakage current	–	–	±1	µA	

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6.4 Timing Specifications

Parameter	Description	Minimum	Typical	Maximum	Units	Notes
T_R	Response time	DI setting × 16 ms	–	LP mode + (DI setting × 16 ms)	ms	Under host control
F_{QT}	Sample frequency	10.5	12.5	–	kHz	Modulated spread-spectrum (chirp)
T_D	Power-up delay to operate/calibration time	–	<230	–	ms	Can be longer if burst is very long.
F_{I2C}	I^2C-compatible clock rate	–	–	400	kHz	–
Fm	Burst modulation, percentage		15	–	%	–
	$\overline{\text{RESET}}$ pulse width	2	–	–	µs	2 µs at 1.8 V

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6.5 Power Consumption

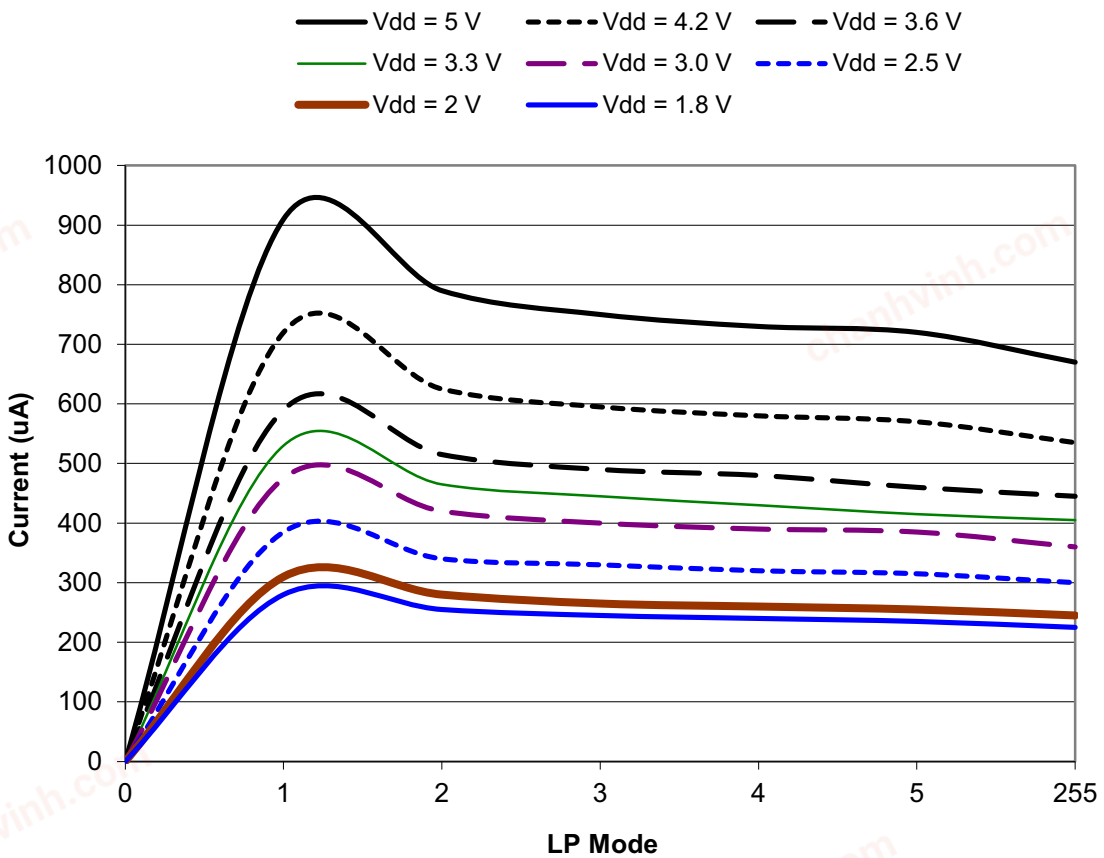
6.5.1 1 Channel Enabled

Table 6-1. Power Consumption (µA)

LP Mode	5 V	4.2 V	3.6 V	3.3 V	3 V	2.5 V	2 V	1.8 V
0	<1	<1	<1	<1	<1	<1	<1	<1
1	910	720	590	530	475	385	310	280
2	790	625	515	465	420	340	280	255
3	750	595	490	445	400	330	265	245
4	730	580	480	430	390	320	260	240
5	720	570	460	415	385	315	255	235
255	670	535	445	405	360	300	245	225

Pulse = 0 and Scale = 0

Figure 6-1. Idd Curve with 1 Channel Enabled



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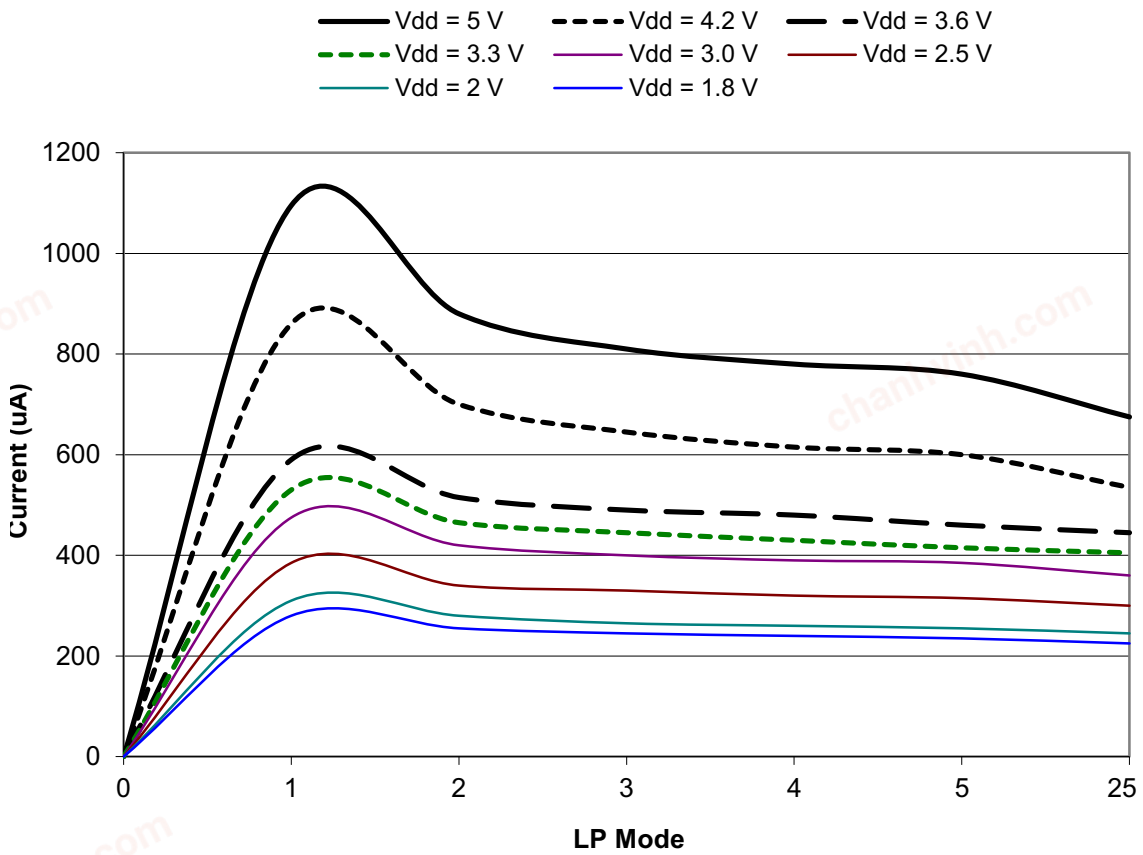
6.5.2 12 Channels Enabled

Table 6-2. Power Consumption (µA)

LP Mode	5 V	4.2 V	3.6 V	3.3 V	3 V	2.5 V	2 V	1.8 V
0	<1	<1	<1	<1	<1	<1	<1	<1
1	1095	860	700	630	560	460	370	330
2	880	700	575	515	460	380	305	280
3	810	645	530	480	425	350	285	260
4	780	615	510	455	410	340	275	250
5	760	600	490	440	400	330	270	240
255	675	535	445	410	360	295	245	225

Pulse = 0 and Scale = 0

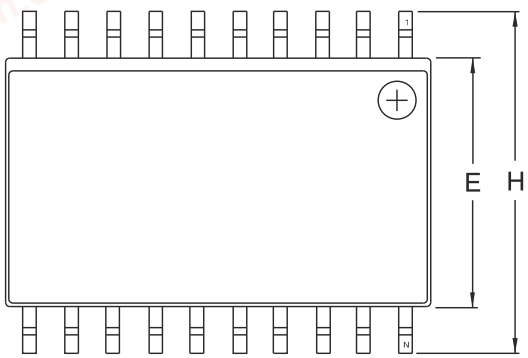
Figure 6-2. Idd Curve with 12 Channels Enabled



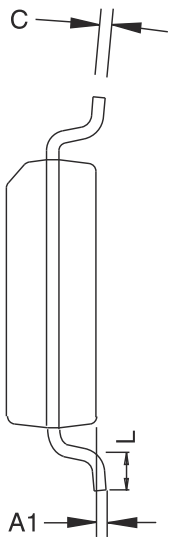
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6.6 Mechanical Dimensions

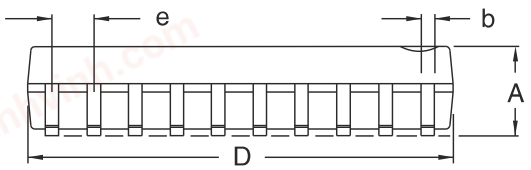
6.6.1 AT42QT2120-SU – 20-pin SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
4. 'L' is the length of the terminal for soldering to a substrate.
5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

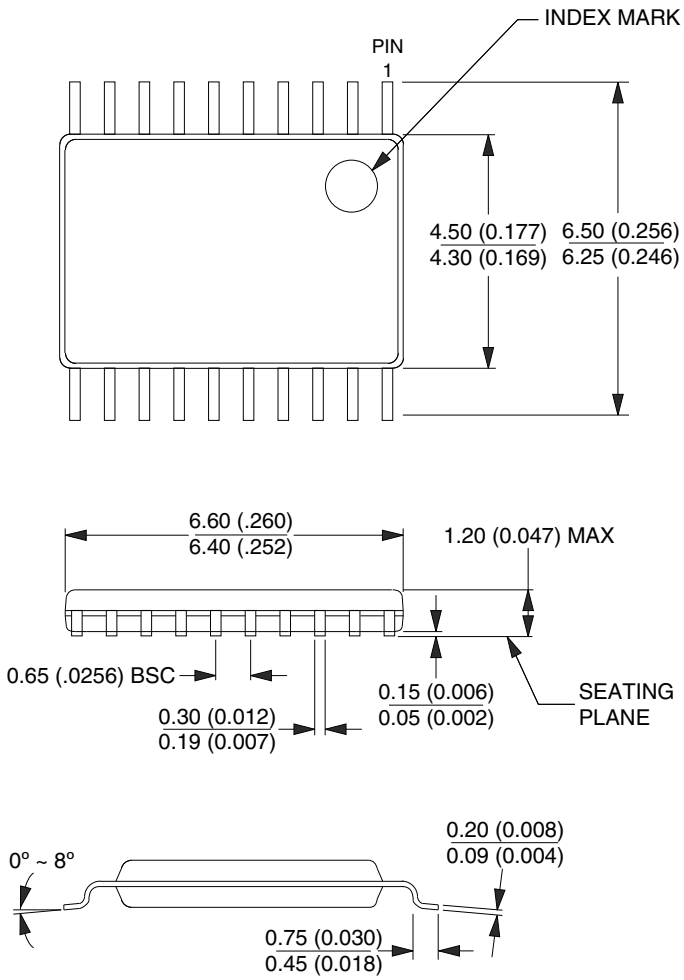
11/6/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S2**, 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	20S2	B

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6.6.2 AT42QT2120-XU – 20-pin TSSOP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MO-153 AC

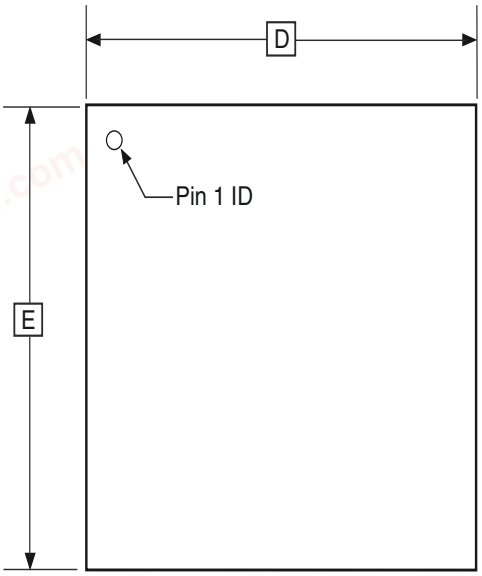


10/23/03

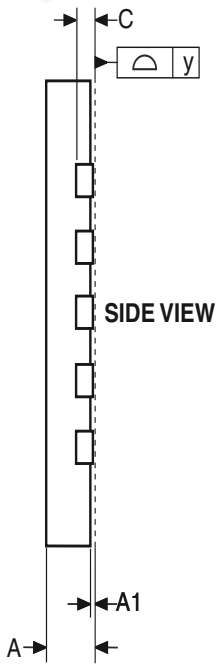
	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	20X	C

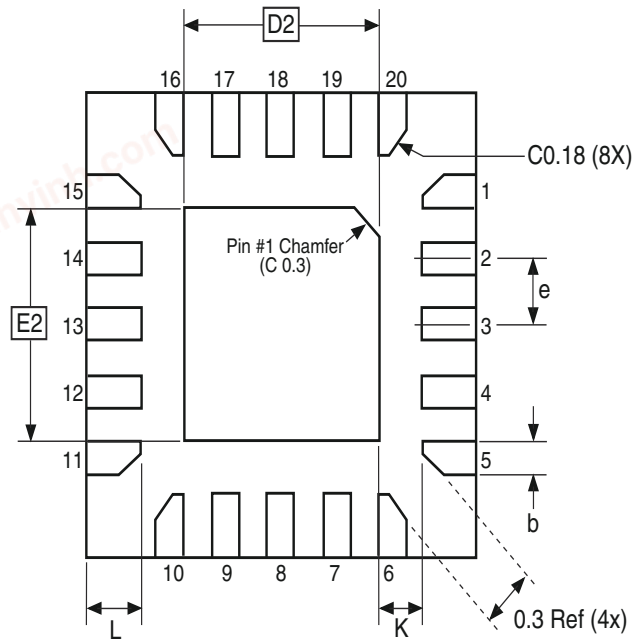
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6.6.3 AT42QT2120-MMH – 20-pin VQFN



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.75	0.80	0.85	
A1	0.00	0.02	0.05	
b	0.17	0.22	0.27	
C		0.152		
D	2.90	3.00	3.10	
D2	1.40	1.55	1.70	
E	2.90	3.00	3.10	
E2	1.40	1.55	1.70	
e	–	0.45	–	
L	0.35	0.40	0.45	
K	0.20	–	–	
y	0.00	–	0.08	

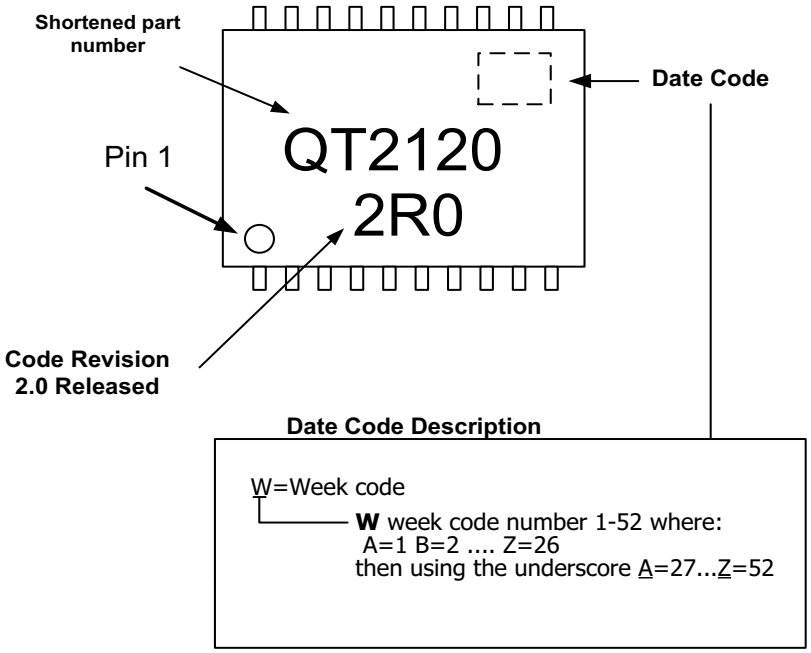
10/24/08

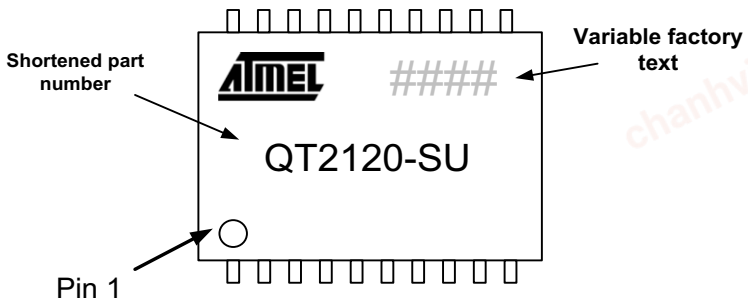
	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**20M2,** 20-pad, 3 x 3 x 0.85 mm Body, Lead Pitch 0.45 mm, 1.55 x 1.55 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)	ZFC	20M2	B

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6.7 Marking

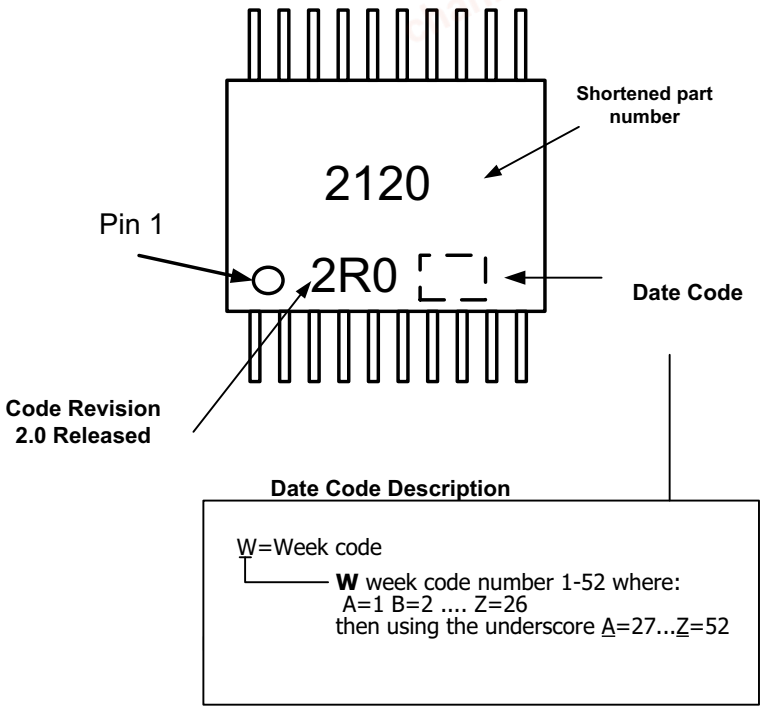
6.7.1 AT42QT2120X-SU

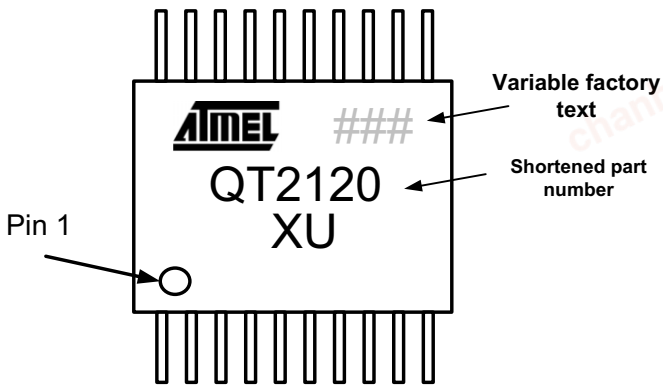




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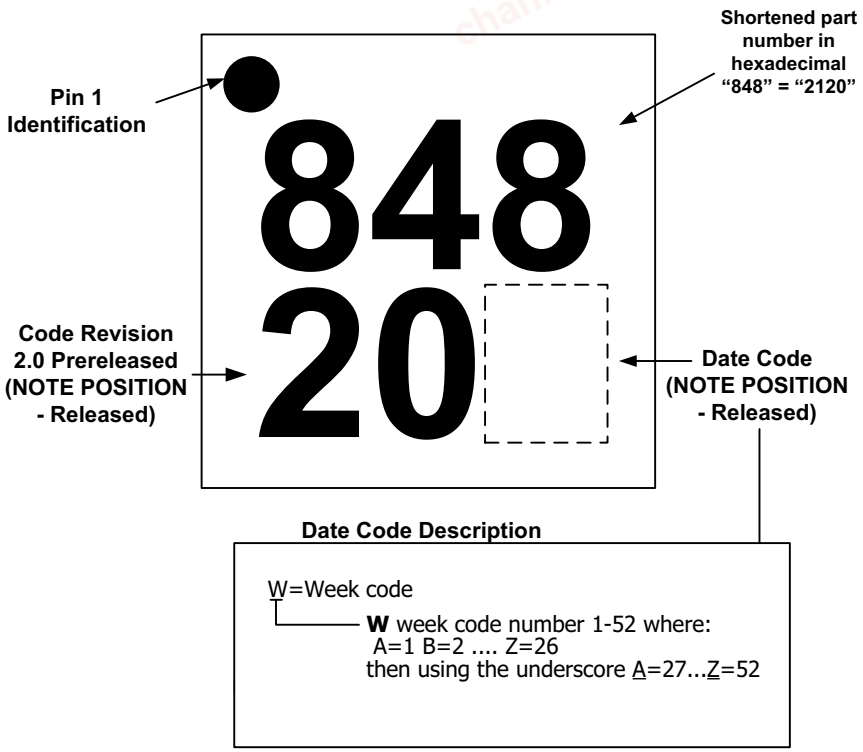
6.7.2 AT42QT2120X-XU

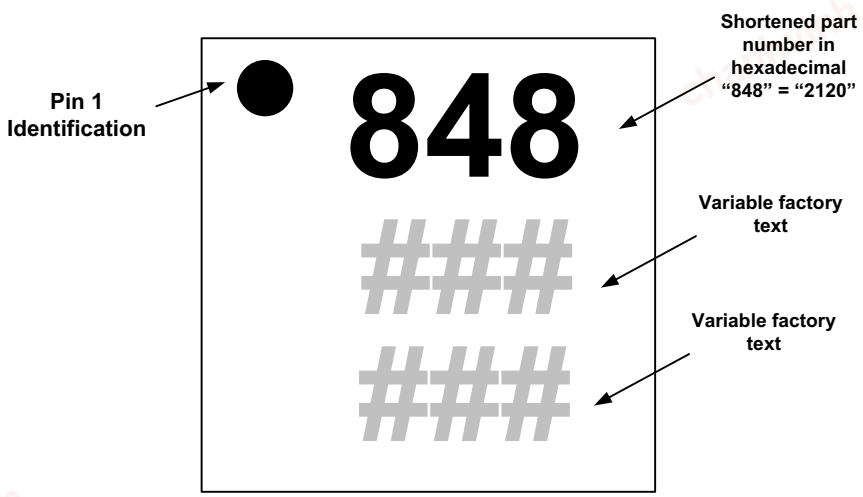




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6.7.3 AT42QT2120X-MMH





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6.8 Part Number

Part Number	Order Code	Description
AT42QT2120-SU AT42QT2120-SUR	QS589	20-pin 0.300 inch wide body, SOIC RoHS-compliant IC
AT42QT2120-XU AT42QT2120-XUR	QS589	20-pin 4.4 mm body, TSSOP RoHS-compliant IC
AT42QT2120-MMH AT42QT2120-MMHR	QS589	20-pad 3 × 3 × 0.85 mm body VQFN RoHS-compliant IC

The part number comprises:

AT = Atmel

42 = Touch Business Unit

QT = Charge-transfer technology

2120 = (2) capable of slider/wheel, (12) number of channels, (0) variant number

SU = SOIC chip

XU = TSSOP chip

MMH = VQFN chip

R = Tape and reel

6.9 Moisture Sensitivity Level (MSL)

MSL Rating	Peak Body Temperature	Specifications
MSL3	260°C	IPC/JEDEC J-STD-020

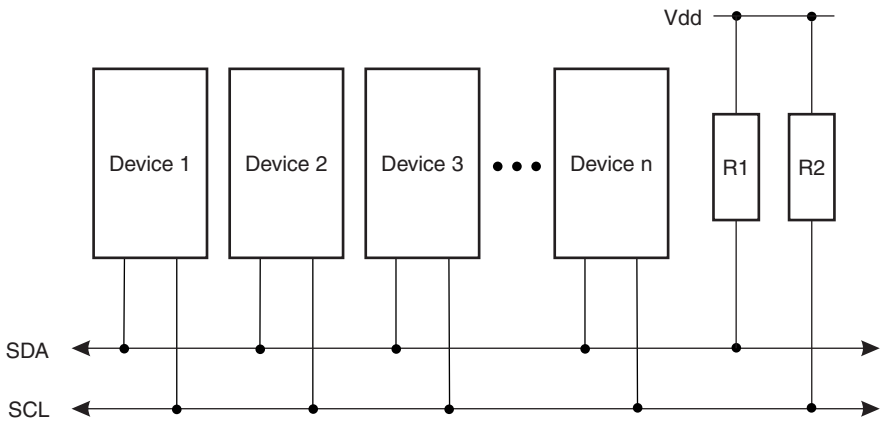
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Appendix A. I²C-compatible Operation

A.1 Interface Bus

The device communicates with the host over an I²C bus. The following sections give an overview of the bus; more detailed information is available from www.i2C-bus.org. Devices are connected to the I²C bus as shown in Figure A-1. Both bus lines are connected to Vdd via pull-up resistors. The bus drivers of all I²C devices must be open-drain type. This implements a wired AND function that allows any and all devices to drive the bus, one at a time. A low level on the bus is generated when a device outputs a zero.

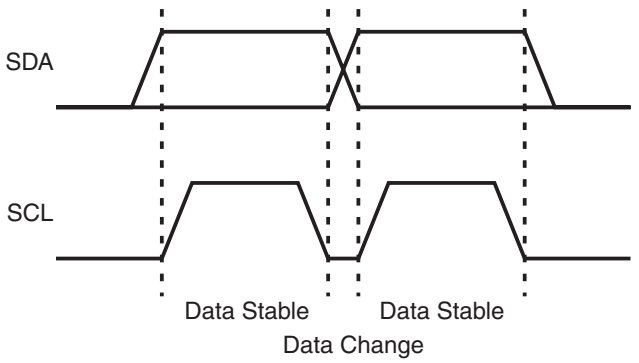
Figure A-1. I²C Interface Bus



A.2 Transferring Data Bits

Each data bit transferred on the bus is accompanied by a pulse on the clock line. The level of the data line must be stable when the clock line is high; the only exception to this rule is for generating START and STOP conditions.

Figure A-2. Data Transfer

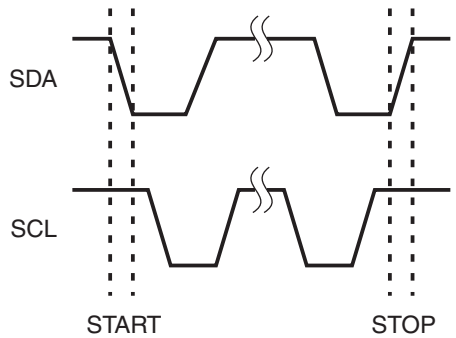


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A.3 START and STOP Conditions

The host initiates and terminates a data transmission. The transmission is initiated when the host issues a START condition on the bus, and is terminated when the host issues a STOP condition. Between the START and STOP conditions, the bus is considered busy. As shown in Figure A-3, START and STOP conditions are signaled by changing the level of the SDA line when the SCL line is high.

Figure A-3. START and STOP Conditions

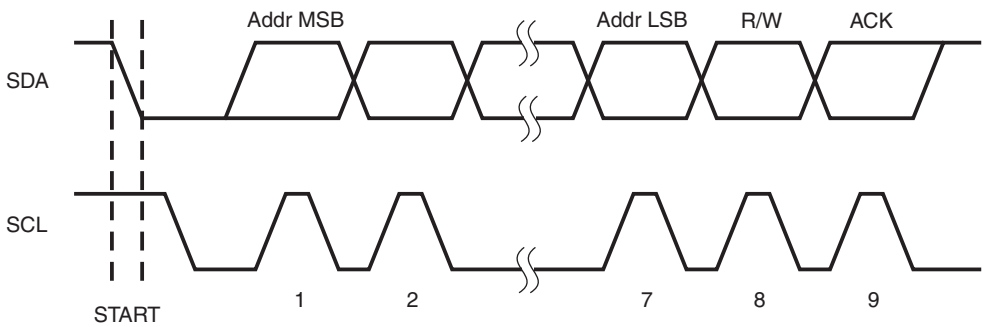


A.4 Address Byte Format

All address bytes are 9 bits long, consisting of 7 address bits, one READ/WRITE control bit and an acknowledge bit. If the READ/WRITE bit is set, a read operation is performed, otherwise a write operation is performed. When the device recognizes that it is being addressed, it will acknowledge by pulling SDA low in the ninth SCL (ACK) cycle. An address byte consisting of a slave address and a READ or a WRITE bit is called SLA+R or SLA+W, respectively.

The most significant bit of the address byte is transmitted first. The address sent by the host must be consistent with that selected with the option jumpers.

Figure A-4. Address Byte Format

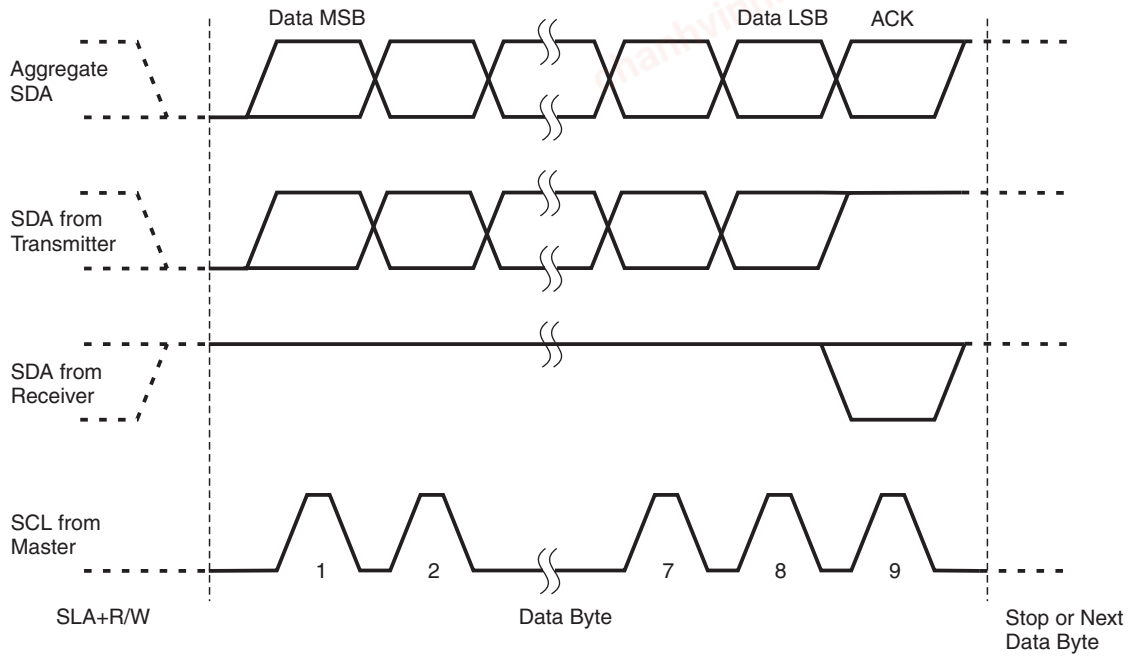


A.5 Data Byte Format

All data bytes are 9 bits long, consisting of 8 data bits and an acknowledge bit. During a data transfer, the host generates the clock and the START and STOP conditions, while the receiver is responsible for acknowledging the reception. An acknowledge (ACK) is signaled by the receiver pulling the SDA line low during the ninth SCL cycle. If the receiver leaves the SDA line high, a NACK is signaled.

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Figure A-5. Data Byte Format



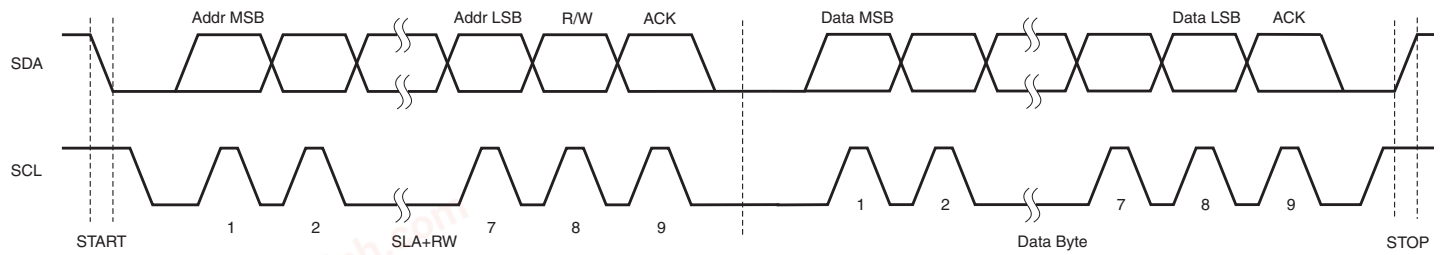
A.6 Combining Address and Data Bytes into a Transmission

A transmission consists of a START condition, an SLA+R/W, one or more data bytes and a STOP condition. The wired “ANDing” of the SCL line is used to implement handshaking between the host and the device. The device extends the SCL low period by pulling the SCL line low whenever it needs extra time for processing between the data transmissions.

Note: Each write or read cycle must end with a stop condition. The device may not respond correctly if a cycle is terminated by a new start condition.

Figure A-6 shows a typical data transmission. Note that several data bytes can be transmitted between the SLA+R/W and the STOP.

Figure A-6. Byte Transmission



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Associated Documents

- *QTAN0079 – Buttons, Sliders and Wheels Touch Sensors Design Guide*
- *QTAN0087 – Proximity Design Guide*
- *Atmel AVR3000: QTouch Conducted Immunity Application Note*

Revision History

Revision Number	History
Revision A – November 2011	• Initial release of document for code revision 1.5
Revision B – December 2011	• Release of document for code revision 1.7 (rev 1.6 unreleased)
Revision C – February 2012	• Small amendment to diagram (code revision 1.7 unreleased)
Revision D – February 2012	• Release of document for code revision 1.8 • Updated Part Markings • Added Power Consumption figures • Updated description for $\overline{\text{CHANGE}}$ Line timings
Revision E – June 2012	• Release of document for code revision 2.0 • Updated Part Markings • Other minor changes

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Notes

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