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8/16-Kbit SPI Serial EEPROM, Industrial Grade

AT25080B/AT25160B

Product Page Links

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- Low-Voltage Operation:
  - V_{CC} = 1.8V to 5.5V
- Industrial Temperature Range: -40°C to +85°C
- High Speed Clock Frequency up to 20 MHz (V_{CC} = 4.5V to 5.5V)
- Supports Page Write up to 32 Bytes
- Self-Timed Write Cycle within 5 ms Maximum
- Block Write Protection:
  - Protect 1/4, 1/2 or entire array
- Write-Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- High Reliability:
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- RoHS Compliant
- Die Sale Options: Wafer Form and Bumped Wafers

Packages

- 8-Lead SOIC, 8-Lead TSSOP and 8-Pad UDFN

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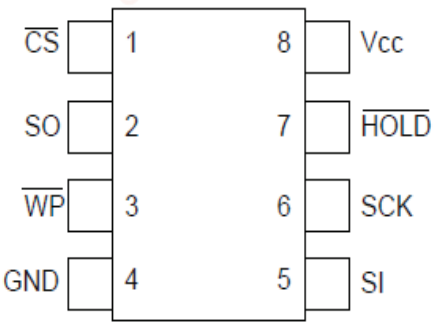
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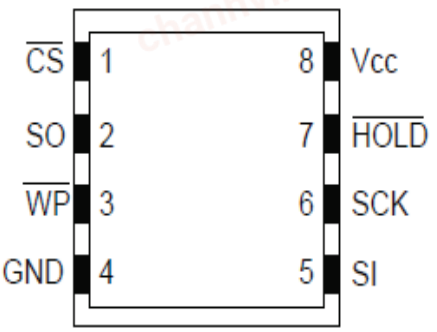
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1. Package Types (not to scale)

8-Lead SOIC/TSSOP
(Top View)



8-Pad UDFN
(Top View)



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2. Pin Description

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	8-Lead SOIC	8-Lead TSSOP	8-Pad UDFN[1]	Function
$\overline{CS}$	1	1	1	Chip Select
SO	2	2	2	Serial Data Output
$\overline{WP}$[2]	3	3	3	Write-Protect
GND	4	4	4	Ground
SI	5	5	5	Serial Data Input
SCK	6	6	6	Serial Data Clock
$\overline{HOLD}$[2]	7	7	7	Suspend Serial Input
V_{CC}	8	8	8	Device Power Supply

Notes:

1. The exposed pad on this package can be connected to GND or left floating.
2. The Write-Protect ($\overline{WP}$) and Hold ($\overline{HOLD}$) pins should be driven high or low, as appropriate.

2.1. Chip Select ($\overline{CS}$)

The AT25080B/AT25160B is selected when the Chip Select ($\overline{CS}$) pin is low. When the device is not selected, data will not be accepted via the Serial Data Input (SI) pin, and the Serial Output (SO) pin will remain in a high-impedance state.

To ensure robust operation, the $\overline{CS}$ pin should follow V_{CC} upon power-up. It is, therefore, recommended to connect $\overline{CS}$ to V_{CC} using a pull-up resistor (less than or equal to 10 kΩ). After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2. Serial Data Output (SO)

The Serial Data Output (SO) pin is used to transfer data out of the AT25080B/AT25160B. During a read sequence, data are shifted out on this pin after the falling edge of the Serial Data Clock (SCK).

2.3. Write-Protect ($\overline{WP}$)

The Write-Protect ($\overline{WP}$) pin will allow normal read/write operations when held high. When the $\overline{WP}$ pin is brought low and the WPEN bit is set to logic '1', all write operations to the STATUS register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write operation to the STATUS register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the STATUS register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the STATUS register is set to logic '0'. This will allow the user to install the AT25080B/AT25160B in a system with the $\overline{WP}$ pin tied to ground and still be able to write to the STATUS register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to logic '1'.

2.4. Ground (GND)

The ground reference for the Device Power Supply (V_{CC}). The Ground (GND) pin should be connected to the system ground.

2.5. Serial Data Input (SI)

The Serial Data Input (SI) pin is used to transfer data into the device. It receives instructions, addresses and data. Data are latched on the rising edge of the Serial Data Clock (SCK).

2.6. Serial Data Clock (SCK)

The Serial Data Clock (SCK) pin is used to synchronize the communication between a host and the AT25080B/AT25160B. Instructions, addresses or data present on the Serial Data Input (SI) pin are latched in on the rising edge of SCK, while output on the Serial Data Output (SO) pin is clocked out on the falling edge of SCK.

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2.7. Suspend Serial Input ($\overline{HOLD}$)

The Suspend Serial Input ($\overline{HOLD}$) pin is used in conjunction with the Chip Select ($\overline{CS}$) pin to pause the AT25080B/AT25160B. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause serial communication with the host device without resetting the serial sequence. To pause communication, the $\overline{HOLD}$ pin must be brought low while the Serial Data Clock (SCK) pin is low. To resume serial communication, the $\overline{HOLD}$ pin must be brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the Serial Data Input (SI) pin will be ignored while the Serial Data Output (SO) pin remains in the high-impedance state.

2.8. Device Power Supply (V_{CC})

The Device Power Supply (V_{CC}) pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

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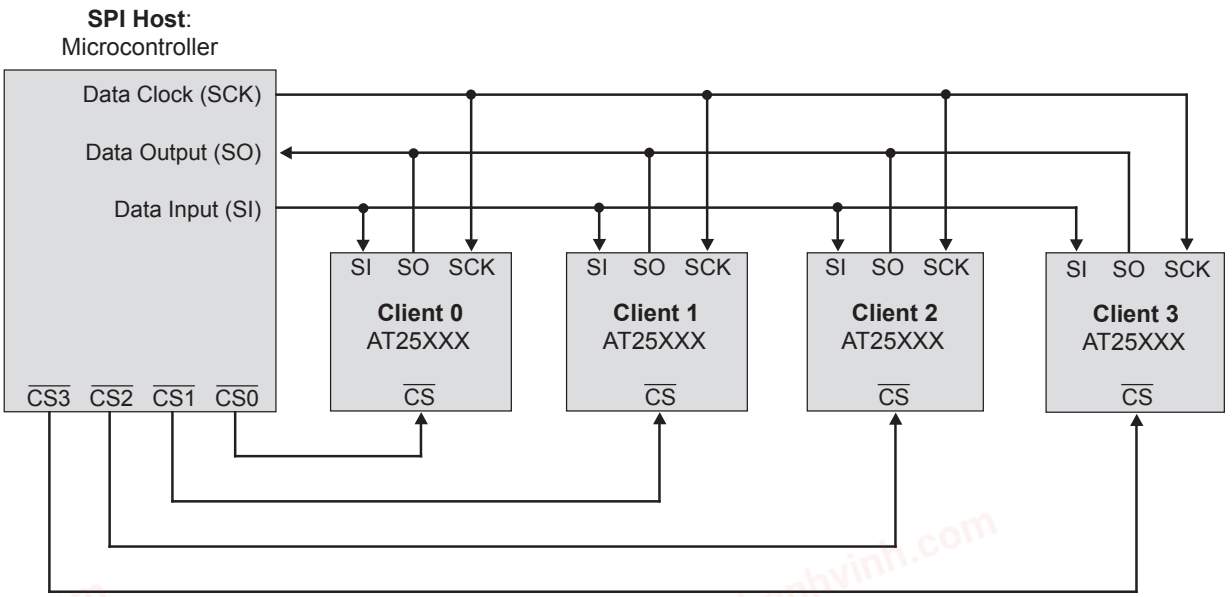
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3. Description

The AT25080B/AT25160B provides 8,192/16,384 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 1,024/2,048 words of 8 bits each. The device is optimized for use in a wide range of industrial and commercial applications where low-power and low-voltage operations are essential. The device is available in space-saving 8-lead SOIC, 8-lead TSSOP and 8-pad UDFN packages. All packages operate from 1.8V to 5.5V.

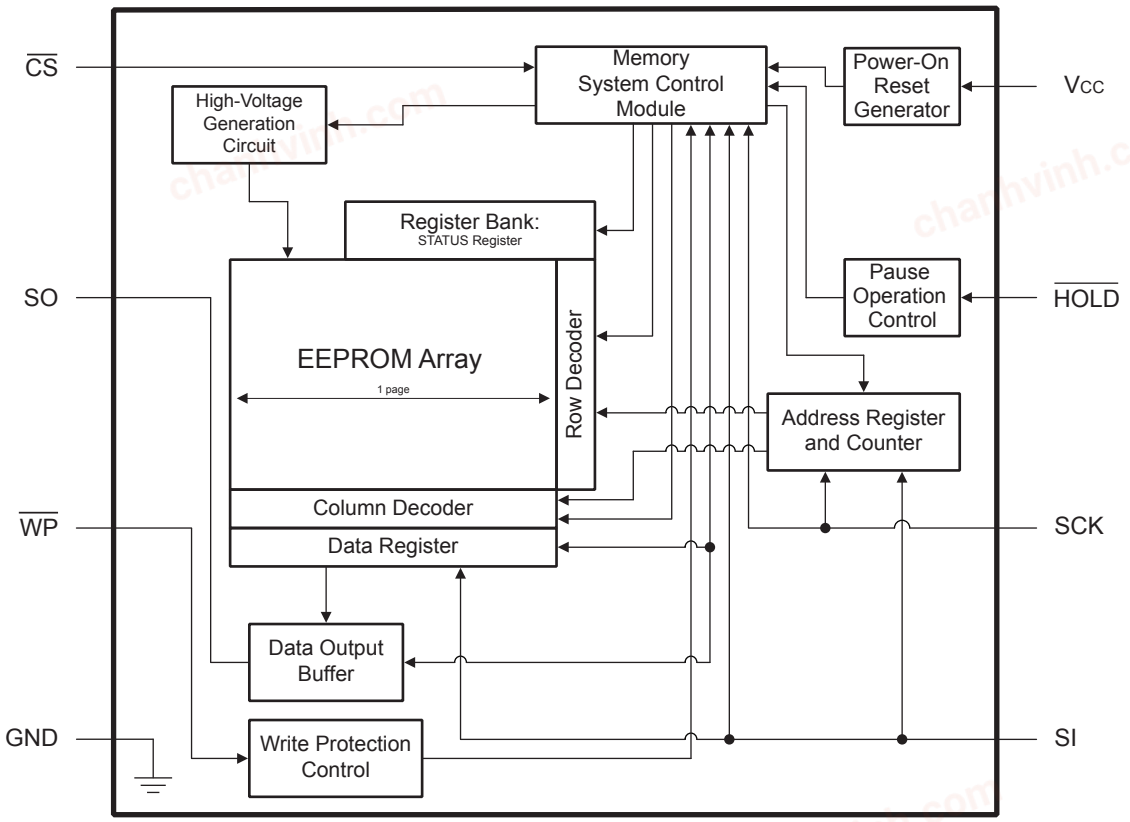
3.1. SPI Bus Host Connections to Serial EEPROMs



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3.2. Block Diagram



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4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
V_{CC}	6.25V
Voltage on any pin with respect to ground	-1.0V to +7.0V
DC output current	5.0 mA
ESD protection	> 2 kV

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2. DC and AC Operating Range

Table 4-1. DC and AC Operating Range

AT25080B/AT25160B		
Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low-Voltage Grade	1.8V to 5.5V

4.3. DC Characteristics

Table 4-2. DC Characteristics[1]

Parameter	Symbol	Minimum	Maximum	Units	Conditions	
Supply Voltage	V_{CC1}	1.8	5.5	V		
Supply Voltage	V_{CC2}	2.5	5.5	V		
Supply Voltage	V_{CC3}	4.5	5.5	V		
Supply Current	I_{CC1}	—	10.0	mA	V_{CC} = 5.0V at 20 MHz, SO = Open, Read	
Supply Current	I_{CC2}	—	10.0	mA	V_{CC} = 5.0V at 20 MHz, SO = Open, Read, Write	
Supply Current	I_{CC3}	—	6.0	mA	V_{CC} = 5.0V at 5 MHz, SO = Open, Read, Write	
Standby Current	I_{SB1}	—	6.0[3]	µA	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}	
Standby Current	I_{SB2}	—	7.0[3]	µA	V_{CC} = 2.5V, $\overline{CS}$ = V_{CC}	
Standby Current	I_{SB3}	—	10.0[3]	µA	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}	
Input Leakage	I_{IL}	-3.0	3.0	µA	V_{IN} = 0V to V_{CC}	
Output Leakage	I_{OL}	-3.0	3.0	µA	V_{IN} = 0V to V_{CC}, T_A = 0°C to +70°C	
Input Low- Voltage	V_{IL}[2]	-0.6	V_{CC} x 0.3	V		
Input High-Voltage	V_{IH}[2]	V_{CC} x 0.7	V_{CC} + 0.5	V		
Output Low-Voltage	V_{OL1}	—	0.4	V	3.6V ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0 mA
Output High-Voltage	V_{OH1}	V_{CC} - 0.8	—	V	3.6V ≤ V_{CC} ≤ 5.5V	I_{OH} = -1.6 mA
Output Low-Voltage	V_{OL2}	—	0.2	V	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA
Output High-Voltage	V_{OH2}	V_{CC} - 0.2	—	V	1.8V ≤ V_{CC} ≤ 3.6V	I_{OH} = -100 µA

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Notes:

1. Applicable over recommended operating ranges: T_A = -40°C to +85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).
2. V_{IL} min and V_{IH} max are for reference only and are not tested.
3. Worst-case values are measured at +85°C.

4.4. AC Characteristics

Table 4-3. AC Characteristics[1]

Parameter	Symbol	Minimum	Maximum	Units	Conditions
SCK Clock Frequency	f_{SCK}	0	20	MHz	V_{CC} = 4.5V to 5.5V
		0	10	MHz	V_{CC} = 2.5V to 5.5V
		0	5	MHz	V_{CC} = 1.8V to 5.5V
Input Rise Time	t_{RI}	—	2000	ns	V_{CC} = 4.5V to 5.5V
		—	2000	ns	V_{CC} = 2.5V to 5.5V
		—	2000	ns	V_{CC} = 1.8V to 5.5V
Input Fall Time	t_{FI}	—	2000	ns	V_{CC} = 4.5V to 5.5V
		—	2000	ns	V_{CC} = 2.5V to 5.5V
		—	2000	ns	V_{CC} = 1.8V to 5.5V
SCK High Time	t_{WH}	20	—	ns	V_{CC} = 4.5V to 5.5V
		40	—	ns	V_{CC} = 2.5V to 5.5V
		80	—	ns	V_{CC} = 1.8V to 5.5V
SCK Low Time	t_{WL}	20	—	ns	V_{CC} = 4.5V to 5.5V
		40	—	ns	V_{CC} = 2.5V to 5.5V
		80	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{CS}$ High Time	t_{CS}	25	—	ns	V_{CC} = 4.5V to 5.5V
		50	—	ns	V_{CC} = 2.5V to 5.5V
		100	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{CS}$ Setup Time	t_{CSS}	25	—	ns	V_{CC} = 4.5V to 5.5V
		50	—	ns	V_{CC} = 2.5V to 5.5V
		100	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{CS}$ Hold Time	t_{CSH}	25	—	ns	V_{CC} = 4.5V to 5.5V
		50	—	ns	V_{CC} = 2.5V to 5.5V
		100	—	ns	V_{CC} = 1.8V to 5.5V
Data In Setup Time	t_{SU}	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.8V to 5.5V
Data In Hold Time	t_H	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{HOLD}$ Setup Time	t_{HD}	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{HOLD}$ Hold Time	t_{CD}	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.8V to 5.5V

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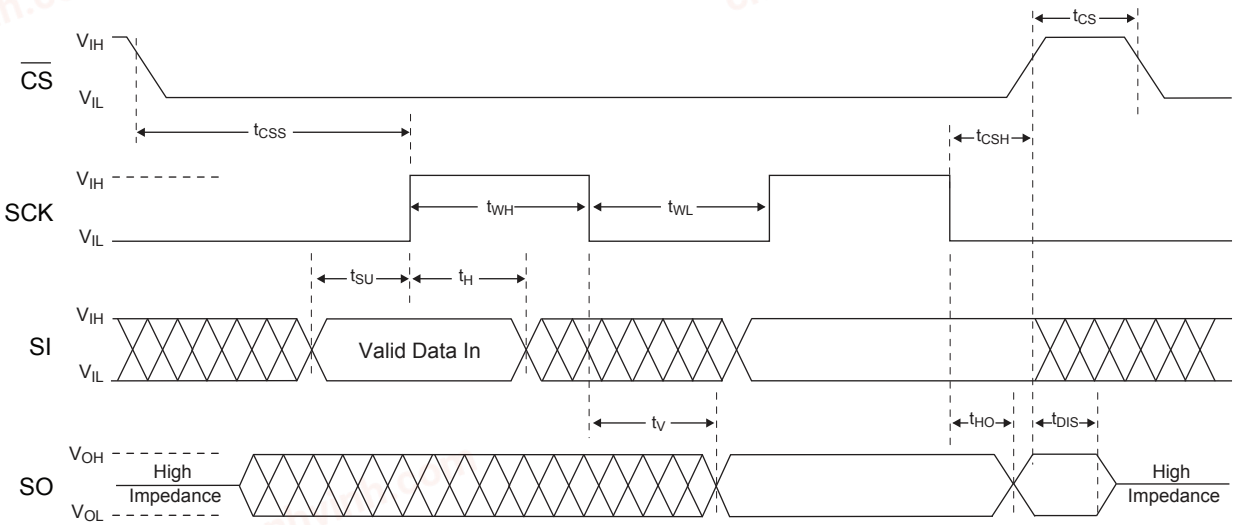
Table 4-3. AC Characteristics[1] (continued)

Parameter	Symbol	Minimum	Maximum	Units	Conditions
Output Valid	t_V	0	20	ns	V_{CC} = 4.5V to 5.5V
		0	40	ns	V_{CC} = 2.5V to 5.5V
		0	80	ns	V_{CC} = 1.8V to 5.5V
Output Hold Time	t_{HO}	0	—	ns	V_{CC} = 4.5V to 5.5V
		0	—	ns	V_{CC} = 2.5V to 5.5V
		0	—	ns	V_{CC} = 1.8V to 5.5V
$\overline{HOLD}$ to Output Low-Z	t_{LZ}	0	25	ns	V_{CC} = 4.5V to 5.5V
		0	50	ns	V_{CC} = 2.5V to 5.5V
		0	100	ns	V_{CC} = 1.8V to 5.5V
$\overline{HOLD}$ to Output High-Z	t_{HZ}	—	40	ns	V_{CC} = 4.5V to 5.5V
		—	80	ns	V_{CC} = 2.5V to 5.5V
		—	200	ns	V_{CC} = 1.8V to 5.5V
Output Disable Time	t_{DIS}	—	40	ns	V_{CC} = 4.5V to 5.5V
		—	80	ns	V_{CC} = 2.5V to 5.5V
		—	200	ns	V_{CC} = 1.8V to 5.5V
Write Cycle Time	t_{WC}	—	5	ms	V_{CC} = 4.5V to 5.5V
		—	5	ms	V_{CC} = 2.5V to 5.5V
		—	5	ms	V_{CC} = 1.8V to 5.5V

Note:

1. Applicable over recommended operating ranges: T_A = -40°C to +85°C, V_{CC} = As Specified, C_L = 1 TTL Gate and 30 pF (unless otherwise noted).

4.5. SPI Synchronous Data Timing



4.6. Electrical Specifications

4.6.1. Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the AT25080B/AT25160B should monotonically rise from GND to the minimum V_{CC} level (as specified in Table 4-1), with a slew rate no faster than 0.1 V/µs.

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4.6.1.1. Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT25080B/AT25160B includes a Power-On Reset (POR) circuit. Upon power-up, the device will not respond to any instructions until the V_{CC} level crosses the internal voltage threshold (V_{POR}), which brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level. Additionally, once V_{CC} is greater than or equal to the minimum V_{CC} level, the bus host must wait at least t_{PUP} before sending the first instruction to the device. See Table 4-4 for the values associated with these power-up parameters.

Table 4-4. Power-Up Conditions[1]

Symbol	Parameter	Min.	Max.	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept instructions	100	—	µs
V_{POR}	Power-On Reset Threshold Voltage	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles	0.03	—	ms

Note:

1. These parameters are characterized but are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT25080B/AT25160B drops below the maximum V_{POR} level specified, it is recommended that a full power-cycle sequence be performed by first driving the V_{CC} pin to GND in less than 1 ms, waiting at least the minimum t_{POFF} time, and then performing a new power-up sequence in compliance with the requirements defined in this section.

4.6.2. Pin Capacitance

Table 4-5. Pin Capacitance[1,2]

Symbol	Test Condition	Max.	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Notes:

1. This parameter is characterized but is not 100% tested in production.
2. Applicable over recommended operating ranges: T_A = +25°C, f_{SCK} = 1.0 MHz, V_{CC} = 5.0V (unless otherwise noted).

4.6.3. EEPROM Cell Performance Characteristics

Table 4-6. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance[1]	T_A = +25°C, V_{CC} = 3.3V, Page Write mode	1,000,000	—	Write Cycles
Data Retention[1]	T_A = +55°C	100	—	Years

Note:

1. Performance is determined through characterization and the qualification process.

4.6.4. Software Reset

The SPI interface of the AT25080B/AT25160B can be reset by toggling the $\overline{CS}$ input. If the $\overline{CS}$ line is already in the Active state, it must complete a transition from the Inactive state (≥ V_{IH}) to the Active

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state (≤ V_{IL}) and then back to the Inactive state (≥ V_{IH}) without sending clocks on the SCK line. Upon completion of this sequence, the device will be ready to receive a new opcode on the SI line.

4.6.5. Device Default State at Power-Up

The AT25080B/AT25160B default state upon power-up consists of:

- Standby Power mode
- A high-to-low-level transition on $\overline{CS}$ is required to enter Active state
- Write Enable Latch (WEL) bit in the STATUS register = 0
- $\overline{Ready}$/Busy bit in the STATUS register = 0, indicating the device is ready to accept a new command
- Device is not selected
- Not in Hold condition
- WPEN, BP1 and BP0 bits in the STATUS register are unchanged from their previous state, as they are nonvolatile values

4.6.6. Device Default Condition

The AT25080B/AT25160B is shipped from Microchip to the customer with the EEPROM array set to an all FFh data pattern (logic '1' state). The Write-Protect Enable bit in the STATUS register is set to logic '0', and the Block Write-Protect bits in the STATUS register are set to logic '0'.

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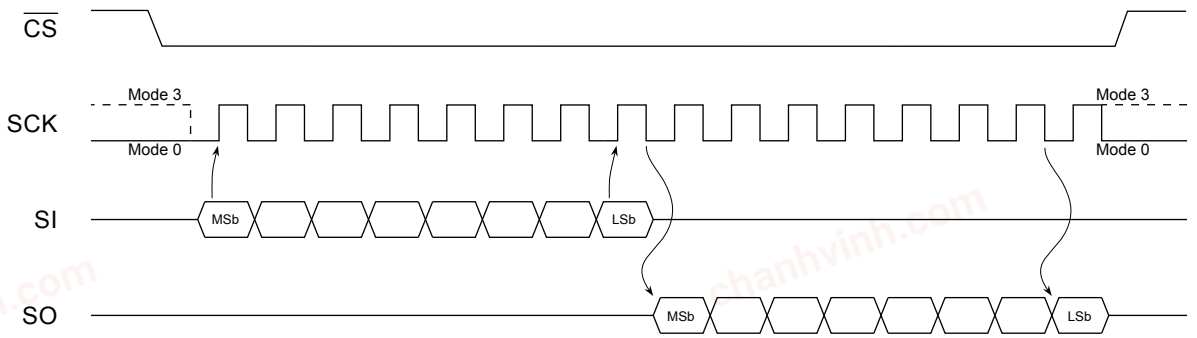
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5. Device Operation

The AT25080B/AT25160B is controlled by a set of instructions sent from a host controller, commonly referred to as the SPI host. The SPI host communicates with the AT25080B/AT25160B via the SPI bus, which comprises four signal lines: Chip Select ($\overline{CS}$), Serial Data Clock (SCK), Serial Data Input (SI) and Serial Data Output (SO).

The SPI protocol defines four modes of operation (Mode 0, 1, 2 and 3), with each mode differing in terms of SCK polarity and phase, which control the flow of data on the SPI bus. The AT25080B/AT25160B supports the two most common modes, SPI Modes 0 and 3. In SPI Modes 0 and 3, data are always latched in on the rising edge of SCK and output on the falling edge of SCK. The only difference between SPI Modes 0 and 3 is the polarity of the SCK signal when in the Inactive state (when the SPI host is in Standby mode and not transferring any data). SPI Mode 0 is defined as having SCK low while $\overline{CS}$ is not asserted (at V_{CC}), whereas SPI Mode 3 has SCK high in the Inactive state. The SCK Idle state must match when $\overline{CS}$ is deasserted, both before and after the communication sequence, in SPI Modes 0 and 3. The figures in this document depict Mode 0 with a solid line on SCK while $\overline{CS}$ is inactive and Mode 3 with a dotted line.

Figure 5-1. SPI Mode 0 and Mode 3



5.1. Interfacing the AT25080B/AT25160B on the SPI Bus

Communication to and from the AT25080B/AT25160B must be initiated by the SPI host device, such as a microcontroller. The SPI host device must generate the serial clock for the AT25080B/AT25160B on the Serial Data Clock (SCK) pin. The AT25080B/AT25160B always operates as a client because SCK is always an input.

5.1.1. Selecting the Device

The AT25080B/AT25160B is selected when the Chip Select ($\overline{CS}$) pin is low. When the device is not selected, data will not be accepted via the Serial Data Input (SI) pin, and the Serial Data Output (SO) pin will remain in a high-impedance state.

5.1.2. Sending Data to the Device

The AT25080B/AT25160B uses the SI pin to receive information. All instruction, address and data input bytes are clocked into the device with the Most Significant bit (MSb) first. The SI pin is sampled on the first rising edge of the SCK line after $\overline{CS}$ has been asserted.

5.1.3. Receiving Data from the Device

Data output from the device is transmitted on the SO pin, with the MSb output first. The SO data are latched on the first falling edge of SCK after the instruction has been clocked into the device, such as the Read from Memory Array (`READ`) and Read STATUS Register (`RDSR`) instructions. See Read Sequence for more details.

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5.2. Device Opcodes

5.2.1. Serial Opcode

After the device is selected by driving $\overline{CS}$ low, the first byte will be received on the SI pin. This byte contains the opcode that defines the operation to be performed. Refer to Table 6-1 for a list of all opcodes to which the AT25080B/AT25160B will respond.

5.2.2. Invalid Opcode

If an invalid opcode is received, no data will be shifted into AT25080B/AT25160B, and the SO pin will remain in a high-impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

5.3. Hold Function

The Suspend Serial Input ($\overline{HOLD}$) pin is used to pause the serial communication with the device without having to stop or reset the clock sequence. Hold mode, however, does not affect the internal write cycle. Therefore, if a write cycle is in progress, asserting the $\overline{HOLD}$ pin will not pause the operation, and the write cycle will continue to completion.

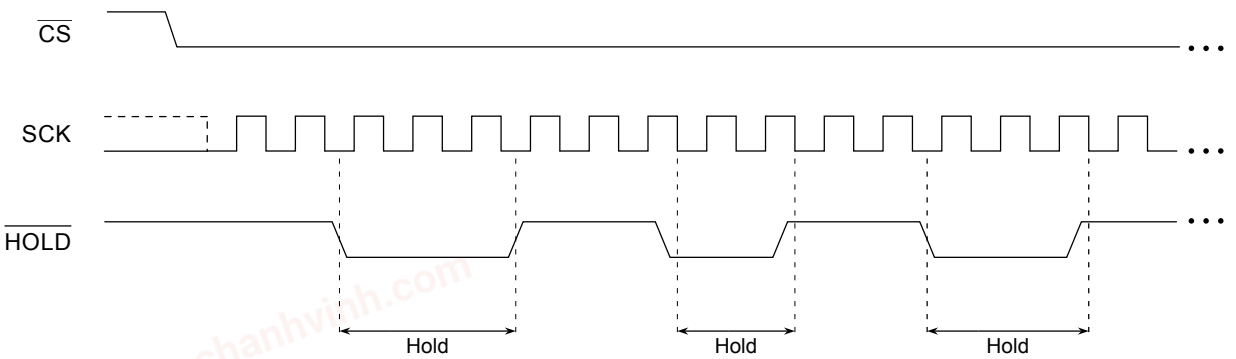
Hold mode can only be entered while the $\overline{CS}$ pin is asserted. Hold mode is activated by asserting the $\overline{HOLD}$ pin during the SCK low pulse. If the $\overline{HOLD}$ pin is asserted during the SCK high pulse, then Hold mode will not start until the beginning of the next SCK low pulse. The device will remain in Hold mode as long as the $\overline{HOLD}$ pin and $\overline{CS}$ pin are asserted.

While in Hold mode, the SO pin will be in a high-impedance state. In addition, both the SI pin and the SCK pin will be ignored. The Write-Protect ($\overline{WP}$) pin, however, can still be asserted or deasserted while in Hold mode.

To end Hold mode and resume serial communication, the $\overline{HOLD}$ pin must be deasserted during the SCK low pulse. If the $\overline{HOLD}$ pin is deasserted during the SCK high pulse, then Hold mode will not end until the beginning of the next SCK low pulse.

If the $\overline{CS}$ pin is deasserted while the $\overline{HOLD}$ pin is still asserted, then any operation that may have been started will be aborted, and the device will reset the WEL bit in the STATUS register back to the logic '0' state.

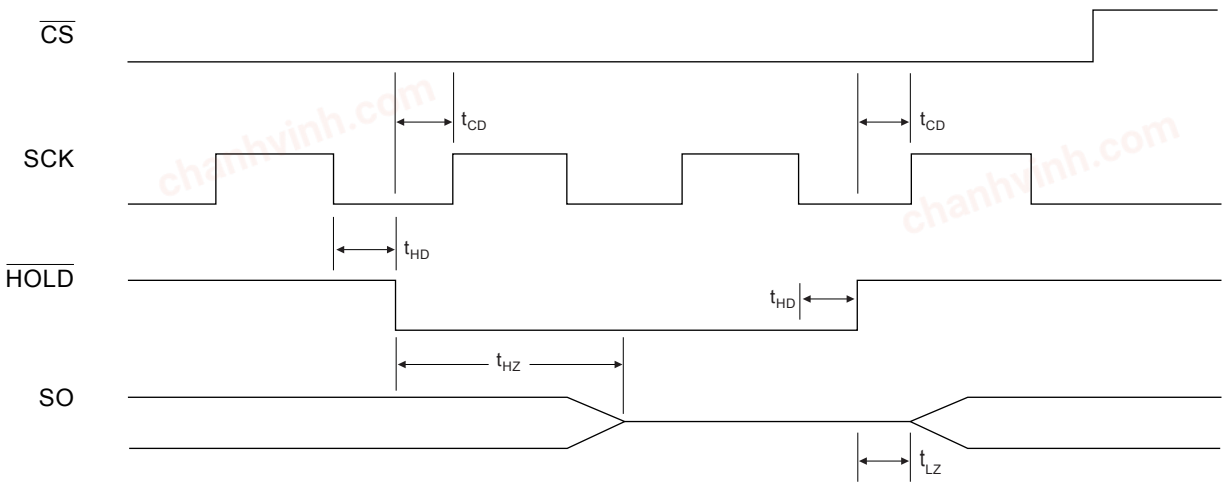
Figure 5-2. Hold Mode



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Figure 5-3. Hold Timing



5.4. Write Protection

The Write-Protect ($\overline{WP}$) pin allows normal read and write operations when held high. When the $\overline{WP}$ pin is brought low and WPEN bit is logic '1', all write operations to the STATUS register are inhibited. If the $\overline{WP}$ pin goes low while $\overline{CS}$ is still low, it will interrupt a Write STATUS Register (WRSR) operation. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the STATUS register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the STATUS register is logic '0'. This allows the user to install the AT25080B/AT25160B device in a system with the $\overline{WP}$ pin tied to ground and still be able to write to the STATUS register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to logic '1'.

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6. Device Commands and Addressing

The AT25080B/AT25160B is designed to interface directly with the synchronous Serial Peripheral Interface (SPI). The AT25080B/AT25160B utilizes an 8-bit instruction register. The instruction set and corresponding codes are contained in Table 6-1. All instructions, addresses and data are transferred with the MSb first and begin with a high-to-low transition on $\overline{CS}$.

Table 6-1. Instruction Set for the AT25080B/AT25160B

Instruction Name	Instruction Format	Operates On	Operation Description
WREN	0000 X110	STATUS Register	Set Write Enable Latch (WEL)
WRDI	0000 X100	STATUS Register	Reset Write Enable Latch (WEL)
RDSR	0000 X101	STATUS Register	Read STATUS Register
WRSR	0000 X001	STATUS Register	Write STATUS Register
READ	0000 X011	Memory Array	Read from Memory Array
WRITE	0000 X010	Memory Array	Write to Memory Array

6.1. STATUS Register Bit Definition and Function

The AT25080B/AT25160B includes an 8-bit STATUS register. The STATUS register bits modulate various device features, as shown in Table 6-2 and Table 6-3. These bits can be changed by specific instructions detailed in the following sections.

Table 6-2. STATUS Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEL	$\overline{RDY}$/BSY

Table 6-3. STATUS Register Bit Definition

Bit	Name		Type	Description	
7	WPEN	Write-Protect Enable	R/W	0	See Table 6-5 (Factory Default)
				1	See Table 6-5 (Factory Default)
6:4	RFU	Reserved for Future Use	R	0	Reads as zeros when the device is not in a write cycle
				1	Reads as ones when the device is in a write cycle
3:2	BP1 BP0	Block Write Protection	R/W	00	No array write protection (Factory Default)
				01	Quarter-array write protection (see Table 6-4)
				10	Half-array write protection (see Table 6-4)
				11	Entire-array write protection (see Table 6-4)
1	WEL	Write Enable Latch	R	0	Device is not write-enabled (Power-Up Default)
				1	Device is write-enabled
0	$\overline{RDY}$/BSY	Ready/Busy Status	R	0	Device is ready for a new sequence
				1	Device is busy with an internal operation

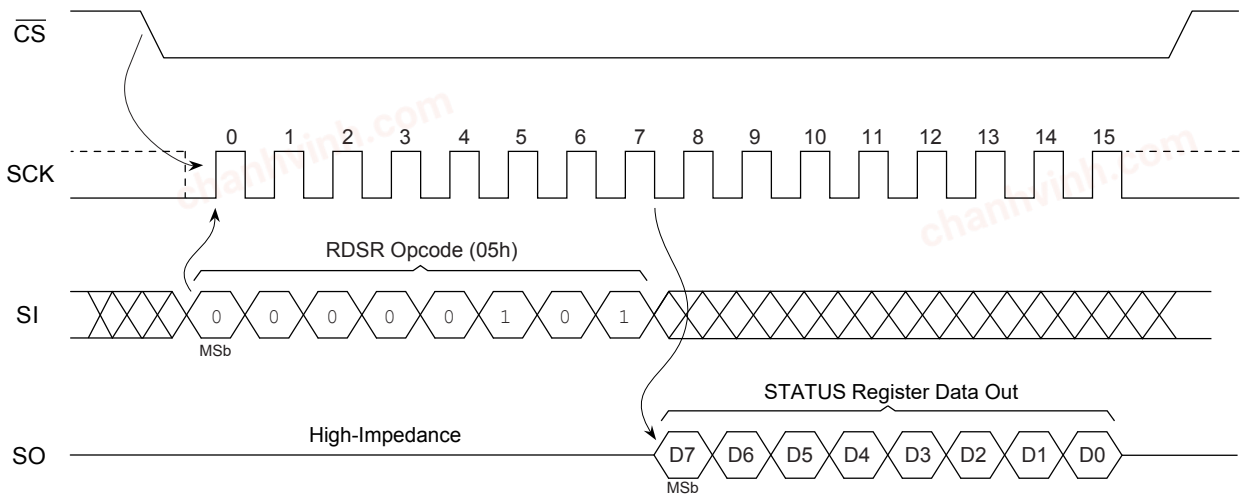
6.2. Read STATUS Register (RDSR)

The Read STATUS Register (RDSR) instruction provides access to the STATUS register. The ready/busy and write-enable status of the device can be determined using the RDSR instruction. Similarly, the Block Write-Protect (BP1, BP0) bits indicate the extent of memory-array protection employed. The STATUS register is read by asserting the $\overline{CS}$ pin, followed by sending a 05h opcode on the SI pin. Upon completion of the opcode, the device returns the 8-bit STATUS register value on the SO pin.

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Figure 6-1. RDSR Waveform



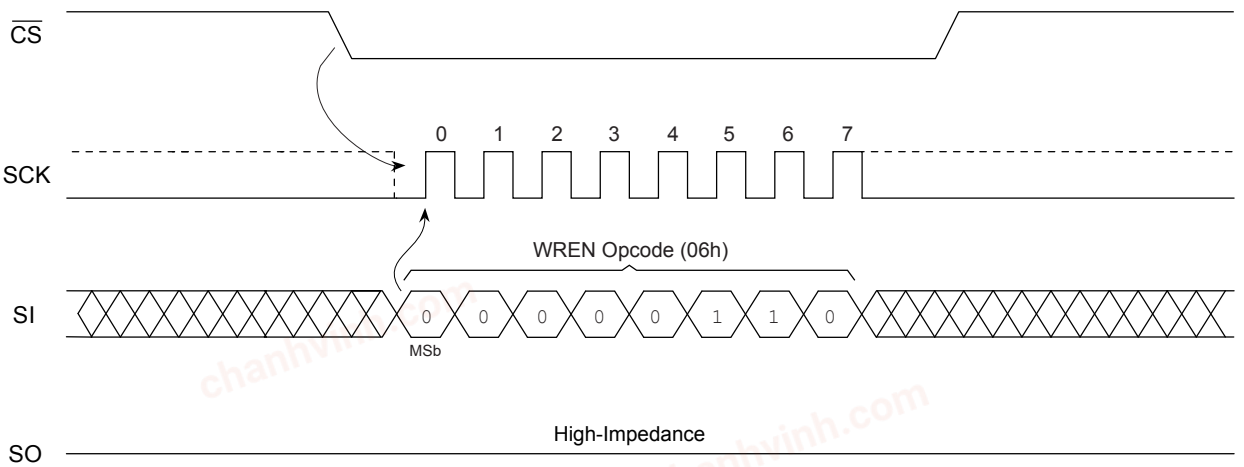
6.3. Write Enable (WREN) and Write Disable (WRDI)

Enabling and disabling writing to the STATUS register and EEPROM array is accomplished through the Write Enable (WREN) and Write Disable (WRDI) instructions. These functions change the status of the WEL bit in the STATUS register.

6.3.1. Write Enable Instruction (WREN)

The Write Enable Latch (WEL) bit of the STATUS register must be set to logic '1' prior to each Write STATUS Register (WRSR) and Write to Memory Array (WRITE) instruction. This is accomplished by sending a WREN (06h) instruction to the AT25080B/AT25160B. First, the $\overline{CS}$ pin is driven low to select the device, and then a WREN instruction is clocked in on the SI pin. After that, the $\overline{CS}$ pin can be driven high, and the WEL bit will be updated in the STATUS register to logic '1'. The device will power up in the Write Disable state (WEL = 0).

Figure 6-2. WREN Timing



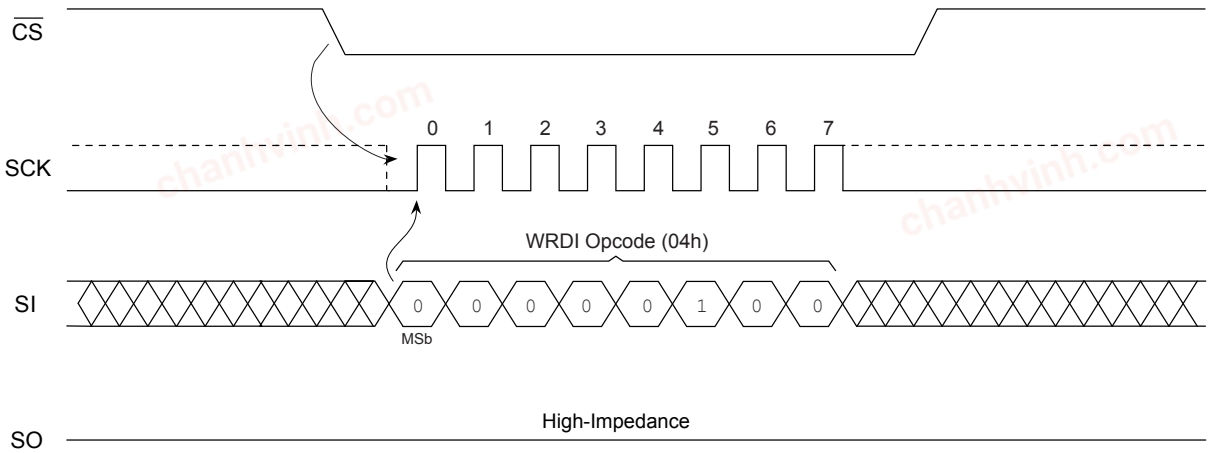
6.3.2. Write Disable Instruction (WRDI)

To protect the device against inadvertent writes, the Write Disable (WRDI) instruction (opcode 04h) disables all programming modes by setting the WEL bit to logic '0'. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

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Figure 6-3. WRDI Timing



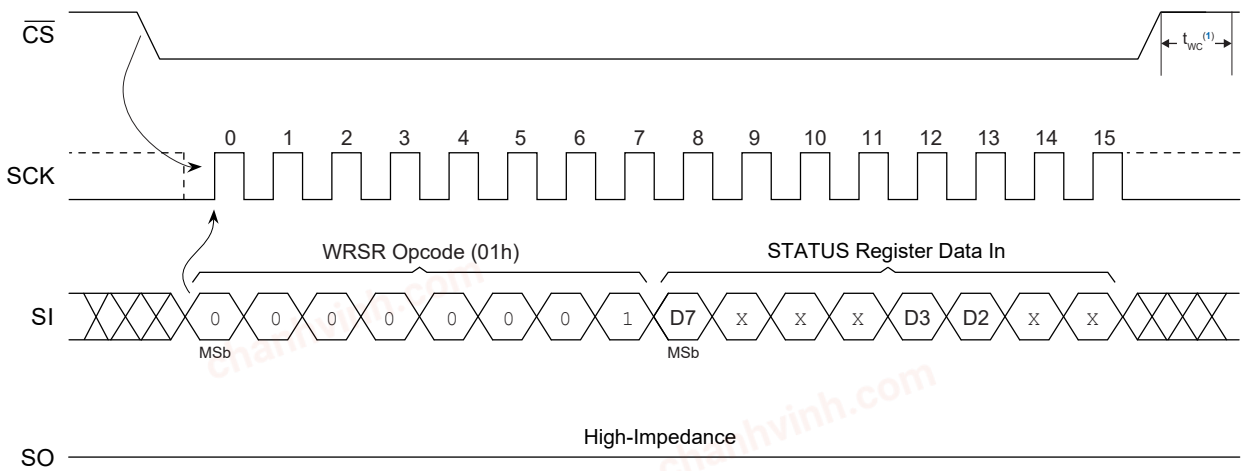
6.4. Write STATUS Register (WRSR)

The Write STATUS Register (WRSR) instruction enables the SPI host to change selected bits of the STATUS register. Before a WRSR instruction can be initiated, a WREN instruction must be executed to set the WEL bit to logic '1'. Upon completion of a WREN instruction, a WRSR instruction can be executed.

Note: The WRSR instruction has no effect on bit 6, bit 5, bit 4, bit 1 or bit 0 of the STATUS register. Only bit 7, bit 3 and bit 2 can be changed using the WRSR instruction. These modifiable bits are the Write-Protect Enable (WPEN) bit and the Block Protect (BP1, BP0) bits. These three bits are nonvolatile bits and have the same properties and functions as regular EEPROM cells. Their values are retained when power is removed from the device.

The AT25080B/AT25160B will not respond to commands other than RDSR following a WRSR instruction until the self-timed internal write cycle has completed. When the write cycle is completed, the WEL bit in the STATUS register is reset to logic '0'.

Figure 6-4. WRSR Waveform



Note:

1. This instruction initiates a self-timed internal write cycle (t_{WC}) on the rising edge of $\overline{CS}$ after a valid sequence.

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6.4.1. Block Write-Protect Function

The WRSR instruction allows the user to configure one of four possible memory array write-protection modes by setting the Block Write-Protect bits (BP1, BP0). The available protection levels are:

- No protection applied to the memory array
- The upper quarter (¼) of the address range is write-protected, making the highest address range read-only
- The upper half (½) of the address range is write-protected, making the highest address range read-only
- The entire memory array is write-protected, making all addresses read-only

The Block Write-Protect levels and their corresponding STATUS register control bits are listed in Table 6-4.

Table 6-4. Block Write-Protect Bits

Level	STATUS Register Bits		Write-Protected/Read-Only Address Range	
	BP1	BP0	AT25080B	AT25160B
0	0	0	None	None
1 (1/4)	0	1	0300h-03FFh	0600h-07FFh
2 (1/2)	1	0	0200h-03FFh	0400h-07FFh
3 (All)	1	1	0000h-03FFh	0000h-07FFh

6.4.2. Write-Protect Enable Function

The WRSR instruction allows the user to enable or disable the Write-Protect ($\overline{WP}$) pin through the use of the Write-Protect Enable (WPEN) bit. When the WPEN bit is set to logic '0', the ability to write to the EEPROM array is determined by the values of the Block Write-Protect (BP1, BP0) bits. The ability to write to the STATUS register is controlled by the WEL bit. When the WPEN bit is set to logic '1', the STATUS register is read-only.

Hardware Write Protection is enabled when both the $\overline{WP}$ pin is low and the WPEN bit is set to logic '1'. When the device is Hardware Write-Protected, writes to the STATUS register—including the Block Write-Protect, WEL and WPEN bits—as well as writes to the sections of the memory array selected by the Block Write-Protect bits, are disabled. When Hardware Write Protection is enabled, writes are allowed only to sections of memory that are not block-protected.

Hardware Write Protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is set to logic '0'. When Hardware Write Protection is disabled, writes are allowed only to sections of memory that are not block-protected. Refer to Table 6-5 for additional information.

Note: When the WPEN bit is hardware write-protected, it cannot be reset to logic '0' while the $\overline{WP}$ pin is held low.

Table 6-5. WPEN Operation

WPEN	$\overline{WP}$ Pin	WEL	Protected Blocks	Unprotected Blocks	STATUS Register
0	x	0	Protected	Protected	Protected
0	x	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
x	High	0	Protected	Protected	Protected
x	High	1	Protected	Writable	Writable

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7. Read Sequence

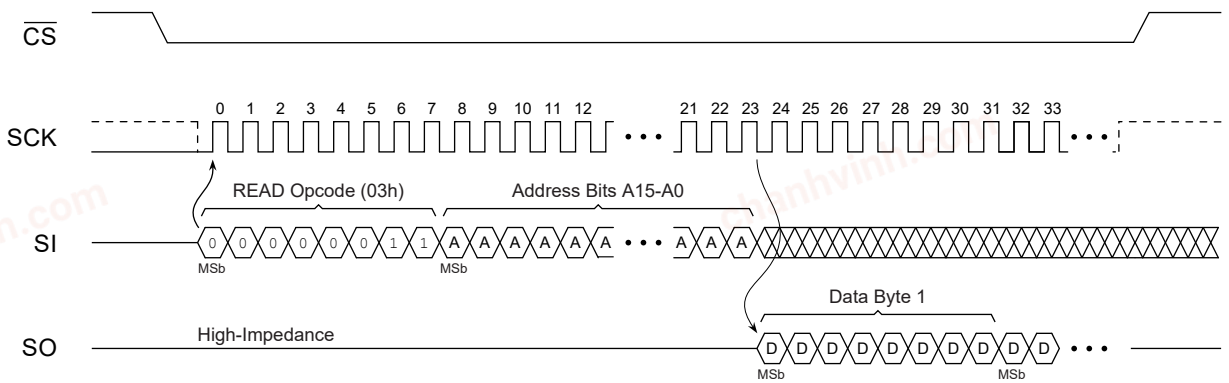
Reading data from the AT25080B/AT25160B via the SO pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the READ (03h) instruction is transmitted via the SI line, followed by the 16-bit address to be read. Refer to Table 7-1 for the AT25080B/AT25160B address bits.

Table 7-1. AT25080B/AT25160B Address Bits

Address	AT25080B	AT25160B
A_N	A_9–A_0	A_{10}–A_0
Don't Care Bits	A_{15}–A_{10}	A_{15}–A_{11}

Upon completion of the 16-bit address, any data present on the SI line will be ignored. The data (D7-D0) at the specified address are then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data are output. The read sequence can continue because the byte address is automatically incremented, allowing data to continue shifting out. When the highest-order address is reached, the address counter rolls over to the lowest-order address, allowing the entire memory array to be read in one continuous read cycle regardless of the starting address.

Figure 7-1. Read Waveform



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8. Write Sequence

To program the AT25080B/AT25160B, two separate instructions must be executed. First, the device *must be write-enabled* using the Write Enable (WREN) instruction. Then, one of the two write sequences described in this section may be executed.

Note: If the device is not write-enabled (WREN), it will ignore the WRITE instruction and return to the Standby state when $\overline{CS}$ is brought high. A new $\overline{CS}$ assertion is required to reinitiate communication.

The address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands except the RDSR instruction are ignored. Refer to Table 8-1 for the AT25080B/AT25160B address bits.

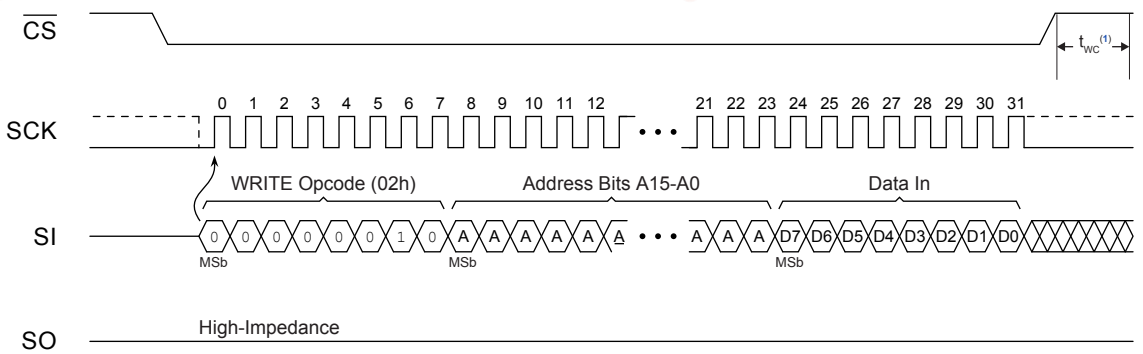
Table 8-1. AT25080B/AT25160B Address Bits

Address	AT25080B	AT25160B
A_N	A_9–A_0	A_{10}–A_0
Don't Care Bits	A_{15}–A_{10}	A_{15}–A_{11}

8.1. Byte Write

A byte write requires the following sequence and is depicted in Figure 8-1. After the $\overline{CS}$ line is pulled low to select the device, the WRITE (02h) instruction is transmitted via the SI line, followed by the 16-bit address and the data (D7-D0) to be programmed. Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low time (Mode 0) and SCK high time (Mode 3) immediately after clocking in the D0 (LSB) data bit. The AT25080B/AT25160B is automatically returned to the Write Disable state (STATUS register bit WEL = 0) at the completion of a write cycle.

Figure 8-1. Byte Write



Note:

1. This instruction initiates a self-timed internal write cycle (t_{WC}) on the rising edge of $\overline{CS}$ after a valid sequence.

8.2. Page Write

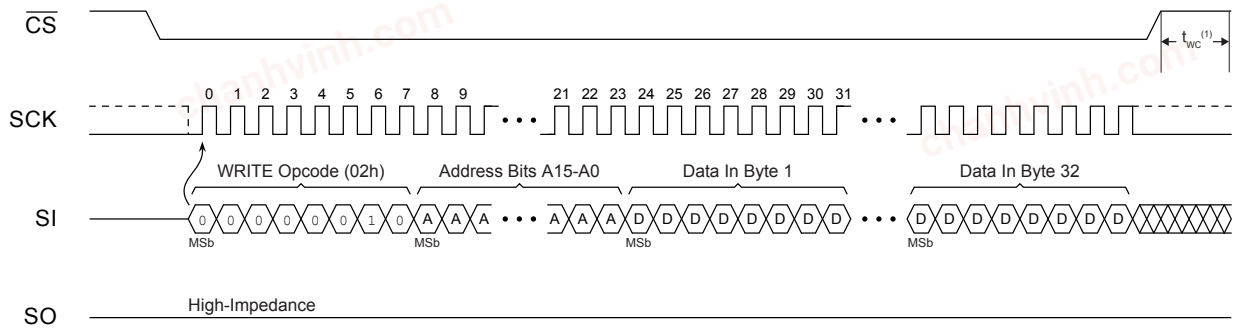
A page write sequence allows up to 32 bytes to be written during the same write cycle, provided that all bytes are within the same row of the memory array. Partial page writes of fewer than 32 bytes are allowed. After each byte of data is received, the five lowest-order address bits are internally incremented. The higher-order address bits are not incremented and therefore retain the memory-array page location. If more bytes of data are transmitted than can fit within the current memory row, the address counter rolls over to the beginning of the same row. However, rollover events should be avoided as previously loaded data in the page may be unintentionally altered. The

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AT25080B/AT25160B automatically returns to the Write Disable state (WEL = 0) upon completion of a write cycle.

Figure 8-2. Page Write



Note:

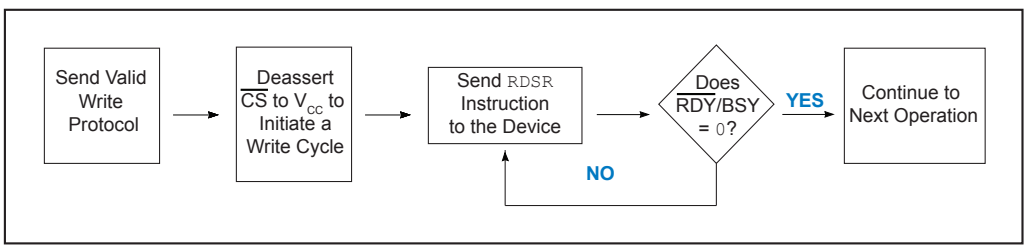
1. This instruction initiates a self-timed internal write cycle (t_{WC}) on the rising edge of $\overline{CS}$ after a valid sequence.

8.3. Polling Routine

A polling routine can be implemented to optimize time-sensitive applications that prefer not to wait the fixed maximum write cycle time (t_{WC}). This method allows the application to determine when the write cycle has completed so that a subsequent operation can begin.

Once the internally timed write cycle has started, a polling routine can be initiated. This involves repeatedly sending a Read STATUS Register (RDSR) instruction to determine whether the device has completed its self-timed internal write cycle. If the $\overline{RDY}$/BSY bit (bit 0 of STATUS register) = 1, the write cycle is still in progress. If bit 0 = 0, the write cycle has ended. If the $\overline{RDY}$/BSY bit = 1, repeated RDSR commands can be executed until the $\overline{RDY}$/BSY bit = 0, signaling that the device is ready to execute a new instruction. Only the Read STATUS Register (RDSR) instruction is enabled during the write cycle.

Figure 8-3. Polling Flowchart



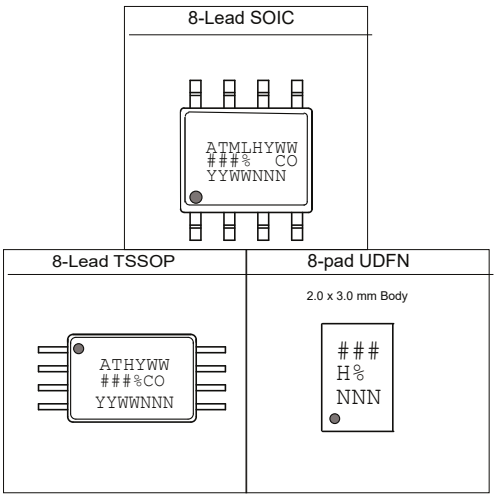
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9. Packaging Information

9.1. Package Marking Information

AT25080B and AT25160B: Package Marking Information



Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

Catalog Number Truncation	
AT25080B	Truncation Code ###: 58B
AT25160B	Truncation Code ###: 5AB

Date Codes	**Voltage**
Y = Year code (last digit of calendar year) YY = Year code (last 2 digits of calendar year) WW = Week code (week of January 1 is week '01')	% = Minimum Voltage L: 1.8V min

Country of Origin	**Device Grade**	**Atmel Truncation**
CO = Country of Origin	H or U: Industrial Grade	AT: Atmel ATM: Atmel ATML: Atmel

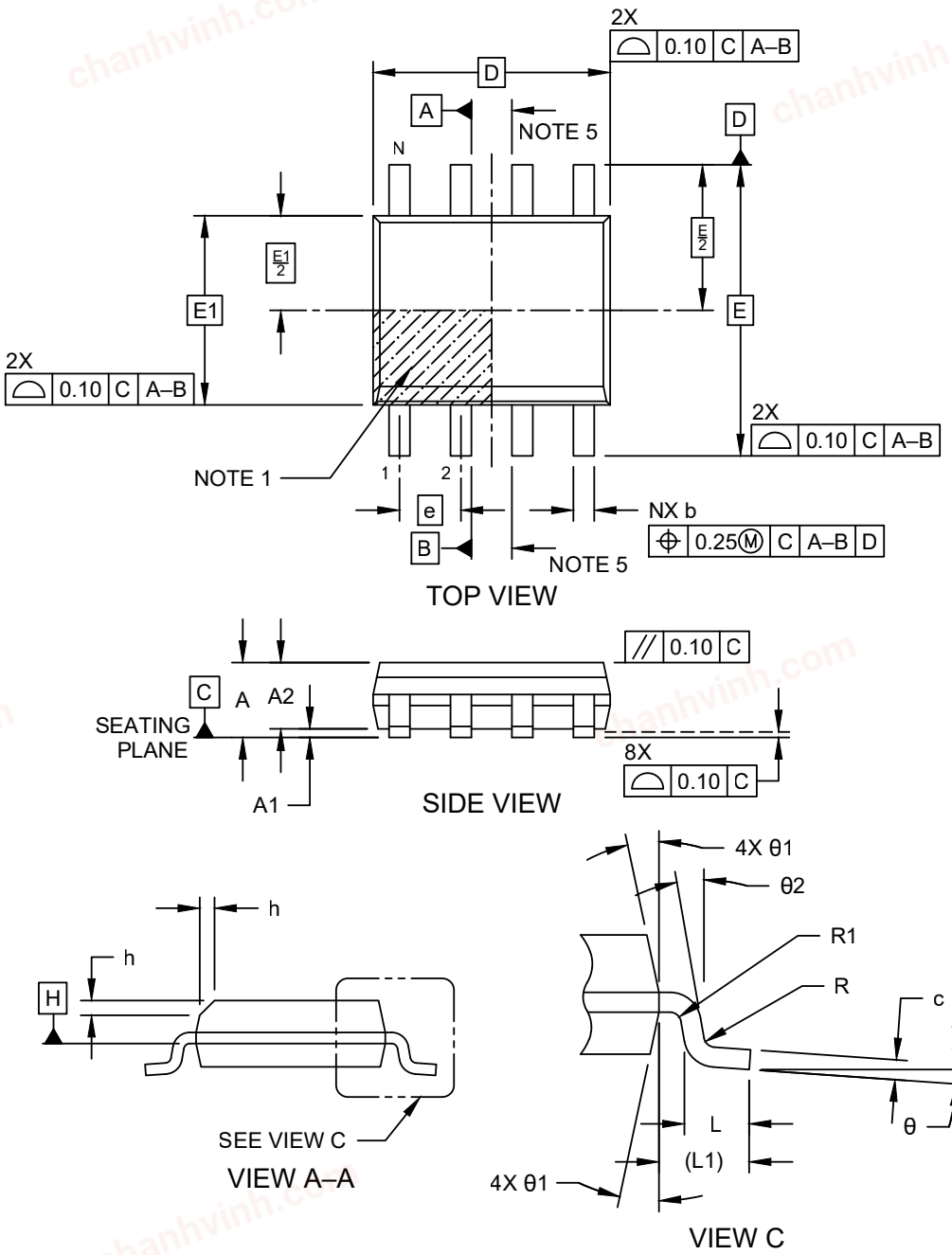
Lot Number or Trace Code
NNN = Alphanumeric Trace Code (2 Characters for Small Packages)

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



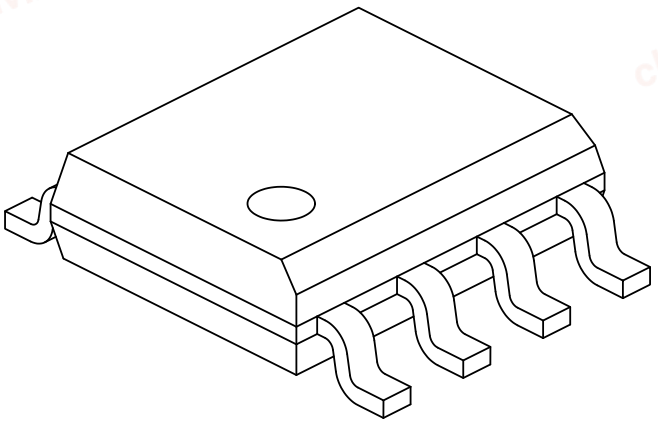
Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 1 of 2

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Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

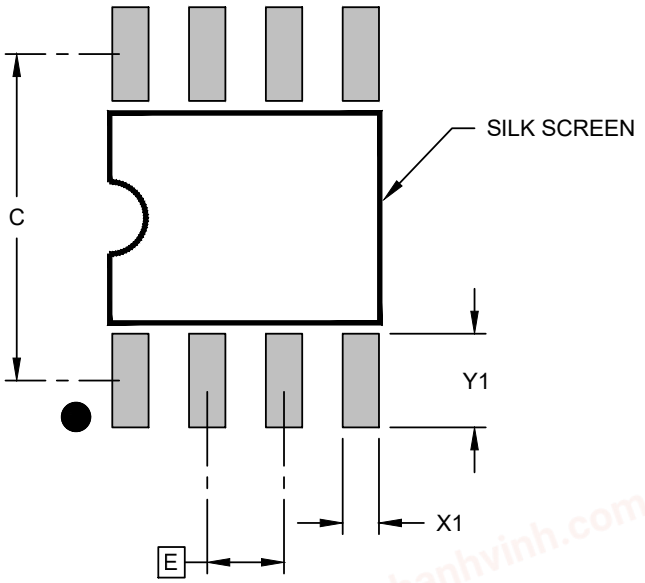
Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

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RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

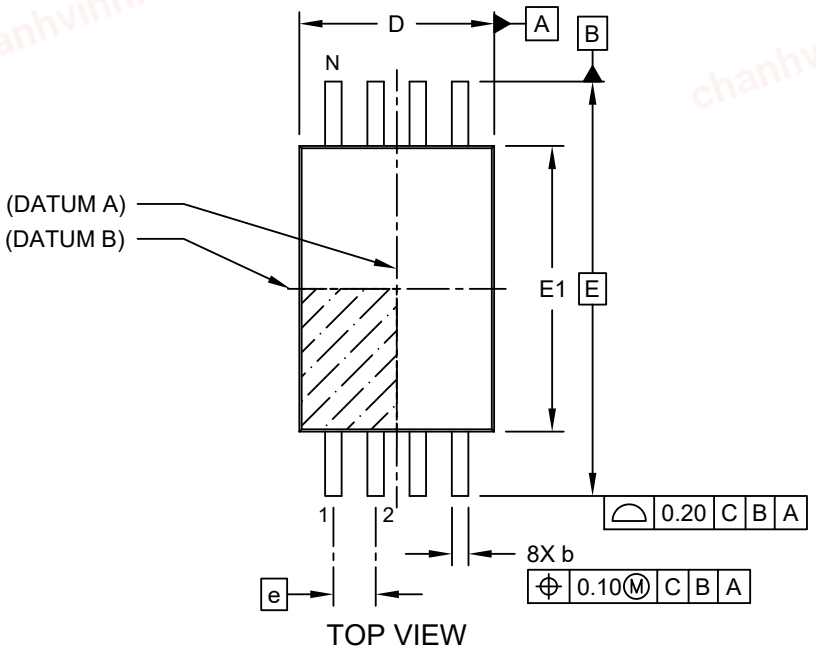
Microchip Technology Drawing C04-02057-SN Rev L

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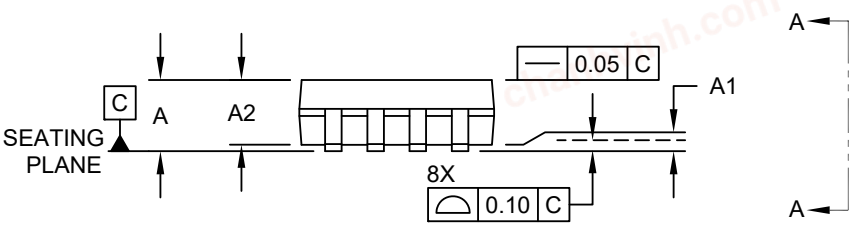
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8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

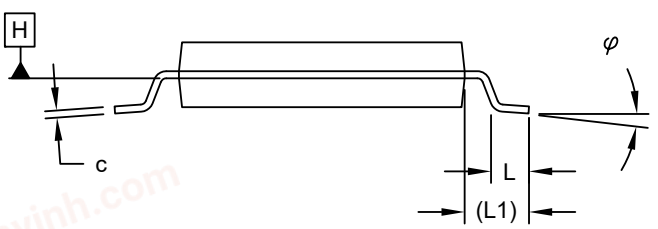
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

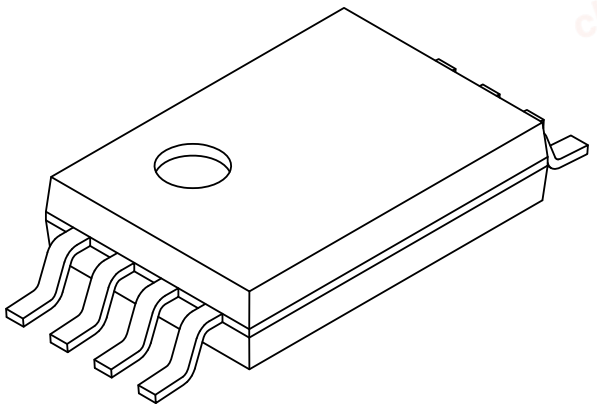
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Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	-
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

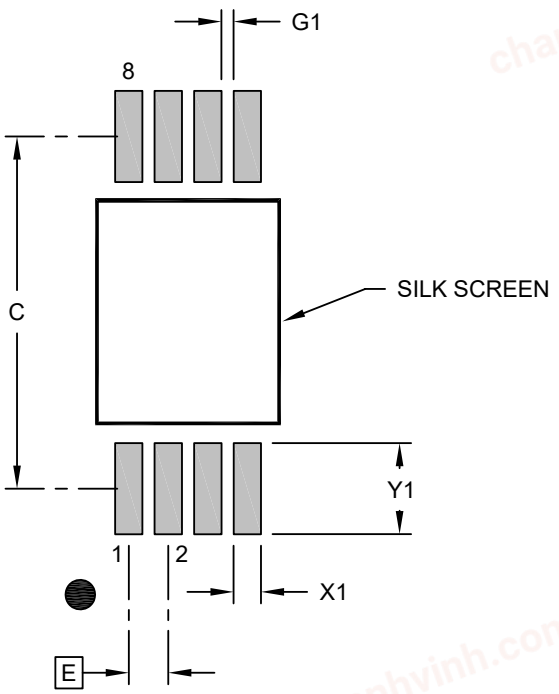
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8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

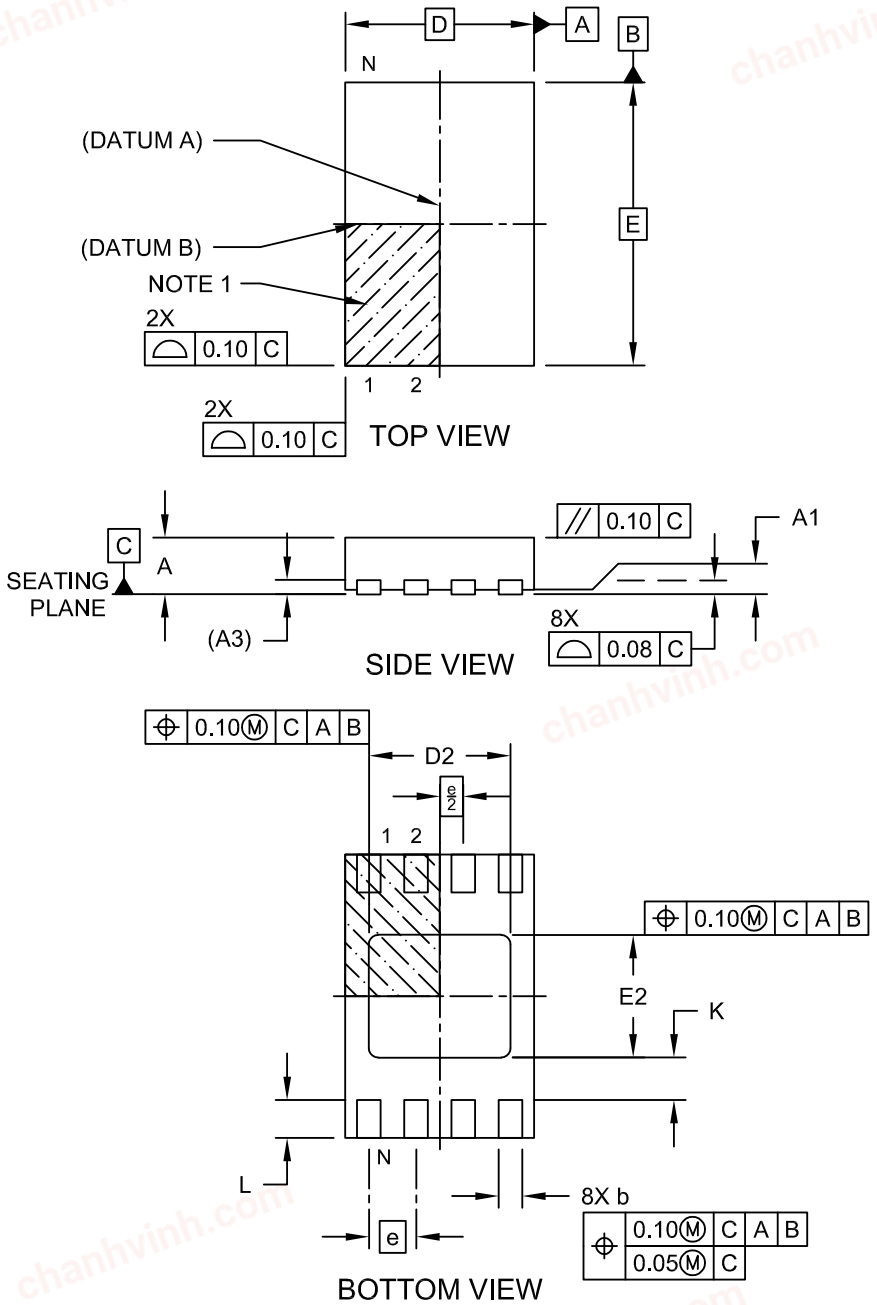
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8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



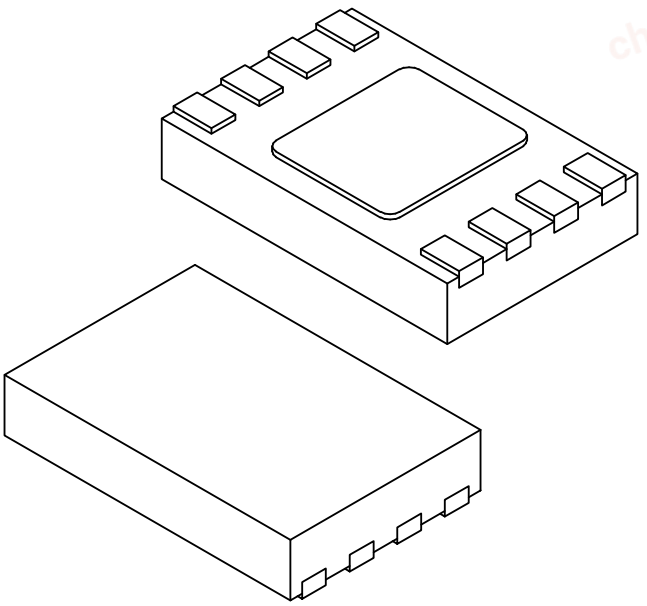
Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 1 of 2

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8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.25	0.35	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

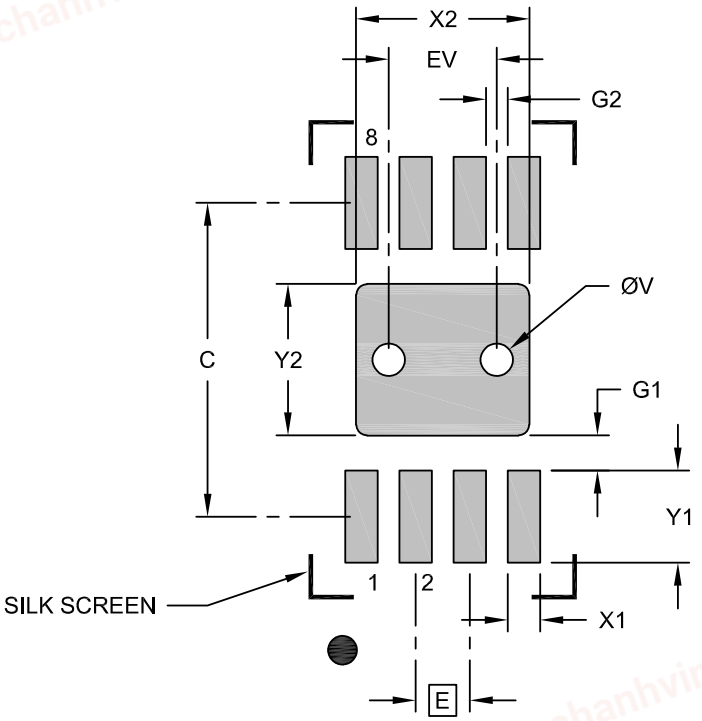
Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 2 of 2

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8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.33		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23355-Q4B Rev C

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10. Revision History

Revision C (September 2026)
Removed VFBGA package that has reached end-of-life status. Made minor editorial updates throughout the document.

Revision B (February 2024)
Removed 8-pad XDFN product offering. Replaced terminology "Master" and "Slave" with "Host" and "Client," respectively.

Revision A (August 2019)
Updated to the Microchip template. Microchip DS20006244 replaces Atmel document 5228. Updated Part Marking Information. Added ESD rating. Removed the 8-ball WLCSP detail and ordering code. Removed lead finish designation. Added POR recommendations section. Updated trace code format in package markings. Updated section content throughout for clarification. Updated the 8U3-1 VFBGA package drawing. Updated the SOIC, TSSOP and UDFN package drawings to the Microchip equivalents.

Atmel Document 5228 Revision G (January 2015)
Add the AT25080B-MAHL-E and AT25160B-MAHL-E package options. Update the 8MA2 and 8U-12 package drawings and the ordering information.

Atmel Document 5228 Revision F (July 2014)
Add WLSCP package option. Update 8X, 8MA2, 8ME1, and 8U3-1 package drawings. Update template, Atmel logos, disclaimer page.

Atmel Document 5228 Revision E (March 2012)
Update 8A2 to 8X and 8S1, 8MA2, 8U3-1 package drawings.

Atmel Document 5228 Revision D (April 2010)
Update Ordering Code Detail and Ordering Information.

Atmel Document 5228 Revision C (August 2009)
Change Catalog Scheme and add Marking Details.

Atmel Document 5228 Revision B (July 2008)
Change ‘Endurance’ parameter on page 6.

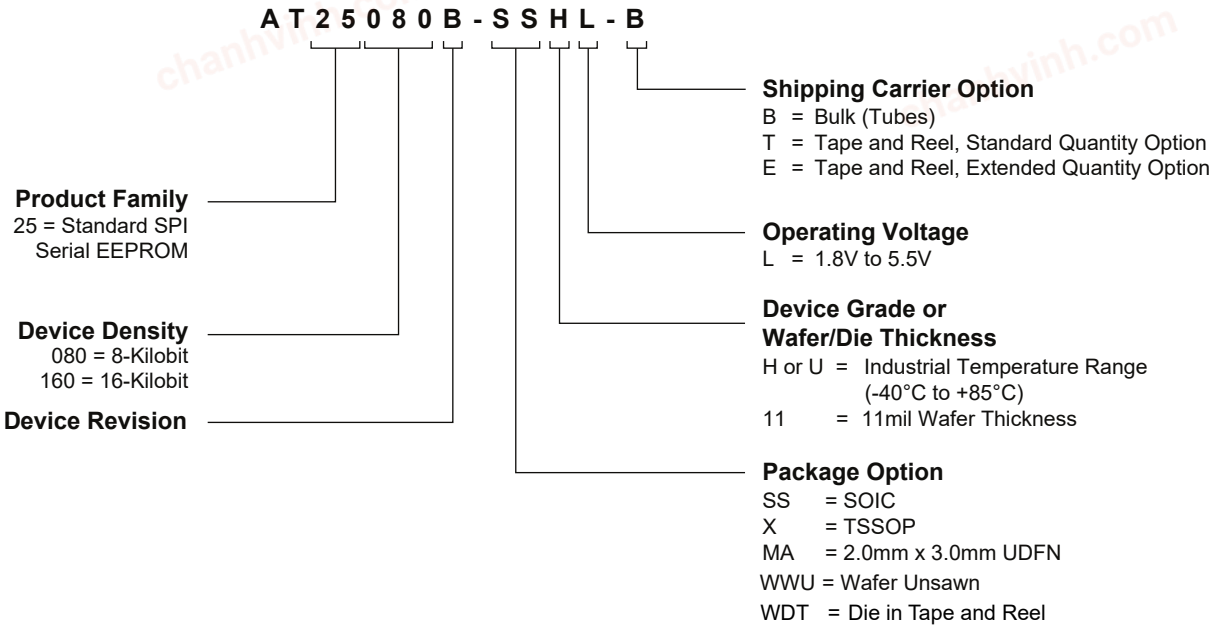
Atmel Document 5228 Revision A (September 2007)
Initial document release.

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11. Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.



Note: Refer to automotive data sheet for automotive grade ordering information.

Examples:

Device	Package	Package Drawing Code	Package Option	Shipping Carrier Option	Device Grade
AT25080B-SSHL-B	SOIC	SN	SS	Bulk (Tubes)	Industrial Temperature (-40°C to 85°C)
AT25080B-SSHL-T	SOIC	SN	SS	Tape and Reel	
AT25160B-SSHL-T	SOIC	SN	SS	Tape and Reel	
AT25080B-XHL-B	TSSOP	ST	X	Bulk (Tubes)	
AT25160B-XHL-T	TSSOP	ST	X	Tape and Reel	
AT25080B-MAHL-E	UDFN	Q4B	MA	Tape and Reel	
AT25160B-MAHL-T	UDFN	Q4B	MA	Tape and Reel	
AT25160B-MAHL-E	UDFN	Q4B	MA	Tape and Reel	

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Product Page Links

AT25080B, AT25160B

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