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AT21CS01/AT21CS11

Single-Wire, I/O Powered 1-Kbit (128 x 8) Serial EEPROM with a Unique, Factory-Programmed 64-Bit Serial Number

Features

- Low-Voltage Operation:
  - AT21CS01 is self-powered via the 1.7V to 3.6V pull-up voltage on the SI/O line
  - AT21CS11 is self-powered via the 2.7V to 4.5V pull-up voltage on the SI/O line
- Internally Organized as 128 Words of Eight Bits Each (1-Kbit)
- Single-Wire Serial Interface with I^2C Protocol Structure:
  - Device communication is achieved through a single I/O pin
- Standard Speed and High-Speed Mode Options:
  - 15.4 kbps maximum bit rate in Standard Speed mode (AT21CS01 only)
  - 125 kbps maximum bit rate in High-Speed mode (AT21CS01 and AT21CS11)
- 8-Byte Page Write or Single Byte Writes Allowed
- Discovery Response Feature for Quick Detection of Devices on the Bus
- ROM Zone Support:
  - Device is segmented into four 256-bit zones, each of which can be permanently made read-only (ROM)
- 256-bit Security Register:
  - Lower eight bytes contains a factory-programmed, read-only, 64-bit serial number that is unique to all Microchip single-wire products
  - Next eight bytes are reserved for future use and will read FFh
  - Upper 16 bytes are user-programmable and permanently lockable
- Self-Timed Write Cycle (5 ms maximum)
- Manufacturer Identification Register:
  - Device responds with unique value for Microchip as well as density and revision information
- High Reliability:
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
  - IEC 61000-4-2 Level 4 ESD Compliant (±8 kV Contact, ±15 kV Air Discharge)
- Green (Lead-free/Halide-free/RoHS Compliant) Package Options
- Die Sale Options in Wafer Form and Tape and Reel

Packages

2-pad XSFN, 3-lead SOT23, 8-lead SOIC and 4-ball thin WLCSP.

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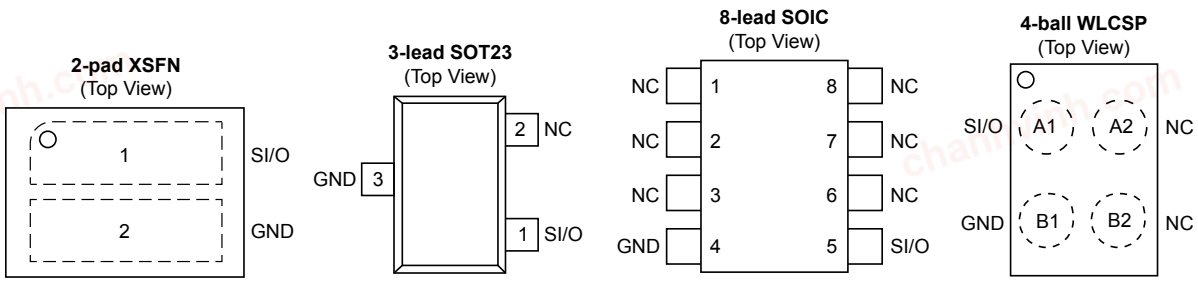
Package Types (not to scale)



Description

The AT21CS01/11 is a 2-pin memory (SI/O signal and Ground) that harvests energy from the signal pin to power the integrated circuit. It provides 1,024 bits of Serial Electrically Erasable and Programmable Read-Only Memory (SEEPROM) organized as 128 words of eight bits each.

The device is optimized to add configuration and use information in unpowered attachments using a two-point mechanical connection that brings only one signal (SI/O) and GND to the unpowered attachment. Some unpowered attachment application examples include analog sensor calibration data storage, ink and toner printer cartridge identification, and management of after-market consumables. The device's software addressing scheme allows up to eight devices to share a common single-wire bus. The device is available in space-saving package options and operates with an external pull-up voltage from 1.7V to 3.6V on the SI/O line (AT21CS01) or from 2.7V to 4.5V on the SI/O line (AT21CS11).

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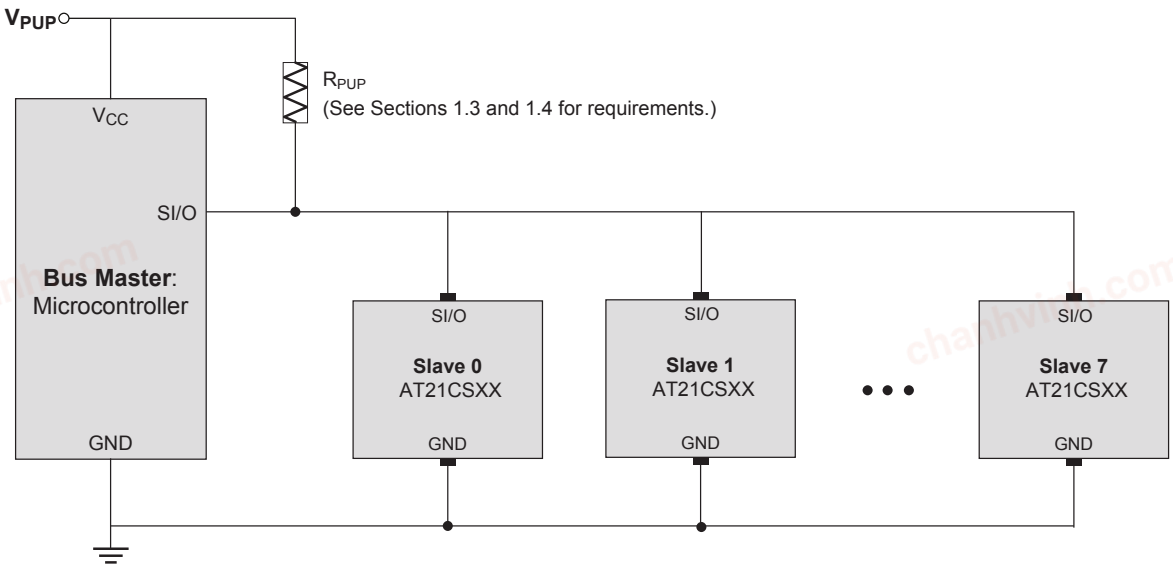
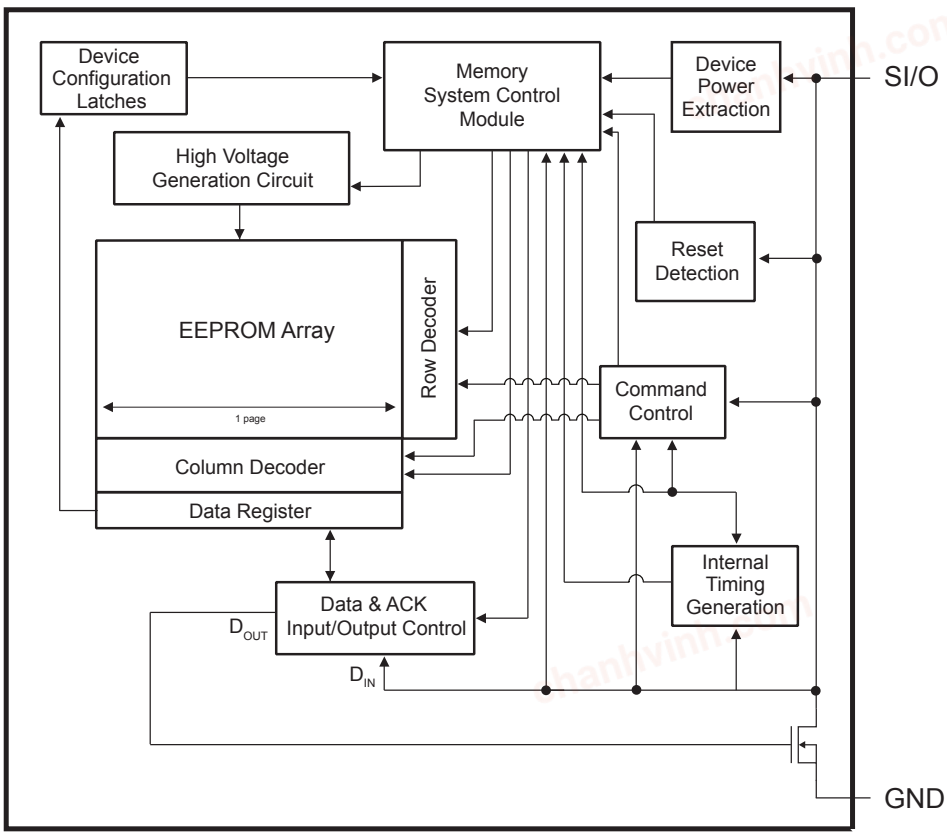
System Configuration Using Single-Wire Serial EEPROMs



Block Diagram



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1. Electrical Characteristics

1.1 Absolute Maximum Ratings(1)

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-0.6V to V_{PUP} +0.5V
DC output current	15.0 mA

Note:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.2 AT21CS01/11 DC and AC Operating Range

		AT21CS01	AT21CS11
Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C	-40°C to +85°C
V_{PUP} Voltage tied to SI/O	Voltage Range	1.7V to 3.6V	2.7V to 4.5V

1.3 AT21CS01 DC Characteristics(1)

Parameter	Symbol	Minimum	Typical(2)	Maximum	Units	Test Conditions
Pull-up Voltage	V_{PUP}	1.7	—	3.6	V	High-Speed mode
		2.7	—	3.6	V	Standard Speed mode
Pull-up Resistance	R_{PUP}	130	—	200	Ω	V_{PUP} = 1.7V
		0.2	—	1.8	kΩ	V_{PUP} = 2.7V
		0.33	—	4	kΩ	V_{PUP} = 3.6V
Active Current, Read	I_{A1}	—	0.08	0.3	mA	V_{PUP} = 3.6V; SI/O = V_{PUP}
Active Current, Write	I_{A2}	—	0.20	0.5	mA	V_{PUP} = 3.6V
Standby Current	I_{SB}	—	0.6	1.5	µA	V_{PUP} = 1.8V(3); SI/O = V_{PUP}
		—	0.7	2.5	µA	V_{PUP} = 3.6V
Input Low Level(3)(4)	V_{IL}	–0.6	—	0.5	V	
Input High Level(3)(4)	V_{IH}	V_{PUP} x 0.7	—	V_{PUP} + 0.5	V	

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Parameter	Symbol	Minimum	Typical(2)	Maximum	Units	Test Conditions
SI/O Hysteresis(3)(4)(5)	V_{HYS}	0.128	—	1.17	V	
Output Low Level	V_{OL}	0	—	0.4	V	I_{OL} = 4 mA
Bus Capacitance	C_{BUS}	—	—	1000	pF	

Note:

1. Parameters are applicable over the operating range in AT21CS01/11 DC and AC Operating Range, unless otherwise noted.
2. Typical values characterized at T_A = +25°C unless otherwise noted.
3. This parameter is characterized but is not 100% tested in production.
4. V_{IH}, V_{IL}, and V_{HYS} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, C_{BUS}, and timing used. Use of a lower V_{PUP}, higher R_{PUP}, higher C_{BUS}, and shorter t_{RCV} creates lower V_{IH}, V_{IL} and V_{HYS} values.
5. Once V_{IH} is crossed on a rising edge of SI/O, the voltage on SI/O must drop at least by V_{HYS} to be detected as a logic '0'.

1.4 AT21CS11 DC Characteristics(1)

Parameter	Symbol	Minimum	Typical(2)	Maximum	Units	Test Conditions
Pull-up Voltage	V_{PUP}	2.7	—	4.5	V	High-Speed mode
Pull-up Resistance	R_{PUP}	0.2	—	1.8	kΩ	V_{PUP} = 2.7V
		0.4	—	5.4	kΩ	V_{PUP} = 4.5V
Active Current, Read	I_{A1}	—	0.08	0.3	mA	V_{PUP} = 4.5V; SI/O = V_{PUP}
Active Current, Write	I_{A2}	—	0.20	0.5	mA	V_{PUP} = 4.5V
Standby Current	I_{SB}	—	0.6	1.5	µA	V_{PUP} = 2.7V(3); SI/O = V_{PUP}
		—	0.7	3.0	µA	V_{PUP} = 4.5V; SI/O = V_{PUP}
Input Low Level(3)(4)	V_{IL}	–0.6	—	0.5	V	
Input High Level(3)(4)	V_{IH}	V_{PUP} x 0.7	—	V_{PUP} + 0.5	V	
SI/O Hysteresis(3)(4)(5)	V_{HYS}	0.128	—	1.4	V	
Output Low Level	V_{OL}	0	—	0.4	V	I_{OL} = 4 mA
Bus Capacitance	C_{BUS}	—	—	1000	pF	

Note:

1. Parameters are applicable over the operating range in AT21CS01/11 DC and AC Operating Range, unless otherwise noted.
2. Typical values characterized at T_A = +25°C unless otherwise noted.
3. This parameter is characterized but is not 100% tested in production.

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4. V_{IH}, V_{IL}, and V_{HYS} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, C_{BUS}, and timing used. Use of a lower V_{PUP}, higher R_{PUP}, higher C_{BUS}, and shorter t_{RCV} creates lower V_{IH}, V_{IL} and V_{HYS} values.
5. Once V_{IH} is crossed on a rising edge of SI/O, the voltage on SI/O must drop at least by V_{HYS} to be detected as a logic '0'.

1.5 AT21CS01/11 AC Characteristics

1.5.1 Reset and Discovery Response Timing

Parameter and Condition[1][2]	Symbol	Standard Speed[3][4]		High Speed		Units
		Min.	Max.	Min.	Max.	
Reset Low Time, Device in Inactive State	t_{RESET}	480	—	48	—	µs
Discharge Low Time, Device in Active Write Cycle (t_{WR})	t_{DSCHG}	150	—	150	—	µs
Reset Recovery Time	t_{RRT}	N/A	N/A	8	—	µs
Discovery Response Request	t_{DRR}	N/A	N/A	1	2 - t_{PUP}[5]	µs
Discovery Response Acknowledge Time	t_{DACK}	N/A	N/A	8	24	µs
Master Strobe Discovery Response Time	t_{MSDR}	N/A	N/A	2	6	µs
SI/O High Time for Start/Stop Condition	t_{HTSS}	N/A	N/A	150	—	µs

Note:

1. Parameters applicable over operating range in AT21CS01/11 DC and AC Operating Range, unless otherwise noted.
2. AC measurement conditions for the table above:
   - Loading capacitance on SI/O: 100 pF
   - R_{PUP} (bus line pull-up resistor to V_{PUP}): 1 kΩ; V_{PUP}: 2.7V
3. Due to the fact that the device will default to High-Speed mode upon Reset, the Reset and Discovery Response Timing after t_{RESET} does not apply for Standard Speed mode. High-Speed mode timing applies in all cases after t_{RESET}.
4. Standard Speed is not available on the AT21CS11.
5. t_{PUP} is the time required once the SI/O line is released to be pulled up from V_{IL} to V_{IH}. This value is application specific and is a function of the loading capacitance on the SI/O line as well as the R_{PUP} chosen. Limits for these values are provided in AT21CS01 DC Characteristics(1) and AT21CS11 DC Characteristics(1).

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1.5.2 Data Communication Timing

Parameter and Condition[1][2]	Symbol	Frame Type	Standard Speed[3]		High Speed		Units
			Min.	Max.	Min.	Max.	
Bit Frame Duration	t_{BIT}	Input and Output Bit Frame	40	100	t_{LOW0} + t_{PUP}[4] + t_{RCV}	25	µs
SI/O High Time for Start/Stop Condition	t_{HTSS}	Input Bit Frame	600	—	150	—	µs
SI/O Low Time, Logic '0' Condition	t_{LOW0}	Input Bit Frame	24	64	6	16	µs
SI/O Low Time, Logic '1' Condition	t_{LOW1}	Input Bit Frame	4	8	1	2	µs
Master SI/O Low Time During Read	t_{RD}	Output Bit Frame	4	8 - t_{PUP}[4]	1	2 - t_{PUP}[4]	µs
Master Read Strobe Time	t_{MRS}	Output Bit Frame	t_{RD} + t_{PUP}[4]	8	t_{RD} + t_{PUP}[4]	2	µs
Data Output Hold Time (Logic '0')	t_{HLD0}	Output Bit Frame	8	24	2	6	µs
Slave Recovery Time	t_{RCV}	Input and Output Bit Frame	8	—	2[5]	—	µs
Noise Filtering Capability on SI/O	t_{NOISE}	Input Bit Frame	0.5	—	—	—	µs

Note:

1. Parameters applicable over operating range in AT21CS01/11 DC and AC Operating Range, unless otherwise noted.
2. AC measurement conditions for the table above:
   - Loading capacitance on SI/O: 100 pF
   - R_{PUP} (bus line pull-up resistor to V_{PUP}): 1 kΩ; V_{PUP}: 2.7V
3. Standard Speed is not available on the AT21CS11.
4. t_{PUP} is the time required once the SI/O line is released to be pulled up from V_{IL} to V_{IH}. This value is application specific and is a function of the loading capacitance on the SI/O line as well as the R_{PUP} chosen. Limits for these values are provided in AT21CS01 DC Characteristics(1).
5. The system designer must select an combination of R_{PUP}, C_{BUS}, and t_{BIT} such that the minimum t_{RCV} is satisfied. The relationship of t_{RCV} within the bit frame can be expressed by the following formula: $t_{BIT} = t_{LOW0} + t_{PUP} + t_{RCV}$.

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1.5.3 EEPROM Cell Performance Characteristics

Operation	Min.	Max.	Units	Test Condition
Write Cycle Time (t_{WR})	—	5	ms	V_{PUP} (min.) < V_{PUP} < V_{PUP} (max.), T_A = 25°C, Byte or Page Write mode
Write Endurance(1)	1,000,000	—	Write Cycles	V_{PUP} (min.) < V_{PUP} < V_{PUP} (max.), T_A = 25°C, Byte or Page Write mode
Data Retention(2)	100	—	Years	V_{PUP} (min.) < V_{PUP} < V_{PUP} (max.), T_A = 55°C

Note:

1. Write endurance performance is determined through characterization and the qualification process.
2. The data retention capability is determined through qualification and checked on each device in production.

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2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	2-pad XSFN	3-lead SOT23	8-lead SOIC	4-ball WLCSP	Function
NC	—	—	1	—	No Connect
NC	—	—	2	—	No Connect
NC	—	2	3	—	No Connect
GND	2	3	4	B1	Ground
SI/O	1	1	5	A1	Serial Input and Output
NC	—	—	6		No Connect
NC	—	—	7	—	No Connect
NC	—	—	8	—	No Connect

2.1 No Connect

The NC pins are not internally connected. These pins can be connected to GND or left floating.

2.2 Serial Input and Output

The SI/O pin is an open-drain, bidirectional input/output pin used to serially transfer data to and from the device.

The SI/O pin must be pulled high using an external pull-up resistor (not to exceed 4 kΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

The device also uses the SI/O pin as its voltage source by drawing and storing power during the periods that the pin is pulled high to a voltage level between 1.7V and 3.6V (AT21CS01) and between 2.7V and 4.5V (AT21CS11).

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3. Device Operation and Communication

The AT21CS01/11 operates as a slave device and utilizes a single-wire digital serial interface to communicate with a host controller, commonly referred to as the bus master. The master controls all read and write operations to the slave devices on the serial bus. The device has two speeds of operation, Standard Speed mode (AT21CS01) and High-Speed mode (AT21CS01 and AT21CS11).

The device utilizes an 8-bit data structure. Data is transferred to and from the device via the single-wire serial interface using the Serial Input/Output (SI/O) pin. Power to the device is also provided via the SI/O pin, thus only the SI/O pin and the GND pin are required for device operation. Data sent to the device over the single-wire bus is interpreted by the state of the SI/O pin during specific time intervals or slots. Each time slot is referred to as a bit frame and lasts t_{BIT} in duration. The master initiates all bit frames by driving the SI/O line low. All commands and data information are transferred with the Most Significant bit (MSb) first.

The software sequence sent to the device is an emulation of what would be sent to an I^2C Serial EEPROM with the exception that typical 4-bit device type identifier of `1010b` in the device address is replaced by a 4-bit opcode. The device has been architected in this way to allow for rapid deployment and significant reuse of existing I^2C firmware. For more details about the way the device operates, refer to Device Addressing and I2C Protocol Emulation .

During bus communication, one data bit is transmitted in every bit frame, and after eight bits (one byte) of data has been transferred, the receiving device must respond with either an acknowledge (ACK) or a no-acknowledge (NACK) response bit during a ninth bit window. There are no unused clock cycles during any read or write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle. In the event where an unavoidable system interrupt is required, refer to the requirements outlined in Communication Interruptions.

3.1 Single-Wire Bus Transactions

Types of data transmitted over the SI/O line:

- Reset and Discovery Response
- Logic '0' or Acknowledge (ACK)
- Logic '1' or No Acknowledge (NACK)
- Start Condition
- Stop Condition

The Reset and Discovery Response is not considered to be part of the data stream to the device, whereas the remaining four transactions are all required in order to send data to and receive data from the device. The difference between the different types of data stream transactions is the duration that SI/O is driven low within the bit frame.

3.1.1 Device Reset/Power-up and Discovery Response

3.1.1.1 Resetting the Device

A Reset and Discovery Response sequence is used by the master to reset the device as well as to perform a general bus call to determine if any devices are present on the bus.

To begin the Reset portion of the sequence, the master must drive SI/O low for a minimum time. If the device is not currently busy with other operations, the master can drive SI/O low for a time of t_{RESET}. The length of t_{RESET} differs for Standard Speed mode and for High-Speed mode.

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However, if the device is busy, the master must drive SI/O for a longer time of t_{DSCHG} to ensure the device is reset as discussed in Interrupting the Device during an Active Operation. The Reset time forces any internal charge storage within the device to be consumed, causing the device to lose all remaining standby power available internally.

Upon SI/O being released for a sufficient amount of time to allow the device time to power-up and initialize, the master must then always request a Discovery Response Acknowledge from the AT21CS01/11 prior to any commands being sent to the device. The master can then determine if an AT21CS01/11 is present by sampling for the Discovery Response Acknowledge from the device.

3.1.1.2 Device Response Upon Reset or Power-Up

After the device has been powered up or after the master has reset the device by holding the SI/O line low for t_{RESET} or t_{DSCHG}, the master must then release the line which will be pulled high by an external pull-up resistor. The master must then wait an additional minimum time of t_{RRT} before the master can request a Discovery Response Acknowledge from the device.

The Discovery Response Acknowledge sequence begins by the master driving the SI/O line low which will start the AT21CS01/11 internal timing circuits. The master must continue to drive the line low for t_{DRR}.

During the t_{DRR} time, the AT21CS01/11 will respond by concurrently driving SI/O low. The device will continue to drive SI/O low for a total time of t_{DACK}. The master should sample the state of the SI/O line at t_{MSDR} past the initiation of t_{DRR}. By definition, the t_{DACK} minimum is longer than the t_{MSDR} maximum time, thereby ensuring the master can always correctly sample the SI/O for a level less than V_{IL}. After the t_{DACK} time has elapsed, the AT21CS01/11 will release SI/O which will then be pulled high by the external pull-up resistor.

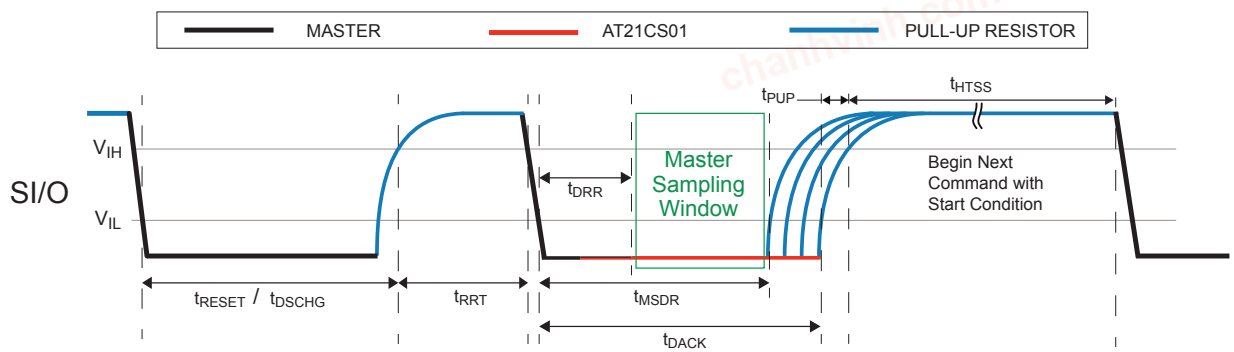
The master must then wait t_{HTSS} to create a Start condition before continuing with the first command (see Start/Stop Condition for more details about Start conditions). By default, the device will come out of Reset in High-Speed mode. Changing the device to Standard Speed mode is covered in Standard Speed Mode (Opcode Dh). The AT21CS01/11 will power-up with its internal Address Pointer set to zero.

The timing requirements for the Reset and Discovery Response sequence for both Standard Speed and High-Speed mode can be found in AT21CS01/11 AC Characteristics.

3.1.2 Interrupting the Device during an Active Operation

To conserve the stored energy within the onboard parasitic power system and minimize overall active current, the AT21CS01/11 will not monitor the SI/O line for new commands while it is busy executing a previously sent command. As a result, the device is not able to sense how long SI/O has been in a given state. If the master requires to interrupt the device during an active operation, it must drive SI/O low long enough to deplete all of its remaining stored power. This time is defined as t_{DSCHG}, after which a normal Discovery Response can begin by releasing the SI/O line.

Figure 3-1. Reset and Discovery Response Waveform



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3.1.3 Data Input and Output Bit Frames

Communication with the AT21CS01/11 is conducted in time intervals referred to as a bit frame and lasts t_{BIT} in duration. Each bit frame contains a single binary data value. Input bit frames are used to transmit data from the master to the AT21CS01/11 and can either be a logic '0' or a logic '1'. An output bit frame carries data from the AT21CS01/11 to the master. In all input and output cases, the master initiates the bit frame by driving the SI/O line low. Once the AT21CS01/11 detects the SI/O being driven below the V_{IL} level, its internal timing circuits begin to run.

The duration of each bit frame is allowed to vary from bit to bit as long as the variation does not cause the t_{BIT} length to exceed the specified minimum and maximum values (see AT21CS01/11 AC Characteristics). The t_{BIT} requirements will vary depending on whether the device is set for Low-Speed or High-Speed mode. For more information about setting the speed of the device, refer to Setting the Device Speed.

3.1.3.1 Data Input Bit Frames

A data input bit frame can be used by the master to transmit either a logic '0' or logic '1' data bit to the AT21CS01/11. The input bit frame is initiated when the master drives the SI/O line low. The length of time that the SI/O line is held low will dictate whether the master is transmitting a logic '0' or a logic '1' for that bit frame. For a logic '0' input, the length of time that the SI/O line must be held low is defined as t_{LOW0}. Similarly, for a logic '1' input, the length of time that the SI/O line must be held low is defined as t_{LOW1}.

The AT21CS01/11 will sample the state of the SI/O line after the maximum t_{LOW1} but prior to the minimum t_{LOW0} after SI/O was driven below the V_{IL} threshold to determine if the data input is a logic '0' or a logic '1'. If the master is still driving the line low at the sample time, the AT21CS01/11 will decode that bit frame as a logic '0' as SI/O will be at a voltage less than V_{IL}. If the master has already released the SI/O line, the AT21CS01/11 will see a voltage level greater than or equal to V_{IH} because of the external pull-up resistor, and that bit frame will be decoded as a logic '1'. The timing requirements for these parameters can be found in AT21CS01/11 AC Characteristics.

A logic '0' condition has multiple uses in the I^2C emulation sequences. It is used to signify a '0' data bit, and it also is used for an Acknowledge (ACK) response. Additionally, a logic '1' condition is also is used for a No Acknowledge (NACK) response in addition to the nominal '1' data bit.

Figure 3-2 and Figure 3-3 depict the logic '0' and logic '1' input bit frames.

Figure 3-2. Logic 0 Input Condition Waveform

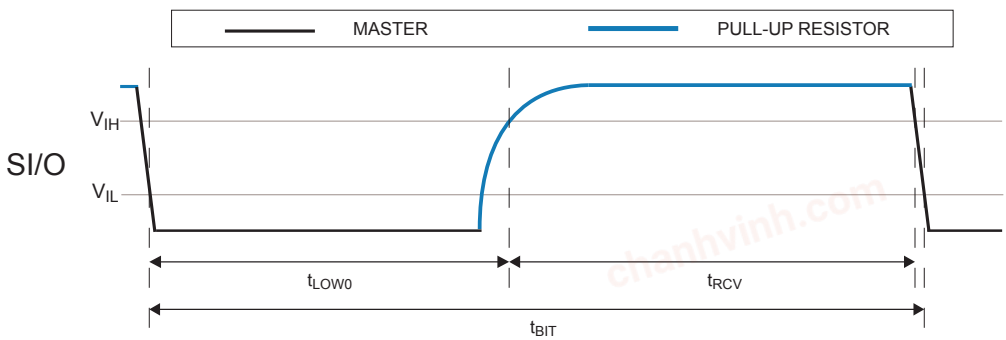

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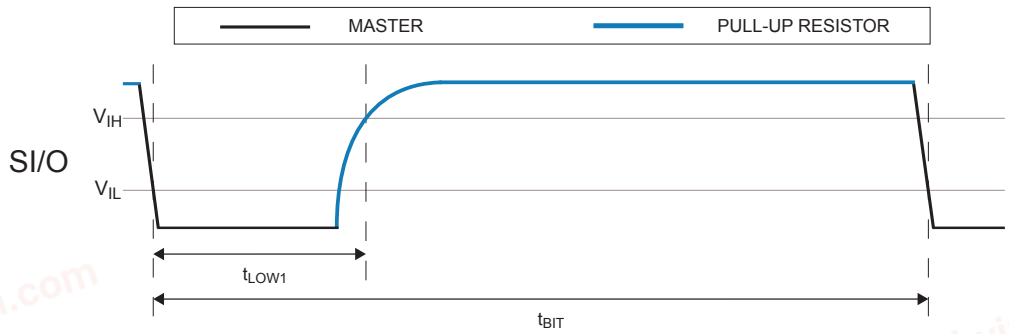
Figure 3-3. Logic 1 Input Condition Waveform



3.1.3.2 Start/Stop Condition

All transactions to the AT21CS01/11 begin with a Start condition; therefore, a Start can only be transmitted by the master to the slave. Likewise, all transactions are terminated with a Stop condition and thus a Stop condition can only be transmitted by the master to the slave.

The Start and Stop conditions require identical biasing of the SI/O line. The Start/Stop condition is created by holding the SI/O line at a voltage of V_{PUP} for a duration of t_{HTSS}. Refer to AT21CS01/11 AC Characteristics for timing minimums and maximums.

Figure 3-4 and Figure 3-5 depict the Start and Stop conditions.

Figure 3-4. Start Condition Waveform

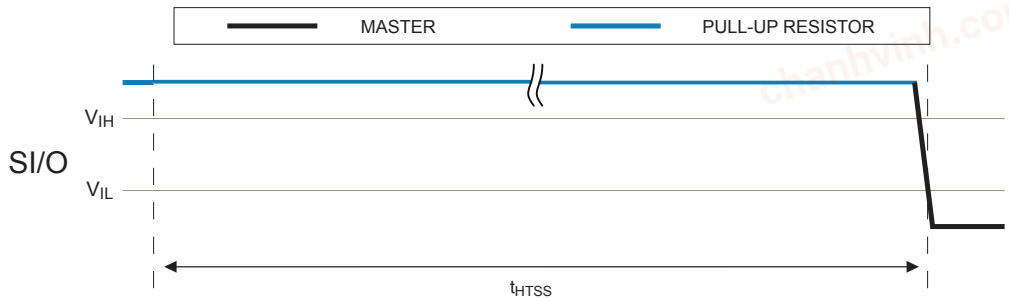
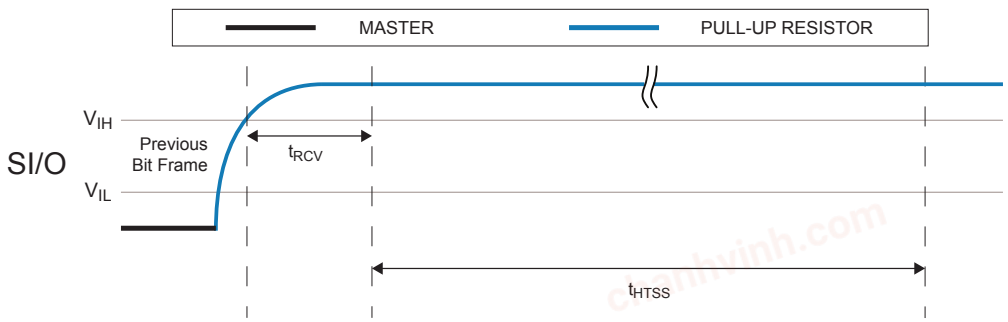


Figure 3-5. Stop Condition Waveform



3.1.3.3 Communication Interruptions

In the event that a protocol sequence is interrupted midstream, this sequence can be resumed at the point of interruption if the elapsed time of inactivity (where SI/O is idle) is less that the maximum t_{BIT} time. The maximum allowed value will differ if the device is High-Speed mode or Low-Speed mode (see Setting the Device Speed).

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Note: The interruption of protocol must not occur during a write sequence immediately after a logic '0' "ACK" response when sending data to be written to the device. In this case, the interruption will be interpreted as a Stop condition and will cause an internal write cycle to begin. The device will be busy for t_{WR} time and will not respond to any commands.

Note: For systems that cannot accurately monitor the location of interrupts, it is recommended to ensure that a minimum interruption time be observed consistent with the longest busy operation of the device (t_{WR}). Communicating with the device while it is in an internal write cycle by the master driving SI/O low could cause the byte(s) being written to become corrupted and must be avoided. The behavior of the device during a write cycle is described in more detail in Device Behavior During Internal Write Cycle.

If the sequence is interrupted for longer than the maximum t_{BIT}, the master must wait at least the minimum t_{HTSS} before continuing. By waiting the minimum t_{HTSS} time, a new Start condition is created and the device is ready to receive a new command. It is recommended that the master start over and repeat the transaction that was interrupted midstream.

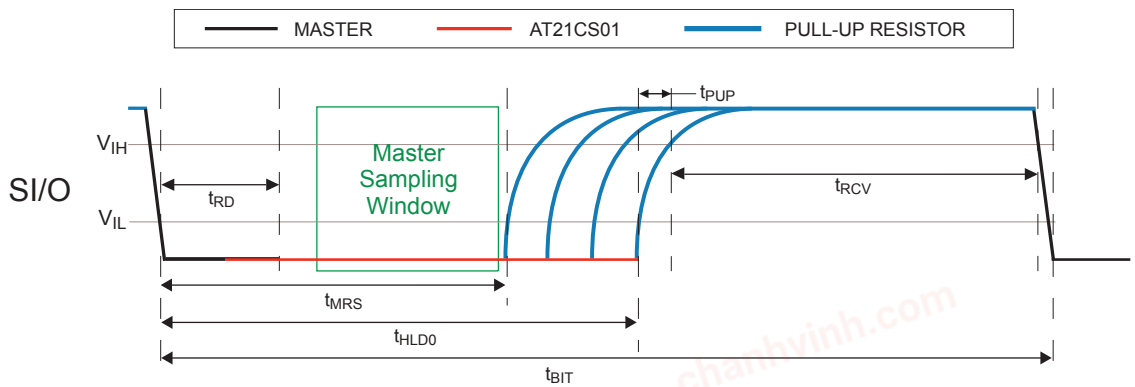
3.1.3.4 Data Output Bit Frame

A data output bit frame is used when the master is to receive communication back from the AT21CS01/11. Data output bit frames are used when reading any data out as well as any ACK or NACK responses from the device. Just as in the input bit frame, the master initiates the sequence by driving the SI/O line below the V_{IL} threshold which engages the AT21CS01/11 internal timing generation circuit.

Within the output bit frame is the critical timing parameter t_{RD}, which is defined as the amount of time the master must continue to drive the SI/O line low after crossing the below V_{IL} threshold to request a data bit back from the AT21CS01/11. Once the t_{RD} duration has expired, the master must release the SI/O line.

If the AT21CS01/11 is responding with a logic '0' (for either a '0' data bit or an ACK response), it will begin to pull the SI/O line low concurrently during the t_{RD} window and continue to hold it low for a duration of t_{HLD0}, after which it will release the line to be pulled back up to V_{PUP} (see Figure 3-6). Thus, when the master samples SI/O within the t_{MRS} window, it will see a voltage less than V_{IL} and decode this event as a logic '0'. By definition, the t_{HLD0} time is longer than the t_{MRS} time and therefore, the master is ensured to sample while the AT21CS01/11 is still driving the SI/O line low.

Figure 3-6. Logic 0 Data Output Bit Frame Waveform



If the AT21CS01/11 intends to respond with a logic '1' (for either a '1' data bit or a NACK response), it will not drive the SI/O line low at all. Once the master releases the SI/O line after the maximum t_{RD} has elapsed, the line will be pulled up to V_{PUP}. Thus, when the master samples the SI/O line within the t_{MRS} window, it will detect a voltage greater than V_{IH} and decode this event as a logic '1'.

The data output bit frame is shown in greater detail below in Figure 3-7.

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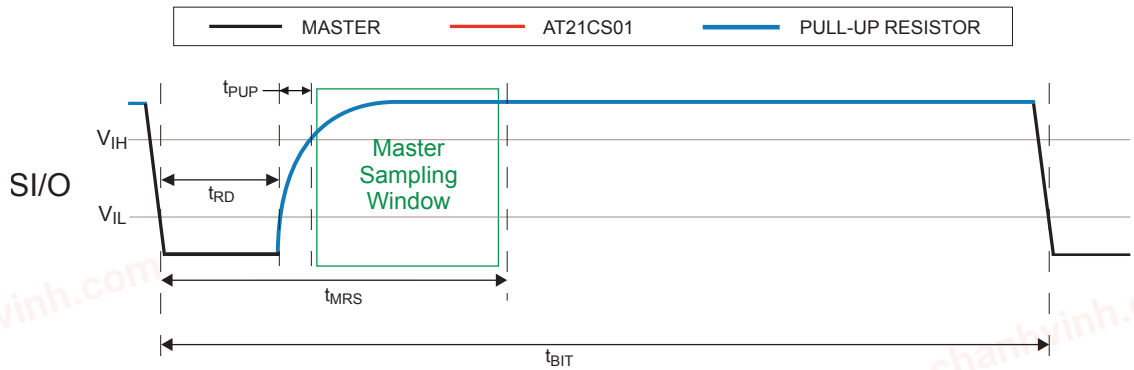
Figure 3-7. Logic 1 Data Output Bit Frame Waveform



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4. Device Addressing and I²C Protocol Emulation

Accessing the device requires a Start condition followed by an 8-bit device address word.

The AT21CS01/11 protocol sequence emulates what would be required for an I²C Serial EEPROM, with the exception that the beginning four bits of the device address are used as an opcode for the different commands and actions that the device can perform.

Since multiple slave devices can reside on the bus, each slave device must have its own unique address so that the master can access each device independently. After the 4-bit opcode, the following three bits of the device address byte are comprised of the slave address bits. The three slave address bits are preprogrammed prior to shipment and are read-only. Obtaining devices with different slave address bit values is done by purchasing a specific ordering code. Refer to Packaging Information for explanation of which ordering code corresponds with a specific slave address value.

Following the three slave address bits is a Read/$\overline{\text{Write}}$ select bit where a logic '1' indicates a read and a logic '0' indicates a write. Upon the successful comparison of the device address, the EEPROM will return an ACK (logic '0'). If the 4-bit opcode is invalid or the three bits of slave address do not match what is preprogrammed in the device, the device will not respond on the SI/O line and will return to a Standby state.

Table 4-1. Device Address Byte

4-bit Opcode				Preprogrammed Slave Address Bits			Read/$\overline{\text{Write}}$
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Refer to Available Opcodes				A2	A1	A0	R/$\overline{\text{W}}$

Following the device address byte, a memory address byte must be transmitted to the device immediately. The memory address byte contains a 7-bit memory array address to specify which location in the EEPROM to start reading or writing. Refer to Table 4-2 to review these bit positions.

Table 4-2. Memory Address Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Don't Care	A6	A5	A4	A3	A2	A1	A0

4.1 Memory Organization

The AT21CS01/11 internal memory array is partitioned into two regions. The main 1-Kbit EEPROM is organized as 16 pages of eight bytes each. The Security register is 256 bits in length, organized as four pages of eight bytes each. The lower two pages of the Security register are read-only and have a factory-programmed, 64-bit serial number that is unique across all AT21CS series Serial EEPROMs. The upper two pages of the Security register are user-programmable and can be subsequently locked (see Locking the Security Register).

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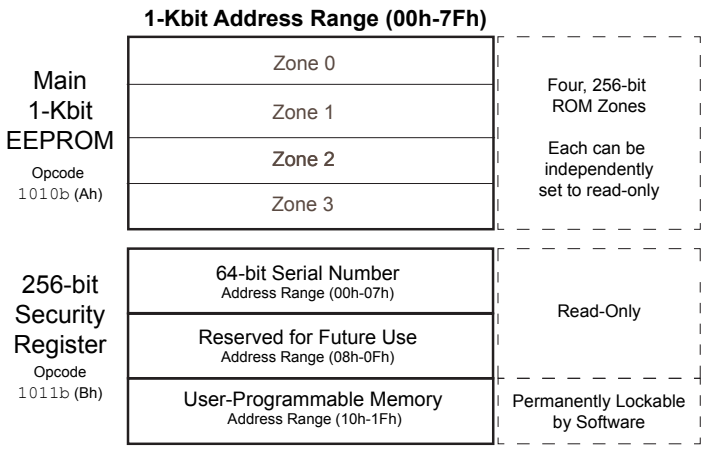
Figure 4-1. Memory Architecture Diagram



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5. Available Opcodes

Table 5-1 outlines available opcodes for the AT21CS01/11.

Table 5-1. Opcodes used by the AT21CS01/11

Command	4-Bit Opcode	Brief Description of Functionality
EEPROM Access	1010 (Ah)	Read/Write the contents of the main memory array.
Security Register Access	1011 (Bh)	Read/Write the contents of the Security register.
Lock Security Register	0010 (2h)	Permanently lock the contents of the Security register.
ROM Zone Register Access	0111 (7h)	Inhibit further modification to a zone of the EEPROM array.
Freeze ROM Zone State	0001 (1h)	Permanently lock the current state of the ROM Zone registers.
Manufacturer ID Read	1100 (Ch)	Query manufacturer and density of device.
Standard Speed Mode	1101 (Dh)	Switch to Standard Speed mode operation (AT21CS01 only command, the AT21CS11 will NACK this command).
High-Speed Mode	1110 (Eh)	Switch to High-Speed mode operation (AT21CS01/11 power-on default. AT21CS11 will ACK this command).

5.1 EEPROM Access (Opcode Ah)

The opcode Ah is used to read data from and write data to the EEPROM. Refer to Read Operations for more details about reading data from the device. For details about writing to the EEPROM, refer to Write Operations.

5.2 Security Register Access (Opcode Bh)

The opcode Bh is used to read data from and write data to the Security register. Refer to Read Operations in the Security Register for more details about reading data from the Security register. For details about writing to the user-programmable portion of the Security register, refer to section Writing to the Security Register.

5.3 Lock Security Register (Opcode 2h)

The opcode 2h is used to permanently lock the user-programmable portion of the Security register. Refer to Locking the Security Register.

5.4 ROM Zone Register Access (Opcode 7h)

The AT21CS01/11 is partitioned into four, 256-bit zones, each of which can be independently and permanently made read-only (ROM). The state of each zone is stored in a Configuration register which can be read from or written to using the opcode 7h. The ROM Zone functionality is explained in greater detail in ROM Zones.

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5.5 Freeze ROM Zone State (Opcode 1h)

The opcode 1h is used to permanently freeze the current state of the ROM Zone registers. Once set, the ROM Zone registers are read-only.

Therefore, any zone that is not already read-only cannot be subsequently converted to ROM. Refer to Freeze ROM Zone Registers for additional details.

5.6 Manufacturer ID Read (Opcode Ch)

Manufacturer identification, device density, and device revision information can be read from the device using the opcode Ch. The full details of the format of the data returned by this command are found in Manufacturer ID Read.

5.7 Standard Speed Mode (Opcode Dh)

The AT21CS01 can be set to Standard Speed mode or checked to see whether or not it is in Standard Speed mode with the use of the Dh opcode. Further details are covered in Standard Speed Mode (AT21CS01). The AT21CS11 does not offer Standard Speed mode and therefore will NACK this command.

5.8 High-Speed Mode (Opcode Eh)

The AT21CS01 can be set to High-Speed mode or checked to see whether or not it is in High-Speed mode with the use of the Eh opcode. The AT21CS11 only operates in High-Speed mode and therefore will ACK this command. Further details are covered in High-Speed Mode.

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6. Write Operations

All write operations for the AT21CS01/11 begin with the master sending a Start condition, followed by a device address byte (opcode Ah for the EEPROM and opcode Bh for the Security register) with the R/$\overline{W}$ bit set to '0' followed by the memory address byte. Next, the data value(s) to be written to the device are sent. Data values must be sent in 8-bit increments to the device followed by a Stop condition. If a Stop condition is sent somewhere other than at the byte boundary, the current write operation will be aborted.

The AT21CS01/11 allows single byte writes, partial page writes, and full page writes.

6.1 Device Behavior During Internal Write Cycle

To ensure that the address and data sent to the device for writing are not corrupted while any type of internal write operation is in progress, commands sent to the device are blocked from being recognized until the internal operation is completed. If a write interruption occurs (SI/O pulsed low) and is small enough to not deplete the internal power storage, the device will NACK signaling that the operation is in progress. If an interruption is longer than t_{DSCHG} then internal write operation will be terminated and may result in data corruption.

6.2 Byte Write

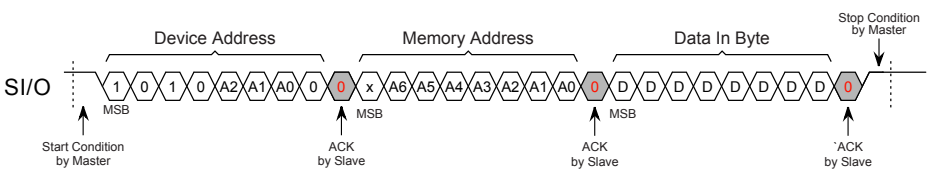
The AT21CS01/11 supports writing of a single 8-bit byte and requires a 7-bit memory word address to select which byte to write.

Upon receipt of the proper device address byte (with opcode of Ah) and memory address byte, the EEPROM will send a logic '0' to signify an ACK. The device will then be ready to receive the data byte. Following receipt of the complete 8-bit data byte, the EEPROM will respond with an ACK. A Stop condition must then occur; however, since a Stop condition is defined as a null bit frame with SI/O pulled high, the master does not need to drive the SI/O line to accomplish this. If a Stop condition is sent at any other time, the write operation is aborted. After the Stop condition is complete, the EEPROM will enter an internally self-timed write cycle, which will complete within a time of t_{WR}, while the data is being programmed into the nonvolatile EEPROM. The SI/O pin must be pulled high via the external pull-up resistor during the entire t_{WR} cycle. After the maximum t_{WR} time has elapsed, the master may begin a new bus transaction.

Note:

1. Any attempt to interrupt the internal write cycle by driving the SI/O line low may cause the byte being programmed to be corrupted. Other memory locations within the memory array will not be affected. Note Device Behavior During Internal Write Cycle for the behavior of the device while the write cycle is in progress. If the master must interrupt a write operation, the SI/O line must be driven low for t_{DSCHG} as noted in Interrupting the Device during an Active Operation.

Figure 6-1. Byte Write



Note:

1. x = Don't Care bit in the place of A7 as this bit falls outside the 1-Kbit addressable range.

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6.3 Page Write

A page write operation allows up to eight bytes to be written in the same write cycle, provided all bytes are in the same row (address bits A6 through A3 are the same) of the memory array. Partial page writes of less than eight bytes are allowed.

A page write is initiated the same way as a byte write, but the bus master does not send a Stop condition after the first data byte is clocked in. Instead, after the EEPROM acknowledges receipt of the first data byte, the bus master can transmit up to an additional seven data bytes.

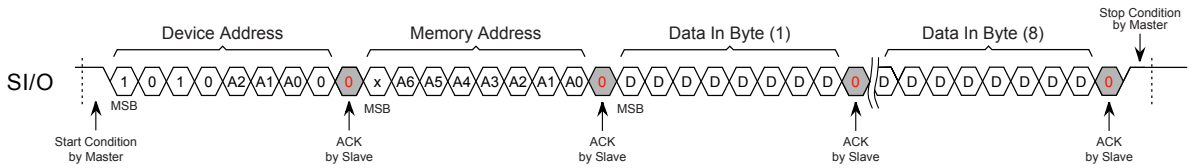
The EEPROM will respond with an ACK after each data byte is received. Once all data bytes have been sent, the device requires a Stop condition to begin the write cycle. However, since a Stop condition is defined as a null bit frame with SI/O pulled high, the master does not need to drive the SI/O line to accomplish this. If a Stop condition is sent at any other time, the write operation is aborted. After the Stop condition is complete, the internally self-timed write cycle will begin.The SI/O pin must be pulled high via the external pull-up resistor during the entire t_{WR} cycle. Thus, in a multi-slave environment, communication to other single-wire devices on the bus should not be attempted while any devices are in an internal write cycle.

The lower three bits of the memory address are internally incremented following the receipt of each data byte. The higher order address bits are not incremented, and the device retains the memory page location. Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. When the incremented word address reaches the page boundary, the address counter will “roll over” to the beginning of the same page. Nevertheless, creating a roll over event should be avoided as previously loaded data in the page could become unintentionally altered. After the maximum t_{WR} time has elapsed, the master may begin a new bus transaction.

Note:

1. Any attempt to interrupt the internal write cycle by driving the SI/O line low may cause the bytes being programmed to be corrupted. Other memory locations within the memory array will not be affected. Note Device Behavior During Internal Write Cycle for the behavior of the device while the write cycle is in progress. If the master must interrupt a write operation, the SI/O line must be driven low for t_{DSCHG} as noted in Interrupting the Device during an Active Operation.

Figure 6-2. Page Write



Note:

1. x = Don’t Care bit in the place of A7 as this bit falls outside the 1-Kbit addressable range.

6.4 Writing to the Security Register

The Security register supports bytes writes, page writes, and partial page writes in the upper 16 bytes (upper two pages of eight bytes each) of the region. Page writes and partial page writes in the Security register have the same page boundary restrictions and behavior requirements as they do in the EEPROM.

Upon receipt of the proper device address byte (with opcode of Bh specified) and memory address byte, the EEPROM will send a logic ‘0’ to signify an ACK. The device will then be ready to receive the first data byte.

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Following receipt of the data byte, the EEPROM will respond with an ACK and the master can send up to an additional seven bytes if desired. The EEPROM will respond with an ACK after each data byte is successfully received. Once all of the data bytes have been sent, the device requires a Stop condition to begin the write cycle. However, since a Stop condition is defined as a null bit frame with SI/O pulled high, the master does not need to drive the SI/O line to accomplish this. After the Stop condition is complete, the EEPROM will enter an internally self-timed write cycle, which will complete within a time of t_{WR}, while the data is being programmed into the nonvolatile EEPROM. The SI/O pin must be pulled high via the external pull-up resistor during the entire t_{WR} cycle. Figure 6-3 is included below as an example of a byte write operation in the Security register.

Figure 6-3. Byte Write in the Security Register



Note:

1. x = Don't Care values in the place of A7-A5 as these bits falls outside the addressable range of the Security register.
2. Any attempt to interrupt the internal write cycle by driving the SI/O line low may cause the byte being programmed to be corrupted. Other memory locations within the memory array will not be affected. Note Device Behavior During Internal Write Cycle for the behavior of the device while the write cycle is in progress. If the master must interrupt a write operation, the SI/O line must be driven low for t_{DSCHG} as noted in Interrupting the Device during an Active Operation.

6.5 Locking the Security Register

The Lock command is an irreversible sequence that will permanently prevent all future writing to the upper 16 bytes of the Security register on the AT21CS01/11. Once the Lock command has been executed, the entire 32-byte Security register becomes read-only. Once the Security register has been locked, *it is not possible to unlock it*.

The Lock command protocol emulates a byte write operation to the Security register, however, the opcode 0010b (2h) is required along with the A7 through A4 bits of the memory address being set to 0110b (6h). The remaining bits of the memory address, as well as the data byte are "don't care" bits. Even though these bits are "don't cares", they still must be transmitted to the device. An ACK response to the memory address and data byte indicates the Security register is not currently locked. A NACK response indicates the Security register is already locked. Refer to Figure 6-5 for details about determining the Lock status of the Security register.

The sequence completes with a Stop condition to initiate a self-timed internal write cycle. If a Stop condition is sent at any other time, the Lock operation is aborted. Since a Stop condition is defined as a null bit frame with SI/O pulled high, the master does not need to drive the SI/O line to accomplish this. Upon completion of the write cycle, (taking a time of t_{WR}), the Lock operation is complete and the Security register will become permanently read-only.

Note:

1. Any attempt to drive the SI/O line low during the t_{WR} time period may cause the Lock operation to not complete successfully, and must be avoided.

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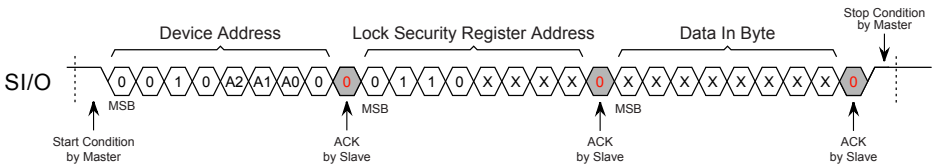
Figure 6-4. Lock Command



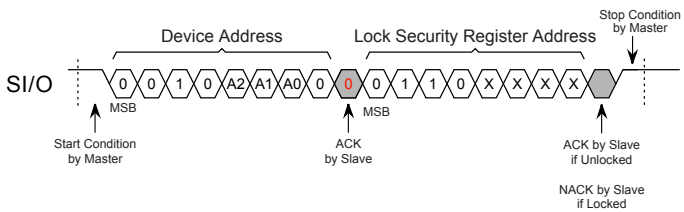
6.5.1 Device Response to a Write Command on a Locked Device

A locked device will respond differently to a Write command to the Security register compared to a device that has not been locked. Writing to the Security register is accomplished by sending a Start condition followed by a device address byte with the opcode of 1011b (Bh), the appropriate slave address combination, and the Read/$\overline{\text{Write}}$ bit set as a logic '0'. Both a locked device and a device that has not been locked will return an ACK. Next, the 8-bit word address is sent and again, both devices will return an ACK. However, upon sending the data input byte, a device that has already been locked will return a NACK and be immediately ready to accept a new command, whereas a device that has not been locked will return an ACK to the data input byte as per normal operation for a Write command as described in Write Operations.

6.5.2 Check Lock Command

The Check Lock command follows the same sequence as the Lock command (including 0110b in the A7 through A4 bits of the memory address byte) with the exception that only the device address byte and memory address byte need to be transmitted to the device. An ACK response to the memory address byte indicates that the lock has not been set while a NACK response indicates that the lock has been set. If the lock has already been enabled, it cannot be reversed. The Check Lock command is completed by the master sending a Stop bit to the device (defined as a null bit frame).

Figure 6-5. Check Lock Command



6.6 Setting the Device Speed

The AT21CS01 can be set to Standard Speed mode (15.4 kbps maximum) or High-Speed mode (125 kbps maximum) through a software sequence. Upon executing a Reset and Discovery Response sequence (see Device Reset/Power-up and Discovery Response), the device will default to High-Speed mode. The AT21CS11 does not have Standard Speed mode.

6.6.1 Standard Speed Mode (AT21CS01)

The AT21CS01 can be set to Standard Speed mode or checked to see whether or not it is in Standard Speed mode with the use of the Dh opcode. This transaction only requires eight bits.

To set the device to Standard Speed mode, the master must send a Start condition, followed by the device address byte with the opcode of 1101b (Dh) specified, along with the appropriate slave address combination and the Read/$\overline{\text{Write}}$ bit set to a logic '0'. The device will return an ACK (logic '0') and will be immediately ready to receive commands for standard speed operation.

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To determine if the device is already set to Standard Speed mode, the device address byte with the opcode of 1101b (Dh) must be sent to the device, along with the appropriate slave address combination and the Read/$\overline{\text{Write}}$ bit set to a logic '1'. The device will return an ACK (logic '0') if it was set for Standard Speed mode. It will return a NACK (logic '1') if the device was not currently set for Standard Speed mode.

Note: The AT21CS11 will NACK this command.

6.6.2 High-Speed Mode

The device can be set to High-Speed mode or checked to see whether or not it is in High-Speed mode with the use of the Eh opcode. This transaction only requires eight bits. The power-on default for the AT21CS01/11 is High-Speed mode.

To set the device to High-Speed mode, the master must send a Start condition, followed by the device address byte with the opcode of 1110b (Eh) specified, along the appropriate slave address combination and the Read/$\overline{\text{Write}}$ bit set to a logic '0'. The device will return an ACK (Logic 0) and will be immediately ready to receive commands for high-speed operation.

To determine if the device is already set to High-Speed mode, the device address byte with the opcode of 1110b (Eh) specified must be sent to the device along with the appropriate slave address combination and the Read/$\overline{\text{Write}}$ bit set to a logic '1'. The device will return an ACK (logic '0') if it was set for High-Speed mode. It will return a NACK (logic '1') if the device was not currently set for High-Speed mode.

Note: The AT21CS11 will ACK this command.

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7. Read Operations

Read operations are initiated in a similar way as write operations with the exception that the Read/$\overline{\text{Write}}$ select bit in the device address byte must be set to a logic '1'. There are multiple read operations supported by the device:

- Current Address Read within the EEPROM
- Random Read within the EEPROM
- Sequential Read within the EEPROM
- Read from the Security Register
- Manufacturer ID Read

Note:

1. The AT21CS01/11 contains a single, shared-memory Address Pointer that maintains the address of the next byte in the EEPROM or Security register to be accessed. For example, if the last byte read or written was memory location 0Dh of the EEPROM, then the Address Pointer will be pointing to memory location 0Eh of the EEPROM. As such, when changing from a read in one region to the other, the first read operation in the new region should begin with a random read instead of a current address read to ensure the Address Pointer is set to a known value within the desired region.

If the end of the EEPROM or the Security register is reached, then the Address Pointer will "roll over" back to the beginning (address 00h) of that region. The Address Pointer retains its value between operations as long as the pull-up voltage on the SI/O pin is maintained or as long as the device has not been reset.

7.1 Current Address Read within the EEPROM

The internal Address Pointer must be pointing to a memory location within the EEPROM in order to perform a current address read from the EEPROM. To initiate the operation, the master must send a Start condition, followed by the device address byte with the opcode of 1010b (Ah) specified, along with the appropriate slave address combination and the Read/$\overline{\text{Write}}$ bit set to a logic '1'. After the device address byte has been sent, the AT21CS01/11 will return an ACK (logic '0').

Following the ACK, the device is ready to output one byte (eight bits) of data. The master initiates the all bits of data by driving the SI/O line low to start. The AT21CS01/11 will hold the line low after the master releases it to indicate a logic '0'. If the data is logic '1', the AT21CS01/11 will not hold the SI/O line low at all, causing it to be pulled high by the pull-up resistor once the master releases it. This sequence repeats for eight bits.

After the master has read the first data byte and no further data is desired, the master must return a NACK (logic '1') response to end the read operation and return the device to the Standby mode. Figure 7-1 depicts this sequence.

If the master would like the subsequent byte, it would return an ACK (logic '0') and the device will be ready output the next byte in the memory array. Refer to Sequential Read within the EEPROM for details about continuing to read beyond one byte.

Note:

1. If the last operation to the device was an access to the Security register, then a random read should be performed to ensure that the Address Pointer is set to a known memory location within the EEPROM.

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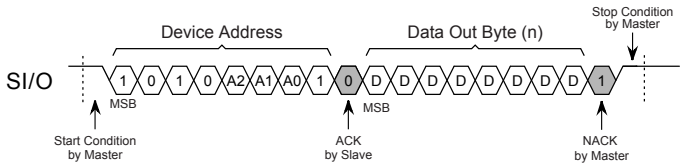
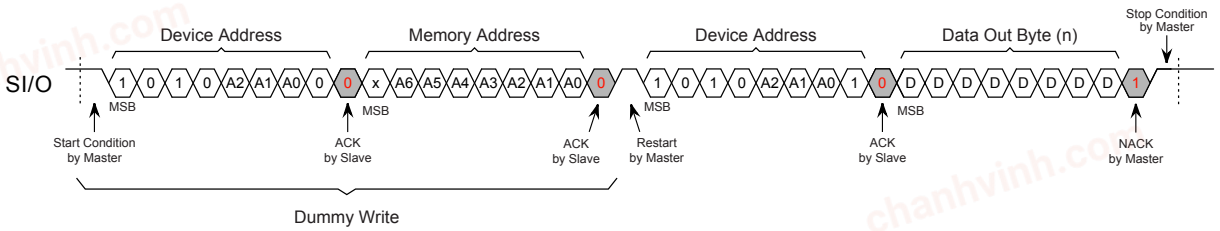
Figure 7-1. Current Address Read



7.2 Random Read within the EEPROM

A random read begins in the same way as a byte write operation which will load a new EEPROM memory address into the Address Pointer. However, instead of sending the data byte and Stop condition of the byte write, a repeated Start condition is sent to the device. This sequence is referred to as a “dummy write”. After the device address and memory address bytes of the “dummy write” have been sent, the AT21CS01/11 will return an ACK response. The master can then initiate a current address read, beginning with a new Start condition, to read data from the EEPROM. Refer to Current Address Read within the EEPROM for details on how to perform a current address read.

Figure 7-2. Random Read



7.3 Sequential Read within the EEPROM

Sequential reads start as either a current address read or as a random read. However, instead of the master sending a NACK (logic ‘1’) response to end a read operation after a single byte of data has been read, the master sends an ACK (logic ‘0’) to instruct the AT21CS01/11 to output another byte of data. As long as the device receives an ACK from the master after each byte of data has been output, it will continue to increment the address counter and output the next byte data from the EEPROM. If the end of the EEPROM is reached, then the Address Pointer will “roll over” back to the beginning (address 00h) of the EEPROM region. To end the sequential read operation, the master must send a NACK response after the device has output a complete byte of data. After the device receives the NACK, it will end the read operation and return to the Standby mode.

Note:

1. If the last operation to the device accessed the Security register, then a random read should be performed to ensure that the Address Pointer is set to a known memory location within the EEPROM.

Figure 7-3. Sequential Read from a Current Address Read

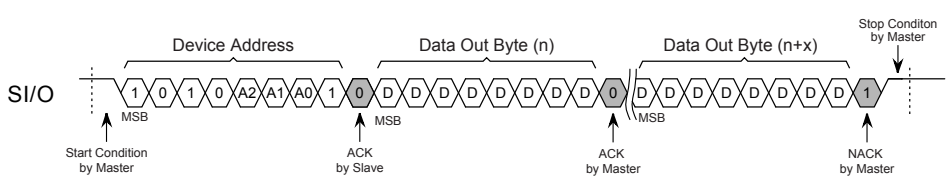


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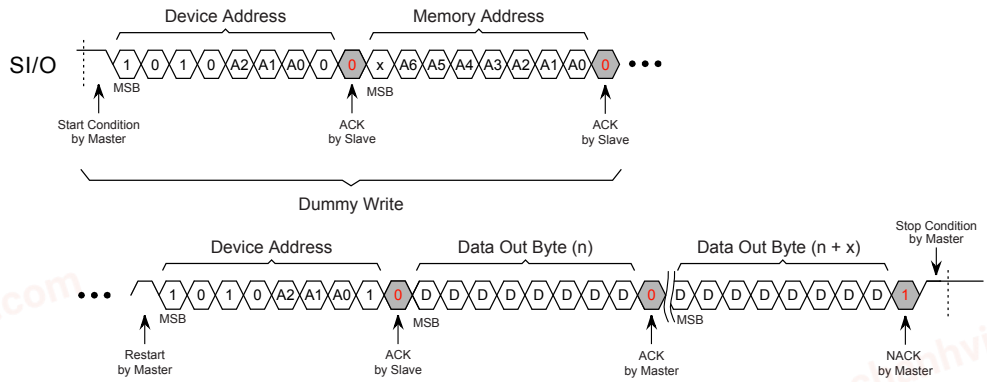
Figure 7-4. Sequential Read from a Random Read



7.4 Read Operations in the Security Register

The Security register can be read by using either a random read or a sequential read operation. Due to the fact that the EEPROM and Security register share a single Address Pointer register, a “dummy write” must be performed to correctly set the Address Pointer in the Security register. This is why a random read or sequential read must be used as these sequences include a “dummy write.” Bits A7 through A5 are "don’t care" bits as these fall outside the addressable range of the Security register. Current address reads of the Security register are not supported.

In order to read the Security register, the device address byte must be specified with the opcode `1011b` (Bh) instead of the opcode `1010b` (Ah).The Security register can be read to read the 64-bit serial number or the remaining user-programmable data.

7.4.1 Serial Number Read

The lower eight bytes of the Security register contain a factory-programmed, unique, 64-bit serial number. In order to ensure a unique value, the entire 64-bit serial number must be read starting at Security register address location 00h. Therefore, it is recommended that a sequential read started with a random read operation be used, ensuring that the random read sequence uses a device address byte with opcode `1011b` (Bh) specified in addition to the memory address byte being set to 00h.

The first byte read out of the 64-bit serial number is the product identifier (A0h). Following the product identifier, a 48-bit unique number is contained in bytes 1 through 6. The last byte of the serial number contains a cyclic redundancy check (CRC) of the other 56 bits. The CRC is generated using the polynomial $X^8 + X^5 + X^4 + 1$. The structure of the 64-bit serial number is depicted in Table 7-1.

Table 7-1. 64-Bit Factory-Programmed Serial Number Organization

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
8-bit Product Identifier (A0h)	48-bit Unique Number						8-bit CRC Value

After all eight bytes of the serial number have been read, the master can return a NACK (logic ‘`1`’) response to end the read operation and return the device to the Standby mode. If the master sends an ACK (logic ‘`0`’) instead of a NACK, then the next byte (address location 08h) in the Security register will be output. If the end of the Security register is reached, then the Address Pointer will “roll over” back to the beginning (address location 00h) of the Security register.

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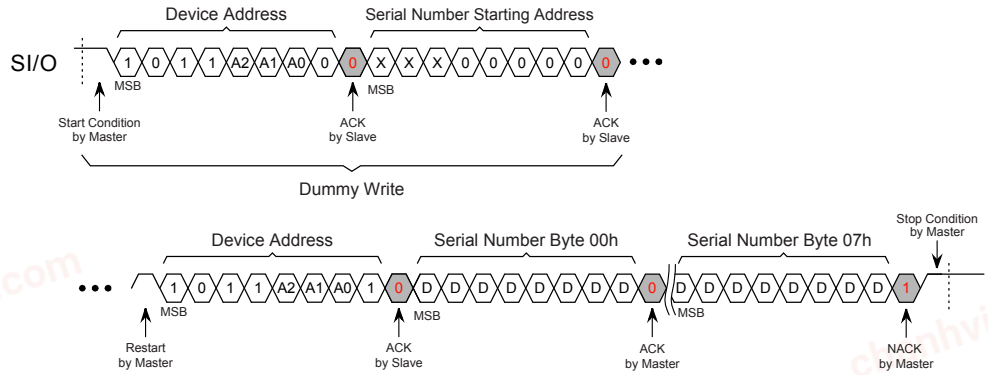
Figure 7-5. Serial Number Read



7.5 Manufacturer ID Read

The AT21CS01/11 offers the ability to query the device for manufacturer, density, and revision information. By using a specific opcode and following the format of a current address read, the device will return a 24-bit value that corresponds with the I^2C identifier value reserved for Microchip, along with further data to signify a 1-Kbit density and the device revision.

To read the Manufacturer ID data, the master must send a Start condition, followed by the device address byte with the opcode of `1100b` (Ch) specified, along the appropriate slave address combination and the Read/$\overline{\text{Write}}$ bit set to a logic '`1`'. After the device address byte has been sent, the AT21CS01/11 will return an ACK (logic '`0`'). If the Read/$\overline{\text{Write}}$ bit is set to a logic '`0`' to indicate a write, the device will NACK (logic '`1`') since the Manufacturer ID data is read-only.

After the device has returned an ACK, it will then send the first byte of Manufacturer ID data which contains the eight Most Significant bits (D23-D16) of the 24-bit data value. The master can then return an ACK (logic '`0`') to indicate it successfully received the data, upon which the device will send the second byte (D15-D8) of Manufacturer ID data. The process repeats until all three bytes have been read out and the master sends a NACK (logic '`1`') to complete the sequence. Figure 7-6 depicts this sequence below. If the master ACKs (logic '`0`') the third byte, the Internal Pointer will roll over back to the first byte of Manufacturer ID data.

Figure 7-6. Manufacturer ID Read

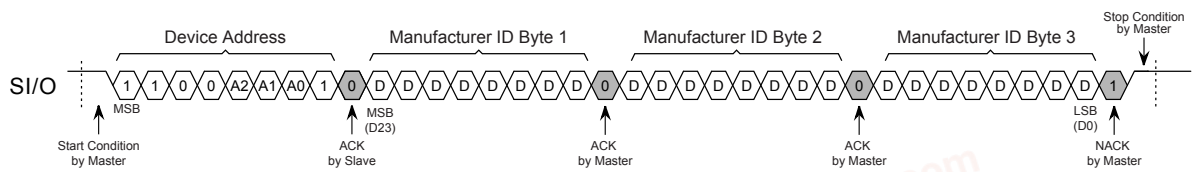


Table 7-2 below provides the format of the Manufacturer ID data.

Table 7-2. Manufacturer ID Data Format

Device	Manufacturer Code <D23:D12>	Device Code <D11:D3>	Revision Code <D2:D0>	Hex Value <D23:D0>
AT21CS01	0000-0000-1101	0010-0000-0	000	00D200h
AT21CS11	0000-0000-1101	0011-1000-0	000	00D380h

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The Manufacturer Identifier portion of the ID is returned in the 12 Most Significant bits of the three bytes read out. The value reserved for Microchip is 0000-0000-1101b (00Dh). Therefore, the first byte read out by the device will be 00h. The upper nibble of the second byte read out is Dh.

The Least Significant 12 bits of the 24-bit ID is comprised of a Microchip defined value that indicates the device density and revision. Bits D11 through D3 indicate the device code and bits D2 through D0 indicate the device revision. The output is shown more specifically in Table 7-2.

The overall 24-bit value returned by the AT21CS01 is 00D200h. The overall 24-bit value returned by the AT21CS11 is 00D380h.

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8. ROM Zones

8.1 ROM Zone Size and ROM Zone Registers

Certain applications require that portions of the EEPROM memory array be permanently protected against malicious attempts at altering program code, data modules, security information, or encryption/decryption algorithms, keys, and routines. To address these applications, the memory array is segmented into four different memory zones of 256 bits each. A ROM Zone mechanism has been incorporated that allows any combination of individual memory zones to be permanently locked so that they become read-only (ROM). Once a memory zone has been converted to ROM, it can never be erased or programmed again, and it can never be unlocked from the ROM state. Table 8-2 shows the address range of each of the four memory zones.

8.1.1 ROM Zone Registers

Each 256-bit memory zone has a corresponding single-bit ROM Zone register that is used to control the ROM status of that zone. These registers are nonvolatile and will retain their state even after a device power cycle or Reset operation. The following table outlines the two states of the ROM Zone registers. Each ROM Zone register has specific ROM Zone register address that is reserved for read or write access.

Table 8-1. ROM Zone Register Values

Value	ROM Zone Status
0	ROM Zone is not enabled and that memory zone can be programmed and erased (the default state).
1	ROM Zone is enabled and that memory zone can never be programmed or erased again.

Issuing the ROM Zone command to a particular ROM Zone register address will set the corresponding ROM Zone register to the logic '1' state. Each ROM Zone register can only be set once; therefore, once set to the logic '1' state, a ROM Zone cannot be reset back to the logic '0' state.

Table 8-2. ROM Zone Address Ranges

Memory Zone	Starting Memory Address	Ending Memory Address	ROM Zone Register Address
0	0h	1Fh	01h
1	20h	3Fh	02h
2	40h	5Fh	04h
3	60h	7Fh	08h

8.2 Programming and Reading the ROM Zone Registers

8.2.1 Reading the Status of a ROM Zone Register

To check the current status of a ROM Zone register, the master must emulate a random read sequence with the exception that the opcode 0111b (7h) will be used. The dummy write portion of the random read sequence is needed to specify which ROM Zone register address is to be read.

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This sequence begins by the master sending a Start condition, followed by a device address byte with the opcode of 7h in the four Most Significant bits, along with the appropriate slave address combination and the Read/$\overline{\text{Write}}$ bit set to a logic '0'. The AT21CS01/11 will respond with an ACK.

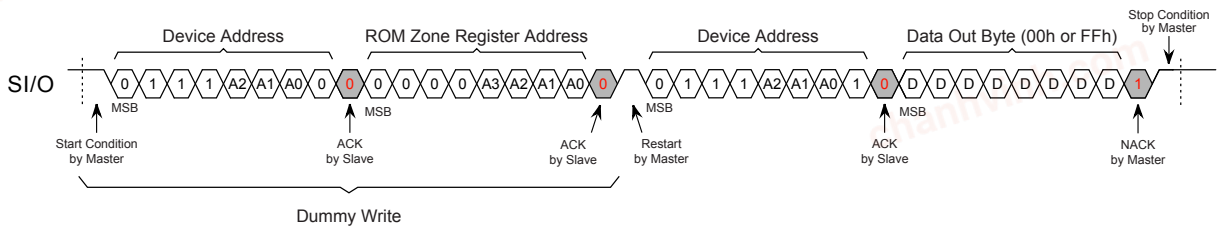
Following this device address byte is an 8-bit ROM Zone register address byte. The four Most Significant bits are not used and are therefore "don't care" bits. The address sent to the device must match one of the ROM Zone register addresses specified in Table 8-3. After the ROM Zone register address has been sent, the AT21CS01/11 will return an ACK (logic '0').

Then an additional Start condition is sent to the device with the same device address byte as before, but now with the Read/$\overline{\text{Write}}$ bit set to a logic '1', to which the device will return an ACK. After the AT21CS01/11 has sent the ACK, the device will output either 00h or FFh data byte. A 00h data byte indicates that the ROM Zone register is zero, meaning the zone has not been set as ROM. If the device outputs FFh data, then the memory zone has been set to ROM and cannot be altered.

Table 8-3. Read ROM Zone Register – Output Data

Output Data	ROM Zone Register Value
00h	ROM Zone register value is zero (zone is not set as ROM).
FFh	ROM Zone register value is one (zone is permanently set as ROM).

Figure 8-1. Reading the State of a ROM Zone Register



8.2.2 Writing to a ROM Zone Register

A ROM Zone register can only be written to a logic '1' which will set the corresponding memory zone to a ROM state. Once a ROM Zone register has been written, it can never be altered again.

To write to a ROM Zone register, the master must send a Start condition, followed by the device address byte with the opcode of 0111b (7h) specified, along with the appropriate slave address combination and the Read/$\overline{\text{Write}}$ bit set to a logic '0'. The device will return an ACK. After the device address byte has been sent, the AT21CS01/11 will return an ACK.

Following the device address byte is an 8-bit ROM Zone register address byte. The address sent to the device must match one of the ROM Zone register addresses specified in Table 8-2. After the ROM Zone register address has been sent, the AT21CS01/11 will return an ACK.

After the AT21CS01/11 has sent the ACK, the master must send an FFh data byte in order to set the appropriate ROM Zone register to the logic '1' state. The device will then return an ACK and, after a Stop condition is executed, the device will enter a self-time internal write cycle, lasting t_{WR}. If a Stop condition is sent at any other point in the sequence, the write operation to the ROM Zone register is aborted. The device will not respond till any commands until the t_{WR} time has completed. This sequence is depicted in Figure 8-2.

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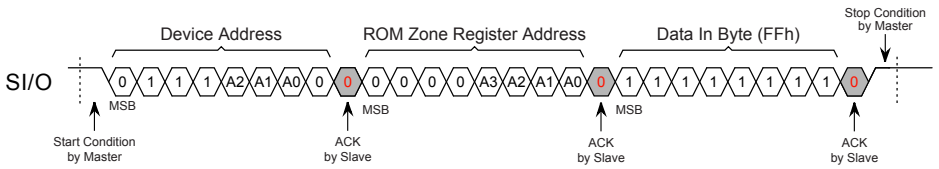
Figure 8-2. Writing to a ROM Zone Register



Note:

1. Any attempt to interrupt the internal write cycle by driving the SI/O line low may cause the register being programmed to become corrupted. Note Device Behavior During Internal Write Cycle for the behavior of the device while a write cycle is in progress. If the master must interrupt a write operation, the SI/O line must be driven low for t_{DSCHG} as noted in Interrupting the Device during an Active Operation.

8.2.3 Freeze ROM Zone Registers

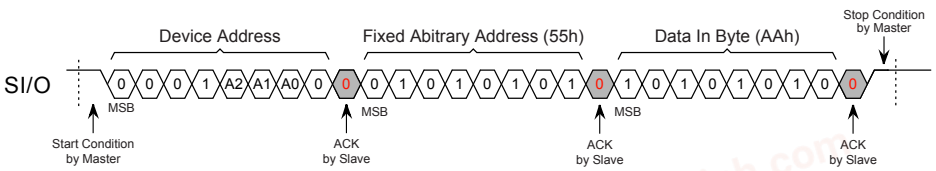
The current ROM Zone state can be frozen so that no further modifications to the ROM Zone registers can be made. Once frozen, this event cannot be reversed.

To freeze the state of the ROM Zone registers, the master must send a Start condition, followed by the device address byte with the opcode of 0001b (1h) specified, along with the appropriate slave address combination and the Read/$\overline{\text{Write}}$ bit set to a logic '0'. The device will return either an ACK (logic '0') response if the ROM Zone registers have not been previously frozen or a NACK (logic '1') response if the registers have already been frozen.

If the AT21CS01/11 returns an ACK, the master must send a fixed arbitrary address byte value of 55h, to which the device will return an ACK (logic '0'). Following the 55h address byte, a data byte of AAh must be sent by the master. The device will ACK after the AAh data byte. If an address byte other than 55h or a data byte other than AAh is sent, the device will NACK (logic '1') and the freeze operation will not be performed.

To complete the Freeze ROM Zone register sequence, a Stop condition is required. If a Stop condition is sent at any other point in this sequence, the operation is aborted. Since a Stop condition is defined as a null bit frame with SI/O pulled high, the master does not need to drive the SI/O line to accomplish this. After the Stop condition is complete, the internally self-timed write cycle will begin.The SI/O pin must be pulled high via the external pull-up resistor during the entire t_{WR} cycle.

Figure 8-3. Freezing the ROM Zone Registers



Note:

1. Any attempt to drive the SI/O line low during the t_{WR} time period may cause the Freeze operation to not complete successfully, and must be avoided.

8.3 Device Response to a Write Command Within an Enabled ROM Zone

The AT21CS01/11 will respond differently to a Write command in a memory zone that has been set to ROM compared to Write command in a memory zone that has not been set to ROM. Writing to the EEPROM is accomplished by sending a Start condition followed by a device address byte with the

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opcode of 1010b (Ah), the appropriate slave address combination, and the Read/$\overline{\text{Write}}$ bit set as a logic '0'. Since a memory address has not been input at this point in the sequence, the device returns an ACK. Next, the 8-bit word address is sent which will result in an ACK from the device, regardless if that address is in a memory zone that has been set to ROM. However, upon sending the data input byte, a Write command to an address that was in a memory zone that was set to ROM will result in a NACK response from the AT21CS01/11 and the device will be immediately ready to accept a new command. If the address being written was in a memory zone that had not been set to ROM, the device will return an ACK to the data input byte as per normal operation for write operations as described in Write Operations.

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9. Device Default Condition from Microchip

The AT21CS01/11 is delivered with the EEPROM array set to logic '1' state resulting in FFh data in all locations.

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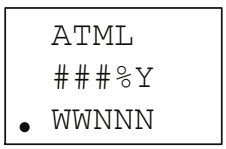
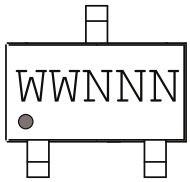
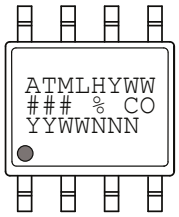
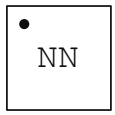
10. Packaging Information

10.1 Package Marking Information

AT21CS01/AT21CS11: Package Marking Information

2-ld XSFN	3-lead SOT-23
	
8-lead SOIC	**4-ball WLCSP**
	 (AT21CS01 only)

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT21CS01		Truncation Code ###: K1M	
AT21CS11		Truncation Code ###: K2	
Date Codes			**Slave Address**
Y = Year		M = Month	WW = Work Week of Assembly	% = Slave Address
7: 2017	1: 2021	A: January	02: Week 2	A: Address 000 E: Address 100
8: 2018	2: 2022	B: February	04: Week 4	B: Address 001 F: Address 101
9: 2019	3: 2023	...	...	C: Address 010 G: Address 110
0: 2020	4: 2024	L: December	52: Week 52	D: Address 011 H: Address 111
Country of Assembly		**Trace Code**		**Atmel Truncation**
CO = Country of Assembly		NNN or NN		AT: Atmel ATM: Atmel ATML: Atmel

9/11/17

	TITLE	DRAWING NO.	REV.
	AT21CS01/11SM, AT21CS01 and AT21CS11 Package Marking Information	21CS01/11SM	A

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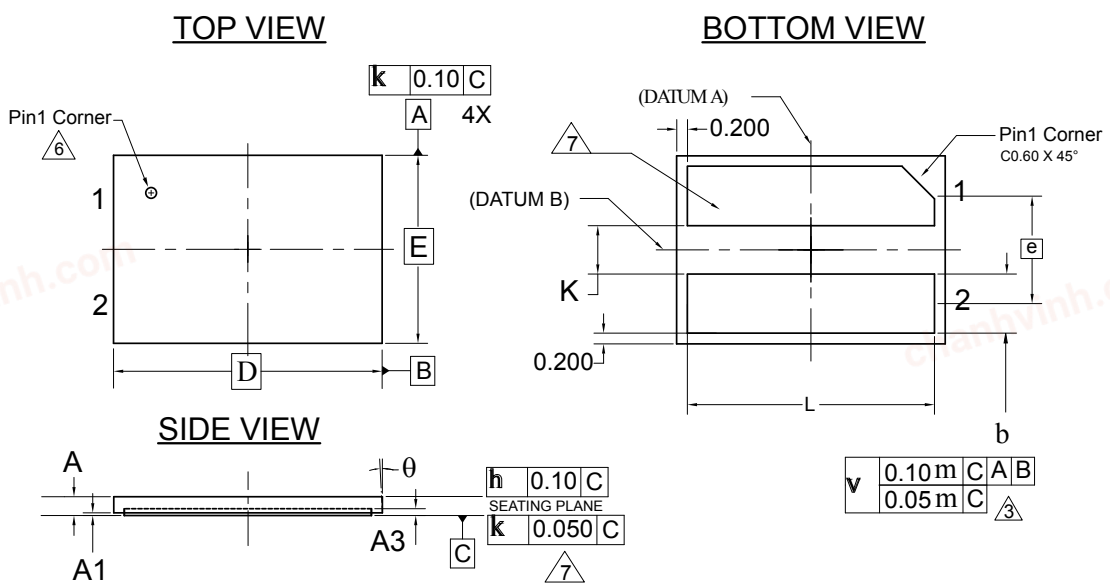

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5M - 1994.
2. All dimensions are in millimeters, 0 is in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension 'b' should not be measured in that radius area.
4. Maximum package warpage is 0.05mm.
5. Maximum allowable burrs is 0.076mm in all directions.
6. Pin #1 on top will be laser marked.
7. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.30	0.35	0.40	
A1	0.00	0.035	0.05	
A3		0.127 REF		
b	1.05	1.10	1.15	3
L	4.55	4.60	4.65	
D		5.00 BSC		
E		3.50 BSC		
e		2.00 BSC		
θ	0°	-	-	2
K		0.90 REF		

10/14/14

	TITLE	GPC	DRAWING NO.	REV.
	2MS-1, 2-pad 5.0x3.5 mm Body, 0.40 thick, Extra Thin Single Flat No Lead Package (XSFN)	YDR	2MS-1	B

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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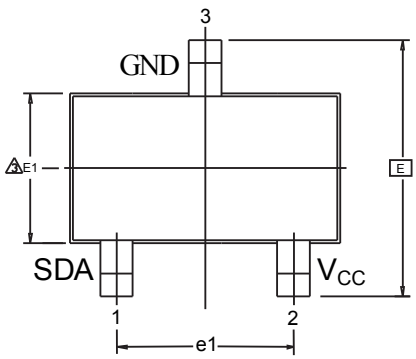
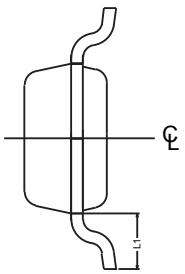
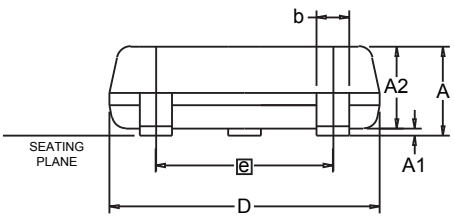


Top View



End View



Side View

Notes:
1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
2. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15mm from the lead tip.

This drawing is for general information only. Refer to JEDEC Drawing TO-236, Variation AB for additional information.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.89	-	1.12	
A1	0.01	-	0.10	
A2	0.88	-	1.02	
D	2.80	2.90	3.04	1,2
E	2.10	-	2.64	
E1	1.20	1.30	1.40	1,2
L1		0.54 REF		
e1		1.90 BSC		
b	0.30	-	0.50	3

12/11/09

	TITLE	GPC	DRAWING NO.	REV.
	3TS1, 3-lead, 1.30mm Body, Plastic Thin Shrink Small Outline Package (Shrink SOT)	TBG	3TS1	B

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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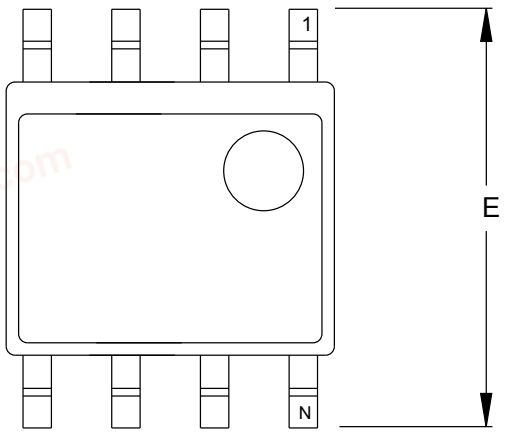
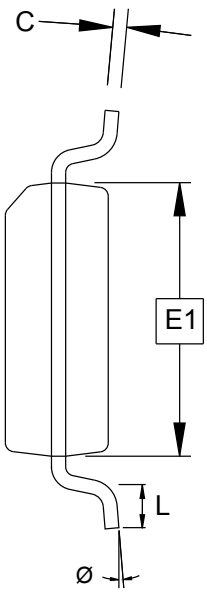
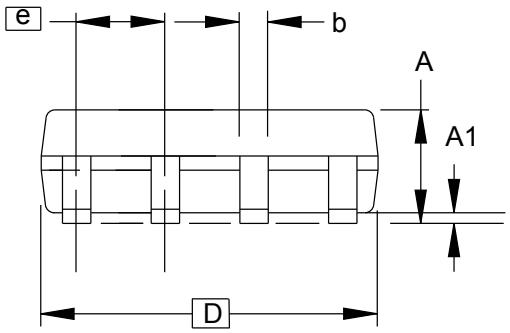


TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.90 BSC			
E	6.00 BSC			
E1	3.90 BSC			
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

3/6/2015

	TITLE	GPC	DRAWING NO.	REV.
	8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	SWB	8S1	H

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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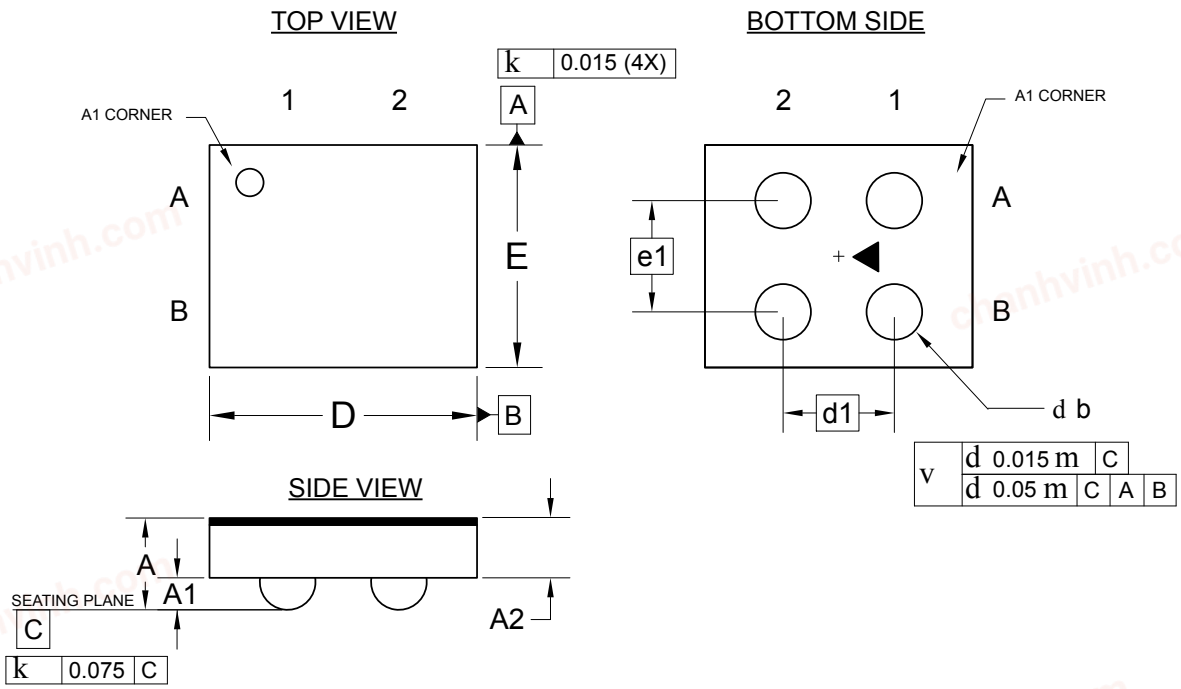

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.313	0.334	0.355	
A1	—	0.094	—	
A2	—	0.240	—	3
D	Contact Microchip for details			
d1	0.400 BSC			
E	Contact Microchip for details			
e1	0.400 BSC			
b	0.170	0.185	0.200	

Note: 1. Dimensions are NOT to scale.
2. Solder ball composition is 95.5Sn-4.0Ag-0.5Cu.
3. Product offered with Back Side Coating.

PIN ASSIGNMENT MATRIX

	1	2
A	SI/O	NC
B	GND	NC

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	TITLE	GPC	DRAWING NO.	REV.
	4U-6, 4-ball 2x2 Array, 0.40mm Pitch Wafer Level Chip-Scale Package (WLCSP) with BSC	GPH	4U-6	B

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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11. Revision History

Atmel AT21CS01 Document 8903 Revision A (August 2015)
Initial document release.

Atmel AT21CS11 Document 8975 Revision A (August 2015)
Initial document release, Preliminary Status.

Atmel AT21CS11 Document 8975 Revision B (November 2015)
Removed Standard Speed mode

Revision A (October 2017)
Updated to Microchip template. This replaces Atmel documents 8903 and 8975. Added XSFN package. Updated DC output current absolute maximum rating. Removed lead finish designation. Updated trace code format in package markings.

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PART NO.	–	XX	X	X	XX	–	X[1]
Device		Package	Device Grade	Operating Voltage	Product Variation		Tape and Reel Option

Device:	AT21CS01/11: Single-Wire, I/O Powered 1-Kbit (128 x 8) Serial EEPROM with Unique, Factory-Programmed 64-bit Serial Number
Package Option:	**MS** = 2-Pad XSFN **ST** = 3-Lead SOT23 **SS** = 8-Lead SOIC **U** = 4-Ball WLCSP (AT21CS01 only) **WWU** = Wafer Unsawn
Package Device Grade or Wafer/Die Thickness:	**H** = Green, Industrial Temperature Range (-40°C to +85°C) **U** = Green, Industrial Temperature Range (-40°C to +85°C) **11** = 11 mil Wafer Thickness
Operating Voltage:	**M** = 1.7V to 3.6V (AT21CS01) **blank** = 2.7V to 4.5V (AT21CS11)
Product Variation:	**10** = 0-0-0 Slave Address (A2, A1, A0)(2) **0B** = 0-0-0 Slave Address (A2, A1, A0), WLCSP package with Back Side Coating
Tape and Reel Option:	**B** = Standard packaging (tube or tray) **T** = Tape and Reel(1)

Note:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Please contact Microchip Sales to order devices with non 0-0-0 slave addresses.

Examples:

- AT21CS01-SSHM10-T, 1.7V-3.6V, Industrial Temp., Tape and Reel, SOIC package, Slave Address 0-0-0
- AT21CS01-SSHM11-B, 1.7V-3.6V, Industrial Temp., SOIC package, Slave Address 0-0-1(2)
- AT21CS01-MSHM15-T, 1.7V-3.6V, Industrial Temp., Tape and Reel, XSFN package, Slave Address 1-0-1(2)
- AT21CS01-UUM0B-T, 1.7V-3.6V, Industrial Temp., Tape and Reel, UDFN package, Slave Address 0-0-0

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- AT21CS11-STU10, 2.7V-4.5V, Industrial Temp., SOT23 package, Slave Address 0-0-0
- AT21CS11-MSH17-T, 2.7V-4.5V, Industrial Temp., XSFN package, Slave Address 1-1-1(2)
- AT21CS11-WWU11(1), 2.7V-4.5V, Industrial Temp., 11 mil Thick Wafer Thickness, Slave Address 0-0-0 all die

Note:

1. Contact Microchip Sales for wafer sales.
2. Please contact Microchip Sales to order non 0-0-0 slave addressed devices.

Microchip Devices Code Protection Feature

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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