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# 2N6660

## N-Channel, Enhancement-Mode, Vertical DMOS FET

### Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low $C_{ISS}$ and fast switching speeds
- Excellent thermal stability
- Integral source-drain diode
- High input impedance and high gain

### Applications

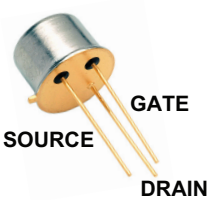
- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers: relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.

### Description

2N6660 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power-handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very-low threshold voltage, high breakdown voltage, high-input impedance, low-input capacitance, and fast switching speeds are desired.

### Package Types




**TO-39**
**Case: Drain**

See Table 2-1 for pin information

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# 2N6660

## 1.0 ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS†

Drain-to-source voltage ..... $BV_{DSS}$
Drain-to-gate voltage ..... $BV_{DGS}$
Gate-to-source voltage ..... ±20V
Operating and Storage Temperature ..... -55 to 150 °C

**† Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise specified, for all specifications $T_A$ = +25°C

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **DC Parameters** (Note 1, unless otherwise stated) | | | | | | |
| Drain-to-source breakdown voltage | $BV_{DSS}$ | 60 | - | - | V | $V_{GS}$= 0V, $I_D$= 10µA |
| Gate threshold voltage | $V_{GS(th)}$ | 0.8 | - | 2.0 | V | $V_{GS}$= $V_{DS}$, $I_D$= 1.0mA |
| $V_{GS(th)}$ change with temperature | $\Delta V_{GS(th)}$ | - | -3.8 | -5.5 | mV/°C | $V_{GS}$= $V_{DS}$, $I_D$= 1.0mA (Note 2) |
| Gate body leakage current | $I_{GSS}$ | - | - | 100 | nA | $V_{GS}$= ±20V, $V_{DS}$= 0V |
| Zero gate voltage drain current | $I_{DSS}$ | - | - | 10 | µA | $V_{GS}$= 0V, $V_{DS}$= Max rating |
| | | - | - | 500 | | $V_{DS}$= 0.8 Max Rating, $V_{GS}$= 0V, $T_A$= 125°C (Note 2) |
| On-state drain current | $I_{D(ON)}$ | 1.5 | - | - | A | $V_{GS}$= 10V, $V_{DS}$= 10V |
| Static drain-to-source on-state resistance | $R_{DS(ON)}$ | - | - | 5.0 | Ω | $V_{GS}$= 5.0V, $I_D$= 0.3A |
| | | - | - | 3.0 | | $V_{GS}$= 10V, $I_D$= 1.0A |
| **AC Parameters** (Note 2) | | | | | | |
| Forward transconductance | $G_{FS}$ | 170 | - | - | mmho | $V_{DS}$= 25V, $I_D$= 0.5A |
| Input capacitance | $C_{ISS}$ | - | - | 50 | pF | $V_{GS}$= 0V, $V_{DS}$= 24V, f = 1.0MHz |
| Common source output capacitance | $C_{OSS}$ | - | - | 40 | | |
| Reverse transfer capacitance | $C_{RSS}$ | - | - | 10 | | |
| Turn-on time | $t_{(ON)}$ | - | - | 10 | ns | $V_{DD}$= 25V, $I_D$= 1.0A, $R_{GEN}$= 25Ω |
| Turn-off time | $t_{(OFF)}$ | - | - | 10 | | |
| **Diode Parameters** | | | | | | |
| Diode forward voltage drop | $V_{SD}$ | - | 1.2 | - | V | $V_{GS}$= 0V, $I_{SD}$= 1.0A (Note 1) |
| Reverse recovery time | $t_{rr}$ | - | 350 | - | ns | $V_{GS}$= 0V, $I_{SD}$= 1.0A (Note 2) |

**Note 1:** All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle.

**2:** Specification is obtained by characterization and is not 100% tested.

### TEMPERATURE SPECIFICATIONS

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Operating and Storage Temperature | $T_A$ | -55 | – | 150 | °C | |


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## THERMAL CHARACTERISTICS

| Package | $I_D$(1) continuous (mA) | $I_D$ pulsed (A) | Power Dissipation @$T_A$ = 25°C (W) | $I_{DR}$(1) (mA) | $I_{DRM}$ (A) |
|---|---|---|---|---|---|
| TO-39 | 410 | 3.0 | 6.25 | 410 | 3.0 |

**Note 1:** $I_D$ (continuous) is limited by max rated $T_J$.

### Product Summary

| $BV_{DSX}/BV_{DGS}$ (V) | $R_{DS(ON)}$ (max) (Ω) | $I_{DSS}$ (min) (A) |
|---|---|---|
| 60 | 3.0 | 1.5 |

## 2.0 PIN DESCRIPTION

The locations of the pins are listed in Package Types and Packaging Information.

**TABLE 2-1: PIN DESCRIPTION**

| Pin # TO-39 | Function |
|---|---|
| 1 | SOURCE |
| 2 | GATE |
| 3 | DRAIN |

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## 3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 shows the switching waveform and test circuit for 2N6660.

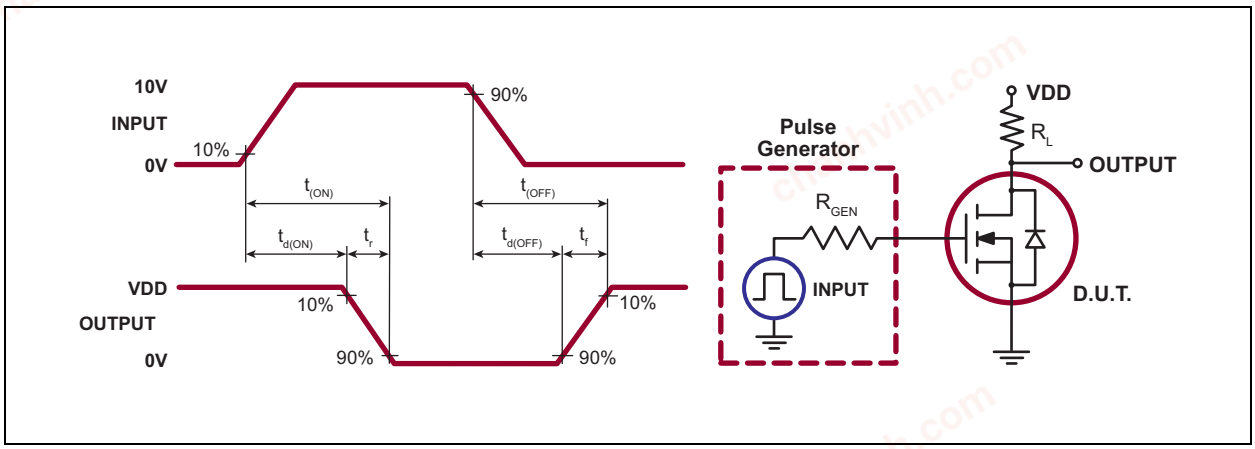



***FIGURE 3-1:*** *Switching Waveforms and Test Circuit*


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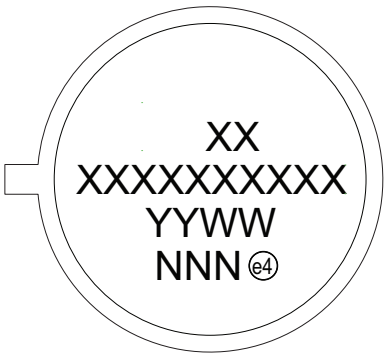
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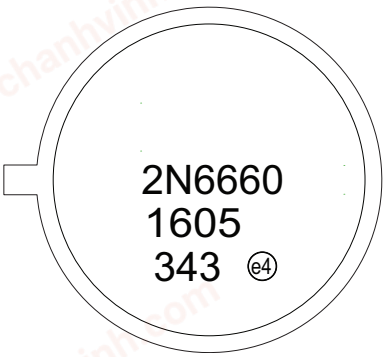
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

3-Lead TO-39




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

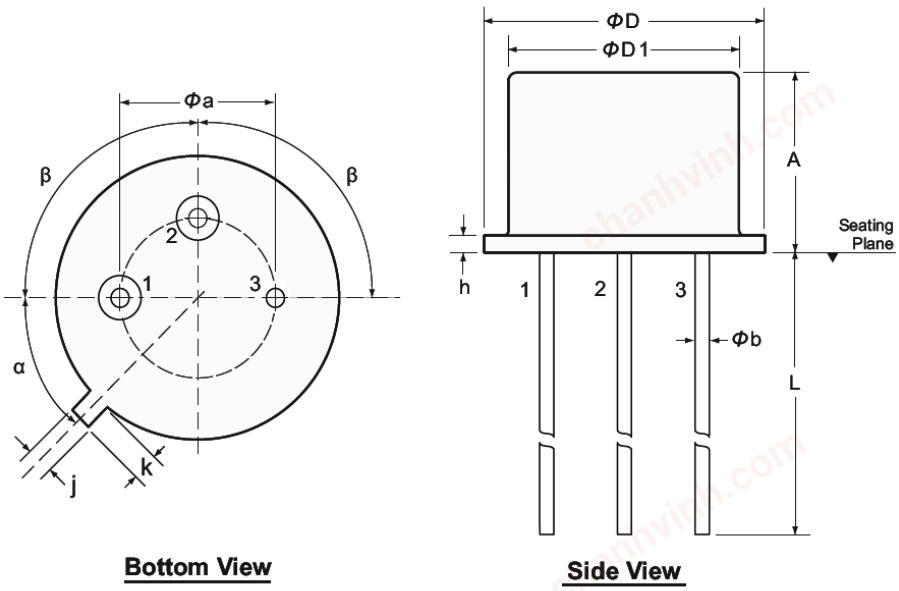
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

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## 3-Lead TO-39 Package Outline (N2)




**Bottom View** **Side View**

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

| Symbol | | α | β | A | Φa | Φb | ΦD | ΦD1 | h | j | k | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (inches) | MIN | 45° NOM | 90° NOM | .240 | .190 | .016 | .350 | .315 | .009 | .028 | .029 | .500 |
| | NOM | | | - | - | - | - | - | - | - | - | - |
| | MAX | | | .260 | .210 | .021 | .370 | .335 | .125 | .034 | .040 | .560* |

*JEDEC Registration TO-39.*
** This dimension is not specified in the JEDEC drawing.*
***Drawings not to scale.***


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## APPENDIX A: REVISION HISTORY

### Revision A (March 2016)

- Converted Supertex Doc #DSFP-2N6660 to Microchip DS20005509A.
- Minor text changes throughout.
- Update to **Features**.

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# 2N6660

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | XX | - | X | - | X |
|---|---|---|---|---|---|
| Device | Package Options | | Environmental | | Media Type |

| | | | |
|---|---|---|---|
| Device: | 2N6660 | = | N-Channel, Enhancement-Mode, Vertical DMOS FET |
| Package: | (blank) | = | TO-39, 3-lead |
| Environmental | (blank) | = | Lead (Pb)-free/ROHS-compliant package |
| Media Type: | (blank) | = | 500/Bag for TO-39 packages |

**Examples:**

a) 2N6660 TO-39 package, 500/bag


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