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24AA512/24LC512/24FC512

512-Kbit I²C Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges	Packages
24AA512	1.7-5.5V	400 kHz(1)	I	CSP, MF, P, SM, SN, ST, ST14
24LC512	2.5-5.5V	400 kHz	I, E	MF, P, SM, SN, ST, ST14
24FC512	1.7-5.5V	1 MHz(2)	I, E	MF, Q4B, P, OT, SM, SN, ST, ST14

Note 1: 100 kHz for Vcc < 2.5V
2: 400 kHz for Vcc < 2.5V

Features

- Single Supply with Operation down to 1.7V for 24AA512 and 24FC512 Devices and 2.5V for 24LC512 Devices
- Low-Power CMOS Technology:
  - Read current: 400 µA, maximum
  - Standby current: 1 µA maximum (I-Temp.)
- Two-Wire Serial Interface, I²C Compatible
- Cascadable for up to Eight Devices
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz, 400 kHz and 1 MHz Clock Compatibility
- Page Write Time: 5 ms, Maximum
- Self-Timed Erase/Write Cycle
- 128-Byte Page Write Buffer
- Hardware Write-Protect
- ESD Protection: > 4,000V
- More than 1 Million Erase/Write Cycles
- Data Retention: > 200 years
- RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- AEC-Q100 Automotive Qualified

Packages

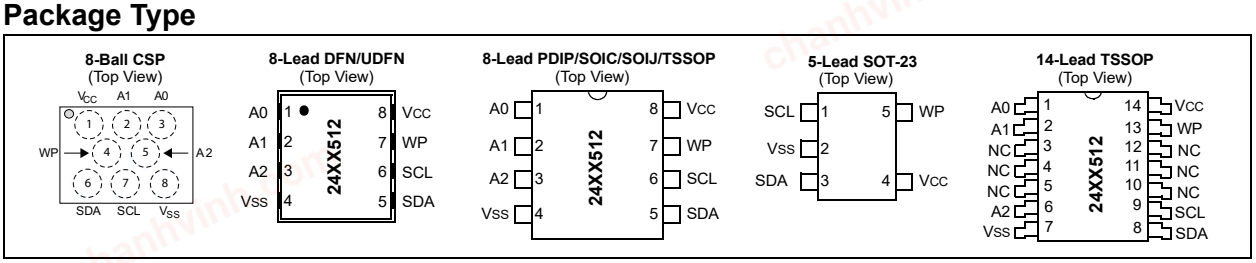
- 8-Ball CSP, 8-Lead DFN, 8-Lead PDIP, 8-Lead SOIC, 8-Lead SOIJ, 5-Lead SOT-23, 8-Lead TSSOP, 14-Lead TSSOP and 8-Lead UDFN

Description

The Microchip Technology Inc. 24XX512(1) is a 512-Kbit Electrically Erasable PROM (EEPROM). The device is organized as a single block of 64K x 8-bit memory with a two-wire serial interface. Its low-voltage design permits operation down to 1.7V, with standby and active currents of only 1 µA and 400 µA, respectively. The 24XX512 also has a page write capability for up to 128 bytes of data. This device is capable of both random and sequential reads up to the 512K boundary. Functional address lines allow up to eight devices on the same bus, for up to 4 Mbit address space.

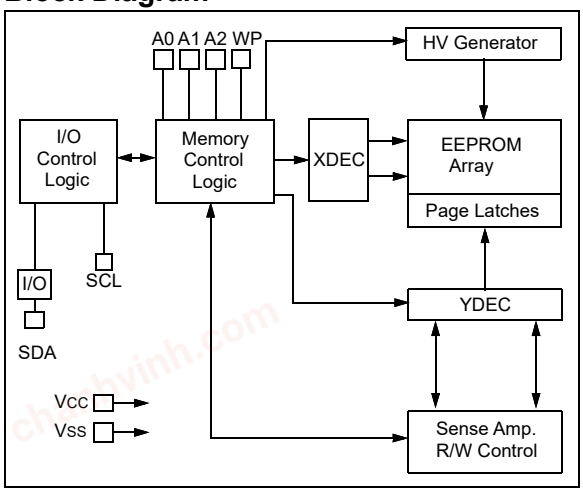
Note 1: 24XX512 is used in this document as a generic part number for the 24AA512/24LC512/24FC512 devices.

Package Type



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Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins.....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Extended (E): VCC = +2.5V to 5.5V TA = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
D1	VIH	High-Level Input Voltage	0.7 VCC	—	V	
D2	VIL	Low-Level Input Voltage	—	0.3 VCC	V	VCC ≥ 2.5V
			—	0.2 VCC	V	VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger Inputs (SDA, SCL pins)	0.05 VCC	—	V	VCC ≥ 2.5V **(Note 1)**
D4	VOL	Low-Level Output Voltage	—	0.40	V	IOL = 3.0 mA, VCC = 4.5V
			—	0.40	V	IOL = 2.1 mA, VCC = 2.5V
D5	ILI	Input Leakage Current	—	±1	µA	VIN = VSS or VCC, WP = VSS
			—	±1	µA	VIN = VSS or VCC, WP = VCC
D6	ILO	Output Leakage Current	—	±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin Capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V **(Note 1)** TA = 25°C, FCLK = 1 MHz
D8	ICCREAD	Operating Current	—	400	µA	VCC = 5.5V, SCL = 400 kHz
	ICCWRITE		—	5	mA	VCC = 5.5V
D9	ICCS	Standby Current	—	1	µA	SDA = SCL = VCC = 5.5V A0, A1, A2, WP = VSS, I-Temp.
			—	5	µA	SDA = SCL = VCC = 5.5V A0, A1, A2, WP = VSS, E-Temp.

Note 1: This parameter is periodically sampled and not 100% tested.

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TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Extended (E): VCC = +2.5V to 5.5V TA = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock Frequency	—	100	kHz	1.7V ≤ VCC < 2.5V
			—	400	kHz	2.5V ≤ VCC ≤ 5.5V
			—	400	kHz	1.7V ≤ VCC < 2.5V **(24FC512)**
			—	1000	kHz	2.5V ≤ VCC ≤ 5.5V **(24FC512)**
2	THIGH	Clock High Time	4000	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.7V ≤ VCC < 2.5V **(24FC512)**
			500	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC512)**
3	TLOW	Clock Low Time	4700	—	ns	1.7V ≤ VCC < 2.5V
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.7V ≤ VCC < 2.5V **(24FC512)**
			500	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC512)**
4	TR	SDA and SCL Rise Time **(Note 1)**	—	1000	ns	1.7V ≤ VCC< 2.5V
			—	300	ns	2.5V ≤ VCC ≤ 5.5V
			—	300	ns	1.7V ≤ VCC ≤ 5.5V **(24FC512)**
5	TF	SDA and SCL Fall Time **(Note 1)**	—	300	ns	All except **24FC512**
			—	100	ns	1.7V ≤ VCC ≤ 5.5V **(24FC512)**
6	THD:STA	Start Condition Hold Time	4000	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.7V ≤ VCC < 2.5V **(24FC512)**
			250	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC512)**
7	TSU:STA	Start Condition Setup Time	4700	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.7V ≤ VCC < 2.5V **(24FC512)**
			250	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC512)**
8	THD:DAT	Data Input Hold Time	0	—	ns	**(Note 2)**
9	TSU:DAT	Data Input Setup Time	250	—	ns	1.7V ≤ VCC < 2.5V
			100	—	ns	2.5V ≤ VCC ≤ 5.5V
			100	—	ns	1.7V ≤ VCC ≤ 5.5V **(24FC512)**
10	TSU:STO	Stop Condition Setup Time	4000	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.7V ≤ VCC < 2.5V **(24FC512)**
			250	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC512)**
11	TSU:WP	WP Setup Time	4000	—	ns	1.7V ≤ VCC < 2.5V
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.7V ≤ VCC ≤ 5.5V **(24FC512)**

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization.

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AC CHARACTERISTICS (Continued)			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Extended (E): VCC = +2.5V to 5.5V TA = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
12	THD:WP	WP Hold Time	4700	—	ns	1.7V ≤ VCC < 2.5V
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.7V ≤ VCC ≤ 5.5V **(24FC512)**
13	TAA	Output Valid from Clock **(Note 2)**	—	3500	ns	1.7V ≤ VCC < 2.5V
			—	900	ns	2.5V ≤ VCC ≤ 5.5V
			—	900	ns	1.7V ≤ VCC < 2.5V **(24FC512)**
			—	400	ns	2.5V ≤ VCC ≤ 5.5V **(24FC512)**
14	TBUF	Bus Free Time: The time must be free before a new transmission can start	4700	—	ns	1.7V ≤ VCC < 2.5V
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.7V ≤ VCC < 2.5V **(24FC512)**
			500	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC512)**
15	TSP	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	All except **24FC512** (**Notes 1** and **3**)
16	TWC	Write Cycle Time (byte or page)	—	5	ms	
17		Endurance	1,000,000	—	cycles	25°C, VCC = 5.5V, Page Mode **(Note 4)**

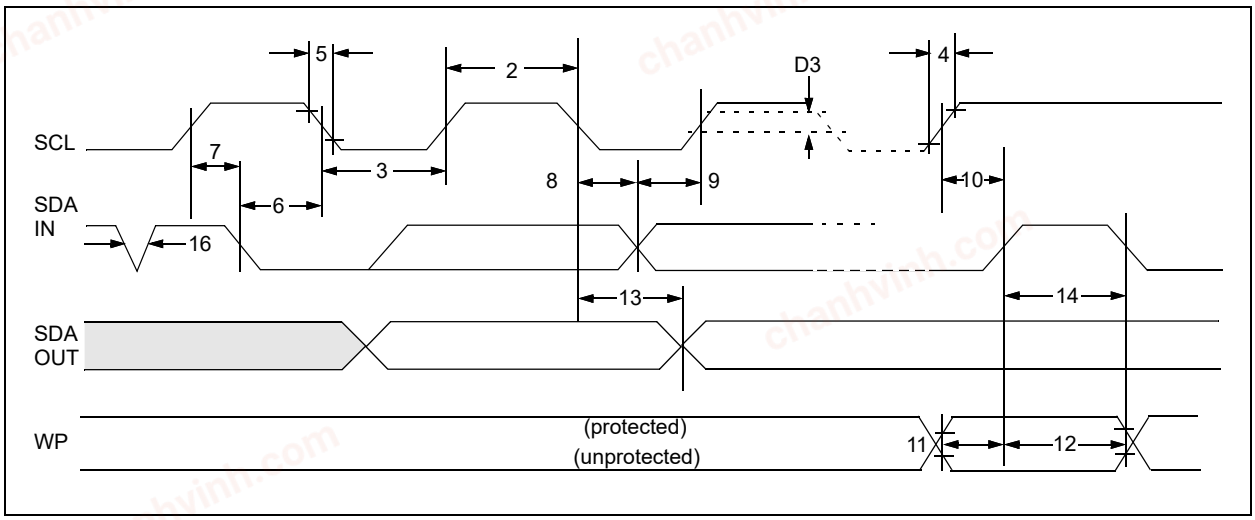
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization.

FIGURE 1-1: BUS TIMING DATA



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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	CSP	DFN(1)	PDIP	SOIC	SOIJ	SOT-23	8-lead TSSOP	14-lead TSSOP	UDFN(1)	Function
A0	3	1	1	1	1	—	1	1	1	User Configured Chip Select
A1	2	2	2	2	2	—	2	2	2	User Configured Chip Select
A2	5	3	3	3	3	—	3	6	3	User Configured Chip Select
Vss	8	4	4	4	4	2	4	7	4	Ground
SDA	6	5	5	5	5	3	5	8	5	Serial Address/Data I/O
SCL	7	6	6	6	6	1	6	9	6	Serial Clock
WP	4	7	7	7	7	5	7	13	7	Write-Protect
Vcc	1	8	8	8	8	4	8	14	8	Power Supply

Note 1: Exposed pad on DFN/UDFN can be connected to VSS or left floating.

2.1 A0, A1 and A2 Chip Address Inputs

The A0, A1 and A2 inputs are used by the 24XX512 for multiple device operations. The logic levels on these inputs are compared with the corresponding bits in the client address. The chip is selected if the comparison is true.

Up to eight devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VCC or VSS.

In most applications, the chip address inputs A0, A1 and A2 are hardwired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable logic device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

Note:	For the SOT-23 package, Chip Address Inputs are not available and are not connected.

2.2 Serial Data (SDA)

SDA is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.3 Serial Clock (SCL)

The SCL input is used to synchronize the data transfer from and to the device.

2.4 Write-Protect (WP)

The WP pin must be connected to either VSS or VCC. If tied to VSS, write operations are enabled. If tied to VCC, write operations are inhibited but read operations are not affected.

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3.0 FUNCTIONAL DESCRIPTION

The 24XX512 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The bus must be controlled by a host device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX512 works as a client. Both host and client can operate as transmitter or receiver, but the host device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the host device and is, theoretically, unlimited (although only the last 128 bytes will be stored when doing a write operation). When an overwrite does occur, it will replace data in a First-In First-Out (FIFO) principle.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The host device must generate an extra clock pulse which is associated with this Acknowledge bit. See Figure 4-2 for acknowledge timing.

Note:	The 24XX512 does not generate any Acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. During reads, a host must signal an end of data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24XX512) will leave the data line high to enable the host to generate the Stop condition.

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FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

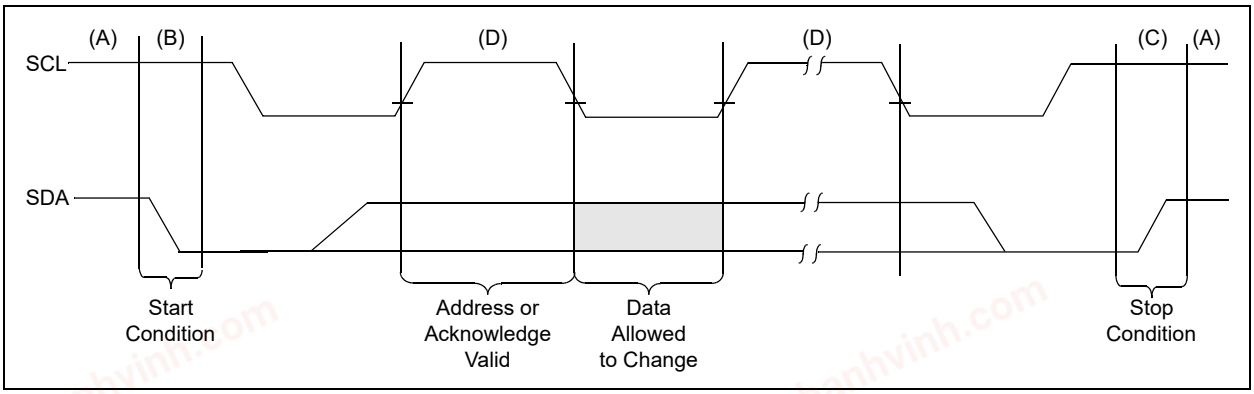
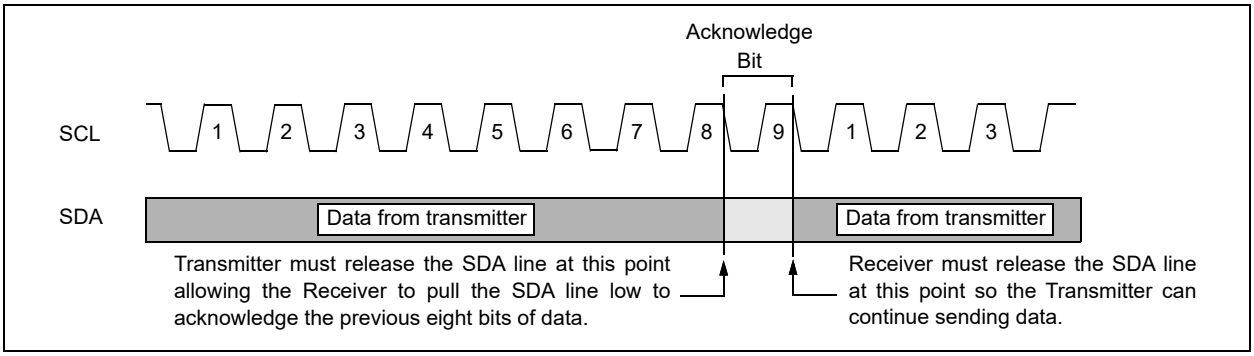


FIGURE 4-2: ACKNOWLEDGE TIMING



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5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the host device. The control byte consists of a 4-bit control code. For the 24XX512, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1 and A0). The Chip Select bits allow the use of up to eight 24XX512 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are, in effect, are the three Most Significant bits of the word address. The combination of the 4-bit control code and the next three bits are called the client address.

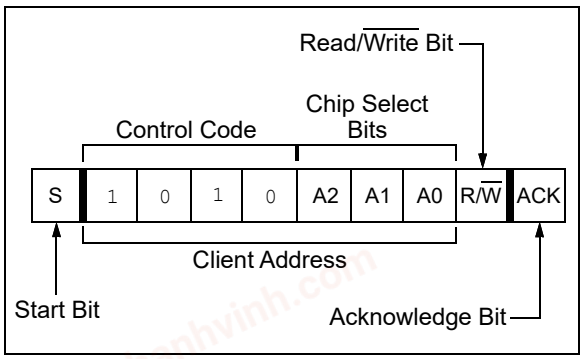
For the SOT-23 package, the address pins are not available. During device addressing, the A2, A1, and A0 Chip Selects bits should be set to '0'.

The last bit of the control byte is the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit and it defines the operation to be performed. When set to a '1', a read operation is selected. When set to a '0', a write operation is selected.

Following the Start condition, the 24XX512 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a valid client address and the R/$\overline{\text{W}}$ bit, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{\text{W}}$ bit, the 24XX512 will select a read or write operation.

The next two bytes received define the address of the first data byte (Figure 5-2). Because all A15...A0 are used, there are no upper address bits that are "don't care". The upper address bits are transferred first, followed by the Less Significant bits.

FIGURE 5-1: CONTROL BYTE FORMAT

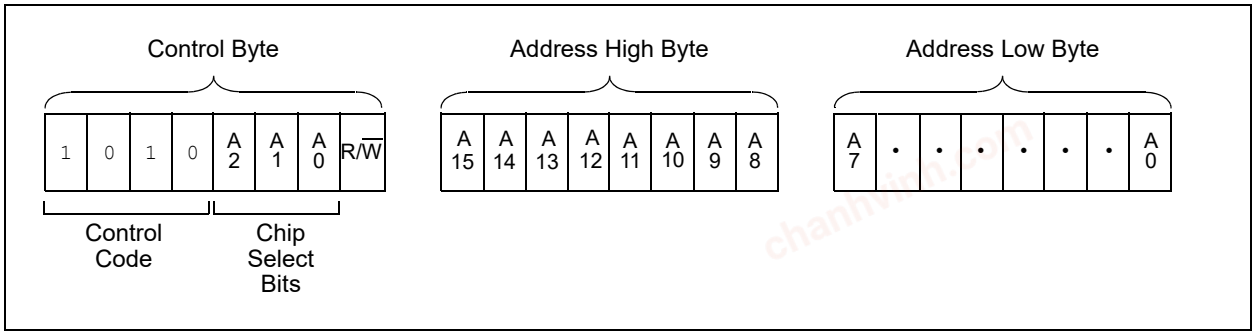


5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 4 Mbit by adding up to eight 24XX512 devices on the same bus. In this case, software can use A0 of the control byte as address bit A16; A1 as address bit A17; and A2 as address bit A18. It is not possible to sequentially read across device boundaries.

The SOT-23 package do not support multiple device addressing on the same bus.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



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6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start condition from the host, the control code (four bits), the Chip Select (three bits) and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the host transmitter. This indicates to the addressed client receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the high-order byte of the word address and will be written into the Address Pointer of the 24XX512.

The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX512, the host device will transmit the data word to be written into the addressed memory location. The 24XX512 acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and, during this time, the 24XX512 will not generate Acknowledge signals (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command. After a byte Write command, the internal address counter will point to the address location following the one that was just written.

Note:	When doing a write of less than 128 bytes, the data on the rest of the page are refreshed along with the data bytes being written. Consequently, the entire page undergoes a write cycle. Therefore, endurance is specified on a per-page basis.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX512 in the same way as in a byte write. However, instead of generating a Stop condition, the host transmits up to 127 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory after the host has transmitted a Stop condition. Upon receipt of each word, the seven lower Address Pointer bits, which form the byte counter, are internally incremented by one. The higher-order nine bits of the word address remain constant.

If the host should transmit more than 128 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of page size – 1. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is, therefore, necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

6.3 Write Protection

The WP pin allows the user to write-protect the entire array (0000-FFFF) when the pin is tied to VCC. If tied to VSS, the write protection is disabled. The WP pin is sampled at the Stop bit for every Write command (Figure 4-1). Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

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FIGURE 6-1: BYTE WRITE

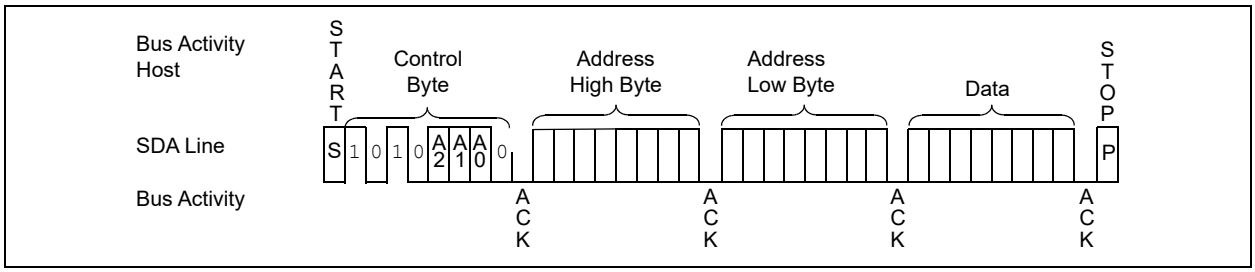
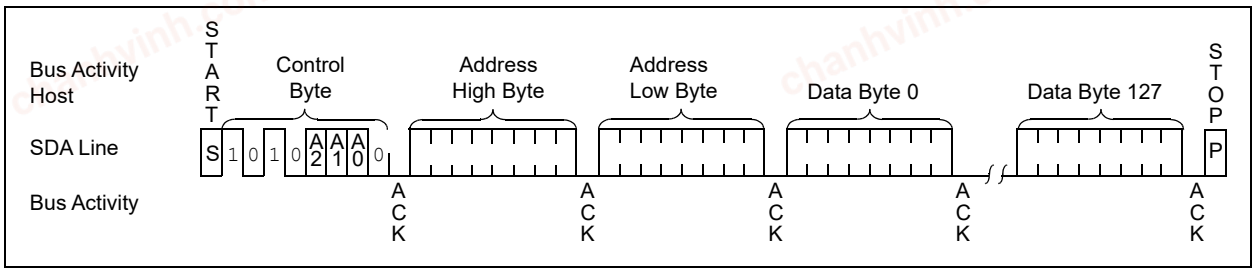


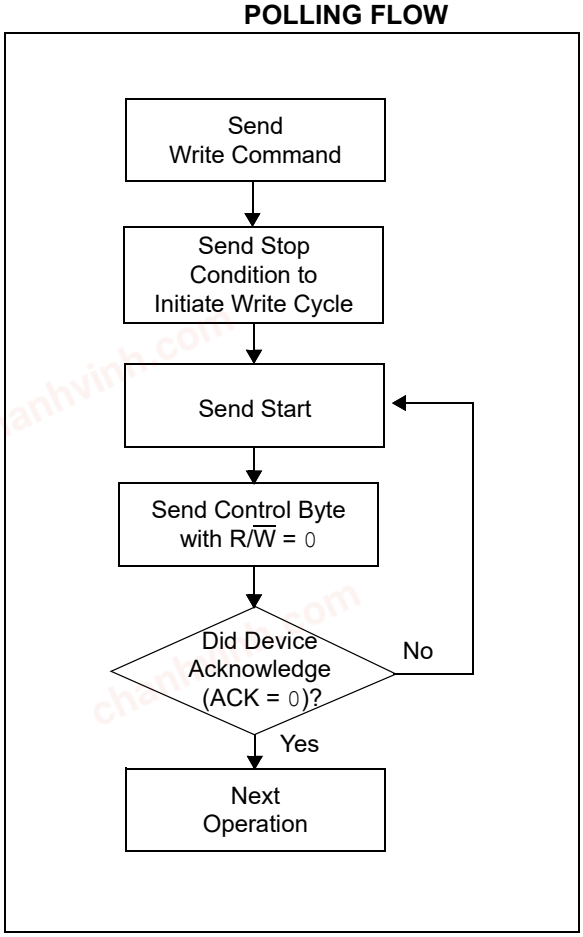
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the host, the device initiates the internally timed write cycle, and ACK polling can be initiated immediately. This involves the host sending a Start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be resent. If the cycle is complete, the device will return the ACK and the host can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



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8.0 READ OPERATION

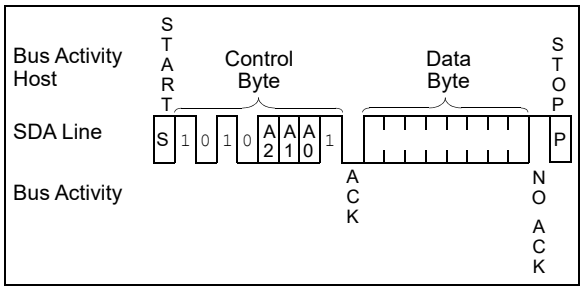
Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the control byte is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XX512 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address '**n**' (n is any legal address), the next current address read operation would access data from address **n + 1**.

Upon receipt of the control byte with R/$\overline{W}$ bit set to '1', the 24XX512 issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer but will generate a Stop condition and the 24XX512 discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24XX512 as part of a write operation (R/$\overline{W}$ bit set to '0'). After the word address is sent, the host generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 24XX512 will then issue an Acknowledge and transmit the 8-bit data word. The host will not acknowledge the transfer but does generate a Stop condition, which causes the 24XX512 to discontinue transmission (Figure 8-2). After a random Read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as random reads, except that after the 24XX512 transmits the first data byte, the host issues an Acknowledge (as opposed to the Stop condition used in a random read). This Acknowledge directs the 24XX512 to transmit the next sequentially-addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the host, the host will NOT generate an Acknowledge, but will generate a Stop condition.

To provide sequential reads, the 24XX512 contains an internal Address Pointer, which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address FFFF to address 0000 if the host acknowledges the byte received from the array address FFFF.

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FIGURE 8-2: RANDOM READ

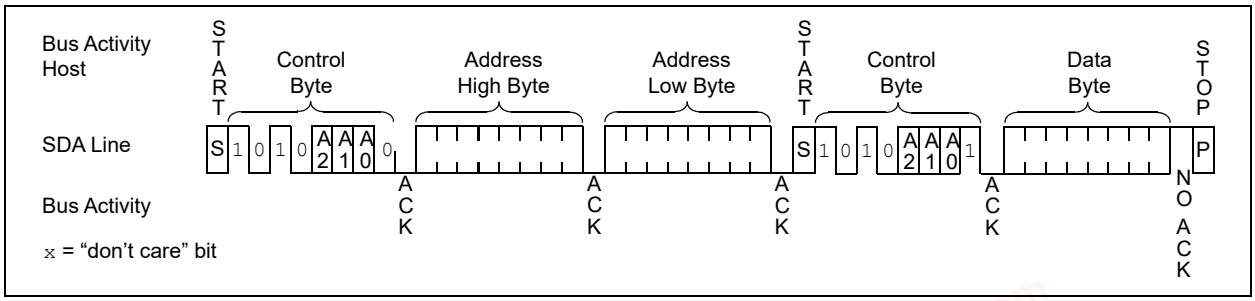
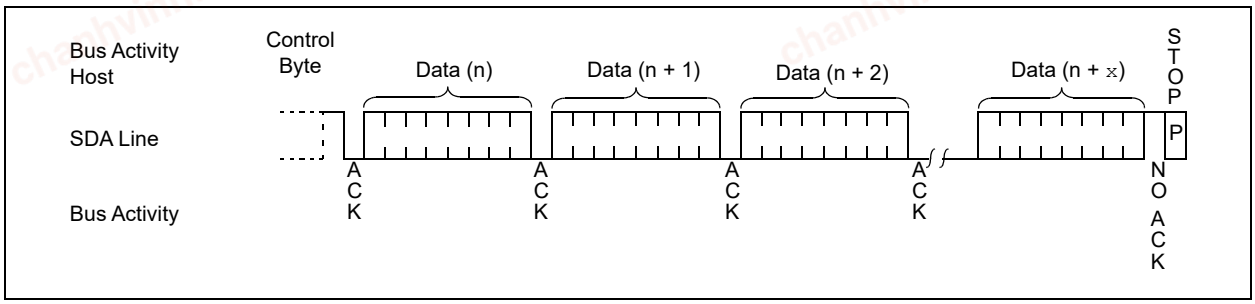


FIGURE 8-3: SEQUENTIAL READ

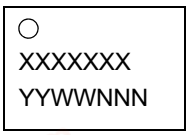


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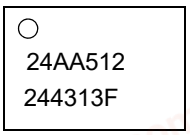
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

8-Lead Chip Scale



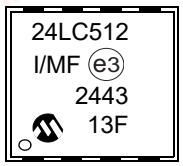
Example:



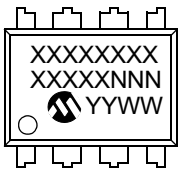
8-Lead 5x6x0.9 DFN-S



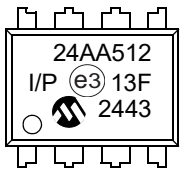
Example:



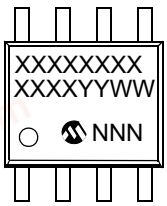
8-Lead PDIP (300 mil)



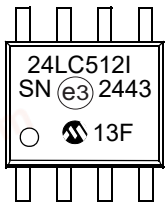
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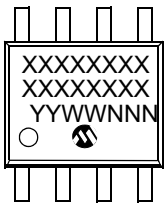
8-Lead SOIC (3.90 mm)



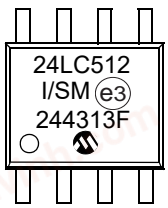
Example:



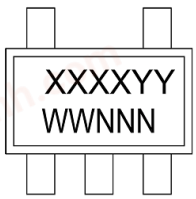
8-Lead SOIJ (5.28 mm)



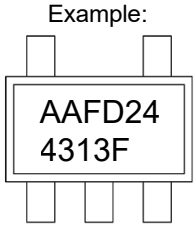
Example:



5-Lead SOT-23



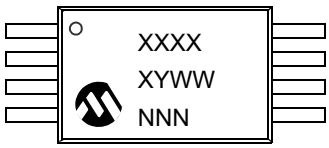
Example:



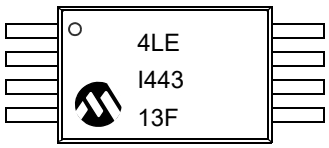
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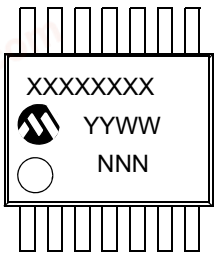
8-Lead TSSOP



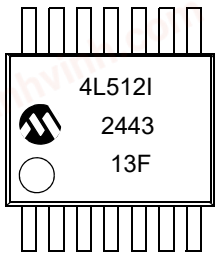
Example:



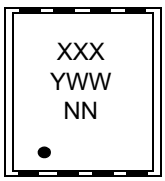
14-Lead TSSOP



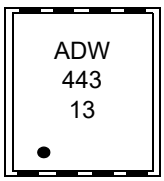
Example:



8-Lead UDFN (Q4B)



Example



Part Number	First Line Marking Code								
	CSP	DFN	PDIP	SOIC	SOIJ	SOT-23	8-Lead TSSOP	14-Lead TSSOP	UDFN
24AA512	24AA512	24AA512	24AA512	24AA512T	24AA512	—	4AE	4A512T	—
24LC512	—	24LC512	24LC512	24LC512T	24LC512	—	4LE	4L512T	—
24FC512	—	24FC512	24FC512	24FC512T	24FC512	AAFDYY	4FE	4F512T	ADW

Legend:

XX...X	Part number or part number code
T	Temperature (I, E)
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code (2 characters for small packages)
(e3)	JEDEC® designator for Matte Tin (Sn)

Note: Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

Note: For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

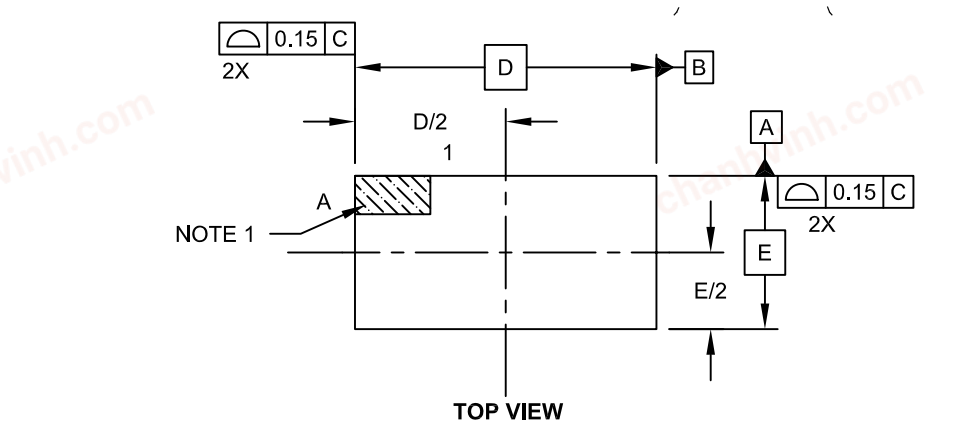
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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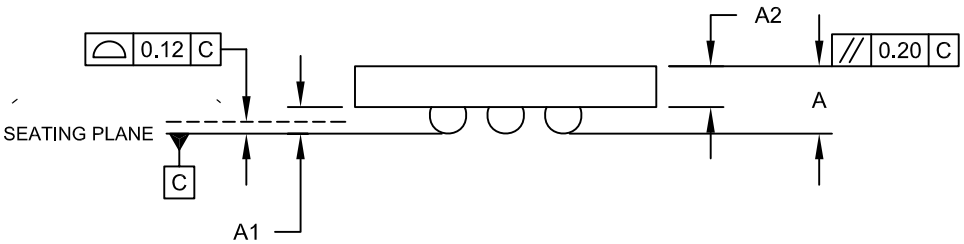
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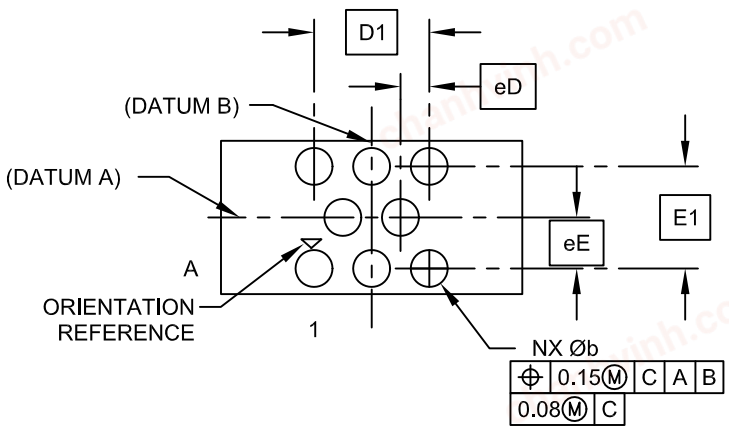
8-Lead Chip Scale Package (CS) - [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW





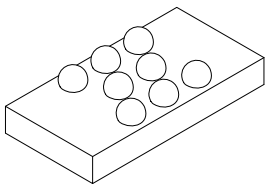
BOTTOM VIEW

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8-Lead Chip Scale Package (CS) - [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Contacts	N		8	
Overall Grid X-Pitch	E1		0.886 BSC	
Overall Grid Y-Pitch	D1		1.00 BSC	
Adjacent Column X-Pitch	eE		0.443 BSC	
Adjacent Row Y-Pitch	eD		0.25 BSC	
Overall Height	A	0.53	0.59	0.64
Die Height	A2	0.33	0.36	0.38
Bump Height	A1	0.20	0.23	0.26
Overall Width	E		NOTE 4	
Overall Length	D		NOTE 4	
Ball Diameter	b	0.30	0.32	0.34

Notes:

1. Orientation reference feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
4. Package size varies with specific devices. Please contact your local Microchip representative for specific details

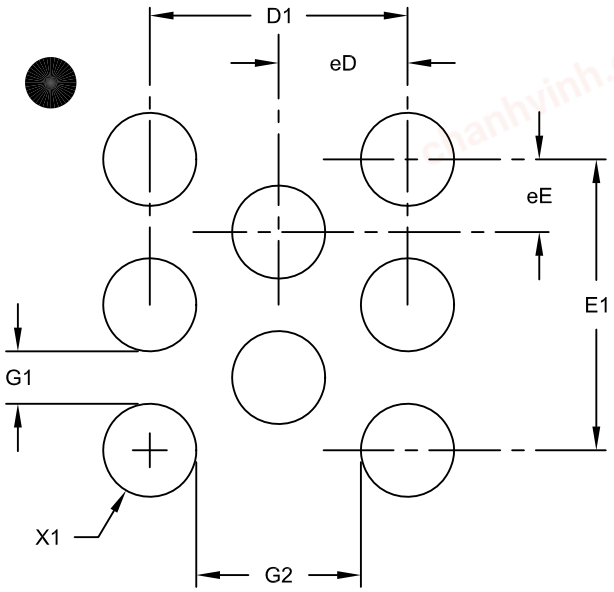
Microchip Technology Drawing C04-6001C Sheet 2 of 2

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8-Lead Chip Scale Package (CS) - [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Contacts	N		8	
Contact Pitch Y	eE		0.25	
Contact Pitch X	eD		0.443	
Contact Pad Spacing	E1		1.00	
Contact Pad Spacing	D1		0.886	
Contact Pad Diameter (X8)	X1			0.32
Distance Between Pads	G1	0.18		
Distance Between Pads	G2	0.56		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

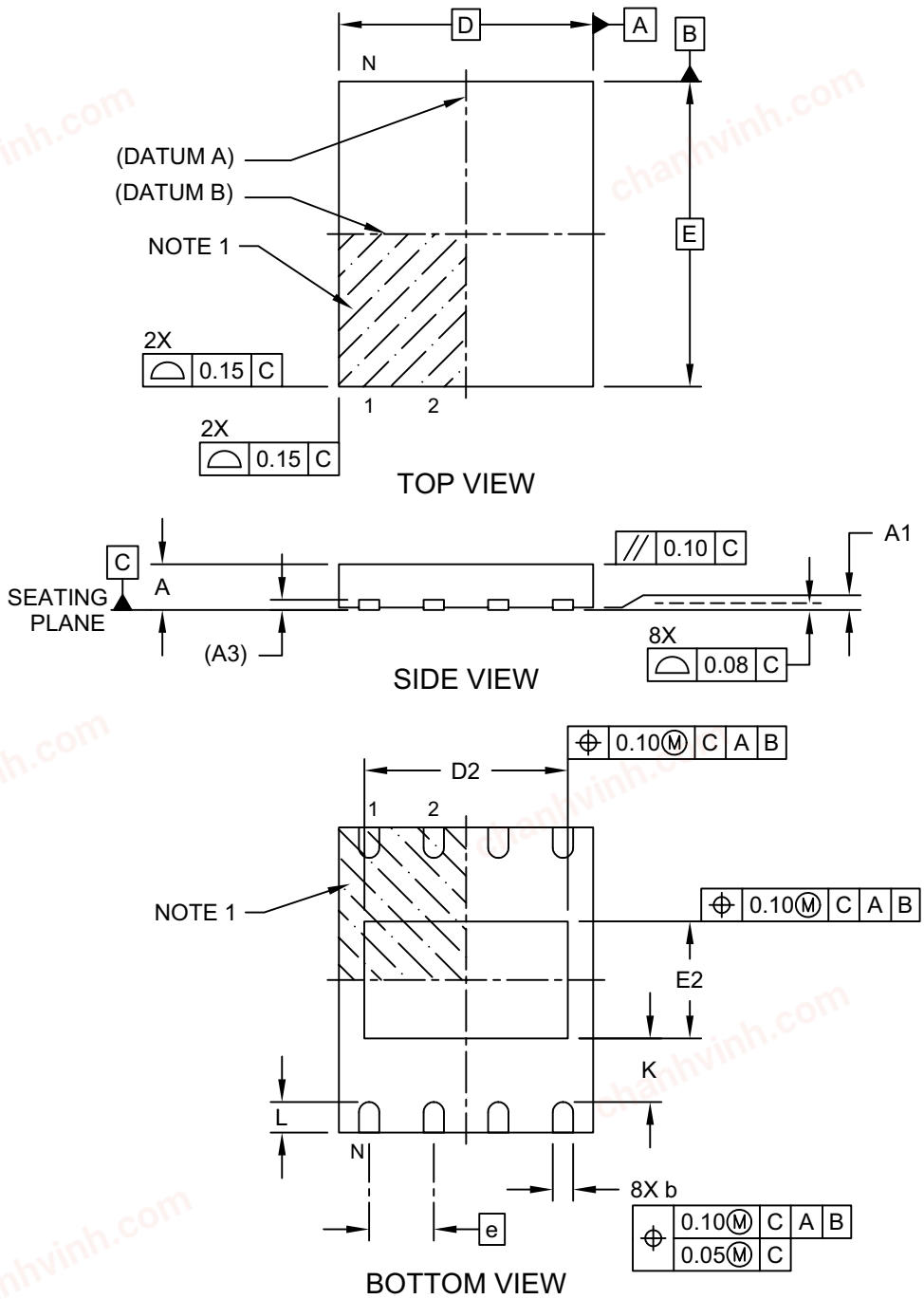
Microchip Technology Drawing No. C04-8001A

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8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



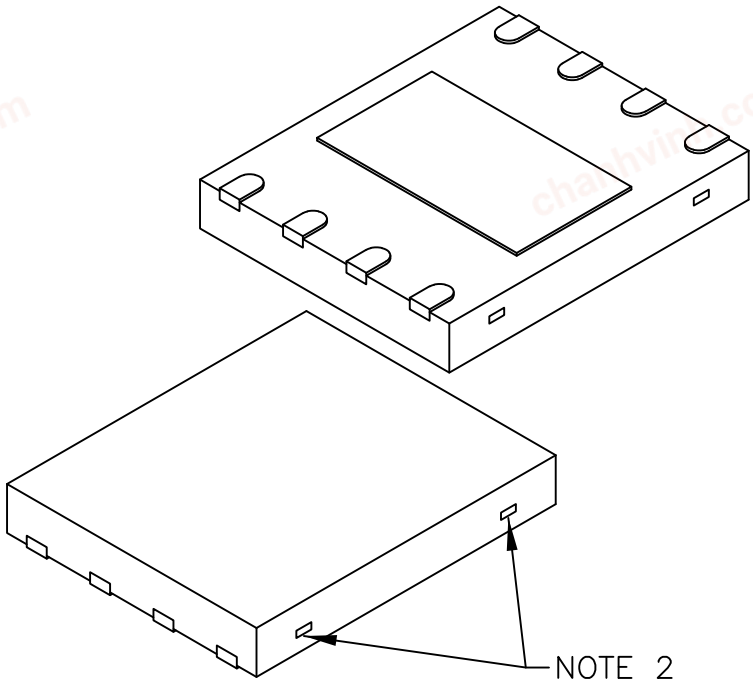
Microchip Technology Drawing C04-122 Rev D Sheet 1 of 2

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8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.90	4.00	4.10
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	2.20	2.30	2.40
Terminal Width	b	0.30	0.40	0.50
Terminal Length	L	0.50	0.60	0.75
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one ore more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

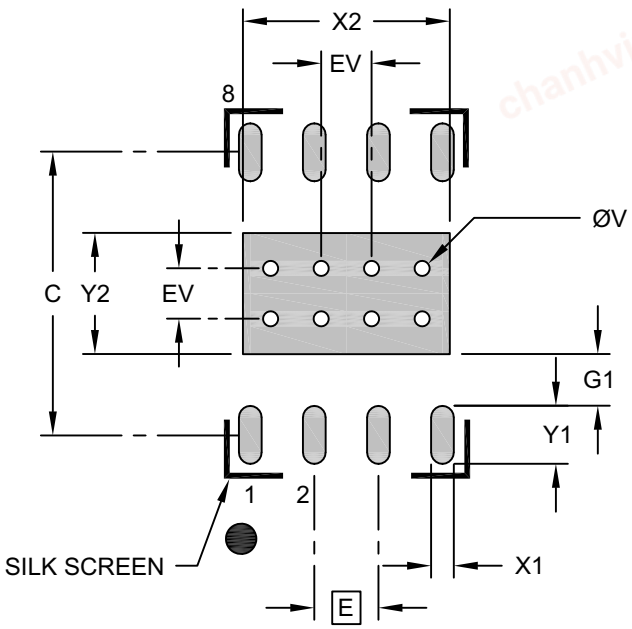
Microchip Technology Drawing C04-122 Rev D Sheet 2 of 2

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8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Length	X2			4.10
Optional Center Pad Width	Y2			2.40
Contact Pad Spacing	C		5.60	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.15
Contact Pad to Center Pad (X20)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

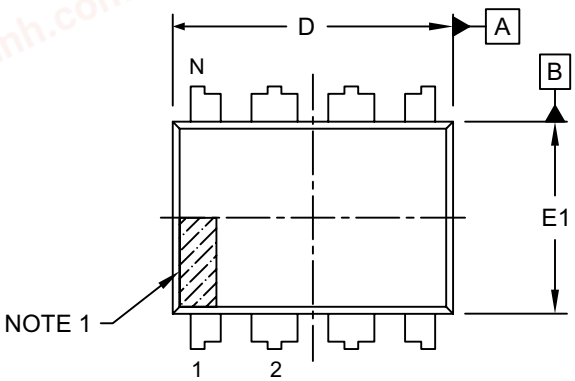
Microchip Technology Drawing C04-2122 Rev D

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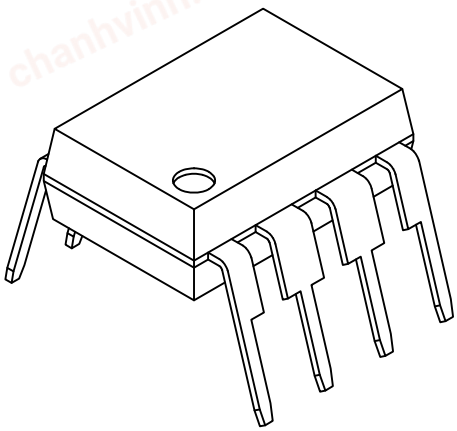
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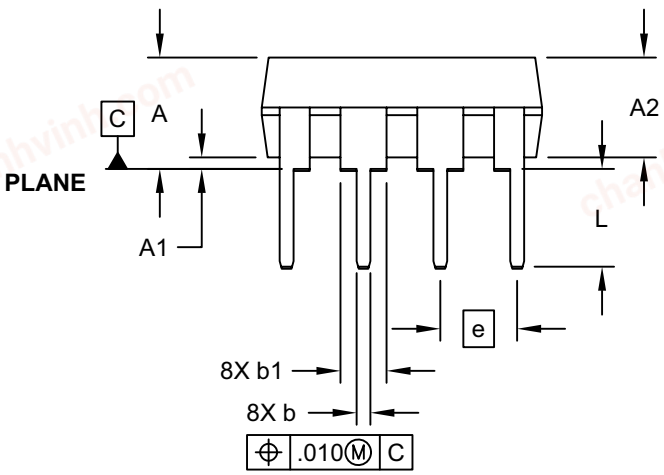
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

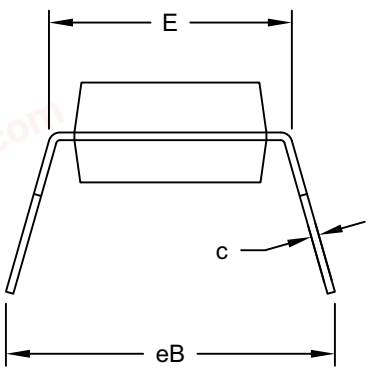


TOP VIEW





SIDE VIEW



END VIEW

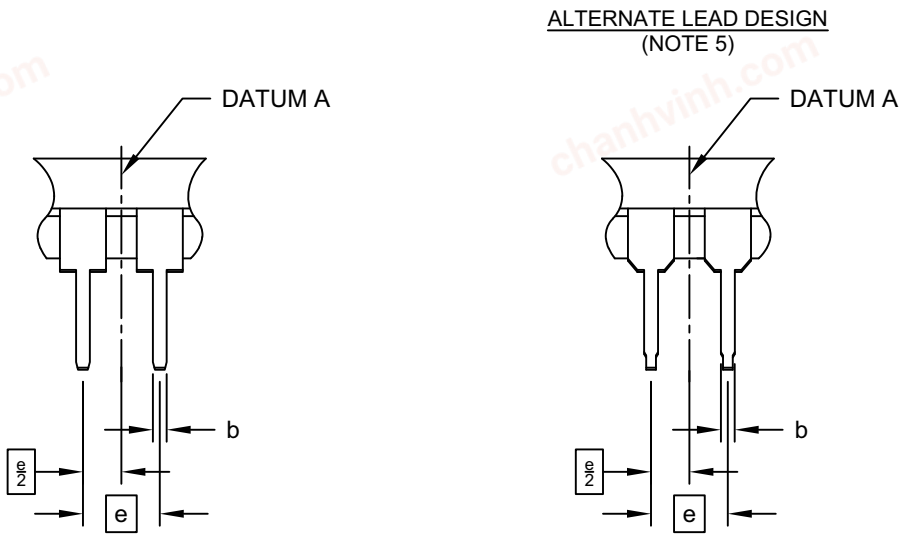
Microchip Technology Drawing No. C04-018-P Rev G Sheet 1 of 2

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8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

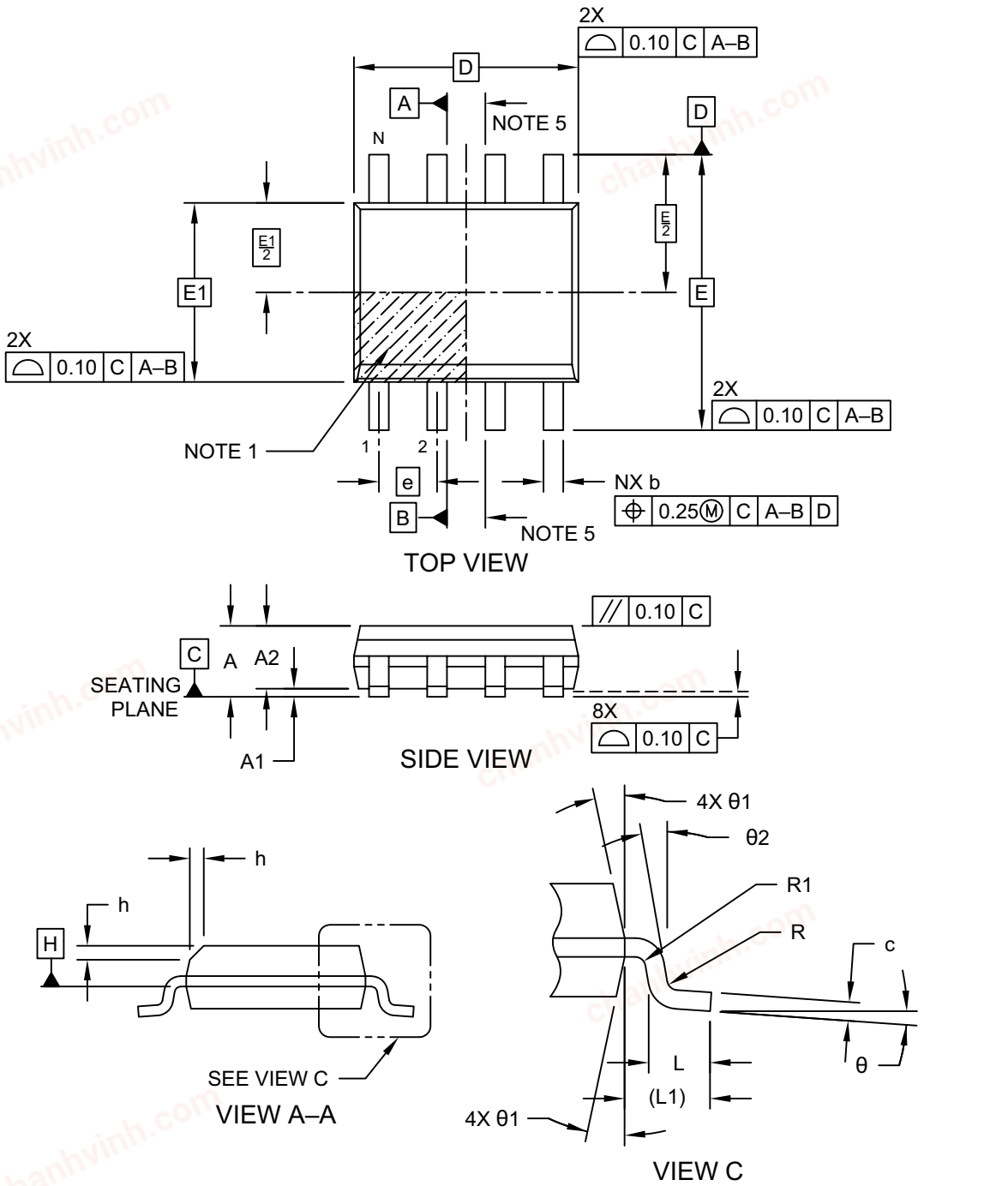
Microchip Technology Drawing No. C04-018-P Rev G Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

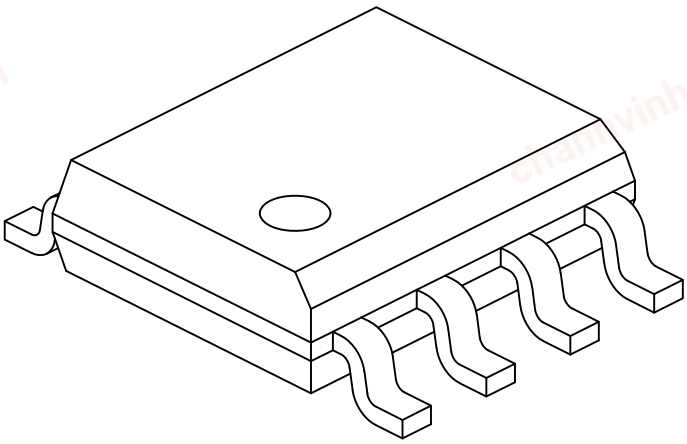


Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

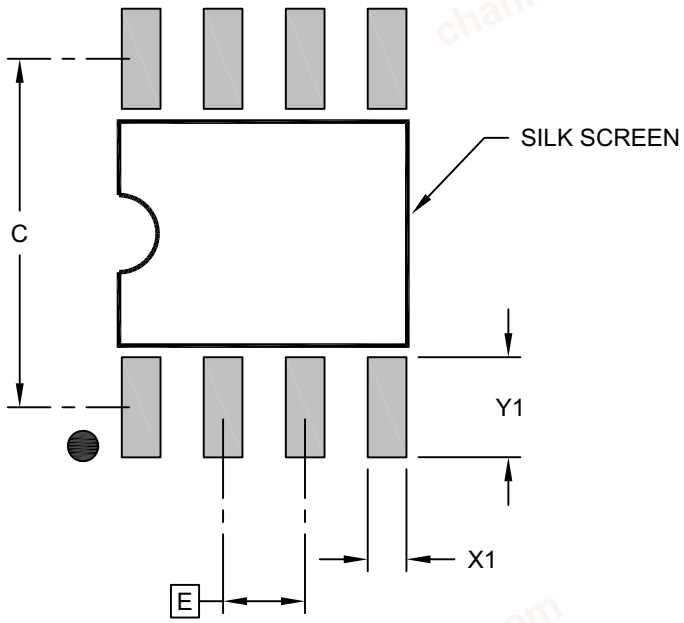
Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

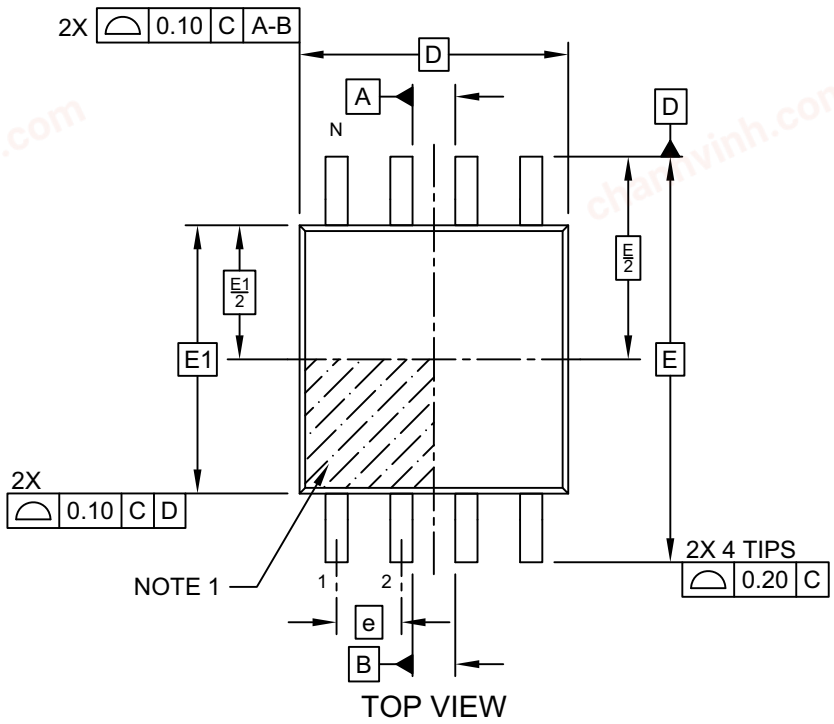
Microchip Technology Drawing C04-2057-SN Rev K

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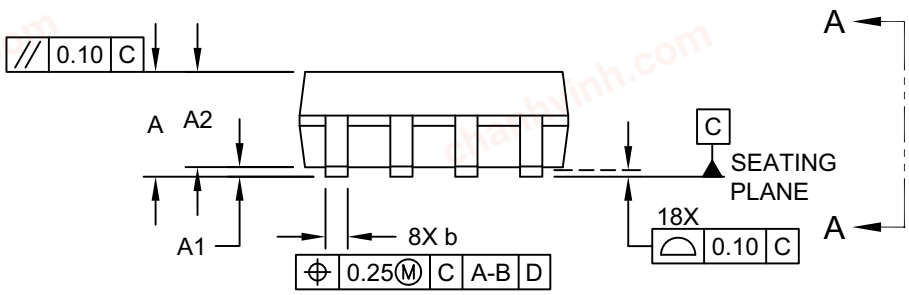
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8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

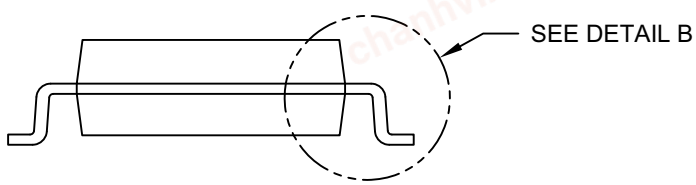
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A–A

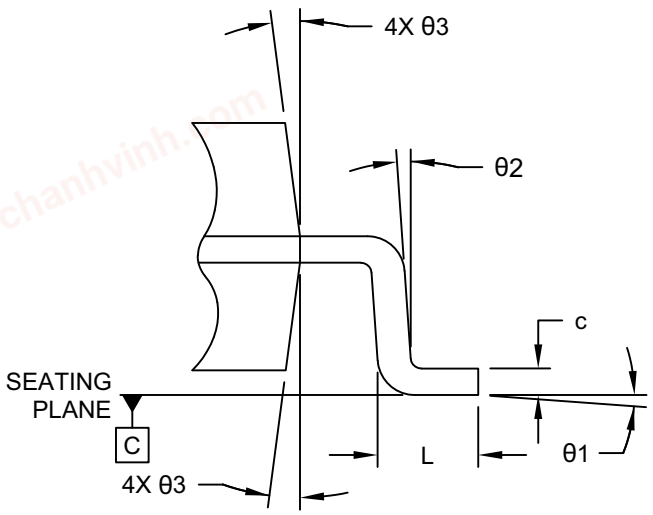
Microchip Technology Drawing C04-056 Rev E Sheet 1 of 2

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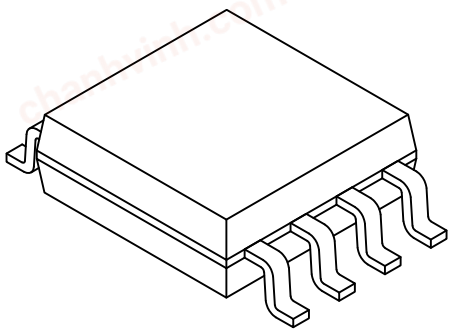
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8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.77	–	2.03
Standoff §	A1	0.05	–	0.25
Molded Package Thickness	A2	1.75	–	1.98
Overall Length	D		5.26 BSC	
Overall Width	E		7.94 BSC	
Molded Package Width	E1		5.25 BSC	
Terminal Width	b	0.36	–	0.51
Terminal Thickness	c	0.15	–	0.25
Terminal Length	L	0.51	–	0.76
Foot Angle	θ1	0°	–	8°
Lead Angle	θ2	0°	–	–
Mold Draft Angle	θ3	–	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. SOIJ – JEITA/EIAJ Standard, Formerly called SOIC
3. § – Significant Characteristic
4. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
5. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

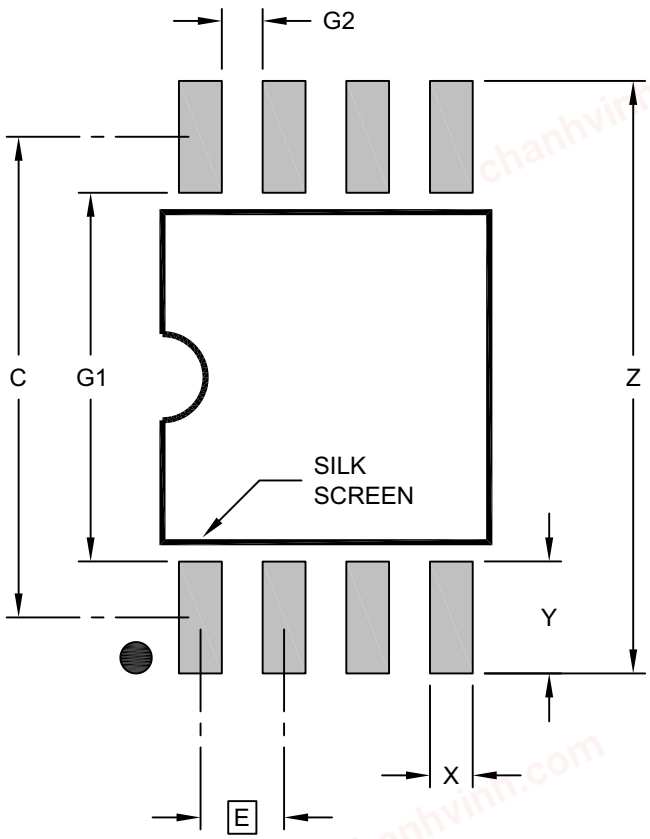
Microchip Technology Drawing C04-056 Rev E Sheet 2 of 2

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8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Overall Width	Z			9.00
Contact Pad Spacing	C		7.30	
Contact Pad Width (X8)	X			0.65
Contact Pad Length (X8)	Y			1.70
Contact Pad to Contact Pad (X4)	G1	5.60		
Contact Pad to Contact Pad (X6)	G2	0.62		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

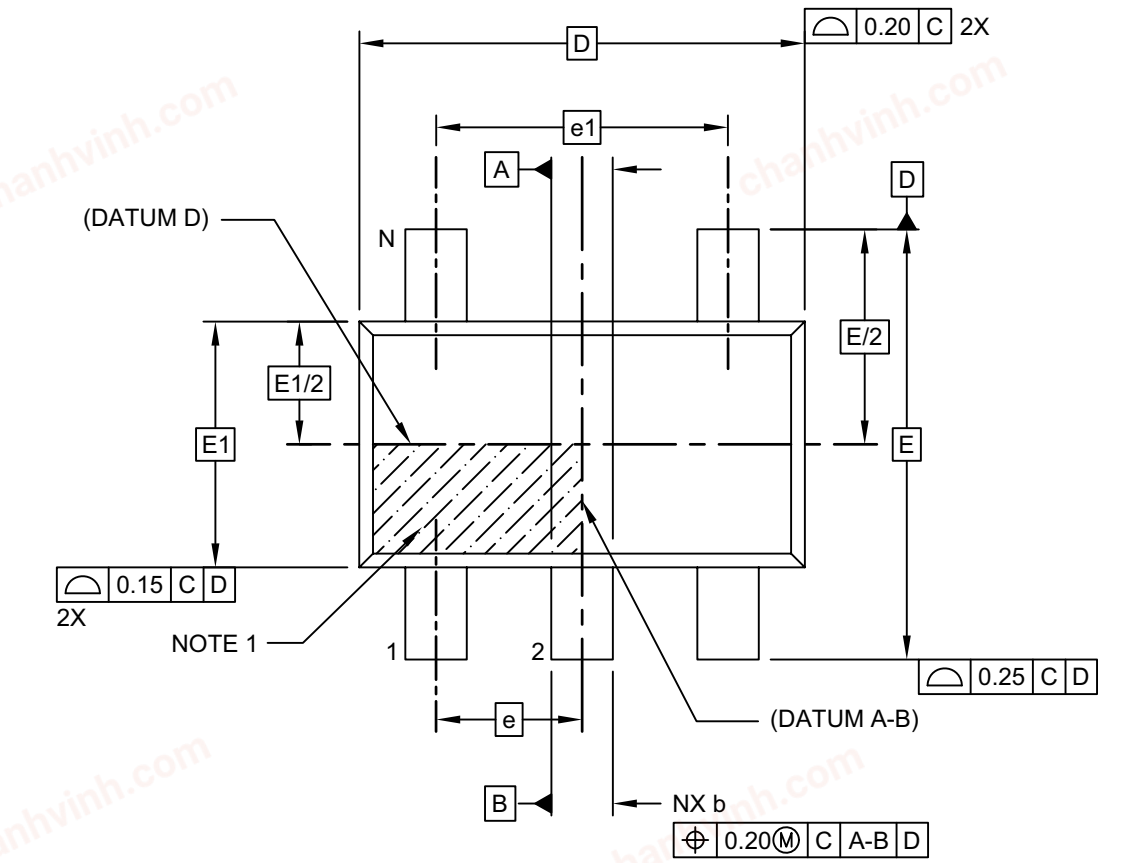
Microchip Technology Drawing C04-2056 Rev E

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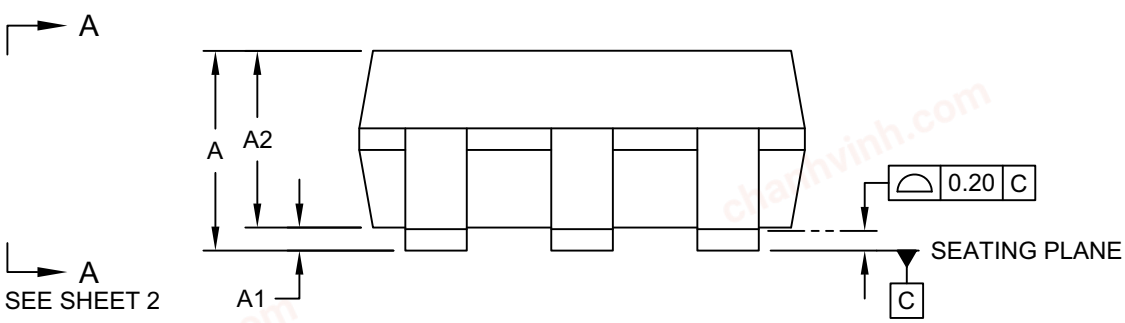
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5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



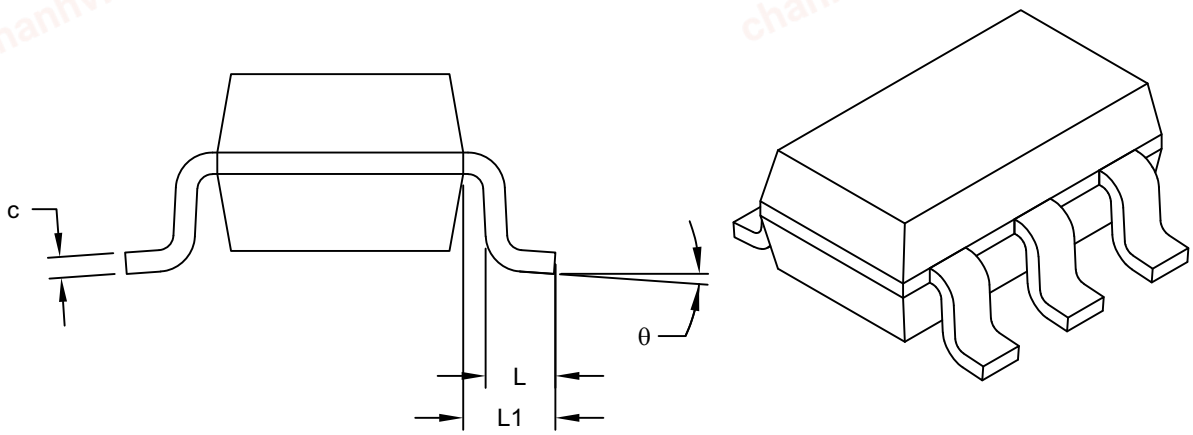
SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2

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5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

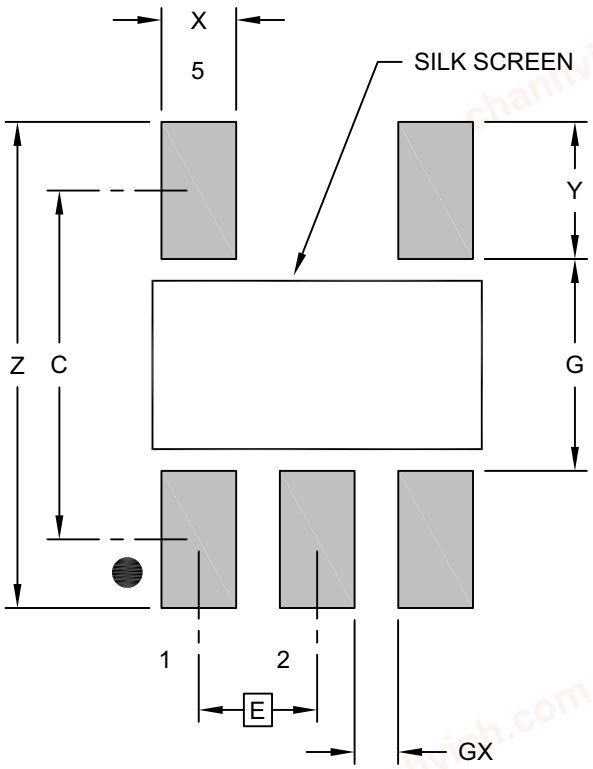
Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2

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5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

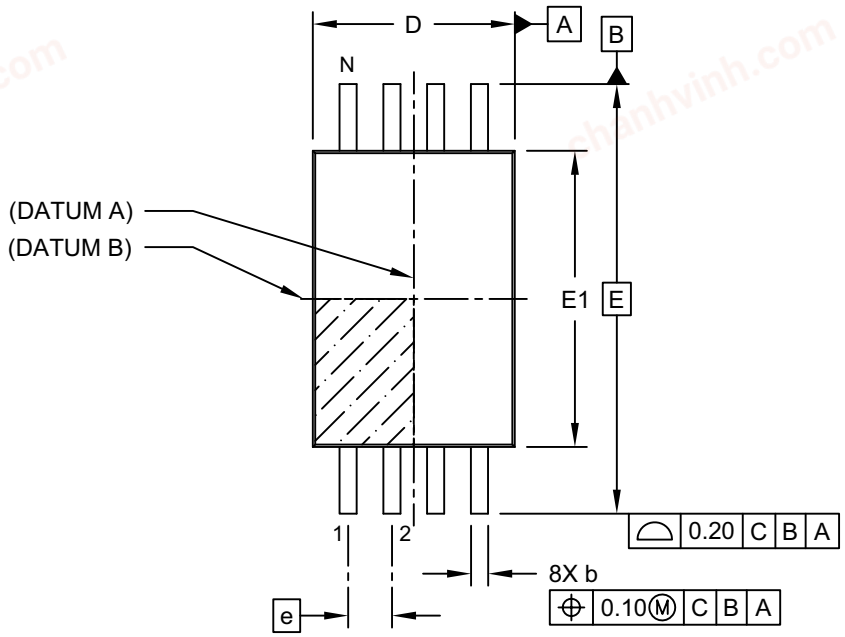
Microchip Technology Drawing No. C04-2091-OT Rev H

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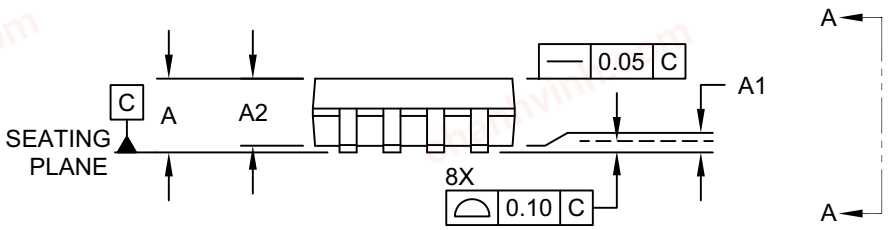
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8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

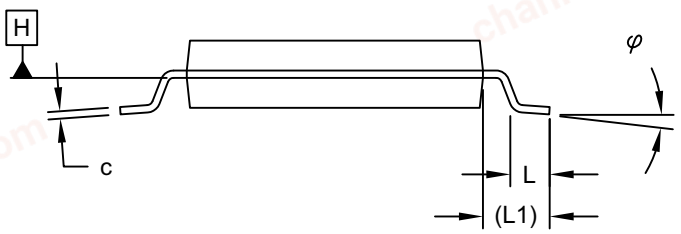
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



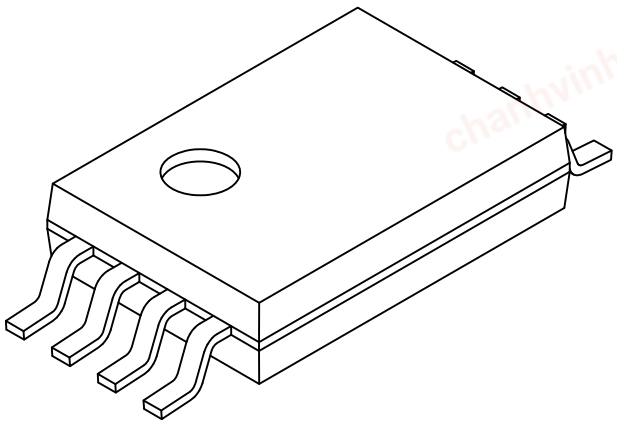
VIEW A-A

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8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	-
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

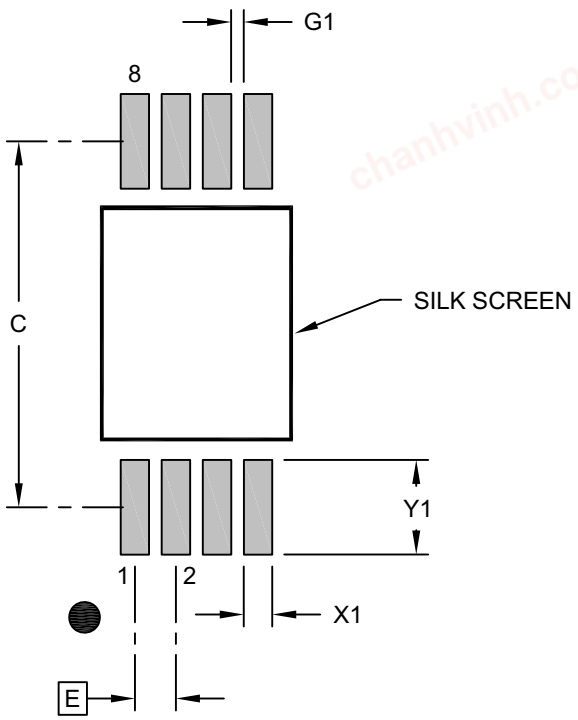
Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

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8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

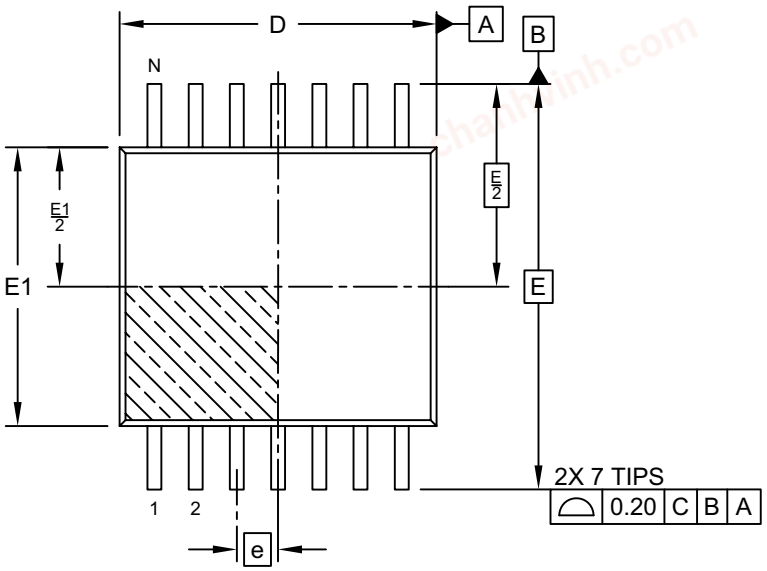
Microchip Technology Drawing C04-2086 Rev B

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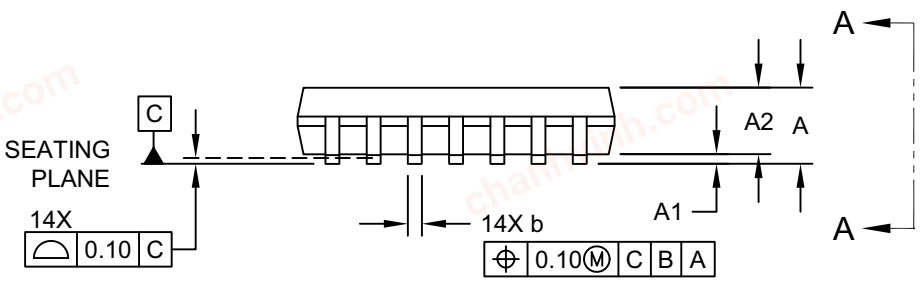
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14-Lead Plastic Thin Shrink Small Outline Package [ST] - 4.4 mm Body [TSSOP]

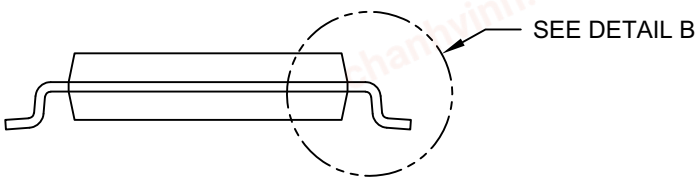
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



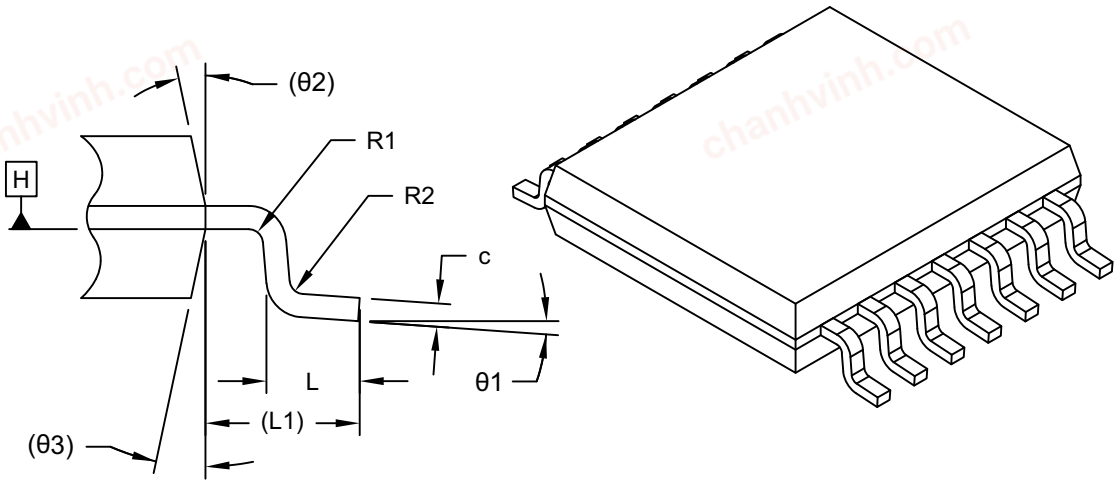
VIEW A–A

Microchip Technology Drawing C04-087-ST Rev F Sheet 1 of 2

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14-Lead Plastic Thin Shrink Small Outline Package [ST] - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

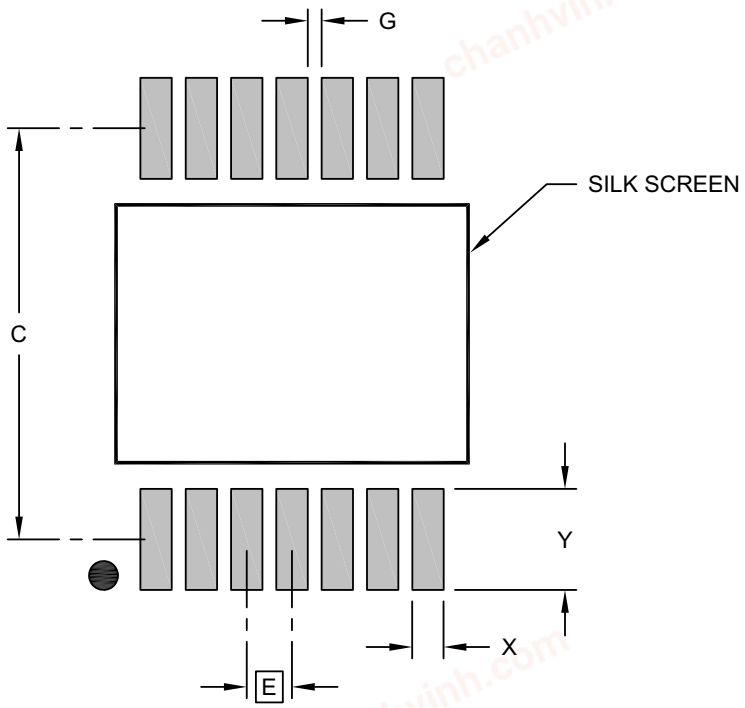
Microchip Technology Drawing C04-087-ST Rev F Sheet 2 of 2

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14-Lead Plastic Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		5.90	
Contact Pad Width (X14)	X			0.45
Contact Pad Length (X14)	Y			1.45
Contact Pad to Contact Pad (X12)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

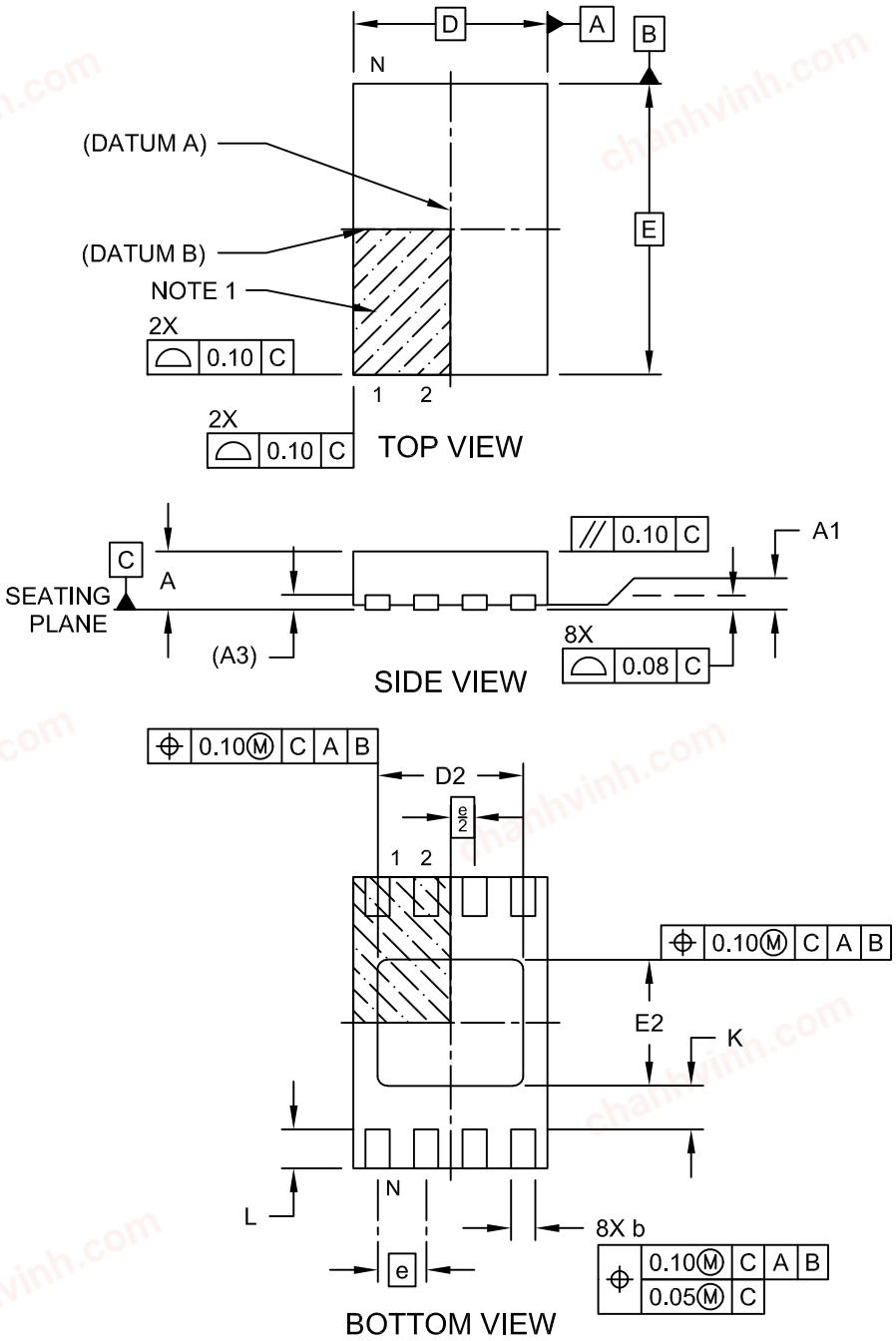
Microchip Technology Drawing C04-2087-ST Rev F

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8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



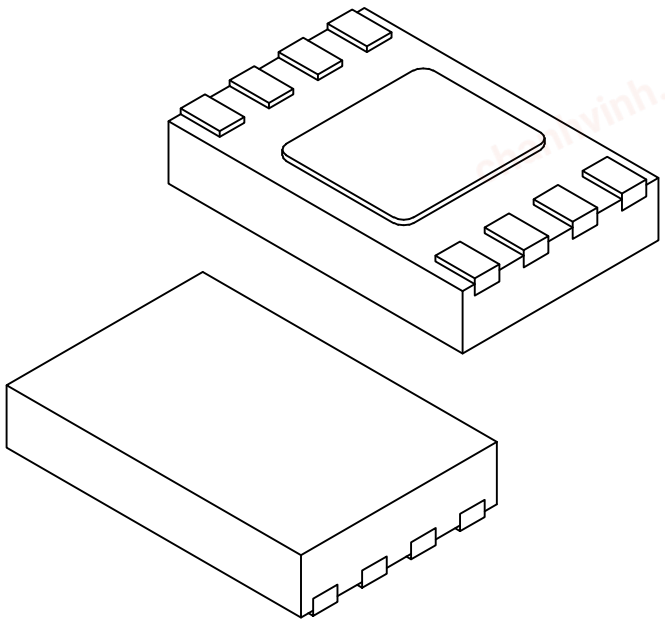
Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 1 of 2

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8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.25	0.35	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

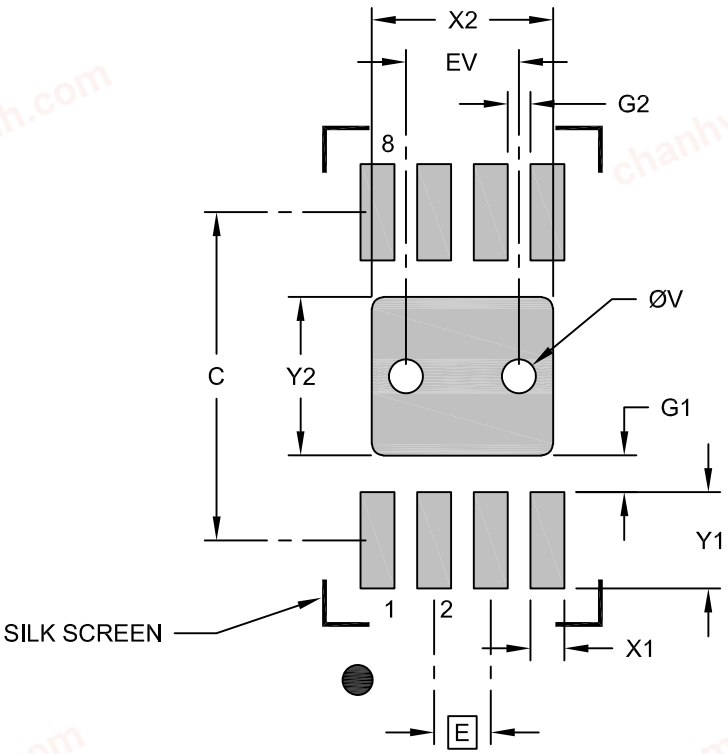
Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 2 of 2

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8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.33		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23355-Q4B Rev C

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APPENDIX A: REVISION HISTORY

Revision R (12/2024)

Updated 8-Lead UDFN and 5-Lead SOT-23 packages. Editorial updates throughout document.

Revision Q (02/2021)

Updated formatting to current template. Replaced terminology “Master” and “Slave” with “Host” and “Client” respectively. Added 8-Lead UDFN and 5-Lead SOT-23 package. Added Automotive Product Identification System.

Revision P (06/2015)

Updated ICCS; Removed TDFN and MSOP packages.

Revision N (11/2013)

Updated ICCS and added TDFN and MSOP packages.

Revision M (03/2010)

Added 8-Lead Chip Scale package.

Revision L (12/2009)

Added note to Section 6.1.

Revision K (06/2009)

Removed CMOS from title; Revised Table 1-2, Para. 18; Added SOIC and TSSOP packaging; Updated Pin Descriptions; Updated Product ID.

Revision J

Revised Table 1-2, AC Characteristics; Updated Packaging.

Revision H

Revised Features section; Revised 1.8V voltage to 1.7V; Replaced Package Drawings; Revised Product ID System; Removed 14 Lead TSSOP.

Revision G

Revised Sections 2.1, 2.4 and 6.3.

Revision F

Add E3 (Pb-free) to marking examples.
Updated Marking Legend and On-line Support.

Revision E

Correction to Section 1.0., Ambient Temperature.
Correction to Section 6.2, Page Write.

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PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	24AA512 =	512-Kbit 1.7V I^2C Serial EEPROM
	24LC512 =	512-Kbit 2.5V I^2C Serial EEPROM
	24FC512 =	512-Kbit 1 MHz I^2C Serial EEPROM
Tape and Reel Option:	Blank =	Standard packaging (tube or tray)
	T =	Tape and Reel(1)
Temperature Range:	I =	-40°C to +85°C (Industrial)
	E =	-40°C to +125°C (Extended)
Package:	P =	Plastic Dual In-Line - 300 mil Body, 8-lead (PDIP)
	SN =	Plastic Small Outline - Narrow, 3.90 mm Body, 8-lead (SOIC)
	SM =	Plastic Small Outline - Medium, 5.28 mm Body, 8-lead (SOIJ)
	ST =	Plastic Thin Shrink Small Outline - 4.4 mm, 8-lead (TSSOP)
	MF =	Plastic Dual Flat, No Lead Package - 5x6x0.85 mm Body, 8-lead (DFN-S)
	ST14 =	Plastic Thin Shrink Small Outline - 4.4 mm, 14-lead (TSSOP)
	Q4B =	Plastic Dual Flat, No Lead Package - 2x3x0.6 mm Body, 8-lead (UDFN)
	OT =	Plastic Small Outline Transistor, 5-lead (SOT-23) (Tape and Reel only)
	CS17K(2) =	Chip Scale, 8-lead (CSP)

Examples:

a) 24AA512-I/P: Industrial Temp., 1.7V, PDIP package.

b) 24AA512T-I/SM: Tape and Reel, Industrial Temp., 1.7V, SOIJ package.

c) 24AA512-I/MF: Industrial Temp., 1.7V, DFN package.

d) 24LC512-E/P: Extended Temp., 2.5V, PDIP package.

e) 24LC512-I/SN: Industrial Temp., 2.5V, SOIC package.

f) 24LC512T-I/SM: Tape and Reel, Industrial Temp., 2.5V, SOIJ package.

g) 24LC512-I/ST: Industrial Temp., 2.5V, TSSOP package.

h) 24FC512-I/P: Industrial Temp., 1.7V, High Speed, PDIP package.

i) 24FC512-I/SM: Industrial Temp., 1.7V, High Speed, SOIJ package.

j) 24FC512T-I/SN: Tape and Reel, Industrial Temp., 1.7V, High Speed, SOIC package.

k) 24AA512T-I/CS17K: Tape and Reel, Industrial Temp., 1.7V, Chip Scale package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: "17K" indicates 160K technology.

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PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX	XXX(2,3)
Device	Tape and Reel Option	Temperature Range	Package	Variant

Device:	24LC512 =	512-Kbit 2.5V I^2C Serial EEPROM
	24FC512 =	512-Kbit 1MHz I^2C Serial EEPROM
Tape and Reel Option:	Blank =	Standard packaging (tube or tray)
	T =	Tape and Reel(1)
Temperature Range:	I	= -40°C to +85°C AEC-Q100 Grade 3
	E	= -40°C to+125°C AEC-Q100 Grade 1
Package:	SM =	Plastic Small Outline – Medium, 5.28 mm Body, 8-Lead (SOIJ)
	SN =	Plastic Small Outline – Narrow, 3.90 mm Body, 8-Lead (SOIC)
	ST =	Plastic Thin Shrink Small Outline – 4.4 mm, 8-Lead (TSSOP)
Variant(2,3):	16KVAO =	Standard Automotive, 16K Process
	16KVXX =	Customer-Specific Automotive, 16K Process

Examples:

a) 24LC512T-E/SN16KVAO: Tape and Reel, Automotive Grade 1, 2.5V, SOIC Package.

b) 24LC512-E/ST16KVAO: Automotive Grade 1, 2.5V, TSSOP Package.

c) 24FC512-E/SN16KVAO: Automotive Grade 1, 1.7V, SOIC Package.

d) 24FC512T-E/ST16KVAO: Tape and Reel, Automotive Grade 1,1.7V, TSSOP Package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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