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19-3251; Rev 1; 6/06

EVALUATION KIT AVAILABLE

200Mbps SFP Limiting Amplifier

MAX3969

General Description

The MAX3969 limiting amplifier with PECL data outputs is ideal for low-cost ATM, Fast Ethernet, FDDI and ESCON fiber optic receivers.

The MAX3969 features 1mVP-P input sensitivity and an integrated power detector that senses the input signal power. It provides a received-signal-strength indicator (RSSI), which is an analog indication of the power level. Signal strength is also indicated by the complementary TTL loss-of-signal (LOS) outputs and the PECL signal-detect (SD) output, both of which indicate the power level relative to a programmable threshold.

The threshold can be adjusted to detect signal amplitudes as low as 2.7mVP-P. An optional squelch function disables switching of the data outputs by holding them at a known state when the signal is below the programmed threshold.

The MAX3969 is available in die form and a 4mm x 4mm, 20-pin thin QFN package.

Applications

SFP/SFF Transceivers

Fast Ethernet/FDDI Transceivers

155Mbps LAN ATM Transceivers

ESCON Receivers

FTTx Transceivers

Features

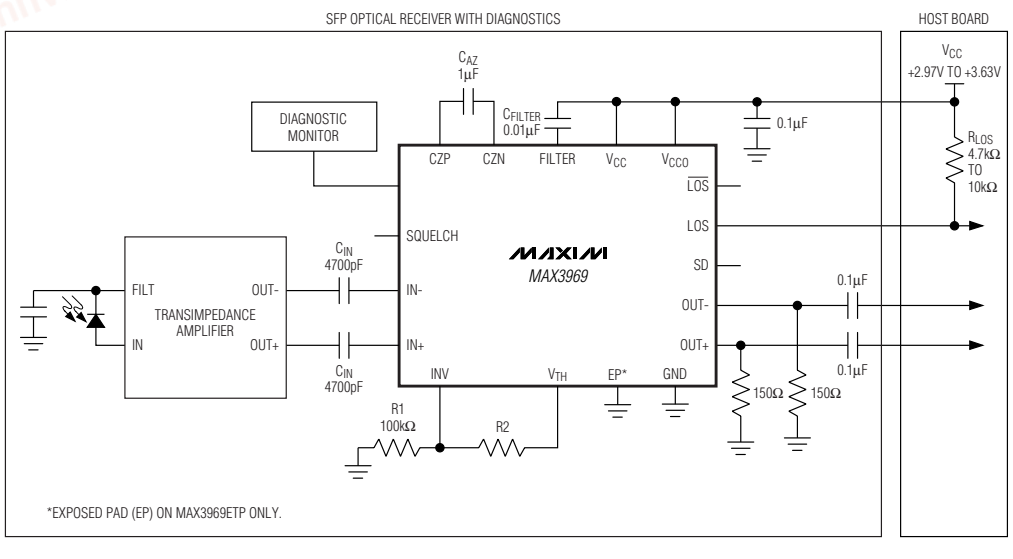
- ♦ 1mVP-P Input Sensitivity
- ♦ Loss-of-Signal Detector with Programmable Threshold
- ♦ TTL LOS and PECL Signal Detect
- ♦ Analog Received-Signal-Strength Indicator
- ♦ Output Squelch Function
- ♦ Compatible with 4B/5B Data Coding

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3969ETP	-40°C to +85°C	20 Thin QFN	T2044-2
MAX3969E/D	—	Dice*	—

*Dice are designed to operate over a -40°C to +100°C junction temperature (T_J) range, but are tested and guaranteed only at T_A = +25°C.

Typical Application Circuits



Typical Application Circuits continued at end of data sheet.

Pin Configuration appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage Range (V_{CC}, V_{CCO}) .....-0.5V to +7.0V
Voltage at FILTER, RSSI, IN+, IN-, CZP, CZN, SQUELCH, INV, V_{TH}.....-0.5V to (V_{CC} + 0.5V)
TTL Output Current (LOS, $\overline{LOS}$) .....±9mA
PECL Output Current (OUT+, OUT-, SD) .....±50mA
Differential Voltage Between CZP and CZN.....-1.5V to +1.5V
Differential Voltage Between IN+ and IN- .....-1.5V to +1.5V

Continuous Power Dissipation (T_A = +85°C)
20-Pin Thin QFN (derate 16.9mW/°C above +85°C) 1099mW
Operating Junction Temperature Range (die).....-40°C to +150°C
Die Attach Temperature.....+400°C
Storage Temperature Range .....-50°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +5.5V, PECL outputs terminated with 50Ω to V_{CC} - 2V, R1 = 100kΩ, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	PECL outputs open		22	45	mA
LOS Hysteresis	Input = 4.0mV$_{P-P}$ (Note 2)	3.0	5	8.0	dB
Squelch Input Current			27	100	µA
PECL Output-Voltage High	(Note 3)	-1085		-880	mV
PECL Output-Voltage Low	(Note 3)	-1830		-1550	mV
LOS Assert Accuracy	Input = 7mV$_{P-P}$ or 90mV$_{P-P}$, 0°C to +85°C	-3.0		+3.0	dB
	Input = 7mV$_{P-P}$ or 90mV$_{P-P}$, -40°C to +85°C	-3.6		+3.6	dB
Minimum LOS Assert Input				2.7	mV$_{P-P}$
Maximum LOS Deassert Input		143			mV$_{P-P}$
Input Sensitivity	(Note 4)		1	4	mV$_{P-P}$
Input Overload	(Note 4)	1500			mV$_{P-P}$
TTL Output High	R_{LOS} = 4.7kΩ to 10kΩ	2.4	3.0		V
TTL Output Leakage	(Note 5)		1	20	µA
TTL Output Low	I_{OL} = 800µA		0.2	0.5	V
Data Output Transition Time	20% to 80%, Input > 4mV$_{P-P}$ (Note 4)	0.35	0.8	1.20	ns
Pulse-Width Distortion	Input > 4mV$_{P-P}$ (Notes 4, 6)		50	250	ps
LOS, SD Assert/Deassert Time	C_{FILTER} = 0.01µF		10		µs

Note 1: Dice are tested and guaranteed only at T_A = +25°C.
Note 2: LOS hysteresis = 20log($V_{LOS-DEASSERT}$ / $V_{LOS-ASSERT}$).
Note 3: Relative to supply voltage (V_{CCO}).
Note 4: AC characteristics are guaranteed by design and characterization.
Note 5: Input < LOS threshold (LOS = HIGH), V_{LOS} = 2.4V.
Note 6: Pulse-width distortion = [(width of wider pulse) - (width of narrower pulse)] / 2, measured with 100Mbps 1-0 pattern.

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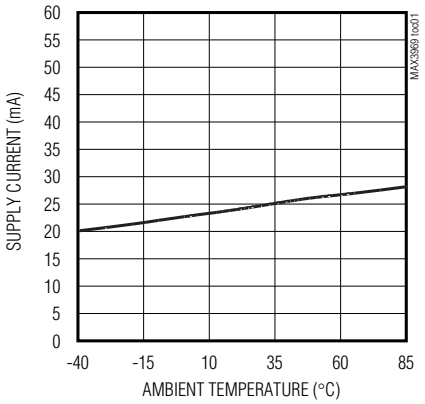
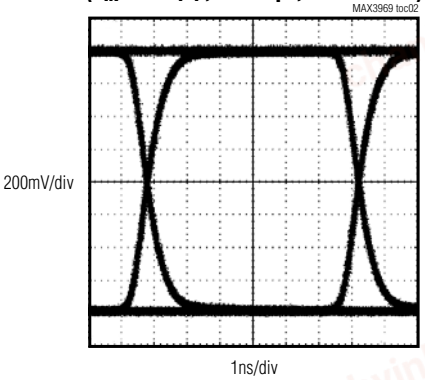
Typical Operating Characteristics

(V_{CC} = +3.3V, PECL outputs terminated with 50Ω to V_{CC} - 2V, R1 = 100kΩ, T_A = +25°C, unless otherwise noted.)

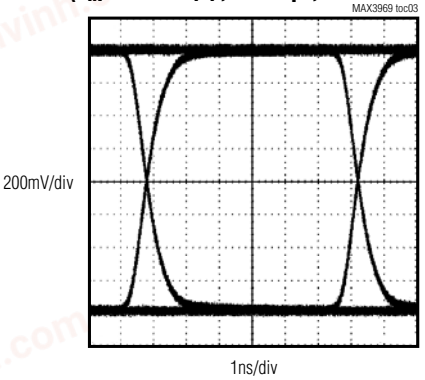
SUPPLY CURRENT vs. TEMPERATURE (PECL OUTPUTS OPEN)



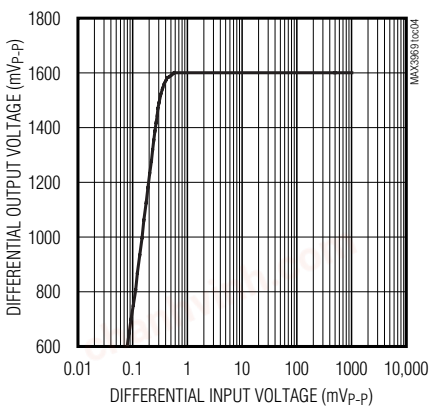
OUTPUT EYE DIAGRAM (V_{IN} = 2mV$_{P-P}$, 155Mbps, 2^{23} - 1 PRBS)



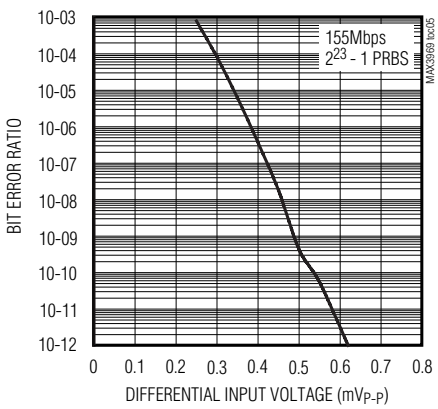
OUTPUT EYE DIAGRAM (V_{IN} = 1500mV$_{P-P}$, 155Mbps, 2^{23} - 1 PRBS)



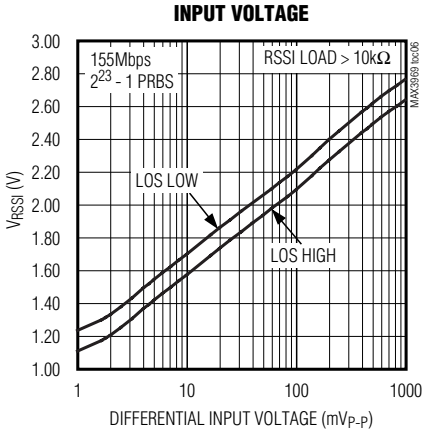
TRANSFER FUNCTION



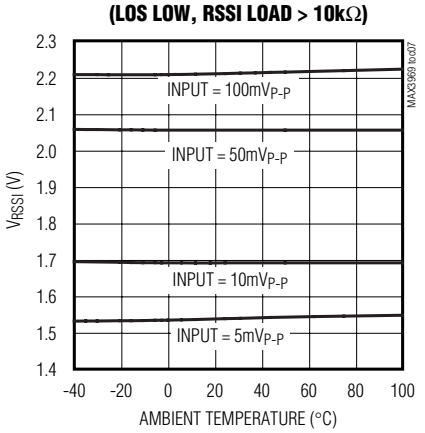
BIT ERROR RATIO vs. DIFFERENTIAL INPUT VOLTAGE



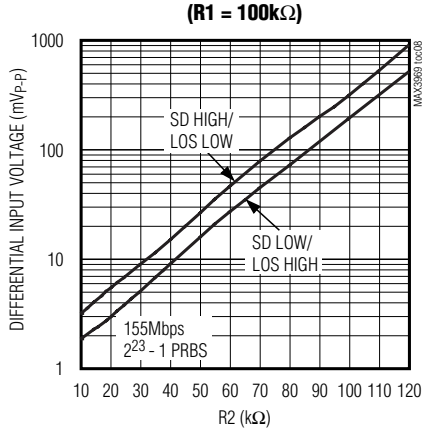
RSSI VOLTAGE vs. DIFFERENTIAL INPUT VOLTAGE



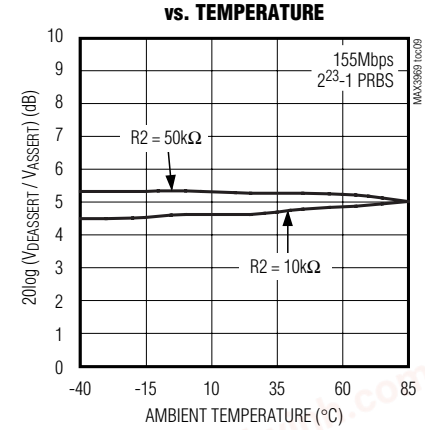
RSSI VOLTAGE vs. TEMPERATURE (LOS LOW, RSSI LOAD > 10kΩ)



POWER-DETECT THRESHOLD vs. R2 (R1 = 100kΩ)



LOSS-OF-SIGNAL HYSTERESIS vs. TEMPERATURE



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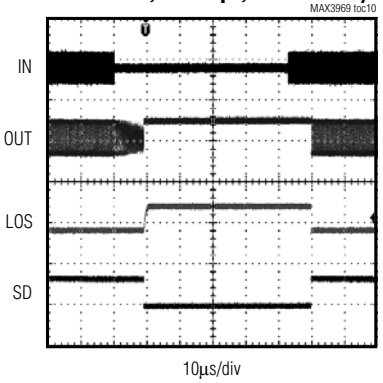
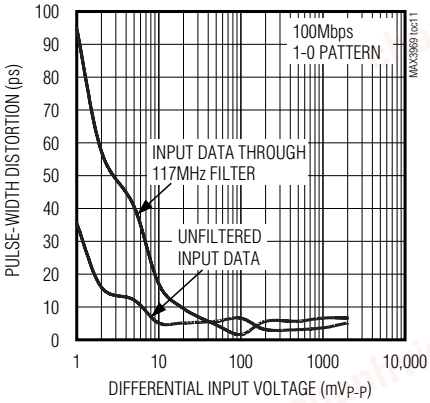
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, PECL outputs terminated with 50Ω to V_{CC} - 2V, R1 = 100kΩ, T_A = +25°C, unless otherwise noted.)

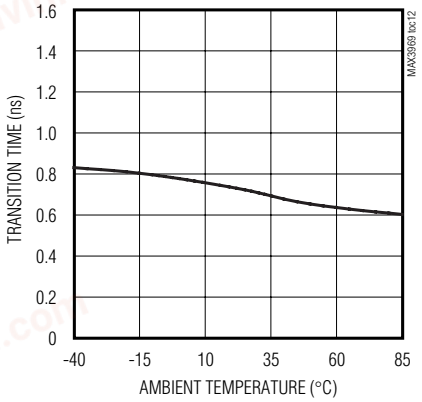
POWER-DETECT TIMING WITH SQUELCH (INPUT = 12mV$_{P-P}$, C_{FILTER} = 0.01µF, R2 = 15kΩ, 155Mbps, 2^{23} - 1 PRBS)



PULSE-WIDTH DISTORTION vs. DIFFERENTIAL INPUT VOLTAGE



DATA OUTPUT TRANSITION TIME vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	INV	Inverting Input of Internal Op Amp that Sets Power-Detect Threshold Voltage (Figure 1). Connect a resistor from V_{TH} to INV (R2), and from INV to ground (R1 = 100kΩ), to program the desired threshold voltage.
2	FILTER	Filter Output of Logarithmic Full-Wave Detectors (FWDs). The FWD outputs are summed together at FILTER to generate the RSSI output. Connect a capacitor from FILTER to V_{CC} for proper operation.
3	RSSI	Received-Signal-Strength Indicator Output. The voltage at RSSI indicates the input-signal power. The RSSI output is reduced approximately 120mV when LOS is asserted.
4	IN-	Inverting Data Input
5	IN+	Noninverting Data Input
6 , 7, 8	GND	Ground
9	CZP	Autozero Capacitor Input. Connect a capacitor between CZP and CZN.
10	CZN	Autozero Capacitor Input. Connect a capacitor between CZP and CZN.
11	V_{CCO}	Output-Buffer Supply Voltage. Connect to the same potential as V_{CC}.
12	OUT+	Noninverting PECL Data Output. Terminate with 50Ω to (V_{CC} - 2V).
13	OUT-	Inverting PECL Data Output. Terminate with 50Ω to (V_{CC} - 2V).
14	SD	Signal Detect, PECL Output. The SD output is high when input power is above the power-detect threshold, and low when input power is below the power-detect threshold. This pin is PECL-compatible and should be terminated with 50Ω to (V_{CC} - 2V) or equivalent.
15	LOS	Loss-of-Signal Output, TTL Open Collector (with ESD Protection). The LOS output is high when input power is below the power-detect threshold, and low when input power is above the power-detect threshold.
16	$\overline{LOS}$	Inverted Loss-of-Signal Output, TTL Open Collector (with ESD Protection). The $\overline{LOS}$ output is low when input power is below the power-detect threshold, and high when input power is above the power-detect threshold.

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Pin Description

PIN	NAME	FUNCTION
17, 18	V_{CC}	Supply Voltage
19	SQUELCH	Squelch Input. The squelch function disables the data outputs by forcing OUT- low and OUT+ high when the signal is below the power-detect threshold. Connect to GND or leave unconnected to disable squelch. Connect to V_{CC} to enable squelch.
20	V_{TH}	Output of Internal Op Amp that Sets Power-Detect Threshold Voltage (Figure 1). Connect a resistor from V_{TH} to INV (R2) and from INV to ground (R1 = 100kΩ), to program the desired threshold voltage.
EP	Exposed Pad	Ground. The exposed pad must be soldered to the circuit board ground for proper thermal and electrical performance.

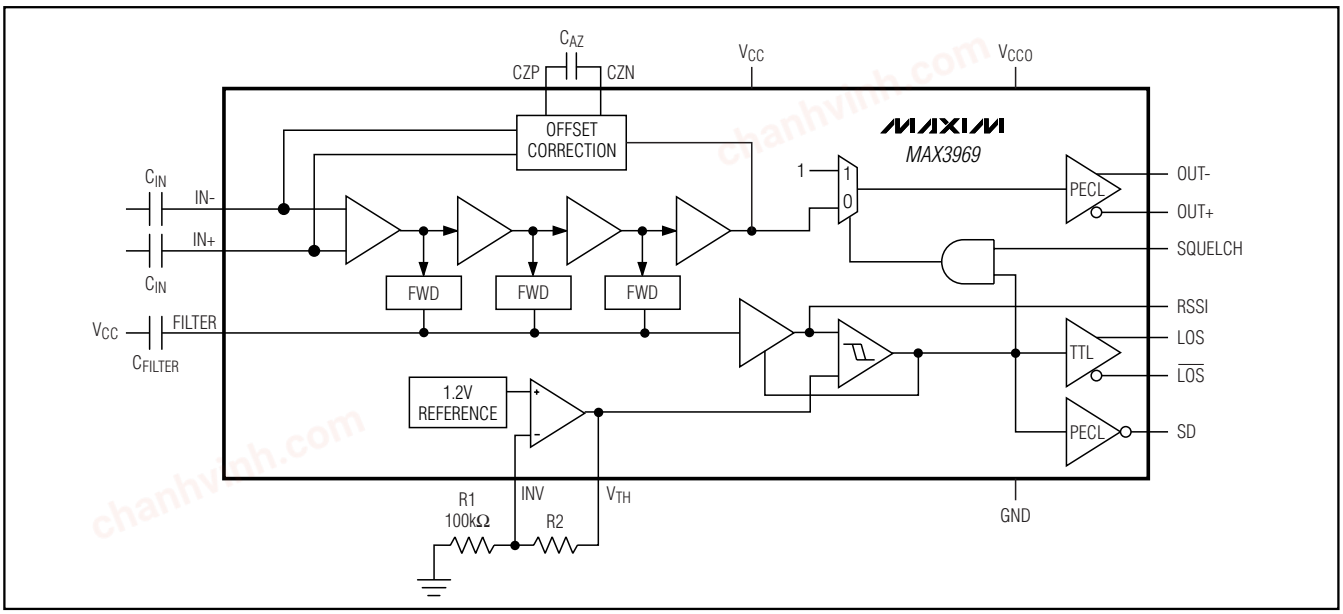

Figure 1. Functional Diagram

Detailed Description

The MAX3969 contains a series of limiting amplifiers and power detectors, offset correction, data-squelch circuitry, TTL buffers for LOS outputs, and PECL output buffers for signal detect (SD) and data outputs. See Figure 1 for the functional diagram.

Gain Stages and Offset Correction

A cascade of limiting amplifiers provides approximately 65dB of combined small-signal gain. The large gain makes the amplifier susceptible to small DC offsets in the signal path. To correct DC offsets, the amplifier has an internal feedback loop that acts as a DC autozero circuit. By correcting the DC offsets, the limiting amplifier sensitivity and power-detector accuracy are improved.

The offset correction is optimized for data streams with a 50% duty cycle. A different average duty cycle results in increased pulse-width distortion and loss of sensitivity. The offset-correction circuitry is less sensitive to variations of input duty cycle (for example, the 40% to 60% duty cycle encountered in 4B/5B coding) when the input is less than 30mVP-P.

The data inputs must be AC-coupled for the offset correction loop to function properly. Differential input impedance is >5kΩ.

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Power Detector

Each amplifier stage contains a logarithmic FWD, which indicates the RMS input signal power. The FWD outputs are summed together at the FILTER pin where the signal is filtered by an external capacitor (C_{FILTER}) connected between FILTER and V_{CC}. The FILTER signal generates the RSSI output voltage (V_{RSSI}), which is proportional to the input power in decibels. When LOS is low, V_{RSSI} is approximated by the following equation:

$$V_{RSSI}\ (V) = 1.2V + 0.5\log\ (V_{IN})$$

where, V_{IN} is the data input voltage measured in mV_{P-P}.

This relation translates to a 25mV increase in V_{RSSI} for every 1dB increase in V_{IN}. The RSSI output is reduced approximately 120mV when LOS is high.

Typically the RSSI output is connected to an A/D converter for diagnostic monitoring. This output can be left open if not required in the application. The RSSI output is designed to drive a minimum load resistance of 10kΩ to ground, and a maximum capacitance of 10pF. A 10kΩ series resistor is required to buffer loads greater than 10pF.

Signal-Strength Comparator

A comparator is used to indicate the input signal strength relative to a user-programmable threshold. One of the comparator inputs is connected to the RSSI output signal, and the other is connected to the threshold voltage (V_{TH}), which is set externally and provides a trip point for signal-strength indication. When the signal strength is above the threshold, the SD output asserts high and the LOS output deasserts low. Likewise, when the signal strength falls below the threshold, SD deasserts low and LOS asserts high. To ensure chatter-free operation, the comparator is designed with approximately 5dB of hysteresis.

Squelch

The squelch function disables the data outputs by forcing OUT- low and OUT+ high when the input signal is below the programmed threshold. This function ensures that when there is a loss of signal, the limiting amplifier and all downstream devices do not respond to input noise. Connect SQUELCH to GND or leave it unconnected to disable squelch. Connect SQUELCH to V_{CC} to enable squelch.

PECL Outputs

The data outputs (OUT+, OUT-) and signal-detect output (SD) are supply-referenced PECL outputs. See Figure 2 for the equivalent output circuit.

Both data outputs must be terminated for proper operation, but the SD output can be left open if not required in the application. The proper termination for a PECL output is 50Ω to (V_{CC} - 2V), but other standard termination techniques can be used. For more information on PECL terminations and how to interface with other logic families, refer to Maxim Application Note *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

TTL Outputs

The LOS outputs (LOS, $\overline{LOS}$) are implemented with open-collector, Schottky-clamped, ESD-protected, TTL-compatible outputs. See Figure 3 for the equivalent output circuit. The LOS outputs require external pullup resistors for proper operation. Resistor values between 4.7kΩ and 10kΩ are recommended.

If the LOS outputs are not required for the application, they can be left open.

Design Procedure

Program the Power-Detect Threshold

The suggested procedure for setting the power-detect threshold is given below and is illustrated in Figure 4.

1) Determine the maximum receiver sensitivity (RX_MAX) in dBm and the PIN-TIA responsivity (G) in V/W.
2) Calculate the differential voltage swing (VIN_SEN) at the MAX3969 inputs while operating at sensitivity.

$$V_{IN_SEN} = 10^{(RX_MAX\ /\ 10)} \times 2 \times G$$

3) Calculate the threshold voltage (V_{IN_TH}) at which LOS must be low (SD must be high) by allowing 3.6dB (1.8dB optical) margin for power-detector accuracy.

$$V_{IN_TH} = V_{IN_SEN} \times 0.66$$

4) Use V_{IN_TH} and the line labeled (SD HIGH / LOS LOW) in the Power-Detect Threshold vs. R2 graph in the *Typical Operating Characteristics* to determine the value of R2. Select R1=100kΩ.

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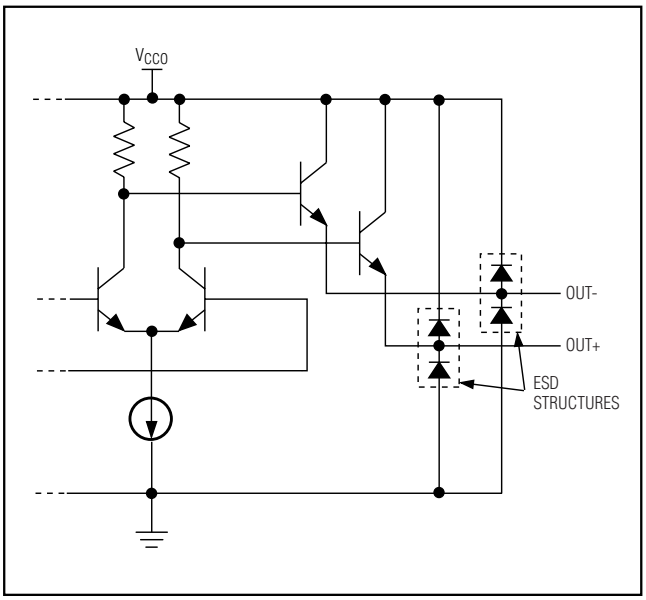

Figure 2. Equivalent PECL Output Circuit

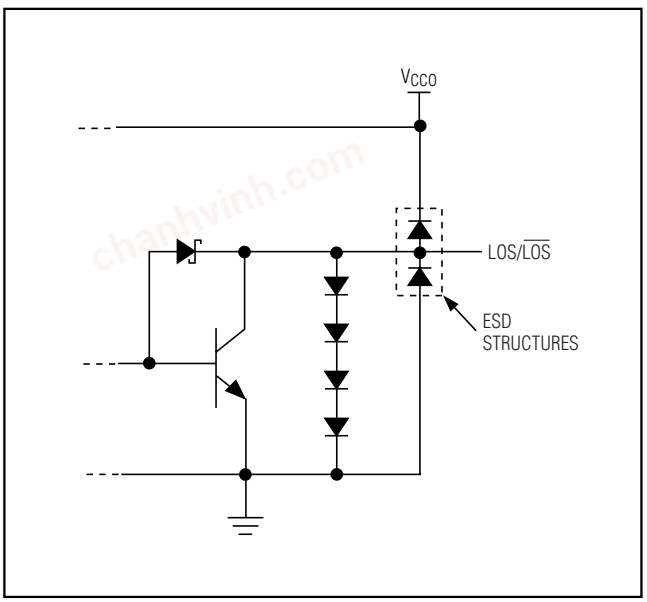

Figure 3. Equivalent TTL Output Circuit

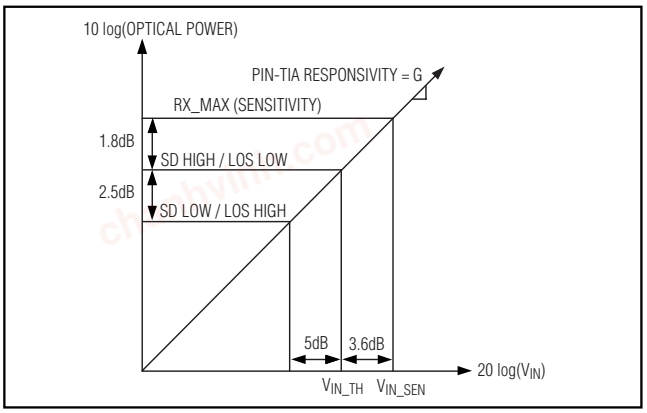

Figure 4. Signal Levels for Power-Detect Threshold

Select C_{FILTER}

For SFP/SFF, FDDI, 155Mbps ATM LAN, Fast Ethernet, and ESCON receivers, Maxim recommends C_{FILTER} = 0.01µF. This capacitor value ensures chatter-free LOS/SD and provides a typical assert/deassert time of 10µs. For other applications, the value of C_{FILTER} can be calculated using the following equation:

$$C_{FILTER} = \tau / 825\Omega$$

where τ is the desired time constant of the power detector.

Select C_{AZ} and C_{IN}

External-coupling capacitors (C_{IN}) are required on the data inputs for the offset correction loop to function properly. The offset correction loop bandwidth is determined by the external capacitor (C_{AZ}) connected between CZP and CZN. The poles associated with C_{IN} and C_{AZ} must work together to provide a flat response at the lower -3dB corner frequency. For SFP/SFF, FDDI, 155Mbps ATM LAN, Fast Ethernet, and ESCON receivers, Maxim recommends the following:

$$C_{IN} = 4700pF$$

$$C_{AZ} = 1\mu F$$

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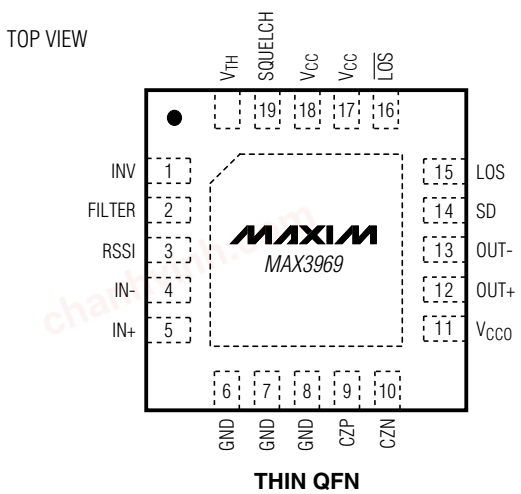
Applications Information

Wire Bonding

For high-current density and reliable operation, the MAX3969 uses gold metalization. For best results, use gold-wire ball-bonding techniques. Use caution if attempting wedge bonding. Die pad size is 4 mils x 4 mils. Die thickness is 16 mils.

Table 1 lists the bond pad coordinates for the MAX3969. The origin for pad coordinates is defined as the bottom left corner of the bottom left pad. All pad locations are referenced from the origin and indicate the center of the pad where the bond wire should be connected. Refer to Maxim Application Note HFAN-08.0.1: *Understanding Bonding-Coordinates and Physical Die Size* for detailed information.

Pin Configuration



THIN QFN

CONNECT EXPOSED PAD (EP) TO CIRCUIT BOARD GROUND.

Table 1. Bond Pad Coordinates

PAD	NAME	COORDINATES (µm)	
		X	Y
1	INV	46.6	659.5
2	FILTER	46.6	505.6
3	RSSI	46.6	351.7
4	IN-	46.6	197.8
5	IN+	46.6	46.6
6	GND	195.1	-99.1
7	GND	432.7	-99.1
8	GND	589.3	-99.1
9	CZP	743.2	-99.1
10	CZN	945.7	-99.1
11	V_{CCO}	1204.9	-96.4
12	OUT+	1204.9	81.7
13	OUT-	1204.9	262.6
14	SD	1204.9	492.1
15	LOS	1204.9	697.3
16	$\overline{LOS}$	1053.7	818.8
17	V_{CC}	808.0	818.8
18	V_{CC}	586.6	818.8
19	SQUELCH	432.7	818.8
20	V_{TH}	195.1	818.8

Chip Information

TRANSISTOR COUNT: 915

SUBSTRATE CONNECTED TO GND

PROCESS: Silicon Bipolar

DIE THICKNESS: 16 mils

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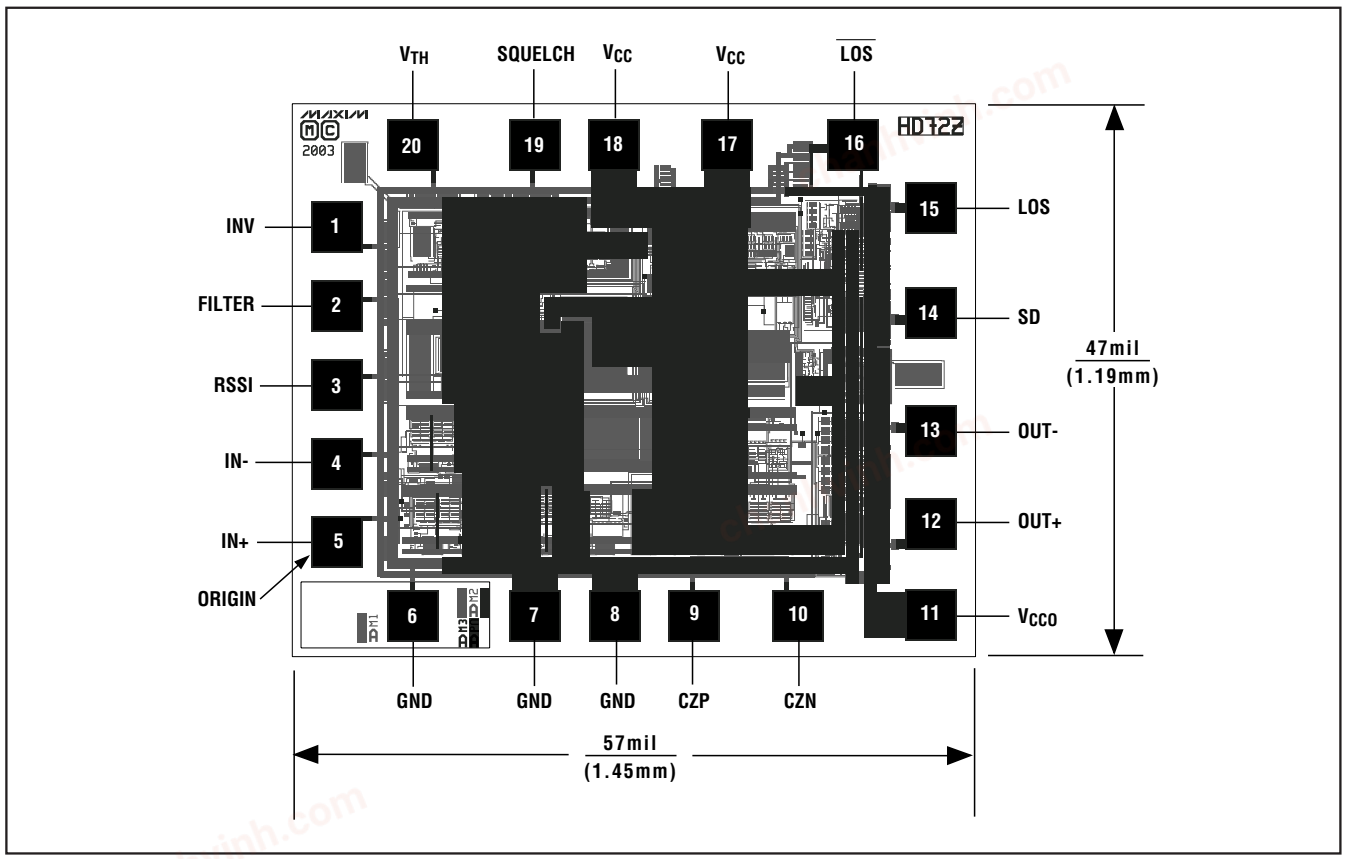
Chip Topography



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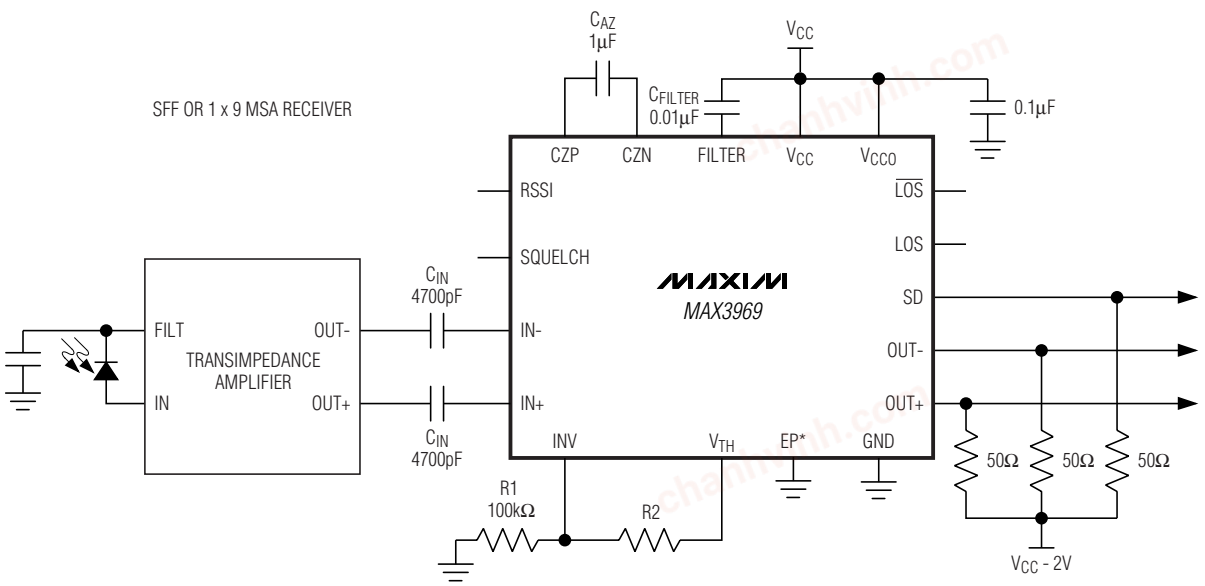
Typical Application Circuits (continued)



*EXPOSED PAD (EP) PAD ON MAX3969ETP ONLY.

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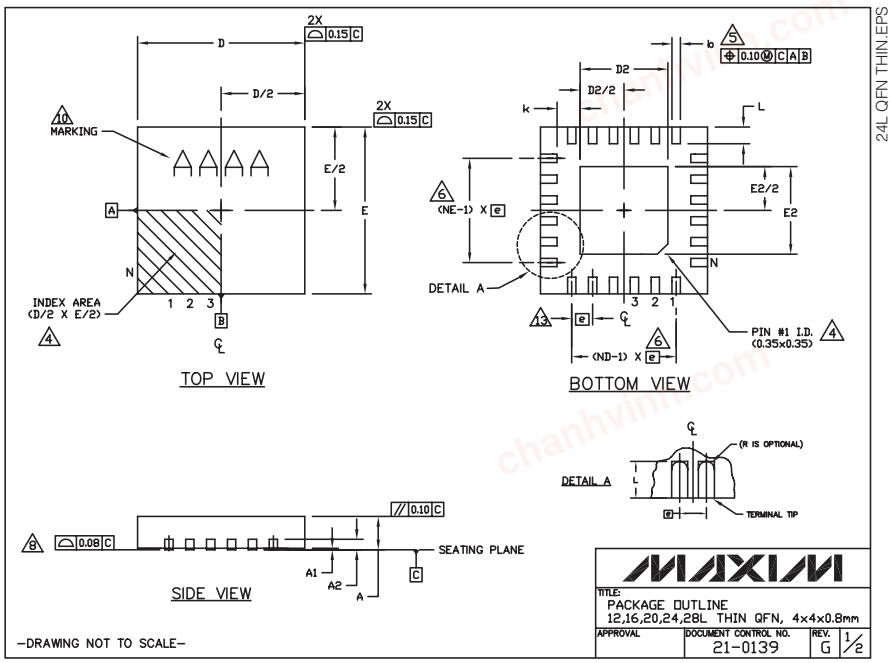
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (–) & PbFREE (+) PACKAGE CODES.

–DRAWING NOT TO SCALE–

TITLE:
PACKAGE OUTLINE
12,16,20,24,28L THIN QFN, 4x4x0.8mm
APPROVAL
DOCUMENT CONTROL NO.
21-0139
REV.
G
2/2

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