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19-3985; Rev 2; 7/96

MAXIM

Quad, SPST, Ultra-Low Leakage, CMOS Analog Switches

General Description

The MAX326/MAX327 quad, single-pole-single-throw (SPST), CMOS analog switches upgrade the DG201A/DG202 and DG211/DG212 with at least 100 times less leakage—the MAX326/MAX327 have 10pA maximum leakage, while the DG201A/DG202 have 1000pA and the DG211/DG212 have 5000pA. Low leakage currents support high system accuracy and make the devices useful for switching into high impedances, such as large-value feedback resistors in closed-loop gain configurations. And the MAX326/MAX327 logic inputs are CMOS and TTL compatible.

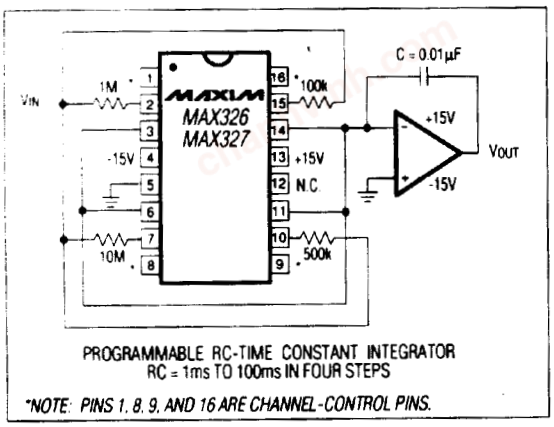
The MAX326/MAX327's low charge injection (2pC typ) minimizes signal error. Operation from single supplies (+10V to +30V), dual supplies (±5V to ±18V), and unbalanced combinations (i.e. +12V and -5V, or +5V and -15V) maximizes design flexibility. Both parts also feature interchangeable inputs/outputs and Maxim's standard latchup-proof construction.

Extremely low power consumption (5.25mW max) makes the MAX326/MAX327 ideal for portable applications. Other programmable applications include integrators with long RC time constants, current-to-voltage converters, high-gain amplifiers, and voltage dividers.

Applications

High-Accuracy Data Acquisition Systems
Sample-and-Hold Circuits
Communication Systems
Guidance and Control Systems
Test Equipment

Typical Operating Circuit



PROGRAMMABLE RC-TIME CONSTANT INTEGRATOR
RC = 1ms TO 100ms IN FOUR STEPS

*NOTE: PINS 1, 8, 9, AND 16 ARE CHANNEL-CONTROL PINS.

Features

- ♦ **10pA Max Leakage (<1pA Typ)**
- ♦ **Plug-In, Low-Leakage Upgrades for DG201A/DG202 and DG211/DG212**
- ♦ **Interchangeable Inputs/Outputs**
- ♦ **CMOS and TTL Compatible**
- ♦ **2pC Typ Charge Injection**
- ♦ **Single- (+10V to +30V), Bipolar- (±5V to ±18V), or Unbalanced- (i.e. +12V and -5V) Supply Operation**
- ♦ **5.25mW Max Power Consumption**
- ♦ **Latchup-Proof Construction**

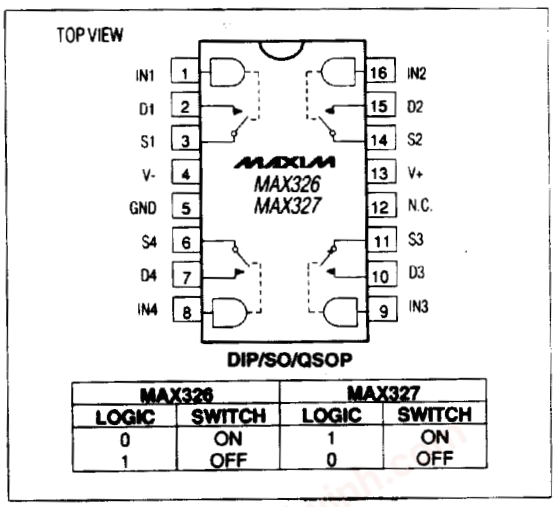
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX326CPE	0°C to +70°C	16 Plastic DIP
MAX326CEE	0°C to +70°C	16 QSOP
MAX326CSE	0°C to +70°C	16 Narrow SO
MAX326CJE	0°C to +70°C	16 CERDIP**
MAX326C/D	0°C to +70°C	Dice*
MAX326EPE	-40°C to +85°C	16 Plastic DIP
MAX326EEE	-40°C to +85°C	16 QSOP
MAX326ESE	-40°C to +85°C	16 Narrow SO
MAX326EJE	-40°C to +85°C	16 CERDIP**
MAX326MJE	-55°C to +125°C	16 CERDIP**

Ordering Information continued on page 6.

**Contact factory for dice specifications.*
***Contact factory for availability.*

Pin Configuration



DIP/SO/QSOP

MAX326		MAX327	
LOGIC	SWITCH	LOGIC	SWITCH
0	ON	1	ON
1	OFF	0	OFF

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

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Quad, SPST, Ultra-Low Leakage, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... +44V
V_{IN} to GND ..... V, V+
V_S, V_D (Note 1) ..... (V- - 0.3V) to (V+ + 0.3V)
V+ to GND (V- = 0V ..... +40V
Current (any terminal, except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D 70mA
(pulsed at 1ms, 10% duty cycle max)
Continuous Total Power Dissipitaition (Note 2)
16-Pin Plastic DIP (derate 7.5mW/°C above +70°C) 470mW
16-Pin QSOP (derate 9.52mW/°C above +70°C 762mW
16-Pin Narrow SO (derate 10mW/°C above +70°C) 400mW
16-Pin CERDIP (derate 10mW/°C above +70°C) 900mW

Operating Temperature Ranges:
MAX32 _ C _ _ ..... 0°C to +70°C
MAX32 _ E _ _ ..... -40°C to +85°C
MAX32 _ MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Exceeding this limit is acceptable as long as the S or D current is less than 20mA.
Note 2: All leads soldering or welding to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MAX32_M MIN	MAX32_M TYP	MAX32_M MAX	MAX32_C/E MIN	MAX32_C/E TYP	MAX32_C/E MAX	UNITS
SWITCH										
Analog-Signal Range	V_{ANALOG}		T_{MIN} to T_{MAX}			±15			±15	V
Drain-Source On Resistance	$r_{DS(ON)}$	V_{IN} = 0.8V (MAX326), V_{IN} = 2.4V (MAX327), V_D = ±10V, I_S = 100µA	T_A = +25°C		1.5	2.5		1.5	3.5	kΩ
			T_{MIN} to T_{MAX}		2.2	4		1.9	5	
On-Resistance Match			T_A = +25°C		5			5		%
Source-Off Leakage Current (Note 3)	$I_{S(OFF)}$	V_{IN} = 2.4V (MAX326), V_{IN} = 0.8V (MAX327), V_S = 14V, V_D = -14V	T_A = +25°C		0.1	±10		0.1	±10	pA
			T_{MIN} to T_{MAX}			±5			±5	nA
		V_{IN} = 2.4V (MAX326), V_{IN} = 0.8V (MAX327), V_S = 14V, V_D = 14V	T_A = +25°C		0.2	±10		0.2	±10	pA
			T_{MIN} to T_{MAX}			±5			±5	nA
Drain-Off Leakage Current (Note 3)	$I_{D(OFF)}$	V_{IN} = 2.4V (MAX326), V_{IN} = 0.8V (MAX327), V_S = 14V, V_D = -14V	T_A = +25°C		0.1	±10		0.1	±10	pA
			T_{MIN} to T_{MAX}			±5			±5	nA
		V_{IN} = 2.4V (MAX326), V_{IN} = 0.8V (MAX327), V_S = 14V, V_D = 14V	T_A = +25°C		0.2	±10		0.2	±20	pA
			T_{MIN} to T_{MAX}			±5			±5	nA
Drain-On Leakage Current (Note 3)	$I_{D(ON)}$	V_{IN} = 0.8V (MAX326), V_{IN} = 2.4V (MAX327), V_S = V_D = 14V	T_A = +25°C		1	±10		1	±10	pA
			T_{MIN} to T_{MAX}			±10			±10	nA
		V_{IN} = 0.8V (MAX326), V_{IN} = 2.4V (MAX327), V_S = V_D = -14V	T_A = +25°C		2	±10		2	±10	pA
			T_{MIN} to T_{MAX}			±10			±10	nA
INPUT										
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V	T_{MIN} to T_{MAX}	-1	-0.0004		-1	-0.0004		µA
		V_{IN} = 15V	T_{MIN} to T_{MAX}		0.003	1		0.003	1	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0V	T_{MIN} to T_{MAX}	-1	-0.0004		-1	-0.0004		µA

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ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX32_M MIN	MAX32_M TYP	MAX32_M MAX	MAX32_C/E MIN	MAX32_C/E TYP	MAX32_C/E MAX	UNITS
SUPPLY									
Positive Supply Current	I+	V_{IN} = 0V or 5V on all inputs		0.09	0.25		0.09	0.25	mA
Negative Supply Current	I-	V_{IN} = 0V or 5V on all inputs	-0.1	-0.00001		-0.1	-0.00001		mA
Power-Supply Range for Continuous Operation		(Note 4)	±4.5		±18	±4.5		±18	V
DYNAMIC									
Turn-On Time	t_{ON}	V_S = 2V, R_L = 1kΩ, C_L = 35pF (Figure 1)		500	1000		500	1000	ns
Turn-Off Time	t_{OFF}	V_S = 2V, R_L = 1kΩ, C_L = 35pF (Figure 1)		50	500		50	500	ns
Charge Injection (Note 5)	Q	C_L = 0.01µF, V_{GEN} = 0V, R_{GEN} = 0Ω		2	5		2	5	pC
Off Isolation (Note 4)	OIRR	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = 1V_{RMS}, f = 100kHz		70			70		dB
Crosstalk (Channel-to-Channel)	CCRR	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = 1V_{RMS}, f = 100kHz		90			90		dB
Source-Off Capacitance	$C_{S(OFF)}$	V_S = 0V, V_{IN} = 5V, f = 1MHz		1.7			1.7		pF
Drain-Off Capacitance	$C_{D(OFF)}$	V_S = 0V, V_{IN} = 5V, f = 1MHz		1.7			1.7		pF
Channel-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	V_D = V_S = 0V, V_{IN} = 0V, f = 1MHz		6			6		pF

Note 3: All leakage parameters are 100% tested at maximum rated operating temperatures, i.e. +70°C, +85°C, or +125°C, and guaranteed by correlation at +25°C.

Note 4: Electrical characteristics, such as $r_{DS(ON)}$, will change when power supplies other than ±15V are used. Power-supply range is a design characteristic, not production tested.

Note 5: Guaranteed by design.

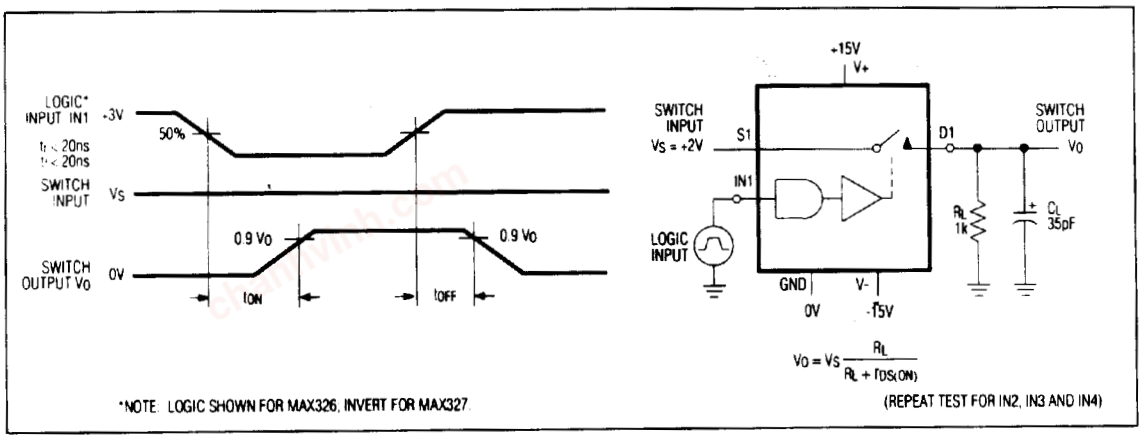
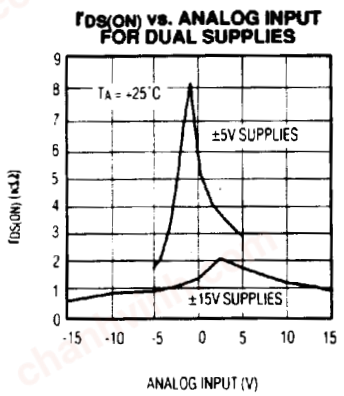


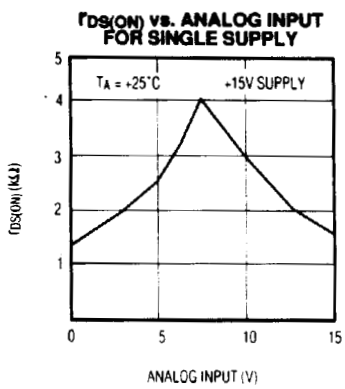
Figure 1. Switching-Time Test Circuit. Switch-output waveform shown for V_S = constant with logic-input waveform as shown. Note: V_S may be positive or negative as per switching-time test circuit. V_O is the steady-state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

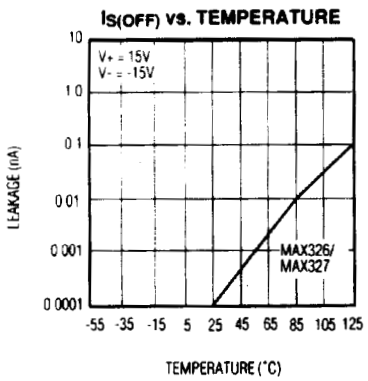
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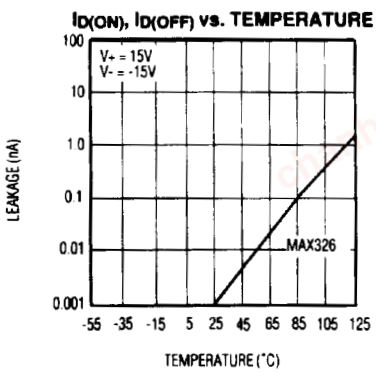
Quad, SPST, Ultra-Low Leakage, CMOS Analog Switches

Typical Operating Characteristics









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Application Hints

The MAX326/MAX327 are pin-compatible upgrades for the DG201A/DG202 and DG211/DG212. The MAX326/MAX327 feature significantly lower leakages (at least 100 times less at +25°C), but with higher on resistance. Low leakage minimizes signal error in most applications that require signal switching into high-impedance inputs of A/Ds or op amps. Switching times are virtually identical, as shown in Table 1.

Table 1. Switching Speeds with Various Power-Supply Combinations

POWER SUPPLY (V)	tON (µs)	tOFF (ns)
±15	0.5	50
±10	1	80
±5	2.5	200
+10	2.5	200
+15	1.5	100

The MAX326/MAX327 work well in single-supply applications from +10V to +30V. For these applications, V- should be connected to ground, and signal levels equal to the rail can be switched. ±5V to ±18V dual supplies can also be used to increase design flexibility.

Channel-to-channel on-resistance matching is typically better than 95% for a given analog input level. *Typical Operating Characteristics* show how $r_{DS(ON)}$ changes with various analog inputs and power-supply combinations.

While specified at TTL threshold levels, the logic threshold is roughly 1.5V ±0.2V and switches properly with CMOS input levels from -15V to +15V. Logic input levels should never be allowed to exceed the supply rails.

Protecting Against Fault Conditions

Fault conditions develop when power supplies are turned off with input signals still present, or when overvoltages occur at the inputs during normal operation. In either case, source-to-body diodes can be forward biased to conduct current from the signal source. If low current levels are required, the addition of external protection diodes is recommended (Figure 2).

To provide protection for overvoltages up to 20V above the supply rails, a 1N4001 or 1N914 diode should be placed in series with the positive and negative supplies (Figure 2). The addition of these diodes will reduce the analog signal range to 1V below the positive supply and 1V above the negative supply.

For signals that can be momentarily shorted to the 110VAC line, the addition of a 47kΩ, 1/2W resistor in series with the channel input is recommended. This will protect the switch and allow normal operation to continue once the fault condition abates. The throughput resistance will then be 47kΩ plus $r_{DS(ON)}$, but low switch leakage will reduce the error while maintaining superior system reliability.

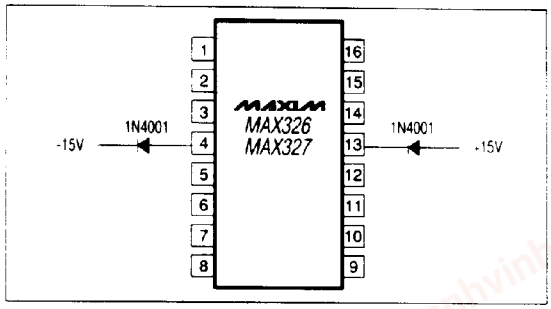


Figure 2. Protection Against Fault Conditions

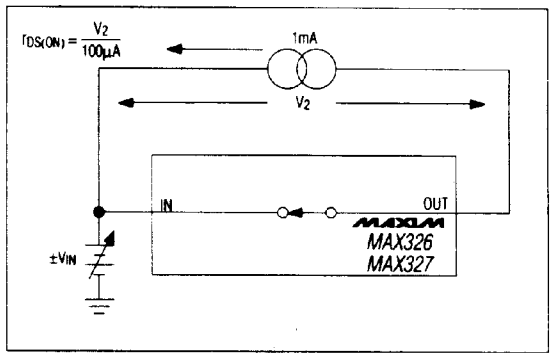


Figure 3. On Resistance vs. Analog-Signal Level Supply Voltage

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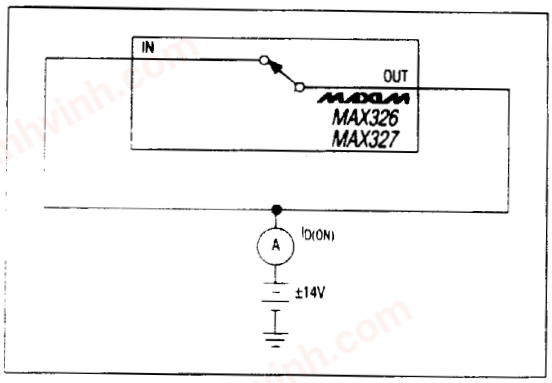


Figure 4. On Leakage Current Test Circuit

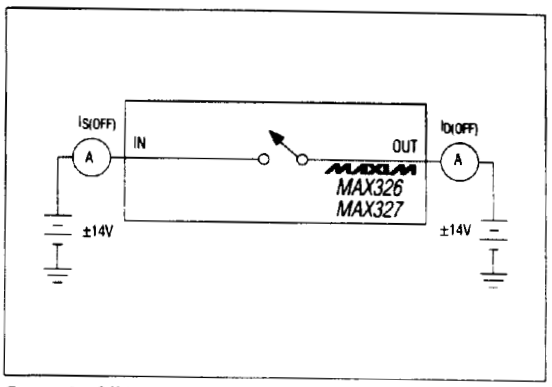


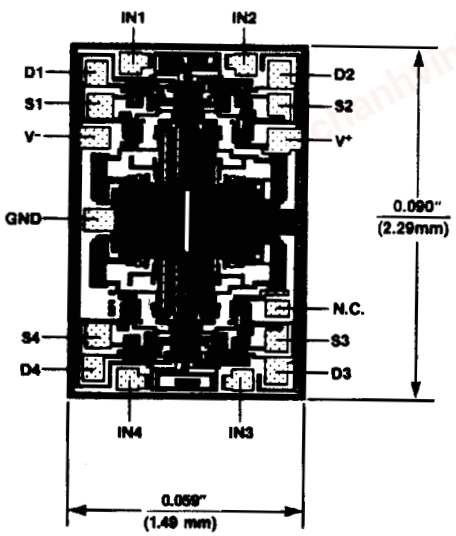
Figure 5. Off Leakage Current Test Circuit

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX327CPE	0°C to +70°C	16 Plastic DIP
MAX327CEE	0°C to +70°C	16 QSOP
MAX327CSE	0°C to +70°C	16 Narrow SO
MAX327CJE	0°C to +70°C	16 CERDIP**
MAX327C/D	0°C to +70°C	Dice*
MAX327EPE	-40°C to +85°C	16 Plastic DIP
MAX327EEE	-40°C to +85°C	16 QSOP
MAX327ESE	-40°C to +85°C	16 Narrow SO
MAX327EJE	-40°C to +85°C	16 CERDIP**
MAX327MJE	-55°C to +125°C	16 CERDIP**

*Contact factory for dice specifications. Substrate may be allowed to float or be tied to V+.
**Contact factory for availability.

Chip Topography

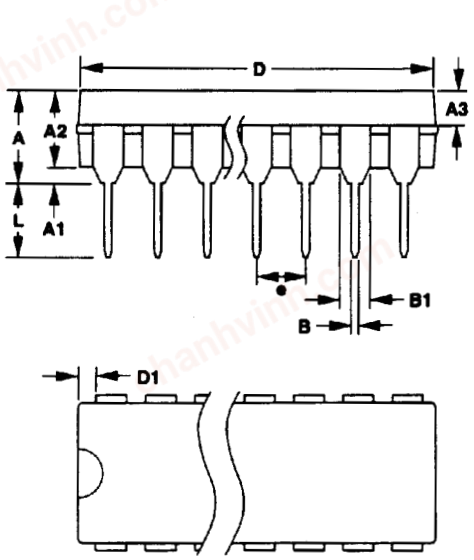


SUBSTRATE CONNECTED TO V+

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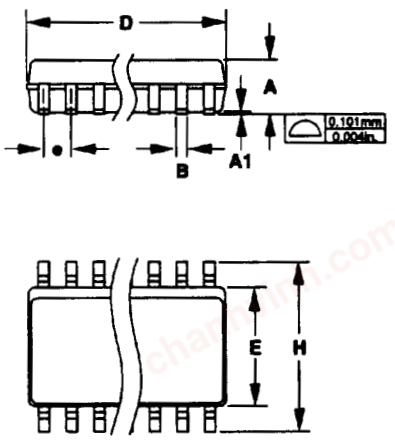
Package Information



Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.348	0.390	8.84	9.91
D	14	0.735	0.765	18.67	19.43
D	16	0.745	0.765	18.92	19.43
D	18	0.885	0.915	22.48	23.24
D	20	1.015	1.045	25.78	26.54
D	24	1.14	1.265	28.96	32.13



SO
SMALL OUTLINE
PACKAGE
(0.150 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

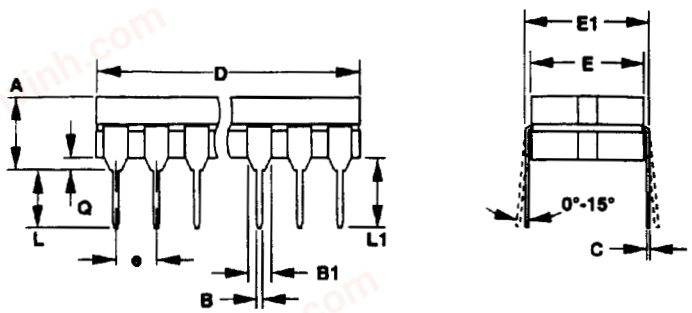
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A

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Package Information (continued)

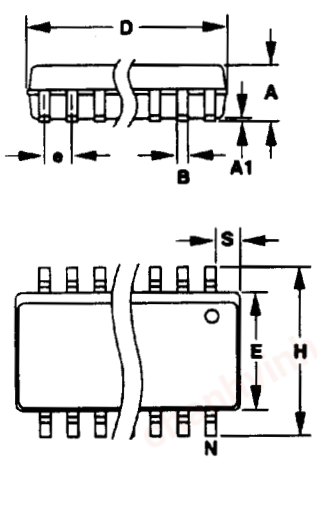


CERDIP CERAMIC DUAL-IN-LINE PACKAGE (0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

21-0045A



QSOP QUARTER SMALL-OUTLINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.127	0.25
A2	0.055	0.061	1.40	1.55
B	0.008	0.012	0.20	0.31
C	0.0075	0.0098	0.19	0.25
D	SEE VARIATIONS			
E	0.150	0.157	3.81	3.99
e	0.25 BSC		0.635 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.189	0.196	4.80	4.98
S	16	0.0020	0.0070	0.05	0.18
D	20	0.337	0.344	8.56	8.74
S	20	0.0500	0.0550	1.27	1.40
D	24	0.337	0.344	8.56	8.74
S	24	0.0250	0.0300	0.64	0.76
D	28	0.386	0.393	9.80	9.98
S	28	0.0250	0.0300	0.64	0.76

21-0055A

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