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MAX20057

36V Boost Controller with Two Synchronous Buck Converters (3.5A/2A) for Automotive Applications

General Description

The MAX20057 is an automotive highly integrated triple output PMIC. It includes two synchronous buck converters and an asynchronous boost controller with 2.1MHz and 400kHz options. The boost controller can be used to provide power to buck converters and keep them in regulation during cold-crank operation down to 2V battery input. Two high-voltage synchronous step-down converters operate 180° out-of-phase. The IC operates with an input voltage supply from 3.5V to 36V and can operate in dropout conditions by running at 95% duty cycle. It is intended for applications with mid- to high-power requirements that operate at a wide input voltage range such as during automotive cold-crank or engine stop-start conditions.

High switching frequency up to 2.1MHz allows small external components, reduced output ripple, and guarantees no AM band interference. The switching frequency is fixed at 400kHz or 2.1MHz. FSYNC input programmability enables three modes for optimized performance: forced fixed-frequency operation, skip mode with ultra-low quiescent current, and phase-locked synchronization to an external clock. The spread spectrum option minimizes EMI interference.

The IC features the power-OK indicators for buck converters and undervoltage lockout for each power rail. Protection features include cycle-by-cycle current limit and thermal shutdown. The MAX20057 is specified for operation over the -40°C to +125°C automotive temperature range.

Applications

- Automotive Start-Stop System
- Instrument Cluster
- Distributed DC Power Systems
- Navigation and Radio Head Units

Benefits and Features

- Meets Stringent OEM Module Power Consumption and Performance Specifications
  - 10µA Supply Current with 5V Buck On
  - 8µA Supply Current with 3.3V Buck On
  - 30µA Supply Current with All Regulators On
- Enables Crank-Ready Designs
  - Output Voltages in Regulation Through Cold Crank Down to 2V Battery Voltage
  - Wide Input Supply Range from 3.5V to 36V
- EMI Reduction Features Reduce Interference with Sensitive Radio Bands without Sacrificing Wide Input Voltage Range
  - 20ns (typ) Minimum On-Time Guarantees Skip-Free Operation for 3.3V Output at 2.1MHz
  - Spread-Spectrum Option
  - Phase-Locked Loop (PLL) Frequency Synchronization
- Integration and Thermally Enhanced Packages Save Board Space and Cost
  - Two 2.1MHz Buck Converters with Asynchronous Boost Controller
  - Current-Mode Controller with Forced Fixed Frequency and Skip Modes
  - Thermally Enhanced 5mm x 5mm, 28-Pin TQFN-EP Package
- Protection Features Improve System Reliability
  - Supply Undervoltage Lockout
  - Overtemperature and Short-Circuit Protection

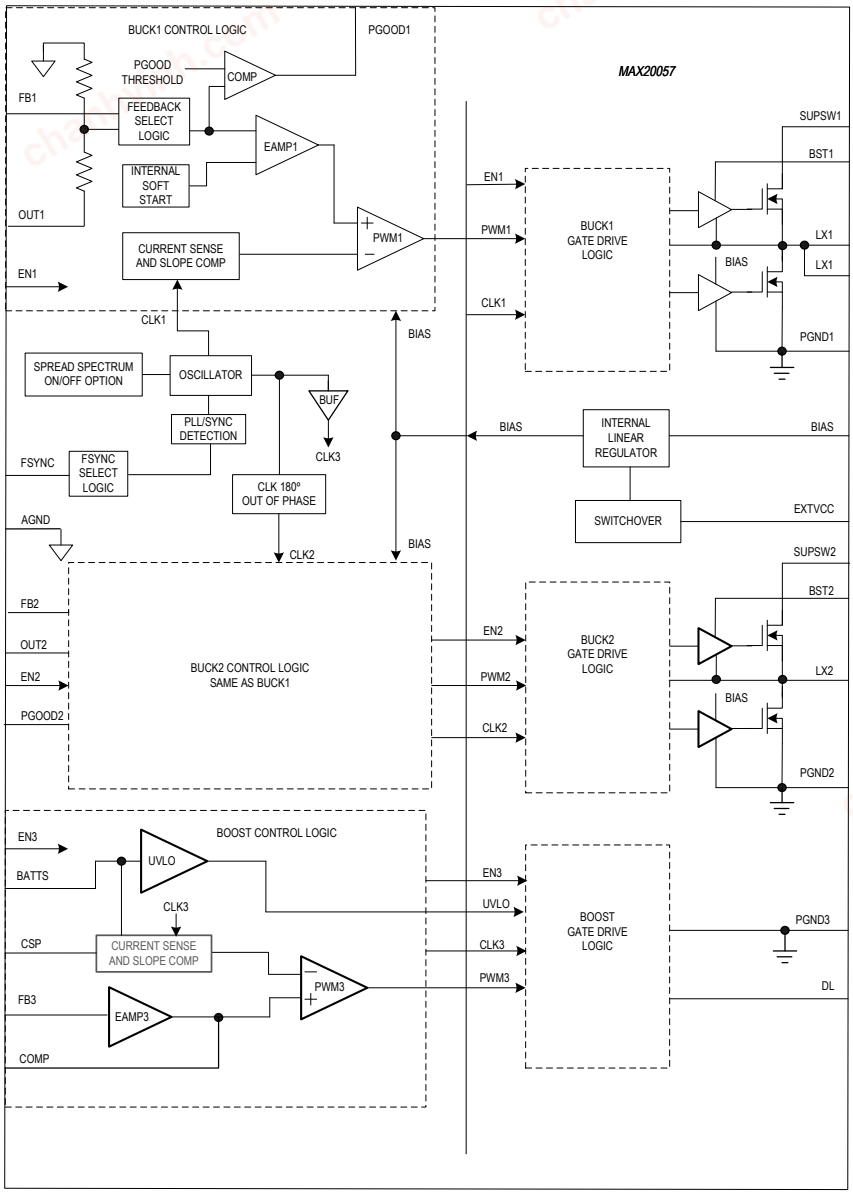
***Ordering Information* appears at end of data sheet.**

19-100442; Rev 4; 3/20

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Simplified Block Diagram



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Absolute Maximum Ratings

SUP, SUPSW1, SUPSW2, FB3, EN_, to AGND ..... -0.3V to 40V
OUT1, OUT2 to AGND ..... -0.4V to 15V
BIAS, FSYNC, PGOOD1, PGOOD2, FB1, FB2 to AGND -0.3V to +6V
EXTVCC, COMP, CSP to AGND .....-0.3V to (BIAS + 0.3)V
DL to PGND3 .....-0.3V to (BIAS + 0.3)V
LX_ to PGND_.....-0.3V to (SUPSW_ + 0.3)V
BST_ to LX_.....-0.3V to 6V
PGND_ to AGND .....-0.3V to 0.3V
Continuous Power Dissipation (T_A = +70°C, derate 28.6mW/°C above +70°C).....2286mW
Operating Temperature Range .....-40ºC to 125ºC
Storage Temperature Range .....-65ºC to +150ºC
Lead Temperature(soldering,10s)..... 300ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28 PIN TQFN

Package Code	T2855Y+5C
Outline Number	21-100130
Land Pattern Number	90-0027
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	27°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Note 2: Package thermal resistances were obtained using the Evaluation Kit. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{SUP} = $V_{SUPSW_}$ = 14V, $V_{EN_}$ = 14V, T_J = -40ºC to +150ºC, unless otherwise noted. Typical values are at T_A = +25ºC) (Notes 3 and 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONOUS STEP-DOWN CONVERTERS						
Supply Voltage Range	V_{SUP}	Normal Operation	3.5		36	V
		With preboost after initial start-up condition is satisfied	2.05		36	

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Electrical Characteristics (continued)

(V_{SUP} = $V_{SUPSW_}$ = 14V, $V_{EN_}$ = 14V, T_J = -40ºC to +150ºC, unless otherwise noted. Typical values are at T_A = +25ºC) (Notes 3 and 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{IN}	V_{EN1} = V_{EN2} = V_{EN3} = 0V		1	5	µA
		V_{EN1} = VSUP, V_{OUT1} =5V, V_{EN2} = V_{EN3} = 0V, V_{EXTVCC} = 5V, No Switching		10	18	
		V_{EN2} = V_{SUP}, V_{OUT2} = 3.3V, V_{EN1} = V_{EN3} = 0V, V_{EXTVCC} = 3.3V, No Switching		8	12	
		V_{EN1} = V_{EN2} = V_{SUP}, V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{EN3} = V_{SUP}, V_{EXTVCC} = 3.3V, V_{FB3} > 1V, No Switching		30		
Buck1 Fixed Output Voltage	V_{OUT1}	V_{FB1} = V_{BIAS}, V_{OUT1} = 5V, PWM mode	4.9	5	5.1	V
		V_{FB1} = V_{BIAS}, V_{OUT1} = 5V, skip mode	4.85	5	5.15	
Buck2 Fixed Output Voltage	V_{OUT2}	V_{FB2} = V_{BIAS}, V_{OUT2} = 3.3V, PWM mode	3.234	3.3	3.366	V
		V_{FB2} = V_{BIAS}, V_{OUT2} = 3.3V, skip mode	3.2	3.3	3.4	
Output Voltage Adjustable Range		Buck1, Buck2 (Note 5)	1		14	V
Regulated Feedback Voltage	V_{FB1}, V_{FB2}		0.985	1	1.015	V
Feedback Leakage Current	I_{FB1}, I_{FB2}	T_A = +25°C		0.01	1	µA
Feedback Line Regulation Error		V_{SUP} = 3.5V to 36V, $V_{FB_}$ = 1V		0.01		%/V
Dead time		Buck1, Buck2 (Note 5)		3		ns
Maximum Duty Cycle		Buck1, Buck2	95			%
Minimum On-Time	t_{ON_MIN}	Buck1, Buck2 (Note 5)		20		ns
PWM Switching Frequency Range	f_{SW}	OTP Option of 400kHz (see the *Ordering Information* for exact part number)		2.1		MHz
Switching Frequency Accuracy			1.9	2.1	2.32	MHz
Current-Limit		Buck1	4.5	6	7.5	A
		Buck2	2.5	3.5	4.5	
Soft-Start Ramp Time		Buck1 and Buck2, fixed soft-start time regardless of frequency.	3	5.5	7	ms
Phase Shift Between Buck1 and Buck 2		PWM Operation (Note 5)		180		deg
LX1, LX2 Leakage Current		V_{IN} = 6V, $V_{LX_}$ = $V_{PGND_}$ or V_{IN}, T_A = +25°C		0.001	5	µA
High-Side Switch On Resistance	$R_{ON_H_BUCK1}$	I_{LX1} = 1A, V_{BIAS} = 5V		50		mΩ
	$R_{ON_H_BUCK2}$	I_{LX2} = 1A , V_{BIAS} = 5V		100		

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Electrical Characteristics (continued)

(V_{SUP} = $V_{SUPSW_}$ = 14V, $V_{EN_}$ = 14V, T_J = -40ºC to +150ºC, unless otherwise noted. Typical values are at T_A = +25ºC) (Notes 3 and 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Side Switch On Resistance	$R_{ON_L_BUCK1}$	I_{LX1} = 1A, V_{BIAS} = 5V		45		mΩ
	$R_{ON_L_BUCK2}$	I_{LX2} = 1A, V_{BIAS} = 5V		90		
PGOOD1, PGOOD2Threshold	V_{PGOOD_H}	% of $V_{OUT_}$, rising	93	95	97	%
	V_{PGOOD_F}	% of $V_{OUT_}$, falling	91.5	93.5	95.5	
PGOOD1, PGOOD2 Leakage Current		V_{PGOOD1} = V_{PGOOD2} = 5V, T_A = +25°C		0.01	1	µA
PGOOD1, PGOOD2 Output Low Voltage		I_{SINK} = 1mA			0.2	V
PGOOD1, PGOOD2 Debounce Time		Fault Detection, Rising and Falling		20		µs
PGOOD1, PGOOD2 Assertion Time		PGOOD1, PGOOD2 Low to High (Note 5)		0		ms
STEP-UP CONTROLLER						
Minimum On Time	t_{ONBST}	(Note 5)		60		ns
Minimum Off Time	t_{OFFBST}			60		ns
Current Limit	V_{LIMBST}	V_{CS} - V_{PGND3}	40	50	60	mV
Undervoltage Lockout	U_{VLO}	Input Voltage Rising		4.5		V
DL Pullup Resistance		V_{BIAS} = 5V, I_{DL} = -100mA		3	6	Ω
DL Pulldown Resistance		V_{BIAS} = 5V, I_{DL} = 100mA		1	2	Ω
Boost Feedback Voltage	V_{FB3}	Pre-Boost Feedback Voltage, No Load on Boost Output	0.985	1.005	1.025	V
Transconductance (from FB3 to COMP)	g_{M_BOOST}	V_{FB3} = 1.005V, V_{BIAS} = 5V	130	230	330	µS
Boost Fixed Output Voltage	V_{OUT3}	Contact factory for other available options	9.75	10	10.2	V
Boost Load Regulation Error		PWM Mode, Load from 1mA to 4A		0.05		%/A
FB3 Leakage Current	I_{FB3}	T_A = +25°C		0.01	1	µA
FSYNC INPUT						
FSYNC frequency Range		Minimum sync pulse of 100ns, f_{OSC} = 2.1MHz	1.8		2.6	MHz
		Minimum sync pulse of 1.5µs, f_{OSC} = 400kHz	250		550	kHz
FSYNC Switching Thresholds		High Threshold	1.4			V
		Low Threshold			0.4	
INTERNAL LDO BIAS AND EXTVCC						
Internal BIAS Voltage		V_{SUPSW1} > 6V		5		V
BIAS UVLO Threshold		V_{BIAS} rising		3.1	3.3	V
		V_{BIAS} falling	2.4	2.6		

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Electrical Characteristics (continued)

(V_{SUP} = $V_{SUPSW_}$ = 14V, $V_{EN_}$ = 14V, T_J = -40ºC to +150ºC, unless otherwise noted. Typical values are at T_A = +25ºC) (Notes 3 and 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTVCC Operating Range			3.25		5.5	V
EXTVCC Threshold	V_{TH_EXTVCC}	EXTVCC rising, hysteresis = 110mV		3	3.25	V
THERMAL OVERLOAD						
Thermal Shutdown Temperature		(Note 5)		170		°C
Thermal Shutdown Hysteresis		(Note 5)		20		°C
EN LOGIC INPUT						
High Threshold		EN_	1.8			V
Low Threshold		EN_			0.8	V
EN Input Bias Current		EN_ Logic Inputs Only, T_A = +25°C		0.01	1	µA
SPREAD SPECTRUM						
Spread Spectrum		Spread spectrum enabled		f_{OSC} ±6%		

Note 3: Limits are 100% tested at +25°C. Limits over operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at +25°C.

Note 4: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours

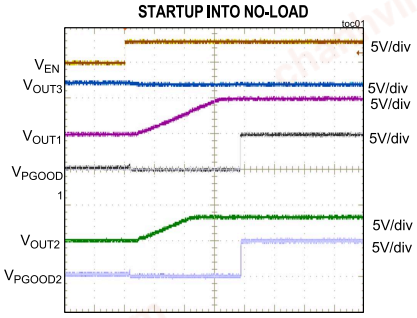
Note 5: Guaranteed by design, not production tested.

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Typical Operating Characteristics

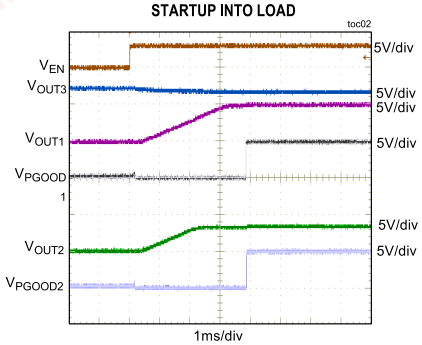
(T_A = +25ºC, unless otherwise noted.))

STARTUP INTO NO-LOAD



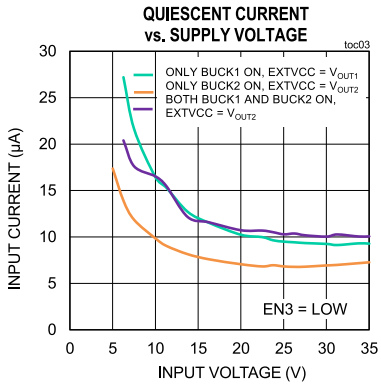
CONDITIONS: EN1 = EN2 = EN3, FSYNC = 1, V_{IN} = 14V, EXTVCC = V_{OUT1}

STARTUP INTO LOAD

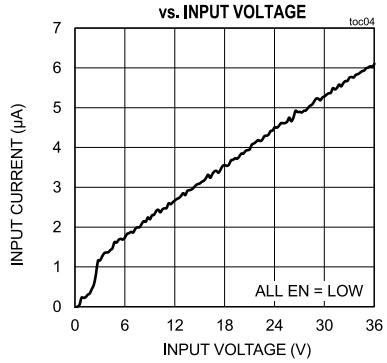


CONDITIONS: EN1 = EN 2= EN3, FSYNC = 1, EXTVCC = V_{OUT1}, V_{IN} = 14V, I_{OUT1} = 3A, I_{OUT2} = 1.5A

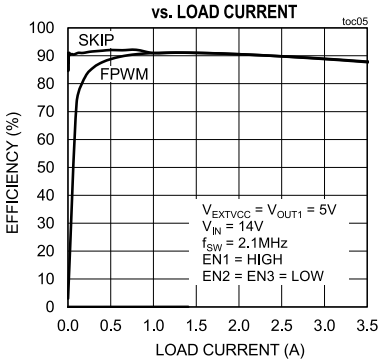
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



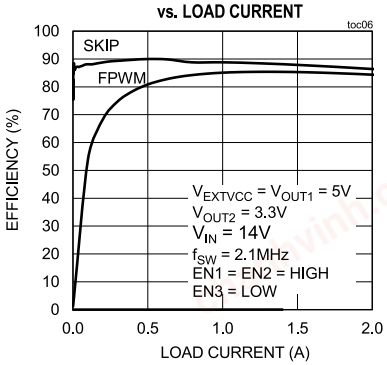
SHUTDOWN CURRENT vs. INPUT VOLTAGE



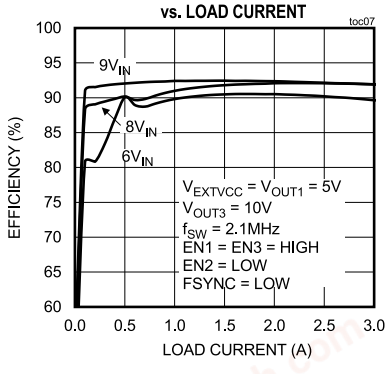
BUCK1 EFFICIENCY vs. LOAD CURRENT



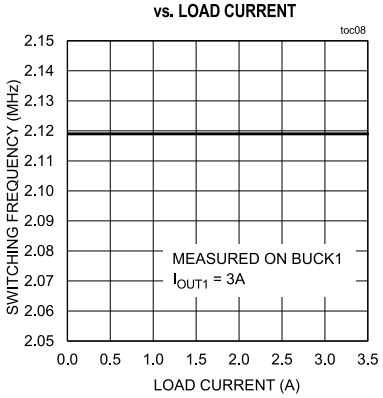
BUCK2 EFFICIENCY vs. LOAD CURRENT



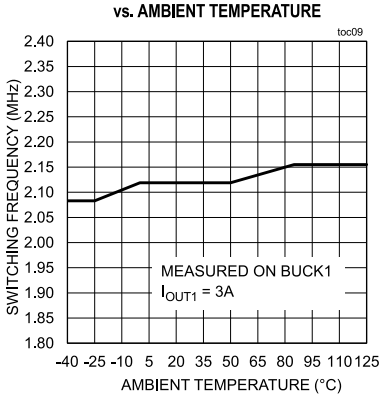
BOOST EFFICIENCY vs. LOAD CURRENT



SWITCHING FREQUENCY vs. LOAD CURRENT



SWITCHING FREQUENCY vs. AMBIENT TEMPERATURE

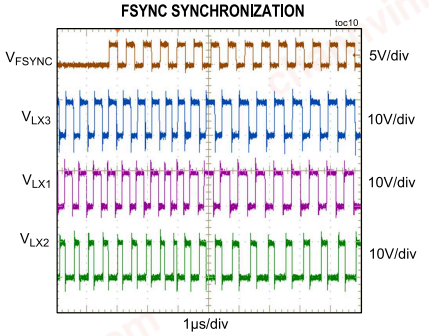


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Typical Operating Characteristics (continued)

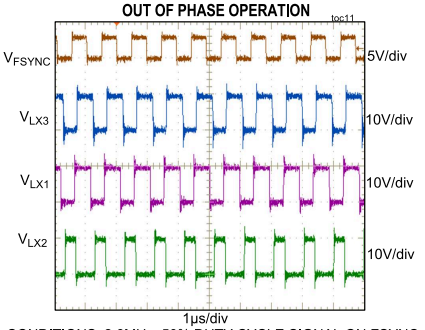
(T_A = +25ºC, unless otherwise noted.))

FSYNC SYNCHRONIZATION



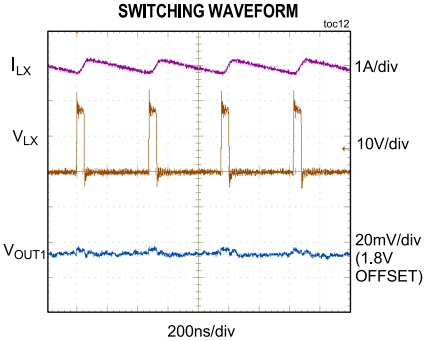
CONDITIONS: 1.8MHz, 50% DUTY CYCLE SIGNAL ON FSYNC
V_{IN} = 6V, I_{OUT1} = 3A, I_{OUT2} = 1.5A

OUT OF PHASE OPERATION



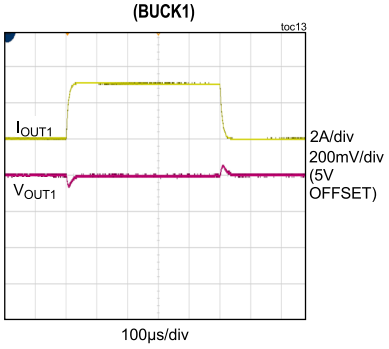
CONDITIONS: 2.6MHz, 50% DUTY CYCLE SIGNAL ON FSYNC,
V_{IN} = 6V, I_{OUT1} = 3A, I_{OUT2} = 1.5A

SWITCHING WAVEFORM



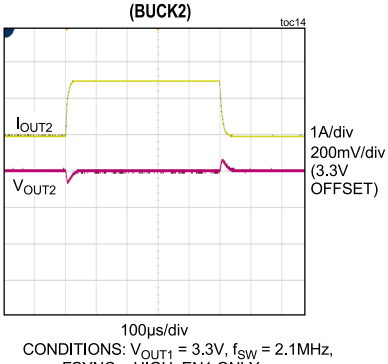
CONDITIONS: V_{IN} = 18V, V_{OUT2} = 1.8V,
f_{SW} = 2.1MHz, I_{OUT2} = 1A

LOAD TRANSIENT RESPONSE (BUCK1)



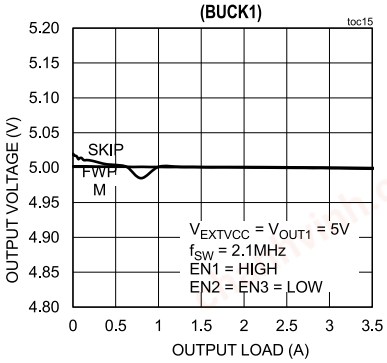
CONDITIONS: V_{OUT1} = 5V, f_{SW} = 2.1MHz,
FSYNC = HIGH. EN1 ONLY

LOAD TRANSIENT RESPONSE (BUCK2)

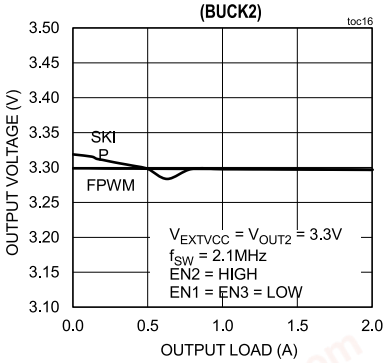


CONDITIONS: V_{OUT1} = 3.3V, f_{SW} = 2.1MHz,
FSYNC = HIGH, EN1 ONLY

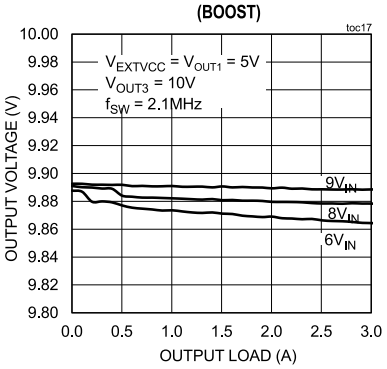
OUTPUT LOAD REGULATION (BUCK1)



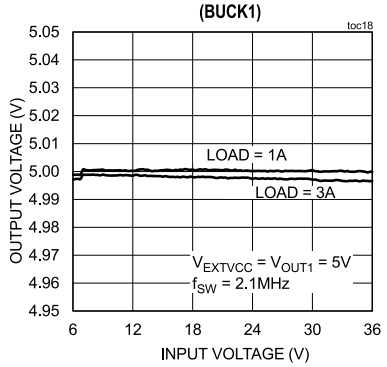
OUTPUT LOAD REGULATION (BUCK2)



OUTPUT LOAD REGULATION (BOOST)



OUTPUT LINE REGULATION (BUCK1)

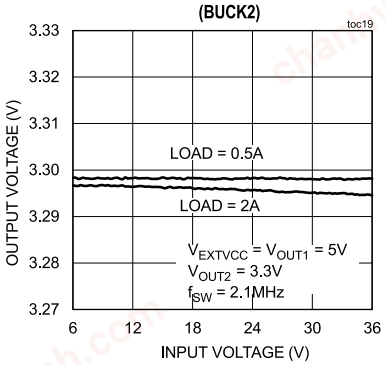


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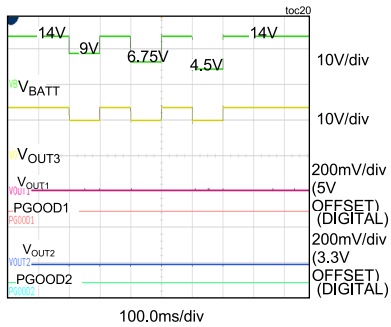
Typical Operating Characteristics (continued)

(T_A = +25ºC, unless otherwise noted.))

OUTPUT LINE REGULATION (BUCK2)

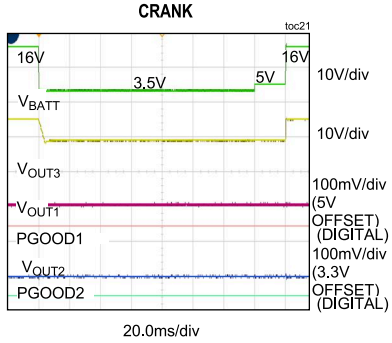


DIPS AND DROPS



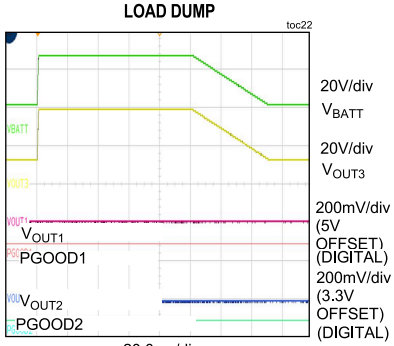
CONDITIONS: V_{EXTVCC} = V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 10V, f_{SW} = 2.1MHz, I_{OUT1} = I_{OUT2} = 1A

CRANK



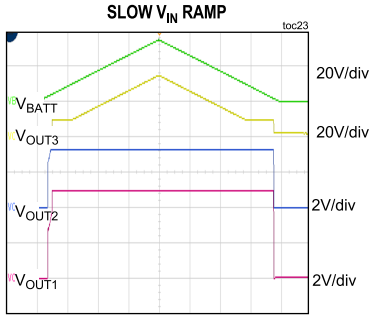
CONDITIONS: V_{EXTVCC} = V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 10V, f_{SW} = 2.1MHz, I_{OUT1} = I_{OUT2} = 1A

LOAD DUMP



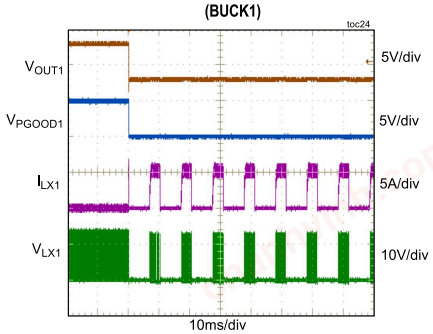
CONDITIONS: V_{EXTVCC} = V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 10V, f_{SW} = 2.1MHz, I_{OUT1} = I_{OUT2} = 1A

SLOW V_{IN} RAMP

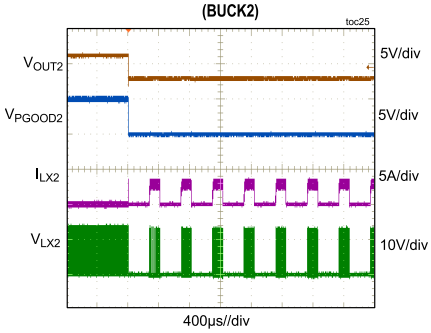


CONDITIONS: V_{EXTVCC} = V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 10V, f_{SW} = 2.1MHz, I_{OUT1} = I_{OUT2} = 1A

SHORT-CIRCUIT AFTER REGULATION (BUCK1)

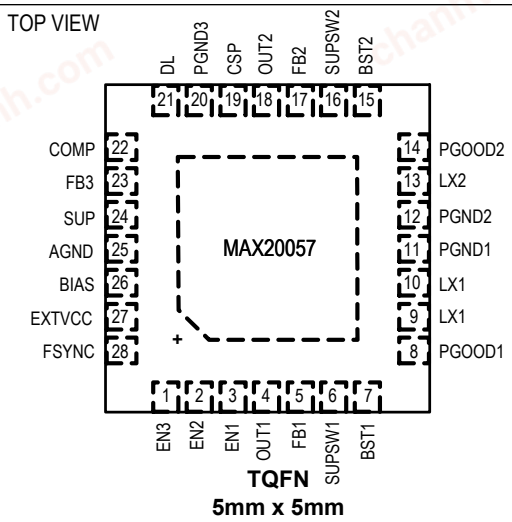


SHORT CIRCUIT AFTER REGULATION (BUCK2)



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Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	EN3	High-Voltage Tolerant, Active-High Digital Enable Input for Boost Controller. Drive EN3 high to enable boost controller.
2	EN2	EN2 High-Voltage Tolerant, Active High Digital Enable Input for Buck 2. Drive EN2 high to enable Buck 2.
3	EN1	High-Voltage Tolerant, Active High Digital Enable Input for Buck 1. Drive EN1 high to enable Buck 1.
4	OUT1	Output Sense Input for Buck 1. When using the internal preset 5V feedback divider, FB1 is connected to BIAS, and Buck 1 uses OUT1 to sense the output voltage.
5	FB1	Feedback Input for Buck 1. Connect FB1 to BIAS for fixed output or to a resistor divider between OUT1 and AGND to adjust the output voltage between 1V and 14V. FB1 is regulated to 1V (typ) in adjustable version.
6	SUPSW1	Buck 1 Internal High-Side Switch Supply Input and BIAS LDO Input. Bypass SUPSW1 to PGND1 with a 4.7µF ceramic capacitor.
7	BST1	Boost Flying Capacitor Connection for High-Side Gate Voltage of Buck 1. Connect a ceramic capacitor between BST1 and LX1.
8	PGOOD1	Open Drain Power-Good Output for Buck 1. PGOOD1 is low if OUT1 falls below 93.5% (typ) of output regulation voltage. PGOOD1 becomes high impedance when OUT1 rises above 95% (typ) of its regulation voltage. PGOOD1 asserts low during soft-start and in shutdown. To obtain a logic signal, pull up PGOOD1 with an external resistor connected to a positive voltage lower than 5.5V.
9,10	LX1	Buck 1 Inductor Connection. Connect an inductor from LX1 to the Buck 1 output.
11	PGND1	Power Ground for Buck 1
12	PGND2	Power Ground for Buck 2
13	LX2	Buck 2 Inductor Connection. Connect an inductor from LX2 to the Buck 2 output.
14	PGOOD2	Open Drain Power-Good Output for Buck 2. PGOOD2 is low if OUT2 falls below 93.5% (typ) of output regulation voltage. PGOOD2 becomes high impedance when OUT2 rises above 95% (typ) of its regulation voltage. PGOOD2 asserts low during soft-start and in shutdown. To obtain a logic signal, pull up PGOOD2 with an external resistor connected to a positive voltage lower than 5.5V.

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Pin Description (continued)

PIN	NAME	FUNCTION
15	BST2	Boost Flying Capacitor Connection for High-Side Gate Voltage of Buck 2. Connect a ceramic capacitor between BST2 and LX2.
16	SUPSW2	Buck 2 Internal High-Side Switch Supply Input. Bypass SUPSW2 to PGND2 with a 4.7µF ceramic capacitor.
17	FB2	Feedback Input for BUCK2. Connect FB2 to BIAS for fixed output or to a resistive divider between OUT2 and AGND to adjust the output voltage between 1V and 14V. FB2 is regulated to 1V (typ) in the adjustable version.
18	OUT2	Output Sense Input for BUCK2. When using the internal preset feedback divider, FB2 is connected to BIAS and Buck 2 uses OUT2 to sense the output voltage.
19	CSP	Positive Current-Sense Input for Boost Controller. Connect CSP to the positive terminal of the current sense resistor.
20	PGND3	Power Ground for Boost Controller. All the high current paths for the boost controller terminates to PGND3.
21	DL	Boost Controller N-Channel MOSFET Low Side Gate Driver Output
22	COMP	Boost Error Amplifier Output. Connect COMP with an RC compensation network.
23	FB3	Boost Controller Feedback Input. Connect an external resistive divider from boost output to FB3, and FB3 to AGND to set the output voltage for the boost adjustable output option. Connect FB3 to boost output for the fixed boost output option.
24	SUP	Boost Controller Input Sense
25	AGND	Quiet Analog Ground for the IC
26	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to ground with a low ESR minimum 2.2µF ceramic capacitor. BIAS provides the power to the internal gate drive circuitry.
27	EXTVCC	Switchover Comparator Input. Connect a voltage between 3.25V and 5.5V to EXTVCC to power the IC and bypass the internal bias LDO. Connect EXTVCC to ground if EXTVCC is not used.
28	FSYNC	External Clock Synchronization Input. Synchronization operating frequency ratio is 1. The duty-cycle of the signal on SYNC determines the phase shift between BUCK1 and BUCK2. Use 50% duty cycle for the external clock to get a 180° phase shift between BUCK1 and BUCK2.
-	EP	Exposed Pad. Connect EP to ground. Connecting EP to ground does not remove the requirement for proper ground connections to PGND and AGND. EP is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

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Detailed Description

The MAX20057 ICs are automotive-grade three output switching power supplies. Each device integrates two synchronous buck converters, and an asynchronous boost controller:

1. The Buck 1 converter provides a fixed 5V/3.3V output voltage, or an adjustable 1V to 14V output voltage option, and up to 3.5A continuous current capability.
2. The Buck 2 converter provides a fixed 5V/3.3V output voltage, or an adjustable 1V to 14V output voltage option, and up to 2A continuous current capability.
3. The preboost controller has 10V fixed or adjustable output voltage options

Each power supply has its individual enable pin. Connect EN1, EN2, or EN3 directly to battery voltage, or to power supply sequencing logic to control each power supply on/off.

In standby mode, the total supply current is reduced to 30µA (typ). When all three controllers are disabled, the total current drawn is further reduced to 1µA.

Internal 5V BIAS LDO

An internal 5V BIAS LDO supplies the IC internal circuitry. SUPSW1 supplies the internal BIAS LDO. Bypass BIAS with a minimum 2.2µF ceramic capacitor. To minimize the internal power dissipation, bypass BIAS to an external 5V rail using the EXTVCC pin.

EXTVCC Switchover

The internal linear regulator can be bypassed by connecting an external 3.25V to 5.5V supply, or one of the buck converter outputs to EXTVCC. With valid supply applied to EXTVCC, BIAS is internally switched to EXTVCC and the internal linear regulator turns off. This configuration has two main advantages:

1. Reduces IC internal power dissipation
2. Improves light-load efficiency as the internal supply current is scaled down proportionally to the duty cycle if connecting any buck output to EXTVCC

If V_{EXTVCC} drops below 3V (typ), the internal regulator is enabled and BIAS is switched back to 5V.

Switching Frequency/External Synchronization

The MAX20057 provides an internal oscillator with 400kHz and 2.1MHz options. 2.1MHz frequency operation optimizes the application for the smallest component size, at the cost of lower efficiency. 400kHz frequency operation offers best overall efficiency at the expense of component size and board space. Apply an external clock to FSYNC to enable frequency synchronization. The MAX20057 uses a phase-locked loop (PLL) to synchronize the internal oscillator to the external clock signal. The Buck 1 converter synchronizes its LX1 falling edge to the FSYNC rising edge, and the Buck 2 converter synchronizes its LX2 falling edge to the FSYNC falling edge, and the boost controller synchronizes the DL3 rising edge (or LX3 falling edge) to the FSYNC falling edge. The FSYNC signal should have a minimum 100ns high pulse width for 2.1MHz and minimum 1.5µs high pulse width for 400kHz.

Spread Spectrum Option

The ICs feature enhanced EMI performance with spread spectrum option. The spread spectrum is available as a factory option. When the spread spectrum is enabled, the operating frequency is varied ±6% centered at switching frequency. The modulation signal is a triangular wave with a period of 110µs at 2.1MHz. Therefore, switching frequency ramps down 6% and back to 2.1MHz in 110µs and also ramps up 6% and back to 2.1MHz in 110µs after which the cycle repeats.

For operations at 400kHz, the modulation signal scales proportionally (the 110µs modulation period for 2.1MHz increases to 110µs x 2.1MHz/0.4MHz = 577.5µs).

The internal spread spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock on the FSYNC pin and pass any modulation (including spread spectrum) present on the driving external clock.

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Overcurrent Protection

The MAX20057 has a cycle-by-cycle current limit and includes hiccup mode to prevent any damage from overcurrent or short-circuit on three power channels. When the inductor current continuously hits the current limit at overcurrent on any channels, the output voltage starts decreasing. If the IC detects the output voltage drops below 0.7V, it turns off that channel. After waiting for about 10ms (2x soft-start time) of hiccup time, the IC restarts that channel in case the overcurrent or short-circuit condition is removed.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ICs. When the junction temperature exceeds +170°C, an internal thermal sensor shuts down the ICs, allowing them to cool. The thermal sensor turns on the ICs again after the junction temperature cools by 20°C.

Buck Converters

The ICs provide two synchronous buck converters. The buck converters use PWM, valley current mode control scheme, making it ideal for applications with high input voltages and low output voltages. Buck 1 and Buck 2 operate 180 degrees out of phase with each other to minimize input current ripple from the minimum to the maximum input voltages.

Undervoltage Lockout (UVLO)

The internal 5V BIAS LDO undervoltage-lockout (UVLO) circuitry inhibits switching if the BIAS voltage drops below its 2.6V (typ) UVLO falling threshold. Once the BIAS voltage rises above its UVLO rising threshold, 3.1V (typ), and EN1 and EN2 enable the buck converters, Buck 1 and Buck 2 start switching and their output voltages begin soft-start.

Soft-Start

Drive EN1 and EN2 high to enable Buck 1 and Buck 2. The soft-start circuitry gradually ramps up the reference voltage during soft-start time (5ms typ) to reduce the input surge currents during startup. BIAS voltage must exceed its UVLO threshold (3.1V typ) before soft-start can be enabled.

FSYNC Mode Selection

Drive FSYNC low to enable skip mode. In skip mode, the high-side FET turns for fixed adaptable on-time (depending on V_{OUT}, V_{SUP} and f_{SW}). The high-side FET then turns off and the low-side FET turns on until the inductor current falls to the zero cross threshold. Once the low-side FET turns off by hitting the zero-crossing threshold, LX becomes high impedance and the output voltage keeps decreasing. When output voltage or FB voltage is detected below the set point, the new cycle starts by turning on the high-side FET again. In this way, the regulator switches only as needed to service load to improve system efficiency. Drive FSYNC high to enable forced PWM (FPWM) mode. FPWM mode prevents the regulator from entering skip mode, by disabling the zero-cross detection of the inductor current. The benefit of FPWM mode is to keep the switching frequency constant under all load conditions; however, FPWM operation diverts a considerable amount of the output current to PGND, reducing the efficiency under light-load conditions. FPWM mode is useful for improving load-transient response and eliminating unknown frequency harmonics that can interfere with AM radio bands.

Frequency Foldback

Frequency Foldback is implemented in buck converters when operating only at 2.1MHz and when the internal fixed output voltage option is selected. This is useful in case the boost controller is not used to protect its input voltage during V_{SUP} transient drops. When the input voltage of buck converter drops close to the output voltage, the converter runs at the maximum duty cycle and the high-side switch off period approaches minimum off time 100ns (typ). To prevent output voltage drifting out of regulation, frequency foldback is used to automatically reduce the switching frequency from 2.1MHz to 350kHz and maintain a high duty cycle of > 95% with 100ns (typ) off time. The frequency foldback occurs when the input voltage drops below a certain threshold calculated by formula of $V_{SUPSW_} = 1.4 \times V_{OUT_}$ (falling).

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High-Side Gate Driver Supply (BST1/BST2)

The buck converter high-side MOSFET is turned on by closing an internal switch between BST1/BST2 and the gate of the high-side MOSFET and transferring the bootstrap capacitor's charge at BST1/BST2 to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX1/LX2 voltage drops down to ground, taking the negative terminal of the capacitor to the same potential. At this time, the bootstrap diode recharges the positive terminal of the bootstrap capacitor to BIAS voltage.

The selected n-channel high-side MOSFET determines the appropriate boost capacitance values ($C_{BST_}$ in the Typical Operating Circuit) according to the following equation:

$$C_{BST_} = Q_G/\Delta V_{BST_}$$

where Q_G is the total gate charge of the high-side MOSFET and $\Delta V_{BST_}$ is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose $\Delta_{VBST_}$ such that the available gate-drive voltage is not significantly degraded (e.g., $\Delta V_{BST_}$ = 100mV to 300mV) when determining $C_{BST_}$. The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF works in most cases.

Power Good Indicator (PGOOD1/PGOOD2)

Each buck converter include a power good indicator to indicate the buck output voltage status. The PGOOD_ indicator can be used to enable circuits that are supplied by the corresponding voltage rail, or to turn-on subsequent supplies. Each PGOOD_ goes from low to high impedance when the corresponding regulator output voltage rises above 95% (typ) of its nominal regulation voltage. Each PGOOD_ goes low when the corresponding regulator output voltage drops below 93.5% (typ) of its nominal regulation voltage. Connect a 10kΩ (typ) pullup resistor from PGOOD_ to the relevant logic rail to level-shift the signal. PGOOD_ asserts low during soft-start, and when the buck converter is disabled.

Boost Controller

The MAX20057 ICs include an asynchronous current-mode boost controller with a fixed or adjustable output voltage option. It can be used independently, and it is also ideally suited for applications that need to stay fully functional during input voltage dropouts, typical for automotive cold-crank or start-stop. It can also be configured as a SEPIC to provide stable regulation voltage over a wide input voltage range. The boost converter is turned on by EN3 high. EN3 can be used for power-supply sequencing and implementing a boost timeout to prevent overheating the components used for the boost converter.

Soft-Start

The MAX20057 boost controller has an internal soft-start time of 1ms. After the controller detects valid BIAS voltage with EN3 high, it enters soft-start. During soft-start, the output voltage ramps linearly to its final value in 1ms.

Undervoltage Lockout (UVLO)

The boost controller UVLO circuitry monitors the SUP voltages to control boost on/off. The boost controller starts switching when UVLO circuitry detects the SUP voltage rises above 4.5V (typ). Once the controller switches, it keeps switching until the SUP voltage drops below 2.05V (min). 2.05V UVLO falling threshold can be disabled to allow the boost controller to maintain its regulation output voltage with low battery voltage. This feature allows operation at cold-crank voltages below 2V battery voltage.

Current Sense Limit

A current-sense resistor (R_{CSP}) connected between the source of the MOSFET and ground to set the current limit of the boost converter. The CSP input has a voltage trip level (V_{CSP}) of 50mV (typ). The low 50mV current-limit threshold reduces the power dissipation in the current-sense resistor. When the voltage produced by the current in the inductor exceeds the current-limit comparator threshold, the MOSFET driver (DL) quickly terminates the on-cycle. In some cases, a short time-constant RC filter can be required to filter out the leading-edge spike on the sense waveform in addition to the internal blanking time. The amplitude and width of the leading edge spike depends on the pcb layout, gate capacitance, drain capacitance, and switching speed of the external MOSFET.

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N-MOSFET Driver

DL drives the gate of an external n-channel MOSFET. The driver is powered by the 5V BIAS LDO if the EXTVCC switchover is not used. This makes the devices suitable for use with logic-level MOSFETs. DL can source and sink up to 1.67A peak current. The average current sourced by DL depends on the switching frequency and total gate charge of the external MOSFET.

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Applications Information

Buck Converters

Setting Output Voltage

Connect FB1 and FB2 to BIAS to enable fixed buck output voltages (5V or 3.3V) set by a preset internal resistive divider connected between OUT1/OUT2 and AGND. To externally adjust the output voltage between 1V and 14V, connect a resistive voltage-divider from the converter output (OUT_) to the corresponding FB_ input and then to AGND. Select the bottom-side resistors (R_{BOTTOM} from FB_-to-AGND) less than or equal to 100kΩ. Calculate the top-side resistors (R_{TOP} from output-to-FB_) with the following equation:

$R_{TOP} = R_{BOTTOM} (V_{OUT}/VFB_-1)$

where $V_{FB1} = V_{FB2} = 1V$ (typ) (see the *Electrical Characteristics* table).

When an external resistive divider is used to program the buck output voltage, a feed-forward capacitor in parallel with R_{TOP} with 2.2pF or 4.7pF capacitance is recommended to improve the control-loop phase margin.

Input Capacitor

A 4.7µF ceramic input capacitor is recommended for proper buck operation. This value can be adjusted based on application input-voltage-ripple requirements.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \times \sqrt{\frac{V_{OUT} \times V_{SUPSW_} - V_{OUT}}{V_{SUPSW_}}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$V_{SUP} = 2 \times V_{OUT}$

Therefore,

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR} that peaks at the end of an on-cycle. Calculate the input capacitance and ESR required for a specific ripple using the following equation:

$$ESR[\Omega] = \frac{\Delta V_{ESR}}{(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2})}$$

$$C_{IN}[\mu F] = \frac{I_{LOAD(MAX)} \times (\frac{V_{OUT}}{V_{IN}})}{(\Delta VQ \times f_{SW})}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and,

$I_{LOAD(MAX)}$ = Maximum output current in A, ΔI_{P-P} = Peak-to-peak inductor current in A, f_{SW} = Switching frequency in MHz, L = Inductor value in µH.

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Inductor Selection

The MAX20057 operates with two switching frequency options: 2.2MHz and 400kHz. The key parameters on inductor selection are: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The minimum required inductance is calculated as:

$$L_{MIN} = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times I_{OUT} \times LIR}$$

where LIR is the ratio of the inductor peak-to-peak AC current to DC average current, and 0.3 is a typical value to use. See Table 1 for the recommended buck inductors. The inductor's saturation current rating must meet or exceed the LX current limit. For optimum transient response and highest efficiency, use inductors with a low DC resistance.

Output Capacitor

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. The capacitor is usually selected by ESR and the voltage rating rather than by capacitance value.

When using low capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot is no longer a problem.

The total voltage sag (V_{SAG}) can be calculated as follows:

$$V_{SAG} = \frac{L \times (\Delta I_{LOAD(MAX)})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})} + \frac{\Delta I_{LOAD(MAX)} \times (t - \Delta t)}{C_{OUT}}$$

The amount of overshoot (V_{SOAR}) during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} = \frac{(\Delta I_{LOAD(MAX)})^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

See Table 1 for recommended output capacitance.

Table 1. Buck Converter Inductor and Output Capacitor Selection

SWITCHING FREQUENCY	BUCK1 INDUCTOR (µH)	BUCK1 OUTPUT CAPACITOR (µF)	BUCK2 INDUCTOR (µH)	BUCK2 OUTPUT CAPACITANCE (µF)
2.2MHz	2.2	2 x 22	2.2	22
400kHz	10	2 x 47	10	47 + 22

ESR Considerations

The output capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load transient requirements. When using high-capacitance, low-ESR capacitors, the ESR of the filter capacitor dominates the output voltage ripple:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

Boost Controller

Setting Output Voltage

The MAX20057 boost controller has two output voltage options: fixed 10V output, and adjustable output voltage. For the fixed 10V output option, connect FB3 to boost output. For the adjustable output option, connect a resistive divider from the output of the boost converter to FB, then to AGND. Calculate the top-side (R_{TOP} from output-to-FB3) and bottom-side (R_{BOTTOM} from FB3-to-AGND) resistors with the following equation:

$$R_{TOP} = R_{BOTTOM} (V_{OUT3}/V_{FB3} - 1.005)$$

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where V_{FB3} = 1.005V (typ) (see the *Electrical Characteristics* table).

Inductor Selection

Duty cycle and frequency are important to calculate the inductor size, as the inductor current ramps up during the on-time of the switch and ramps down during its off-time. The duty cycle is calculated by the formula:

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D}$$

Choose 0.3 as the ratio of the inductor peak-to-peak AC current to DC average current, LIR. The inductor value can be calculated as follows:

$$L[\mu H] = \frac{V_{IN} \times D}{f_{SW}[MHz] \times 0.3 \times I_{OUT}}$$

With a higher switching frequency, a lower inductance value can be selected to minimize the component size and improve transient response at the expense of reduced efficiency. With a lower switching frequency, a higher inductance value can be selected to reduce the inductor ripple current and achieve better efficiency. Select the inductor with low DC resistance and with a saturation current rating higher than the boost peak switch current limit.

$$I_{L_SAT} > I_{L_MAX} + \frac{\Delta I_{L_PK}}{2}$$

Input Capacitor

The input current of the boost converter is continuous and its RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and the maximum ESR using the following equations:

$$C_{IN} = \frac{\Delta I_L \times D}{4 \times f_{SW} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where:

$$\Delta I_L = \frac{(V_{IN} - V_{DS}) \times D}{f_{SW} \times L}$$

and, V_{DS} = Total voltage drop across the external MOSFET plus the voltage drop across the inductor ESR,

ΔI_L = Peak-to-peak inductor ripple current,

ΔV_Q = Portion of input ripple due to the capacitor discharge, ΔV_{ESR} = Contribution due to ESR of the capacitor. Assume the input capacitor ripple contribution due to ESR (ΔV_{ESR}) and capacitor discharge (ΔV_Q) are equal when using a combination of ceramic and aluminium capacitors. During the converter turn-on, a large current is drawn from the input source.

Output Capacitor

In a boost converter, the output capacitor supplies the load current when the main switch is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak-to-peak:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT}}$$

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

where D_{MAX} is the maximum duty cycle at the minimum input voltage. Use a combination of low-ESR ceramic and high-value, low-cost aluminum capacitors for lower output ripple and noise.

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Current Sense Resistor Selection

The current sense resistor R_{CS} connected between CSP and PGND3, sets the boost input current limit. The CSP input has 50mV (typ) voltage trip level. Set the current limit threshold above the peak switch current at the rated output power and minimum input voltage. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{V_{CS}}{I_{IN(MAX)}}$$

where $I_{IN(MAX)}$ is the peak current that flows through the MOSFET at full load and minimum V_{IN}.

$$I_{IN(MAX)} = \frac{I_{LOAD(MAX)}}{1 - D_{MAX}}$$

When the voltage across the current sense resistor by this current exceeds the current limit comparator threshold, the MOSFET driver (DL) quickly terminates the on-cycle.

MOSFET Selection

A wide variety of logic-level n-channel power MOSFETs can be used with the boost controller. To achieve the best performance, the key parameters to be considered in

MOSFET selection are as follows: maximum gate-source threshold voltage ($V_{GS(TH)}$), maximum continuous drain current (I_D), drain-source on-resistance ($R_{DS(ON)}$), maximum drain-source voltage (V_{DS}), and total gate charge (Qg). The boost controller low-side gate driver is powered by the internal 5V BIAS LDO output, or valid external supply connecting to EXTVCC. The chosen MOSFET must be a logic-level type with on-resistance specifications at V_{GS} = 4.5V or lower. The MOSFET must deliver the maximum input current ($I_{IN(MAX)}$) calculated in the *Current Sense Resistor Selection* section. The MOSFET must be chosen with an appropriate maximum drain-to-source voltage (V_{DS}) rating to cover all input voltage conditions. The MOSFET drain-source on-resistance ($R_{DS(ON)}$) is the parameter to decide the MOSFET conduction loss. The total gate charge (Qg) affects the MOSFET switching loss. Low $R_{DS(ON)}$ and low Qg are preferred to minimize the MOSFET power loss to achieve better efficiency.

Diode Selection

Schottky diodes with low forward voltage are recommended to be used. Lower forward voltage is preferred to minimize the diode power loss. The average current rating of the selected Schottky diode must exceed the peak current limit set by boost current sense resistor (R_{CS}). Its maximum reverse voltage rating should be selected above output voltage plus extra voltage stress.

Compensation Component Calculation

The boost regulation loop consists of power modulator, feedback resistor network, and error amplifier, as shown in Figure 1. The power modulator includes current sense circuitry (R_{CS}), the external MOSFET (Q) and rectifier diode (D), the inductor (L), output capacitor (C_{OUT} and its ESR), and the load (R_{LOAD}). Its transfer function is expressed below:

$$G(f) = gM(C) \times R_{LOAD} \times \frac{1 - D}{2} \times \frac{(1 + J\frac{f}{f_{Z_ESR}}) \times (1 - J\frac{f}{f_{Z_RHP}})}{1 + J\frac{f}{f_{P_LOAD}}}$$

where

$$gM(C) = \frac{1}{A_{V_CS} \times R_{CS}}$$

in S, and A_{V_CS} is the

gain of current sense amplifier, 24V/V. The double poles at half of switching frequency are neglected if it is well damped by slope compensation.

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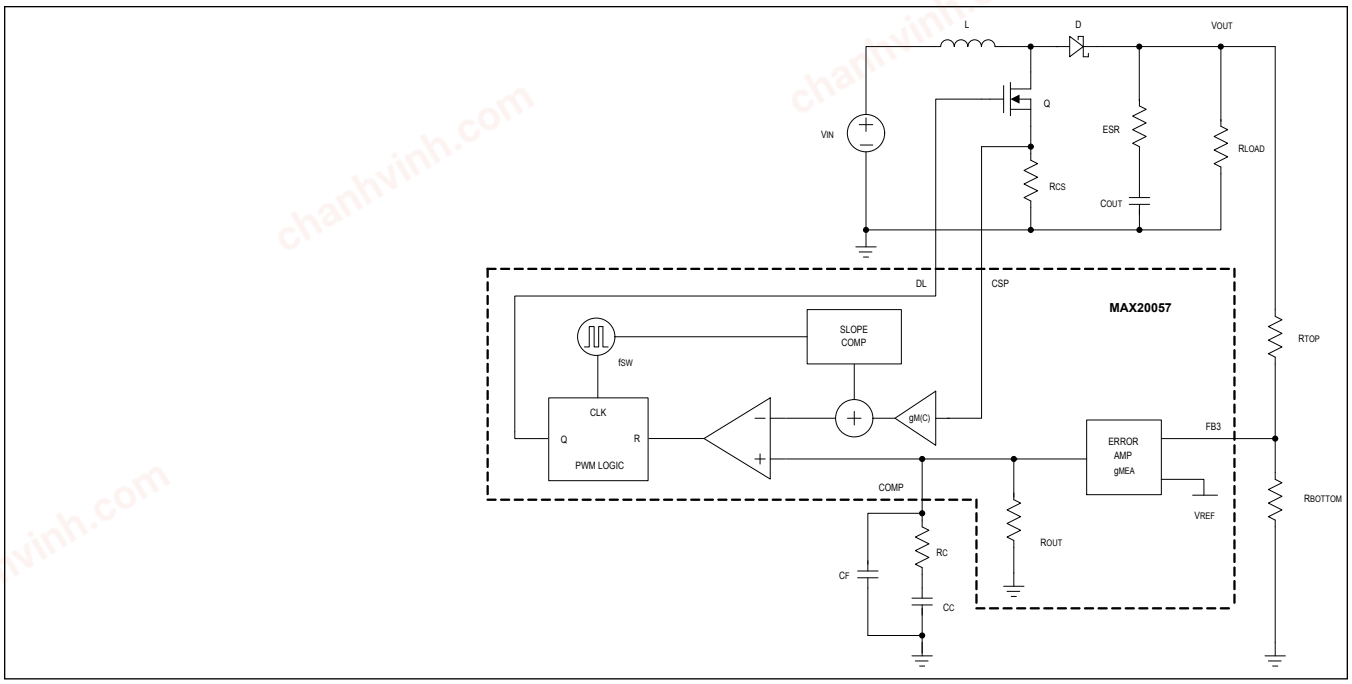


Figure 1. Boost Control Loop

Therefore, the power modulator DC gain,

$$G_{MOD}(DC) = \frac{R_{LOAD} \times (1 - D)}{2 \times A_{V_CS} \times R_{CS}}$$

The output capacitor and load resistance introduce a pole at:

$$f_{P_LOAD} = \frac{1}{\pi \times R_{LOAD} \times C_{OUT}}$$

The output capacitor and its ESR introduce a zero at:

$$f_{Z_ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The right half plane zero is:

$$f_{Z_RHP} = \frac{R_{LOAD} \times (1 - D)^2}{2 \times \pi \times L}$$

For feedback loop, its transfer function can be expressed as:

$$H(f) = gMEA \times R_{OUT_EA} \times \frac{R_{TOP}}{R_{TOP} + R_{BOTTOM}} \times \frac{1 - j\frac{f}{f_{Z_EA}}}{(1 + j\frac{f}{f_{P_EA}}) \times (1 + j\frac{f}{f_{P2_EA}})}$$

The DC gain of transconductance error amplifier is G_{EA} = gMEA × R_{OUT_EA}, where gMEA is the error-amplifier transconductance, which is 230µS (typ), and R_{OUT_EA} is the output resistance of the error amplifier, which is 4.5MΩ (typ).The dominant pole (f_{P_EA}) is set by the compensation capacitor C_C and the amplifier output resistance R_{OUT_EA}. A zero, f_{Z_EA}, is set by the compensation resistor RC and the compensation capacitor C_C. Another pole f_{P2_EA} set by C_F and R_C is optional to cancel the output capacitor ESR zero if it occurs near the crossover frequency f_C, where the loop gain equals 0dB. The error amplifier related pole and zero are calculated as:

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$$f_{P_EA} = \frac{1}{2 \times \pi \times R_{OUT_EA} \times R_C}$$

$$f_{Z_EA} = \frac{1}{2 \times \pi \times C_C \times R_C}$$

$$f_{P2_EA} = \frac{1}{2 \times \pi \times C_F \times R_C}$$

The loop gain crossover frequency, f_C, should be selected lower than 1/10 of switching frequency (f_{SW}) or 1/3 of right-half plane zero frequency (f_{Z_RHP}).

$$f_C \le \text{Lowerof} \frac{f_{SW}}{10} \text{or} \frac{f_{Z_RHP}}{3}$$

At the crossover frequency, the total loop gain equals 1. Therefore,

$$G_{MOD(f_C)} \times \frac{V_{FB3}}{V_{OUT3}} \times G_{EA}(f_C) = 1$$

$$G_{EA}(f_C) = \text{gMEA} \times R_C$$

$$G_{MOD(fC)} = G_{MOD}(DC) \times \frac{f_{P_LOAD}}{fc}$$

Using these formula to solve R_C:

$$R_C = \frac{V_{OUT}3}{\text{gMEA} \times V_{FB3} \times G_{MOD}(f_C)}$$

Set the zero formed by R_C and C_C at the power modulator pole (f_{P_LOAD}) to cancel this pole. Calculated the value of C_C as follows:

$$C_C = \frac{1}{2 \times \pi \times G_{MOD}(fc)}$$

If f_{Z_ESR} is less than 5 x f_C, add the second capacitor (C_F) from COMP3 to AGND to compensate f_{Z_ESR}. The value of C_F is calculated as:

$$C_F = \frac{1}{2 \times \pi \times f_{Z_ESR} \times R_C}$$

SEPIC Operation

For reference, see the example using the MAX20057 boost controller in SEPIC mode in Figure 2.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses, low EMI, and clean, stable operation. If possible, mount all power components on the top side of the board, and minimize the high frequency current loop as small as possible. Refer to the MAX20057 EV kit for an example layout. Follow these guidelines for good PCB layout.

For buck converters, place the input bypass capacitors as close to SUPSW1 and SUPSW2 as possible. The buck input capacitors deliver high di/dt current pulses when its high-side MOSFET turns on. Minimize the parasitic inductance in the power input traces to improve efficiency and reliability.

Minimize the connection from the buck output capacitor's ground terminal to the input capacitor's ground terminal for each buck regulator. This minimizes the area of current loop when the high-side MOSFET is conducting.

Keep buck high-current paths, and power traces wide and short. Minimize the traces from each buck LX node to each inductor and from each inductor to the output capacitors. This minimizes the buck current loop area

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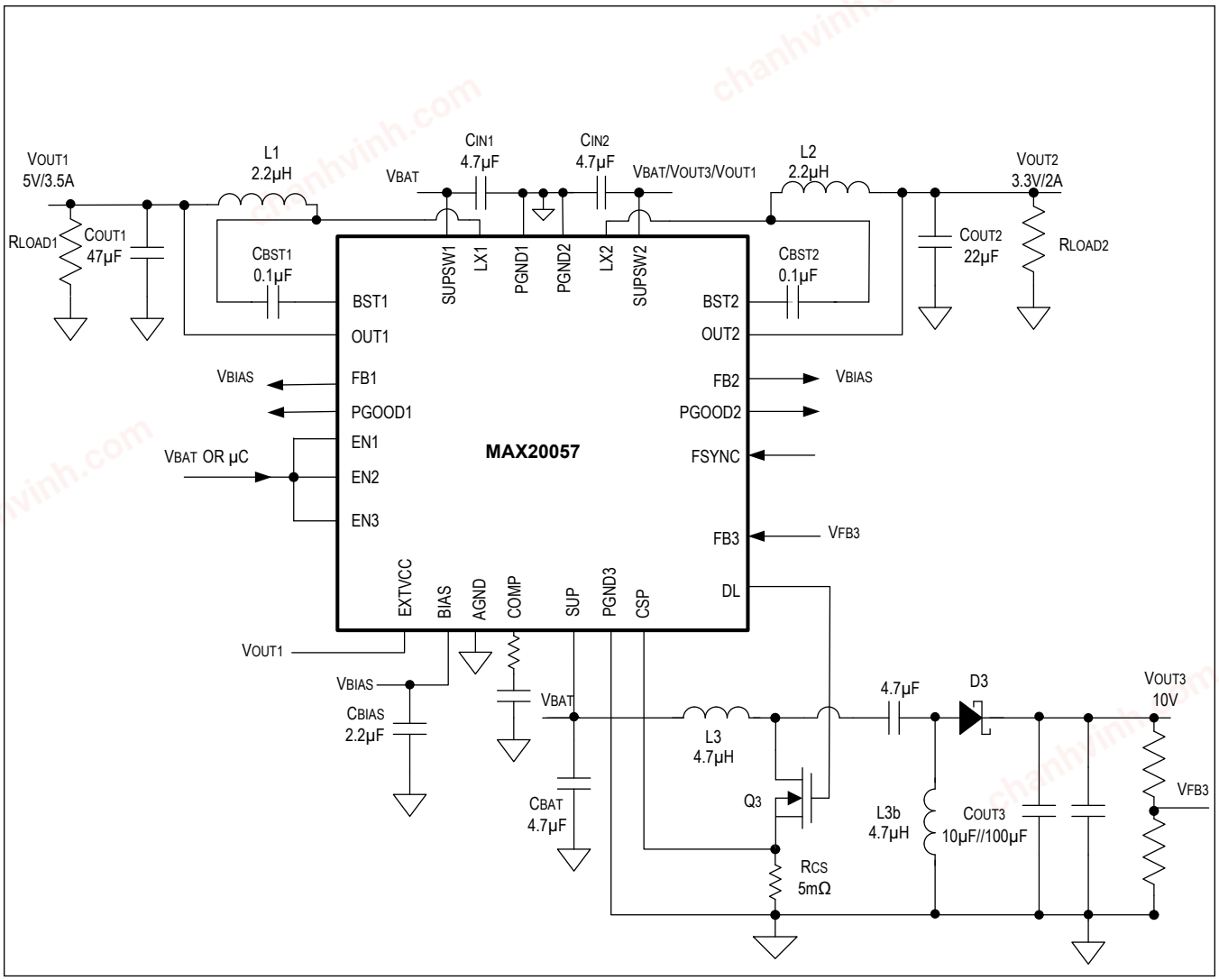


Figure 2. MAX20057 SEPIC Application Circuit

and minimizes LX trace resistance and stray capacitance to achieve optimal efficiency. Using thick copper PCBs (2 ounces vs. 1 ounce) can improve full load efficiency by 1% or more.

The boost controller loop, including the N-channel MOSFET, diode, and output capacitor has high di/dt current pulses. Keep this loop as small as possible.

The trace from the boost controller gate driver output DL to the gate of the low-side N-channel MOSFET should be wide and short. The gate driver has a high di/dt when switching. Minimized gate driver traces can reduce rising and falling time to further reduce the switching loss.

Connect the ground terminal of the current sense resistor, boost output capacitors, and PGND3 as close as possible.

Connect current sense resistor to CSP by Kelvin sensing connection to minimize current sensing error.

Keep all sensitive analog signals (FB1, FB2, FB3, and COMP3) away from noisy switching nodes (LX_, BST_, and DL) and high current loops.

Place the BIAS capacitor as close to the BIAS node as possible. Noise coupling into BIAS can disturb the reference and bias circuitry if this capacitor is installed away from the device.

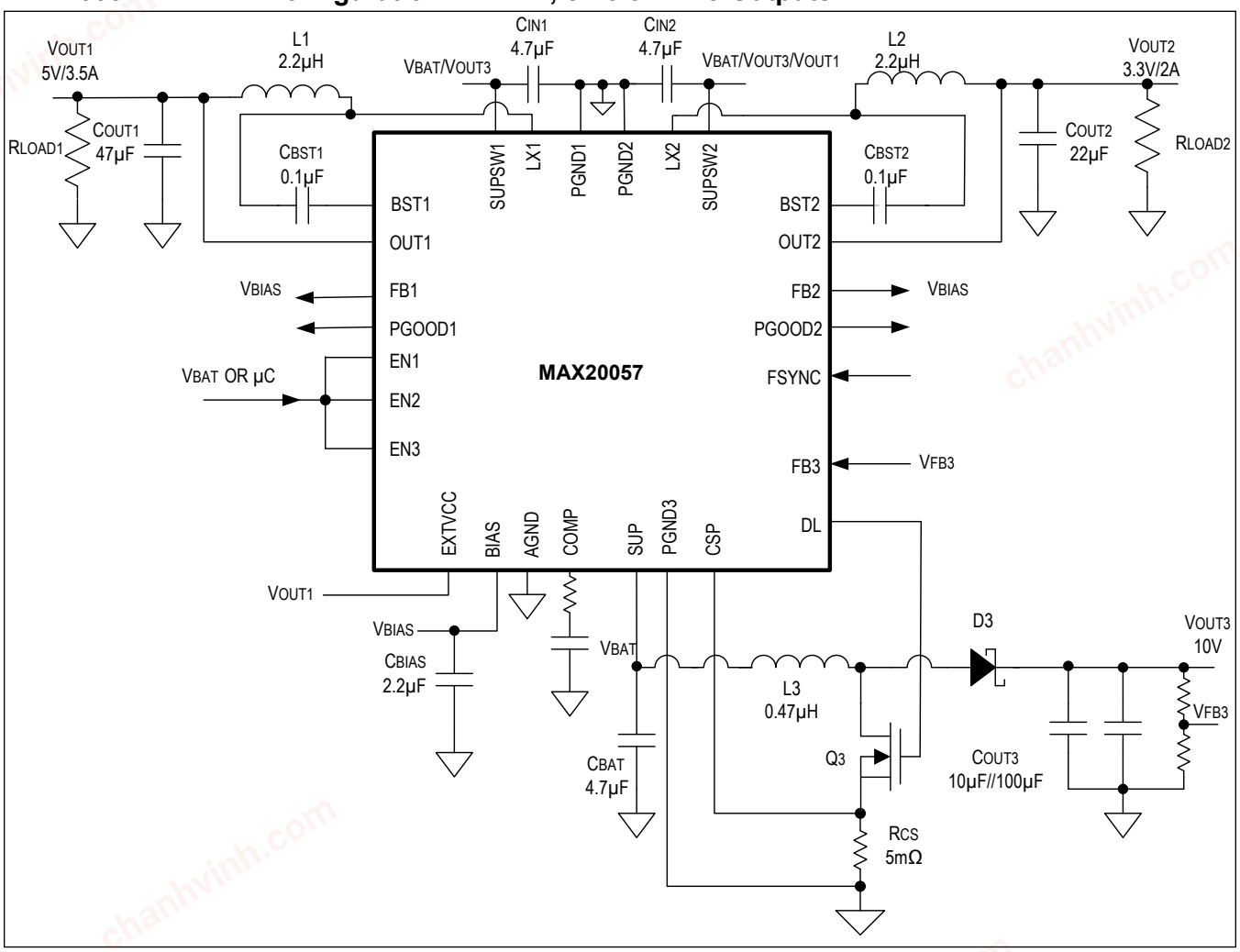
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Ground is the return path for the full load currents flowing into and out of the MAX20057. It is also the common reference voltage for all the analog circuits. Improper ground routing can bring extra resistance and inductance into the current loop, causing different voltage reference and worsening voltage ringing or spikes. Place a solid ground plane layer under the power loop components layer to shield the switching noise from other sensitive traces. Connect all the analog ground (AGND) and power grounds (PGND1, PGND2 and PGND3) together at a single point in a star ground connection. The IC exposed pad can be the point for ground connection.

The exposed pad under the bottom of the package is attached with epoxy to the substrate of the IC, making it an excellent path to remove heat from the IC. Connect the exposed pad to large ground plane areas through external or internal layers. Place multiple small vias under the exposed pad to effectively transfer heat down to the internal ground plane and the back side of the PCB to further improve the thermal resistance from the IC package to the ambient.

Typical Application Circuits

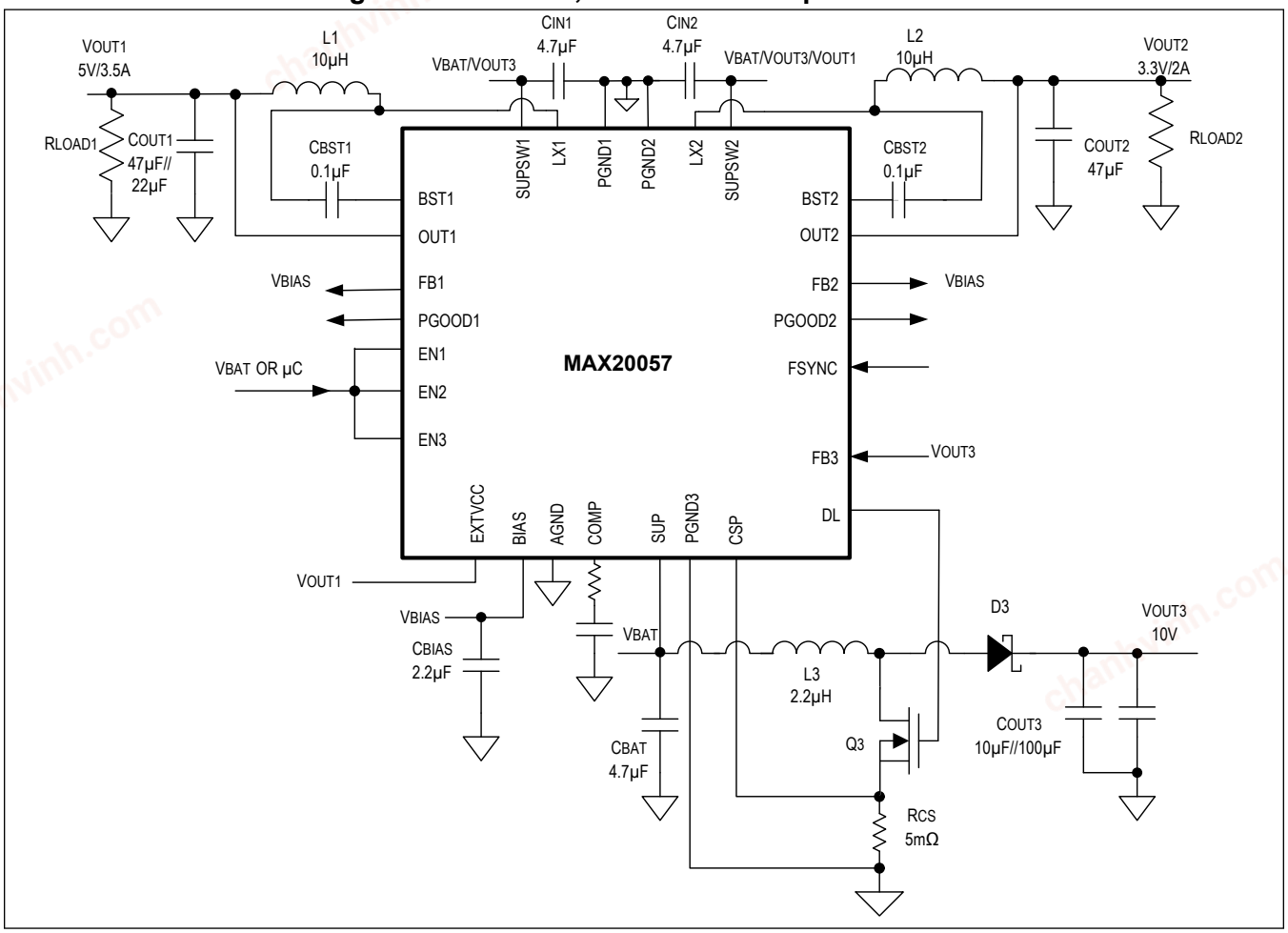
MAX20057ATIF/VY+ Configuration: 2.1MHz, 5V/3.3V/ADJ Outputs



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Typical Application Circuits (continued)

MAX20057ATIC/VY+ Configuration: 400kHz, 5V/3.3V/10V Outputs



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Ordering Information

PART NUMBER	VOUT OPTIONS (VOUT1/VOUT2/ VOUT3) (V)	SWITCHING FREQUENCY	SPREAD SPECTRUM	BOOST UVLO (FALLING)
MAX20057ATIA/VY+	3.3/5/ADJ	2.1MHz	OFF	ON
MAX20057ATIB/VY+	3.3/5/10	2.1MHz	ON	ON
MAX20057ATIC/VY+	5/3.3/10	400kHz	OFF	ON
MAX20057ATID/VY+	5/3.3/ADJ	400kHz	ON	ON
MAX20057ATIE/VY+	5/3.3/10	2.1MHz	OFF	ON
MAX20057ATIF/VY+	5/3.3/ADJ	2.1MHz	ON	ON
MAX20057ATII/VY+**	3.3/5/10	2.1MHz	ON	OFF
MAX20057ATIJ/VY+	5/3.3/11	2.1MHz	ON	ON

*** Future product—contact factory for availability*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

**EP = Exposed pad.*

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/18	Initial release	—
1	4/19	Updated output-voltage setting in *Applications Information* section, removed future-product designation from MAX20057ATIB/VY+ in *Ordering Information* section	14, 22
2	7/19	Removed all future-product designation from *Ordering Information* section	22
3	1/20	Added MAX20057ATII/VY+** and MAX20057ATIF/VY+** to *Ordering Information* section	22
4	3/20	Updated *Detailed Description* and *Ordering Information*	14, 22

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