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Kionix®	**± 8g / 16g / 32g / 64g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER: KX134-1211 Rev. 4.0 24-Nov-2021**

Product Description



The KX134-1211 is a tri-axis ±8g, ±16g, ±32g, or ±64g silicon micromachined accelerometer featuring a user-configurable 3-stage Advanced Data Path (ADP) consisting of a low-pass filter, low-pass/high-pass filter, and RMS calculation engine. The KX134-1211 accelerometer also features an advanced Wake-Up and Back-to-Sleep detection with a high-resolution threshold capability configurable down to 15.6 mg, 512-byte buffer that continues to record data even when being read, as well as embedded engines for orientation, Directional-Tap™/Double-Tap™, and Free fall detection. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device wafer. A separate ASIC device packaged with the sense element provides signal conditioning and intelligent user-programmable application algorithms. The KX134-1211 accelerometers offer lower noise and improved linearity over of the entire temperature range. The accelerometer is delivered in a 2 x 2 x 0.9 mm LGA 12-pin plastic package operating from a 1.7V – 3.6V (VDD) / 1.2V – 3.6V (IO_VDD) DC supplies. Internal voltage regulators are used to maintain constant internal operating voltages over the range of input supply voltages. This results in stable operating characteristics even if the supply voltage changes. I²C or SPI digital protocol is supported to configure the chip, read acceleration outputs, and check for updates to the orientation, Directional-Tap™/Double-Tap™ detection, Free fall detection, and activity monitoring algorithms. Two configurable interrupt pins are also available to show the output of the embedded detection algorithms.

Features

- Operating temperature range from -40ºC to +105ºC
- Small footprint: 2 x 2 x 0.9 mm LGA 12-pin package
- User-configurable g-range up to ±64g and Output Data Rate up to 25600Hz
- A user-configurable 3-stage Advanced Data Path (ADP) consisting of a low-pass filter, low-pass/high-pass filter, and RMS calculation engine.
- High resolution Wake-Up / Back-to-Sleep functions with threshold configurable down to 15.6 mg
- User accessible manufacturer and part ID registers
- Self-test Function
- Integrated Free fall, Directional-Tap™ / Double-Tap™, and Device-orientation algorithms
- Improved ODR accuracy in Low Power mode over temperature
- Embedded 512-byte FIFO buffer continues to record data even when being read
- User-selectable Low Power or High-Performance modes
- Internal voltage regulator
- Digital I²C up to 3.4MHz and Digital SPI up to 10MHz
- Excellent temperature performance with high shock survivability
- RoHS / REACH compliant

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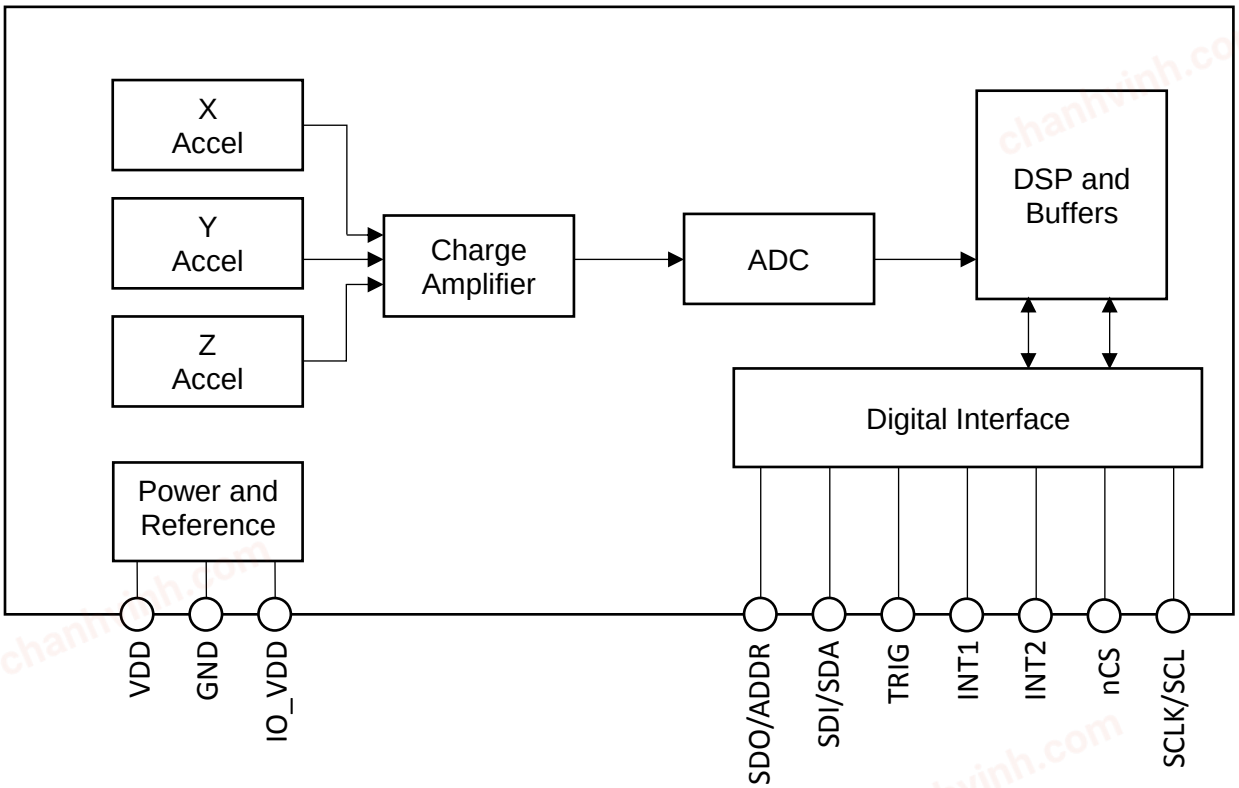
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Kionix®	**± 8g / 16g / 32g / 64g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER: KX134-1211 Rev. 4.0 24-Nov-2021**

Functional Diagram



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Product Specifications

Mechanical

(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		ºC	-40	-	+105
Zero-g Offset		mg		±75	±175
Zero-g Offset Variation from RT over Temp.		mg/ºC		0.5	
Sensitivity[1] (16 bit)	GSEL1=0, GSEL0=0 (±8g)	counts/g	3768	4096	4424
	GSEL1=0, GSEL0=1 (±16g)		1884	2048	2212
	GSEL1=1, GSEL0=0 (±32g)		942	1024	1106
	GSEL1=1, GSEL0=1 (±64g)		471	512	553
Sensitivity (Buffer 8-bit mode)[1,2]	GSEL1=0, GSEL0=0 (±8g)	counts/g		16	
	GSEL1=0, GSEL0=1 (±16g)			8	
	GSEL1=1, GSEL0=0 (±32g)			4	
	GSEL1=1, GSEL0=1 (±64g)			2	
Sensitivity Variation from RT over Temperature		%/ºC		0.01	
Positive Self-Test Output change on Activation		g	0.1	0.5	0.9
Mechanical Signal Bandwidth (-3dB)[3]		Hz		8200 (x) 8500 (y) 5600 (z)	
Non-Linearity		% of FS		0.6	
Cross Axis Sensitivity		%		2	
Noise[4]	RMS	mg		1.6	
	Density	µg/√Hz		300	

Table 1: Mechanical Specifications

Notes:

1. Resolution and acceleration ranges are user selectable via I^2C or SPI. Tolerance specified at ±1g stimulus.
2. Sensitivity is proportional to BRES in BUF_CNTL2.
3. Signal bandwidth varies with Output Data Rate (ODR), and Low Pass Filter setting. Measured with ODR = 25600Hz, LPRO = 1 settings.
4. Noise varies with ODR, power mode, and the Average Filter Control (AVC) settings. Measured with RES = 1, ODR = 50Hz, LPRO = 1, GSEL = 0 settings.

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Electrical

(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Operating	V	1.7	2.5	3.6
I/O Pads Supply Voltage (IO_VDD)	SPI, I²C (Fast/Standard mode)	V	1.2		3.6
	I²C (High Speed mode)		1.7		3.6
Current Consumption (Accelerometer Only)	Operating (High Performance with Wake-up Detection) ODR=400Hz	µA		148	
	Operating (Low power with Wake-up detection) ODR=0.781Hz[1]			0.53	
	Operating (Low Power with Wake-up detection plus Advanced Data Path) ODR=0.781Hz[7]			0.67	
Standby Current Consumption		µA		0.5	
Output Low Voltage (V_{OL}) [2]	(IO_VDD < 2V)	V	-	-	0.2 * IO_VDD
	(IO_VDD ≥ 2V)	V	-	-	0.4
Output High Voltage (V_{OH})		V	0.8 * IO_VDD	-	-
Input Low Voltage (V_{IL})		V	-	-	0.2 * IO_VDD
Input High Voltage (V_{IH})		V	0.8 * IO_VDD	-	-
Start Up Time[3]		ms	2		1300
Power Up Time[4]		ms		20	50
SPI Communication Rate		MHz			10
I²C Communication Rate		MHz		0.4	3.4
I²C Slave Address (7-bit)				0x1E / 0x1F	
WHO_AM_I register value				0x46	
Output Data Rate (ODR)[5]		Hz	0.781	50	25600
Output Signal Bandwidth (-3dB)[6]		Hz		ODR/9 or ODR/2	

Table 2: Electrical Specifications

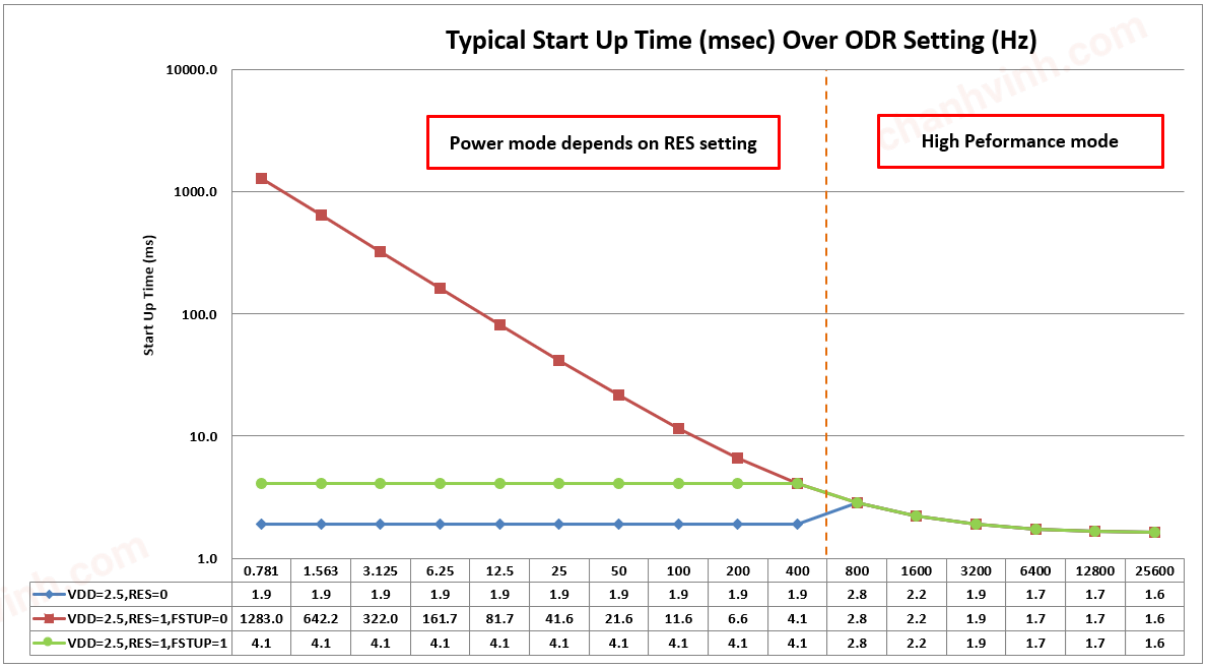
Notes:

1. Current varies with Output Data Rate (ODR) as shown in Figure 2, types and number of enabled digital engines, the average filter control settings, and VDD. Measured with OWUF<2:0> = 0, OSA<3:0> = 0, AVC<2:0> = 1, LPSTPSEL = 1.
2. For I²C communication, this assumes a minimum 1.5kΩ pull-up resistor on SCL and SDA pins.
3. Start up time is from PC1 set to valid outputs. Time varies with ODR, Power Mode, and FSTUP bit setting (see Figure 1).
4. Power up time is from VDD valid to device boot completion.
5. Typical values. ODR is user-selectable via I²C or SPI. See ODCNTL register for details.
6. Refers to accelerometer's raw output data. Additional bandwidth control is available using the Advanced Data Path (ADP) engine.
7. Measured with RMS_AVC<2:0> = 1, OADP<3:0> = 0, LPSTPSEL = 0.

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Start Up Time Profile



	0.781	1.563	3.125	6.25	12.5	25	50	100	200	400	800	1600	3200	6400	12800	25600
VDD=2.5,RES=0	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	2.8	2.2	1.9	1.7	1.7	1.6
VDD=2.5,RES=1,FSTUP=0	1283.0	642.2	322.0	161.7	81.7	41.6	21.6	11.6	6.6	4.1	2.8	2.2	1.9	1.7	1.7	1.6
VDD=2.5,RES=1,FSTUP=1	4.1	4.1	4.1	4.1	4.1	4.1	4.1	4.1	4.1	4.1	2.8	2.2	1.9	1.7	1.7	1.6

Figure 1: Start Up Time Diagram

Current Profile

ODR (Hz)	Typical Current (µA)			
	High Performance with Wake-up	High Performance with Wake-up & ADP	Low Power with Wake-up	Low Power with Wake-up & ADP
Standby	0.50	0.50	0.50	0.50
0.781	148	148	0.53	0.67
1.563	148	148	0.60	0.74
3.125	148	148	0.72	0.83
6.25	148	148	0.97	1.14
12.5	148	148	1.5	1.7
25	148	148	2.4	2.7
50	148	148	4.4	4.9
100	148	148	8.5	9.2
200	148	150	16	18
400	148	150	31	34
800	148	152	148	152
1600	149	154	149	154
3200	150	160	150	160
6400	152	172	152	172
12800	155	194	155	194
25600	162	239	162	239

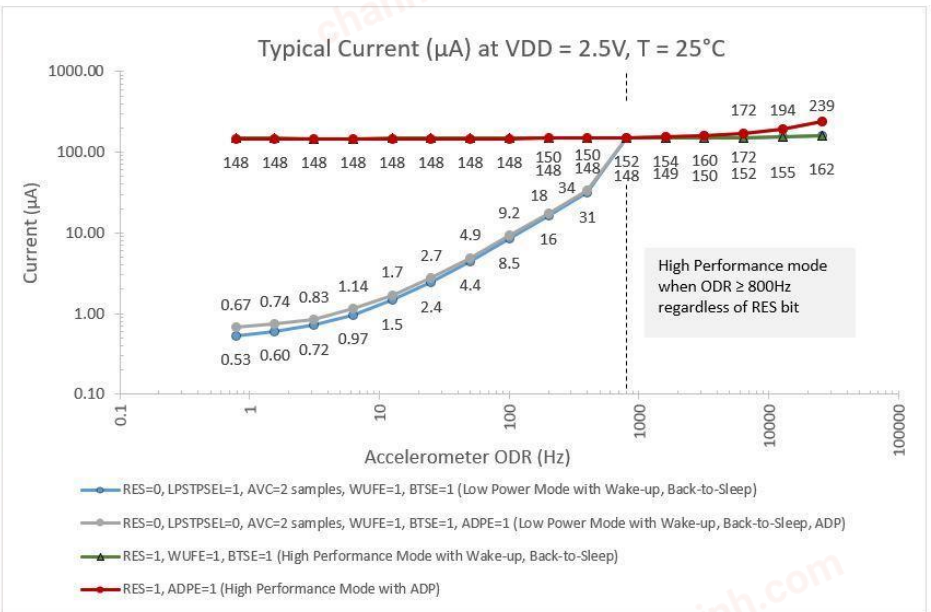


Figure 2: Current as a function of Output Data Rate (ODR) and Power Mode Settings

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Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD, VDD_{LOW}**, **T_{VDD}** (rise time), and **T_{VDD_OFF}** profile of individual applications. It is recommended to minimize **VDD_{LOW}**, and **T_{VDD}**, and maximize **T_{VDD_OFF}**. It is also advised that the **VDD** ramp up time **T_{VDD}** be monotonic. Note that the outputs will not be stable until **VDD** has reached its final value.

To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD_{LOW}, T_{VDD}, T_{VDD_OFF} and temperature as POR performance can vary depending on these parameters.

Please refer to Technical Note ***TN027 Power-On Procedure*** for more information.

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Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Absolute Limits	V	-0.3	-	3.60
Operating Temperature Range		ºC	-40	-	+105
Storage Temperature Range		ºC	-55	-	+150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Table 3: Environmental Specifications



Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.







This product is in conformance with RoHS directive, REACH regulation, and is Halogen-Free. For the current certificate of compliance, visit www.kionix.com website.

Handling, Mounting, Soldering

For package handling, mounting, and soldering guidelines, see TN007 Package Handling, Mounting, and Soldering Guidelines technical note.

Floor Life

Factory floor life exposure of the KX134-1211 reels removed from the moisture barrier bag should not exceed a maximum of 168 hours at 30C/60%RH. If this floor life is exceeded, the parts should be dried per the IPC/JEDEC J-STD-033D standard (or latest revision).

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Terminology

g

A unit of acceleration equal to the acceleration of gravity at the earth's surface.

$$1g = 9.8 \frac{m}{s^2}$$

One thousandth of a g (0.0098 m/ s^2) is referred to as 1 milli-g (1 mg).

Sensitivity

The sensitivity of an accelerometer is the change in output per unit of input acceleration at nominal VDD and temperature. The term is essentially the gain of the sensor expressed in counts per g (counts/g) or LSB's per g (LSB/g). Occasionally, sensitivity is expressed as a resolution, i.e. milli-g per LSB (mg/LSB) or milli-g per count (mg/count). Sensitivity for a given axis is determined by measurements of the formula:

$$Sensitivit \quad y = \frac{(Output \quad @ + 1g - Output \quad @ - 1g)}{2g}$$

The sensitivity tolerance describes the range of sensitivities that can be expected from a large population of sensors at room temperature and over life. When the temperature deviates from room temperature (25ºC), the sensitivity will vary by the amount shown in Table 1.

Zero-g offset

Zero-g offset or 0-g offset describes the actual output of the accelerometer when no acceleration is applied. Ideally, the output would always be in the middle of the dynamic range of the sensor (content of the OUTX, OUTY, OUTZ registers = 00, expressed as a 2's complement number). However, because of mismatches in the sensor, calibration errors, and mechanical stress, the output can deviate from 00. This deviation from the ideal value is called 0-g offset. The zero-g offset tolerance describes the range of 0-g offsets of a population of sensors over the operating temperature range.

Self-test

Self-test allows a functional test of the sensor without applying a physical acceleration to it. When activated, an electrostatic force is applied to the sensor, simulating an input acceleration. The sensor outputs respond accordingly. If the output signals change within the amplitude specified in Table 1, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

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Functionality

Sense element

The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. This process technology allows Kionix to create mechanical silicon structures, which are essentially mass-spring systems that move in the direction of the applied acceleration. Acceleration sensing is based on the principle of a differential capacitance arising from the acceleration-induced motion. Capacitive plates on the moving mass move relative to fixed capacitive plates anchored to the substrate. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit.

ASIC interface

A separate ASIC device packaged with the sense element provides all of the signal conditioning and communication with the sensor. The complete measurement chain is composed by a low-noise capacitance to voltage amplifier, which converts the differential capacitance of the MEMS sensor into an analog voltage that is sent through an analog-to-digital converter. The acceleration data may be accessed through the I^2C or SPI digital communications provided by the ASIC. In addition, the ASIC contains all of the logic to allow the user to choose data rates, g-ranges, filter settings, and interrupt logic.

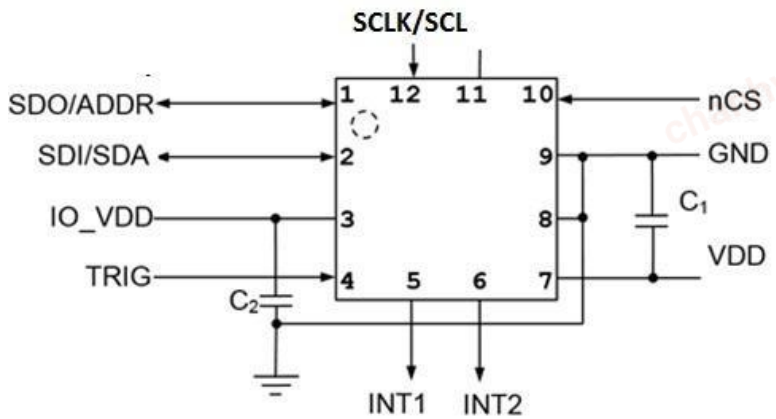
Factory calibration

Kionix trims the offset and sensitivity of each accelerometer by adjusting gain (sensitivity) and 0-g offset trim codes stored in nonvolatile memory (OTP). Additionally, all functional register default values are also programmed into the nonvolatile memory. Every time the device is turned on or a software reset command is issued, the trimming parameters and default register values are downloaded into the volatile registers to be used during active operation. This allows the device to function without further calibration.

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Application Schematic



Pin Description

Pin	Name	Description
1	SDO/ADDR	Serial Data Out pin during 4-wire SPI communication and part of the device address during I2C communication. Do not leave floating.
2	SDI/SDA	SPI Data input / I2C Serial Data
3	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
4	TRIG	Trigger pin for FIFO buffer control. Connect to GND when not using external trigger option.
5	INT1	Physical Interrupt 1 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used.
6	INT2	Physical Interrupt 2 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used.
7	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
8	GND	Ground
9	GND	Ground
10	nCS	Chip Select (active LOW) for SPI communication. Connect to IO_VDD for I2C communication. Do not leave floating.
11	NC	Not Internally Connected. Can be connected to VDD, IO_VDD, GND or leave floating.
12	SCLK/SCL	SPI and I2C Serial Clock

Table 4: Pin Description

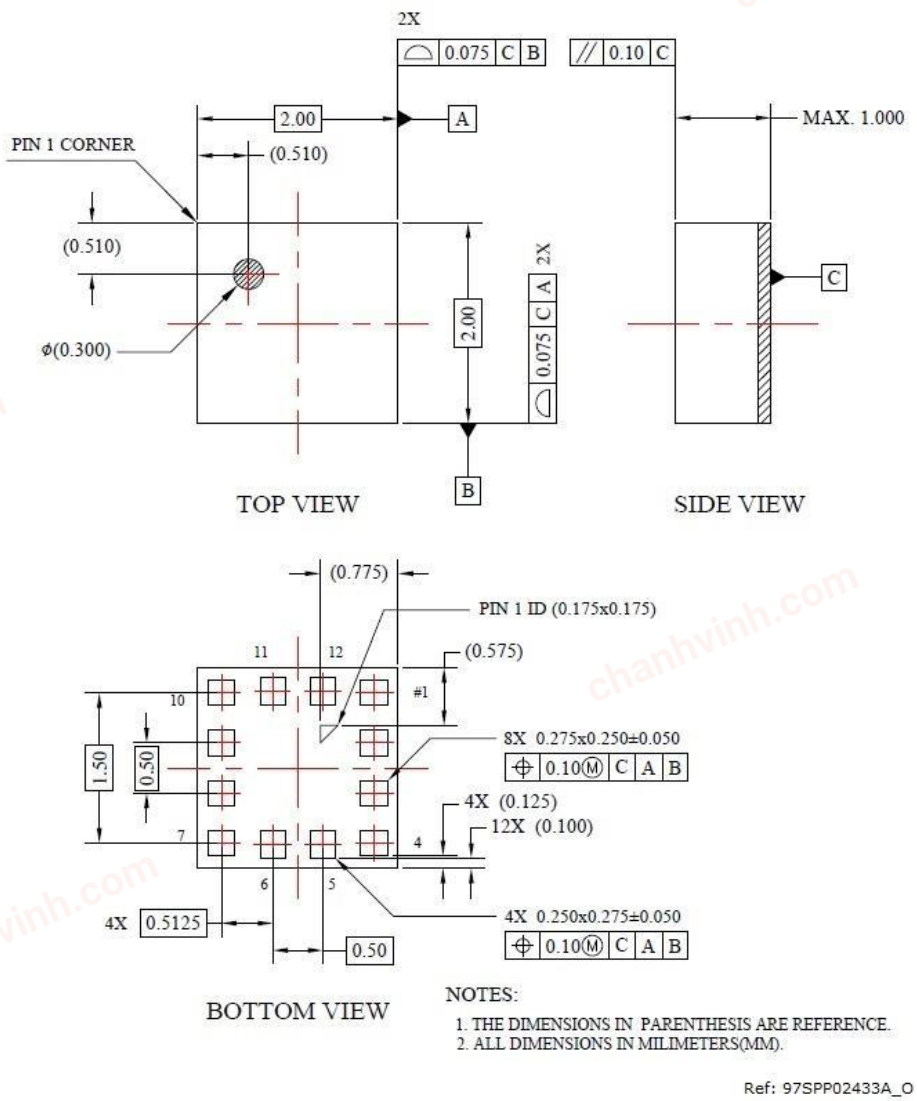
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Package Dimensions and Orientation

Dimensions

2 x 2 x 0.9 mm LGA 12-pin

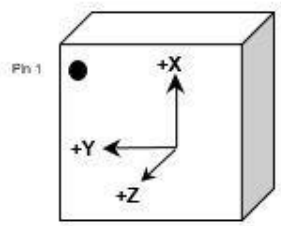


All dimensions and tolerances conform to ASME Y14.5M-1994

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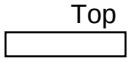
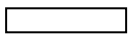
Orientation

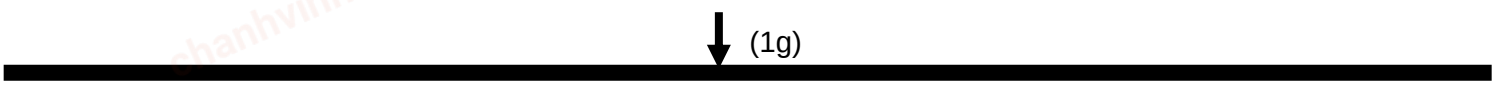


When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=0 (±8g)

Position	1		2		3		4		5		6	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	+4096	+16	0	0	-4096	-16	0	0	0	0	0	0
Y (counts)	0	0	-4096	-16	0	0	+4096	+16	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	+4096	+16	-4096	-16
X-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Y-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	



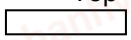
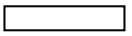
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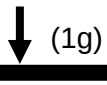
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Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=1 (±16g)

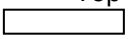
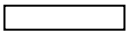
Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	+2048	+8	0	0	-2048	-8	0	0	0	0	0	0
Y (counts)	0	0	-2048	-8	0	0	+2048	+8	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	+2048	+8	-2048	-8
X-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Y-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	



Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=1, GSEL0=0 (±32g)

Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	+1024	+4	0	0	-1024	-4	0	0	0	0	0	0
Y (counts)	0	0	-1024	-4	0	0	+1024	+4	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	+1024	+4	-1024	-4
X-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Y-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	



Earth's Surface

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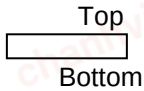
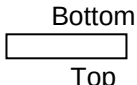
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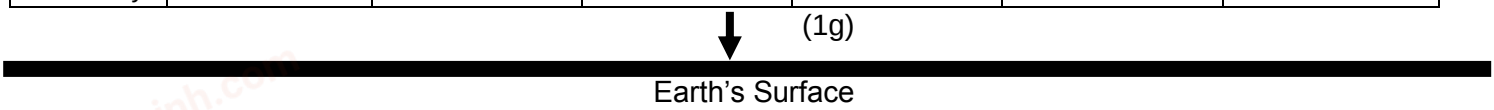
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Kionix®	**± 8g / 16g / 32g / 64g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER: KX134-1211 Rev. 4.0 24-Nov-2021**

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=1, GSEL0=1 (±64g)

Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram									 Top Bottom		 Bottom Top	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	+512	+2	0	0	-512	-2	0	0	0	0	0	0
Y (counts)	0	0	-512	-2	0	0	+512	+2	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	+512	+2	-512	-2
X-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Y-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	



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Digital Interface

The Kionix KX134-1211 digital accelerometer can communicate via the I²C and SPI digital serial interface protocols. This allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers. Note that if the KX134-1211 is accessed with incomplete I²C protocol such as communication without the Stop Condition before SPI communication, it would cause a miss-behavior. For more detail information, please refer the “KX134-1211-Technical-Reference-Manual”.

The serial interface terms and descriptions as indicated in Table 5 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 5: Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KX134-1211 can communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KX134-1211 always operates as a Slave device during standard Master-Slave I²C operation.

I²C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I²C bus is considered free when both lines are HIGH.

The I²C interface is compliant with high-speed mode, fast mode and standard mode I²C protocols.

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I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The KX134-1211 Slave Address is comprised of a user programmable part, a factory programmable part, and a fixed part, which allows for connection of multiple accelerometers to the same I²C bus. The Slave Address associated with the KX134-1211 is 00111YX, where the user programmable bit X, is determined by the assignment of ADDR (pin 1) to GND or IO_VDD. Also, the factory programmable bit Y is set at the factory. **For KX134-1211, the factory programmable bit Y is fixed to 1** (contact your Kionix sales representative for list of available devices). Table 6 lists possible I²C addresses for KX134-1211. As a result, up to four accelerometers can be implemented on a shared I²C bus as shown in Figure 3 (e.g. two KX134-1211 accelerometers and two other accelerometers with factory programmable bit Y set to **0**).

									Y	X	
Description	**ADDR pin**	**7-bit Address**	**Address**	**<7>**	**<6>**	**<5>**	**<4>**	**<3>**	**<2>**	**<1>**	**<0>**
I2C Wr	GND	0x1E	0x3C	0	0	1	1	1	1	0	0
I2C Rd	GND	0x1E	0x3D	0	0	1	1	1	1	0	1
I2C Wr	IO_VDD	0x1F	0x3E	0	0	1	1	1	1	1	0
I2C Rd	IO_VDD	0x1F	0x3F	0	0	1	1	1	1	1	1

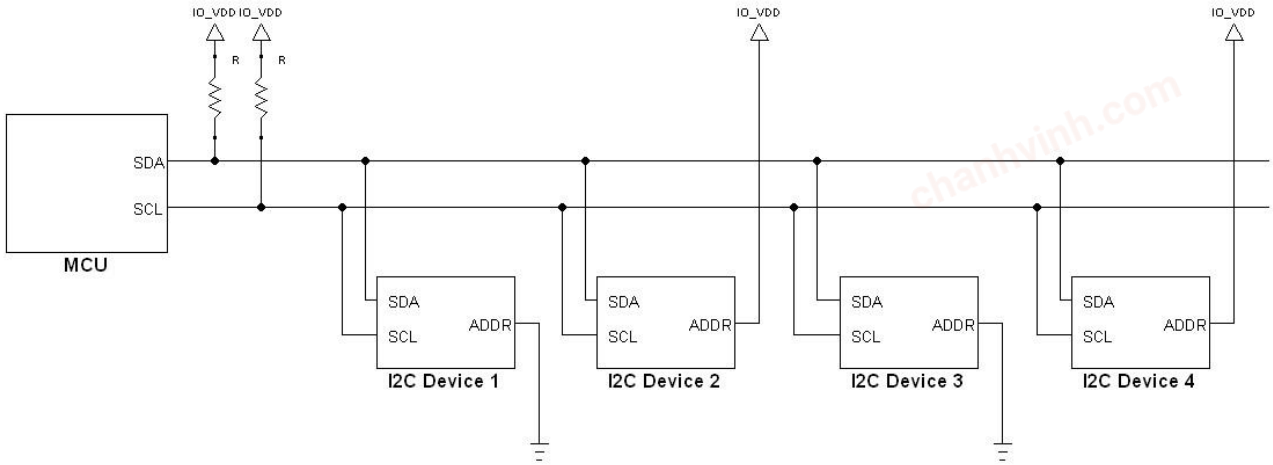
Table 6: I²C Slave Addresses for KX134-1211

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line LOW so that it remains stable LOW during the HIGH period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from LOW to HIGH while SCL is HIGH. The I²C bus is now free. Note that if the KX134-1211 is accessed through I²C protocol before the startup is finished a NACK signal is sent.

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I²C Device	Part Number	ADDR Pin	Slave Address	Bit Y (Bit 1 in 7-bit address)
1	KX134-1211	GND	0x1E	Factory Set to 1
2	KX134-1211	IO_VDD	0x1F	Factory Set to 1
3	*KXMMM	GND	0x1C	Factory Set to 0
4	*KXMMM	IO_VDD	0x1D	Factory Set to 0

* KXMMM – contact Kionix sales representative for list of compatible devices

Figure 3: Multiple KX134-1211 Accelerometers on a Shared I²C Bus

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Writing to an 8-bit Register

Upon power up, the Master must write to the KX134's control registers to set its operational mode. Therefore, when writing to a control register on the I^2C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KX134-1211 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KX134-1211 to which 8-bit register the Master will be writing the data. Since this is I^2C mode, the LSB of the RA command should always be zero (0). The KX134-1211 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KX134-1211 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KX134-1211 is now stored in the appropriate register. The KX134-1211 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.
Note** If a STOP condition is sent on the least significant bit of write data or the following master acknowledge cycle, the last write operation is not guaranteed and it may alter the content of the affected registers

Reading from an 8-bit Register

When reading data from a KX134-1211 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KX134-1211 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KX134-1211 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KX134-1211 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KX134-1211 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page. Reading data from a buffer read register is a special case because if register address (RA) is set to buffer read register (BUF_READ) in Sequence 4, the register auto-increment feature is automatically disabled. Instead, the Read Pointer will increment to the next data in the buffer, thus allowing reading multiple bytes of data from the buffer using a single SAD+R command.
Note** Accelerometer's output data should be read in a single transaction using the auto-increment feature to prevent output data from being updated prior to intended completion of the read transaction.

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Data Transfer Sequences

The following information illustrates the variety of data transfers that can occur on the I²C bus and how the Master and Slave interact during these transfers. Table 7 defines the I²C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 7: I²C Terms

Sequence 1: The Master is writing one byte to the Slave

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2: The Master is writing multiple bytes to the Slave

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3: The Master is receiving one byte of data from the Slave

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4: The Master is receiving multiple bytes of data from the Slave

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

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HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5: HS-mode data transfer of the Master writing multiple bytes to the Slave

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	Sr	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

n bytes + ack.

Sequence 6: HS-mode data transfer of the Master receiving multiple bytes of data from the Slave

Speed	FS-mode			HS-mode				
Master	S	M-code	NACK	Sr	SAD + W		RA	
Slave						ACK		ACK

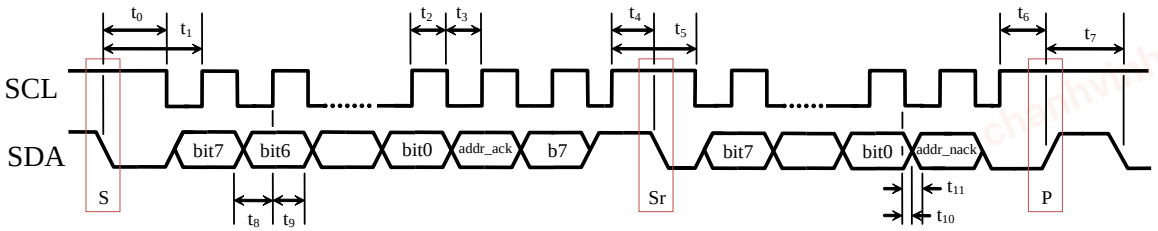
Speed	HS-mode								FS-mode
Master	Sr	SAD + R					NACK	P	
Slave			ACK	DATA	ACK	DATA			

(n-1) bytes + ack.

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I²C Timing Diagram



Number	Description	MIN	MAX	Units
t_0	SDA LOW to SCL LOW transition (Start event)	50	-	ns
t_1	SDA LOW to first SCL rising edge	100	-	ns
t_2	SCL pulse width: HIGH	100	-	ns
t_3	SCL pulse width: LOW	100	-	ns
t_4	SCL HIGH before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: HIGH during a S/Sr/P event	100	-	ns
t_6	SCL HIGH before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: HIGH	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I²C CLK	2.5	-	µs

Table 8: I²C Timing (Fast Mode)

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SPI Communications

4-Wire SPI Interface

The KX134-1211 also utilizes an integrated 4-Wire Serial Peripheral Interface (SPI) for digital communication. The SPI interface is primarily used for synchronous serial communication between one Master device and one or more Slave devices. The Master, typically a micro controller, provides the SPI clock signal (SCLK) and determines the state of Chip Select (nCS). The KX134-1211 always operates as a Slave device during standard Master-Slave SPI operation.

4-wire SPI is a synchronous serial interface that uses two control and two data lines. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDI or MOSI) and the Data Input (SDO or MISO) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes LOW at the start of transmission and goes back HIGH at the end. The Slave Data Output (SDO) line, remains in a high-impedance (hi-z) state when the device is not selected, so it does not interfere with any active devices. This allows multiple Slave devices to share a master SPI port as shown in Figure 4 below.

NOTE: if the MOSI line has the code 0x3C, 0x3D, 0x3D or 0x3F, it might cause a misbehavior in the KX134-1211. Please toggle nCS of the KX134-1211 L/H to recover the misbehavior condition.

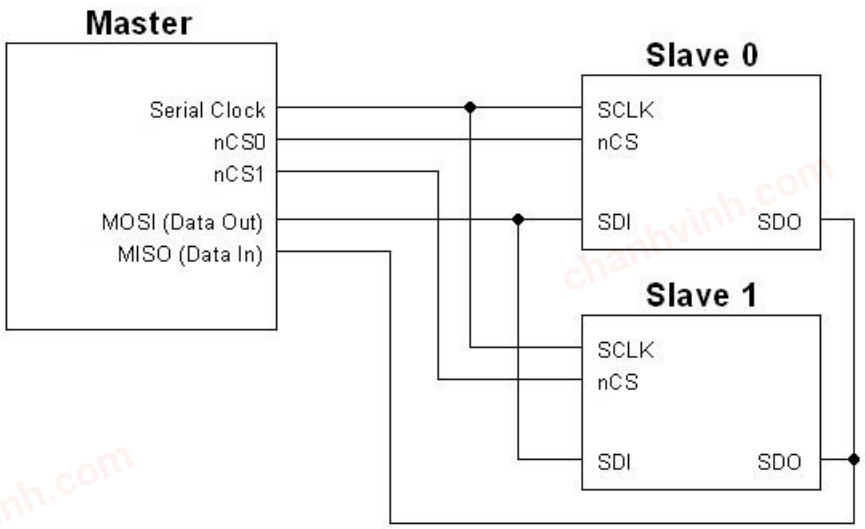
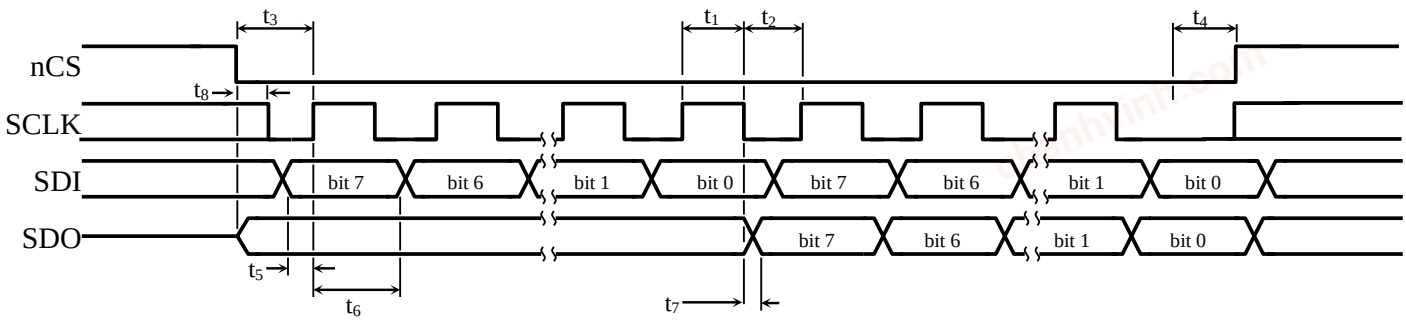


Figure 4. 4-wire SPI Connections

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4-Wire SPI Timing Diagram



Number	Description	MIN	MAX	Units
t_1	CLK pulse width: HIGH	45		ns
t_2	CLK pulse width: LOW	45		ns
t_3	nCS LOW to first CLK rising edge	20		ns
t_4	nCS LOW after the final CLK rising edge to nCS HIGH	20		ns
t_5	SDI valid to CLK rising edge	10		ns
t_6	CLK rising edge to SDI invalid	10		ns
t_7	CLK falling edge to SDO valid		35	ns
t_8	nCS LOW to first CLK falling edge	10		ns

Table 9: 4-Wire SPI Timing

Notes

1. t_7 is only present during reads.
2. Timings are for VDD of 1.8V to 3.6V with 1kΩ pull-up resistor and maximum 20pF load capacitor on SDO.

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4-Wire Read and Write Registers

The registers embedded in the KX134-1211 accelerometer have 8-bit addresses. Upon power up, the Master must write to the accelerometer's control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate "0" when writing to the register and "1" when reading from the register. This operation occurs over 16 clock cycles. All commands are sent MSB first. **The host must return nCS HIGH for at least one clock cycle before the next data request.** However, when data is being read from a buffer read register (BUF_READ), the nCS signal can remain LOW until the buffer is read. Figure 5 below shows the timing diagram for carrying out an 8-bit register write operation.

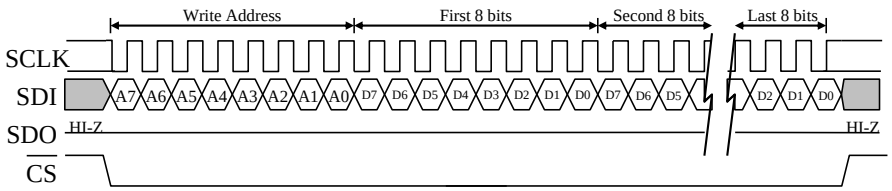


Figure 5: Timing Diagram for 8-Bit Register Write Operation

In order to read an 8-bit register, an 8-bit register address must be written to the accelerometer to initiate the read. The MSB of this register address byte will indicate "0" when writing to the register and "1" when reading from the register. Upon receiving the address, the accelerometer returns the 8-bit data stored in the addressed register. This operation also occurs over 16 clock cycles. All returned data is sent MSB first, and the host must return nCS HIGH for at least one clock cycle before the next data request. Figure 6 shows the timing diagram for an 8-bit register read operation.

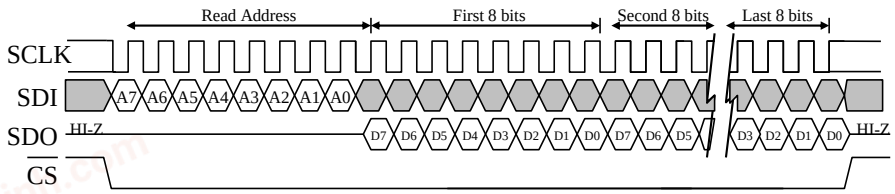


Figure 6: Timing Diagram for 8-Bit Register Read Operation

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3-Wire SPI Interface

The KX134-1211 also utilizes an integrated 3-Wire Serial Peripheral Interface (SPI) for digital communication. 3-wire SPI is a synchronous serial interface that uses two control lines and one data line. With respect to the Master, the Serial Clock output (SCLK), the Data Output/Input (SDI) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes LOW at the start of transmission and goes back HIGH at the end. This allows multiple Slave devices to share a master SPI port as shown in Figure 7 below.

NOTE: if the MOSI line has the code 0x3C, 0x3D, 0x3D or 0x3F, it might cause a misbehavior in the KX134-1211. Please toggle nCS of the KX134-1211 L/H to recover the misbehavior condition.

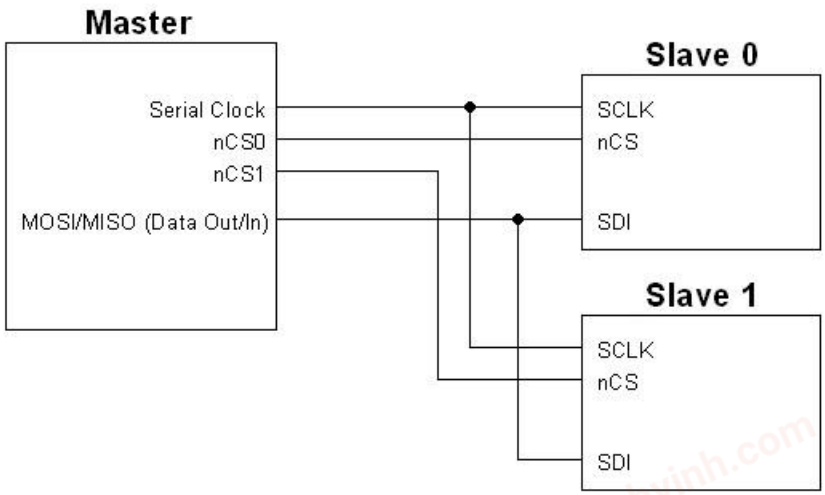
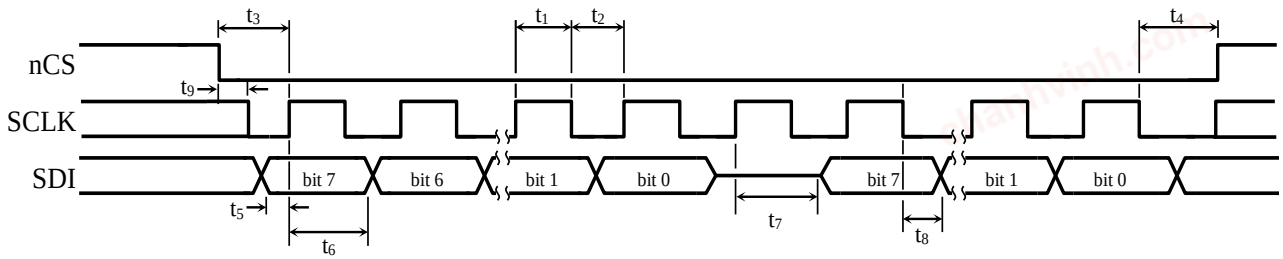


Figure 7: KX134-1211 3-wire SPI Connections

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3-Wire SPI Timing Diagram



Number	Description	MIN	MAX	Units
t_1	CLK pulse width: HIGH	45	-	ns
t_2	CLK pulse width: LOW	45	-	ns
t_3	nCS LOW to first CLK rising edge	20	-	ns
t_4	nCS LOW after the final CLK falling edge to nCS HIGH	20	-	ns
t_5	SDI valid to CLK rising edge	10	-	ns
t_6	CLK rising edge to SDI input invalid	10	-	ns
t_7	CLK extra clock cycle rising edge to SDI output becomes	-	-	ns
t_8	CLK falling edge to SDI output becomes valid	-	35	ns
t_9	nCS LOW to first CLK falling edge	10		ns

Table 10: 3-Wire SPI Timing

Notes

1. t_7 and t_8 are only present during reads
2. Timings are for VDD of 1.8V to 3.6V with 1kΩ pull-up resistor and maximum 20pF load capacitor on SDI.
3. The SDO/ADDR pin is configured in a high-impedance input-state, and must be externally tied to GND or IO_VDD

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3-Wire Read and Write Registers

The registers embedded in the KX134-1211 accelerometer have 8-bit addresses. Upon power up, the Master must write to the accelerometer's control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate "0" when writing to the register and "1" when reading from the register. A read operation and a write operation occurs over 16 clock cycles. All commands are sent MSB first. **The host must return nCS HIGH for at least one clock cycle before the next data request**. However, when data is being read from a buffer read register (BUF_READ), the nCS signal can remain LOW until the buffer is read. Figure 8 below shows the timing diagram for carrying out an 8-bit register write operation.

NOTE** If a STOP condition is sent on the least significant bit of write data or the following master acknowledge cycle, the last write operation is not guaranteed and it would cause unexpected register write.

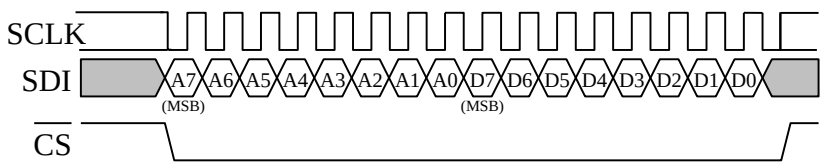


Figure 8: Timing Diagram for 8-Bit Register Write Operation

In order to read an 8-bit register, an 8-bit register address must be written to the accelerometer to initiate the read. The MSB of this register address byte will indicate "0" when writing to the register and "1" when reading from the register. Upon receiving the address, the accelerometer returns the 8-bit data stored in the addressed register. All returned data is sent MSB first, and the host must return nCS HIGH for at least one clock cycle before the next data request. Figure 9 shows the timing diagram for an 8-bit register read operation.

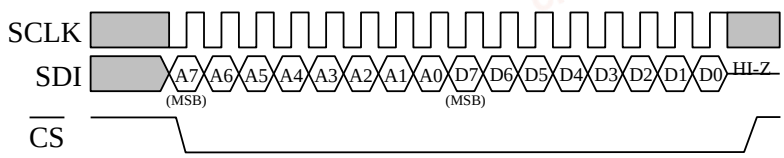


Figure 9: Timing Diagram for 8-Bit Register Read Operation

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Kionix®	**± 8g / 16g / 32g / 64g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER: KX134-1211 Rev. 4.0 24-Nov-2021**

Revision History

Revision	Description	Date
1.0	Production Release.	31-Jul-2019
2.0	Added SPI communication maximum rate and I2C communication typical rate in Electrical Specifications table. Updated Note 1 (Sensitivity) under Mechanical Specifications table to indicate that tolerance specified at ±1g stimulus. Revised Noise measurement test condition description. Removed a note under Mechanical Specification table to change the value of STPOL bit to perform the self-test since the POR value of the bit should be used.	06-Feb-2020
3.0	Updated the “Digital Interface” section description to include I2C transaction without stop condition on a shared bus with another SPI device. Updated the “4-Wire SPI Timing Diagram” to include SCLK start-H condition. Added t8 parameter in the “4-Wire SPI Timing” table. Updated the “Timing Diagram for 8-Bit Register Write Operation” figure to include SCLK start-H condition. Updated the “Timing Diagram for 8-Bit Register Read Operation” figure to include SCLK start-H condition. Updated the “3-Wire SPI Timing Diagram” timing figure to include start-H condition. Added t9 parameter in the “3-Wire SPI Timing” table. Updated description for noise measurement conditions.(GSEL=0)	30-Nov-2020
4.0	Revised Noise RMS from 1.9 to 1.6 in Mechanical Specifications. Removed description of SCL clock stretching in I^2C Serial Interface. Revised t11 description of Table 8 in I2C Timing Diagram. Revised description and Figure 9 about extra clock in 3-Wire Read and Write Registers. Add Note of SPI communication in 3-Wire SPI Interface and 4-Wire SPI Interface.	24-Nov-2021

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Appendix

The following Notice is included to guide the use of Kionix products in its application and manufacturing processes. Kionix, Inc., is a ROHM Group company. For purposes of this Notice, the name “ROHM” would also imply Kionix, Inc.

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Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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5. Please verify and confirm characteristics of the final or mounted products in using the Products.

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7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

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