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DATASHEET

High Efficiency Buck-Boost Regulator with 4.1A Switches

ISL91107IR

The ISL91107IR is a highly-integrated buck-boost switching regulator that accepts input voltages either above or below the regulated output voltage. Unlike other buck-boost regulators, this regulator automatically transitions between operating modes without significant output disturbance.

This device is capable of delivering up to 2A of output current (PVIN = 2.8V, V_{OUT} = 3.3V) and provides excellent efficiency due to its fully synchronous 4-switch architecture. No-load quiescent current of only 45µA also optimizes efficiency under light load conditions.

The ISL91107IR is designed for standalone applications and supports 3.3V fixed output voltages or variable output voltages with an external resistor divider. Output voltages as low as 1V or as high as 5.2V are supported using an external resistor divider.

The ISL91107IR requires only a single inductor and very few external components. Power supply solution size is minimized by its 2.5MHz switching frequency, allowing small size external components.

The ISL91107IR is available in a 3x4 20 Ld TQFN package.

Features

- Accepts input voltages above or below regulated output voltage
- Automatic and seamless transitions between buck and boost modes
- Input voltage range: 1.8V to 5.5V
- Output current: up to 2A (PVIN = 2.8V, V_{OUT} = 3.3V)
- High efficiency: up to 96%
- 45µA quiescent current maximizes light load efficiency
- 2.5MHz switching frequency minimizes external component size
- Selectable forced PWM mode
- Fully protected for short-circuit, over-temperature and undervoltage
- Small 3mmx4mm TQFN package

Applications

- Smartphones and tablet PCs
- Wireless communication devices
- Optical modules networking equipment

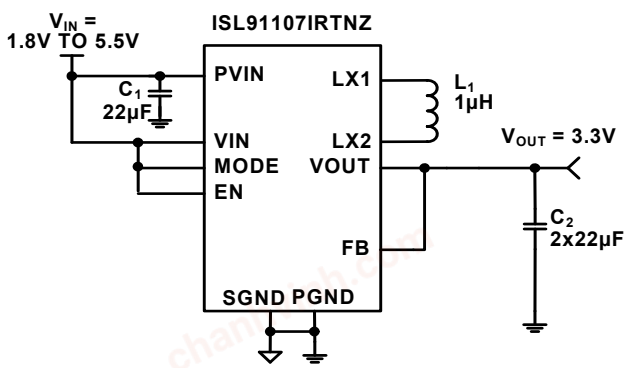


FIGURE 1. TYPICAL ISL91107IRTNZ APPLICATION

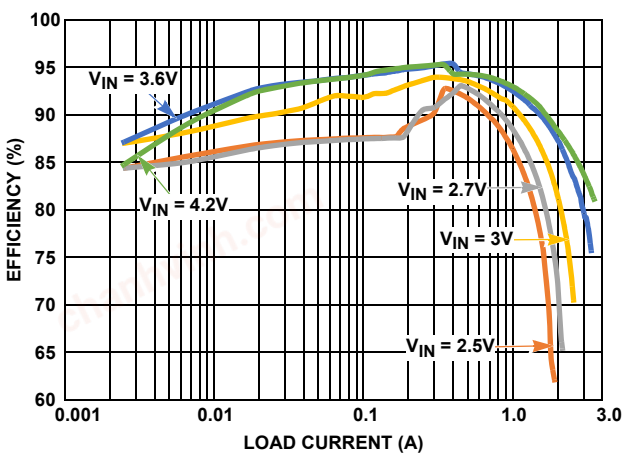
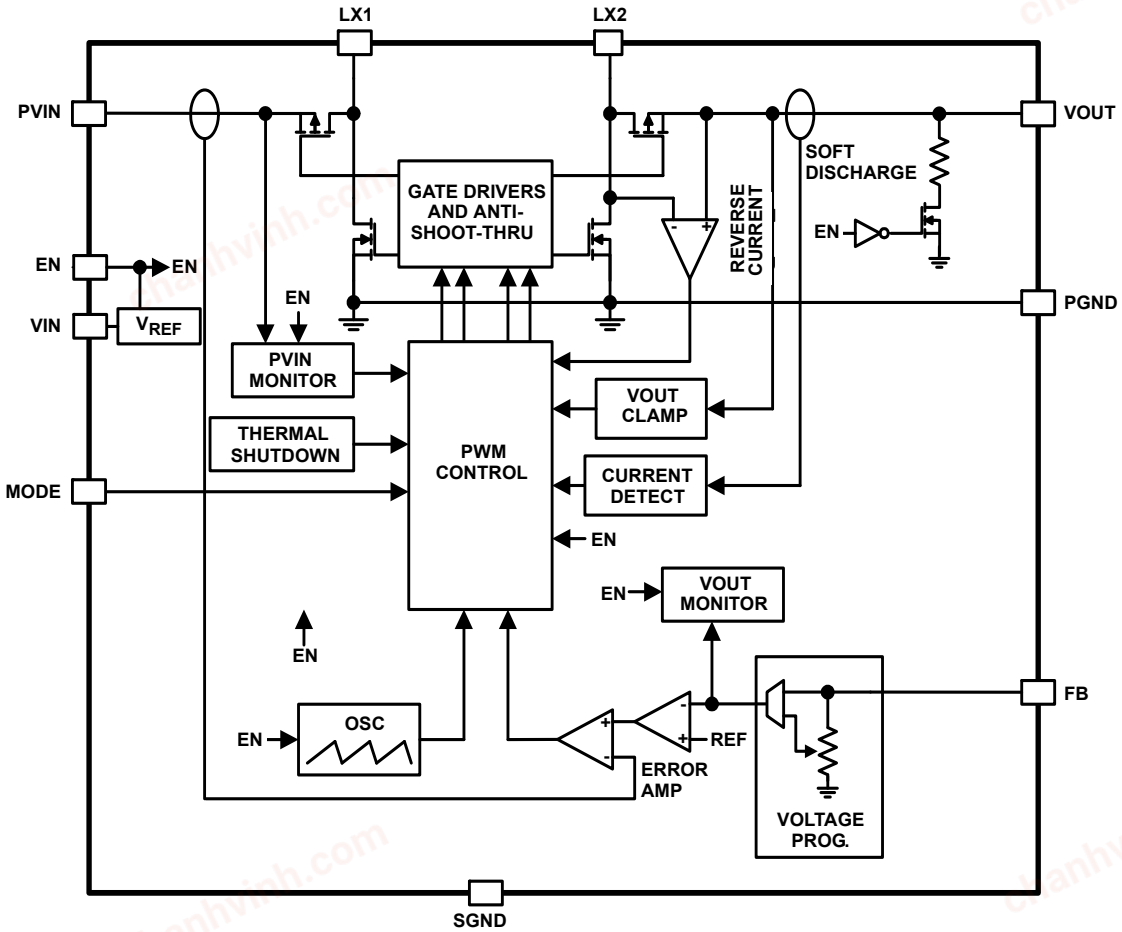


FIGURE 2. EFFICIENCY vs OUTPUT CURRENT (V_{OUT} = 3.3V)

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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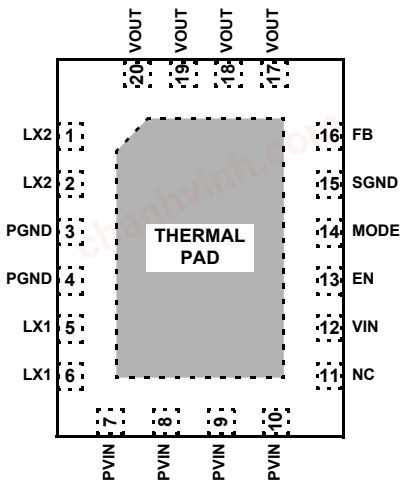
Block Diagram



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Pin Configuration

ISL91107IR
(20 LD TQFN)
TOP VIEW



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
7, 8, 9, 10	PVIN	Power input. Range: 1.8V to 5.5V. Connect 22µF capacitor to PGND.
12	VIN	Supply input. Range: 1.8V to 5.5V.
5, 6	LX1	Inductor connection, input side.
13	EN	Logic input for enable. Drive HIGH to enable device, LOW to disable. Do not leave this pin floating
3, 4	PGND	Power ground for high switching current.
14	MODE	Logic input, HIGH for auto PFM mode. LOW for forced PWM operation. Do not leave this pin floating
1, 2	LX2	Inductor connection, output side.
15	SGND	Analog ground pin
17, 18, 19, 20	VOUT	Buck-boost output. Connect 2x22µF capacitor to PGND.
16	FB	Voltage feedback pin.
-	EPAD	Thermal pad. Connect to PGND

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	VOUT (V)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL91107IRTNZ (Note 1)	107N	3.3	-40 to +85	20 Ld TQFN	L20.3x4A
ISL91107IRTAZ (Note 1)	107A	Adj	-40 to +85	20 Ld TQFN	L20.3x4A
ISL91107IRN-EVZ	Evaluation Board for ISL91107IRTNZ for 3.3 Voltage Output				
ISL91107IRA-EVZ	Evaluation Board for ISL91107IRTAZ for ADJ Voltage Output				

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL91107IR. For more information on MSL, please see tech brief TB363.

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Absolute Maximum Ratings

PVIN, VIN . . . . . -0.3V to 6.5V
LX1, LX2 . . . . . -0.3V to 6.5V
FB . . . . . -0.3V to 6.5V
SGND, PGND . . . . . -0.3V to 0.3V
All Other Pins . . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 3kV
Machine Model (Tested per JESD22-A115-A) 250V
Latch-up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
3x4mm TQFN Package (Notes 4, 5)	41	5.5

Maximum Junction Temperature . . . . . +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Supply Voltage (V_{IN}) Range . . . . . 1.8V to 5.5V
Load Current (I_{OUT}) Range (DC) . . . . . 0A to 2A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Analog Specifications

V_{IN} = PVIN = EN = 3.6V, V_{OUT} = 3.3V, L_1 = 1µH, C_1 = 1x22µF, C_2 = 2x22µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V).**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
POWER SUPPLY						
VIN	Input Voltage Range		**1.8**		**5.5**	V
V_{UVLO}	V_{IN} Undervoltage Lockout Threshold	Rising		1.75	**1.795**	V
		Falling	**1.60**	1.71		V
I_{VIN}	V_{IN} Supply Current	PFM mode, no external load on V_{OUT}, no switching, $V_{IN} \le 5V$		45	**60**	µA
		PFM mode, no external load on V_{OUT}, with switching		60		
I_{SD}	V_{IN} Supply Current, Shutdown	EN = SGND, $V_{IN} \le 5V$		0.05	**0.6**	µA
OUTPUT VOLTAGE REGULATION						
VOUT	Output Voltage Accuracy	I_{OUT} = 1mA, PWM mode	**-2**		**+2**	%
		I_{OUT} = 1mA, PFM mode	**-3**		**+4**	%
VFB	Feedback Voltage	For adjustable version only	**0.788**	0.8	**0.812**	V
ΔVOUT/ ΔVIN	Line Regulation, PWM Mode	I_{OUT} = 500mA, MODE = SGND, V_{IN} step from 2.3V to 5.5V		±0.005		mV/mV
ΔVOUT/ ΔIOUT	Load Regulation, PWM Mode	V_{IN} = 3.7V, MODE = SGND, I_{OUT} step from 0mA to 500mA		±0.005		mV/mA
ΔVOUT/ ΔVIN	Line Regulation, PFM Mode	I_{OUT} = 100mA, MODE = V_{IN}, V_{IN} step from 2.3V to 5.5V		±12.5		mV/V
ΔVOUT/ ΔIOUT	Load Regulation, PFM Mode	V_{IN} = 3.7V, MODE = V_{IN}, I_{OUT} step from 0mA to 100mA		±0.4		mV/mA
V_{CLAMP}	Output Voltage Clamp	Rising	**5.35**		**5.85**	V
V_{CLAMP_HS}	Output Voltage Clamp Hysteresis			400		mV
DC/DC SWITCHING SPECIFICATIONS						
f_{SW}	Oscillator Frequency	$2.5 \le V_{IN} \le 5V$	**2.25**	2.5	**2.75**	MHz
t_{ONMIN}	Minimum On Time			80		ns
$I_{PFETLEAK}$	LX1 Pin Leakage Current		**-0.1**		**0.1**	µA
$I_{NFETLEAK}$	LX2 Pin Leakage Current		**-0.1**		**0.1**	µA

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Analog Specifications

V_{IN} = PVIN = EN = 3.6V, V_{OUT} = 3.3V, L_1 = 1µH, C_1 = 1x22µF, C_2 = 2x22µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V). (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
SOFT-START and SOFT DISCHARGE						
t_{SS}	Soft-start Time	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in buck mode. V_{IN} = 4V, I_{OUT} = 200mA		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in boost mode. V_{IN} = 2V, I_{OUT} = 200mA		2		ms
R_{DISCHG}	V_{OUT} Soft-discharge ON-resistance	V_{IN} = 3.6V, EN < V_{IL}		35		Ω
POWER MOSFET						
r_{DSON_P}	P-channel MOSFET ON-resistance	V_{IN} = 3.6V		55		mΩ
R_{DSON_N}	N-channel MOSFET ON-resistance	V_{IN} = 3.6V		47		mΩ
I_{PK_LMT}	P-channel MOSFET Peak Current Limit	V_{IN} = 3.6V	**3.8**	4.1	**4.8**	A
PFM/PWM TRANSITION						
	Load Current Threshold, PFM to PWM	V_{IN} = 3V, V_{OUT} = 3.3V		375		mA
	Load Current Threshold, PWM to PFM	V_{IN} = 3V, V_{OUT} = 3.3V		300		mA
THERMAL SHUTDOWN						
	Thermal Shutdown			150		°C
	Thermal Shutdown Hysteresis			30		°C
LOGIC INPUTS						
I_{LEAK}	Input Leakage			0.05	**0.1**	µA
V_{IH}	Input HIGH Voltage		**1.4**			V
V_{IL}	Input LOW Voltage				**0.4**	V

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

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Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 22µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 2A.

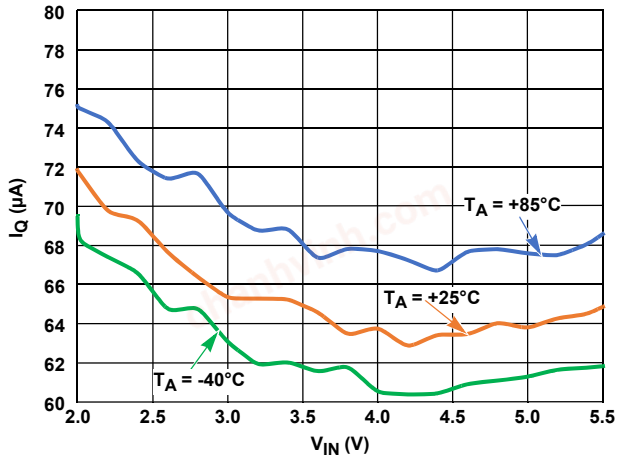


FIGURE 3. QUIESCENT CURRENT vs INPUT VOLTAGE (MODE = HIGH, V_{OUT} = 3.3V)

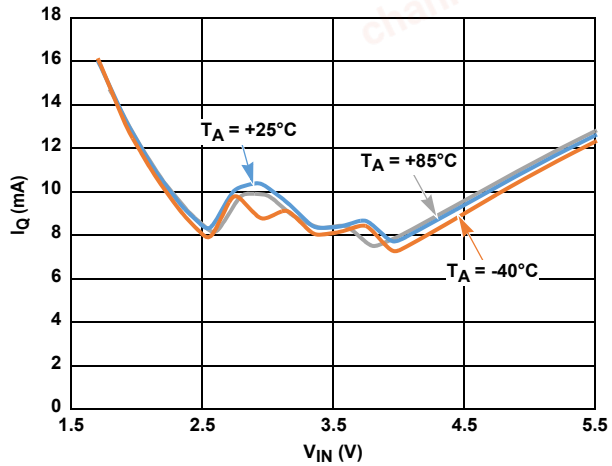


FIGURE 4. QUIESCENT CURRENT vs INPUT VOLTAGE (MODE = LOW, V_{OUT} = 3.3V)

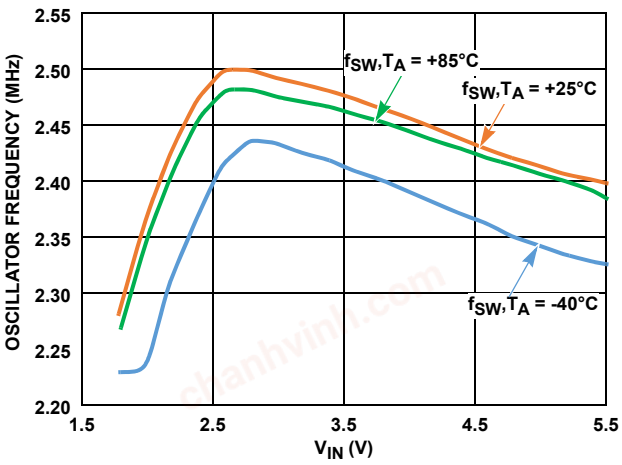


FIGURE 5. SWITCHING FREQUENCY vs INPUT VOLTAGE

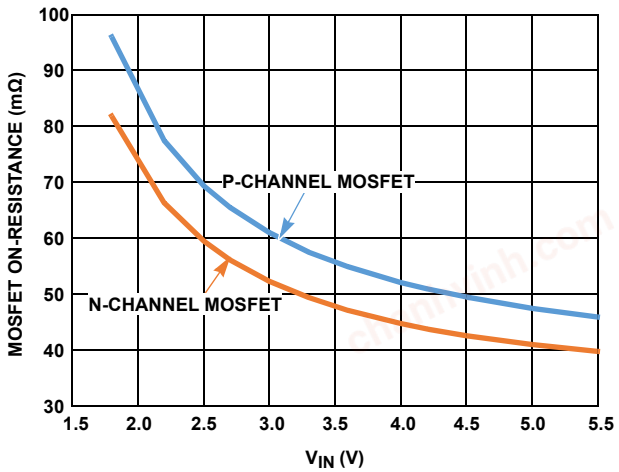


FIGURE 6. MOSFET ON-RESISTANCE vs INPUT VOLTAGE

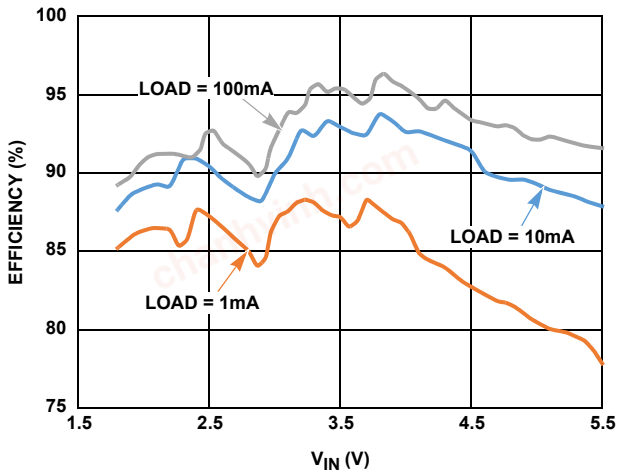


FIGURE 7. LIGHT-LOAD EFFICIENCY vs INPUT VOLTAGE (V_{OUT} = 3.3V)

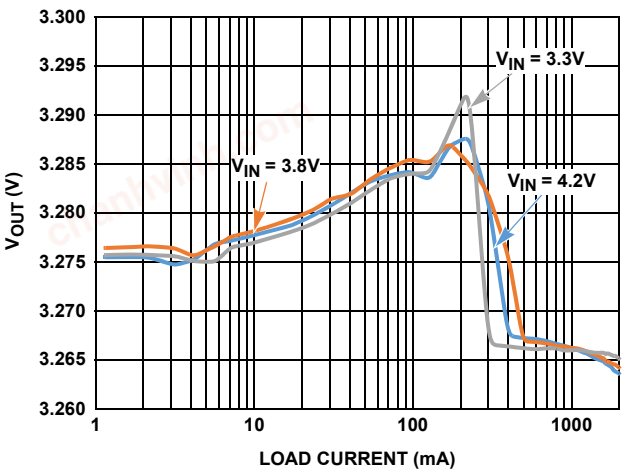


FIGURE 8. OUTPUT VOLTAGE vs LOAD CURRENT

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Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 22µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 2A. **(Continued)**

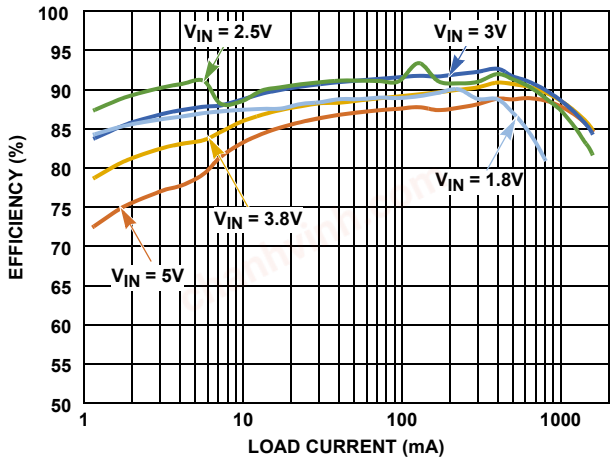


FIGURE 9. EFFICIENCY vs LOAD CURRENT (V_{OUT} = 2V)

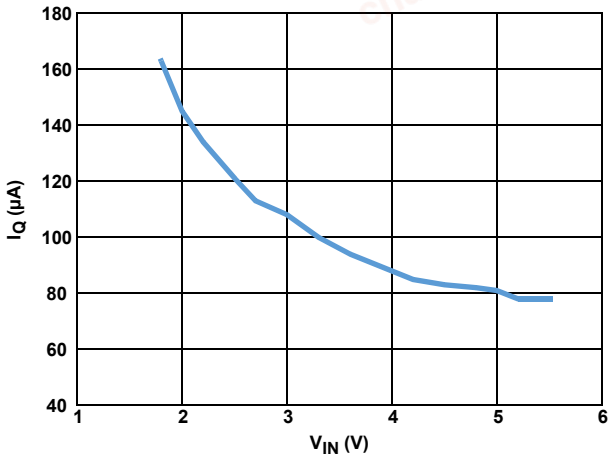


FIGURE 10. SUPPLY CURRENT (SWITCHING) (V_{OUT} = 5V)

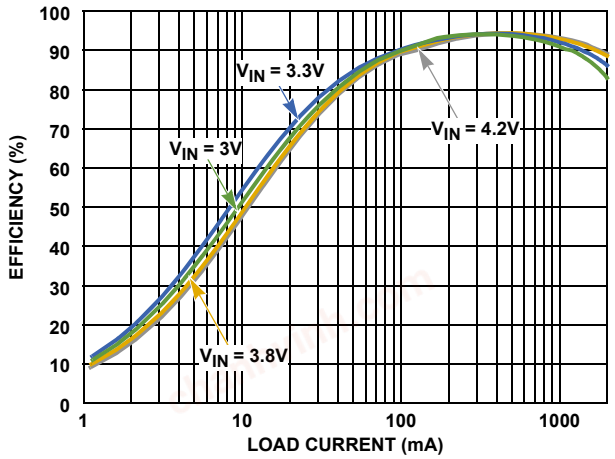


FIGURE 11. EFFICIENCY vs LOAD CURRENT (MODE = LOW, V_{OUT} = 3.3V)

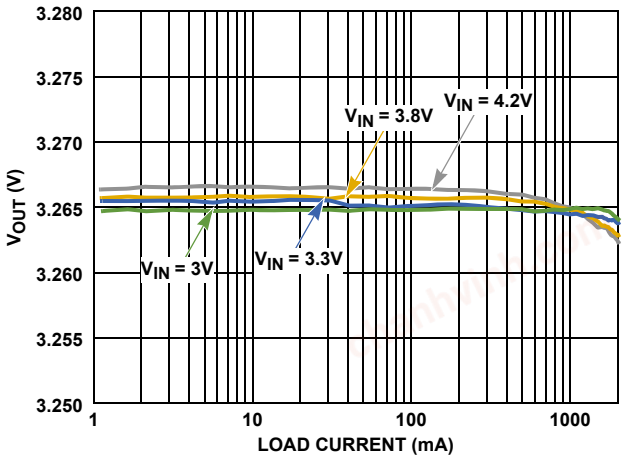


FIGURE 12. OUTPUT VOLTAGE vs LOAD CURRENT (MODE = LOW, V_{OUT} = 3.265V)

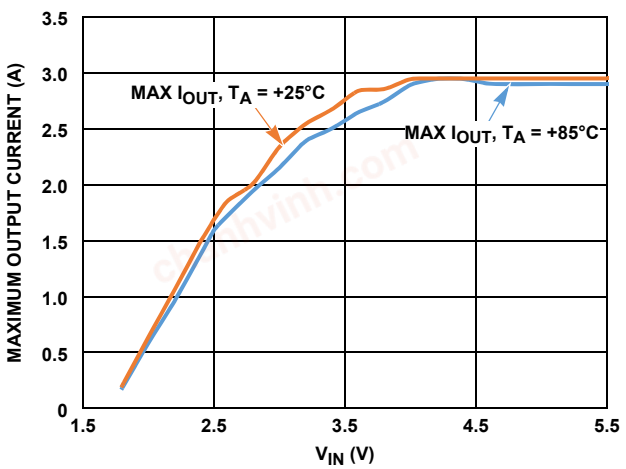


FIGURE 13. MAXIMUM OUTPUT CURRENT vs INPUT VOLTAGE (V_{OUT} = 3.3V)

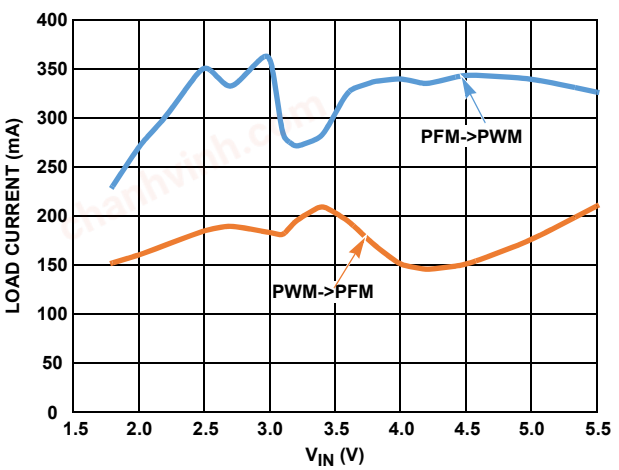


FIGURE 14. PFM<->PWM TRANSITION THRESHOLDS vs V_{IN} (V_{OUT} = 3.3V)

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Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 22µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 2A. **(Continued)**

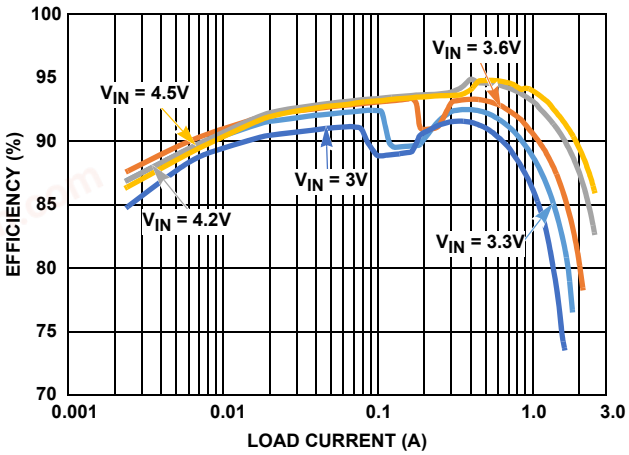


FIGURE 15. EFFICIENCY vs OUTPUT CURRENT (V_{OUT} = 5V)

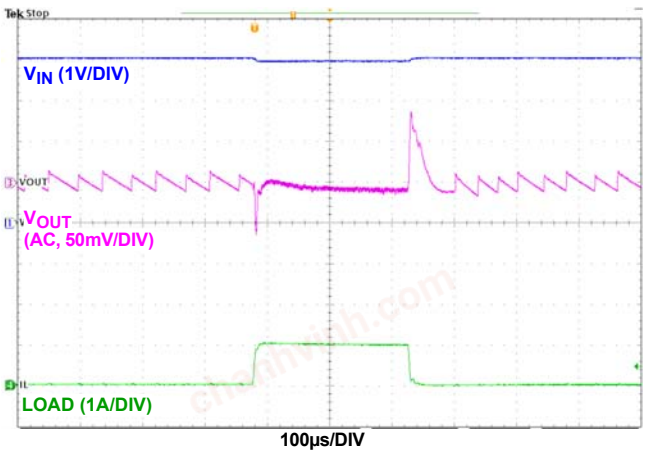


FIGURE 16. 0A TO 1A LOAD TRANSIENT, V_{OUT} = 3.3V

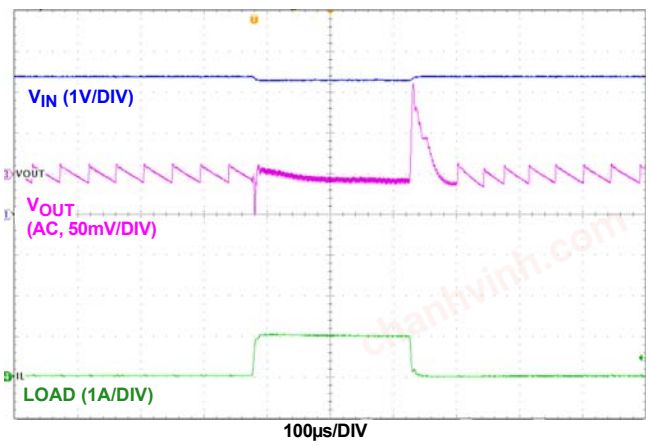


FIGURE 17. 0A TO 1A LOAD TRANSIENT, V_{OUT} = 3.3V

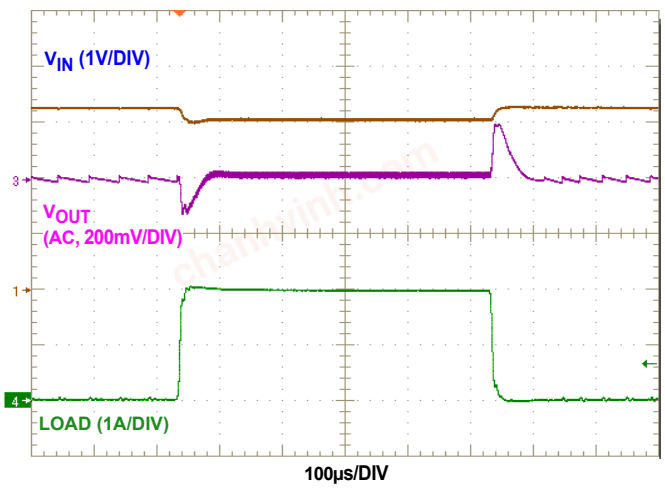


FIGURE 18. 0A TO 1A LOAD TRANSIENT, V_{IN} = 3V, V_{OUT} = 5V

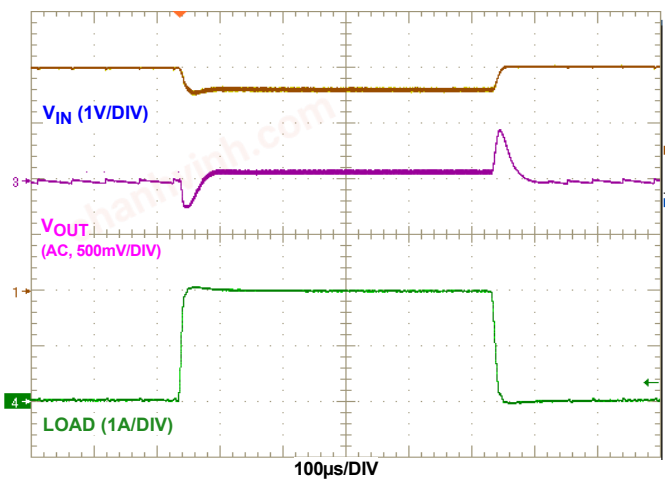


FIGURE 19. 0A TO 2A LOAD TRANSIENT, V_{IN} = 3.6V, V_{OUT} = 5V

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Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 22µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 2A. **(Continued)**

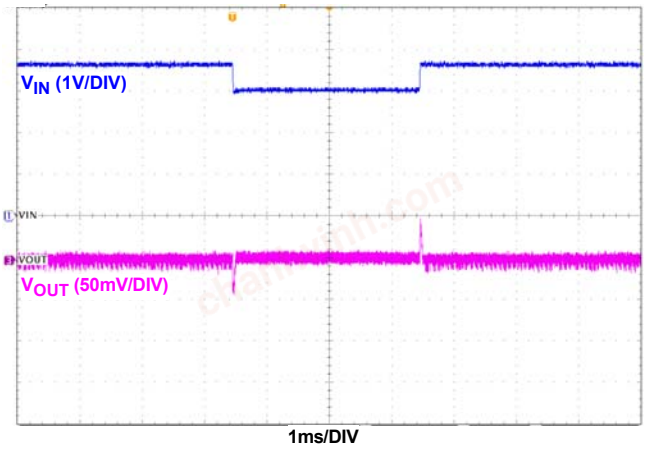


FIGURE 20. 3.6V TO 3V LINE TRANSIENT RESPONSE, V_{OUT} = 3.3V, LOAD = 1.5A

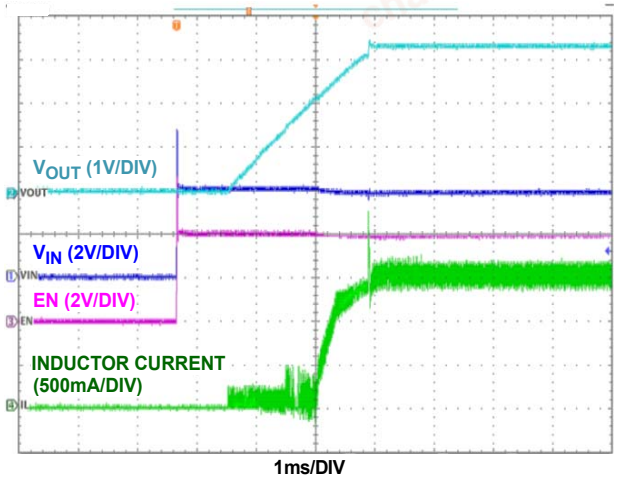


FIGURE 21. START-UP WITH V_{IN} = 4V, R_{LOAD} = 1.5A, V_{OUT} = 3.3V

Functional Description

Functional Overview

Refer to the "Block Diagram" on page 2. The ISL91107IR implements a complete buck-boost switching regulator with PWM controller, internal switches, references, protection circuitry and control inputs.

The PWM controller automatically switches between buck and boost modes as necessary to maintain a steady output voltage with changing input voltages and dynamic external loads.

Internal Supply and References

Referring to the "Block Diagram" on page 2, the ISL91107IR provides two power input pins. The PVIN pin supplies input power to the DC/DC converter, while the VIN pin provides operating voltage source required for stable V_{REF} generation. Separate ground pins (SGND and PGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

A master enable pin EN allows the device to be enabled. Driving EN LOW invokes a power-down mode, where most internal device functions are disabled.

Soft Discharge

When the device is disabled by driving EN LOW, an internal resistor between VOUT and SGND is activated. This internal resistor has a typical resistance of 35Ω.

POR Sequence and Soft-start

Bringing the EN pin HIGH allows the device to power-up. A number of events occur during the start-up sequence. The internal voltage reference powers up and stabilizes. The device then starts to operate. There is a 1ms (typical) delay between assertion of the EN pin and the start of the switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input inrush currents. During soft-start, the reference voltage is ramped to provide a ramping V_{OUT} voltage. While output voltage is lower than approximately 20% of the target output voltage, switching frequency is reduced to a fraction of the normal switching frequency to aid in producing low duty cycles necessary to avoid input inrush current spikes. Once the output voltage exceeds 20% of the target voltage, the switching frequency is increased to its nominal value.

When the target output voltage is higher than the input voltage, there will be a transition from buck mode to boost mode during the soft-start sequence. At the time of this transition, the ramp rate of the reference voltage is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

The V_{OUT} ramp time is not constant for all operating conditions. Soft-start into boost mode will take longer than soft-start into buck mode. The total soft-start time into buck operating mode is typically 2ms, whereas the typical soft-start time into boost mode operating mode is typically 3ms. Increasing the load current will increase these typical soft-start times.

Overcurrent Protection

The ISL91107IR provides short-circuit protection by monitoring the FB voltage. When FB voltage is sensed to be lower than a certain threshold, the PWM oscillator frequency is reduced in order to protect the device from damage. The P-channel MOSFET peak current limit remains active during this state.

Undervoltage Lockout

The undervoltage lockout (UVLO) feature prevents abnormal operation in the event that the supply voltage is too low to guarantee proper operation. When the V_{IN} voltage falls below the UVLO threshold, the regulator is disabled.

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Thermal Shutdown

A built-in thermal protection feature protects the ISL91107IR if the die temperature reaches +150°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal-shutdown mode. When the die temperature falls to +120°C (typical), the device will resume normal operation.

When exiting thermal shutdown, the ISL91107IR will execute its soft-start sequence.

Buck-Boost Conversion Topology

The ISL91107IR operates in either buck or boost mode. When operating in conditions where V_{IN} is close to V_{OUT}, the ISL91107IR alternates between buck and boost mode as necessary to provide a regulated output voltage.

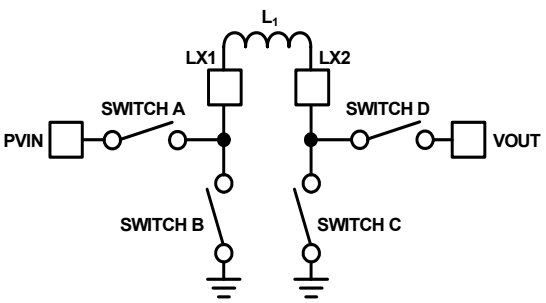


FIGURE 22. BUCK-BOOST TOPOLOGY

Figure 22 shows a simplified diagram of the internal switches and external inductor.

PWM Operation

In buck PWM mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate as a synchronous buck converter when in this mode.

In boost PWM mode, Switch A remains closed and Switch B remains open. Switches C and D operate as a synchronous boost converter when in this mode.

PFM Operation

During PFM operation in buck mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation. During PFM operation in boost mode, the ISL91107IR closes Switch A and Switch C to ramp up the current in the inductor. When the inductor current reaches a certain threshold, the device turns OFF Switches A and C, then turns ON Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

In most operating conditions, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller.

Operation with V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the ISL91107IR will rapidly and smoothly switch from boost-to-buck mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

Applications Information

Component Selection

The fixed output versions of the ISL91107IR require only three external power components to implement the buck boost converter: an inductor, an input capacitor and an output capacitor.

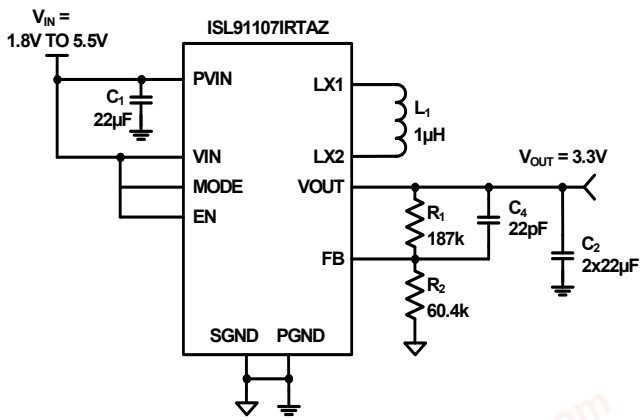


FIGURE 23. TYPICAL APPLICATION

The adjustable ISL91107IR version requires three additional components to program the output voltage. Two external resistors program the output voltage and a small capacitor is added to improve stability and response.

Setting and controlling the output voltage of the ISL91107IR (adjustable output version) can be accomplished by selecting the external resistor values.

Equation 1 can be used to derive the R_1 and R_2 resistor values:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 1)}$$

When designing a PCB, include an SGND guard band around the feedback resistor network to reduce noise and improve accuracy and stability. Resistors R_1 and R_2 should be positioned close to the FB pin.

Inductor Selection

An inductor with high frequency core material (e.g., ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 1µH inductor with ≥4.1A saturation current rating is recommended. Select an inductor with low DCR to provide good

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efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

TABLE 1. INDUCTOR VENDOR INFORMATION

MANUFACTURER	MFR P/N	DESCRIPTION
Cyntec	PIFE32251B-1R0MS	1µH, 3.2x2.5x1.2mm
TOKO	DFE322512C	1µH, 3.2x2.5x1.2mm

PVIN and V_{OUT} Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 22µF, as this would provide adequate RMS current to minimize the input voltage ripple. A minimum of 10µF is required to maintain full functionality of the part.

The recommended output capacitor is 2x22µF, 10V, X5R. Note that the effective value of a ceramic capacitor derates with DC voltage bias across it. This derating may be up to 70% of the rated capacitance.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	PN	DESCRIPTION
Murata	GRM188R61A226ME15D	22µF, 0603, 10V, X5R
TDK	C1608X5R1A226M080AC	22µF, 0603, 10V, X5R

Refer to the capacitor datasheet to ensure the combined effective output capacitance is at least 14µF for proper operation over the entire recommended load current range. Low output capacitance may lead to large output voltage drop during load transient or unstable operation.

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL91107IR. The following are some general guidelines for the recommended layout:

1. The input and output capacitors should be positioned as close to the IC as possible.
2. The ground connections of the input and output capacitors should be kept as short as possible. The objective is to minimize the current loop between the ground pads of the input and output capacitors and the PGND pins of the IC. Use vias, if required, to take advantage of a PCB ground layer underneath the regulator.
3. The analog ground pin (SGND) should be connected to a large/low-noise ground plane on the top or an intermediate layer on the PCB, away from the switching current path of PGND. This ensures a low noise signal ground reference.
4. Minimize the trace lengths on the feedback loop to avoid switching noise pick-up. Vias should be avoided on the feedback loop to minimize the effect of board parasitic, particularly during load transients.
5. The LX1 and LX2 traces should be short and must be routed on the same layer as the IC.

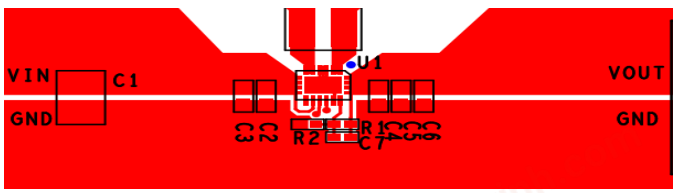


FIGURE 24. RECOMMENDED LAYOUT

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 2, 2015	FN8687.0	Initial Release.

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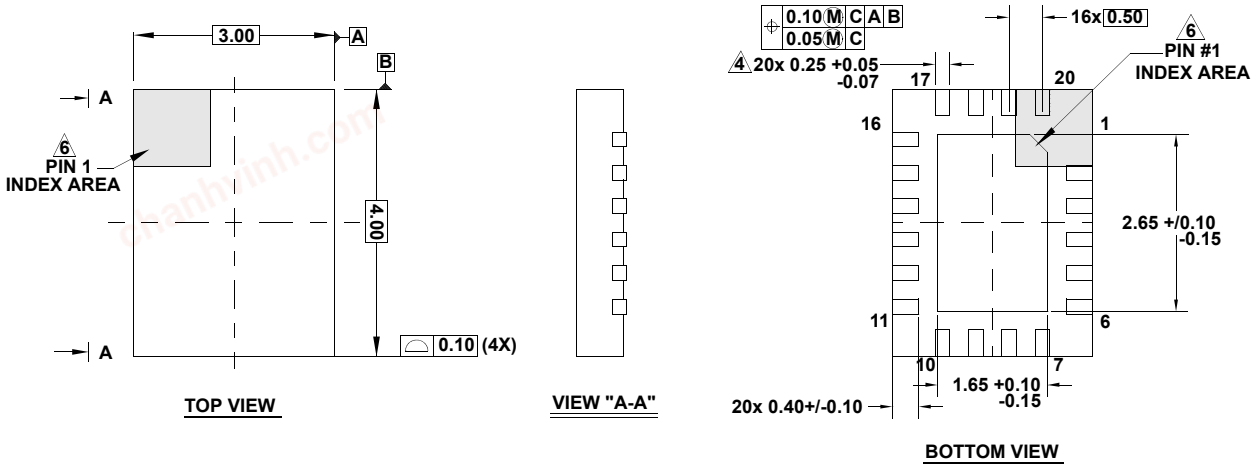
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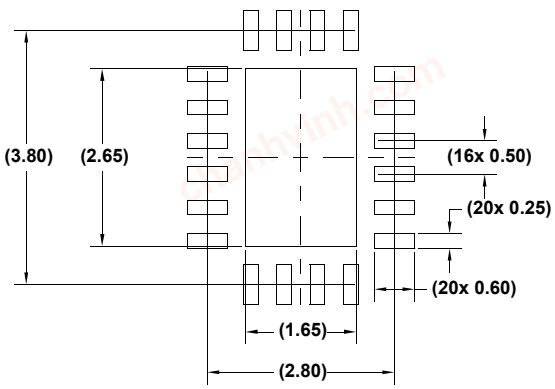
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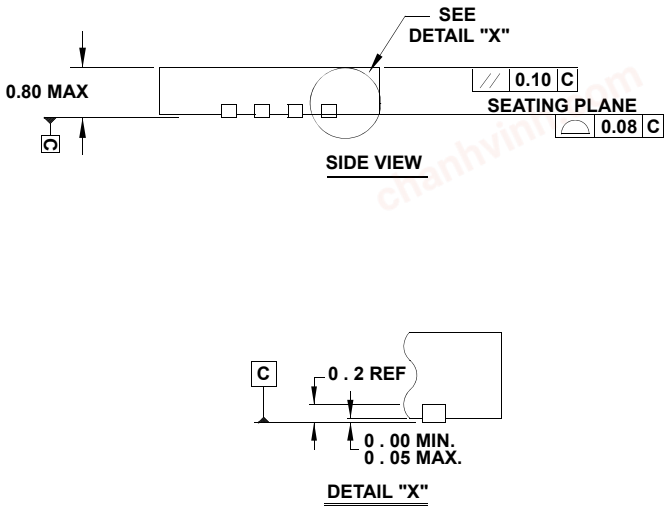
Package Outline Drawing

L20.3x4A

20 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 6/10







NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220VEGD-NJI.