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DATASHEET

5V, Rail-to-Rail I/O, Zero-Drift, Programmable Gain Instrumentation Amplifiers

ISL28533, ISL28534, ISL28535, ISL28633, ISL28634, ISL28635

The ISL28533, ISL28534, ISL28535, ISL28633, ISL28634 and ISL28635 are 5V zero-drift rail-to-rail input/output Programmable Gain Instrumentation Amplifiers (PGIA). These instrumentation amplifiers feature low offset, low noise, low gain error and high CMRR. They are ideal for high precision applications over the wide industrial temperature range.

These instrumentation amplifiers are designed with a unique 2-bit, 3-state logic interface that allows up to 9 selectable gain settings. The ISL2853x single-ended output includes an additional uncommitted zero-drift amplifier, useful to buffer the REF input or used as a precision amplifier. The ISL2863x differential output amplifier includes a reference pin to set the common-mode output voltage to interface with differential input ADCs.

Applications

- Pressure and strain gauge transducers
- Weight scales
- Flow sensors
- Biometric: ECG/blood glucose
- Temperature sensors
- Test and measurement
- Data acquisition systems
- Low ohmic current sense

Features

- Ultra high precision front-end amplifier
- Zero-drift instrumentation amplifier
- Pin selectable 9 gain settings: G = 1 to 1,000
- Rail-to-rail input/output
- Single-ended output (ISL28533, ISL28534, ISL28535)
- Differential output (ISL28633, ISL28634, ISL28635)
- RFI filtered inputs improve EMI rejection
- Single supply . . . . . 2.5V to 5.5V
- Dual supply . . . . . ±1.25V to ±2.75V
- Low input offset . . . . . 5µV, Maximum
- Low input offset drift . . . . . 50nV/°C, Maximum
- High CMRR . . . . . 138dB, G = 100
- Low gain error. . . . . <0.4%, All Gains, Maximum
- Gain bandwidth 2.3MHz
- Input voltage noise (0.1Hz to 10Hz). . . . . 0.4µV_{P-P}
- Operating temperature range. . . . . -40°C to +125°C

Related Literature

- AN1880 “ISL2853x_63xEV2Z User's Guide”

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	OUTPUT	ADDITIONAL UNCOMMITTED OP AMP
ISL28533/34/35	Single-ended	Yes
ISL28633/34/35	Differential	No

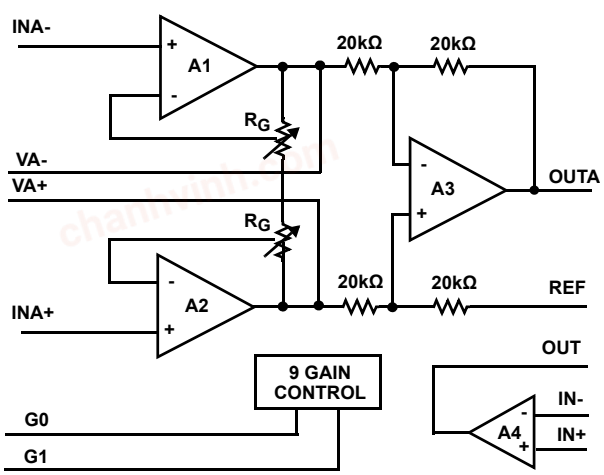


FIGURE 1. ISL2853x SINGLE-ENDED OUTPUT

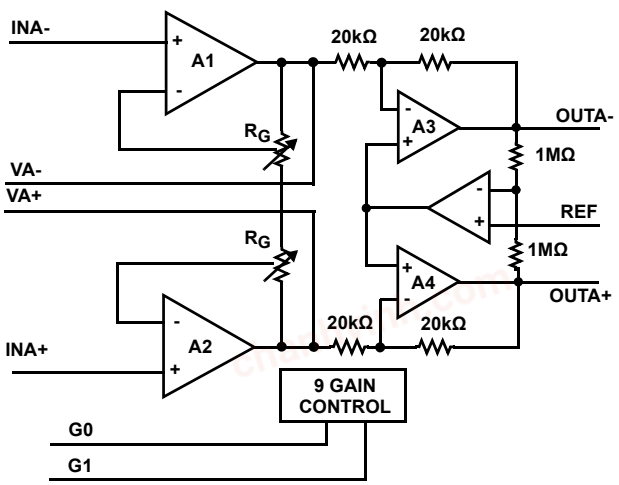


FIGURE 2. ISL2863x DIFFERENTIAL OUTPUT

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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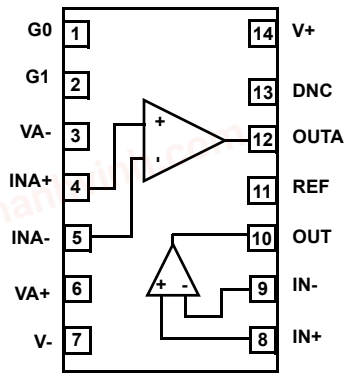
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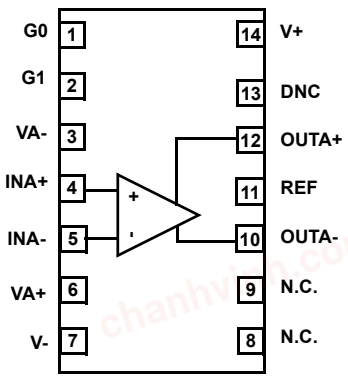
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Pin Configurations

ISL28533, ISL28534, ISL28535 SINGLE-ENDED OUTPUT
(14 LD TSSOP)
TOP VIEW

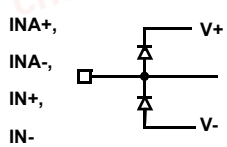


ISL28633, ISL28634, ISL28635 DIFFERENTIAL OUTPUT
(14 LD TSSOP)
TOP VIEW

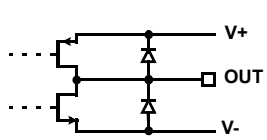


Pin Descriptions

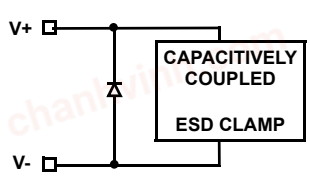
ISL28533 ISL28534 ISL28535 (SINGLE-ENDED OUTPUT)	ISL28633 ISL28634 ISL28635 (DIFFERENTIAL OUTPUT)	PIN NAME	EQUIVALENT CIRCUIT	FUNCTION	COMMENTS
4	4	INA+	Circuit 1	INA+ Input	Positive Differential Input
5	5	INA-	Circuit 1	INA- Input	Negative Differential Input
12	-	OUTA	Circuit 2	INA Output	Single Ended Output
-	12	OUTA+	Circuit 2	INA +Output	Positive Differential Output
-	10	OUTA-	Circuit 2	INA -Output	Negative Differential Output
6	6	VA+	Circuit 1	A2 Output	INA Gain Stage +Output
3	3	VA-	Circuit 1	A1 Output	INA Gain Stage -Output
11	11	REF	Circuit 1	Output Reference	INA Output Reference
1	1	G0	Circuit 1	Gain Control Logic Input	
2	2	G1	Circuit 1	Gain Control Logic Input	
8	-	IN+	Circuit 1	Non-Inverting Op Amp Input	Auxiliary Amplifier IN+
9	-	IN-	Circuit 1	Inverting Op Amp Input	Auxiliary Amplifier IN-
10	-	OUT	Circuit 2	Op Amp Output	Auxiliary Amplifier OUT
14	14	V+	Circuit 3	Positive supply	Single Supply: +2.5V to +5.5V Dual Supply: ±1.25V to ±2.75V
7	7	V-	Circuit 3	Negative supply	
-	8, 9	N.C.		No Connect	
13	13	DNC		Do Not Connect	Pin must float



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

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Typical Sensor Application Block Diagram, ISL28533 Single-Ended Output

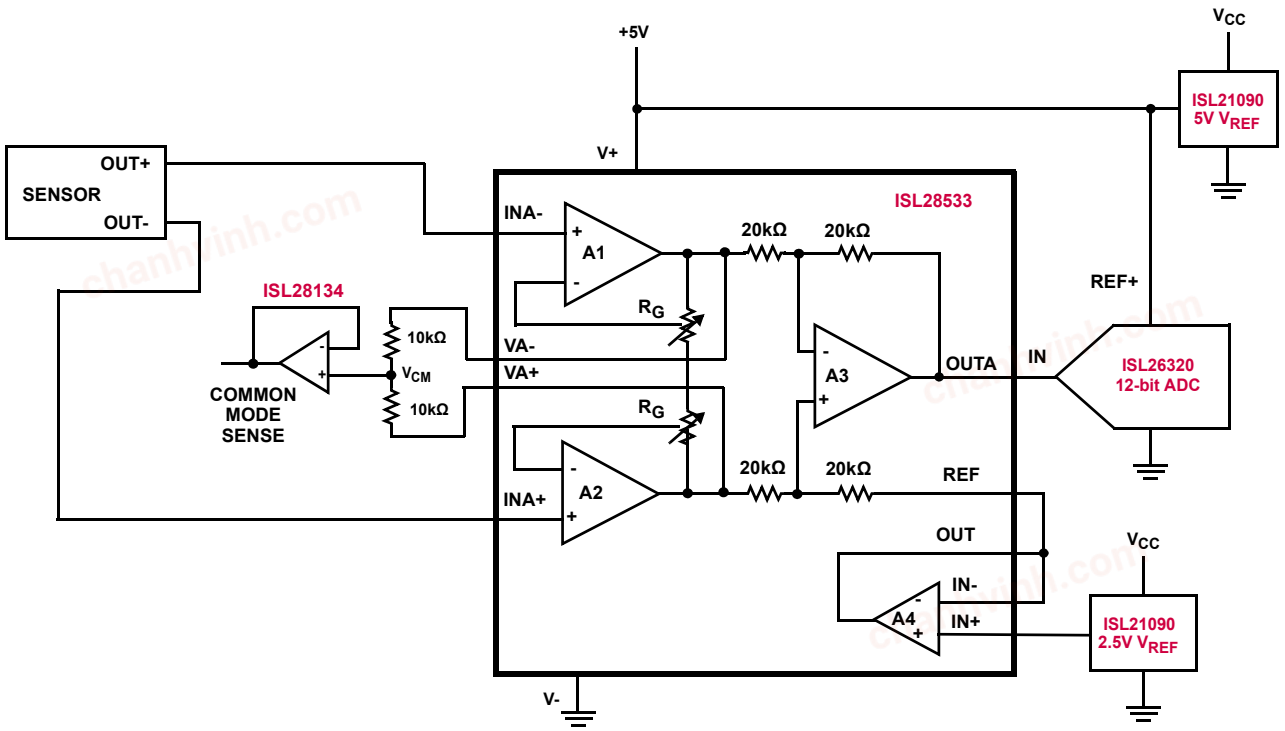


FIGURE 3. SENSOR APPLICATION WITH COMMON-MODE SENSING AND BUFFERED REFERENCE DRIVE

Typical Bridge Sensor Application Block Diagram, ISL28634 Differential Output

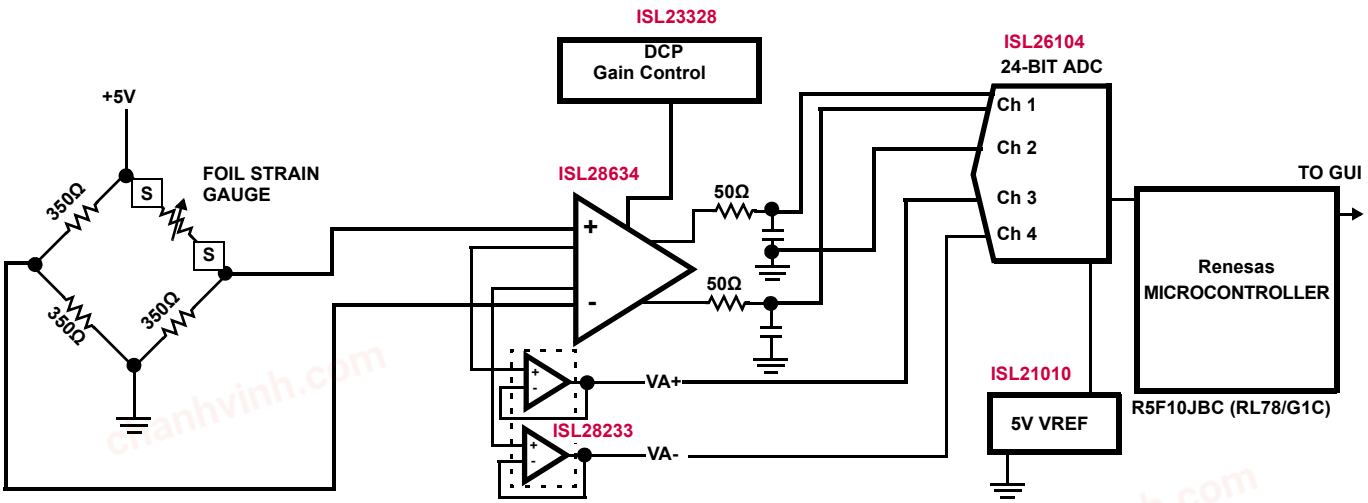


FIGURE 4. SIMPLIFIED STRAIN GAUGE SCHEMATIC

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G0 and G1 Programmable Gain Setting

G1 (NOTE)	G0 (NOTE)	ISL28533 ISL28633	ISL28534 ISL28634	ISL28535 ISL28635
0	0	1	1	1
0	Z	2	2	100
0	1	4	10	120
Z	0	5	50	150
Z	Z	10	100	180
Z	1	20	200	200
1	0	40	300	300
1	Z	50	500	500
1	1	100	1000	1000
APPLICATIONS		Medical Piezo-Electric Pressure Sensor Fluid Sensor	Shunt Sense Optical Sensors Strain Gauge Thermocouple	Strain Gauge

NOTE: For valid logic "Z" state leave G0/G1 pins in high impedance state. Internal 100kΩ pull-up and pull-down resistors on these pins establishes logic "Z". See "Applications Information" on page 25 for more information.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL28533FVZ	28533 FVZ	-40 to +125	14 Ld TSSOP	M14.173
ISL28534FVZ	28534 FVZ	-40 to +125	14 Ld TSSOP	M14.173
ISL28535FVZ	28535 FVZ	-40 to +125	14 Ld TSSOP	M14.173
ISL28633FVZ	28633 FVZ	-40 to +125	14 Ld TSSOP	M14.173
ISL28634FVZ	28634 FVZ	-40 to +125	14 Ld TSSOP	M14.173
ISL28635FVZ	28635 FVZ	-40 to +125	14 Ld TSSOP	M14.173
ISL28533EV2Z	ISL28533 Evaluation Board			
ISL28534EV2Z	ISL28534 Evaluation Board			
ISL28535EV2Z	ISL28535 Evaluation Board			
ISL28633EV2Z	ISL28633 Evaluation Board			
ISL28634EV2Z	ISL28634 Evaluation Board			
ISL28635EV2Z	ISL28635 Evaluation Board			

NOTES:

1. Add "-T13" suffix for 2.5k unit or "-T7A" suffix for 250 unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28533, ISL28534, ISL28535, ISL28633, ISL28634, ISL28635. For more information on MSL please see tech brief TB363.

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Absolute Maximum Ratings

Supply Voltage V+ to V- 6V
Input Voltage V_{IN} to GND . . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
Input Differential Voltage . . . . . V+ to V-
Input Current 5mA
Output Current I_{OUT} (10s) . . . . . ±40mA
Latch-Up
  Class 2 Level 100mA
ESD Rating
  Human Body Model 8kV
  Machine Model 700V
  Charged Device Model 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld TSSOP (Notes 4, 5)	92	30

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +125°C
Maximum Junction Temperature . . . . . +140°C
Supply Voltage . . . . . 2.5V (±1.25V) to 5.5V (±2.75V)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V+ = 5V, V- = 0V, $V_{IN+} = V_{IN-} = V_{REF} = 2.5V$, $T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
POWER SUPPLY DC SPECIFICATIONS						
V_S	Supply Voltage	V_S = (V+) - (V-)	**2.5**	-	**5.5**	V
I_S	Supply Current V_S = 5V	ISL2853x, R_L = OPEN	-	2.9	3.4	mA
			-	-	**3.5**	mA
		ISL2863x, R_L = OPEN	-	3.0	3.5	mA
			-	-	**3.6**	mA
5V DC SPECIFICATIONS INSTRUMENTATION AMPLIFIER						
$V_{OS, I}$	Input Stage Offset Voltage	+25°C	-5.0	±0.6	5.0	µV
		-40°C to +85°C	-9	-	9	µV
		-40°C to +125°C	**-10**	-	**10**	µV
$TCV_{OS, I}$	Input Stage Offset Voltage Temperature Coefficient	-40°C to +125°C	**-50**	±5	**50**	nV/°C
$V_{OS, O}$	Output Stage Offset Voltage	+25°C	-15	±2	15	µV
		-40°C to +85°C	-45	-	45	µV
		-40°C to +125°C	**-65**	-	**65**	µV
$TCV_{OS, O}$	Output Stage Offset Voltage Temperature Coefficient	-40°C to +125°C	**-0.50**	±0.15	**0.50**	µV/°C
I_B	Input Bias Current	+25°C	-400	±50	400	pA
		-40°C to +85°C	-400	-	400	pA
		-40°C to +125°C	**-1**	-	**1**	nA
I_{OS}	Input Offset Current	+25°C	-300	±50	300	pA
		-40°C to +85°C	-350	-	350	pA
		-40°C to +125°C	**-1**	-	**1**	nA
Z_{IN}	Input Impedance	Common-mode	-	10	-	GΩ
			-	5	-	pF

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Electrical Specifications

$V+ = 5V, V- = 0V, V_{IN+} = V_{IN-} = V_{REF} = 2.5V, T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
E_{GAIN}	Gain Error	G = 1 to 50	-0.20	±0.05	0.20	%
			-0.35	-	**0.35**	%
		G = 100 to 500	-0.30	±0.05	0.30	%
			-0.4	-	**0.4**	%
		G = 1000	-0.40	±0.05	0.40	%
			-0.5	-	**0.5**	%
GAIN_TC	Gain Drift	G = 1 to 1,000 -40°C to +125°C	-	10	-	ppm/°C
G_{NL}	Gain Non-Linearity	V_{OUT} = +0.1V to +4.9V; R_L = 10kΩ				
		G = 1	-	5	-	ppm
		G = 10	-	5	-	ppm
		G = 100	-	10	-	ppm
		G = 1000	-	10	-	ppm
CMRR	Common-Mode Rejection Ratio	V_{CM} = +0.1V to +4.9V				
		G = 1	80	100	-	dB
		G = 10	100	114	-	dB
			90	-	-	dB
		G = 100	110	138	-	dB
			100	-	-	dB
		G = 1000	120	150	-	dB
			110	-	-	dB
CMIR	Common-Mode Input Range	Guaranteed by CMRR	**(V-) + 0.1**	-	**(V+) - 0.1**	V
V_{REF} Range	Reference Voltage Range	ISL2853x	**V-**	-	**V+**	V
		ISL2863x	**(V-) + 0.6**	-	**(V+) - 1**	V
I_{REF}	Reference Input Current	ISL2853x $V_{IN+} = V_{IN-} = V_{REF} = 2.5V$	-0.5	0.1	0.5	µA
			-1	-	**1**	µA
		ISL2863x V_{REF} = 2.5V	-500	150	500	pA
			-25	-	**25**	nA
Z_{REF}	Reference Input Impedance	ISL2853x	36	40	44	kΩ
		ISL2863x	-	10	-	GΩ
PSRR	Power Supply Rejection Ratio	Vs = +2.5V to +5.5V				
		G = 1V/V	110	130	-	dB
		G = 10V/V	110	140	-	dB
		G = 100V/V	120	140	-	dB
		G = 1000V/V	120	140	-	dB
I_{SC}	Short-Circuit Output Source Current	R_L = Short to V-	-	45	-	mA
	Short-Circuit Output Sink Current	R_L = Short to V+	-	-45	-	mA
V_{OH}	High Output Voltage from V+ ((V+) - V_{OUT})	R_L = 10kΩ V+ to V_{REF}	-	10	15	mV
			-	-	**20**	mV

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Electrical Specifications

$V+ = 5V, V- = 0V, V_{IN+} = V_{IN-} = V_{REF} = 2.5V, T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OL}	Low Output Voltage from V- ((V-) + V_{OUT})	R_L = 10kΩ V- to V_{REF}	-	10	15	mV
			-	-	**20**	mV
5V GO/G1 LOGIC INPUTS INSTRUMENTATION AMPLIFIER						
V_{IH}	Logic Input High Threshold	Vs = (V+) - (V-)	**0.8 * (Vs)**	-	-	V
V_{IL}	Logic Input Low Threshold	Vs = (V+) - (V-)	-	-	**0.2 * (Vs)**	V
V_{IH_Z}/V_{IL_Z}	Hi-Z Logic Input Range	Vs = (V+) - (V-)	0.4 * (Vs)	-	0.6 * (Vs)	V
V_{OC}	Open Circuit Logic Voltage	Set by 2 internal 100kΩ resistors; V_S = (V+) - (V-)	**0.45 * V_S**	-	**0.55 * V_S**	V
Z_{IN}	Logic Input Impedance		-	50k	-	kΩ
5V AC SPECIFICATIONS INSTRUMENTATION AMPLIFIER						
e_N	Total Input Referred Voltage Noise	$e_N = \sqrt{(e_{Ni}^2 + (e_{No}/G)^2 + (I_N*R_S)^2)}$				
e_{Ni}	Input Noise Voltage	f = 0.1Hz to 10Hz; G = 100	-	0.4	-	μV_{P-P}
		f = 1kHz; G = 100	-	17	-	$nV/\sqrt{Hz}$
e_{No}	Output Noise Voltage	f = 0.1Hz to 10Hz; G = 1	-	1.8	-	μV_{P-P}
		f = 1kHz; G = 1	-	65	-	$nV/\sqrt{Hz}$
I_N	Input Noise Current	f = 10Hz; R_S = 5MΩ; G = 100	-	100	-	$fA/\sqrt{Hz}$
GBWP	Gain Bandwidth Product	G ≥ 10	-	2.3	-	MHz
		G < 10	-	1.6	-	MHz
5V TRANSIENT RESPONSE INSTRUMENTATION AMPLIFIER						
SR	Slew Rate 20% to 80%	V_{OUT} = $4V_{P-P}$; G = 1	-	0.8	-	V/µs
		V_{OUT} = $4V_{P-P}$; G = 100	-	0.28	-	V/µs
t_{GPD}	Gain Select Prop Delay	All gains, 2V to 4V output after gain change	-	1	-	µs
t_s	Settling Time	To 0.1%, $4V_{P-P}$ step	-	20	-	µs
		To 0.01%, $4V_{P-P}$ step	-	70	-	µs
$t_{recover}$	Output Overload Recovery Time, Recovery to 90% of Output Saturation	G = 1	-	1	-	µs
5V DC SPECIFICATIONS OPERATIONAL AMPLIFIER						
Av_{OPEN}	Open Loop Gain		-	140	-	dB
V_{OS}	Input Offset Voltage	T_A = +25°C	-2.5	-0.2	2.5	µV
		T_A = -40°C to +85°C	-3.475	-	3.475	µV
		T_A = -40°C to +125°C	**-4**	-	**-4**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	T_A = -40°C to +125°C	**-15**	-0.5	**15**	nV/°C
I_B	Input Bias Current	T_A = +25°C	-300	±15	300	pA
		T_A = -40°C to +85°C	-300	-	300	pA
		T_A = -40°C to +125°C	**-550**	-	**550**	pA

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Electrical Specifications

$V+ = 5V, V- = 0V, V_{IN+} = V_{IN-} = V_{REF} = 2.5V, T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{OS}	Input Offset Current		-600	±50	600	pA
		T_A = -40°C to +85°C	-600	-	600	pA
		T_A = -40°C to +125°C	**-1100**	-	**1100**	pA
Common-Mode Input Voltage Range		V+ = 5.0V, V- = 0V Guaranteed by CMRR	**0**	-	**5**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	110	135	-	dB
			97	-	-	dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 5.5V	120	135	-	dB
I_{SC}	Short-Circuit Output Source Current	R_L = Short to V-	-	40	-	mA
	Short-Circuit Output Sink Current	R_L = Short to V+	-	-40	-	mA
V_{OH}	Output Voltage Swing, HIGH From V_{OUT} to V_+	R_L = 10kΩ to V_-	-	20	45	mV
		R_L = 10kΩ to V_-	-	-	**50**	mV
V_{OL}	Output Voltage Swing, LOW From V_- to V_{OUT}	R_L = 10kΩ to V_+	-	20	45	mV
		R_L = 10kΩ to V_+	-	-	**50**	mV
5V AC SPECIFICATIONS OPERATIONAL AMPLIFIER						
C_{IN}	Input Capacitance	Differential	-	5.2	-	pF
		Common-mode	-	5.6	-	pF
e_N	Input Noise Voltage	f = 0.1Hz to 10Hz	-	0.25	-	μV_{P-P}
		f = 1kHz	-	10	-	$nV/\sqrt{Hz}$
I_N	Input Noise Current	f = 1kHz	-	200	-	$fA/\sqrt{Hz}$
GBWP	Gain Bandwidth Product		-	3	-	MHz

Operating Specifications

$V+ = 2.5V, V- = 0V, VCM = 1.25V, T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
2.5V DC SPECIFICATIONS INSTRUMENTATION AMPLIFIER						
$V_{OS, I}$	Input Stage Offset Voltage	+25°C	-5.0	±0.6	5.0	µV
		-40°C to +85°C	-9	-	9	µV
		-40°C to +125°C	**-10**	-	**10**	µV
$TCV_{OS, I}$	Input Stage Offset Voltage Temperature Coefficient	-40°C to +125°C	**-50**	±5	**50**	nV/°C
$V_{OS, O}$	Output Stage Offset Voltage	+25°C	-15	±2	15	µV
		-40°C to +85°C	-45	-	45	µV
		-40°C to +125°C	**-65**	-	**65**	µV
$TCV_{OS, O}$	Output Stage Offset Voltage Temperature Coefficient	-40°C to +125°C	**-0.50**	±0.15	**0.50**	µV/°C
I_B	Input Bias Current	+25°C	-400	±50	400	pA
		-40°C to +85°C	-400	-	400	pA
		-40°C to +125°C	**-1**	-	**1**	nA

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Operating Specifications

$V+ = 2.5V$, $V- = 0V$, $VCM = 1.25V$, $T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{OS}	Input Offset Current	+25°C	-300	±50	300	pA
		-40°C to +85°C	-350	-	350	pA
		-40°C to +125°C	**-1**	-	**1**	nA
Z_{IN}	Input Impedance	Common-mode	-	10	-	GΩ
			-	5	-	pF
E_{GAIN}	Gain Error	G = 1 to 50	-0.20	±0.05	0.20	%
			-0.35	-	**0.35**	%
		G = 100 to 500	-0.30	±0.05	0.30	%
			-0.4	-	**0.4**	%
		G = 1000	-0.40	±0.05	0.40	%
			-0.5	-	**0.5**	%
GAIN_TC	Gain Drift	G = 1 to 1,000 -40°C to +125°C	-	10	-	ppm/°C
CMRR	Common-Mode Rejection Ratio	V_{CM} = +0.1V to +2.4V				
		G = 1	80	100	-	dB
		G = 10	100	114	-	dB
			90	-	-	dB
		G = 100	110	138	-	dB
			100	-	-	dB
		G = 1000	120	150	-	dB
			110	-	-	dB
CMIR	Common-Mode Input Range	Guaranteed by CMRR	**(V-) + 0.1**	-	**(V+) - 0.1**	V
V_{REF} Range	Reference Voltage Range	ISL2853x	**V-**	-	**V+**	V
		ISL2863x	**(V-) + 0.6**	-	**(V+) - 1**	V
I_{REF}	Reference Input Current	ISL2853x $V_{IN+} = V_{IN-} = V_{REF} = 1.25V$	-0.5	0.1	0.5	µA
			-1	-	**1**	µA
		ISL2863x	-500	150	500	pA
			-25	-	**25**	nA
Z_{REF}	Reference Input Impedance	ISL2853x	36	40	44	kΩ
		ISL2863x	-	10	-	GΩ
PSRR	Power Supply Rejection Ratio	Vs = +2.5V to +5.5V				
		G = 1V/V	110	130	-	dB
		G = 10V/V	110	140	-	dB
		G = 100V/V	120	140	-	dB
		G = 1000V/V	120	140	-	dB
I_{SC}	Short-Circuit Output Source Current	R_L = Short to V-	-	25	-	mA
	Short-Circuit Output Sink Current	R_L = Short to V+	-	-25	-	mA
V_{OH}	Output Voltage Swing, HIGH	R_L = 10kΩ to V_{REF}	-	5	15	mV
			-	-	**20**	mV

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Operating Specifications

$V+ = 2.5V$, $V- = 0V$, $VCM = 1.25V$, $T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OL}	Output Voltage Swing, LOW	$R_L = 10k\Omega$ to V_{REF}	-	5	15	mV
			-	-	**20**	mV
2.5V G0/G1 LOGIC INPUTS INSTRUMENTATION AMPLIFIER						
V_{IH}	Logic Input High Threshold	Vs = (V+) - (V-)	**0.8 * (Vs)**	-	-	V
V_{IL}	Logic Input Low Threshold	Vs = (V+) - (V-)	-	-	**0.2 * (Vs)**	V
V_{IH_Z}/V_{IL_Z}	Hi-Z Logic Input Range	Vs = (V+) - (V-)	0.4 * (Vs)	-	0.6 * (Vs)	V
V_{OC}	Open Circuit Logic Voltage	Set by 2 internal 100kΩ Resistors; V_S = (V+) - (V-)	**0.45 * V_S**	-	**0.55 * V_S**	V
Z_{IN}	Logic Input Impedance		-	50k	-	kΩ
2.5V AC SPECIFICATIONS INSTRUMENTATION AMPLIFIER						
e_N	Total Input Referred Voltage Noise	$e_N = \sqrt{(e_{Ni}^2 + (e_{No}/G)^2 + (I_N*R_S)^2)}$				
e_{Ni}	Input Noise Voltage	f = 0.1Hz to 10Hz; G = 100	-	0.4	-	μV_{P-P}
		f = 1kHz; G = 100	-	17	-	$nV/\sqrt{Hz}$
e_{No}	Output Noise Voltage	f = 0.1Hz to 10Hz; G = 1	-	1.8	-	μV_{P-P}
		f = 1kHz; G = 1	-	65	-	$nV/\sqrt{Hz}$
I_N	Input Noise Current	f = 10Hz; R_S = 5MΩ; G = 100	-	100	-	$fA/\sqrt{Hz}$
GBWP	Gain Bandwidth Product	G ≥ 10	-	2.3	-	MHz
		G < 10	-	1.6	-	MHz
2.5V TRANSIENT RESPONSE INSTRUMENTATION AMPLIFIER						
SR	Slew Rate 10% to 90%	$V_{OUT} = 2V_{P-P}$; G = 1	-	0.8	-	V/µs
		$V_{OUT} = 2V_{P-P}$; G = 100	-	0.1	-	V/µs
t_{GPD}	Gain Select Prop Delay	All gains	-	1	-	µs
t_s	Settling Time to 0.1%, $4V_{P-P}$ Step	To 0.1%, $2V_{P-P}$ step	-	20	-	µs
		To 0.01%, $2V_{P-P}$ step	-	70	-	µs
$t_{recover}$	Output Overload Recovery Time, Recovery to 90% of output saturation		-	1.5	-	µs
2.5V DC SPECIFICATIONS OPERATIONAL AMPLIFIER						
Av_{OPEN}	Open Loop Gain		-	140	-	dB
V_{OS}	Input Offset Voltage	$T_A = +25°C$	-2.5	-0.2	2.5	µV
		$T_A = -40°C$ to $+85°C$	-3.475	-	3.475	µV
		$T_A = -40°C$ to $+125°C$	**-4**	-	**-4**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	$T_A = -40°C$ to $+125°C$	**-15**	-0.5	**15**	nV/°C
I_B	Input Bias Current	$T_A = +25°C$	-300	±15	300	pA
		$T_A = -40°C$ to $+85°C$	-300	-	300	pA
		$T_A = -40°C$ to $+125°C$	**-550**	-	**550**	pA

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Operating Specifications

V+ = 2.5V, V- = 0V, VCM = 1.25V, T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{OS}	Input Offset Current	T_A = +25°C	-600	±50	600	pA
		T_A = -40°C to +85°C	-600	-	600	pA
		T_A = -40°C to +125°C	**-1100**	-	**1100**	pA
Common-Mode Input Voltage Range		V+ = 2.5V, V- = 0V Guaranteed by CMRR	**0**	-	**2.5**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 2.5V	110	135	-	dB
			97	-	-	dB
PSRR	Power Supply Rejection Ratio	Vs = 2.5V to 5.5V	120	135	-	dB
I_{SC}	Short-Circuit Output Source Current	R_L = Short to V-	-	25	-	mA
	Short-Circuit Output Sink Current	R_L = Short to V+	-	-25	-	mA
V_{OH}	Output Voltage Swing, HIGH From V_{OUT} to V_+	R_L = 10kΩ to V_{CM}	-	10	20	mV
		R_L = 10kΩ to V_{CM}	-	-	**25**	mV
V_{OL}	Output Voltage Swing, LOW From V_- to V_{OUT}	R_L = 10kΩ to V_{CM}	-	10	20	mV
		R_L = 10kΩ to V_{CM}	-	-	**25**	mV
2.5V AC SPECIFICATIONS OPERATIONAL AMPLIFIER						
C_{IN}	Input Capacitance	Differential	-	5.2	-	pF
		Common-mode	-	5.6	-	pF
e_N	Input Noise Voltage	f = 0.1Hz to 10Hz	-	0.25	-	μV_{P-P}
		f = 1kHz	-	10	-	$nV/\sqrt{Hz}$
I_N	Input Noise Current	f = 1kHz	-	200	-	$fA/\sqrt{Hz}$
GBWP	Gain Bandwidth Product		-	3	-	MHz

NOTE:

6. Compliance to data sheet limits are assured by one or more methods: production test, characterization and/or design.

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Typical Instrumentation Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified.

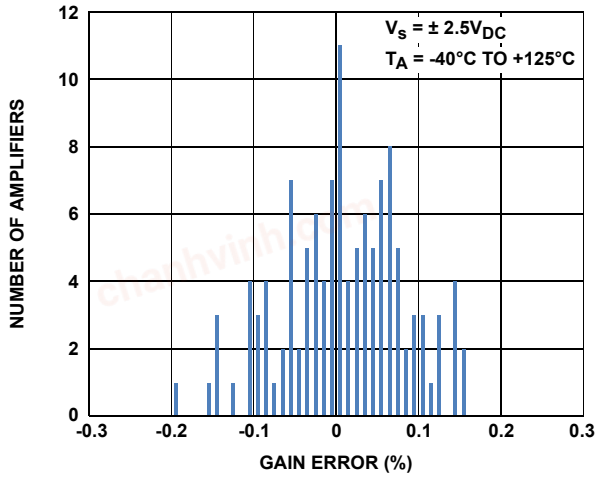


FIGURE 5. PGIA GAIN ERROR DISTRIBUTION, G = 1

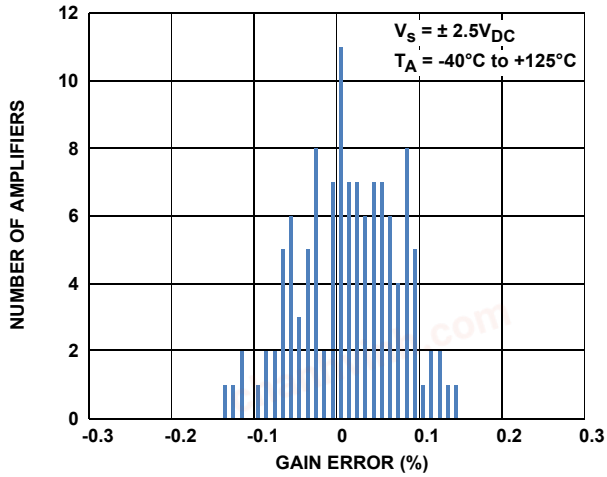


FIGURE 6. PGIA GAIN ERROR DISTRIBUTION, G = 10

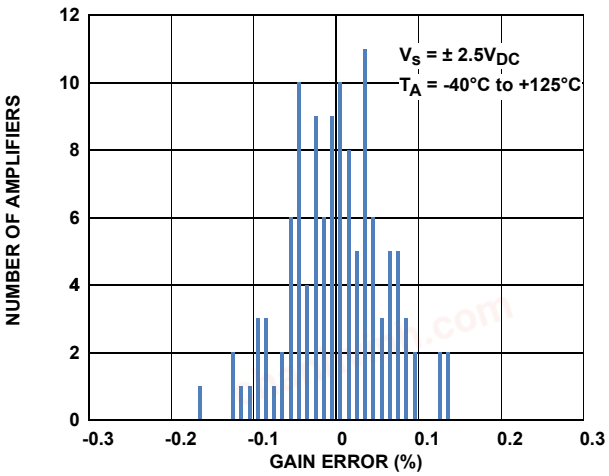


FIGURE 7. PGIA GAIN ERROR DISTRIBUTION, G = 100

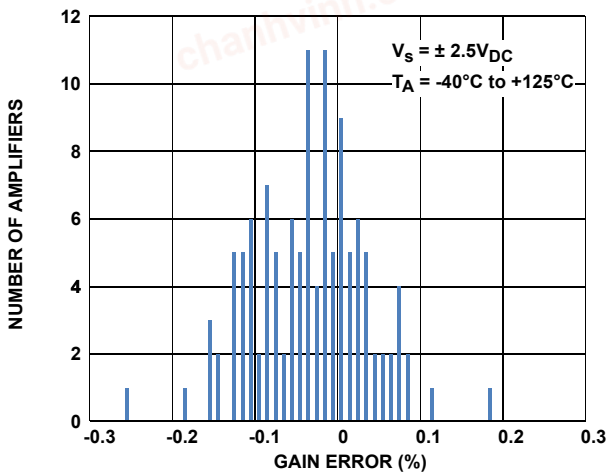


FIGURE 8. PGIA GAIN ERROR DISTRIBUTION, G = 1,000

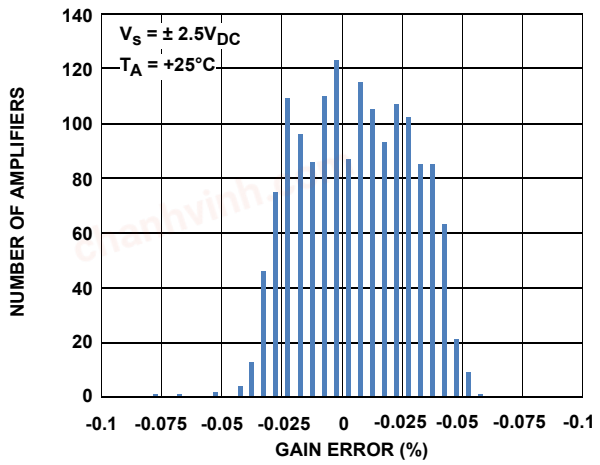


FIGURE 9. PGIA GAIN ERROR DISTRIBUTION, G = 1 TO 1,000

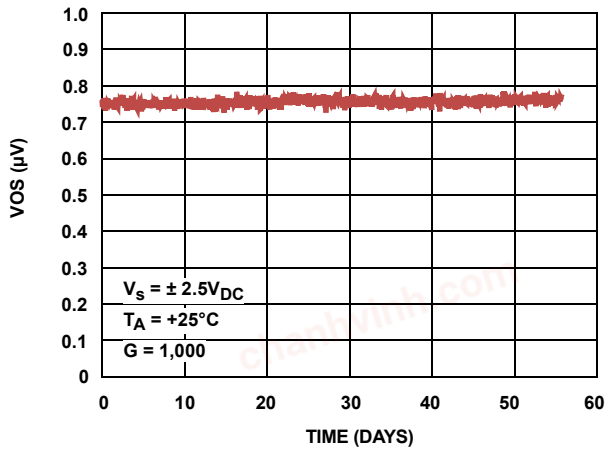


FIGURE 10. PGIA LONG TERM DRIFT OFFSET VOLTAGE

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Typical Instrumentation Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified. **(Continued)**

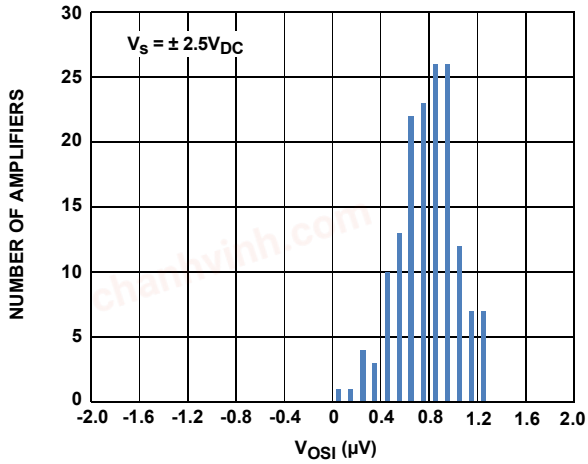


FIGURE 11. PGIA INPUT OFFSET VOLTAGE DISTRIBUTION

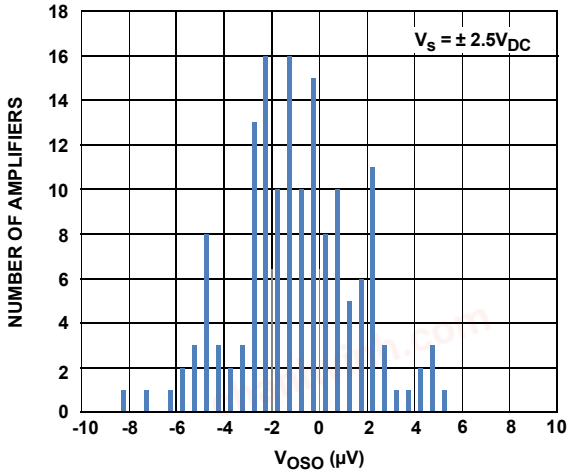


FIGURE 12. PGIA OUTPUT OFFSET VOLTAGE DISTRIBUTION

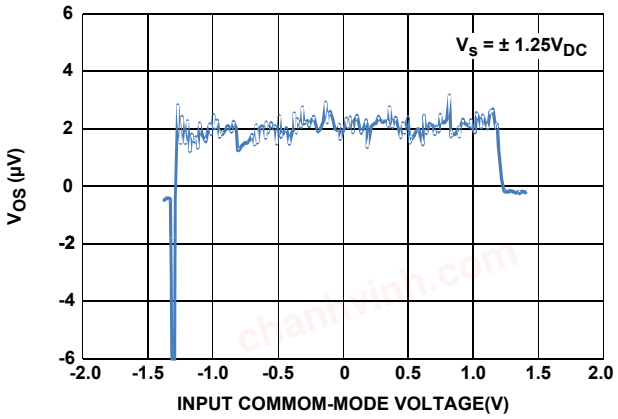


FIGURE 13. PGIA RTI VOS vs COMMON-MODE VOLTAGE

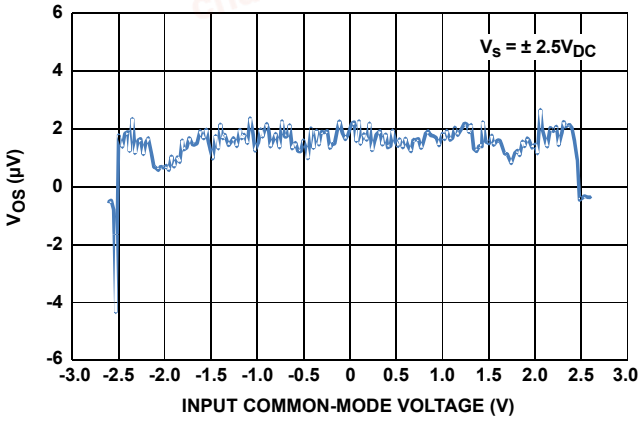


FIGURE 14. PGIA RTI VOS vs COMMON-MODE VOLTAGE

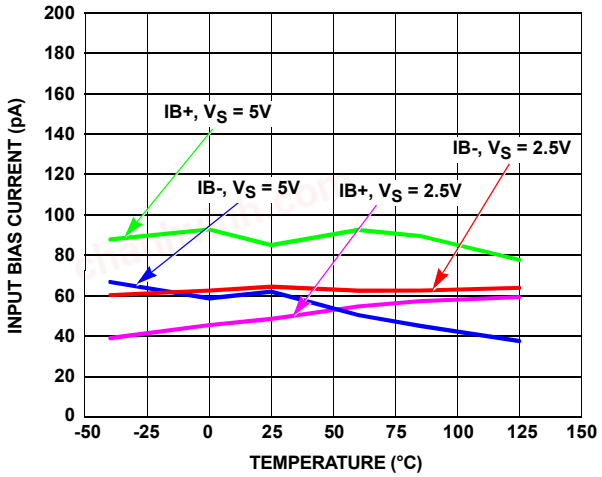


FIGURE 15. PGIA INPUT BIAS CURRENT vs TEMPERATURE

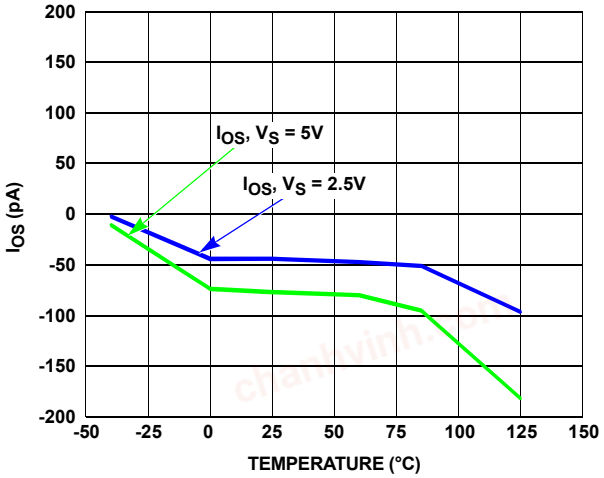


FIGURE 16. PGIA I_{OS} vs TEMPERATURE

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Typical Instrumentation Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified. **(Continued)**

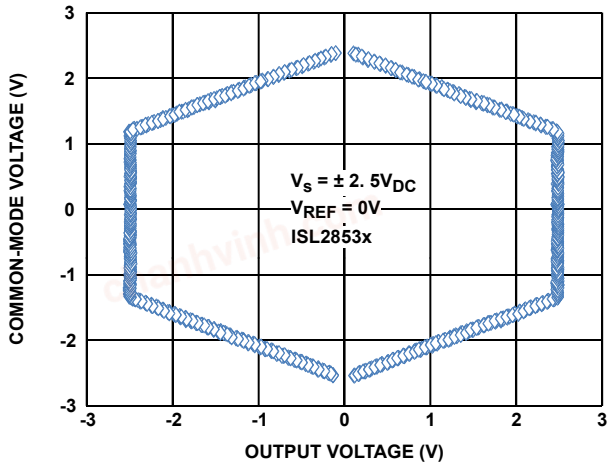


FIGURE 17. PGIA INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE

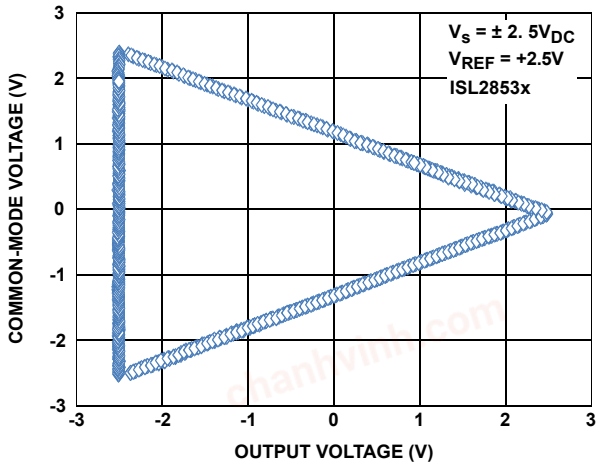


FIGURE 18. PGIA INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE

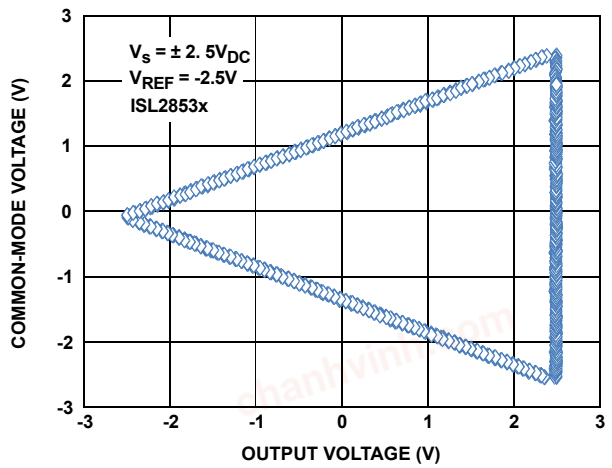


FIGURE 19. PGIA INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE

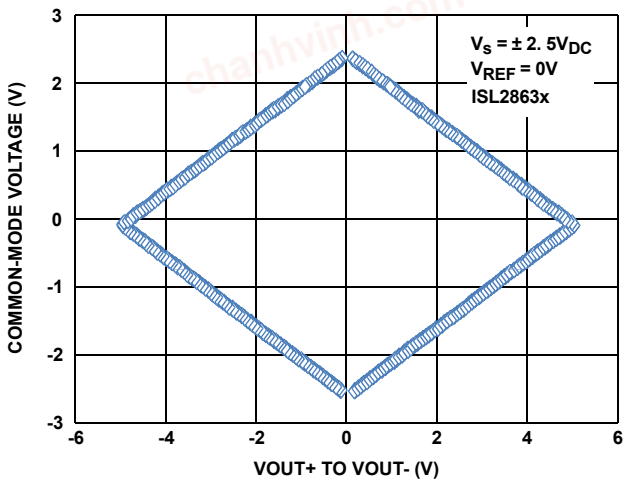


FIGURE 20. PGIA INPUT COMMON-MODE RANGE vs DIFFERENTIAL OUTPUT VOLTAGE

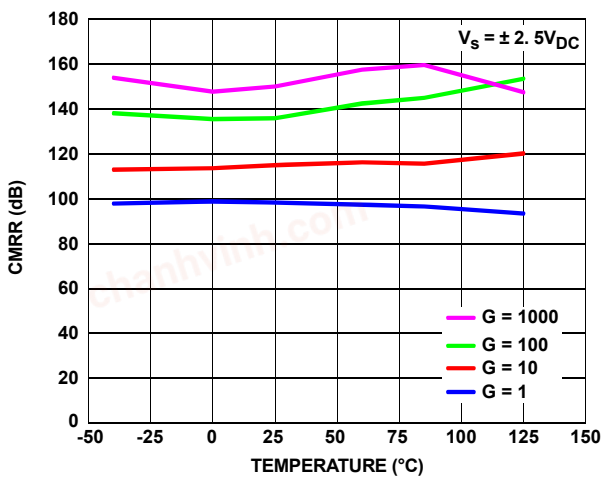


FIGURE 21. PGIA CMRR vs TEMPERATURE

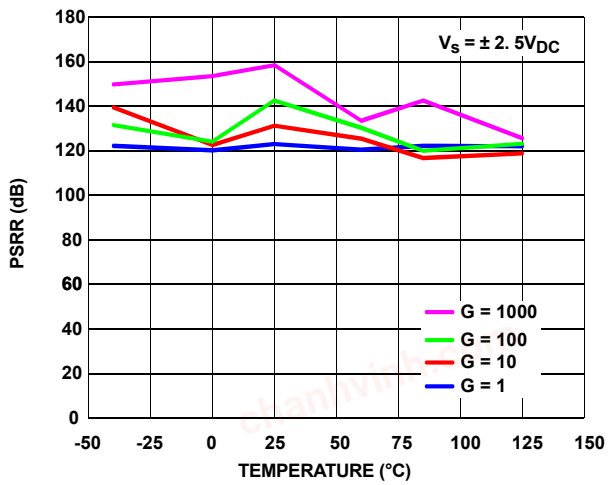


FIGURE 22. PGIA PSRR vs TEMPERATURE

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Typical Instrumentation Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified. **(Continued)**

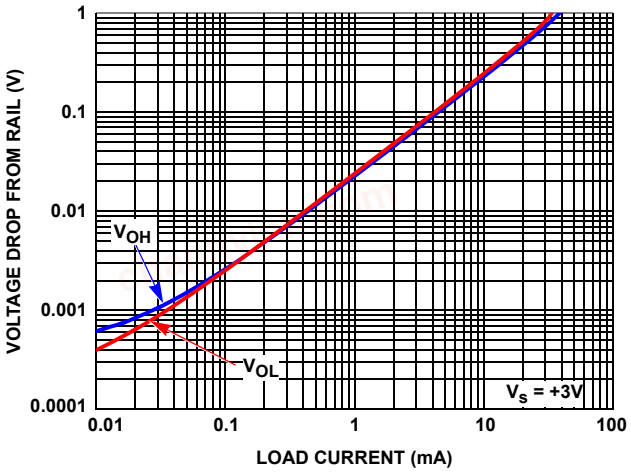


FIGURE 23. PGIA OUTPUT VOLTAGE SWING vs OUTPUT CURRENT, ISL2853x

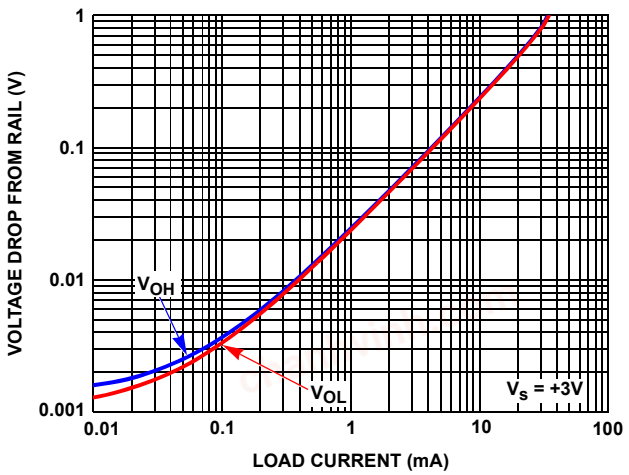


FIGURE 24. PGIA OUTPUT VOLTAGE SWING vs OUTPUT CURRENT, ISL2863x

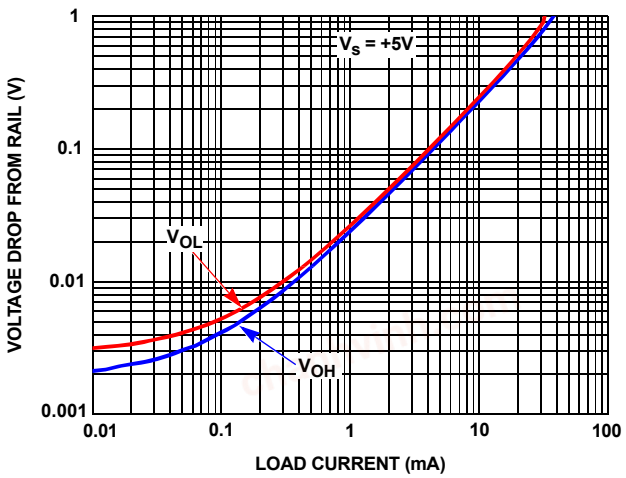


FIGURE 25. PGIA OUTPUT VOLTAGE SWING vs OUTPUT CURRENT, ISL2853x

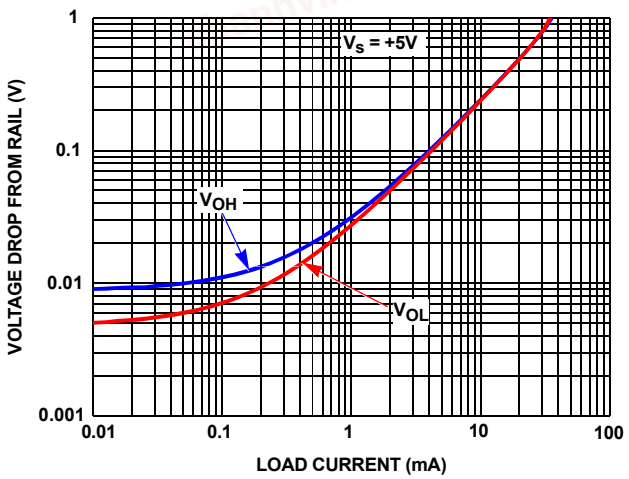


FIGURE 26. PGIA OUTPUT VOLTAGE SWING vs OUTPUT CURRENT, ISL2863x

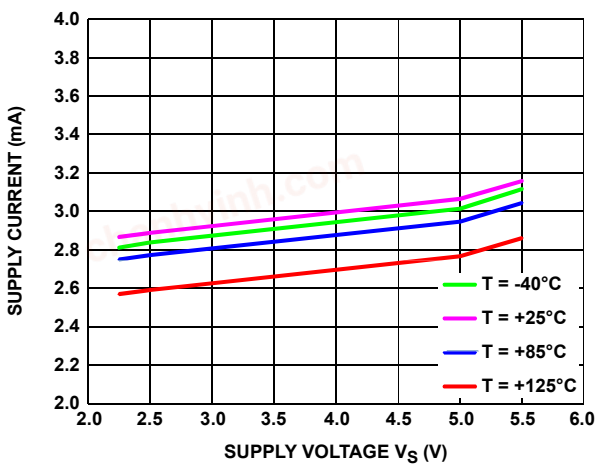


FIGURE 27. SUPPLY CURRENT vs SUPPLY VOLTAGE vs TEMPERATURE

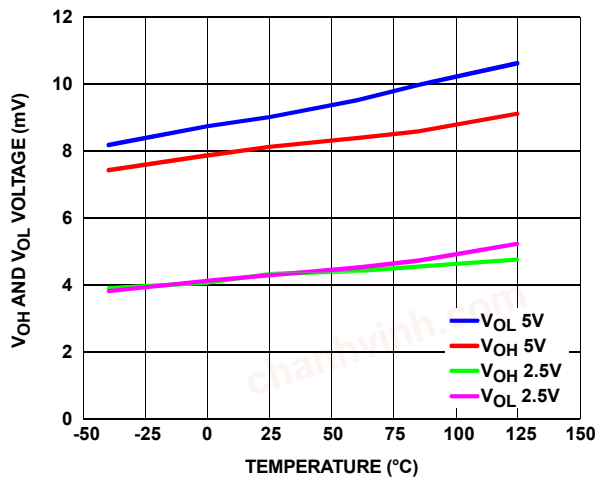


FIGURE 28. PGIA V_{OH} AND V_{OL} vs TEMPERATURE

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Typical Instrumentation Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified. **(Continued)**

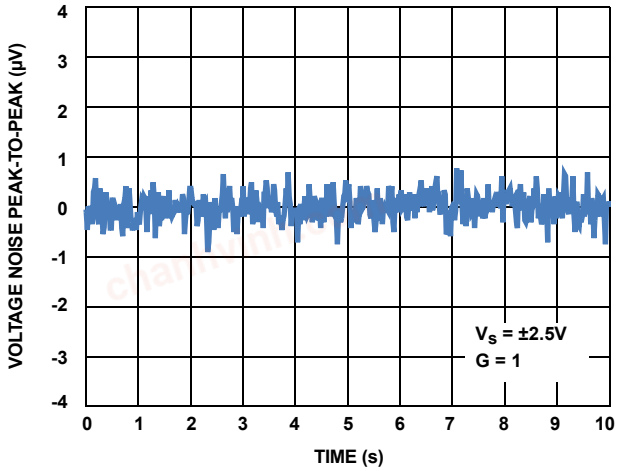


FIGURE 29. PGIA 0.1Hz TO 10Hz NOISE

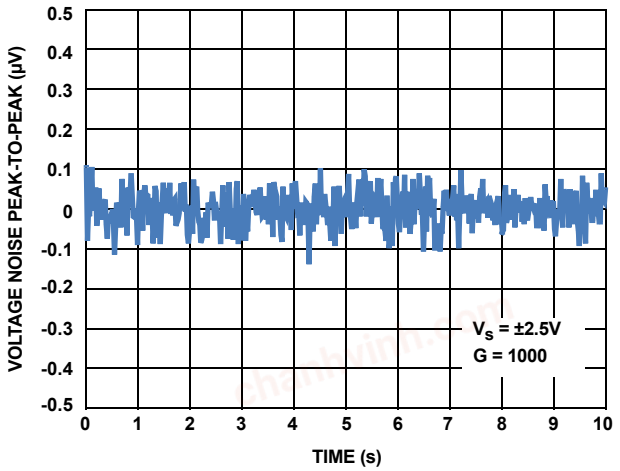


FIGURE 30. PGIA 0.1Hz TO 10Hz NOISE

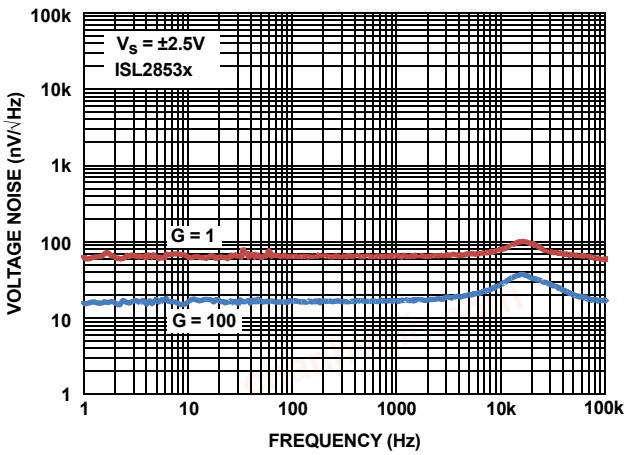


FIGURE 31. PGIA VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY, 1Hz TO 100kHz

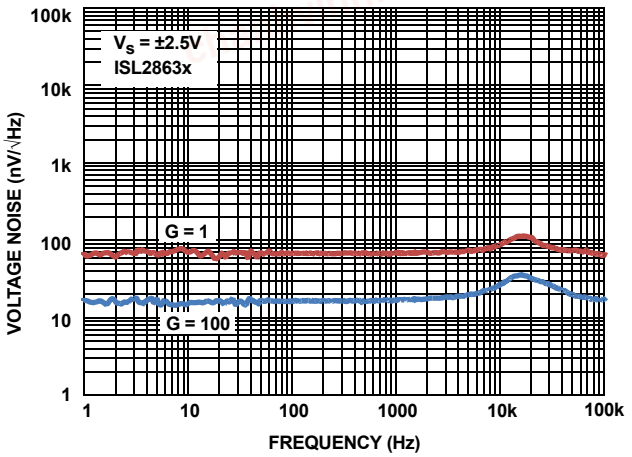


FIGURE 32. PGIA VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY, 1Hz TO 100kHz

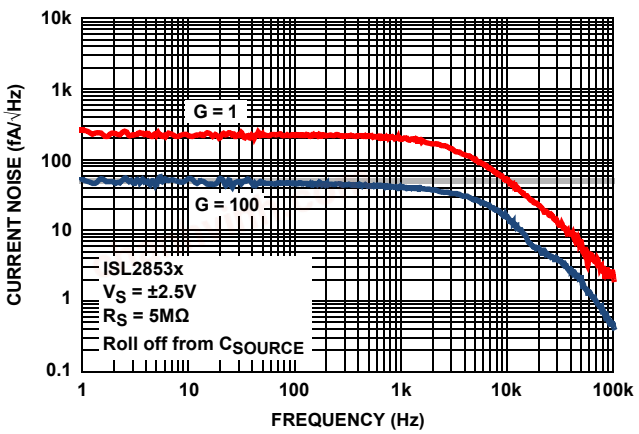


FIGURE 33. PGIA CURRENT NOISE SPECTRAL DENSITY 1Hz TO 100kHz, ISL2853x

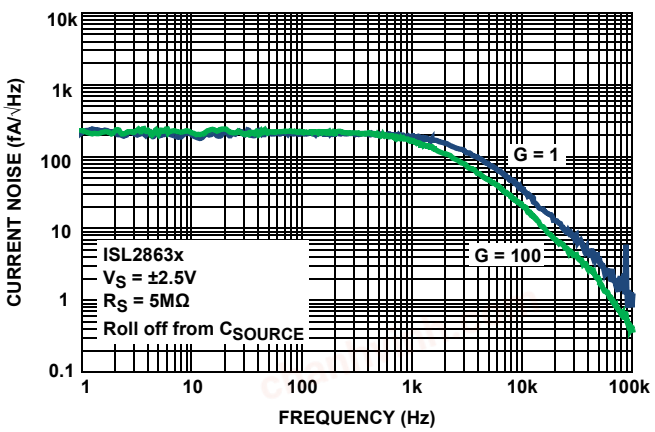


FIGURE 34. PGIA CURRENT NOISE SPECTRAL DENSITY 1Hz TO 100kHz, ISL2863x

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Typical Instrumentation Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified. **(Continued)**

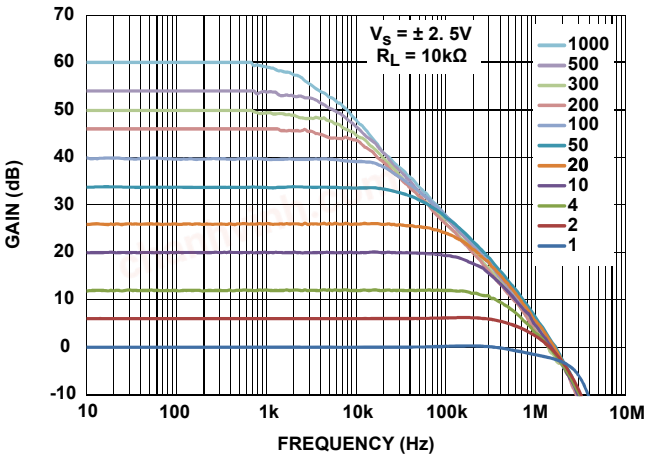


FIGURE 35. PGIA GAIN VS FREQUENCY vs GAIN SETTINGS

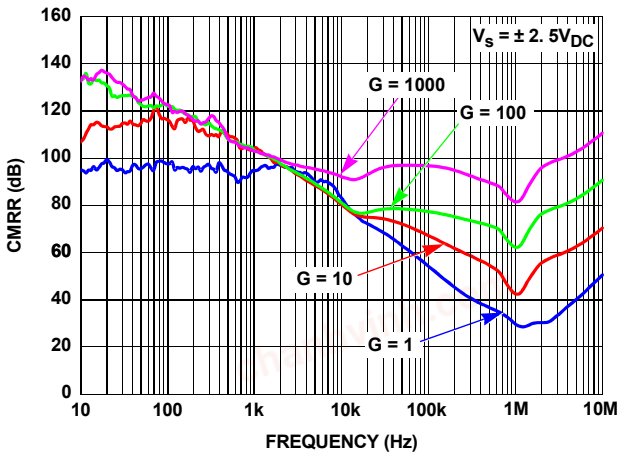


FIGURE 36. PGIA CMRR vs FREQUENCY

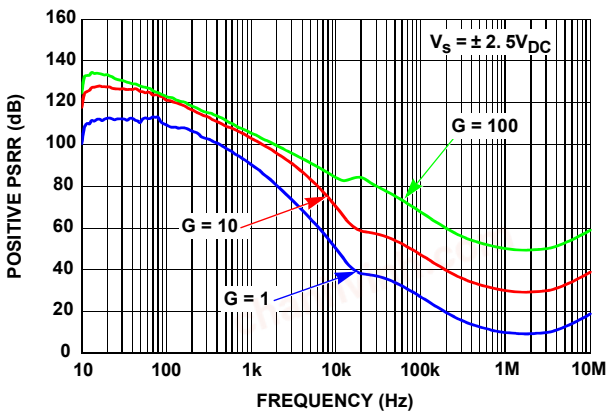


FIGURE 37. PGIA POSITIVE PSRR vs FREQUENCY

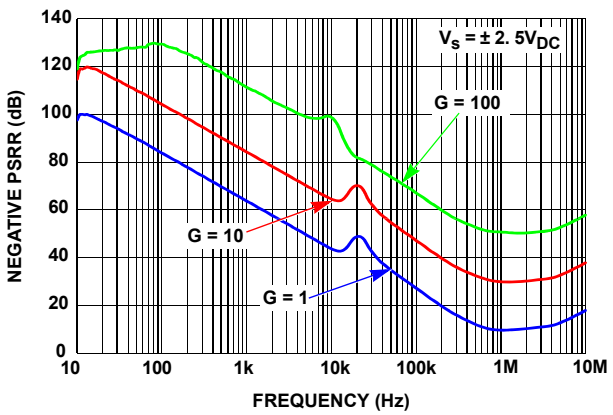


FIGURE 38. PGIA NEGATIVE PSRR vs FREQUENCY

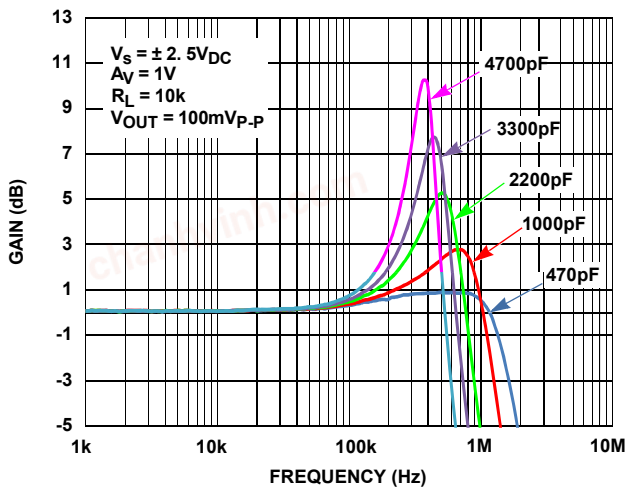


FIGURE 39. PGIA GAIN vs FREQUENCY vs CL, ISL2853x

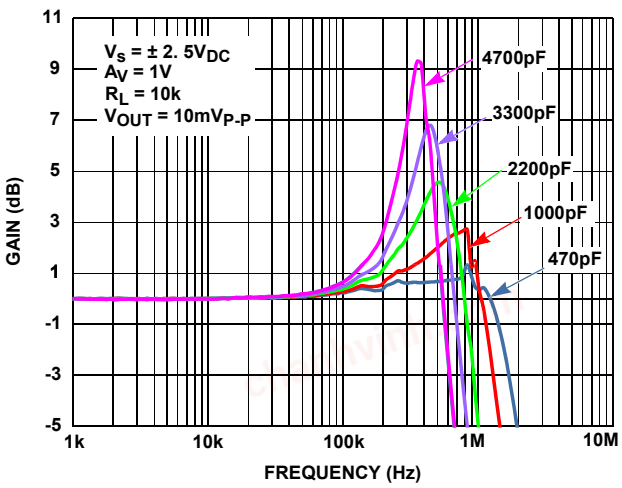


FIGURE 40. PGIA GAIN vs FREQUENCY vs CL, ISL2863x

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Typical Instrumentation Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified. **(Continued)**

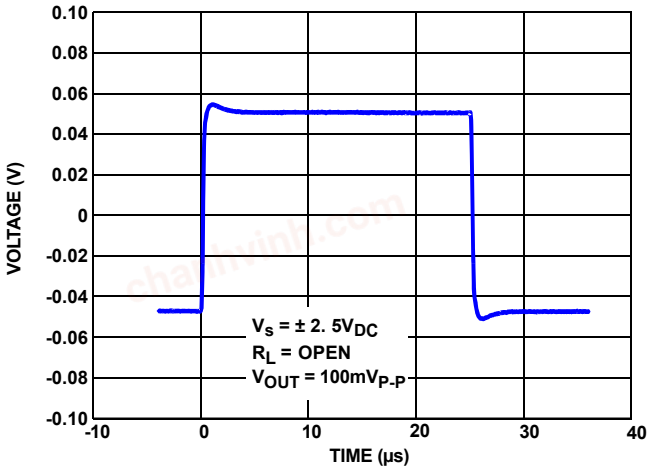


FIGURE 41. PGIA SMALL SIGNAL PULSE RESPONSE, G = 1, ISL2853x

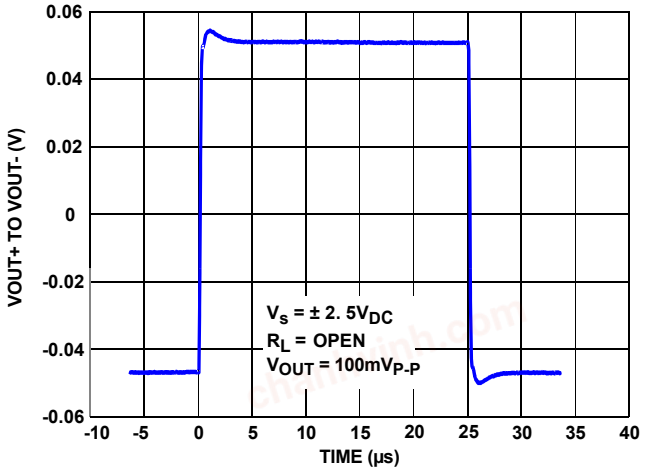


FIGURE 42. PGIA SMALL SIGNAL PULSE RESPONSE, G = 1, ISL2863x

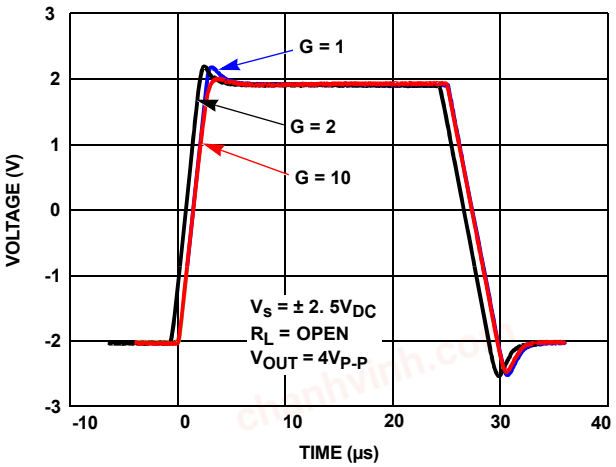


FIGURE 43. PGIA LARGE SIGNAL PULSE RESPONSE, G = 1, 2, 10 ISL2853x

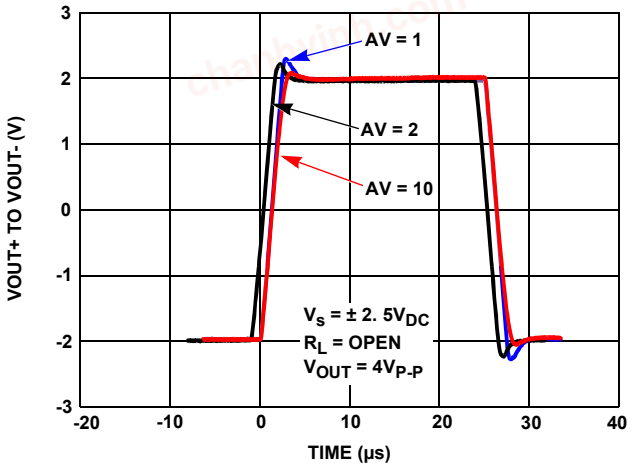


FIGURE 44. PGIA LARGE SIGNAL PULSE RESPONSE, G = 1, 2, 10 ISL2863x

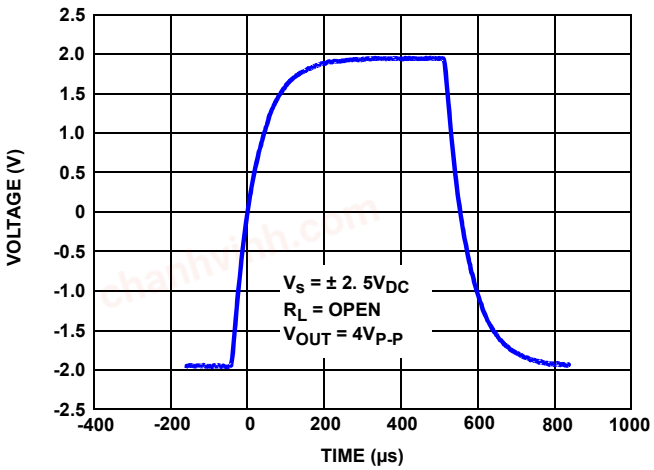


FIGURE 45. PGIA LARGE SIGNAL PULSE RESPONSE, G = 1000, ISL2853x

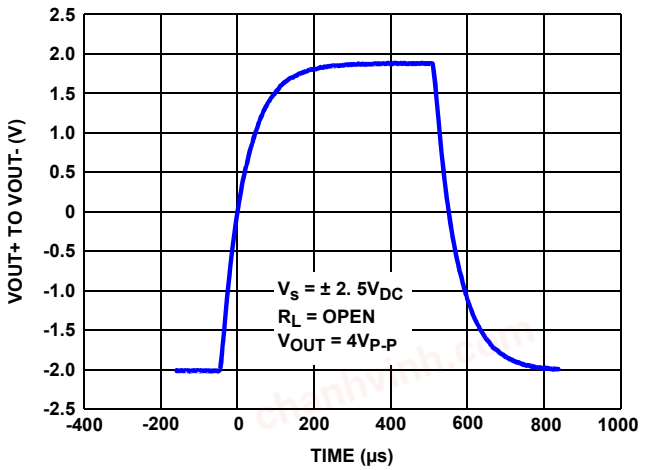


FIGURE 46. PGIA LARGE SIGNAL PULSE RESPONSE, G = 1000, ISL2863x

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Typical Instrumentation Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified. **(Continued)**

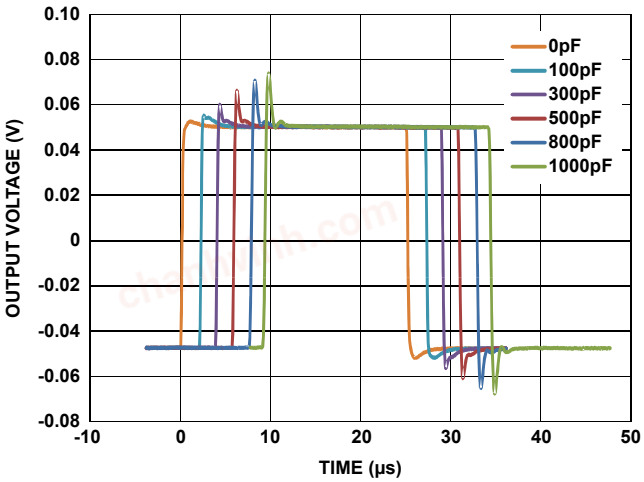


FIGURE 47. CAPACITIVE LOAD OVERSHOOT; ISL2853x

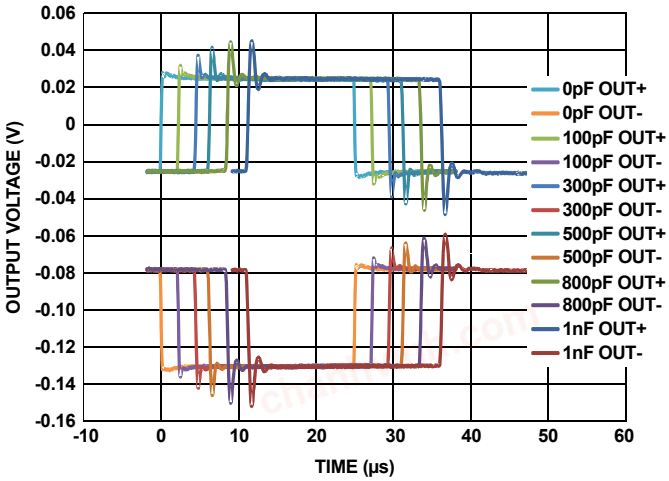


FIGURE 48. CAPACITIVE LOAD OVERSHOOT; ISL2863x

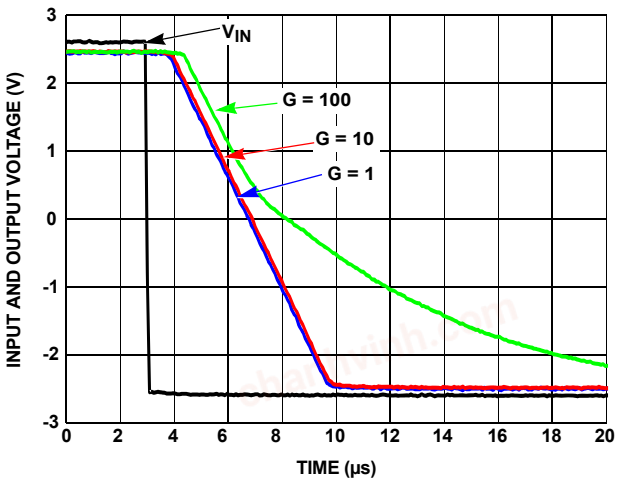


FIGURE 49. POSITIVE OVERLOAD RECOVERY TIME, ISL2853x

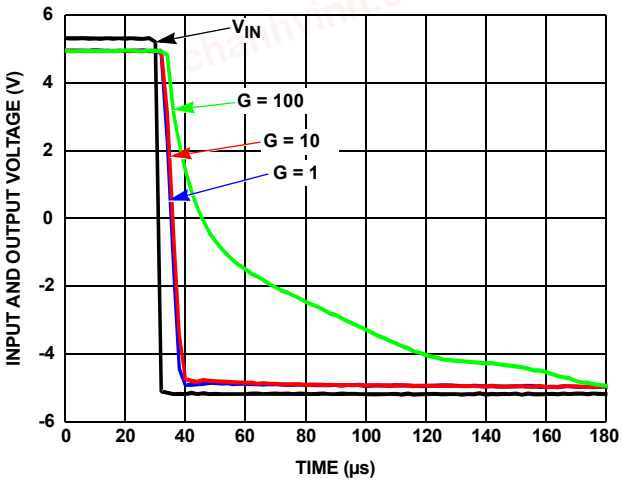


FIGURE 50. POSITIVE OVERLOAD RECOVERY TIME, ISL2863x

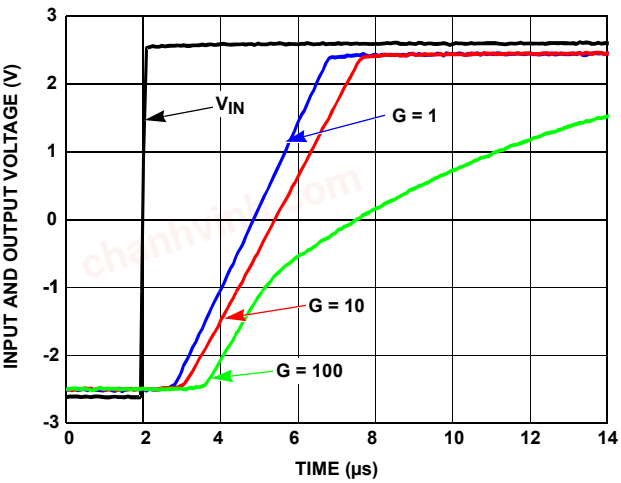


FIGURE 51. NEGATIVE OVERLOAD RECOVERY TIME, ISL2853x

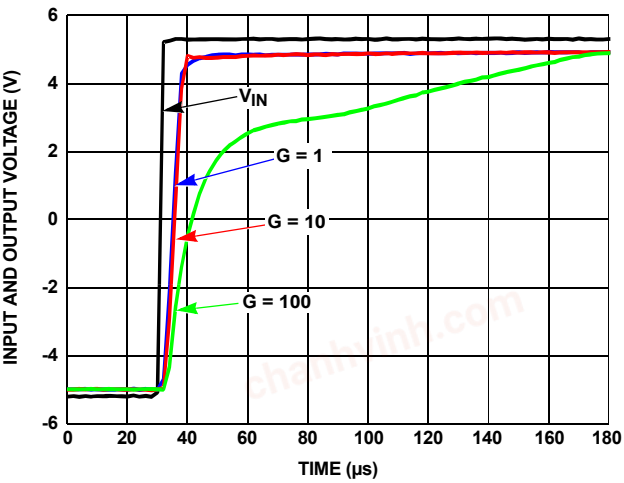


FIGURE 52. NEGATIVE OVERLOAD RECOVERY TIME, ISL2863x

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Typical Instrumentation Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified. **(Continued)**

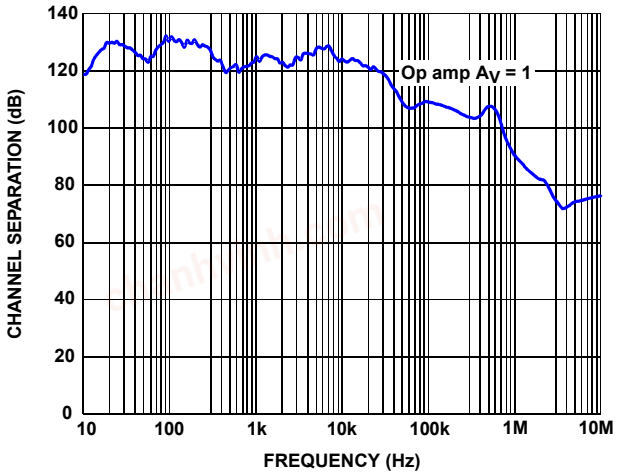


FIGURE 53. CHANNEL SEPARATION vs FREQUENCY, HOSTILE INA, MONITOR OPAMP

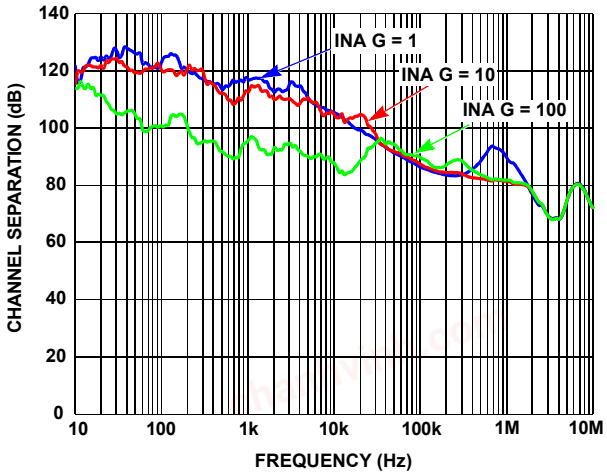


FIGURE 54. CHANNEL SEPARATION vs FREQUENCY, HOSTILE OPAMP, MONITOR INA

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Typical Operational Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified.

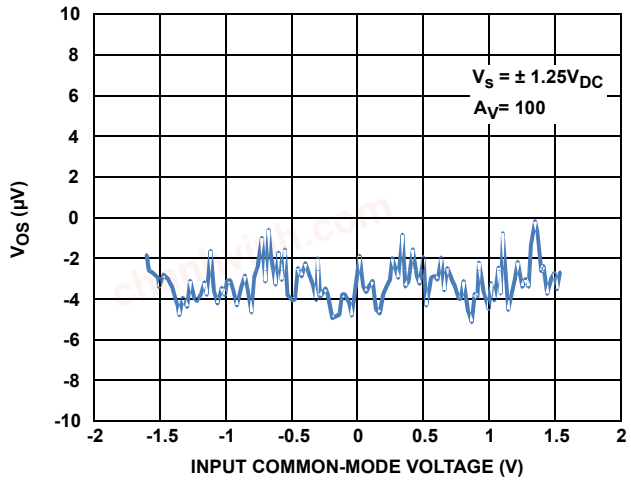


FIGURE 55. OP AMP V_{OS} vs COMMON-MODE

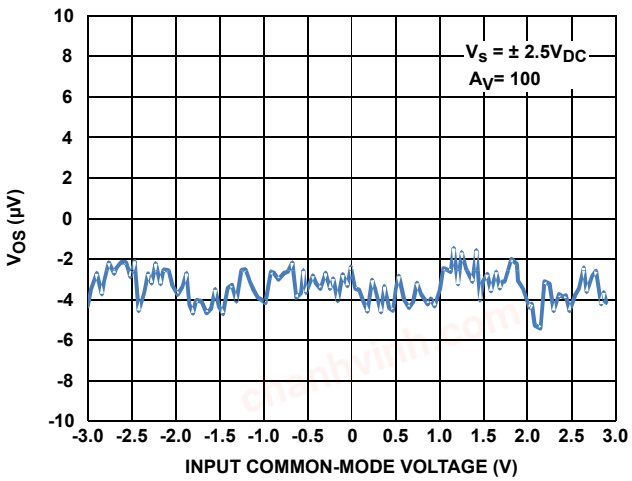


FIGURE 56. OP AMP V_{OS} vs COMMON-MODE

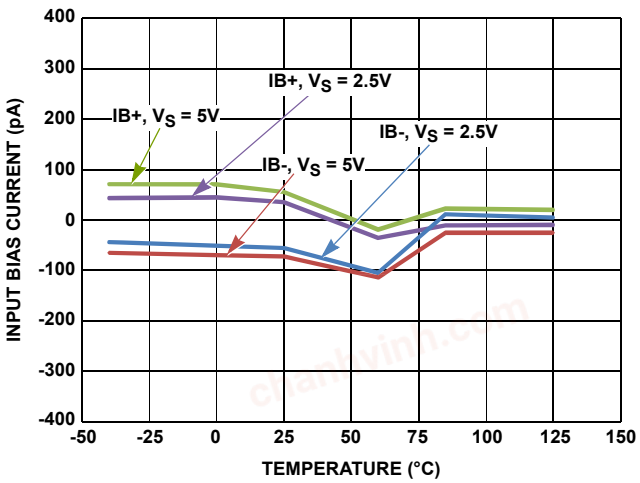


FIGURE 57. OP AMP BIAS CURRENT vs TEMPERATURE

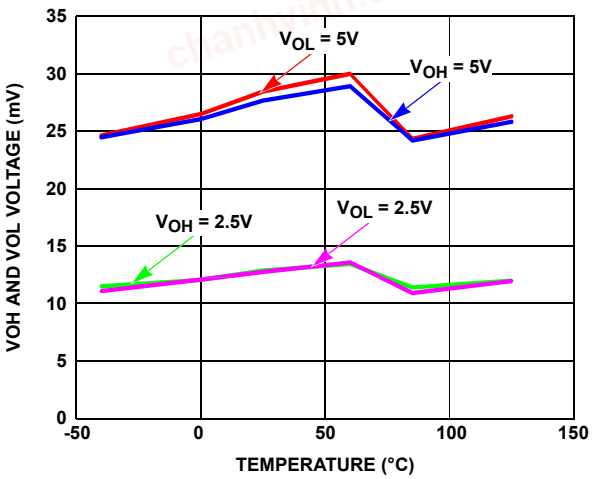


FIGURE 58. OP AMP V_{OH} AND V_{OL} vs TEMPERATURE

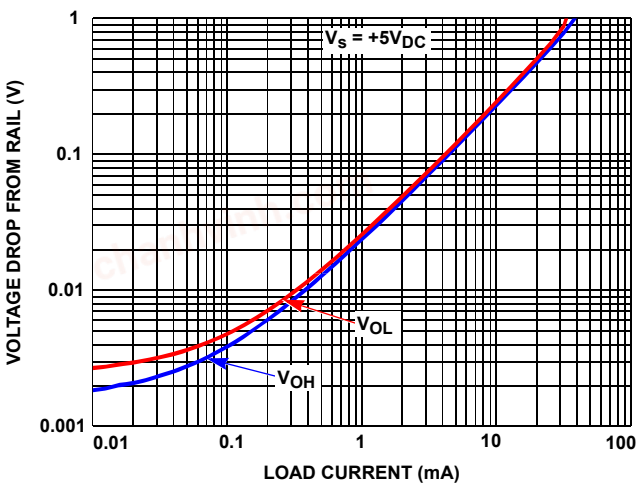


FIGURE 59. OP AMP OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

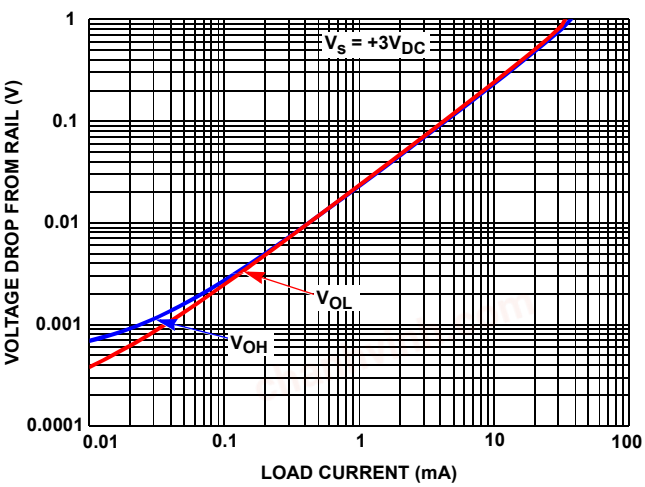


FIGURE 60. OP AMP OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

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Typical Operational Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified. **(Continued)**

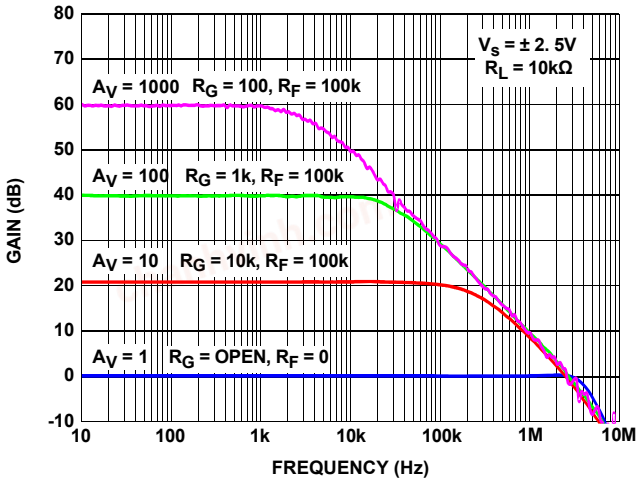


FIGURE 61. OP AMP GAIN vs FREQUENCY

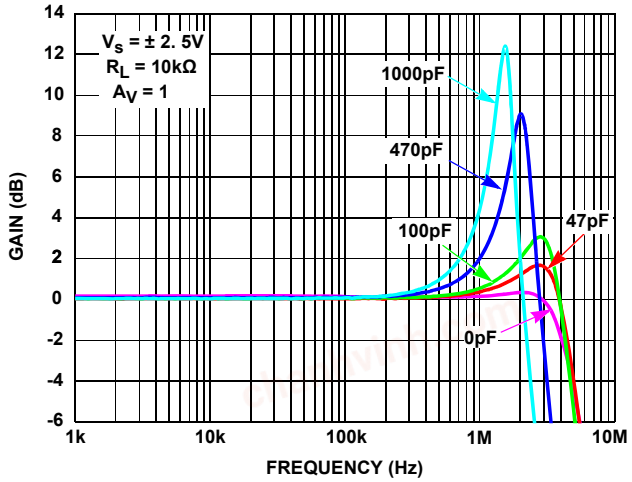


FIGURE 62. OP AMP CAPACITIVE LOAD vs FREQUENCY

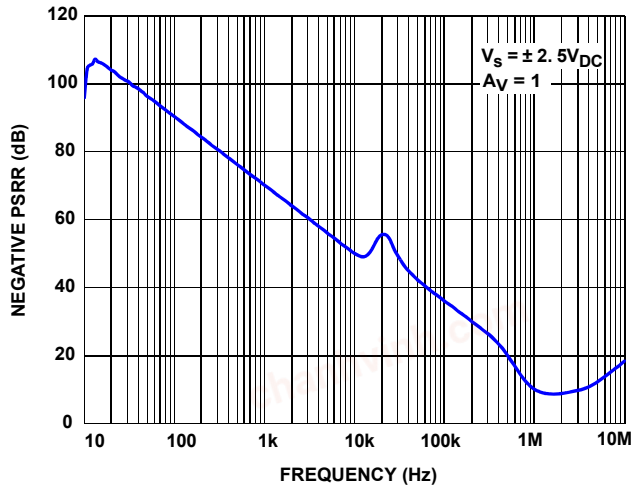


FIGURE 63. OP AMP POWER SUPPLY REJECTION RATIO

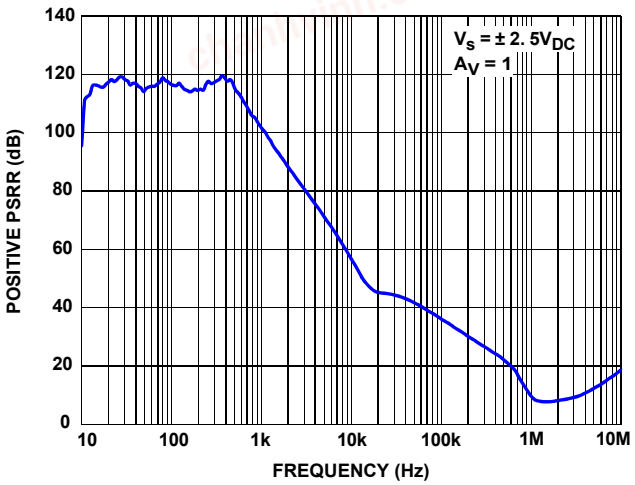


FIGURE 64. OP AMP POWER SUPPLY REJECTION RATIO

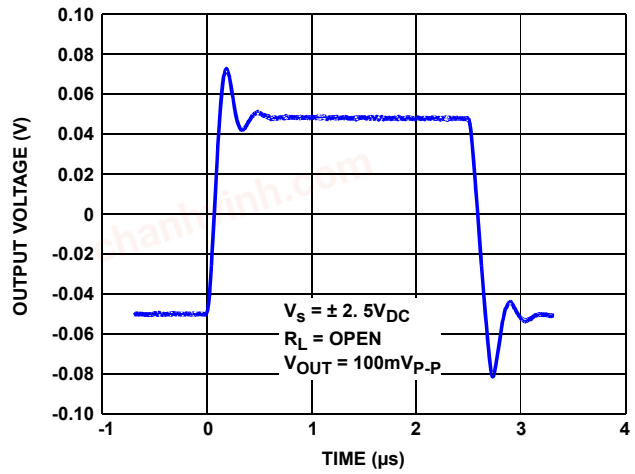


FIGURE 65. OP AMP SMALL SIGNAL TRANSIENT RESPONSE

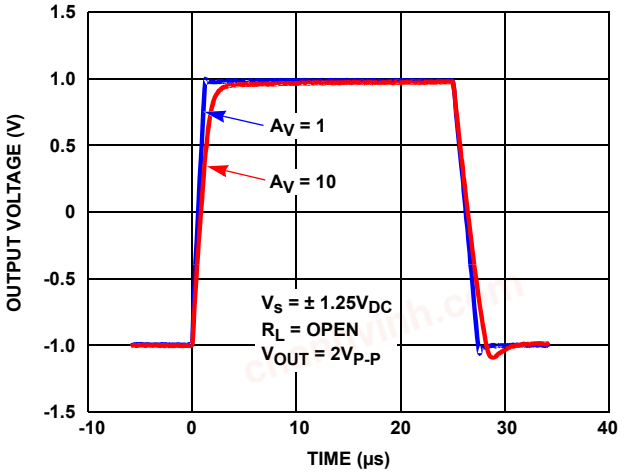


FIGURE 66. OP AMP LARGE SIGNAL TRANSIENT RESPONSE

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Typical Operational Amplifier Performance Curves

T_A = +25°C, V_{CM} = Mid Supply, unless otherwise specified. **(Continued)**

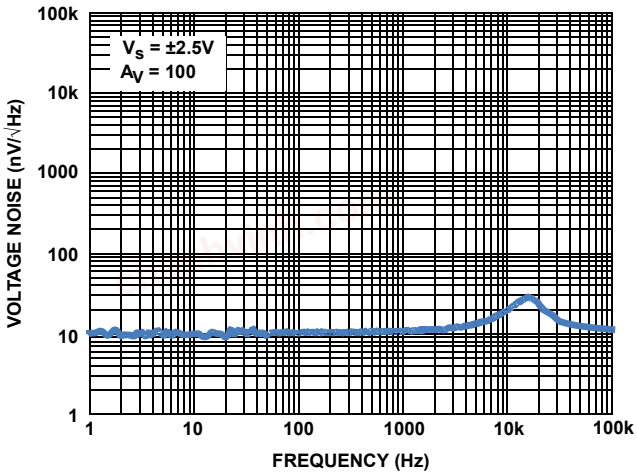


FIGURE 67. OP AMP VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

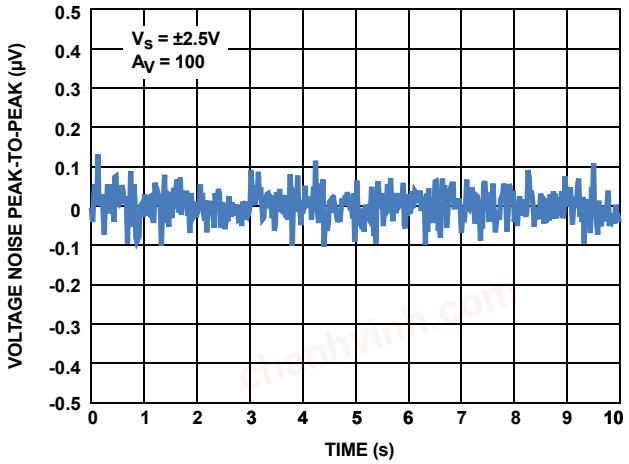


FIGURE 68. OP AMP 0.1Hz TO 10Hz PEAK-TO-PEAK VOLTAGE NOISE

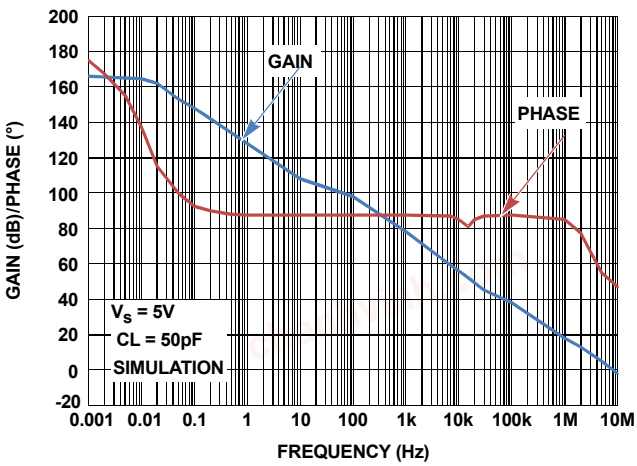


FIGURE 69. OP AMP OPEN-LOOP GAIN AND PHASE vs FREQUENCY

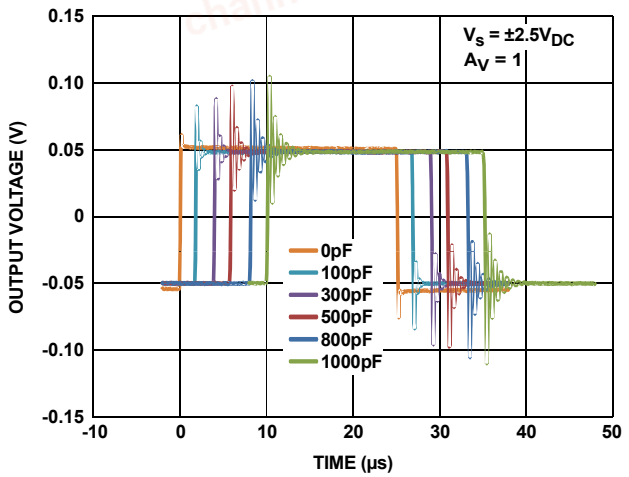


FIGURE 70. OP AMP CAPACITIVE LOAD OVERSHOOT

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Applications Information

Precision Sensor Amplifier

The ISL2853x and ISL2863x are a family of ultra high precision instrumentation amplifiers. These amplifiers feature zero drift circuitry that provide auto offset voltage correction and noise reduction, delivering very low offset voltage drift of 5nV/°C and a low 1/F noise frequency corner down in the sub Hz range. The instrumentation amplifier integrates precision matched resistors for the front gain stage and the differential second stage, providing very high gain accuracy and excellent CMRR. The precision performance makes these amplifiers ideal for analog sensor front-end, instrumentation and data acquisition applications such as weigh scales, flow sensors and shunt current sensing that require very low noise and high dynamic range.

SINGLE-ENDED OUTPUT

The ISL28533, ISL28534 and ISL28535 family of parts are differential input, single-ended output instrumentation amplifiers using a three op amp architecture (see Figure 71). The first stage is differential input/differential output and is used to set the gain. The second stage is a difference amplifier, which is used to remove the common-mode voltage from the differential signal. With the integrated gain resistors and the programmable gains, these instrumentation amplifiers require no external components for gain setting and operation.

There is an additional uncommitted zero drift operational amplifier included on the chip. This can be used to drive the REF pin if needed to provide a low impedance to REF. The REF pin is used to shift the output DC reference. Note that on this device the REF input is a resistor that is part of the difference amplifier non-inverting input. To ensure good common-mode rejection in the output stage, the REF pin should be driven by a low impedance source such as the output of amplifier A4. Any parasitic resistance added to the REF pin degrades the common-mode rejection of the difference amplifier.

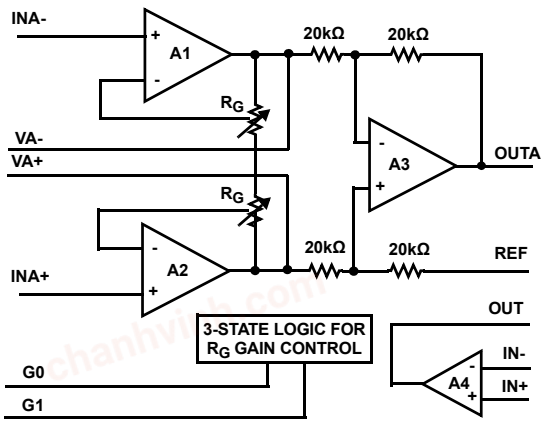


FIGURE 71. ISL2853x BLOCK DIAGRAM

DIFFERENTIAL OUTPUT

The ISL28633, ISL28634 and ISL28635 family of parts are differential input, differential output instrumentation amplifiers and are ideal as a preamplifier/driver for differential input ADCs (see Figure 72). With the integrated gain resistors and the programmable gains, these instrumentation amplifiers require no external components for gain setting and operation.

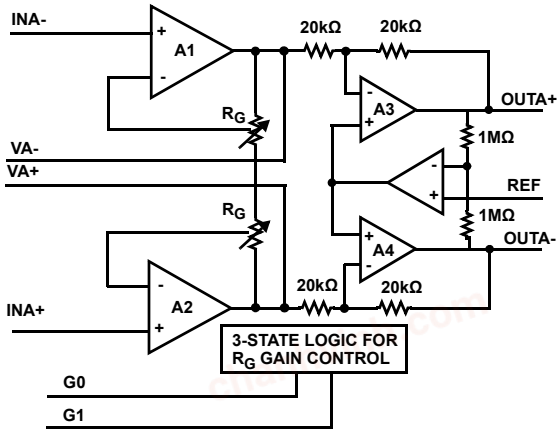


FIGURE 72. ISL2863x BLOCK DIAGRAM

The first stage amplifier is identical to the first stage in the ISL2853x family. The output stage is a difference amplifier, which is configured to provide differential output drive. The REF pin is also available on this device and can be used to provide a DC shift of the output signal. On this device the REF pin is a high impedance input of an operational amplifier. The voltage used to drive this pin can be developed using a resistor divider without the need of an additional buffer without penalty of CMRR degradation.

RFI FILTER

The instrumentation amplifier inputs of the ISL2853x and ISL2863x have RFI filters for Electro Magnetic Interference (EMI) reduction. In EMI sensitive applications, the high frequency RF signal can appear as a rectified DC offset at the output of precision amplifiers. Because the gain of the precision front-end can be 100 or greater, it is critical not to amplify any conducted or radiated noise that may be present at the amplifier inputs. The RFI input is a 1kΩ, 3pF LPF with a corner frequency of approximately 50MHz (see Figure 73).

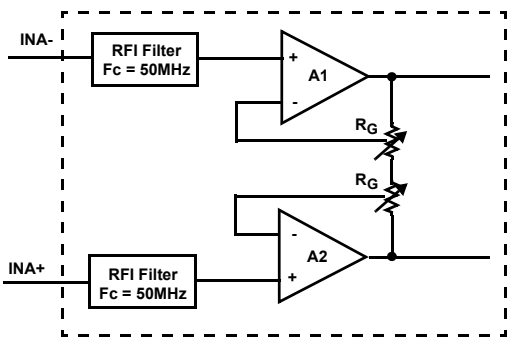


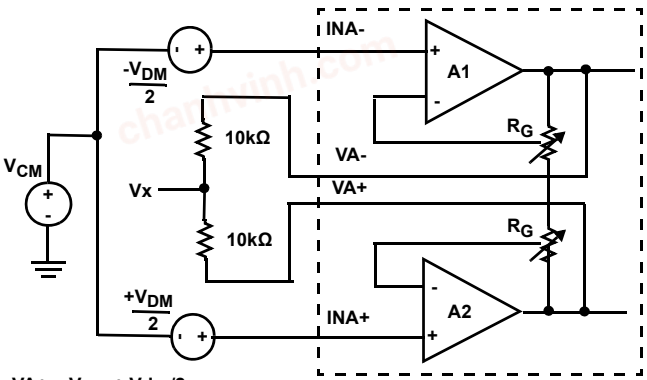
FIGURE 73. RFI FILTER INPUTS

GAIN STAGE OUTPUT VA+/VA- PINS

The ISL2853x and ISL2863x instrumentation amplifiers include pinouts for the output of the differential gain stage. VA+ is referenced to the non-inverting input of the difference amplifier while VA- is referenced to the inverting input. These pins can be

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used for measuring the input common-mode voltage for sensor feedback and health monitoring. The differential gain stage output pins VA+ and VA- buffers the input common-mode voltage while amplifying differential voltage. By tying two resistor across VA+ and VA-, the buffered input common-mode voltage is extracted at the midpoint of the resistors (see Figure 74). This voltage can be sent to an ADC for sensor monitoring or feedback control, improving the precision and accuracy of the sensor.



VA+ = Vcm + Vdm/2
VA- = Vcm - Vdm/2
Vx = [(VA+) + (VA-)] / 2
Vx = Vcm

FIGURE 74. COMMON-MODE SENSING WITH VA+/VA- PINS

PROGRAMMABLE GAIN LOGIC

The ISL2853x and ISL2863x feature a three-state logic interface for digital programming of the amplifier gain. This allows the PGIA's gain to be changed without an external gain setting resistors, improving the gain accuracy and reducing component count.

The three-state logic pins have voltage levels for recognizing valid logic states to set the gain of the amplifier (see Figure 75). With three logic states per input, this allows nine gain settings with just two digital input pins (see Table 3).

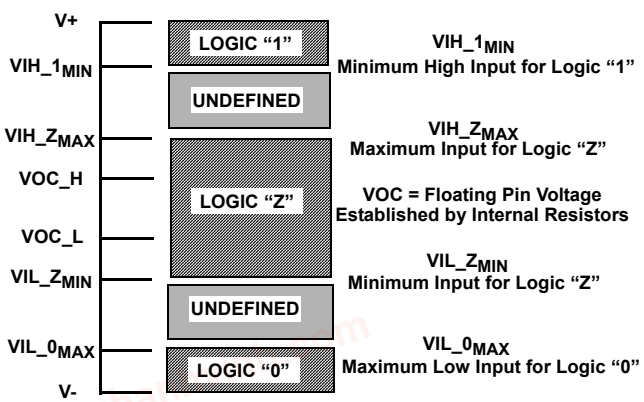


FIGURE 75. G0/G1 LOGIC THRESHOLD LEVELS

Logic states of the G0/G1 pins can be achieved by simple pin-strapping to the supply rails for logic HI/LOW, or may be left floating for logic Z. Internal resistors on the G0/G1 pins set the logic level to mid-supply for logic Z. Alternatively a microcontroller can be used to drive the pins HI/LOW or they may be left in a High-Z state. The V_{IH}, V_{IL} and logic Z threshold levels are TTL/CMOS compatible for single 5V and 3V supplies. See Table 2 for logic threshold levels.

It is important to note that logic threshold levels are referenced to the V- negative supply rail of the amplifier. For dual supply operation of the instrumentation amplifier logic threshold levels are shifted by the magnitude of V-. Externally driven logic signals require level shifting to properly set amplifier gain.

TABLE 2. LOGIC THRESHOLD VALUES

G0/G1	PARAMETER	THRESHOLD VOLTAGE	+5VDC	+3VDC
1	V_{IH_1MIN}	0.8*Vs	4V	2.4V
Z	V_{IH_ZMAX}	0.6*Vs	3V	1.8V
	V_{OC_H}	0.55*Vs	2.75V	1.65V
	V_{OC_L}	0.45*Vs	2.5V	1.35V
	V_{IL_ZMIN}	0.4*Vs	2V	1.2V
0	V_{IL_0MAX}	0.2*Vs	1V	0.6V

NOTE: Vs = (V+) - (V-)

TABLE 3. PROGRAMMABLE GAIN SETTINGS

G1	G0	GAIN (V/V)		
		ISL28533 ISL28633	ISL28534 ISL28634	ISL28535 ISL28635
0	0	1	1	1
0	Z	2	2	100
0	1	4	10	120
Z	0	5	50	150
Z	Z	10	100	180
Z	1	20	200	200
1	0	40	300	300
1	Z	50	500	500
1	1	100	1000	1000

GAIN SETTING WITH DCP

For applications without a tri-state driver the alternative solution for programmable switching the 9 gain settings is to use a DCP. Using a Dual DCP implements the capability to select all 9 gains with an I^2C/SPI bus interface, saving valuable GPIO lines. The ISL23328 is a dual 128 tap DCP that can switch the G0 and G1 pins with an I^2C interface (see Figure 76). The wiper of the DCP can be swept from V+ to V- in 128 steps.

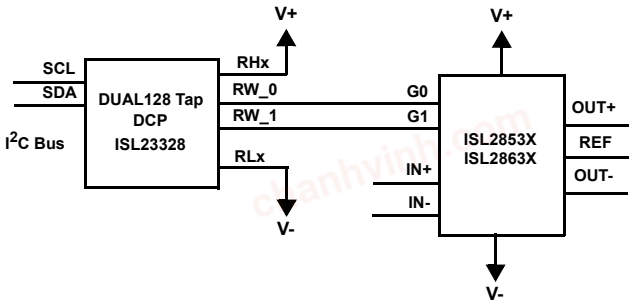


FIGURE 76. GAIN SWITCHING WITH ISL23328 DCP

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GAIN SWITCHING DELAY TIME

The G0 and G1 pins change the gain setting of the PGIA. For applications that must switch gains at high frequency, consider that there is a gain switching propagation delay of ~1µs before output response. The total response time for a gain change must also include the amplifier output settling time. See “Electrical Specifications” on page 8 for output settling time.

DUAL SUPPLY OPERATION

ISL2853x and ISL2863x typical applications utilize single supply operation. The single supply range is from 2.5V to 5V, but the amplifiers can also operate with split supplies from ±1.25V to ±2.5V. The G0 and G1 logic thresholds are referenced to the most negative supply rail (V-), therefore a logic level shifter is needed in split supply applications when the G0 and G1 pins are not strapped to the amplifier supply pins (i.e., when driven by a single supply logic device).

POWER SUPPLY AND REF PIN SEQUENCING

As the REF pin in some applications is tied to a high accuracy voltage reference VREF (such as the ISL21090), proper care must be taken that the voltage at REF does not come up prior to supply voltages V+ and V-. The REF pin ESD protection diodes will be forward biased when the voltage at REF exceeds V+ or V- by more than 0.3V. For applications where REF must be present before V+ or V-, it is recommended to use the ISL2863x family of PGIA. As the REF pin is an very high impedance input, having a series resistance to limit the ESD diode current will not severely impact CMRR performance. Typically a 1kΩ resistor will adequately limit this current.

COMMON-MODE INPUT RANGE

The 3-op amp instrumentation amplifier architecture amplifies differential input voltage. The common-mode voltage is removed by the difference amplifier at the second stage. Consideration of input common-mode and differential voltage must be taken to not saturate the output of the A1 and A2 amplifiers. This is a common mistake when input differential voltages plus the input V_{CM} combined is large enough to saturate the output. The PGIA features rail to rail output amplifiers to maximize output dynamic range thus signals VA+, VA- and VOUT+/VOUT- can drive near the supply rails. Figures 17 through 20 give the typical input common-mode voltage range vs output voltage for different REF voltages.

Application Circuits

Typical application circuits for bridge sensor health monitor and active shield guard driver are shown in Figures 77 and 78.

Sensor Health Monitor

A bridge type sensor uses four matched resistive elements to create a balanced differential circuit. The bridge can be a combination of discrete resistors and resistive sensors for a quarter, half and full bridge applications. The bridge is excited by a low noise, high accuracy voltage reference or current source on two legs. The other two legs are the differential signal whose output voltage change is analogous to changes in the sensed environment. In a bridge circuit, the common-mode voltage of the differential signal is at the mid point potential voltage of the bridge excitation source. For example in a single supply system using a +5V reference for excitation, the common-mode voltage is +2.5V.

The concept of sensor health monitoring is to keep track of the bridge impedance within the data acquisition system. Changes in the environment, degradation over time or a faulty bridge resistive element will imbalance the bridge, causing measurement errors. Since the bridge differential output common-mode voltage is one-half the excitation voltage, by measuring this common mode the sensor impedance health can be monitored, for example through an ADC channel (see Figure 77 on page 28). While common-mode voltage can be measured directly off the bridge, this is not recommended because the bridge impedance is highly sensitive to any additional loading. Sensing off the legs directly can give an erroneous reading of the analog signal being measured. Since the VA+ and VA- pins buffer the input common-mode voltage, this provides a low impedance point to drive the ADC without using additional amplifiers. By continuously monitoring the common-mode voltage this gives an indication of sensor health.

Active Shield Guard Drive

Sensors that operate at far distances from the signal conditioning circuits are subject to noise environments that reduce the signal to noise ratio into an amplifier. Differential signaling and shielded cables are a few techniques that are used to reduce noise from sensitive signal lines. Reducing noise that the instrumentation amplifier cannot reject (high frequency noise or common-mode voltage levels beyond supply rail) improves measuring accuracy. Shielded cables offer excellent rejection of noise coupling into signal lines. However, cable impedance mismatch to signal wires form a common-mode error into the amplifier. Driving the cable shield to a low impedance potential reduces the impedance mismatch. The cable shield is usually tied to chassis ground as it makes an excellent low impedance point and is easily accessible. However, this may not always be the best potential voltage to tie the shield to, in particular for single supply amplifiers.

In some data acquisition systems the sensor signal amplifiers are powered with dual supplies (±5V or ±12V). By tying the shield to analog ground 0V, this places the common-mode voltage of the shield right at the middle of the supply bias - where the amplifiers operate with the best CMR performance. With single supply amplifiers becoming more popular choice as a sensor amplifier, shield at 0V is now at the lower power supply rail of the amplifier - typically a common-mode voltage where the same CMR performance degrades. Tying the shield at common-mode voltage of mid supply rail is most applicable for high impedance sensor applications.

An alternative solution for an improved shield guard drive is to use the VA+ and VA- pins for sensing common-mode and driving the shield to this voltage (see Figure 78 on page 28). Using the VA+ and VA- pins generate a low impedance reference of the input common-mode voltage. Driving the shield to the input common-mode voltage reduces cable impedance mismatch and improves CMR performance in single supply sensor applications. For further buffering of the shield driver, the additional unused op amp on the ISL2853x products can be used, reducing the need of adding an external amplifier.

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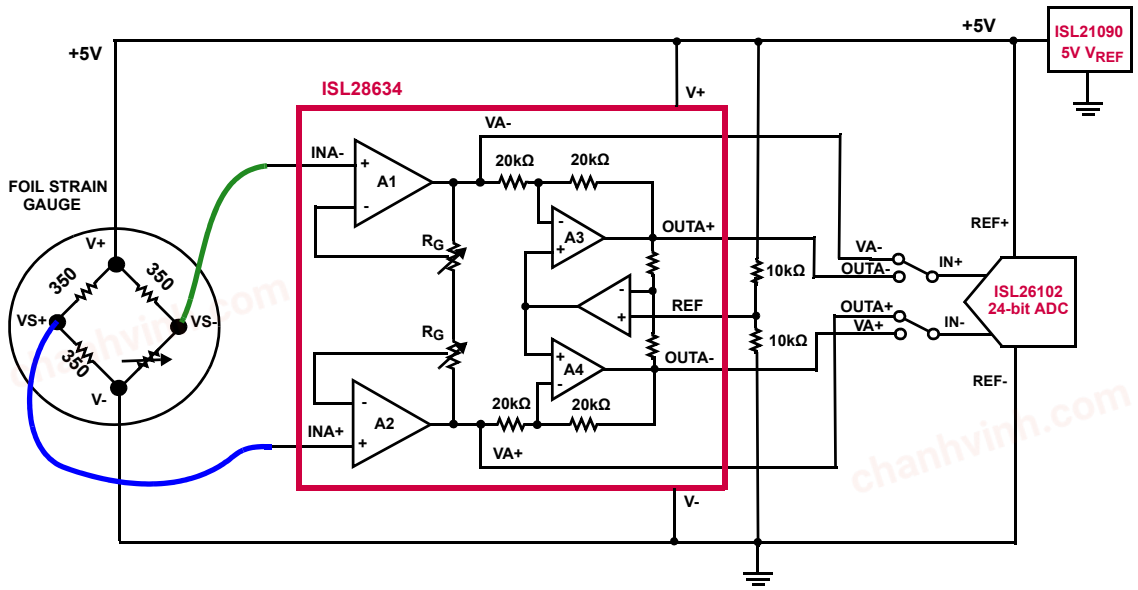


FIGURE 77. APPLICATION CIRCUIT: SENSOR HEALTH MONITOR

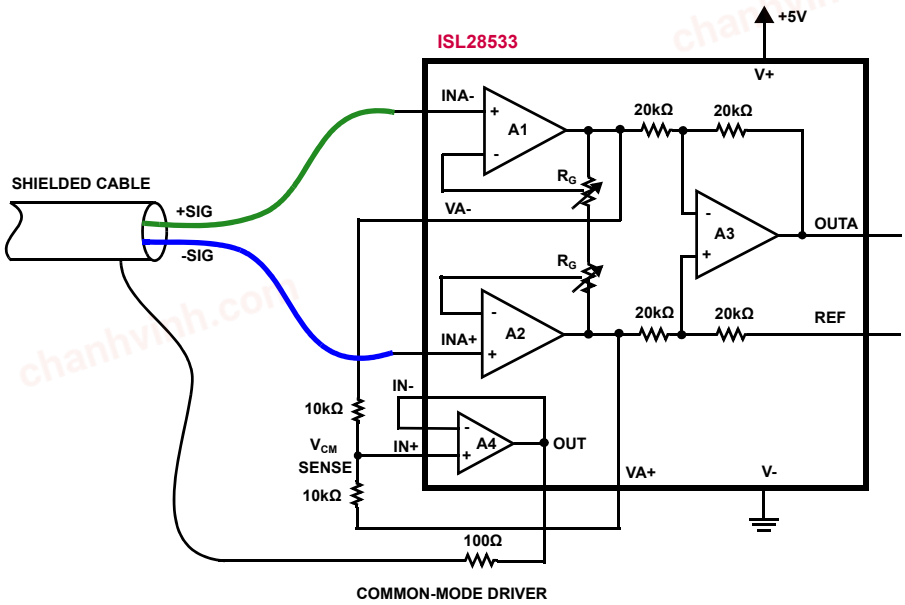


FIGURE 78. APPLICATION CIRCUIT: ACTIVE SHIELD DRIVER

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
January 21, 2016	FN8364.2	Removed DAQ on a stick application note reference from pages 1 and 4. Added Table of differences on page 1. Updated “Ordering Information” on page 5 by adding tape and reel options to note. Updated “About Intersil” verbiage.
November 22, 2013	FN8364.1	Ordering information table on page 5: Removed “coming soon” for ISL28535FVZ and ISL28635FVZ and Evaluation boards.
September 24, 2013	FN8364.0	Initial Release

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Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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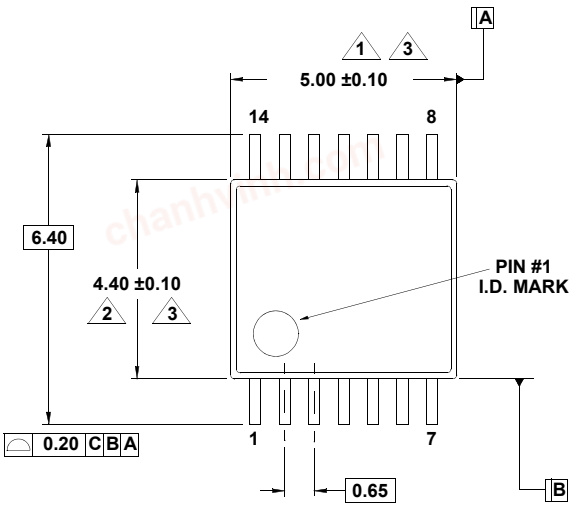
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Package Outline Drawing

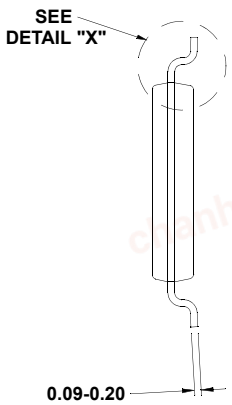
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14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

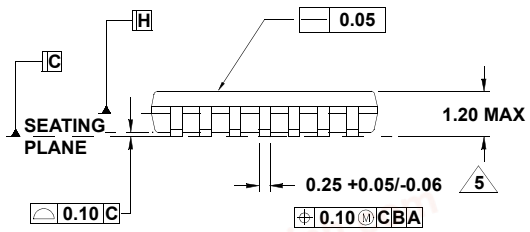
Rev 3, 10/09



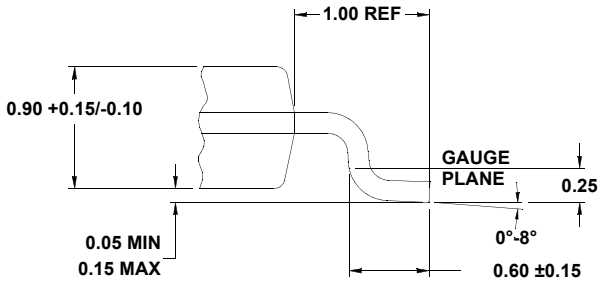
TOP VIEW



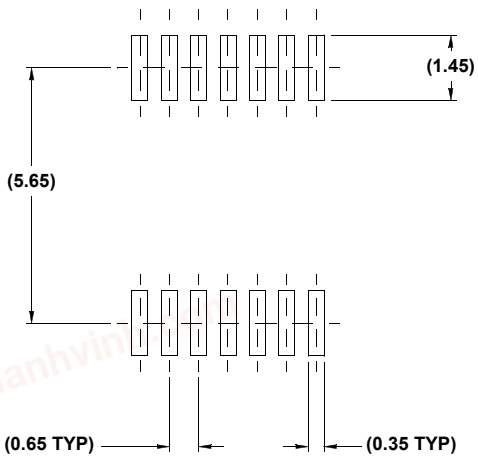
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.