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DATASHEET BEYOND LIMITS INTELLIGENT MEMORY

ECC DRAM

IME(2G/4G/8G)(16/32)L4HA(B/D/Q)
2G/4G/8Gbit LPDDR4 SDRAM with integrated ECC error correction
8 BANKS X 16Mbit X 16 X 1 CHANNEL
8 BANKS X 8Mbit X 16 X 2 CHANNELS
8 BANKS X 32Mbit X 16 X 1 CHANNEL
8 BANKS X 16Mbit X 16 X 2 CHANNELS
8 BANKS X 32Mbit X 16 X 2 CHANNELS

Ordering Speed Code	- 083	- 062
	LPDDR4-2400	LPDDR4-3200
Clock Cycle Time (t_{CK})	0.833ns	0.625ns
System Frequency ($f_{CK\ max}$)	1200 MHz	1600 MHz

Features

- Configuration:
  - x32 for 2-channels per device
  - x16 for 1-channel per device
  - 8 internal banks per each channel
- On-Chip ECC:
  - Integrated SEC-DED (Single Error Correction, Double-Error Detection) logic, which maximizes reliability
  - Hardware ERR signal for each channel, configurable via mode register
  - ECC Register, which controls ECC function
- Low-voltage Core and I/O Power Supplies:
  - V_{DD2} /V_{DDQ} = 1.06-1.17V, V_{DD1} = 1.70-1.95V
- LVSTL(Low Voltage Swing Terminated Logic) I/O Interface
- Internal V_{REF} and V_{REF} Training
- Dynamic ODT :
  - DQ ODT: V_{SSQ} Termination
  - CA ODT: V_{SS} Termination
- Selectable output drive strength (DS)
- Max. Clock Frequency : 1.6GHz (3.2Gbps for one channel)
- 16-bit Pre-fetch DDR data bus
- Single data rate (multiple cycles) command/address bus
- Bidirectional/differential data strobe per byte of data (DQS, $\overline{DQS}$)
- DMI pin support for write data masking and DBI functionality
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL =16, 32)
- Support non-targert DRAM ODT control
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- ZQ Calibration
- On-chip temperature sensor to control self refresh rate
- On-chip temperature sensor whose status can be read from MR4
- 200-ball x16/x32 Discrete Package (Ball Pitch 0.80mm x 0.65mm)
- Operation Temperature range
  - Commercial Tcase = 0°C to +95°C
  - Industrial Tcase = -40°C to +95°C
  - High Temperature Tcase = -40°C to +105°C
  - X-temp and Y-temp of Extreme Temperature Tcase = -40°C to +125°C

*Tc and Ta must not exceed the maximum operating temperature

Option *Marking*

- Configuration
  - 128Mx16 (8 Banks x 16Mbit x16 x1 Channel) 2G16
  - 64Mx32 (8 Banks x 8Mbit x16 x2 Channels) 2G32
  - 256Mx16 (8 Banks x 32Mbit x16 x1 Channel) 4G16
  - 128Mx32 (8 Banks x 16Mbit x16 x2 Channels) 4G32
  - 256Mx32 (8 Banks x 32Mbit x16 x2 Channels) 8G32
- Package
  - 200-ball FBGA (10mm x 14.5mm) for x16/x32 B,D,Q
- Leaded/Lead-free
  - Leaded <blank>
  - Lead-free/RoHS G
- Speed/Cycle Time
  - 0.625ns (LPDDR4-3200) -062
  - 0.833ns (LPDDR4-2400) -083
- Temperature
  - Commercial 0°C to 95°C Tcase <blank>
  - Industrial -40°C to 95°C Tcase I
  - High -40°C to 105°C Tcase H
  - Extreme -40°C to 125°C Tcase X,Y
- Automotive Grade
  - Non-Automotive <blank>
  - Automotive AEC-Q100 A

* In combination with Temperature Grade I = AEC-Q100 Grade 3, H = AEC-Q100 Grade2, X,Y = AEC-Q100 Grade 1

Example Part Number: IME4G32L4HABG-062HA

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Special Features(ECC – Functionality)

- Embedded error correction code (ECC) functionality corrects single bit errors within each 64 bit memory-word.
- The error correction is performed automatically inside the ECC DRAM device.
- Parity data is generated by an internal ECC logic and then stored in additional, dedicated memory space.
- Fully compatible to JEDEC standard DRAM operation and timings.
- JEDEC compliant FBGA package (drop in replacement).

ECC – Functionality / Challenges and Achievements

During the production test, the ECC DRAMs are verified to pass extensive burn-in, core-function and speed tests throughout the complete memory array, including the memory-space for the parity-data. Only when every single memory cell has passed these tests, the ECC function is switched on by hardware and the products get shipped. With the ECC function activated, customers will have unparalleled functionality and quality.

Embedded ECC functionality

Intelligent Memory ECC DRAMs are JEDEC compliant components with integrated error-correction. The internal logic automatically detects and corrects single-bit-errors “on the fly” without any delays or additional latencies compared to conventional DRAM components. ECC DRAMs have additional memory-space to store the ECC-check-bits. Internally, the ECC DRAM works with a 72 bit wide buffer. When writing to the DRAM, an additional 8 ECC check-bits are being generated per each 64 bit data-word. Upon a Read-command, the whole 64+8 bit word is transferred to the buffer and automatically corrected by an ECC Hamming Code (72, 64). The corrected data is then applied to the DQ lines of the ECC DRAM in bit-widths of 4, 8, 16 or 32 bit, depending on the organization of the device.

The ECC algorithm is able to detect and correct one bit-error per 64+8 bit data-word. A 1 Gigabit ECC DRAM component has 16,777,216 data-words of 64 Bits. In each of these data-words, one single-bit error could be corrected, resulting in approximately 16 million times higher reliability of ECC DRAM compared to a conventional DRAM with similar capacity.

Note: If Burst Length x DRAM-I/O-width < 64 bit during a Write-command, the ECC-functionality is limited. Please contact Intelligent Memory for further details.

Comparison to conventional ECC implementation

ECC error correction is very common on high end industrial applications and servers. It normally requires an ECC-capable memory-controller which has an extra-wide data-bus with for example 72 bits (64 data-bits + 8 check-bits). The memory controller generates the required additional check-bits for the data and writes the extra wide data-word to the memory. Upon a Read-command, the memory controller will verify the data-integrity of the data-word + check-bits and performs the correction algorithm. Performing this algorithm affects the systems performance. In addition to the requirement for an ECC-capable memory controller, the conventional way of ECC correction requires multiple DRAMs to be accessed in parallel to achieve the extra-wide bit-width. On Server-memory-modules, for example, 18 DRAM-components with 4 data-lines each are put in parallel to reach the total 72 bit extra-wide data-bus.

With IM ECC DRAM, the check-bit-generation, verification and correction is performed inside the memory device. Every single ECC DRAM performs the error correction by itself, thus it does not require ECC-capable processors/controllers nor any wide data-bus between the controller and the DRAM. Because the ECC DRAM components are JEDEC compliant, they are drop-in replacements to conventional DRAM-memory. Any existing application that is currently built with conventional DRAM can be equipped with error-correction functionality. Note that, if a standard 64 bit memory-module is built using ECC DRAMs, the depth of error-correction is deeper than on 72 bit ECC memory module as each DRAM component on the module performs its own ECC correction-algorithm.

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Why is ECC error correction important?

Numerous analyzes and field-studies have proven DRAM single-bit errors to be the root cause of system-malfunctions or data-corruptions.
According to the field-study by the University Of Toronto called “DRAM Errors In The Wild – A Large-Scale field study”, 25000 to 70000 ECC correctable single-bit errors occur per Megabit of DRAM within 1 billion hours of operation.
While not every single bit error causes a system crash, the application-software may become unstable or important data can be altered and the wrong data can pass through to external media, resulting in unrecoverable data-errors.
While all DRAMs are factory-tested by long burn-in-testing and effective functional and speed testing with different patterns and voltage variations, single-bit errors are technically not avoidable.

The effects are typically transient and difficult-to-repeat single data-bit flips. Many of these single-bit errors appear only under heavy stress or longer time of use of the DRAM, resulting as random system malfunctions or data-corruptions of the application. After a reset, the systems work again until the next occurrence of a single bit error reappears. It is difficult to prove a defect, as it is only a random effect which shows up in different ways at unknown times.

ECC corrects the output, but not the content of the Memory Array. For maximum stability we recommend to do periodical “scrubbing” (read and overwrite)

Possible root-causes for single-bit errors

DRAM cells consist of capacitors holding an electric charge which defines if the memory-cell contains a logical 0 or 1. These capacitor-cells are switched by transistors.

With the trend to smaller process technologies, higher speeds and lower supply-voltages, DRAM memory cells become more sensitive to noise on the signals, electromagnetic fields, cosmic rays or particle radiation. Also power peaks and variations in the signal-timing can cause single-bit errors.

Furthermore, depending on the age and intensity of use of those DRAM components, memory-cells suffer from various degrees of degradation. The isolation of the capacitors gets reduced and leakage increases, leading to lower data-retention-times of some cells. As data-retention times approach the refresh-times, data-bit tend to sometimes show up an incorrect binary value. The effects often appear only with certain data-patterns, at specific temperatures or at high data-traffic to the DRAM. The cell gets “weak”, but the errors in the cell are not easily repeatable as they are not permanent.

There is no way to improve the DRAM technology itself, except by going back to larger processes, lower speeds and higher voltages. Pre-Testing the DRAMs longer, with more stress and wider guardbands, or even with automotive certified screening-processes does not fully protect from the risk of single-bit errors.

The only practical way to avoid single-bit errors is to use error correction algorithms such as ECC.

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1. On-Chip Error Correction Code

I'M LPDDR4 DRAM implement an On-Chip ECC circuit per channel. ECC chunk is 64 bit (SEC-DED Code: Single Error Correction, Double Error Detection) that detects and corrects all single bit error, and detects double bit error , including those introduced by SER events such as cosmic rays, alpha particles, to improve reliability.
ECC is implemented across 64-bit data quantum using 8 ECC parity bits for a total of 72 bits per ECC quantum, to maximize reliability.

Below are key features of ECC Operation.

- Independent 8 ECC parity bits per 64–bits of data (ECC chunk is 64 bits).
- Detect and correct one bit error and detect 2-bit error.
- Programmable ECC ON/OFF function (MR33)
- ERR_A,B Signal ON/OFF, Optional ERR_A, B signals indicate individual ECC event per channel. Each ERR_A,B can be enabled/disabled by setting ERRON bit (MR33)
- ECC Event Counter will store Cumulative ECC Event occurrence (MR34).

LPDDR4 DRAM has Mode Registers per each channel.

- ECC registers are from MR33 toMR34, which are reserved in JEDEC standard LPDDR4/4x as "Do not use".
- ECC features can be set with Mode Register Write Operation on the MR33 register 7
- ECC Event status can be monitored by accessing (Reading out) MR34 to check ECC Event record. Or it can be monitored by optional ERR signal.
- ECC Event type to store is set by OP [1:0] of MR33.

2. ECC Register Information

Table 2.1 Operand vs DQ Mapping Table when accessed by Mode Register

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0

Table 2.2 Mode Register # vs ECC Register # Mapping Table

				MR34	MR33
				ER1	ER0

Table 2.3 MR33 (ER0)

MR#	Access	OP4	OP3	OP2	OP5W	OP1R	OP0R	OP6R/W	OP7R/W
33		Reserved			CLRECC	ERR TYPE		ERRON	ECCON

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MR33 (ER0) is the only register to allow both write and read operation.

- ECCON OP [7]: ECC Circuit ON when OP [7] = 1, OFF when OP [7] = 0.
  - Default : OP [7] is “1”
  - When ECC is disabled (ECCON is “0”), ERR Signal is disabled. ECC functionality disabled.
- ERRON OP [6]: ERR Signal ON when OP [6] = 1, OFF when OP [6] = 0.
  - Default OP [6] is “0”; it means ERR Signal is disabled
  - Note: ERR signal will be Enabled only when both OP [7] and OP [6] are “11”.
  - ERR TYPE OP [1:0]: Set ECC Event type for ERR signal; 1-bit ECC Event, 2-bit ECC Event00: No ECC Event
  - 01: 1-bit ECC Event
  - 10: Reserved
  - 11: 2-bit ECC Event
- CLR ECC OP [5]: ECC Event Record will be Cleared when OP [5] = “1”. Default value for OP [5] is “0”, do not clear event record.
- When a clear ECC operation has completed, OP [5] is returned to “0” automatically.

Table 2.4 MR34 (ER1)

MR#	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
34	R	ECC Event Counter							

- ERROR Counter bits OP [7:0]: Store Cumulative ECC Event Occurrence until clear it with ECC CLR bit in MR33.
  - 8 bits (Max 255 ECC Event) for 1-bit or 2-bit ERROR. More than 255 ECC Event cannot be counted.

3. *OPTIONAL ERR SIGNAL*

ERR_A,B signal indicate ECC event occurrence per each channel.
It is same interface with DQ (1.1V LVSTL). It goes High asynchronous and remains HIGH until being cleared by CLR ECC bit “1” (Sticky bit).

- Enabled by setting ERR ON bit in MR33 OP[6] to “1”.
- ERR_A, B signals stay LOW when ECCON bit MR33 OP[7] is “1” & ERRON bit (OP[6]) is “1”, but no ECC Event occurs.
- ERR_A, B signals stay LOW when is disabled (ECCON bit is “0”, or ERRON bit is “0”).
- Pin location for ERR_A pin is 11A and that for ERR_B is 11AB in 200 BGA, which is NC in JEDEC LPDDR4 pin-out.

ERR Signal

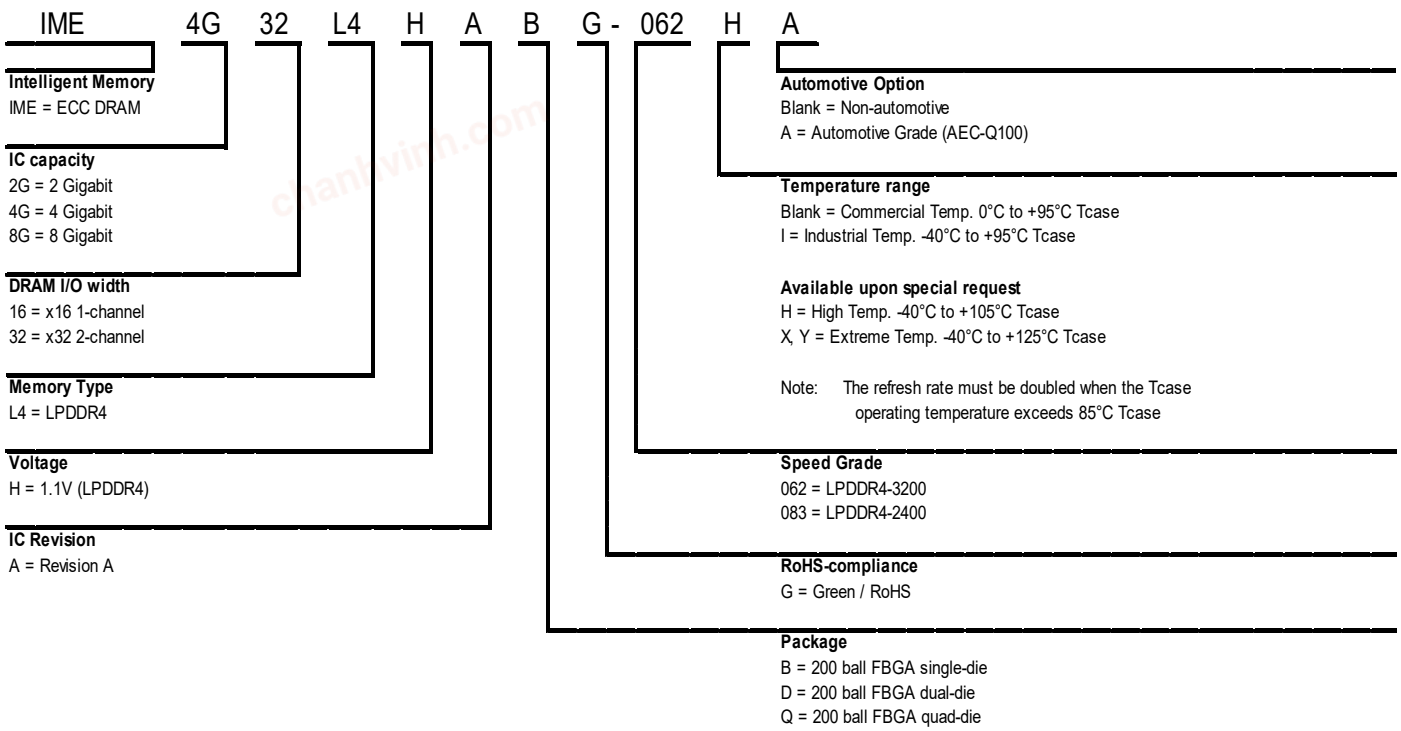
ERR Type	ERR_A,B Signal	Status	Remark
	LOW	No 1-bit Error	
	HIGH	1-bit Error Detected and Corrected or 2-bit Error Detected	Stays High until being cleared by CLR ECC bit.

ERR pin description

SYMBOL	Pin Location	TYPE	DESCRIPTION
ERR_A	11A	OUTPUT	ERR_A,B Signal : Indicates ECC event occurrence per each channel. The same interface with DQ signal.
ERR_B	11AB	OUTPUT	

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Part Number Information



2Gb/4Gb/8Gb LPDDR4 SDRAM Addressing

Memory Density (per Die)		4Gb	4Gb	8Gb	2Gb	2Gb
Die Org.		x32	X16	x32	x32	X16
Number of Channels		2	1	2	2	1
Density per channel		2Gb	4Gb	4Gb	1Gb	2Gb
Configuration		16Mb x 16DQ x 8 banks x 2 channels	32Mb x 16DQ x 8 banks x 1 channel	32Mb x 16DQ x 8 banks x 2 channels	8Mb x 16DQ x 8 banks x 2 channels	16Mb x 16DQ x 8 banks x 1 channel
Number of Banks (per Channel)		8	8	8	8	8
Array Pre-Fetch (Bits, per channel)		256	256	256	256	256
Number of Rows (per channel)		16,384	32,768	32,768	8,192	16,384
Number of Columns (fetch boundaries)		64	64	64	64	64
Page Size (Bytes)		2,048	2,048	2,048	2,048	2,048
Bank Address		BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2
X16	Row Addresses	R0-R13	R0-R14	R0-R14	R0-R12	R0-R13
	Column Addresses	C0-C9	C0-C9	C0-C9	C0-C9	C0-C9
Burst Starting Address Boundary		64-bit	64-bit	64-bit	64-bit	64-bit

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Pin Configurations

200-ball x32 Discrete Package, 0.80mm x 0.65mm using MO-311

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	V_{SS}	V_{DD2}	ZQ0			NC	V_{DD2}	V_{SS}	ERR_A	NC
B	NC	DQ0_A	V_{DDQ}	DQ7_A	V_{DDQ}			V_{DDQ}	DQ15_A	V_{DDQ}	DQ8_A	NC
C	V_{SS}	DQ1 _A	DMI0_A	DQ6_A	V_{SS}			V_{SS}	DQ14_A	DMI1 _A	DQ9_A	V_{SS}
D	V_{DDQ}	V_{SS}	DQS0_T_A	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_T_A	V_{SS}	V_{DDQ}
E	V_{SS}	DQ2_A	DQS0_C_A	DQ5_A	V_{SS}			V_{SS}	DQ13_A	DQS1_C_A	DQ10_A	V_{SS}
F	V_{DD1}	DQ3_A	V_{DDQ}	DQ4_A	V_{DD2}			V_{DD2}	DQ12_A	V_{DDQ}	DQ11 _A	V_{DD1}
G	V_{SS}	ODT_CA_A	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	NC	V_{SS}
H	V_{DD2}	CA0_ A	NC	CS0_A	V_{DD2}			V_{DD2}	CA2 _A	CA3_A	CA4_A	V_{DD2}
J	V_{SS}	CA1_A	V_{SS}	CKE0_A	NC			CK_t_A	CK_ c_A	V_{SS}	CA5_A	V_{SS}
K	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
L												
M												
N	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
P	V_{SS}	CA1_B	V_{SS}	CKE0_B	NC			CK_t_B	CK_c_B	V_{SS}	CA5_B	V_{SS}
R	V_{DD2}	CA0_B	NC	CS0_B	V_{DD2}			V_{DD2}	CA2_B	CA3_B	CA4_B	V_{DD2}
T	V_{SS}	ODT_CA_B	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	RESET_n	V_{SS}
U	V_{DD1}	DQ3_B	V_{DDQ}	DQ4_B	V_{DD2}			V_{DD2}	DQ12_B	V_{DDQ}	DQ11_B	V_{DD1}
V	V_{SS}	DQ2_B	DQS0_C_B	DQ5_B	V_{SS}			V_{SS}	DQ13_B	DQS1_C_B	DQ10_B	V_{SS}
W	V_{DDQ}	V_{SS}	DQS0_T_B	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_T_B	V_{SS}	V_{DDQ}
Y	V_{SS}	DQ1_B	DMI0_B	DQ6_B	V_{SS}			V_{SS}	DQ14_B	DMI1_B	DQ9_B	V_{SS}
AA	NC	DQ0_B	V_{DDQ}	DQ7_B	V_{DDQ}			V_{DDQ}	DQ15_B	V_{DDQ}	DQ8_B	NC
AB	NC	NC	V_{SS}	V_{DD2}	V_{SS}			V_{SS}	V_{DD2}	V_{SS}	ERR_B	NC

Notes:

1. 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows.
2. Top View, A1 in top left corner.
3. ODT_CA_[x] balls are wired to ODT_CA_[x] pads of Rank 0 DRAM die. ODT_CA_[x] pads for other ranks (if present) are disabled in the package.
4. Die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.
5. 11A, 11AB are optional ERR signals.

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Pin Configurations

200-ball x16 Discrete Package, 0.80mm x 0.65mm using MO-311

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	V_{SS}	V_{DD2}	ZQ0			NC	V_{DD2}	V_{SS}	ERR_A	NC
B	NC	DQ0_A	V_{DDQ}	DQ7_A	V_{DDQ}			V_{DDQ}	DQ15_A	V_{DDQ}	DQ8_A	NC
C	V_{SS}	DQ1 _A	DMI0_A	DQ6_A	V_{SS}			V_{SS}	DQ14_A	DMI1 _A	DQ9_A	V_{SS}
D	V_{DDQ}	V_{SS}	DQS0_T_A	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_T_A	V_{SS}	V_{DDQ}
E	V_{SS}	DQ2 _A	DQS0_C_A	DQ5_A	V_{SS}			V_{SS}	DQ13_A	DQS1_C_A	DQ10_A	V_{SS}
F	V_{DD1}	DQ3_A	V_{DDQ}	DQ4_A	V_{DD2}			V_{DD2}	DQ12_A	V_{DDQ}	DQ11 _A	V_{DD1}
G	V_{SS}	ODT_CA_A	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	NC	V_{SS}
H	V_{DD2}	CA0_ A	NC	CS0_A	V_{DD2}			V_{DD2}	CA2 _A	CA3_A	CA4_A	V_{DD2}
J	V_{SS}	CA1 _ A	V_{SS}	CKE0_A	NC			CK_t_A	CK_ c_A	V_{SS}	CA5_A	V_{SS}
K	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
L												
M												
N	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
P	V_{SS}	NC	V_{SS}	NC	NC			NC	NC	V_{SS}	NC	V_{SS}
R	V_{DD2}	NC	NC	NC	V_{DD2}			V_{DD2}	NC	NC	NC	V_{DD2}
T	V_{SS}	NC	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	RESET_n	V_{SS}
U	V_{DD1}	NC	V_{DDQ}	NC	V_{DD2}			V_{DD2}	NC	V_{DDQ}	NC	V_{DD1}
V	V_{SS}	NC	NC	NC	V_{SS}			V_{SS}	NC	NC	NC	V_{SS}
W	V_{DDQ}	V_{SS}	NC	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	NC	V_{SS}	V_{DDQ}
Y	V_{SS}	NC	NC	NC	V_{SS}			V_{SS}	NC	NC	NC	V_{SS}
AA	NC	NC	V_{DDQ}	NC	V_{DDQ}			V_{DDQ}	NC	V_{DDQ}	NC	NC
AB	NC	NC	V_{SS}	V_{DD2}	V_{SS}			V_{SS}	V_{DD2}	V_{SS}	NC	NC

Notes:

6. 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows.
7. Top View, A1 in top left corner.
8. ODT_CA_[x] balls are wired to ODT_CA_[x] pads of Rank 0 DRAM die. ODT_CA_[x] pads for other ranks (if present) are disabled in the package.
9. Die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.
10. 11A is optional ERR signals.

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Signal Pin Description

Pin	Type	Function
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A CKE_B	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A CS_B	Input	**Chip Select:** CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A CA[5:0]_B	Input	**Command/Address Inputs:** CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	**CA ODT Control:** The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_A, DQ[15:0]_B	I/O	**Data Input/Output:** Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	**Data Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function – Data Inversion or Data mask – depends on Mode Register setting.
ZQ	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to V_{DDQ} through a 240Ω ± 1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2}	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
V_{SS}, V_{SSQ}	GND	**Ground Reference:** Power supply ground reference.
RESET_n	Input	**RESET:** When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.

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ECC Register Description

MR33 for ECC control

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ECCON	ERRON	CLR ECC	RFU			ECC 2err	ECC Event

Function	Register Type	Operand	Data
ECCON	READ/WRITE	OP[7]	0: ECC function off 1: ECC function on(default)
ERRON		OP[6]	0: ECC ERR info output through ECC pad function off(default) 1: ECC ERR info output through ECC pad function on
CLR ECC	WRITE only	OP[5]	0: ECC Event Record Clear off(default) 1: ECC Event Record Clear on
ECC 2err	READ only	OP[1]	0: No 2bit err 1: 2bit err detect
ECC Event		OP[0]	0: No ECC event 1: ECC Event detect

Bit “ERRON”(OP6) is valid only if bit “ECCON”(bit7) is valid first.
Bit “CLR ECC”(OP 5) is self clean and will clear both “ECC 2err”(OP 1) and “ECC Event”(OP 0) if it is write with “1”.
Bit “ECC 2err” and “ECC Event” will keep error status valid once set by ECC err information until “CLR ECC” bit sent.

MR34 for ECC error counts

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ECC event Number							

Function	Register Type	Operand	Data
ECC event Number	READ only	OP[7:0]	00000000B: No ECC event detect 00000001B: 1 time ECC event detect 00000010B: 2 times ECC event detect 00000011B: 3 times ECC event detect . . . 11111111B: 255 times ECC event detect

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Refresh Requirement

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self Refresh Exit command, in addition to the normal Refresh command at Trefi interval, the LPDDR4 DRAM requires minimum of one extra Refresh command prior to Self Refresh Entry command.

Refresh Requirement Parameters per die for Dual Channel SDRAM devices

Refresh Requirements		Symbol	2Gb	2Gb	4Gb	4Gb	8Gb	Units	Notes
Density per Channel			**1Gb**	**2Gb**		**4Gb**			
Number of banks per channel			8						
Refresh Window (t_{REFW}) (TCASE ≤ 85°C)		t_{REFW}	32					ms	
Refresh Window (t_{REFW}) (1/2 Rate Refresh)		t_{REFW}	16					ms	
Refresh Window (t_{REFW}) (1/4 Rate Refresh)		t_{REFW}	8					ms	
Required Number of REFRESH Commands in a t_{REFW} window		R	8192					-	
Average Refresh Interval	REFAB	t_{REFI}	3.904					us	
	REFPB	t_{REFIpb}	488					ns	
Refresh Cycle Time (All Banks)		t_{RFCab}	130			180		ns	
Refresh Cycle Time (Per Bank)		t_{RFCpb}	60			90		ns	

Notes:

1. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2. Self refresh abort feature is available for higher density devices starting with 12 Gb device and t_{XSR} — abort(min) is defined as t_{RFCpb} + 17.5ns.

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Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device.
This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Symbol	Parameter	Min	Max	Units	Notes
V_{DD1} supply voltage relative to V_{ss}	V_{DD1}	-0.4	2.1	V	1
V_{DD2} supply voltage relative to V_{ss}	V_{DD2}	-0.4	1.5	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	-0.4	1.5	V	1
Voltage on any ball except V_{DD1} relative to V_{ss}	V_{IN}, V_{OUT}	-0.4	1.5	V	
Storage Temperature	T_{STG}	-55	125	°C	2

Notes:

1. See “Power-Ramp” for relationships between power supplies.
2. Storage Temperature is the case surface temperature on the center/top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2.

Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Notes
Core 1 Power	V_{DD1}	1.70	1.80	1.95	V	1,2
Core 2 Power/Input Buffer Power	V_{DD2}	1.06	1.10	1.17	V	1,2,3
I/O Buffer Power	V_{DDQ}	1.06	1.10	1.17	V	2,3

Notes:

1. V_{DD1} uses significantly less current than V_{DD2}.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. VdIVW and TdIVW limits described elsewhere in this document apply for voltage noise on supply voltages of up to 45 Mv (peak-to-peak) from DC to 20MHz.

Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current	I_L	-4	4	uA	1,2

Notes:

1. For CK__t，CK_c，CKE, CS, CA, ODT_CA and RESET_n. Any input 0V ≤ VIN ≤ VDD2 (All other pins not under test = 0V).
2. CA ODT is disabled for CK_t, CK_c, CS, and CA.

Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output Leakage current	I_{OZ}	-5	5	uA	1,2

Notes:

1. For DQ，DQS_t，DQS_c and DM I. Any I/O 0V ≤ V_{OUT}≤ V_{DDQ}.
2. I/Os status are disabled: High Impedance and ODT Off.

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Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	-25	85	°C
Elevated		85	105	°C
Automotive		105	125	°C

Notes:

1. Operating Temperature is the case surface temperature on the center-top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2.
2. Some applications require operation of LPDDR4 in the maximum temperature conditions in the Elevated Temperature Range between 85 °C and 105 °C case temperature. For LPDDR4 devices, de-rating may be necessary to operate in this range. See MR4.
3. Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Elevated Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

Interface Capacitance

Input/output capacitance

Parameter	Symbol		LPDDR4 1600-3200	Units	Notes
Input capacitance, CK_t and CK_c	CCK	Min	0.5	pF	1,2
		Max	0.9		
Input capacitance delta, CK_t and CK_c	CDCK	Min	0.0	pF	1,2,3
		Max	0.09		
Input capacitance, All other input-only pins	CI	Min	0.5	pF	1,2,4
		Max	0.9		
Input capacitance delta, All other input-only pins	CDI	Min	-0.1	pF	1,2,5
		Max	0.1		
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	CIO	Min	0.7	pF	1,2,6
		Max	1.3		
Input/output capacitance delta, DQS_t,DQS_c	CDDQS	Min	0.0	pF	1,2,7
		Max	0.1		
Input/output capacitance delta, DQ, DMI	CDIO	Min	-0.1	pF	1,2,8
		Max	0.1		
Input/output capacitance, ZQ pin	CZQ	Min	0.0	pF	1,2
		Max	5.0		

Notes:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other pins floating.
3. Absolute value of CCK_ t, CCK_ c.
4. CI applieds to CS_n, CKE, CA0~CA5.
5. CDI = CI – 0.5 * (CCK_t + CCK_c)
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS_t and CDQS_c.
8. CDIO = CIO – 0.5 * (CDQS_t + CDQS_c) in byte-lane.

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Speed Bins

Read and Write Latencies

Read Latency		Write Latency		nWR	nRTP	Lower Clock Frequency Limit [MHz] (>)	Upper Clock Frequency Limit [MHz] (≤)	Notes
No DBI	w/DBI	Set A	Set B					
6	6	4	4	6	8	10	266	1,2,3,4 ,5,6
10	12	6	8	10	8	266	533	
14	16	8	2	16	8	533	800	
20	22	10	18	20	8	800	1066	
24	28	12	22	24	10	1066	1333	
28	32	14	26	30	12	1333	1600	
32	36	16	30	34	14	1600	1866	
36	40	18	34	40	16	1866	2133	

Notes:

1. The LPDDR4 SDRAM device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3 OP[6]. When MR3 OP[6]=0, then the “No DBI” column should be used for Read Latency. When MR3 OP[6]=1, then the “w/DBI” column should be used for Read Latency.
3. Write Latency Set “A” and Set “B” is determined by MR2 OP[6]. When MR2 OP[6]=0, then Write Latency Set “A” should be used. When MR2 OP[6]=1，then Write Latency Set “B” should be used.
4. The programmed value of nWR is the number of clock cycles the LPDDR4 SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (Auto Pre- charge). It is determined by RU(t_{WR}/t_{CK}).
5. The programmed value of nRTP is the number of clock cycles the LPDDR4 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP (Auto Pre- charge). It is determined by RU(t_{RTP}/t_{CK}).
6. Nrtp shown in this table 25 is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a precharge.

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The ODT Mode is enabled if MR11 OP[3:0] are non-zero. In this case, the value of RTT is determined by the settings of those bits.
The ODT Mode is disabled if MR11 OP[3] = 0.

ODTLon and ODTLoff Latency

ODTLon Latency[1]		ODTLoff Latency[2]		Lower Clock Frequency Limit[MHz] (>)	Upper Clock Frequency Limit[Mhz] (≤)
tWPRE = 2tCK					
WL Set "A"	WL Set "B"	WL Set "A"	WL Set "B"		
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	6	N/A	22	533	800
4	12	20	28	800	1066
4	14	22	32	1066	1333
6	18	24	36	1333	1600
6	20	26	40	1600	1866
8	24	28	44	1866	2133

Notes:

1. ODTLon is referenced from CAS-2 command.
2. ODTLoff as shown in table assumes BL=16. For BL32, 8 tCK should be added.

The ODT Mode for non-target DRAM ODT control is enabled if MR11 OP[7,3] is set to a non-zero value.
The ODT Mode for non-target DRAM is disabled if MR11 OP[7,3] = 00B.

ODTLon_rd and ODTLoff_rd Latency Values (MR0 [OP1=0] Normal Latency Support)

ODTLon_rd Latency		ODTLoff_rd Latency[1,2]		Lower Clock Frequency Limit[MHz] (>)	Upper Clock Frequency Limit[MHz] (≤)
No DBI	w/DBI	No DBI	w/ DBI		
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	N/A	N/A	N/A	533	800
14	16	32	34	800	1066
18	22	36	40	1066	1333
22	26	42	46	1333	1600
26	30	46	50	1600	1866
28	32	50	54	1866	2133

Notes:

1. ODTLoff_rd assumes BL=16, For BL32, 8tCK should be added.
2. ODTLoff_rd assumes a fixed Trpst of 1.5tCK

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AC Timing

Clock AC Timing

Parameter	Symbol	LPDDR4-2400		LPDDR4-3200		Units	Notes
		Min	Max	Min	Max		
		Clock Timing					
Average clock period	$t_{CK}(avg)$	0.833	100	0.625	100	ns	
Average High pulse width	$t_{CH}(avg)$	0.46	0.54	0.46	0.54	$t_{CK}(avg)$	
Average Low pulse width	$t_{CL}(avg)$	0.46	0.54	0.46	0.54	$t_{CK}(avg)$	
Absolute clock period	$t_{CK}(abs)$	$t_{CK}(avg)$ MIN + $t_{JIT}(per)$ MIN	-	$t_{CK}(avg)$ MIN + $t_{JIT}(per)$ MIN	-	ns	
Absolute High clock pulse width	$t_{CH}(abs)$	0.43	0.57	0.43	0.57	$t_{CK}(avg)$	
Absolute Low clock pulse width	$t_{CL}(abs)$	0.43	0.57	0.43	0.57	$t_{CK}(avg)$	
Clock period jitter	$t_{JIT}(per)$	-50	50	-40	40	ps	
Maximum Clock Jitter between consecutive cycles	$t_{JIT}(cc)$	-	100	-	80	ps	

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Core AC Timing

Parameter	Symbol	Min/ Max	Data Rate		Unit	Notes
Core Parameters			**2400**	**3200**		
ACTIVATE-to-ACTIVATE command period (same bank)	t_{RC}	MIN	t_{RAS} + t_{RPab} (with all bank precharge) t_{RAS} + t_{RPpb} (with per bank precharge)		ns	
Minimum Self Refresh Time (Entry to Exit)	t_{SR}	MIN	max(15ns, 3nCK)		ns	
Self Refresh exit to next valid command delay	t_{XSR}	MIN	max(t_{RFCab} + 7.5ns, 2nCK)		ns	
Exit Power-Down to next valid command delay	t_{XP}	MIN	max(7.5ns, 5nCK)		ns	
CAS-to-CAS delay	t_{CCD}	MIN	8		t_{CK}(avg)	
Internal READ to PRECHARGE command delay	t_{RTP}	MIN	max(7.5ns, 8nCK)		ns	
RAS-to-CAS delay	t_{RCD}	MIN	max(18ns, 4nCK)		ns	
Row precharge time (single bank)	t_{RPpb}	MIN	m|ax(18ns, 4nCK)		ns	
Row precharge time (all banks)	t_{RPab}	MIN	max(21ns, 4nCK)		ns	
Row active time	t_{RAS}	MIN	max(42ns, 3nCK)		ns	
		MAX	Min(9 * t_{REFI} * Refresh Rate, 70.2) us (Refresh Rate is specified by MR4, OP[2:0])		-	
WRITE recovery time	t_{WR}	MIN	max(18ns, 6nCK)		ns	
WRITE-to-READ delay	t_{WTR}	MIN	max(10ns, 8nCK)		ns	
Active bank-A to active bank-B	t_{RRD}	MIN	max(10ns, 4nCK)		ns	
Precharge to Precharge Delay	t_{PPD}	MIN	4		t_{CK}	1, 2
Four-bank ACTIVATE window	t_{FAW}	MIN	40		ns	

Notes:

1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
2. The value is based on BL16. For BL32 need additional 8 t_{CK}(avg) delay.

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Read output timings (Unit UI = tCK(avg)min/2)

Parameter	Symbol	LPDDR4-2400		LPDDR4-3200		Units	Notes
		Min	Max	Min	Max		
Data Timing							
DQS_t,DQS_c to DQ Skew total, per group, per access (DBI-Disabled)	t_{DQSQ}	-	0.18	-	0.18	UI	
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	t_{QH}	min(t_{QSH}, t_{QSL})	-	min(t_{QSH}, t_{QSL})	-	UI	
DQ output window time total, per pin (DBI-Disabled)	t_{QW_total}	0.73	-	0.7	-	UI	3
DQ output window time deterministic, per pin (DBI-Disabled)	t_{QW_dj}	TBD	-	TBD	-	UI	2,3
DQS_t,DQS_c to DQ Skew total,per group, per access (DBI-Enabled)	t_{DQSQ_DBI}	-	0.18	-	0.18	UI	
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	t_{QH_DBI}	min(t_{QSH_DBI}, t_{QSL_DBI})	-	min(t_{QSH_DBI}, t_{QSL_DBI})	-	UI	
DQ output window time total, per pin (DBI-Enabled)	$t_{QW_total_DBI}$	0.73	-	0.70	-	UI	3
Data Strobe Timing							
DQS, DQS# differential output low time (DBI-Disabled)	t_{QSL}	t_{CL}(abs) -0.05	-	t_{CL}(abs) -0.05	-	t_{CK}(avg)	3,4
DQS, DQS# differential output high time (DBI-Disabled)	t_{QSH}	t_{CH}(abs) -0.05	-	t_{CH}(abs) -0.05	-	t_{CK}(avg)	3,5
DQS, DQS# differential output low time (DBI-Enabled)	t_{QSL_DBI}	t_{CL}(abs) -0.045	-	t_{CL}(abs) -0.045	-	t_{CK}(avg)	4,6
DQS, DQS# differential output high time (DBI-Enabled)	t_{QSH_DBI}	t_{CH}(abs) -0.045	-	t_{CH}(abs) -0.045	-	t_{CK}(avg)	5,6

Notes:

1. The deterministic component of the total timing. Measurement method tbd.
2. This parameter will be characterized and guaranteed by design.
3. This parameter is function of input clock jitter. These values assume the min t_{CH}(abs) and t_{CL}(abs). When the input clock jitter min t_{CH}(abs) and t_{CL}(abs) is 0.44 or greater of t_{CK}(avg) the min value of t_{QSL} will be t_{CL}(abs)-0.04 and t_{QSH} will be t_{CH}(abs) -0.04.
4. t_{QSL} describes the instantaneous differential output low pulse width on DQS_t – DQS_c, as it measured the next rising edge from an arbitrary falling edge.
5. t_{QSH} describes the instantaneous differential output high pulse width on DQS_t – DQS_c, as it measured the next rising edge from an arbitrary falling edge.
6. This parameter is function of input clock jitter. These values assume the min t_{CH}(abs) and t_{CL}(abs). When the input clock jitter min t_{CH}(abs) and t_{CL}(abs) is 0.44 or greater of t_{CK}(avg) the min value of tQSL will be t_{CL}(abs)-0.04 and t_{QSH} will be t_{CH}(abs) -0.04.

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Read AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit	Notes
Read Timing			2400	3200		
READ preamble	t_{RPRE}	Min	1.8		t_{CK}(avg)	
0.5 Tck READ postamble	tRPST	Min	0.4		t_{CK}(avg)	
1.5 Tck READ postamble	t_{RPST}	Min	1.4		t_{CK}(avg)	
DQ low-impedance time from CK_t, CK_c	t_{LZ}(DQ)	Min	(RL x t_{CK}) + t_{DQSCK}(Min) – 200ps		ps	
DQ high impedance time from CK_t, CK_c	t_{HZ}(DQ)	Max	(RL x t_{CK}) + t_{DQSCK}(Max) + t_{DQSQ}(Max) + (BL/2xt_{CK})-100ps		ps	
DQS_c low-impedance time from CK_t, CK_c	t_{LZ}(DQS)	Min	(RL x t_{CK}) + t_{DQSCK}(Min) -(t_{RPRE}(Max) x t_{CK}) – 200ps		ps	
DQS_c high impedance time from CK_t, CK_c	t_{HZ}(DQS)	Max	(RL x t_{CK}) + t_{DQSCK}(Max) +(BL/2 x t_{CK}) + (RPST(Max) x t_{CK}) • 100ps		ps	
DQS-DQ skew	t_{DQSQ}	Max	0.18		UI	

tDQSCK Timing

Parameter	Symbol	Min	Max	Unit	Notes
DQS Output Access Time from CK_t/CK_c	t_{DQSCK}	1.5	3.5	ns	1
DQS Output Access Time from CK_t/CK_c – Temperature Variation	t_{DQSCK_temp}	-	4	ps/°C	2
DQS Output Access Time from CK_t/CK_c – Voltage Variation	t_{DQSCK_volt}	-	7	ps/mV	3
CK to DQS Rank to Rank variation	$t_{DQSCK_rank2rank}$	-	1.0	ns	4,5

Notes:

1. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies> 20 MHz and max voltage of 45 Mv pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
2. t_{DQSCK_temp} max delay variation as a function of Temperature.
3. t_{DQSCK_volt} max delay variation as a function of DC voltage variation for V_{DDQ} and V_{DD2}. t_{DQSCK_volt} should be used to calculate timing variation due to V_{DDQ} and V_{DD2} noise < 20 MHz. Host controller do not need to account for any variation due to V_{DDQ} and V_{DD2} noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{$t_{DQSCKmin}$@V1- $t_{DQSCKmax}$@V2}, abs{$t_{DQSCKmax}$@V1 $t_{DQSCKmin}$@V2}]/abs{V1-V2}. For tester measurement V_{DDQ} = V_{DD2} is assumed.
4. The same voltage and temperature are applied to $t_{DQS2CK_rank2rank}$.
5. $t_{DQSCK_rank2rank}$ parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

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DRAM DQs In Receive Mode (UI = tCK(avg)min/2)

Symbol	Parameter	2400		3200		Unit	Notes
		Min	Max	Min	Max		
VdIVW_total	Rx Mask voltage – p-p total	-	140	-	140	mV	1,2,3,4
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.25	UI	1.2,4
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	UI	1,2,4, 12
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	Mv	5,13
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		UI	6
t_{DQS2DQ}	DQ to DQS offset	200	800	200	800	ps	7
t_{DQ2DQ}	DQ to DQ offset	-	30	-	30	ps	8
t_{DQS2DQ_temp}	DQ to DQS offset temperature variation	-	0.6	-	0.6	ps/°C	9
t_{DQS2DQ_volt}	DQ to DQS offset voltage variation	-	33	-	33	ps/50 Mv	10
SRIN_dIVW	Input Slew Rate over VdIVWJotal	1	7	1	7	V/ns	11
$t_{DQS2DQ_rank2rank}$	DQ to DQS offset rank to rank variation	-	200	-	200	ps	14,15

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20 MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2. The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4. Vcent_DQ must be within the adjustment range of the DQ internal Vref.
5. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.
6. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
7. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
8. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9. TDQS2DQ max delay variation as a function of temperature.
10. TDQS2DQ max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD2}. It includes the V_{DDQ} and V_{DD2} AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement V_{DDQ} = V_{DD2} is assumed.
11. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
12. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
13. VIHL_AC does not have to be met when no transitions are occurring.
14. The same voltage and temperature are applied to $t_{DQS2DQ_rank2rank}$.
15. $t_{DQS2DQ_rank2rank}$ parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

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Write AC Timing

Parameter	Symbol	Min/Max	Data Rate		Unit	Notes
Write Timing			**2400**	**3200**		
Write command to 1st DQS latching	t_{DQSS}	Min	0.75		t_{CK}(avg)	
		Max	1.25			
DQS input high-level	t_{DQSH}	Min	0.4		t_{CK}(avg)	
DQS input low-level width	t_{DQSL}	Min	0.4		t_{CK}(avg)	
DQS falling edge to CK setup time	t_{DSS}	Min	0.2		t_{CK}(avg)	
DQS falling edge hold time from CK	t_{DSH}	Min	0.2		t_{CK}(avg)	
Write preamble	t_{WPRE}	Min	1.8		t_{CK}(avg)	
0.5 t_{CK} Write postamble	t_{WPST}	Min	0.4		t_{CK}(avg)	1
1.5 t_{CK} Write postamble	t_{WPST}	Min	1.4		t_{CK}(avg)	1

Notes:

1. The length of Write Postamble depends on MR3 OP1 setting.

Power-Down AC Timing

Parameter	Symbol	Min/ Max	Data Rate	Unit	Notes
Power Down Timing					
CKE minimum pulse width (HIGH and LOW pulse width)	t_{CKE}	Min	Max(7.5ns, 4nCK)	-	
Delay from valid command to CKE input LOW	t_{CMDCKE}	Min	Max(1.75ns, 3nCK)	ns	1
Valid Clock Requirement after CKE Input low	t_{CKELCK}	Min	Max(5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input Low	t_{CSCKE}	Min	1.75	ns	
Valid CS Requirement after CKE Input low	t_{CKELCS}	Min	Max(5ns, 5nCK)	ns	
Valid Clock Requirement before CKE Input High	t_{CKCKEH}	Min	Max(1.75ns, 3nCK)	ns	1
Exit power- down to next valid command delay	t_{XP}	Min	Max(7.5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input High	t_{CSCKEH}	Min	1.75	ns	
Valid CS Requirement after CKE Input High	t_{CKEHCS}	Min	Max(7.5ns, 5nCK)	ns	
Valid Clock and CS Requirement after CKE Input low after MRW Command	$t_{MRWCKEL}$	Min	Max(14ns, 10nCK)	ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	t_{ZQCKE}	Min	Max(1.75ns, 3nCK)	ns	1

Notes:

1. Delay time has to satisfy both analog time(ns) and clock count(nCK).

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Command Address Input Parameters (UI = Tck(avg)min/2)

Symbol	Parameter	DQ-3200		Unit	Notes
		Min	Max		
VclVW	Rx Mask voltage – p-p	-	155	Mv	1,2,3
TclVW	Rx timing window	-	0.3	UI	1,2,3
VIHL_AC	CA AC input pulse amplitude pk-pk	190	-	Mv	4,7
TclPW	CA input pulse width	0.6		UI	5
SRIN_Civw	Input Slew Rate over VclVW	1	7	V/ns	6

Notes:

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VclVW total(max) must be centered around Vcent_CA(pin mid).
3. Vcent_CA must be within the adjustment range of the CA internal Vref.
4. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VclVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not have to be met when no transitions are occurring.

Mode Register Read/Write AC timing

Parameter	Symbol	Min/ Max	Data Rate	Unit	Notes
Mode Register Read/Write Timing					
Additional time after Txp has expired until MRR command may be issued	t_{MRRI}	Min	t_{RCD} + 3nCK	-	
MODE REGISTER READ command period	t_{MRR}	Min	8	nCK	
MODE REGISTER WRITE command period	t_{MRW}	Min	MAX(10ns, 10nCK)	-	
|Mode register set command delay	t_{MRD}	Min	max(14ns, 10nCK)	-	

Self-Refresh Timing Parameters

Parameter	Symbol	Min/ Max	Data Rate	Unit	Note
Self Refresh Timing					
Delay from SRE command to CKE Input low	t_{ESCKE}	Min	Max(1.75ns, $3t_{CK}$)	ns	1
Minimum Self Refresh Time	t_{SR}	Min	Max(15ns, $3t_{CK}$)	ns	1
Exit Self Refresh to Valid commands	t_{XSR}	Min	Max(t_{RFCab} + 7.5ns, $2t_{CK}$)	ns	1,2

Notes:

1. Delay time has to satisfy both analog time(ns) and clock count(t_{CK}). It means that t_{ESCKE} will not expire until CK has toggled through at least 3 full cycles ($3*t_{CK}$) and 1.75ns has transpired.
2. MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are only allowed during this period.

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Command Bus Training AC Timing

Parameter	Symbol	Min/ Max	Data Rate		Unit	Notes
			2400	3200		
Command Bus Training Timing						
Valid Clock Requirement after CKE Input low	t_{CKELCK}	Min	Max(5ns, 5nCK)		-	
Data Setup for V_{REF} Training Mode	$t_{DStrain}$	Min	2		ns	
Data Hold for V_{REF} Training Mode	$t_{DHtrain}$	Min	2		ns	
Asynchronous Data Read	t_{ADR}	Max	20		ns	
CA Bus Training Command to CA Bus Training Command Delay	t_{CACD}	Min	RU(t_{ADR}/t_{CK})		t_{CK}	2
Valid Strobe Requirement before CKE Low	t_{DQSCKE}	Min	10		ns	1
First CA Bus Training Command Following CKE Low	t_{CAENT}	Min	250		ns	
V_{REF} Step Time -multiple steps	t_{VREFCA_LONG}	Max	250		ns	
V_{ref} Step Time -one step	t_{VREFCA_SHORT}	Max	80		ns	
Valid Clock Requirement before CS High	$t_{CKPRECS}$	Min	$2t_{ck} + t_{XP}$ (t_{XP} = max(7.5ns, 5nCK))		-	
Valid Clock Requirement after CS High	$t_{CKPSTCS}$	Min	max(7.5ns, 5nCK))		-	
Minimum delay from CS to DQS toggle in command bus training	t_{CS_VREF}	Min	2		t_{CK}	
Minimum delay from CKE High to Strobe High Impedance	$t_{CKEHDQS}$		10		ns	
Valid Clock Requirement before CKE input High	t_{CKCKEH}	Min	Max(1.75ns, 3nCK)		-	
CA Bus Training CKE High to DQ Tri-state	t_{MRZ}	Min	1.5		ns	
ODT turn-on Latency from CKE	$tC_{KELODTon}$	Min	20		ns	
ODT tum-off Latency from CKE	$t_{CKELODToff}$	Min	20		ns	
Exit Command Bus Training Mode to next valid command delay	t_{XCBT_Short}	Min	Max(5nCK, 200ns)		-	3
	t_{XCBT_Middle}	Min	Max(5nCK, 200ns)		-	
	t_{XCBT_Long}	Min	Max(5nCK, 250ns)		-	

Notes:

1. DQS_t has to retain a low level during t_{DQSCKE} period, as well as DQS_c has to retain a high level.
2. If t_{CACD} is violated, the data for samples which violate t_{CACD} will not be available, except for the last sample (where t_{CACD} after this sample is met). Valid data for the last sample will be available after t_{ADR}.
3. Exit Command Bus Training Mode to next valid command delay Time depends on value of V_{REF}(CA) setting: MR12 OP[5:0] and V_{REF}(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally exit Command Bus Training Mode to next valid command delay Time may affect V_{REF}(DQ) setting. Settling time of V_{REF}(DQ) level is same as V_{REF}(CA) level.

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Temperature Derating AC Timing

Parameter	Symbol	Min/ Max	Data Rate		Unit	Note
			2400	3200		
Temperature Derating[1]						
DQS output access time from CK_t/CK_c (derated)	t_{DQSCK}	Max	3600		ps	
RAS-to-CAS delay (derated)	t_{RCD}	Min	t_{RCD}+ 1.875		ns	
ACTIVATE-to- ACTIVATE command period (derated)	t_{RC}	Min	t_{RC} + 3.75		ns	
Row active time (derated)	t_{RAS}	Min	t_{RAS} + 1.875		ns	
Row precharge time (derated)	t_{RP}	Min	t_{RP} + 1.875		ns	
Active bank A to active bank B (derated)	t_{RRD}	Min	t_{RRD} + 1.875		ns	

Notes:

1. Timing derating applies for operation at 85 °C to 105 °C.

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I_{DD} Specification

V_{DD2}, V_{DDQ} = 1.06 ~ 1.17V, V_{DD1} = 1.70 ~ 1.95V

Parameter	Supply	4Gbx32	4Gbx16	8Gbx32	2Gbx32	2Gbx16	Units
		3200Mbps					
I_{DD01}	V_{DD1}	18	18	36	18	9	mA
I_{DD02}	V_{DD2}	79	79	158	79	39.5	mA
I_{DD0Q}	V_{DDQ}	0.5	0.5	1	0.5	0.25	mA
I_{DD2P1}	V_{DD1}	1.2	1.2	2.4	1.2	0.6	mA
I_{DD2P2}	V_{DD2}	2.5	2.5	5	2.5	1.25	mA
I_{DD2PQ}	V_{DDQ}	0.3	0.3	0.6	0.3	0.15	mA
I_{DD2PS1}	V_{DD1}	1.2	1.2	2.4	1.2	0.6	mA
I_{DD2PS2}	V_{DD2}	2.5	2.5	5	2.5	1.25	mA
I_{DD2PSQ}	V_{DDQ}	0.3	0.3	0.6	0.3	0.15	mA
I_{DD2N1}	V_{DD1}	1.5	1.5	3	1.5	0.75	mA
I_{DD2N2}	V_{DD2}	35	35	70	35	17.5	mA
I_{DD2NQ}	V_{DDQ}	0.3	0.3	0.6	0.3	0.15	mA
I_{DD2NS1}	V_{DD1}	1.5	1.5	3	1.5	0.75	mA
I_{DD2NS2}	V_{DD2}	25	25	50	25	12.5	mA
I_{DD2NSQ}	V_{DDQ}	0.3	0.3	0.6	0.3	0.15	mA
I_{DD3P1}	V_{DD1}	1.5	1.5	3	1.5	0.75	mA
I_{DD3P2}	V_{DD2}	15	15	30	15	7.5	mA
I_{DD3PQ}	V_{DDQ}	0.3	0.3	0.6	0.3	0.15	mA
I_{DD3PS1}	V_{DD1}	1.5	1.5	3	1.5	0.75	mA
I_{DD3PS2}	V_{DD2}	15	15	30	15	7.5	mA
I_{DD3PSQ}	V_{DDQ}	0.3	0.3	0.6	0.3	0.15	mA
I_{DD3N1}	V_{DD1}	2	2	4	2	1	mA
I_{DD3N2}	V_{DD2}	45	45	90	45	22.5	mA
I_{DD3NQ}	V_{DDQ}	0.5	0.5	1	0.5	0.25	mA
I_{DD3NS1}	V_{DD1}	2	2	4	2	1	mA
I_{DD3NS2}	V_{DD2}	45	45	90	45	15	mA
I_{DD3NSQ}	V_{DDQ}	0.5	0.5	1	0.5	0.25	mA
I_{DD4R1}	V_{DD1}	3	3	4	3	1.5	mA
I_{DD4R2}	V_{DD2}	500	500	600	500	250	mA
I_{DD4RQ}	V_{DDQ}	300	300	360	300	150	mA
I_{DD4W1}	V_{DD1}	3	3	4	3	1.5	mA
I_{DD4W2}	V_{DD1}	400	400	480	400	200	mA
I_{DD4WQ}	V_{DD1}	3	3	4	3	1.5	mA
I_{DD51}	V_{DD1}	50	50	100	50	25	mA
I_{DD52}	V_{DD2}	120	120	240	120	60	mA
I_{DD5Q}	V_{DDQ}	0.5	0.5	1	0.5	0.25	mA
I_{DD5AB1}	V_{DD1}	10	10	20	10	5	mA
I_{DD5AB2}	V_{DD2}	53	53	106	53	26.5	mA
I_{DD5ABQ}	V_{DDQ}	0.5	0.5	1	0.5	0.25	mA
I_{DD5PB1}	V_{DD1}	10	10	20	10	5	mA
I_{DD5PB2}	V_{DD2}	53	53	106	53	26.5	mA
I_{DD5PBQ}	V_{DDQ}	0.5	0.5	1	0.5	0.25	mA

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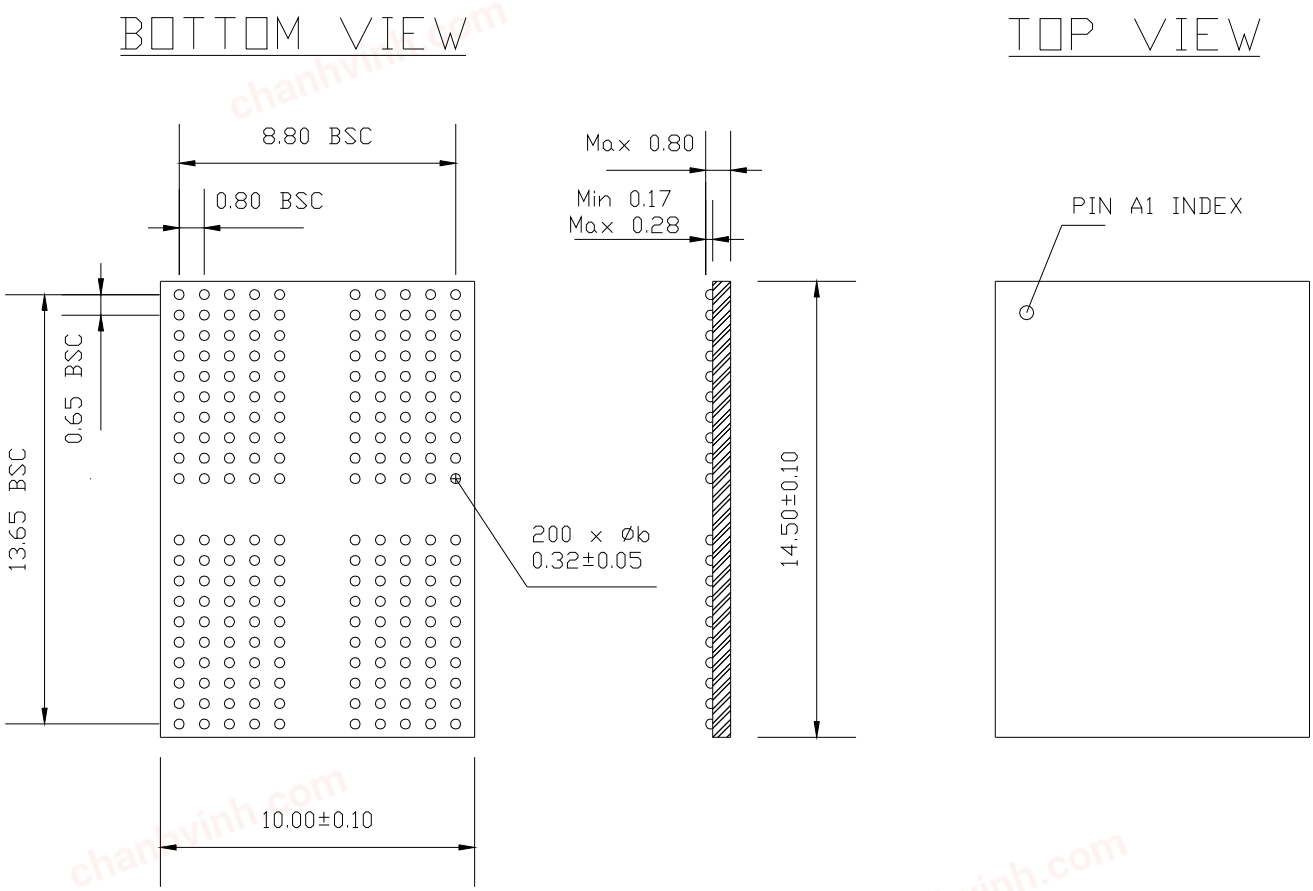
I_{DD6} sepecification

temperature	Parameter	Supply	4Gbx32	4Gbx16	8Gbx32	2Gbx32	2Gbx16	Units
45°C	I_{DD61}	V_{DD1}	2.5	2.5	5	2.5	1.25	mA
	I_{DD62}	V_{DD2}	4	4	8	4	2	mA
	I_{DD6Q}	V_{DDQ}	0.5	0.5	1	0.5	0.25	mA
85°C	I_{DD61}	V_{DD1}	7.5	7.5	14	7.5	4	mA
	I_{DD62}	V_{DD2}	13	13	25	13	7	mA
	I_{DD6Q}	V_{DDQ}	0.5	0.5	1	0.5	0.25	mA

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Package Outlines

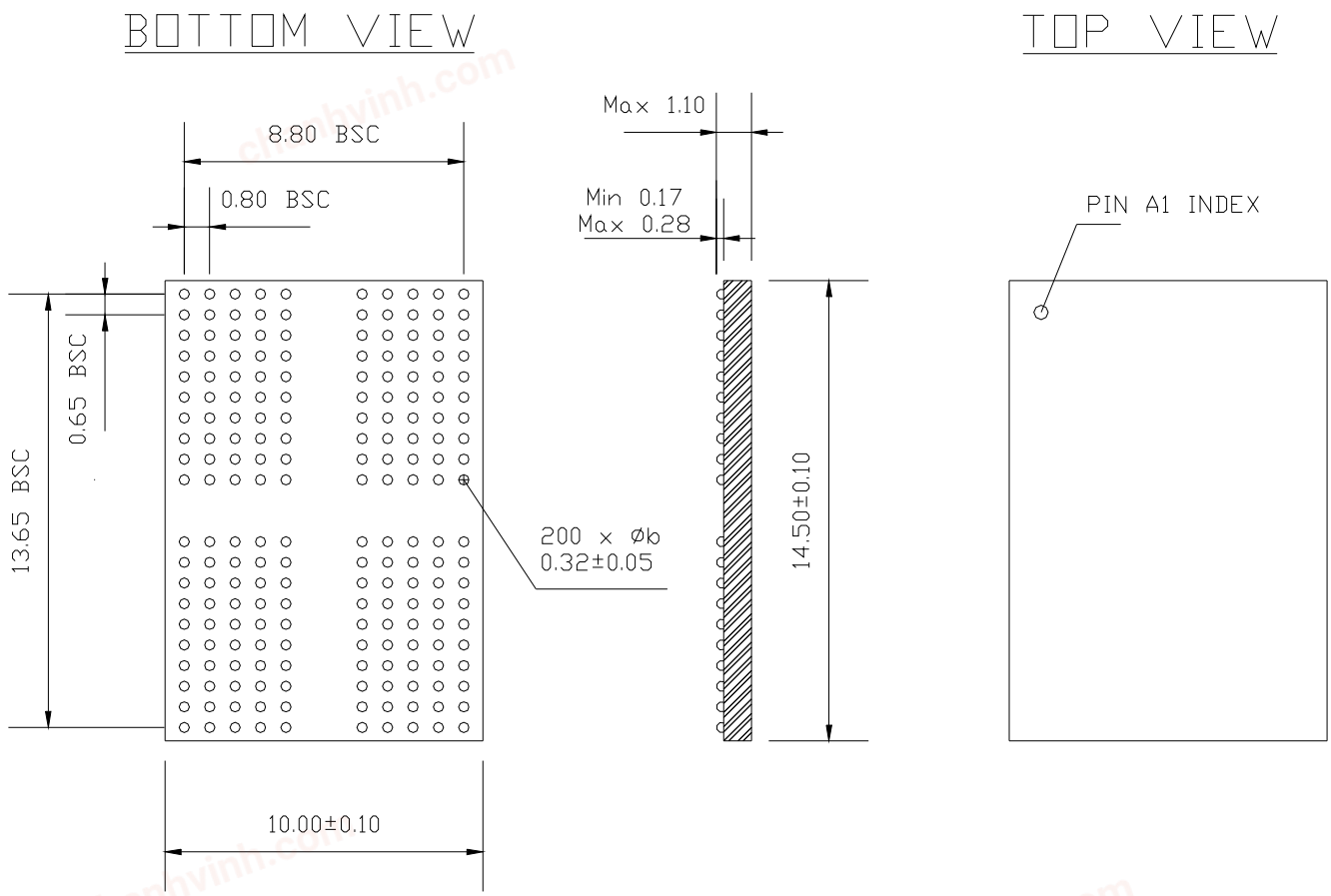
Package outline for 2Gbit abd 4Gbit



NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

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Package outline for 8Gbit



NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

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Revision History

Rev	History	Release Date	Remark
0.1	Initial release	Nov. 2018	
0.2	Add 4Gbx16, 8Gbx32, 2Gbx32, 2Gbx16 products	Aug. 2019	
0.3	1. I_{DD} Specification update 2. Add Automotive A3 and A2 temperature grades 3. Package outline update for IM8G32L4HAB	Oct. 2019	
0.4	Revise the temperature range of Commercial and Industrial Grade	Nov. 2019	
0.5	1. Add High temp. and Extreme temp. (X-temp, Y-temp) 2. Revise Automotive Option 3. Revise Part Number Information 4. Revise Operating Temperature Range 5. Revise IC datasheet format	Nov. 2019	
0.6	1. Revise Part Number Information 2. Revise IC datasheet format	Dec. 2019	
1.0	1. Update I_{DD} Specification 2. Revise IC datasheet format 3. Some typo correction 4. Formal release	Mar. 2020	
2.0	1. Revise the features of On-Chip ECC 2. Add On-Chip Error Correction Code information	Sep. 2020	
2.1	Revise Package Description in Features	Sep. 2021	