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DATASHEET

UNLIMITED INGENUITY

INTELLIGENT MEMORY

Preliminary Product Specification | Rev. 1.1 |

G3 Silver

Embedded Multimedia Card

153 Ball eMMC 5.1 HS400

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1 Product Summary

CAPACITY RANGE	32GB – 256GB
FORM FACTOR	FBGA 153 (11.5x13.0mm, 0.5mm pitch)
INTERFACE	eMMC 5.1 Backward compatible eMMC Specification Ver.4.4, 4.41, 4.5, 5.0
BUS MODE	High-speed eMMC protocol, Clock frequency: 0-200MHz
TRANSFER RATE	Data transfer rate: up to 52Mbyte/s (8 data lines @52 MHz) Single data rate: up to 200Mbyte/s @ 200MHz Dual data rate: up to 400Mbyte/s @ 200MHz
PERFORMANCE	Sequential read: up to 315 MB/s Sequential write: up to 240 MB/s
OPERATION VOLTAGE	VCCQ = 3.3 /1.8 V * VCC = 3.3 V
OPERATING TEMPERATURE	Mobile : -25°C ~ 85°C
STORAGE TEMPERATURE	-40°C ~ 85°C
QUALITY	RoHS compliant **

Note: * refer to detail V_{CCQ} description of each part number in Chapter 2.
** for detailed RoHS declaration, please contact your I'M representative.

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2 Order Information

Table 1 – Part Number

Product Part Number	Density	Operating Voltage	Operation Temperature
IMC1B1A8C2A2A1E3A6A0000	32GB	V_{CC}=3.3V V_{CCQ}=1.8V/3.3V	-25°C ~ 85°C
IMC1B1A8C2A2A1E3A8A0000	64GB		
IMC1B1B1C2A2A1E3B1A0000	128GB		
IMC1B1B3C2A2A1E3B3A0000	256GB		

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3 Product Introduction

I'M eMMC product family provides the ideal embedded storage solution for the Industrial and Medical applications, which require high performance, endurance across a wide range of operating temperatures, and good technical support. I'M eMMC integrates 3D TLC NAND Flash memory and a sophisticated eMMC controller inside a standard package, providing a standard interface to the host. The controller directly manages the NAND flash, implementing functions like bad block management, error handling (ECC), static and dynamic wear-leveling, IOPS optimization and read sensing. I'M eMMC supports Enhanced User Data Area feature which allows the User Data Area of eMMC to be configured as SLC Mode for higher read/write performance, endurance and reliability.

3.1 Device Performance

Table 2 – Read/Write Performance

Device Capacity	Typical value	
	Read Sequential (MB/s)	Write Sequential (MB/s)
32GB	315	215
64GB	315	215
128GB	315	225
256GB	315	240

Notes: 1. Values given for an 8-bit bus width, running HS400 mode from I'M proprietary tool, V_{CC} =3.3V, V_{CCQ} =1.8V.
2. Performance numbers might be subject to changes without notice.

Table 3 – Endurace

Device Capacity	Tera Bytes Written
	Read Sequential (MB/s)
32GB	62
64GB	124
128GB	250
256GB	498

1. TBW values are measured based on Client workload specified according JEDEC standards in JESD219A.
2. Actual lifetime may vary depending on platform and application.

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3.2 User Density and Partition

Table 4 – User Density and Partition

Device Capacity	Partition			
	User Density	Boot 1	Boot 2	RPMB
32GB	31,257,411,584 Bytes	4096 KB	4096 KB	4096 KB
64GB	62,537,072,640 Bytes	4096 KB	4096 KB	4096 KB
128GB	125,074,145,280 Bytes	4096 KB	4096 KB	4096 KB
256GB	250,148,290,560 Bytes	4096 KB	4096 KB	4096 KB
Notes:1. Total user density depends on device type. For example, 52MB in the SLC mode requires 156MB in 3D TLC. This results in decreasing user density.				

3.3 Temperature

Table 5 – Temperature Range

Parameter	Grade	Range	Remark
Operating Temperature	Mobile	-25~+85 °C	
Storage Temperature	All	-40~+85 °C	

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3.4 Power Consumption

Table 6 – Power Consumption

Products	Read (mA)		Write (mA)		Standby (mA)	
Device Capacity	VCCQ(1.8V)	VCC(3.3V)	VCCQ(1.8V)	VCC(3.3V)	VCCQ(1.8V)	VCC(3.3V)
32GB	160	100	85	65	0.15	0.06
64GB	160	100	85	65	0.15	0.06
128GB	160	110	85	105	0.15	0.07
256GB	160	110	85	165	0.15	0.08

Note
1: Values given for an 8-bit bus width, a clock frequency of 200MHz DDR mode, V_{CC} = 3.3V±5%, V_{CCQ} =1.8V±5%
Note 2: Standby current is measured at Vcc=3.3V±5% ,8-bit bus width without frequency.
Note 3: Current numbers might be subject to changes without notice.
Note 4: The measurement for max RMS current is done as average RMS current consumption over a period of 100ms.

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4 eMMC Device and System

4.1 eMMC System Overview

The eMMC specification covers the behavior of the interface and the Device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified. **I'M** eMMC Device consists of a single chip MMC controller and NAND flash memory module. The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

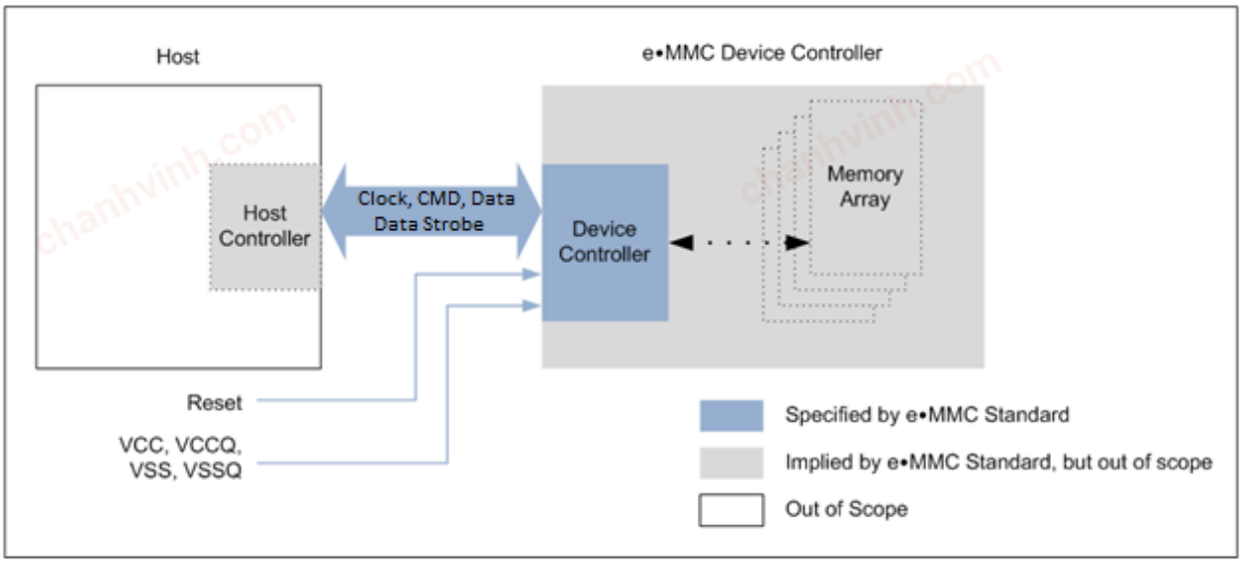


Figure 1 – eMMC System Overview

4.2 Memory Addressing

Previous implementations of the eMMC specification are following byte addressing with 32 bit field. This addressing mechanism permitted for eMMC densities up to and including 2 GB. To support larger densities the addressing mechanism was update to support sector addresses (512 Bytes sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB. To determine the addressing mode use the host should read bit [30:29] in the OCR register.

4.3 eMMC Device Overview

The eMMC device transfers data via a configurable number of data bus signals. The communication signals are:

4.3.1 Clock (CLK)

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Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

4.3.2 Data Strobe(DS)

This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data – one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.

4.3.3 Command (CMD)

This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC host controller to the eMMC Device and responses are sent from the Device to the host.

4.3.4 Input/Outputs (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.

Table 7 – Communication Interface

Name	Type1	Description
CLK	I	Clock
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O

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VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O
DS	O/PP	Data strobe
Notes: 1.I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply.		

Table 8 – eMMC Registers

Name	Width (Bytes)	Description	Implementation
CID	16	Device Identification number, an individual number for identification.	Mandatory
RCA	2	Relative Device Address is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in stan	Mandatory

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry which puts the device into a defined state after the power-on Device.
- A reset signal
- By sending a special command

4.4 Bus Protocol

After a power-on reset, the host must initialize the device by a special message based on eMMC bus protocol. For more details, refer to section 5.3.1 of the JEDEC Standard Specification No.JESD84-B51.

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4.5 Bus Speed Modes

eMMC defines several bus speed modes as shown in Table 8.

Table 9 – Bus Speed Mode

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer (implies x8 bus width)
Backwards Compatibility with legacy MMC card	Single	3.3/1.8V	1, 4, 8	0-26MHz	26MB/s
High speed SDR	Single	3.3/1.8V	4, 8	0-52MHz	52MB/s
High speed DDR	Dual	3.3/1.8V	4, 8	0-52MHz	104MB/s
HS200	Single	1.8V	4, 8	0-200MHz	200MB/s
HS400	Dual	1.8V	8	0-200MHz	400MB/s

4.5.1. HS200 Bus Speed Mode

Figure 2 shows a typical HS200 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For write operations, clock and data direction are the same, write data can be transferred synchronous with CLK, regardless of transmission line delay. For read operations, clock and data direction are opposite; the read data received by Host is delayed by round-trip delay, output delay and latency of Host and Device. For reads, the Host needs to have an adjustable sampling point to reliably receive the incoming data.

The HS200 mode offers the following features:

- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- 8-bits bus width supported
- Single ended signaling with 4 selectable Drive Strength
- Signaling levels of 1.8V
- Tuning concept for Read Operations

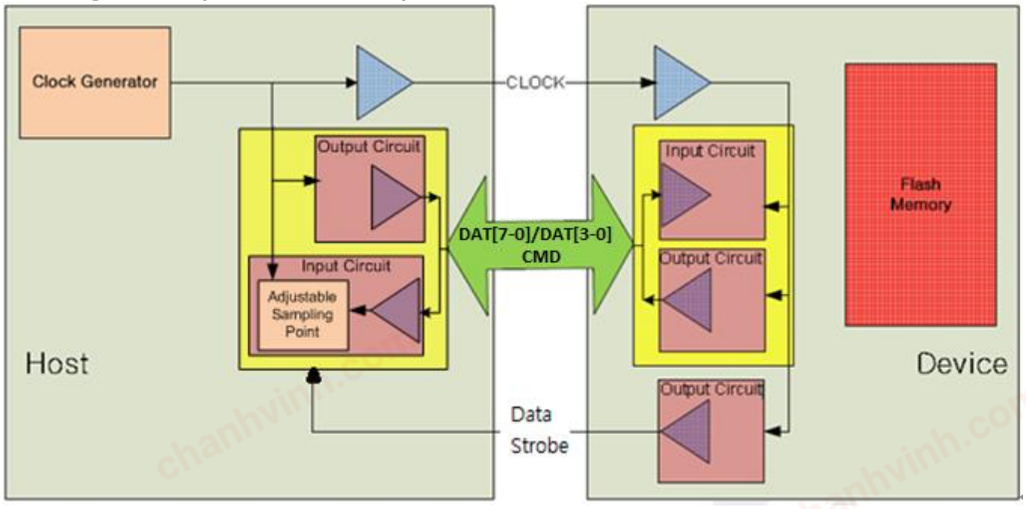


Figure 2 – HS200 Block Diagram

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4.5.2. HS400 Bus Speed Mode

Figure 3 shows a typical HS400 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For read operations, Data Strobe is generated by device output circuit. Host receives the data which is aligned to the edge of Data Strobe.

The HS400 mode offers the following features:

- DDR Data sampling method
- CLK frequency up to 200MHz, Data rate is – up to 400MB/s
- Only 8-bit bus width supported
- Signaling levels of 1.8V
- Support up to 5 selective Drive Strength
- Data strobe signal is toggled only for Data out and CRC response

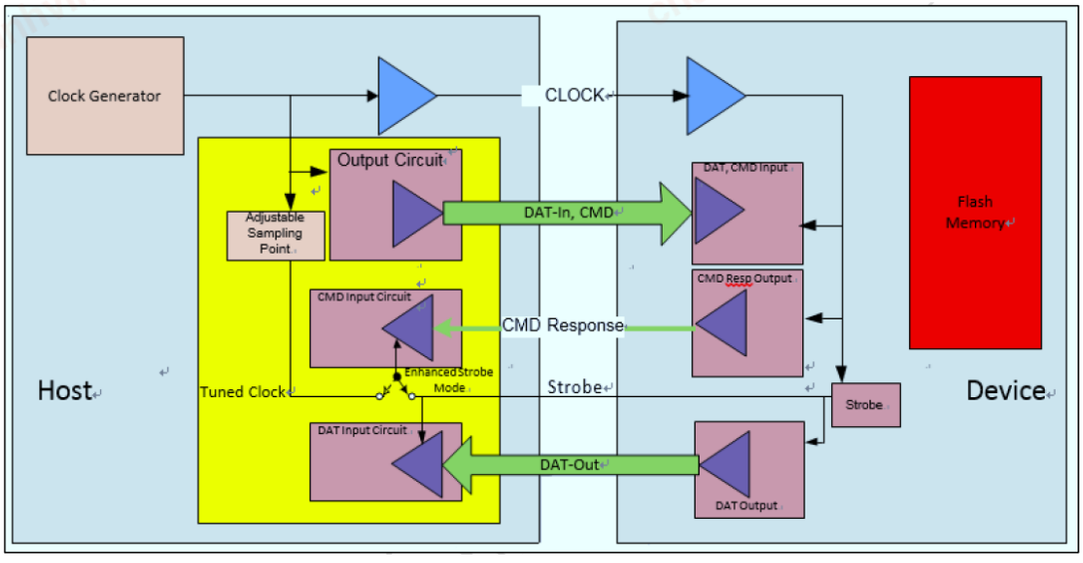


Figure 3 – HS400 Block Diagram

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5 eMMC Function Description

5.1 eMMC Overview

All communication between host and device are controlled by the host (main chip). The host sends a command, which results in a device response. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B51.

Five operation modes are defined for eMMC system:

- Boot operation mode
- Device identification mode
- Interrupt mode
- Data transfer mode
- Inactive mode

5.2 Boot Operation Mode

In boot operation mode, the master (eMMC host) can read boot data from the slave (eMMC device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For more details, refer to section 6.3 of the JEDEC Standard Specification No.JESD84-B51.

5.3 Device Identification Mode

While in device identification mode the host resets the device, validates operation voltage range and access mode, identifies the device and assigns a Relative device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only. For more details, refer to section 6.4 of the JEDEC Standard Specification No.JESD84-B51.

5.4 Interrupt Mode

The interrupt mode on the eMMC system enables the master (eMMC host) to grant the transmission allowance to the slaves (Device) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a Device request for service. Supporting eMMC interrupt mode is an option, both for the host and the Device. For more details, refer to section 6.5 of the JEDEC Standard Specification No.JESD84-B51.

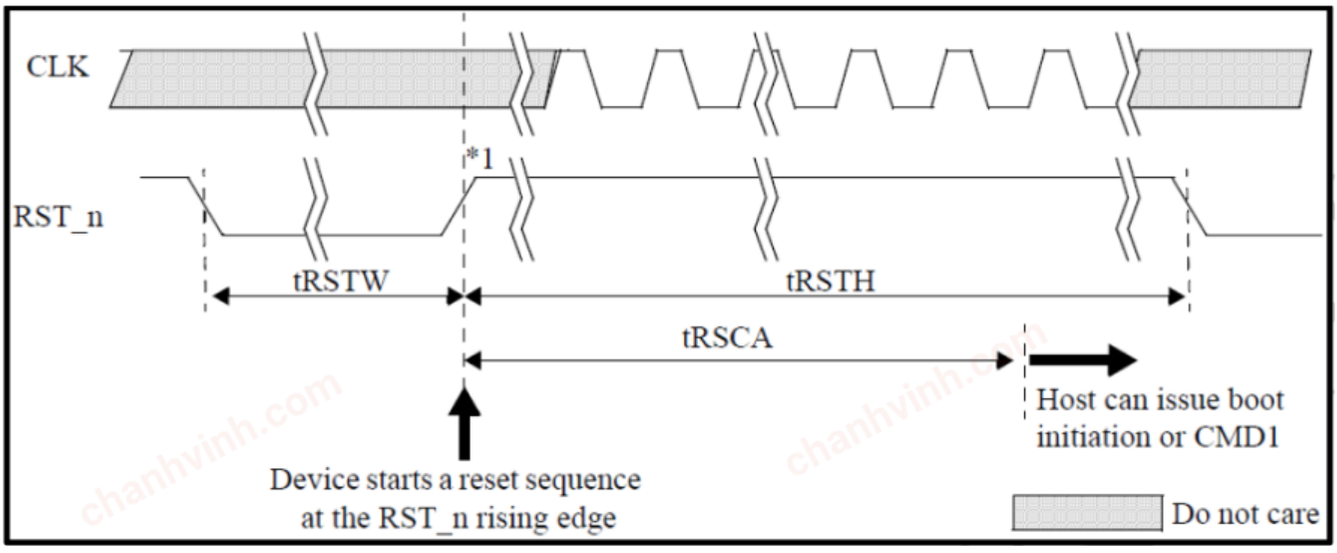
5.5 Data Transfer Mode

When the Device is in Stand-by State, communication over the CMD and DAT lines will be performed in push-pull mode. For more details, refer to section 6.6 of the JEDEC Standard Specification No.JESD84-B51.

5.6 Inactive Mode

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The device will enter inactive mode if either the device operating voltage range or access mode is not valid. The device can also enter inactive mode with GO_INACTIVE_STATE command (CMD15). The device will reset to Pre-idle state with power cycle. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B51.



5.6.1 H/W Reset Operation

Figure 4 – H/W Reset Waveform

Notes: 1. Device will detect the rising edge of RST_n signal to trigger internal reset sequence

Table 10 – H/W Reset Timing Parameters

Symbol	Comment	Min	Max
		Unit(us)	
tRSTW	RST_n pulse width	1	
tRSCA	RST_n to Command time	200[1]	
tRSTH	RST_n high period (interval time)	1	
Notes: 1. 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA			

Noise Filtering Timing for H/W
Device must filter out 5ns or less pulse width for noise immunity
Device must not detect these rising edge.
Device must not detect 5ns or less of positive or negative RST_n pulse.
Device must detect more than or equal to 1us of positive or negative RST_n pulse width.

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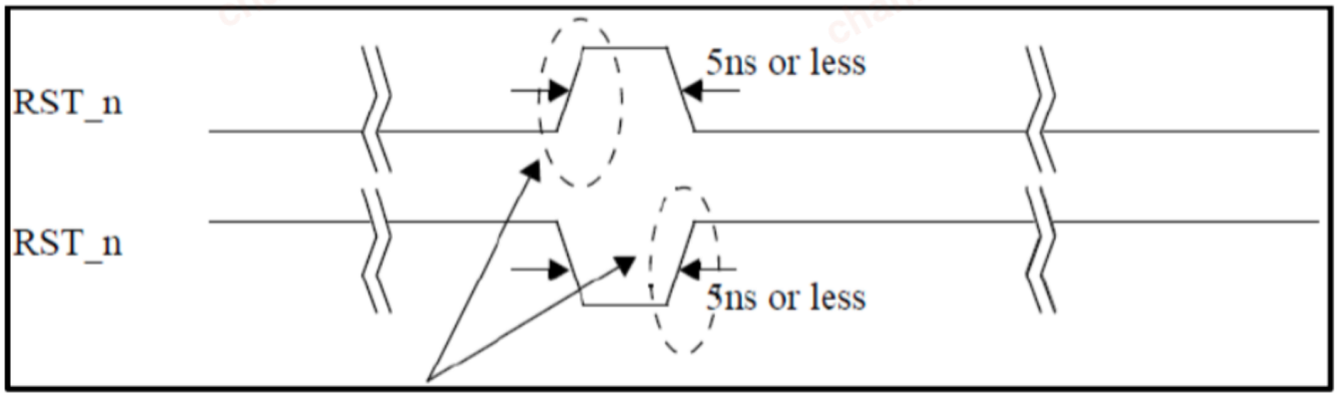


Figure 5 – Noise Filtering Timing for H/W Reset

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5.7 Field Firmware Update(FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism the host downloads a new version of the firmware to the eMMC device and, following a successful download, instructs the eMMC device to install the new downloaded firmware into the device.

In order to start the FFU process the host first checks if the eMMC device supports FFU capabilities by reading SUPPPORTED_MODES and FW_CONFIG fields in the EXT_CSD. If the eMMC device supports the FFU feature the host may start the FFU process. The FFU process starts by switching to FFU Mode in MODE_CONFIG field in the EXT_CSD. In FFU Mode host should use closed-ended or open ended commands for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands to be as defined in FFU_ARG field. In case these commands have a different argument the device behavior is not defined and the FFU process may fail. The host should set Block Length to be DATA_SECTOR_SIZE. Downloaded firmware bundle must be DATA_SECTOR_SIZE size aligned (internal padding of the bundle might be required).Once in FFU Mode the host may send the new firmware bundle to the device using one or more write commands.

The host could regain regular Functionality of write and read commands by setting MODE_CONFIG field in the EXT_CSD back to Normal state. Switching out of FFU Mode may abort the firmware download operation. When host switched back to FFU Mode, the host should check the FFU Status to get indication about the number of sectors which were downloaded successfully by reading the NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED in the extended CSD. In case the number of sectors which were downloaded successfully is zero the host should re-start downloading the new firmware bundle from its first sector. In case the number of sectors which were downloaded successfully is positive the host should continue the download from the next sector, which would resume the firmware download operation.

In case MODE_OPERATION_CODES field is not supported by the device the host sets to NORMAL state and initiates a CMD0/HW_Reset/Power cycle to install the new firmware. In such case the device doesn't need to use NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED. In both cases occurrence of a CMD0/HW_Reset/Power occurred before the host successfully downloaded the new firmware bundle to the device may cause the firmware download process to be aborted.

5.8 Power off Notification for sleep

The host should notify the device before it powers the device off. This allows the device to better prepare itself for being powered off. Power the device off means to turn off all its power supplies. In particular, the host should issue a power off notification (POWER_OFF_LONG, POWER_OFF_SHORT) if it intends to turn off both VCC and VCCQ power I or it may use to a power off notification (SLEEP_NOTIFICATION) if it intends to turn-off VCC after moving the device to Sleep state.

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To indicate to the device that power off notification is supported by the host, a supporting host shall first set the POWER_OFF_NOTIFICATION byte in EXT_CSD [34] to POWERED_ON (0x01). To execute a power off, before powering the device down the host will changes the value to either POWER_OFF_SHORT (0x02) or POWER_OFF_LONG (0x03). Host should waits for the busy line to be de-asserted. Once the setting has changed to either 0x02 or 0x03, host may safely power off the device.

The host may issue SLEEP_AWAKE (CMD5) to enter or to exit from Sleep state if

POWER_OFF_NOTIFICATION byte is set to POWERED_ON. Before moving to Standby state and then to Sleep state, the host sets POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and waits for the DAT0 line de-assertion. While in Sleep (slp) state VCC (Memory supply) may be turned off as defined in 7.1.2 Removing power supplies other than VCC while the device is in the Sleep (slp) state may result in undefined device behavior. Before removing all power supplies, the host should transition the device out of Sleep (slp) state back to Transfer state using CMD5 and CMD7 and then execute a power off notification setting POWER_OFF_NOTIFICATION byte to either POWER_OFF_SHORT or POWER_OFF_LONG.

If host continues to send commands to the device after switching to the power off setting (POWER_OFF_LONG, POWER_OFF_SHORT or SLEEP_NOTIFICATION) or performs HPI during its busy condition, the device shall restore the POWER_OFF_NOTIFICATION byte to POWERED_ON. If host tries to change POWER_OFF_NOTIFICATION to 0x00 after writing another value there, a SWITCH_ERROR is generated.

The difference between the two power-off modes is how urgent the host wants to turn power off. The device should respond to POWER_OFF_SHORT quickly under the generic CMD6 timeout. If more time is acceptable, POWER_OFF_LONG may be used and the device shall respond to it within the POWER_OFF_LONG_TIME timeout.

While POWER_OFF_NOTIFICATION is set to POWERED_ON, the device expects the host to host shall:

- Keep the device power supplies alive (both VCC and VCCQ) and in their active mode
- Not power off the device intentionally before changing POWER_OFF_NOTIFICATION to either POWER_OFF_LONG or POWER_OFF_SHORT
- Not power off VCC intentionally before changing POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and before moving the device to Sleep state

Before moving to Sleep state hosts may set the POWER_OFF_NOTIFICATION byte to SLEEP_NOTIFICATION (0x04) if aware that the device is capable of autonomously initiating background operations for possible performance improvements. Host should wait for the busy line to be de-asserted. Busy line may be asserted up the period defined in SLEEP_NOTIFICATION_TIME byte in EXT_CSD [216]. Once the setting has changed to 0x04 host may set the device into Sleep mode (CMD7+CMD5). After getting out from Sleep the POWER_OFF_NOTIFICATION byte will restore its value to POWERED_ON. HPI may interrupt the

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SLEEP_NOTIFICATION operation. In that case POWER_OFF_NOTIFICATION byte will restore to POWERED_ON.

5.9 Enhanced User Data Area

This eMMC series supports Enhanced User Data Area feature which allows the User Data Area of eMMC to be configured as SLC Mode. Therefore when host set the Enhanced User Data Area, the area will occupy 4 times of original set up size. The Max Enhanced User Data Area size is defined as – (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512 Kbytes). The Enhanced use data area size is defined as – (ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512 Kbytes). The host shall follow the flow chart of JEDEC spec for configuring the parameters of General Purpose Area Partitions and Enhanced User Data Area.

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6 Register Settings

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 6.10 of JESD84-B51).

6.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices. For more details, refer to section 7.1 of the JEDEC Standard Specification No.JESD84-B51.

6.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (eMMC protocol). For details, refer to section 7.2 of JEDEC Standard Specification No.JESD84-B51.

Table 11 – CID Register

Field	Byte	Value
MID	[127:120]	0x9E
Reserved	[119:114]	0x00
CBX	[113:112]	0x01
OID	[111:104]	0x00
PNM	[103:56]	“IM032G” for 32GB, “IM064G” for 64GB, “IM128G” for 128GB, “IM256G” for 256GB,
PRV	[55:48]	0x51
PSN	[47:16]	Random
MDT	[15:8]	month, year
CRC	[7:1]	Follow JEDEC Standard
Reserved	[0:0]	0x01

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6.3 CSD Register

The Card-Specific Data (CSD) register provides information on how to access the contents stored in eMMC. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format...etc. For details, refer to section 7.3 of the JEDEC Standard Specification No.JESD84-B51.

Table 12 – CSD Register

Field	Byte	Value
CSD_Structure	[127:126]	0x03
SPEC_VER	[125:122]	0x04 (V4.0~5.1)
Reserved	[121:120]	0x00
TAAC	[119:112]	0x4F (40ms)
NSAC	[111:104]	0x01
TRAN_SPEED	[103:96]	0x32 (26Mbit/s)
CCC	[95:84]	0x0F5
READ_BL_LEN	[83:80]	0x09 (512 Bytes)
READ_BL_PARTIAL	[79:79]	0x00
WRITE_BLK_MISALIGN	[78:78]	0x00
READ_BLK_MISALIGN	[77:77]	0x00
DSR_IMP	[76:76]	0x00
Reserved	[75:74]	0x00
C_SIZE	[73:62]	0xfff
VDD_R_CURR_MIN	[61:59]	0x07 (100mA)
VDD_R_CURR_MAX	[58:56]	0x07 (200mA)
VDD_W_CURR_MIN	[55:53]	0x07 (100mA)
VDD_W_CURR_MAX	[52:50]	0x07 (200mA)
C_SIZE_MULT	[49:47]	0x07 (512 Bytes)
ERASE_GRP_SIZE	[46:42]	0x1F
ERASE_GRP_MULT	[41:37]	0x1F
WP_GRP_SIZE	[36:32]	0x0F (8GB) 0x1F (16GB) 0x1F (32GB) 0x1F (64GB)
WP_GRP_ENABLE	[31:31]	0x01
DEFAULT_ECC	[30:29]	0x00
R2W_FACTOR	[28:26]	0x02
WRITE_BL_LEN	[25:22]	0x09 (512 Bytes)
WRITE_BL_PARTIAL	[21:21]	0x00
Reserved	[20:17]	0x00
CONTENT_PROT_APP	[16:16]	0x00
FILE_FORMAT_GRP	[15:15]	0x00
COPY	[14:14]	0x00
PERM_WRITE_PROTECT	[13:13]	0x00
TMP_WRITE_PROTECT	[12:12]	0x00
FILE_FORMAT	[11:10]	0x00
ECC	[9:8]	0x00

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CRC	[7:1]	Follow JEDEC Standard
Reserved	[0:0]	0x01

6.4 Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to section 7.4 of the JEDEC Standard Specification No.JESD84-B51.

Table 13 – Extended CSD Register

Field	Byte	Value
Reserved	[511:506]	0
EXT_SECURITY_ERR	[505:505]	0x00
S_CMD_SET	[504:504]	0x01
HPI_FEATURES	[503:503]	0x01
BKOPS_SUPPORT	[502:502]	0x01
MAX_PACKED_READS	[501:501]	0x3C
MAX_PACKED_WRITES	[500:500]	0x20
DATA_TAG_SUPPORT	[499:499]	0x01
TAG_UNIT_SIZE	[498:498]	0x03
TAG_RES_SIZE	[497:497]	0x00
CONTEXT_CAPABILITIES	[496:496]	0x05
LARGE_UNIT_SIZE_M1	[495:495]	tbd
EXT_SUPPORT	[494:494]	0x03
SUPPORTED_MODES	[493:493]	0x01
FFU_FEATURES	[492:492]	0x00
OPERATION_CODE_TIMEOUT	[491:491]	0x00
FFU_ARG	[490:487]	65535
Barrier support	[486:486]	0x01
Reserved	[485:309]	0x00
CMDQ_SUPPORT	[308:308]	0x01
CMQD_DEPTH	[307:307]	0x0F
Reserved	[306:306]	0x00
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	0x00
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	0x00
DEVICE_LIFE_TIME_EST_TYP_B	[269:269]	0x01
DEVICE_LIFE_TIME_EST_TYP_A	[268:268]	0x01
PRE_EOL_INFO	[267:267]	0x01
OPTIMAL_READ_SIZE	[266:266]	0x01
OPTIMAL_WRITE_SIZE	[265:265]	0x08

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OPTIMAL_TRIM_UNIT_SIZE	[264:264]	0x01
DEVICE_VERSION	[263:262]	0x00
FIRMWARE_VERSION	[261:254]	0x01
PWR_CL_DDR_200_360	[253:253]	0x00*
CACHE_SIZE	[252:249]	1024
GENERIC_CMD6_TIME	[248:248]	0x20
POWER_OFF_LONG_TIME	[247:247]	0xFF
BKOPS_STATUS	[246:246]	0x00
CORRECTLY_PRG_SECTORS_NUM	[245:242]	0x00
INI_TIMEOUT_AP	[241:241]	0x64
Reserved	[240:240]	0x01
PWR_CL_DDR_52_360	[239:239]	0x00
PWR_CL_DDR_52_195	[238:238]	0x00
PWR_CL_200_195	[237:237]	0x00
PWR_CL_200_130	[236:236]	0x00
MIN_PERF_DDR_W_8_52	[235:235]	0x00
MIN_PERF_DDR_R_8_52	[234:234]	0x00
Reserved	[233:233]	0x00
TRIM_MULT	[232:232]	0x11: 32/64(GB) 0x22: 128/256(GB)
SEC_FEATURE_SUPPORT	[231:231]	0x55
SEC_ERASE_MULT	[230:230]	0xF7
SEC_TRIM_MULT	[229:229]	0xF7
BOOT_INFO	[228:228]	0x07
Reserved	[227:227]	0x00
BOOT_SIZE_MULT	[226:226]	0x20
ACC_SIZE	[225:225]	tbd
HC_ERASE_GRP_SIZE	[224:224]	0x01
ERASE_TIMEOUT_MULT	[223:223]	tbd
REL_WR_SEC_C	[222:222]	0x01
HC_WP_GRP_SIZE	[221:221]	0x10
S_C_VCC	[220:220]	0x08
S_C_VCCQ	[219:219]	0x08
PRODUCTION_STATE_AWARENESS_TIMEOUT	[218:218]	0x14
S_A_TIMEOUT	[217:217]	0x15
SLEEP_NOTIFICATION_TIME	[216:216]	0x0F
SEC_COUNT	[215:212]	61095936 (32GB) 112,142,720 (64GB) 244,258,440(128GB) 488,570,880(256GB)
Reserved	[211:211]	0x01
MIN_PERF_W_8_52	[210:210]	0x08
MIN_PERF_R_8_52	[209:209]	0x08
MIN_PERF_W_8_26_4_52	[208:208]	0x08
MIN_PERF_R_8_26_4_52	[207:207]	0x08

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MIN_PERF_W_4_26	[206:206]	0x08
MIN_PERF_R_4_26	[205:205]	0x08
Reserved	[204:204]	0x00
PWR_CL_26_360	[203:203]	0x00
PWR_CL_52_360	[202:202]	0x00
PWR_CL_26_195	[201:201]	0x00
PWR_CL_52_195	[200:200]	0x00
PARTITION_SWITCH_TIME	[199:199]	0xFF
OUT_OF_INTERRUPT_TIME	[198:198]	0xFF
DRIVER_STRENGTH	[197:197]	0x1F
DEVICE_TYPE	[196:196]	0x57
Reserved	[195:195]	0x00
CSD_STRUCTURE	[194:194]	0x02
Reserved	[193:193]	0x00
EXT_CSD_REV	[192:192]	0x08
CMD_SET	[191:191]	0x00
Reserved	[190:190]	0x00
CMD_SET_REV	[189:189]	0x00
Reserved	[188:188]	0x00
POWER_CLASS	[187:187]	0x00
Reserved	[186:186]	0x00
HS_TIMING	[185:185]	0x01
Strobe Support	[184:184]	0x01
BUS_WIDTH	[183:183]	0x02
Reserved	[182:182]	0x00
ERASED_MEM_CONT	[181:181]	0x00
Reserved	[180:180]	0x00
PARTITION_CONFIG	[179:179]	0x00
BOOT_CONFIG_PROT	[178:178]	0x00
BOOT_BUS_CONDITIONS	[177:177]	0x00
Reserved	[176:176]	0x00
ERASE_GROUP_DEF	[175:175]	0x00
BOOT_WP_STATUS	[174:174]	0x00
BOOT_WP	[173:173]	0x00
Reserved	[172:172]	0x00
USER_WP	[171:171]	0x00
Reserved	[170:170]	0x00
FW_CONFIG	[169:169]	0x00
RPMB_SIZE_MULT	[168:168]	0x20
WR_REL_SET	[167:167]	0x00
WR_REL_PARAM	[166:166]	0x15
SANITIZE_START	[165:165]	0x00
BKOPS_START	[164:164]	0x00
BKOPS_EN	[163:163]	0x00
RST_n_FUNCTION	[162:162]	0x00
HPI_MGMT	[161:161]	0x00

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PARTITIONING_SUPPORT	[160:160]	0x07
MAX_ENH_SIZE_MULT	[159:157]	tbd
PARTITIONS_ATTRIBUTE	[156:156]	0x00
PARTITION_SETTING_COMPLETED	[155:155]	0x00
GP_SIZE_MULT_4	[154:152]	0x00
GP_SIZE_MULT_3	[151:149]	0x00
GP_SIZE_MULT_2	[148:146]	0x00
GP_SIZE_MULT_1	[145:143]	0x00
ENH_SIZE_MULT	[142:140]	0x00
ENH_START_ADDR	[139:136]	0x00
Reserved	[135:135]	0x00
SEC_BAD_BLK_MGMNT	[134:134]	0x00
PRODUCTION_STATE_AWARENESS	[133:133]	0x00
TCASE_SUPPORT	[132:132]	0x00
PERIODIC_WAKEUP	[131:131]	0x00
PROGRAM *CIDCSDDDR*SUPPORT	[130:130]	0x01
Reserved	[129:128]	0x00
VENDOR_SPECIFIC_FIELD	[127:67]	-
ERROR_CODE	[66:65]	0x00
ERROR_TYPE	[64:64]	0x00
NATIVE_SECTOR_SIZE	[63:63]	0x00
USE_NATIVE_SECTOR	[62:62]	0x00
DATA_SECTOR_SIZE	[61:61]	0x00
INI_TIMEOUT_EMU	[60:60]	0x00
CLASS_6_CTRL	[59:59]	0x00
DYNCAP_NEEDED	[58:58]	0x00
EXCEPTION_EVENTS_CTRL	[57:56]	0x00
EXCEPTION_EVENTS_STATUS	[55:54]	0x00
EXT_PARTITIONS_ATTRIBUTE	[53:52]	0x00
CONTEXT_CONF	[51:37]	0x00
PACKED_COMMAND_STATUS	[36:36]	0x00
PACKED_FAILURE_INDEX	[35:35]	0x00
POWER_OFF_NOTIFICATION	[34:34]	0x00
CACHE_CTRL	[33:33]	0x00
FLUSH_CACHE	[32:32]	0x00
Reserved	[31:31]	0x00
MODE_CONFIG	[30:30]	0x00
MODE_OPERATION_CODES	[29:29]	0x00
Reserved	[28:27]	0x00
FFU_STATUS	[26:26]	0x00
PRE_LOADING_DATA_SIZE	[25:22]	0x00
MAX_PRE_LOADING_DATA_SIZE	[21:18]	tbd
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17:17]	0x01
SECURE_REMOVAL_TYPE	[16:16]	0x01
Reserved	[15:0]	0

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6.5 RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the Stand-by State with CMD7.

6.6 DSR Register

The 16-bit driver stage register (DSR) is described in detail in Section 10.2 of the JEDEC Standard Specification No.JESD84-B51. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage.

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7 The eMMC bus

The eMMC bus has ten communication lines and three supply lines:

- CMD： Command is a bidirectional signal. The host and Device drivers are operating in two
  modes, open drain and push/pull.
- DAT0-7： Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode
- CLK： Clock is a host to Device signal. CLK operates in push-pull mode
- Data Strobe: Data Strobe is a Device to host signal. Data Strobe operates in push-pull mode.

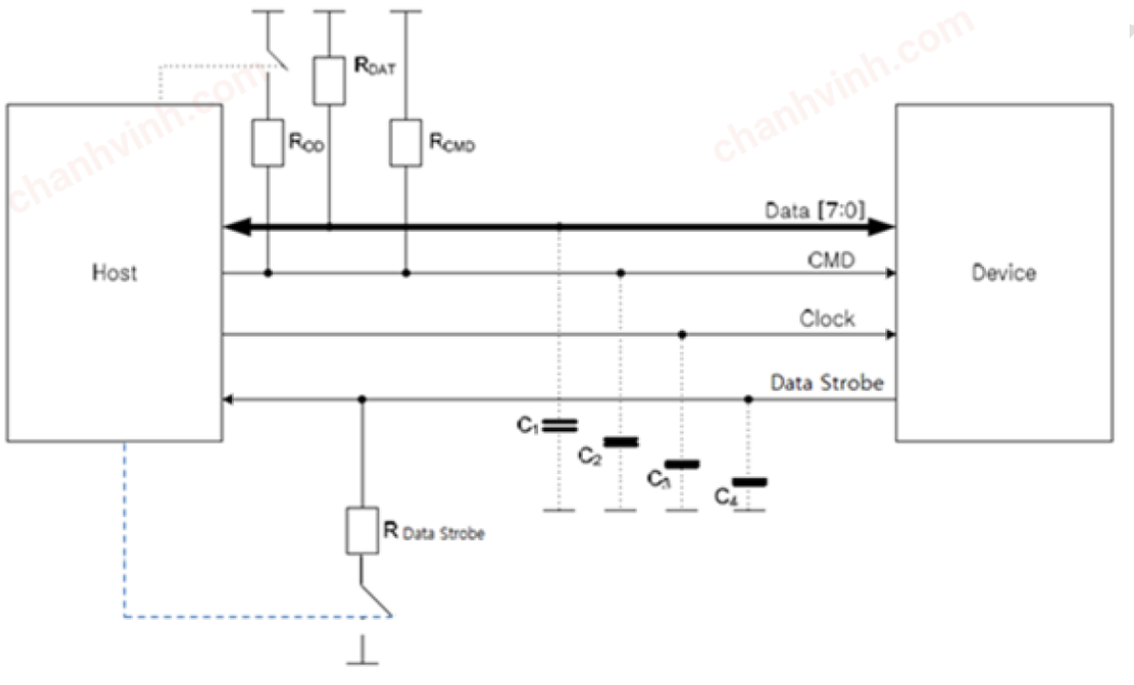


Figure 6 – Bus Circuitry Diagram

The ROD is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the ROD. RDAT and RCMD are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.

A constant current source can replace the ROD by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable ROD implementation, a fixed RCMD can be used).Consequently the maximum operating frequency in the open drain mode has to be reduced if the used RCMD value is higher than the minimal one given in.

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$R_{data\ strobe}$ is pull-down resistor used in HS400 device.

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7.1 Power-up

7.1.1 eMMC power-up

An eMMC bus power-up is handled locally in each device and in the bus master. Figure7 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification No.JESD84-B51 for specific instructions regarding the power-up sequence.

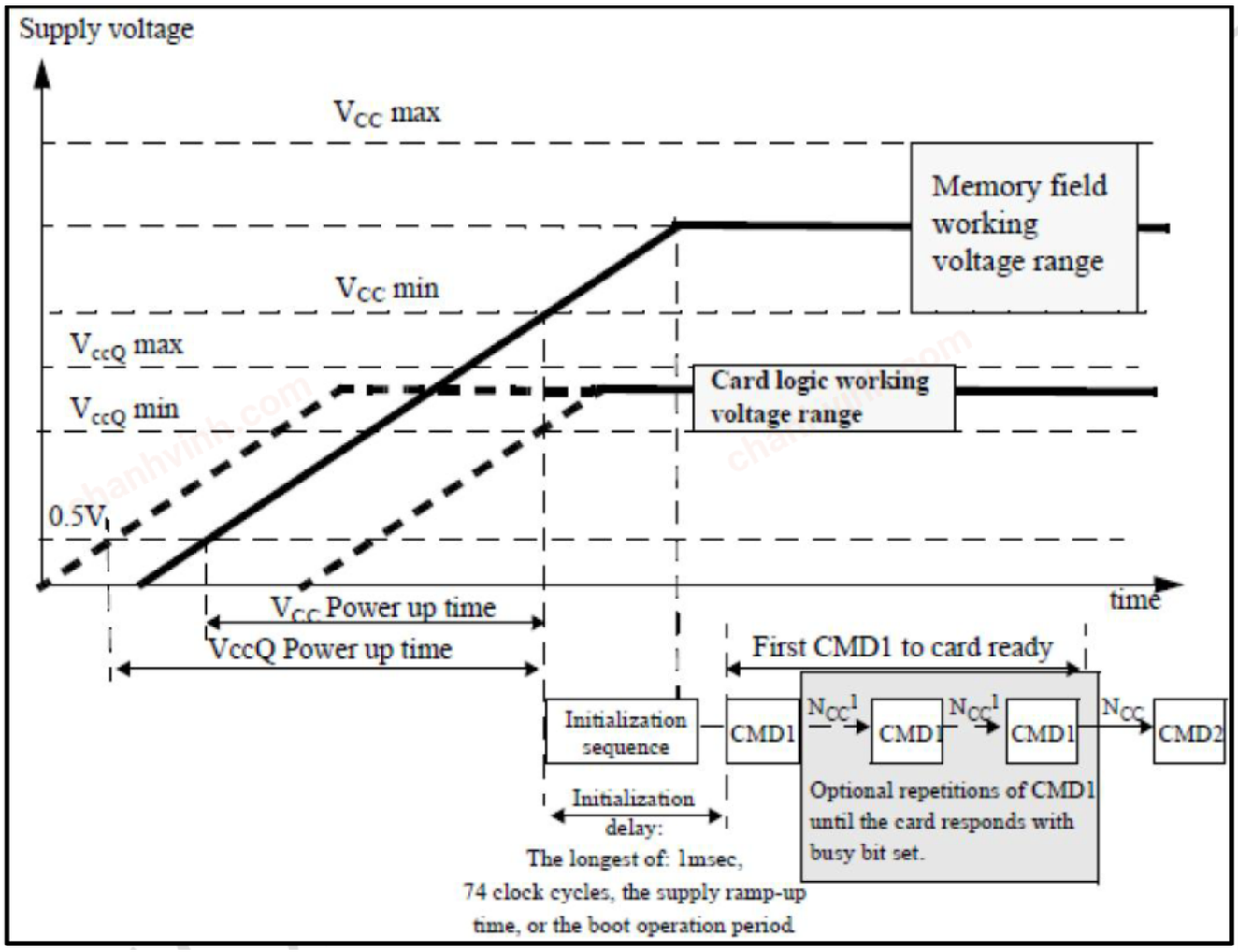
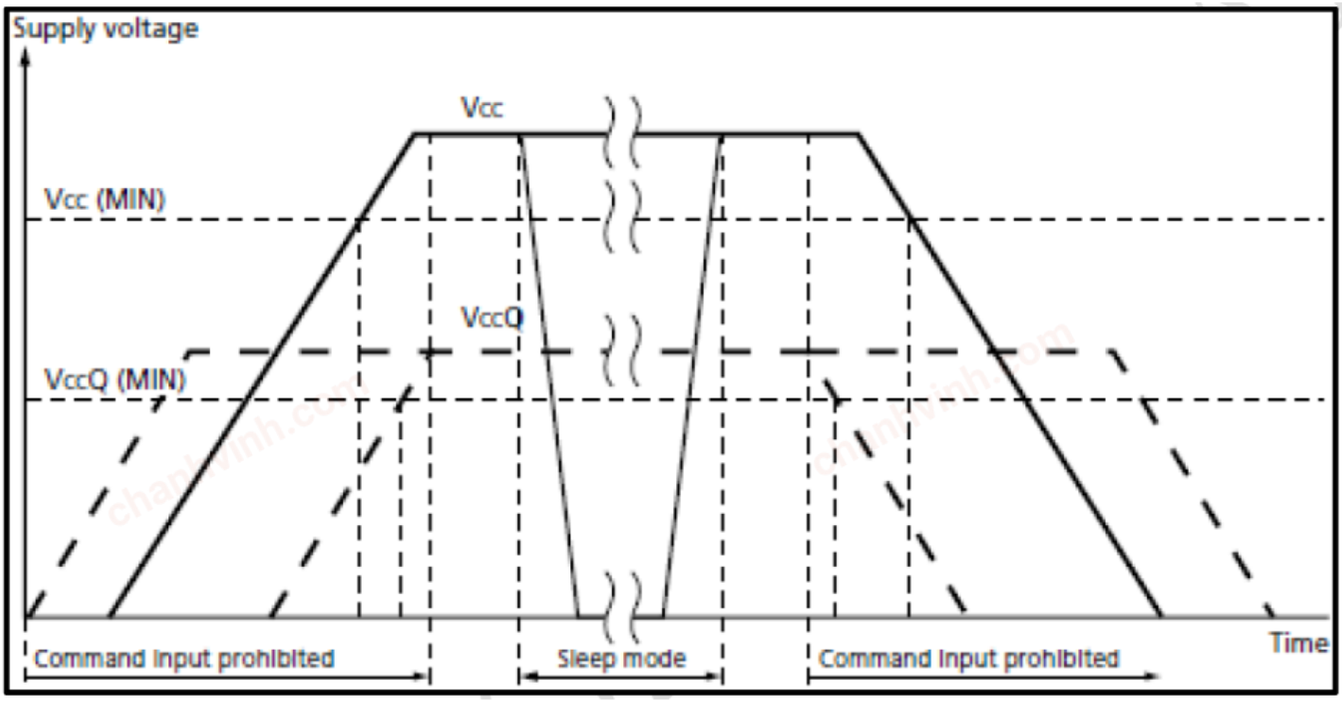


Figure 7 – eMMC Power-up Diagram

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7.1.2 eMMC Power Cycling

The master can execute any sequence of VCC and VCCQ power-up/power-down. However, the master must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down VCC to reduce power consumption. It is necessary for the slave to be ramped up to VCC before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling see



Section 10.1.3 of the JEDEC Standard Specification No.JESD84-B51.

Figure 8 – The eMMC Power Cycle

7.2 Bus Operating Conditions

Table 14 – General Operating Conditions

Parameter	Symbol	Min	Max.	Unit
Peak voltage on all lines		-0.5	VCCQ +0.5	V
All Inputs				
Input Leakage Current (before initialization sequence [1] and/or the internal pull up resistors connected)		-100	100	µA
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)		-2	2	µA
All Outputs				
Output Leakage Current (before initialization sequence)		-100	100	µA

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Output Leakage Current (after initialization sequence) [2]		-2	2	µA
Notes: 1. Initialization sequence is defined in section 10.1 2. DS (Data strobe) pin is excluded.				

7.2.1 Power supply: eMMC

In the eMMC, VCC is used for the NAND flash device and its interface voltage; VCCQ is for the controller and the MMC interface voltage as shown in Figure 8. The core regulator is optional and only required when internal core logic voltage is regulated from VCCQ. A Creg capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

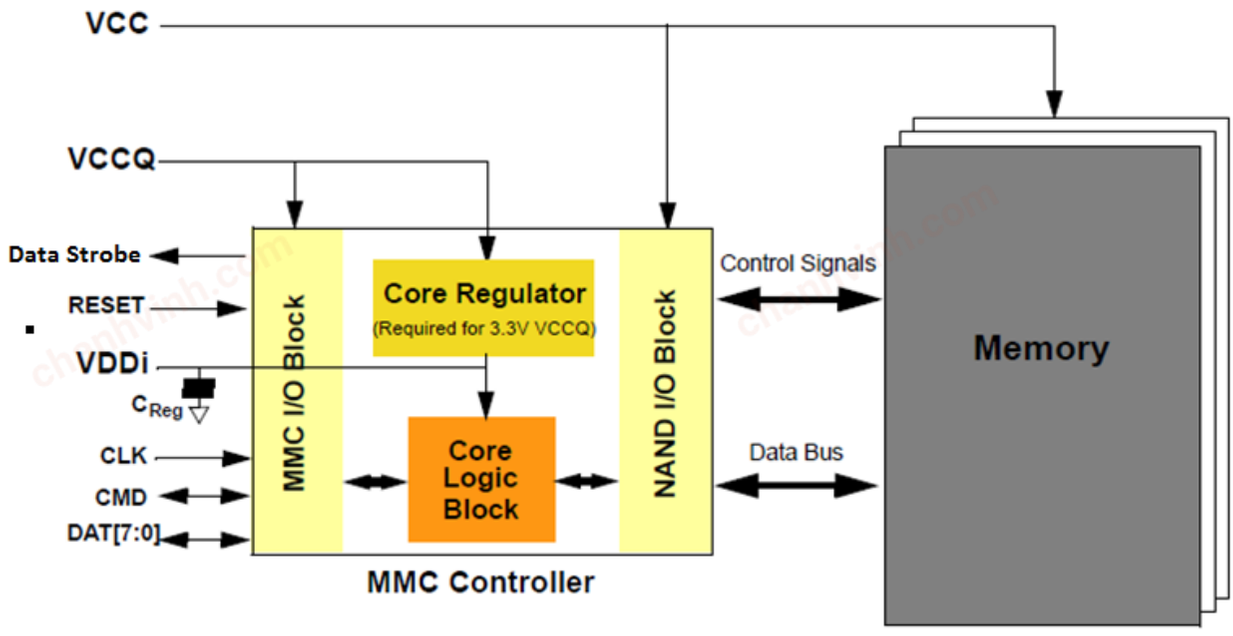


Figure 9 – eMMC Internal Power Diagram

7.2.2 eMMC Power Supply Voltages

The eMMC supports one or more combinations of V_{CC} and V_{CCQ} as shown in Table 8. The V_{CCQ} must be defined at equal to or less than V_{CC}.

Table 15 – eMMC Operating Voltage

Parameter	Symbol	MIN	MAX	Unit
Supply voltage (NAND)	V_{CC}	2.7	3.6	V
Supply voltage (I/O)	V_{CCQ}	2.7	3.6	V
		1.7	1.95	V
Supply power-up for 3.3V	t_{PRUH}		35	ms
Supply power-up for 1.8V	t_{PRUL}		25	ms

The eMMC must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations (see Table15).

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Table 16 – eMMC Voltage Combinations

		V_{CCQ}	
		1.7V–1.95V	2.7V–3.6V[1]
Vcc	2.7V-3.6V	Valid	Valid
Notes: 1. CCQ (I/O) 3.3 volt range is not supported in HS200 /HS400 devices			

7.2.3 Bus Signal Line Load

The total capacitance C_L of each line of the eMMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of eMMC connected to this line:

- $C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$

The sum of the host and bus capacitances must be under 20pF.

Table 17 – Signal Line Load

Parameter	Symbol	Min	Max	Typ	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	50	10	Kohm	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10	50	10	Kohm	to prevent bus floating
Pull-up resistance for RST_n	R_{RST_n}	4.7	50	10	Kohm	It is not necessary to put pull-up resistance on RST_n (H/W rest) line if host does not use H/W reset. (Extended CSD register [162] = 0 b)
Bus signal line capacitance	C_L		30	30	pF	Single Device
Single Device capacitance	C_{DEVICE}		6	6	pF	
Maximum signal line inductance			16	16	nH	
Impedance on CLK / CMD / DAT0~7		45	55	50	ohm	Impedance match
Serial's resistance on CLK line	SR_{CLK}	0	47	0	ohm	

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Serial's resistance on CMD / DAT0~7 line	SR_{CMD} $SR_{DAT0\sim7}$	0	47	0	ohm	
V_{CCQ} decoupling capacitor		2.2+0.1	10+0.22	2.2+0.1	µF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
	CH1	1	2.2	1	µF	CH1 is only for HS200. It should be placed adjacent to VCCQ-VSSQ balls (#K6 and #K4 accordingly, next to DAT [7..0] balls). It should be located as close as possible to the balls defined in order to minimize connection parasitic.
V_{CC} capacitor value		2.2+0.1	10+0.22	4.7+0.1	µF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
V_{Ddi} capacitor value		1+0.1	2.2+0.1	1+0.1	µF	To stabilize regulator output to controller core logics. It should be located as close as possible to the balls defined in order to minimize connection parasitic

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7.2.4 Bus Signal Line Load

The circuit in Figure 10 shows the reference load used to define the HS400 Device Output Timings and overshoot / undershoot parameters. The reference load is made up by the transmission line and the CREFERENCE capacitance.

The reference load is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the reference load to system environment. Manufacturers should correlate to their production test conditions. Delay time (td) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

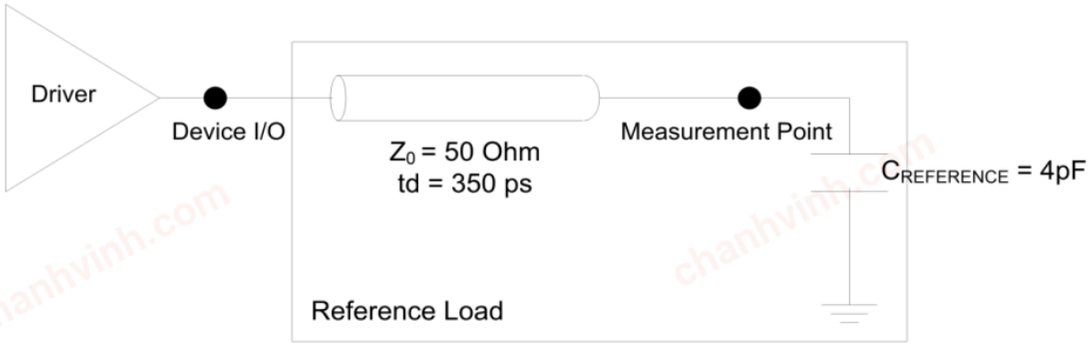


Figure 10 – HS400 reference load

7.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

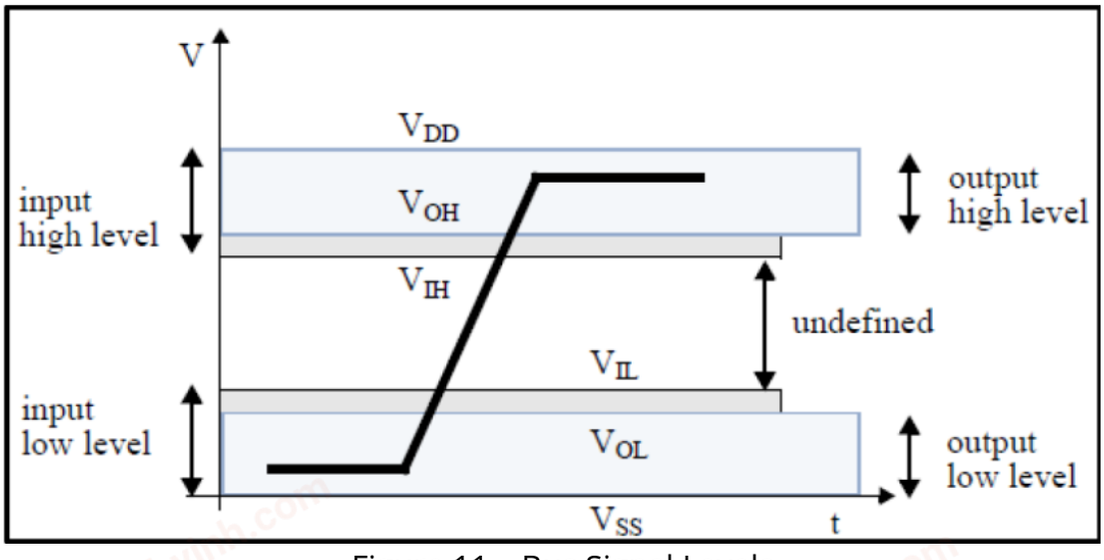


Figure 11 – Bus Signal Levels

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7.3.1 Open-drain Mode Bus Signal Level

Table 18 – Open-drain Bus Signal Level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} – 0.2		V	I_{OH} = -100µA
Output LOW voltage	V_{OL}		0.3	V	I_{OL} = 2 mA

The input levels are identical with the push-pull mode bus signal levels.

7.3.2 Push-pull mode bus signal level— eMMC

The device input and output voltages shall be within the following specified ranges for any VDD of the allowed voltage range

For 2.7V-3.6V VCCQ range (compatible with JESD8C.01)

Table 19 – Push-pull Signal Level—High-voltage eMMC

Parameter	Symbol	Min	Max.	Conditions
		Unit: V		
Output HIGH voltage	V_{OH}	0.75 * V_{CCQ}		I_{OH} = -100 µA @ V_{CCQ} min
Output LOW voltage	V_{OL}		0.125 * V_{CCQ}	I_{OL} = 100 µA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 * V_{CCQ}	V_{CCQ} + 0.3	
Input LOW voltage	V_{IL}	V_{SS} – 0.	0.25 * V_{CCQ}	

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For 1.70V – 1.95V V_{CCQ} range (: Compatible with EIA/JEDEC Standard "EIA/JESD8-7 Normal Range" as defined in the following table.

Table 20 – Push-pull Signal Level—1.70 -1.95 V_{CCQ} Voltage Range

Parameter	Symbol	Min	Max.	Conditions
		Unit: V		
Output HIGH voltage	V_{OH}	V_{CCQ} – 0.45V		I_{OH} = -2mA
Output LOW voltage	V_{OL}		0.45V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 * V_{CCQ}[1]	V_{CCQ} + 0.3	
Input LOW voltage	V_{IL}	V_{SS} – 0.3.	0.35 * V_{DD}[2]	
Notes: 1. 0.7 * V_{DD} for MMC™4.3 and older revisions. 2. 0.3 * V_{DD} for MMC™4.3 and older revisions.				

7.3.3 Bus Operating Conditions for HS200 & HS400

The bus operating conditions for HS200 devices is the same as specified in sections 10.5.1 of JESD84-B51 through 10.5.2 of JESD84-B51. The only exception is that V_{CCQ}=3.3v is not supported.

7.3.4 Device Output Driver Requirements for HS200 & HS400

Refer to section 10.5.4 of the JEDEC Standard Specification No.JESD84-B51

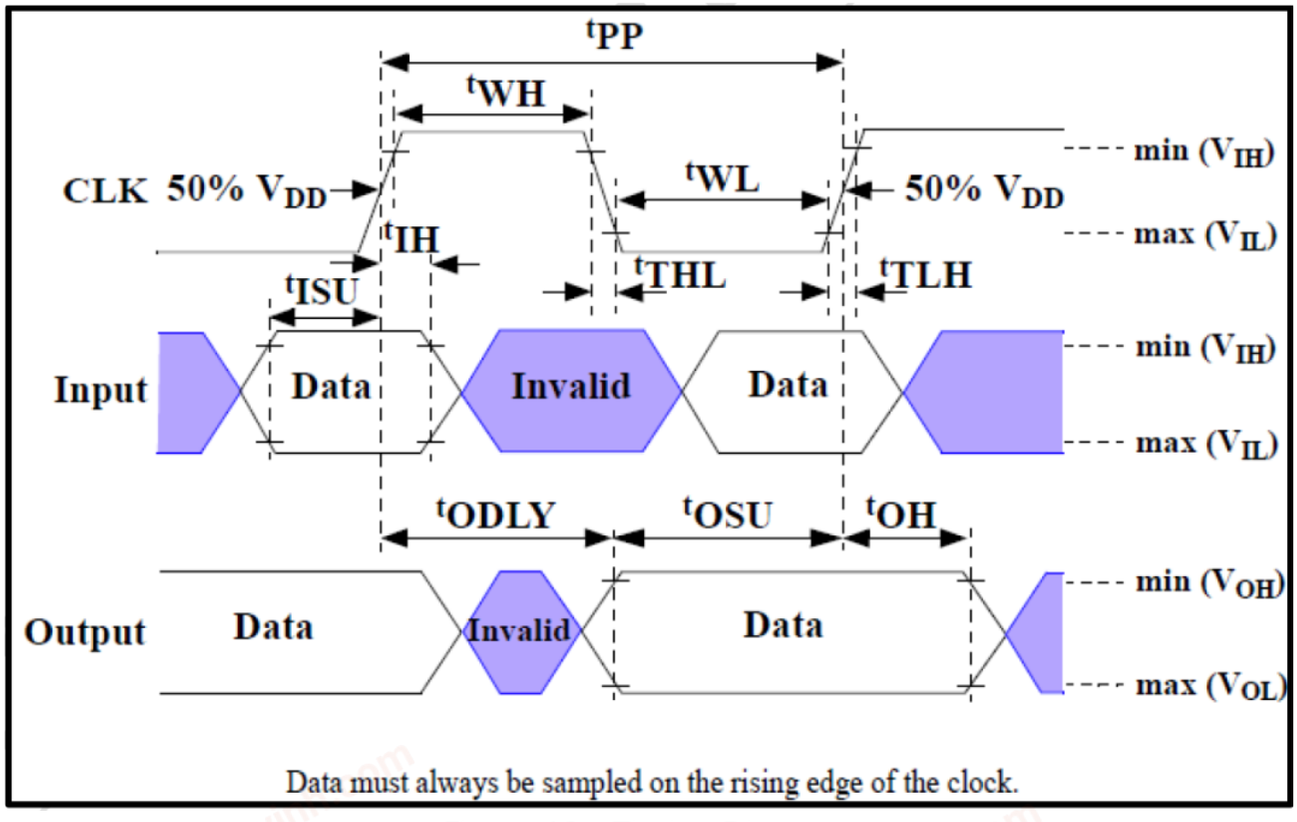


Figure 12 – Timing Diagram

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7.4 Bus Timing

7.4.1 Device Interface Timings

Table 21 – High-speed Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	fPP	0	52[3]	MHz	CL≤30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	CL≤ 30 pF
Clock low time	tWL	6.5		ns	CL≤ 30 pF
Clock rise time[4]	tTLH		3	ns	CL≤ 30 pF
Clock fall time	tTHL		3	ns	CL≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL≤ 30 pF
Input hold time	tIH	3		ns	CL≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	CL≤ 30 pF
Output hold time	tOH	2.5		ns	CL≤ 30 pF
Signal rise time[5]	tRISE		3	ns	CL≤ 30 pF

Notes: 1. CLK timing is measured at 50% of VDD.
2. eMMC shall support the full frequency range from 0-26Mhz or 0-52MHz
3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
4. CLK rise and fall times are measured by min (VIH) and max (VIL).
5. Inputs CMD DAT rise and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL). “

Table 22 – Backward-compatible Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	fPP	0	52[3]	MHz	CL≤30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	CL≤ 30 pF
Clock low time	tWL	6.5		ns	CL≤ 30 pF
Clock rise time[4]	tTLH		3	ns	CL≤ 30 pF
Clock fall time	tTHL		3	ns	CL≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL≤ 30 pF
Input hold time	tIH	3		ns	CL≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					

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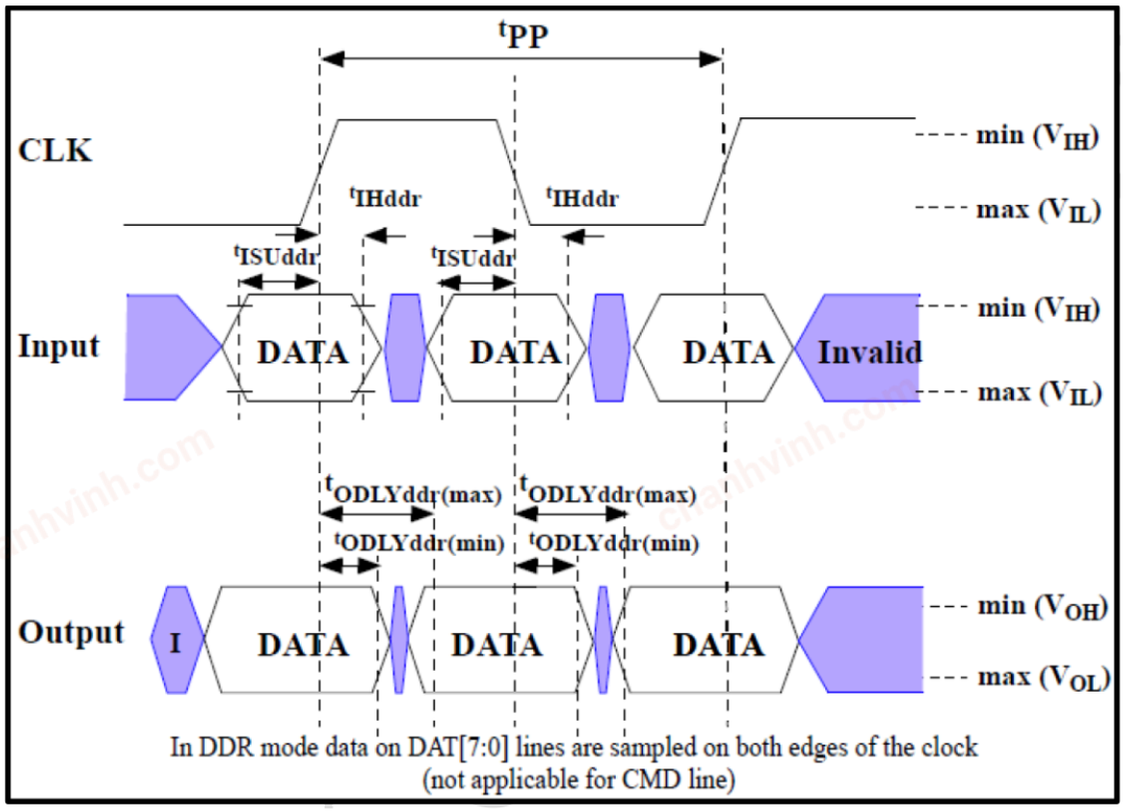
Output delay time during data transfer	tODLY		13.7	ns	CL≤ 30 pF
Output hold time	tOH	2.5		ns	CL≤ 30 pF
Signal rise time[5]	tRISE		3	ns	CL≤ 30 pF

Notes: 1. The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2.CLK timing is measured at 50% of VDD.
3. For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.
4. CLK rise and fall times are measured by min (VIH) and max (VIL).
5. tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its application notes.

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7.4.2 Bus Timing for DAT Signals During Dual Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 10.7 of JESD84-B51, therefore



there is no timing change for the CMD signal.

Figure 13 – Timing Diagram: Data Input/Output in Dual Data Rate Mode

7.4.3 Dual Data Rate Interface Timings

Table 23 – High-speed Dual Data Rate Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					

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Output delay time during data transfer	tODLYddr	1.5	7	ns	CL≤ 30 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL≤ 30 pF
Signal fall time (all signals)	tFALL		2	ns	CL≤ 30 pF
Notes: 1. CLK timing is measured at 50% of VDD. 2. Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL})					

7.5 Bus Timing Specification in HS200 Mode

7.5.1 HS200 Clock Timing

Host CLK Timing in HS200 mode shall conform to the timing specified in Figure 14 and Table23. CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device.

The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.

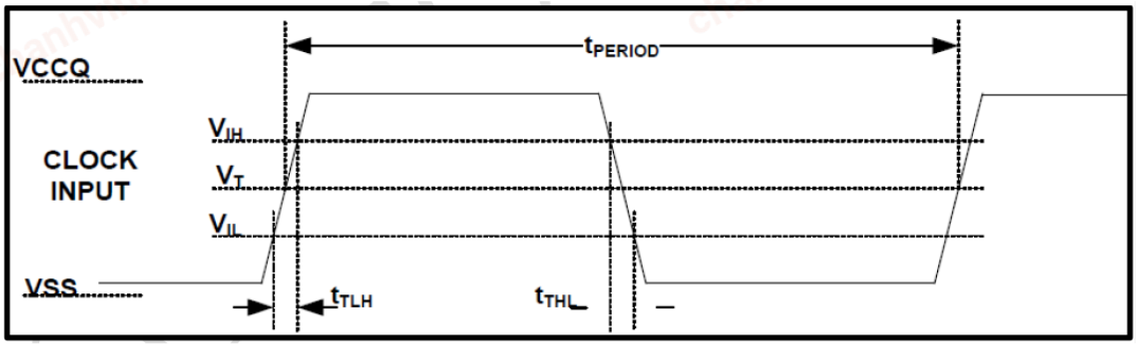


Figure 14 – HS200 Clock Signal Timing

Notes: 1. V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

0. V_T=0.975V – Clock Threshold, indicates clock reference point for timing measurements.

Table 24 – HS200 Clock Signal Timing

Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2* t_{PERIOD}	ns	t_{TLH}, t_{THL} [SEP] < 1ns (max.) at 200MHz, C_{device} =12pF, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

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7.5.2 HS200 Device Input Timing

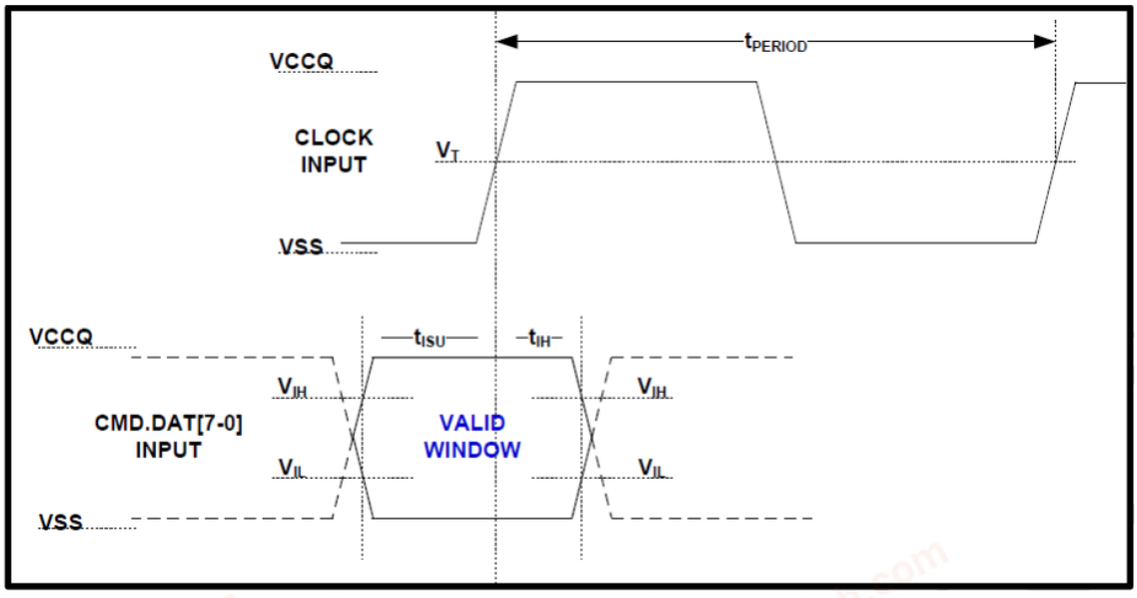


Figure 15 – HS200 Device Input Timing

Notes: 1. T_{ISU} and t_{IH} are measured at VIL (max.) and VIH (min.).
VIH denote VIH (min.) and VIL denotes VIL(max.).

Table 25 – HS200 Device Input Timing

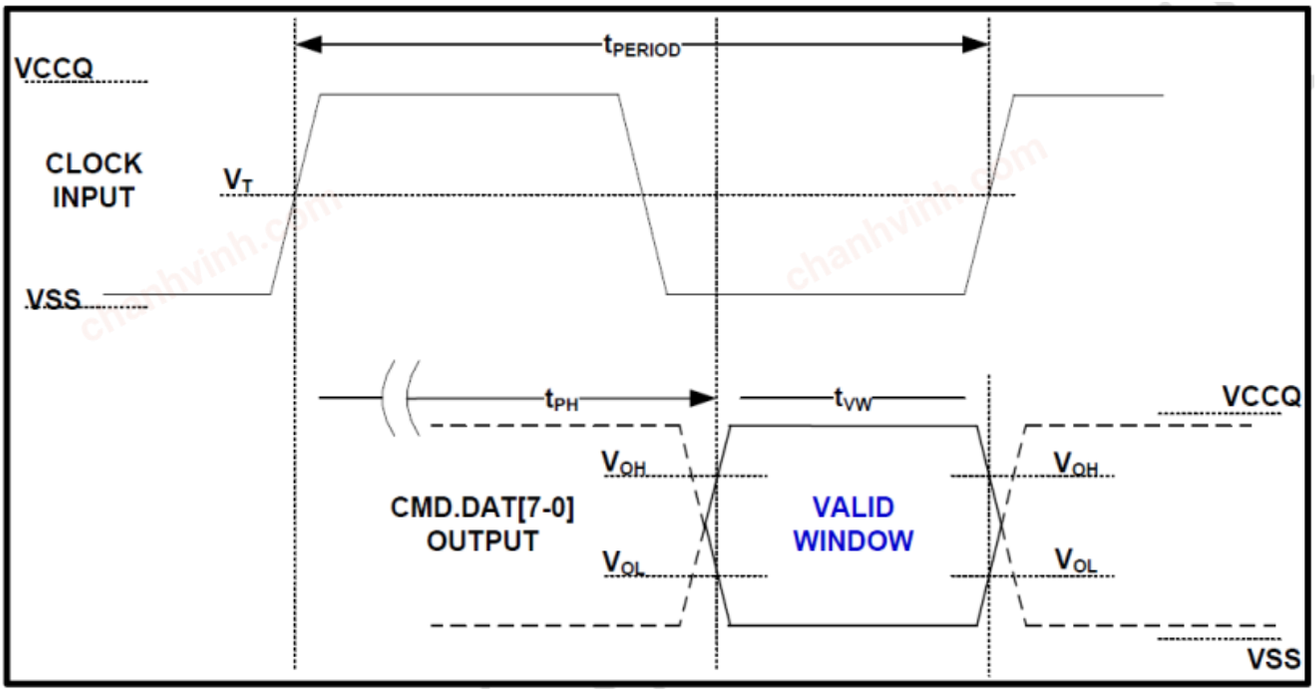
Symbol	Min.	Max.	Unit	Remark
t_{ISU}	1.4	-	ns	C_{device} ≤ 6pF
t_{IH}	0.8	-	ns	C_{device} ≤ 6pF

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7.5.3 HS200 Device Output Timing

tPH parameter is defined to allow device output delay to be longer than tPERIOD. After initialization, the tPH may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode. Figure 16 and Table 20 define Device output timing. While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by ΔTPH. Output valid data window (tVW) is available regardless of the drift (ΔTPH) but position of data window varies by the drift, as described in Figure 17.

Figure 16 – HS200 Device Output Timing



Notes: 1. VOH denotes VOH(min.) and VOL denotes VOL(max.).

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Table 26 – Output Timing

Symbol	Min.	Max.	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT=-20°C)	+1550 (ΔT=90°C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 125°C during operation.
T_{VW}	0.575		UI	t_{VW}=2.88ns at 200MHz Using test circuit in Figure 18 including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected T_{VW} at Host input is larger than 0.475UI.

Notes: 1. Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.

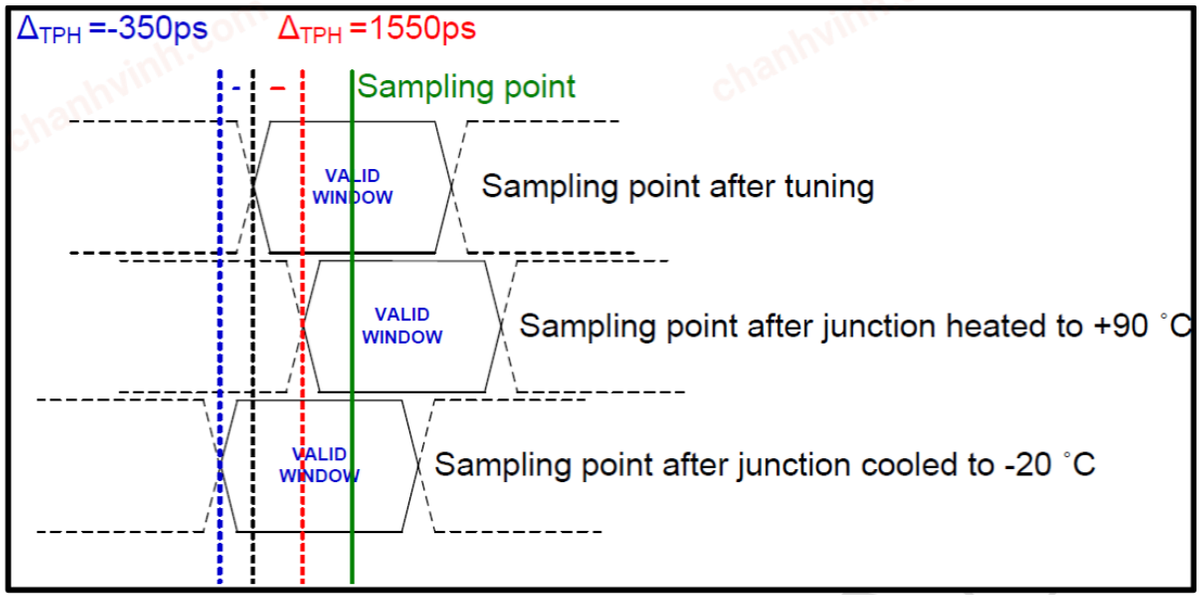


Figure 17 – ΔT_{PH} consideration

Implementation Guide: Host should design to avoid sampling errors that may be caused by the ΔT_{PH} drift. It is recommended to perform tuning procedure while Device wakes up, after sleep. One simple way to overcome the ΔT_{PH} drift is by reduction of operating frequency.

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7.6 Bus Timing Specification in HS400 mode

7.6.1 HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode. Figure 18 show Device input timing

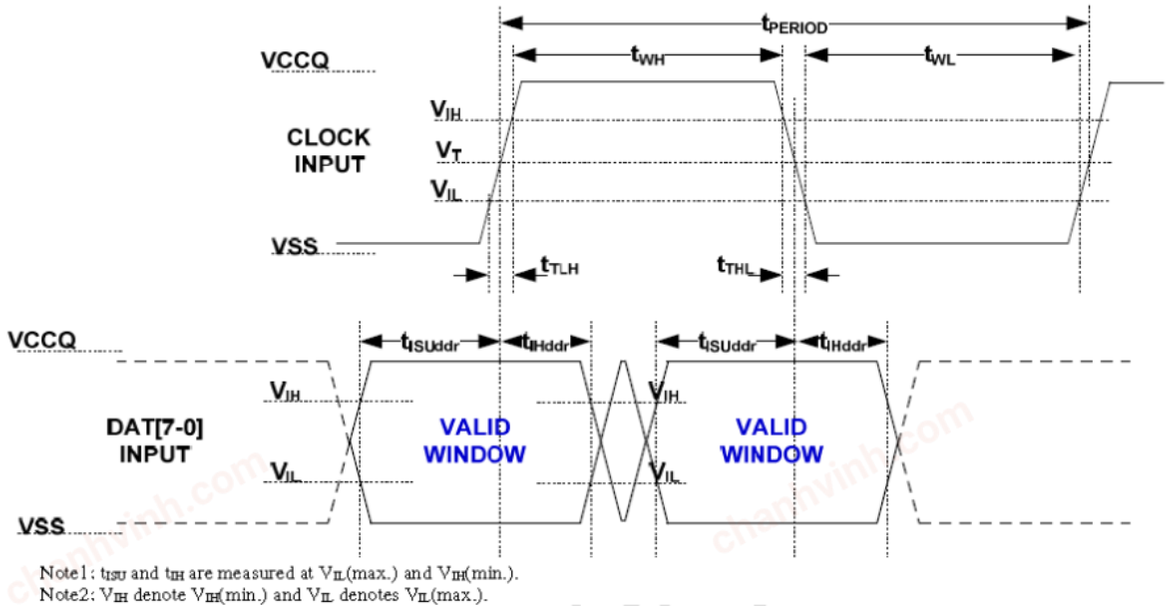


Figure 18 – HS400 Device Data input timing

Table 27 – HS400 Device input timing

	Symbol	Min	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL
Duty cycle distortion	tCKDCD	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to VT. Includes jitter
Minimum pulse width	tCKMPW	2.2		ns	With respect to VT.
Inputs DAT (referenced to CLK)					
Input set-up time	tISUddr	0.4		ns	Cdevice ≤ 6pF With respect to VIH/VIL.
Input hold time	tIHddr	0.4		ns	Cdevice ≤ 6pF With respect to VIH/VIL.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL.

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7.6.2 HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

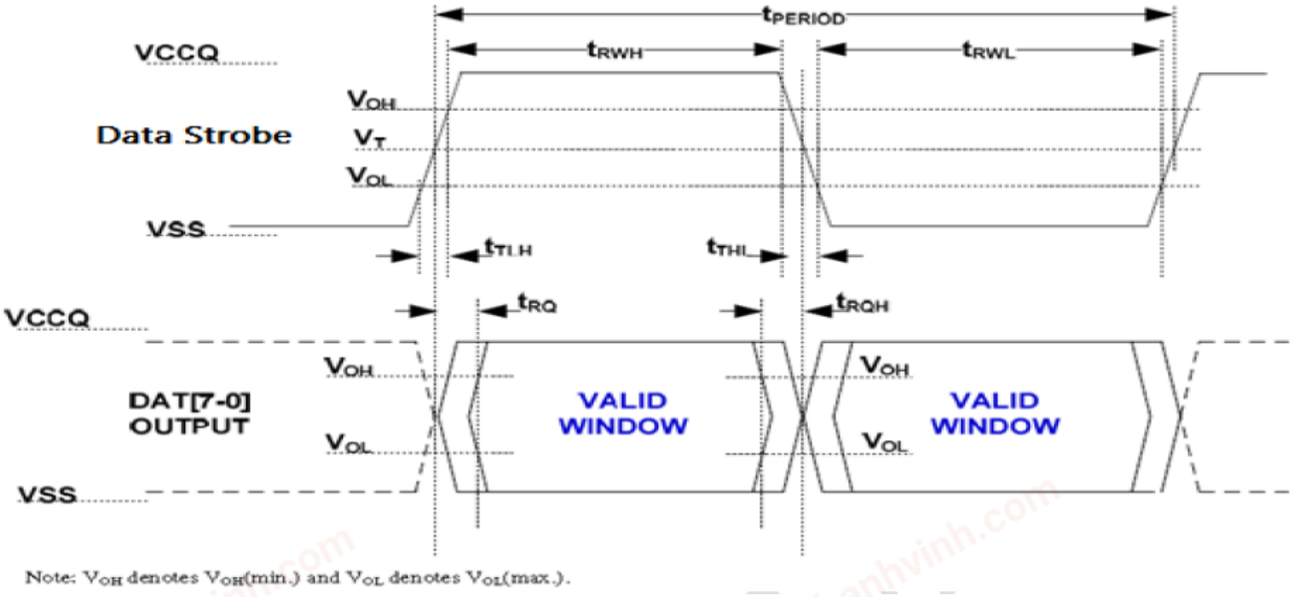


Figure 19 – HS400 Device output timing

Table 28 – HS400 Device Output timing

Parameter	Symbol	Min	Max.	Unit	Remark
Data Strobe					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT.
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (tCKDCD) With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.2		ns	With respect to VT.
Read pre-amble	tRPRE	0.4		ns	Max value is specified by anufacturer. Value up to infinite is valid
Read post-amble	tRPS	0.4		ns	Max value is specified by anufacturer. Value up to infinite is valid
Onputs DAT (referenced to Data Strobe)					
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400

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					reference load

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Table 29 – HS400 Capacitance

Parameter	Symbol	Min	Max.	Unit	Remark
Pull-up resistance for CMD	RCMD	4.7	50	Kohm	
Pull-up resistance for DAT0-7	RDAT	10	50	Kohm	
Pull-down resistance for Data Strobe	RDS	10	50	Kohm	
Internal pull up resistance DAT1-DAT7	Rint	10	150	Kohm	
Single Device capacitance	Cdevic		6	pF	

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8 Package Dimensions

8.1 Package Dimensions

11.5 x 13.0 x 1.0mm

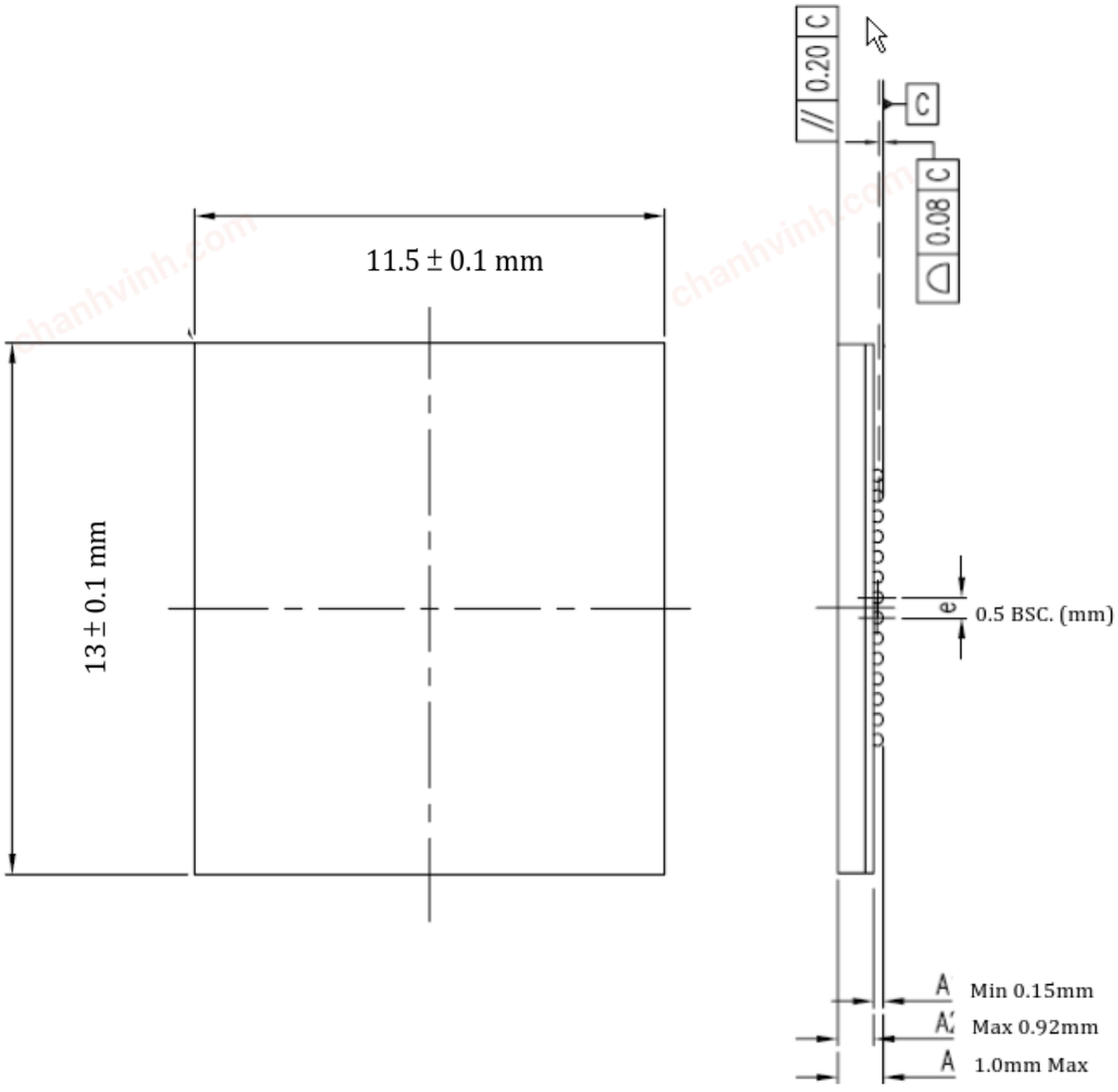
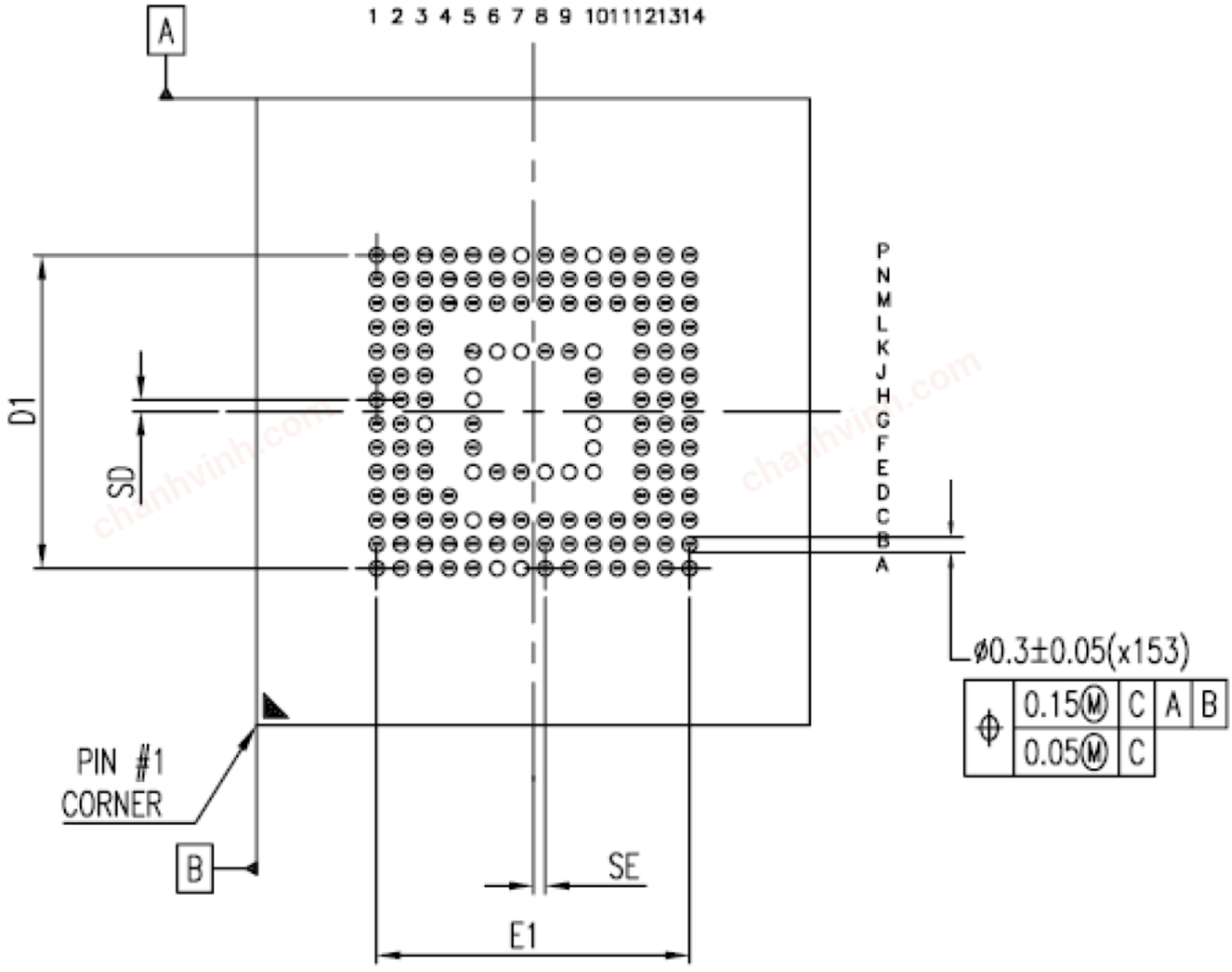


Figure 20 – Outline Dimension

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8.2 Ball Pattern Dimensions (Bottom View)



N	SE(MM)	SD(MM)	E1(MM)	D1(MM)	JEDEC(REF)
153	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

Figure 21 – Ball Pattern Dimensions

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8.3 Ball Assignment (153 balls)

Ball Assignment, Top view

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	14
13	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	13
12	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	12
11	NC	NC	NC									NC	NC	NC	11
10	NC	NC	NC		VSF	VSF	VSF	VSS	VCC	VSF		NC	NC	VSF	10
9	NC	NC	NC		VSF					VCC		NC	NC	NC	9
8	NC	NC	NC		VSF					VSS		NC	NC	NC	8
7	RFU	NC	NC		VSS					RFU		NC	NC	RFU	7
6	VSS	DAT7	VCCQ		VCC					RFU		CLK	NC	VSSQ	6
5	DAT2	DAT6	NC		RFU	VCC	VSS	DS	VSS	RST_n		CMD	VSSQ	VCCQ	5
4	DAT1	DAT5	VSSQ	NC								VCCQ	VCCQ	VSSQ	4
3	DAT0	DAT4	NC	NC	NC	NC	RFU	NC	NC	NC	NC	NC	NC	VCCQ	3
2	NC	DAT3	VDDi	NC	NC	NC	NC	NC	NC	NC	NC	NC	VSSQ	NC	2
1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 22 – Ball Assignment (Top View)

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9 eMMC Device Signal

The eMMC device transfers data via a configurable number of data bus signals. The communication signals as below

Table 30 – Device Signal

Name	Type	Description
CLK	I	**Clock**: Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency
DS	O	**Data Strobe**: This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. 53allst o output each cycle of this signal directs two bits transfer(2x) on the data – one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.
CMD	I/O/PP/OD	**Command**: This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal 53allst operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC host controller 53allst eMMC Device and responses are sent from the Device 53allst host.
DAT[7..0]	I/O/PP	**Data**: These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering 53allst 8-bit mode, the device disconnects the internal pull-ups of lines DAT1–DAT7.
RST_n	I	Hardware Reset: By default, hardware reset is disabled and must be enabled in the EXT_CSD register if used. Otherwise, it can be left un-connected.
RFU	-	Reserved for future use, Left it floating.
NC	-	Not Connected: These pins are not internally connected.
Vddi	-	Internal Voltage Node: This pin provides access to the output of an internal voltage regulator to allow for the connection of an external capacitor.
Vcc	S	Supply Voltage for core
Vccq	S	Supply Voltage for I/O
Vss	S	Supply Ground for core
Vssq	S	Supply Ground for IO
VSF		Vendor specific function. Left it floating.
Note: I=Input; O=Output; PP=Push-Pull; OD=Open_Drain; S=Power Supply		

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Revision History

Revision	Descriptions	Release Date
0.1	Preliminary Release	Jan, 2022
0.2	Revise part number in Table 1	Feb, 2022
0.3	Revise part number in Table 1	Feb, 2022
0.85	Revise Table 4	June, 2022
1.1	Revised Endurance values	April, 2024