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EiceDRIVER™

WCDSC006

Features

- Independent High Side and Low Side TTL logic inputs
- 0.3 V to 7 V Input pin capability for increased robustness
- Integrated bootstrap diode
- Maximum bootstrap voltage of 60 V
- 2 A source/4 A sink current capability for high and low side drivers

Potential applications

- Inductive wireless charger
- Qualified according Jedec Standard

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The WCDSC006 is a half bridge driver designed to drive both high-side and low-side MOSFETs in a half-bridge inverter configuration. The floating high-side driver is capable of driving a high-side MOSFET operating up to 60 V bootstrap voltage. The high-side bias voltage is generated using a bootstrap technique. The inputs of the driver are TTL logic compatible and can withstand input voltages up to 7 V regardless of the VDD voltage. Even though high-side and low-side power device are driven independently, the driver enforces a 5 ns (typ) deadtime to prevent shoot-through. The WCDSC006 is available in PG-WSON-10 pins, with exposed pad, connected to ground, to aid power dissipation.

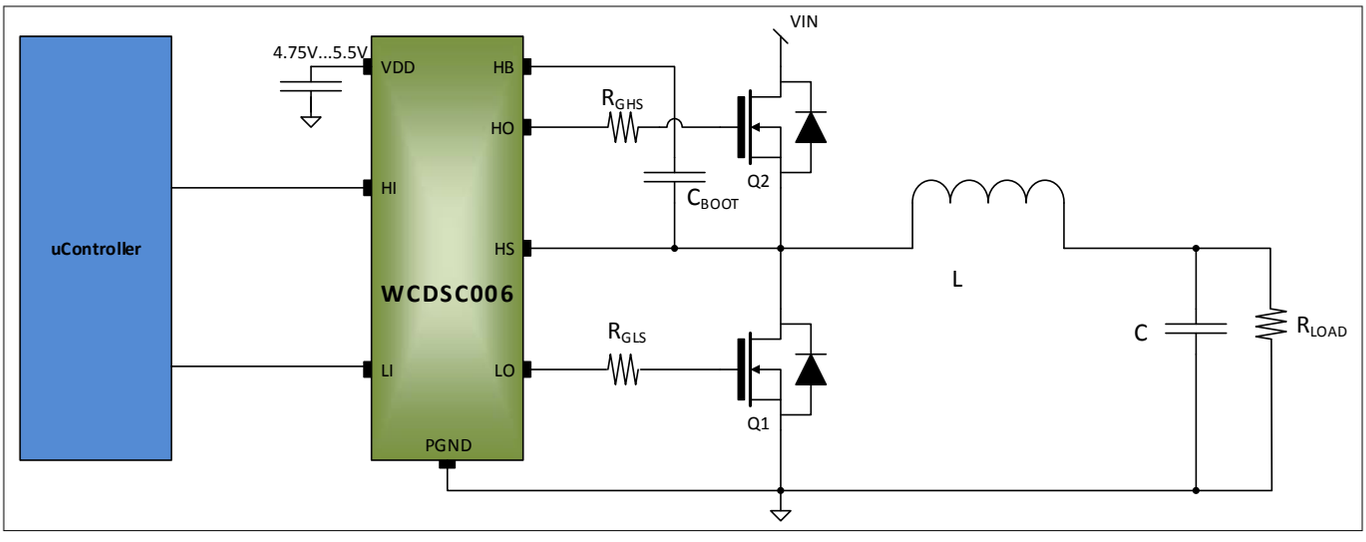


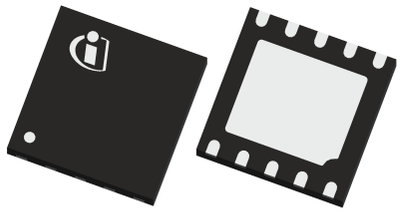
Figure 1 Typical application

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Description

Packages





Ordering information

Base Part Number	Package Type	Standard Pack		Orderable Part Number	Marking Code
		Form	Quantity		
WCDSC006	PG-WSON-10	Tape and Reel	6000	WCDSC006XUMA1	EDrWCDS006

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1 Block diagram reference

A simplified functional block diagram is given in the figure below.

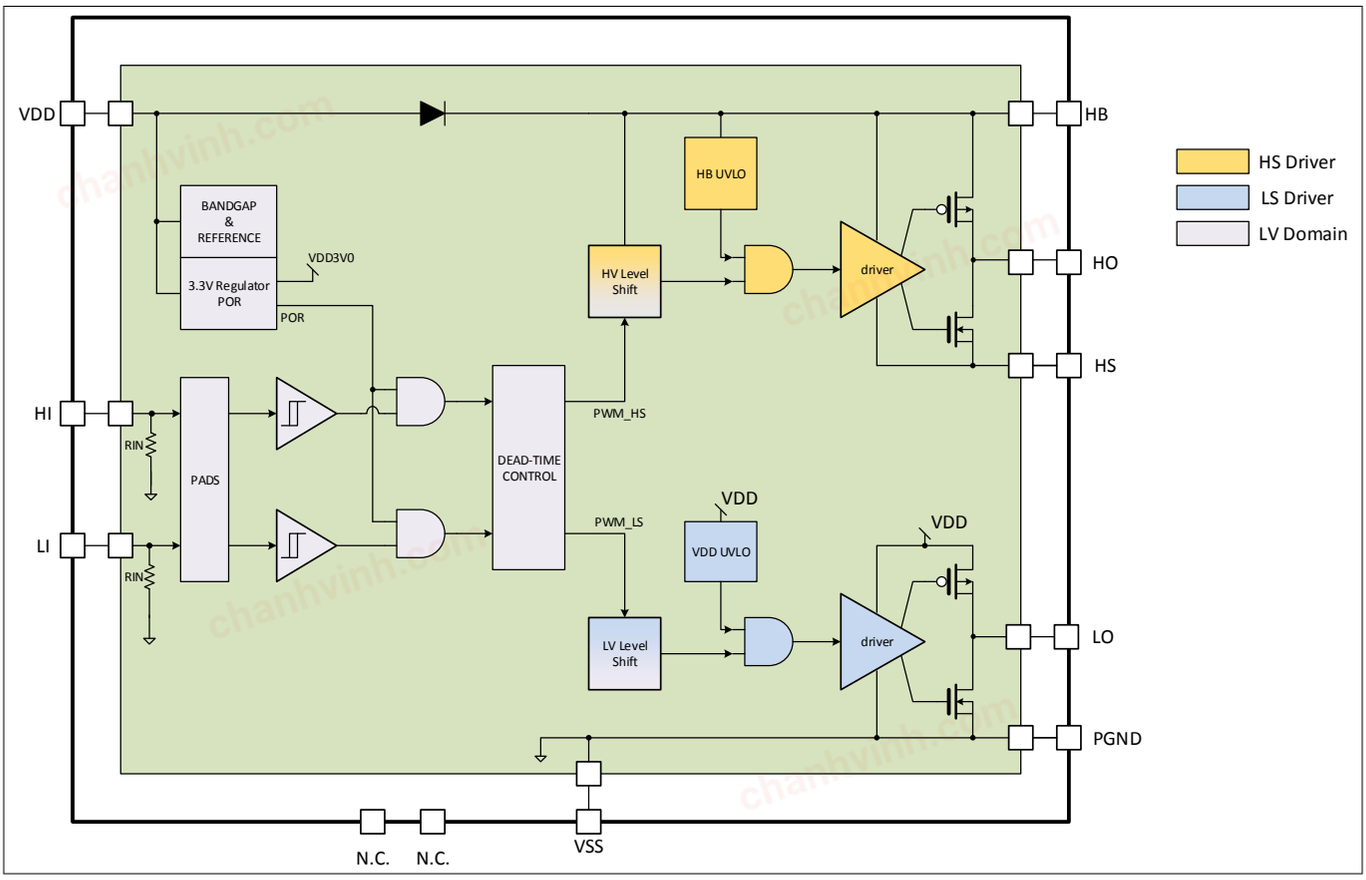


Figure 2 Block diagram

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2 Pin configuration

2.1 Pin assignment

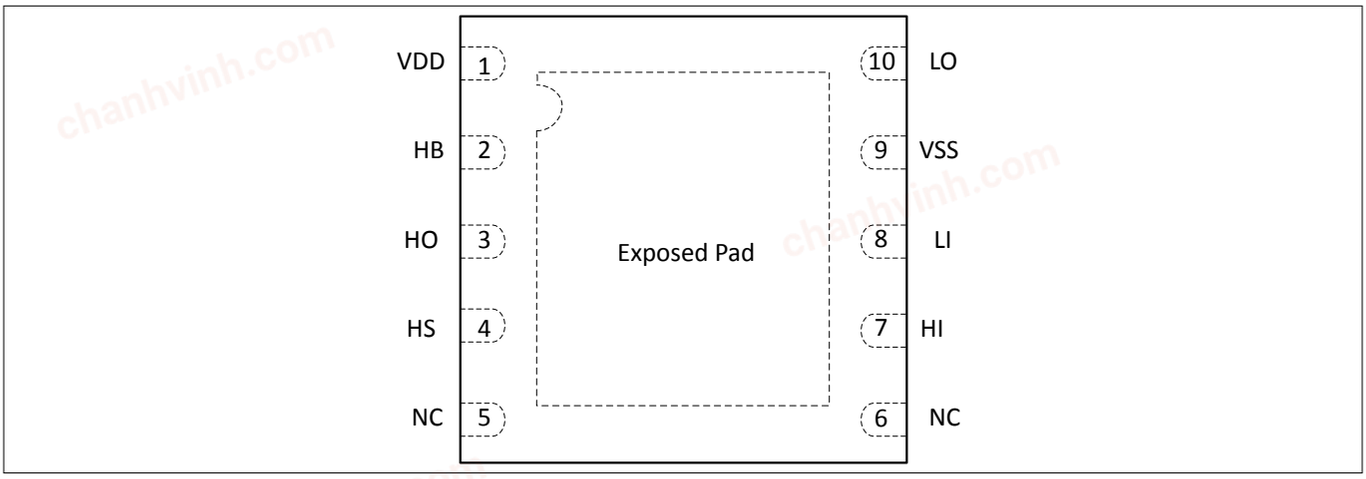


Figure 3 Pin configuration PG-WSON-10, top view

2.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	*VDD*	Gate drive supply
2	*HB*	High Side gate driver bootstrap rail
3	*HO*	High Side gate driver source and sink current output
4	*HS*	High Side FET source connection
5	*NC*	Not connected
6	*NC*	Not connected
7	*HI*	High Side driver control input
8	*LI*	Low Side driver control input
9	*VSS*	Ground return
10	*LO*	Low Side gate driver source and sink current output

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3 Electrical characteristics and parameters

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

Stresses above the listed values may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Parameter	Symbol	Values		Unit	Note or Test Condition
		Min.	Max.		
High Side Bootstrap Voltage DC rating	V_{HB}	–	60	V	
Bootstrap Supply Voltage	V_{HB} to V_{HS}	-0.3	7	V	T_C = 25°C
Driver Supply Voltage	V_{DD} to V_{SS}	-0.3	7	V	T_C = 25°C
Phase voltage to ground	V_{HS}	-(9-V_{DD})	V_{HB}+0.3	V	
Input voltage on HI and LI	V_{HI}, V_{LI}	-0.3	6	V	
Storage Temperature	T_S	-55	150	°C	
Junction Temperature	T_j	-55	150	°C	

3.2 Recommended operating conditions

Table 3 Recommended operating conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Phase Voltage to PGND	V_{HS}	-(8-V_{DD})	–	V_{HB}-V_{DD}	V	
Driver Supply Voltage	V_{DD}	4.75	–	5.5	V	
High Side Bootstrap Voltage	V_{HB}	–	–	50	V	
Junction Temperature	T_J	-40	–	+125	°C	
Input voltage on HI and LI	V_{HI}, V_{LI}	0	–	5.5	V	

3.3 Static electrical characteristics

Table 4 Static electrical characteristics

V_{DD} = V_{HB} = 5 V, V_{HS} = V_{SS} = 0 V, T_C = 25°C unless otherwise specified.
The V_{IN} and I_{IN} parameters are referenced to V_{SS}.

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
V_{DD} Supply *UVLO* Rising Threshold	$UVLO_{VDD}$	3.7	4.1	4.5	V	

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Table 4 Static electrical characteristics (continued)

V_{DD} = V_{HB} = 5 V, V_{HS} = V_{SS} = 0 V, T_C = 25°C unless otherwise specified.
The V_{IN} and I_{IN} parameters are referenced to V_{SS}.

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
V_{DD} Supply *UVLO* Threshold Hysteresis	$UVLO_{VDD,hys}$	–	0.2	–	V	
V_{HB} Supply *UVLO* Rising Threshold	$UVLO_{HB}$	3.5	3.9	4.3	V	
V_{HB} Supply *UVLO* Threshold Hysteresis	$UVLO_{HB,hys}$	–	0.2	–	V	
Boot voltage Quiescent Current	I_{QHB}	–	-	200	µA	V_{LI} = V_{HI} = 0 V
Boot voltage Operating Current	I_{OHB}	–	3.3	-	mA	f = 500 kHz C_{LOAD} = 1 nF
V_{DD} Quiescent Current	I_{QDD}	–	-	400	µA	V_{LI} = V_{HI} = 0 V
V_{DD} Operating Current	I_{ODD}	–	3.6	-	mA	f = 500 kHz C_{LOAD} = 1 nF
Input voltage high (HI and LI)	V_H		2.3	2.6	V	
Input voltage low (HI and LI)	V_L	1.3	1.5	–	V	
Input voltage Hysteresis	V_{HYST}	–	0.8	–	V	
Input Pulldown Resistance	R_{IN}	-	200	-	kΩ	
Peak Source current (HO and LO)(1)	I_{OHL}	–	2	–	A	
Peak Sink Current (HO and LO)(1)	I_{OLL}	–	4	–	A	
Pull down resistance	R_{PD}	–	0.43	0.8	Ω	
Pull up resistance	R_{PU}	–	1.07	2	Ω	
Bootstrap diode dynamic resistance	R_D	–	2.7	-	Ω	I_{VDD-HB} = 100 mA I_{VDD-HB} = 1 mA
Bootstrap forward voltage	V_D	–	0.93	1.3	V	I_{VDD-HB} = 100 mA
Bootstrap diode revers recovery time(1)	T_{rr}	–	50	–	ns	I_F = 20 mA I_{RR} = 500 mA T_C = 25°C

(1) No subject of final test

3.4 Dynamic electrical characteristics

Table 5 Dynamic electrical characteristics

V_{DD} = V_{HB} = 5 V, V_{HS} = V_{SS} = 0 V, T_C = 25°C unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Turn on and Turn off propagation delay of Hi and Low(1)	T_{LH}/T_{HL}	–	40	-	ns	

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Table 5 Dynamic electrical characteristics (continued)

V_{DD} = V_{HB} = 5 V, V_{HS} = V_{SS} = 0 V, T_C = 25°C unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
The delay matching LI to LO and HI to HO, both rising and falling(2)	*DELM*	–	1	8	ns	Gate Driver; V_{LI} = 0 V & V_{HI} = 5 V with no external deadtime
Minimum dead time between HI, LI(2)	$T_{deadtime}$	–	5	–	ns	C_{LOAD} = 0 nF
Minimum input pulse width that changes the output	T_{pw}	–	–	20	ns	
HO rise time	T_{HRC}	–	3	-	ns	C_{LOAD} = 1 nF
LO rise time	T_{LRC}	–	3	-	ns	
HO fall time	T_{HFC}	–	2	-	ns	
LO fall time	T_{LFC}	–	2	-	ns	

(1) A transient detector blocks the toggling of the high side output when it detects moving phase node (due to transition and/or oscillation). It prevents unwanted re-toggling but may increase propagation delay. See ***Figure 6*** and ***Figure 7*** for more information and link to *Understanding the transient detector* (***References***) for more information.

(2) No subject of final test

3.5 Thermal mechanical characteristics

Table 6 Thermal mechanical characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Junction to Case Thermal Resistance	R_{thJC}	–	7	–	°C/W	Bottom
		–	20	–	°C/W	Top
Device on PCB	R_{thJA}	–	40	–	°C/W	6 cm^2 cooling area(1)

(1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB vertical in still air.

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4 Timing diagrams

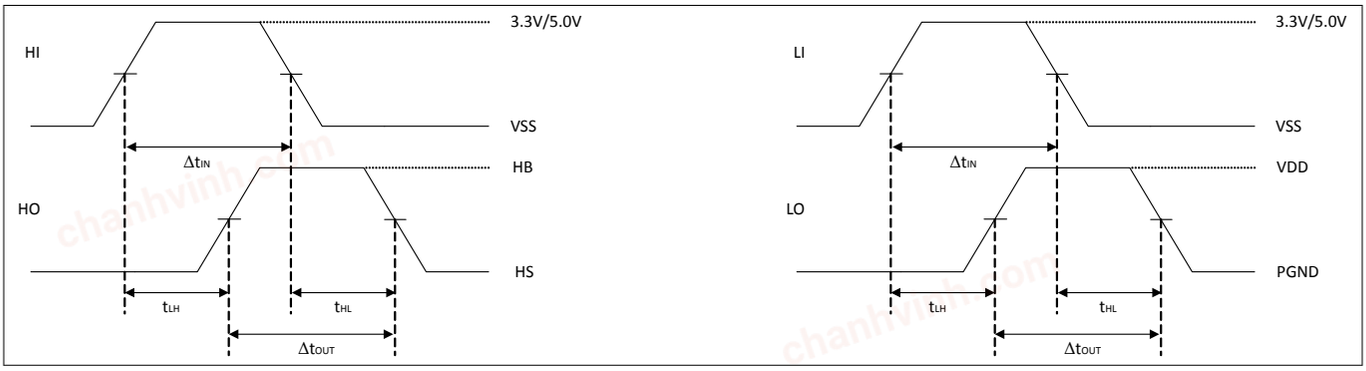


Figure 4 Propagation delay



Figure 5 UVLO behavior

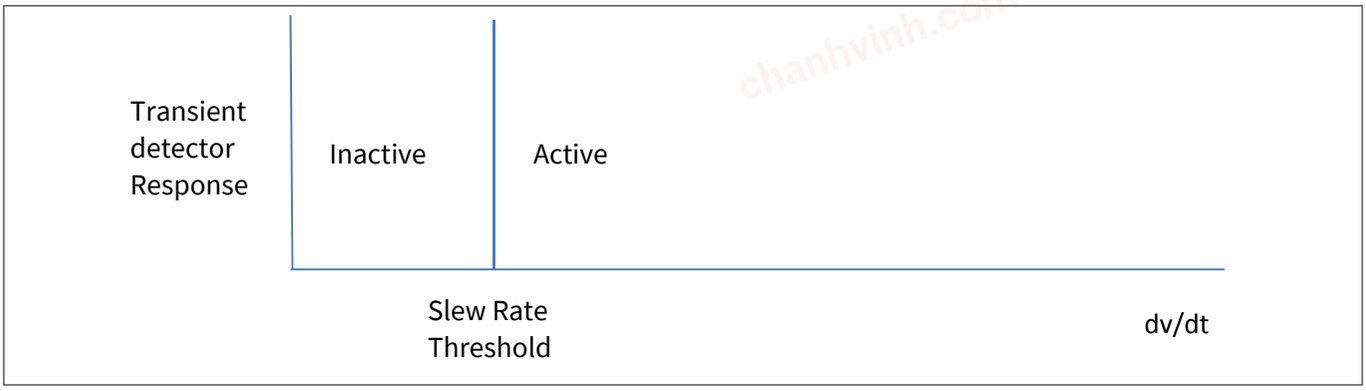


Figure 6 Transient detector response

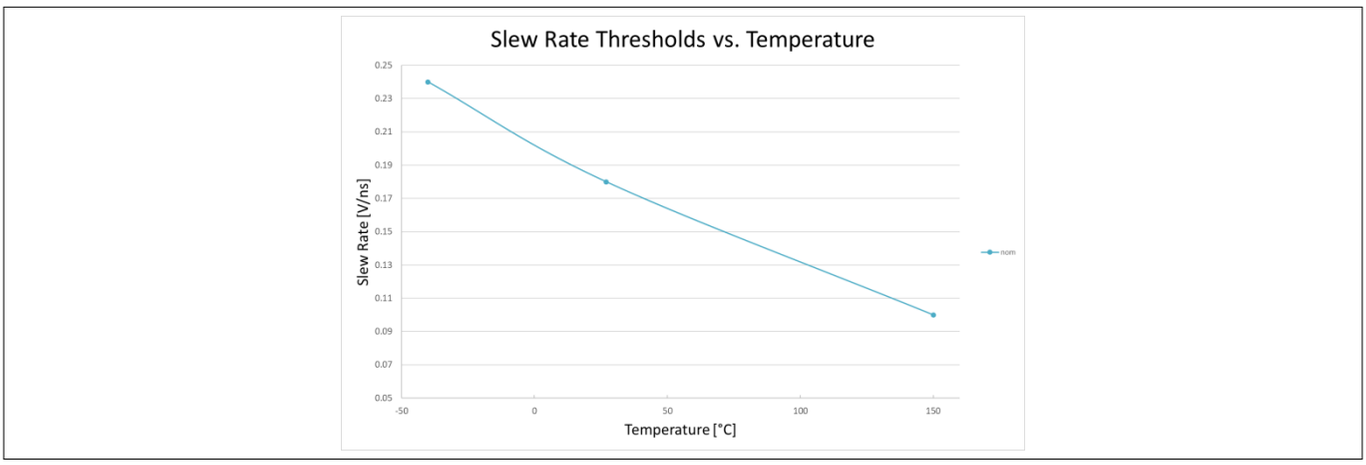
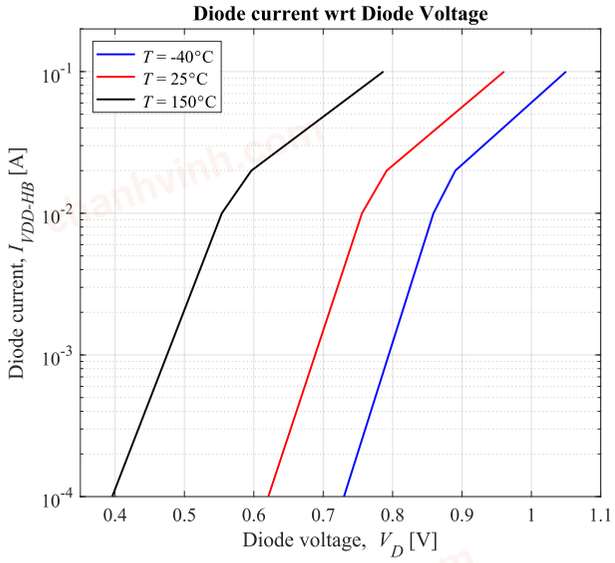
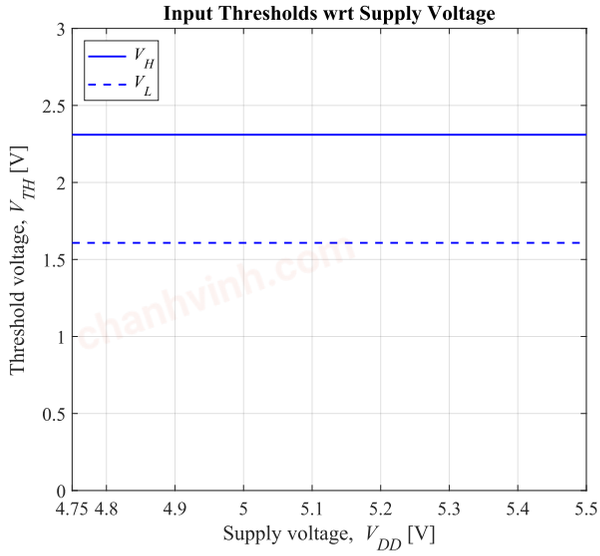


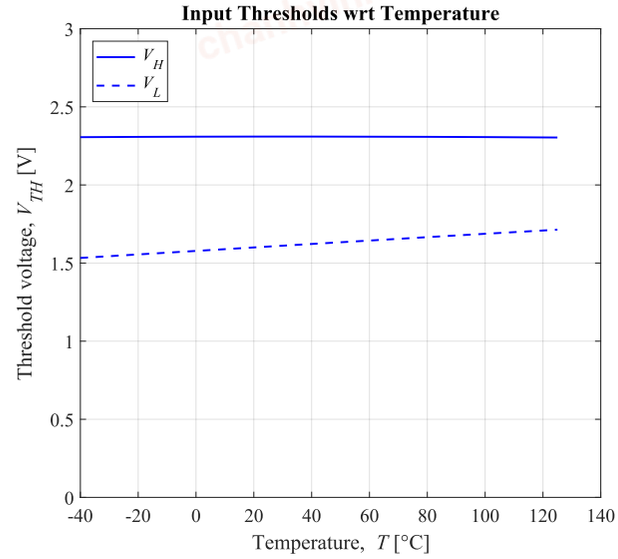
Figure 7 Transient detector slew rate thresholds vs. temperature

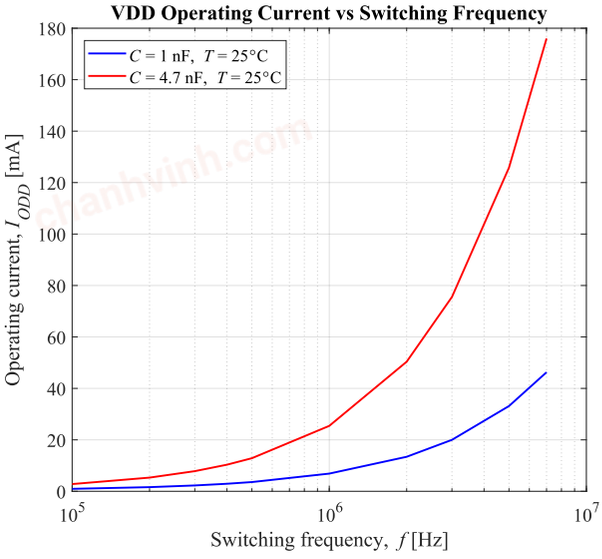
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5 Typical characteristics



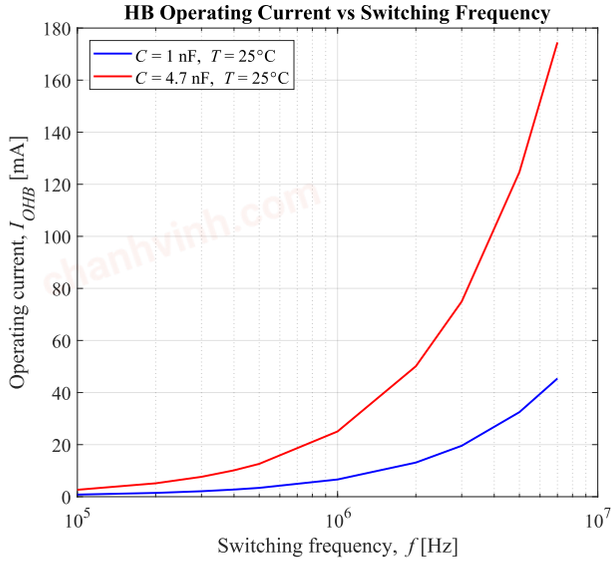


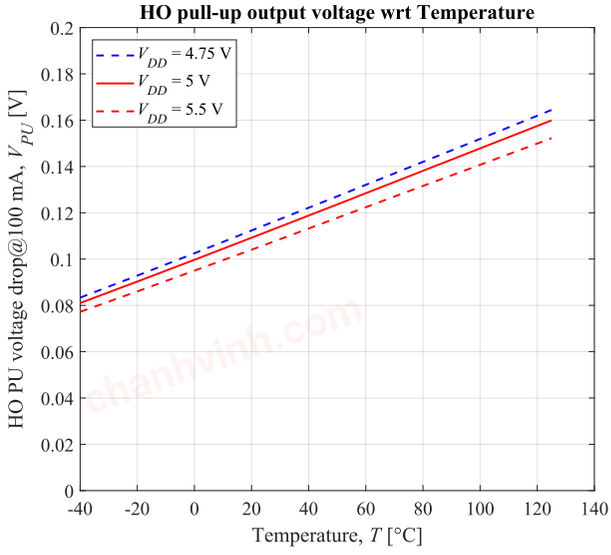


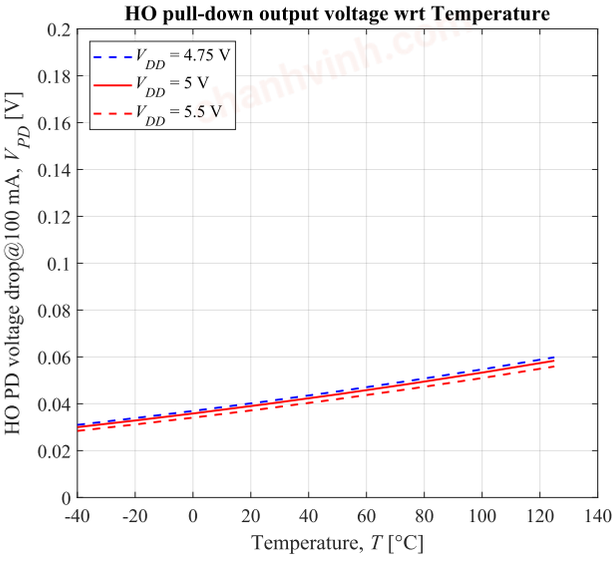


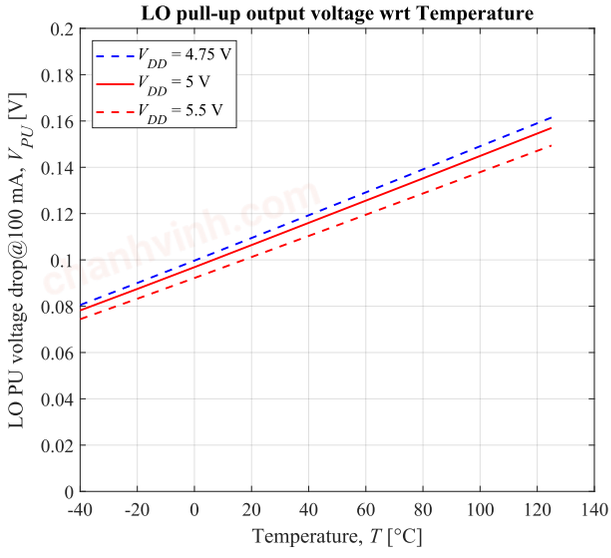
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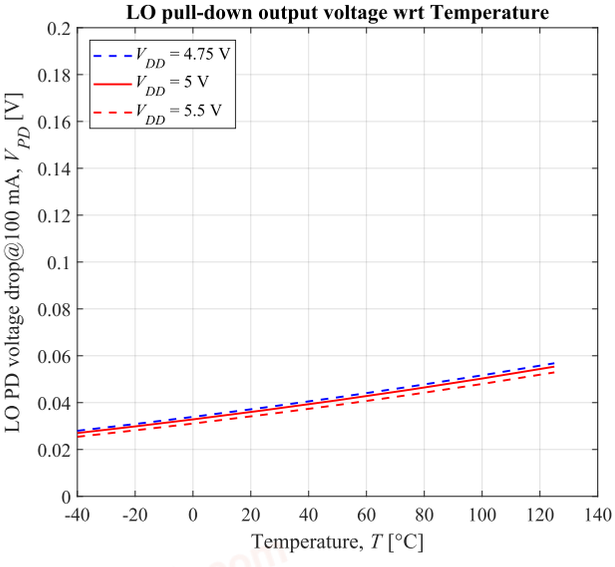
5 Typical characteristics

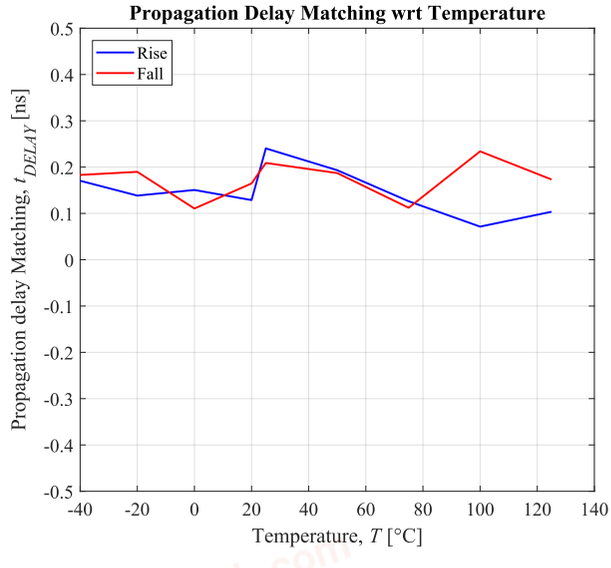






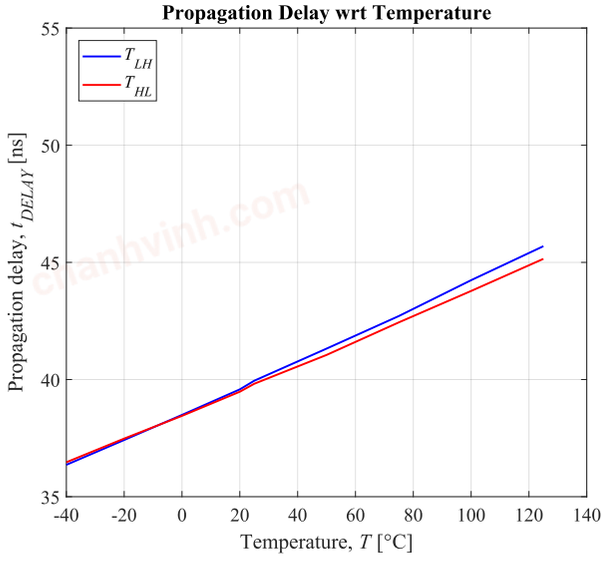


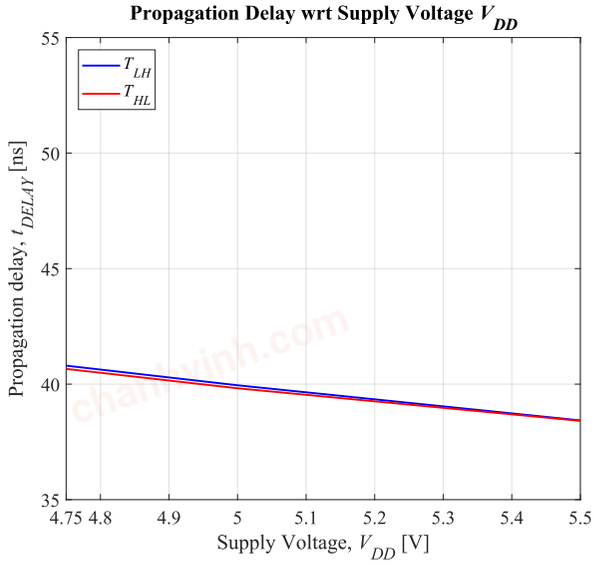


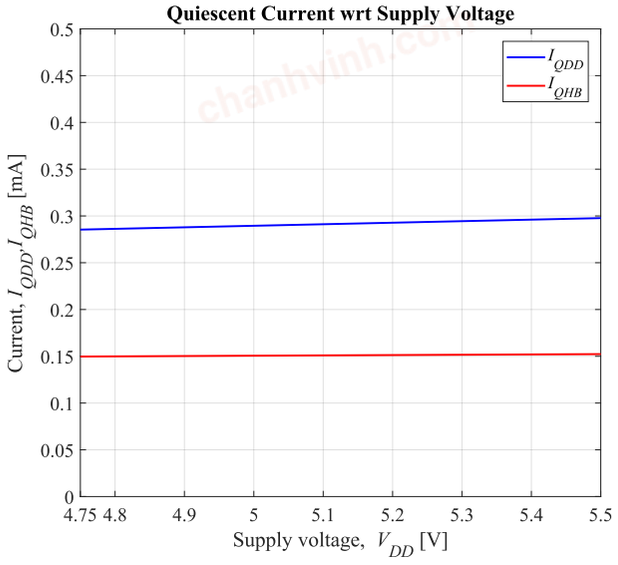


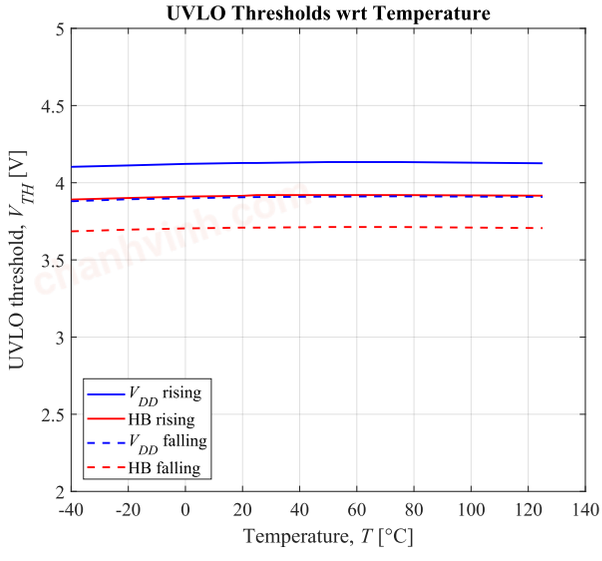
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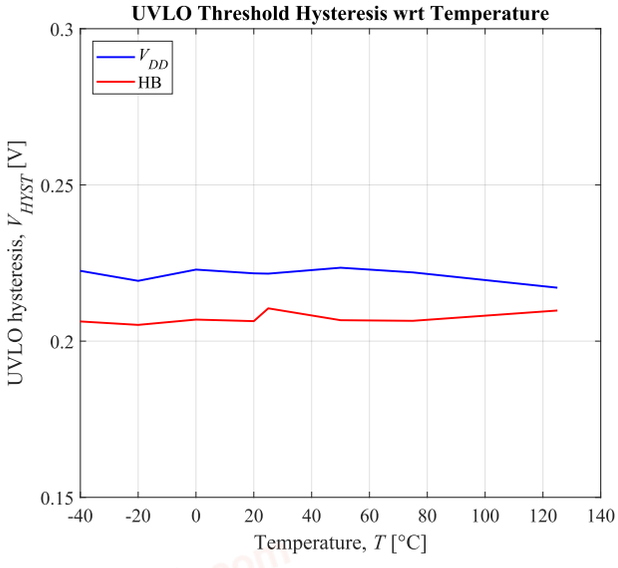
5 Typical characteristics











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6 Functional description

6.1 Introduction

The WCDSC006 is a fast Half-Bridge driver for both high-side and low-side MOSFETs in a wireless charging half-bridge inverter configuration. The focus on robustness at the input and output side additionally gives this device a safety margin in critical abnormal situations. All outputs are robust against reverse current. The interaction with the power MOSFET, even reverse reflected power will be handled by the strong internal output stage. All inputs are compatible with LV-TTL signal levels, signal delays and rise/fall times have been minimized.

6.2 Supply voltage

The absolute maximum supply voltage is 7 V. The minimum operating supply voltage is set by the undervoltage lockout function to a typical default value of 4.1 V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

6.3 Driver outputs

This driver output stage has a shoot through protection and current limiting behavior. After a switching event, current limitation is raised up to achieve the typical current peak for an excellent fast reaction time of the following power MOS transistor. The output impedance is very low with a typical value below 1.07 Ω for the sourcing p-channel MOS and 0.43 Ω for the sinking n-channel MOS transistor. Gate Drive Outputs held active low in case of floating inputs VHI, VLI or during startup or power down once UVLO is not exceeded. Under any situation, startup, UVLO or shutdown, outputs are held under defined conditions.

6.4 Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. Thus it can be guaranteed, that the switch transistor is not switched on if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 4.1 V. The max value of the rising edge is the value that ensures all the device among the production will be turned on during start up; that means designers have to provide a voltage higher than 4.5 V to turn on all the devices in the production of their equipment within the specified temperature range.

On the opposite side the minimum voltage necessary to switch off all the devices is the minimum of the falling edge. Therefore to be sure that all the devices in production will be turned off, in the specified temperature range, a voltage lower than 3.5 V has to be provided.

The hysteresis is the voltage gap between rising edge and falling edge. The UVLO function is implemented for both VDD and HB; this ensures some margin on noise effect, like false turn off. For instance a negative glitch smaller than the hysteresis will not have effect on the device preventing an unwanted turn off.

6.5 Input configuration

The inputs HI and LI control two PWM channels. The input signal is transferred non-inverted to the corresponding gate driver outputs HO and LO. All inputs are compatible with LV-TTL threshold levels and provide a hysteresis of typ. 0.8 V. The hysteresis is independent of the supply voltage VDD. The PWM inputs are internally pulled down to a logic low voltage level (GND). In case the PWM-controller signals have an undefined state during the power-up sequence, the gate driver outputs are forced to the "off"-state(low). ***Table 7*** shows the truth table of the device once the two UVLOs are turned on; in case the VDD-GND voltage or the HB-HS voltage is below the UVLO threshold the corresponding output will be low.

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Table 7 Truth table with VDD-GND and HB-HS higher than UVLO threshold

HI	LI	HO	LO	Notes
H	H	n.a.	n.a.	See note on the anti shoot-through protection
H	L	H	L	
L	L	L	L	
L	H	L	H	
X	X	L	L	

6.6 Minimum On Time

The minimum On time is the minimum duration of the input pulse which is generating an output pulse.

The upper limit is the pulse width at which all the drivers in production will provide an output signal. In other words the designer has to provide a pulse width longer than the upper limit of the minimum on time to ensure an output pulse for every driver of their equipment.

The upper limit of this parameter is determining the maximum switching frequency of the converter according to the formula:

$$t_{SW_{max}} = \frac{V_{IN} \times t_{ON_{max}} \times k}{V_{OUT}} \quad (1)$$

Where V_{IN} is the input voltage, V_{OUT} is the desired output voltage t_{ONmax} is the upper limit of the minimum on time and k is the transformer ratio.

There is a nonlinear transfer function between the inputs (HI, LI) and the outputs gate signals (HO, LO) represented in ***Figure 8***.

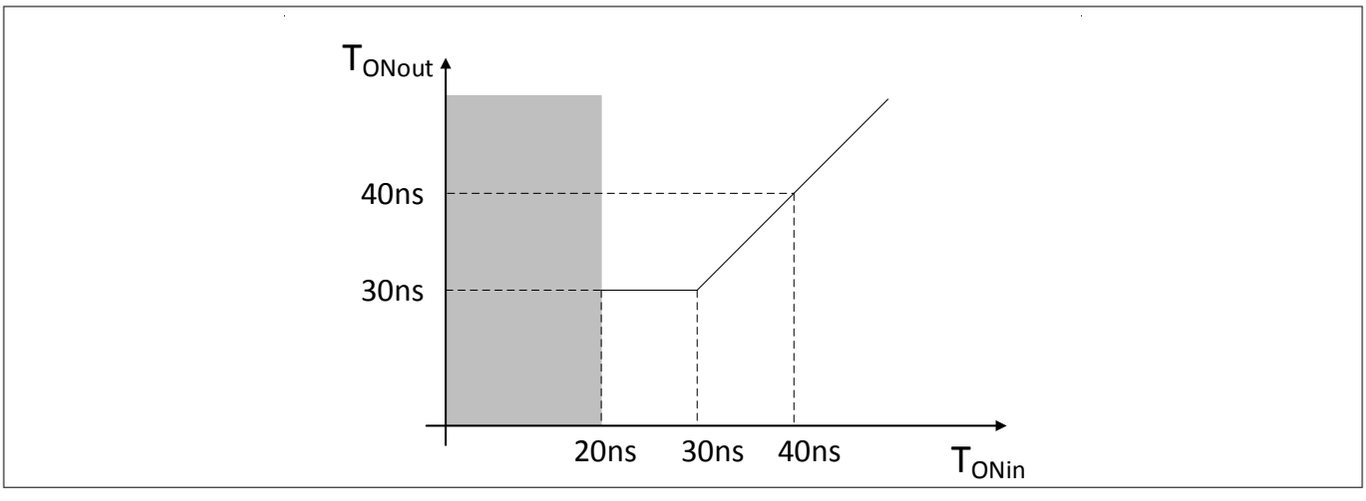


Figure 8 Input output transfer characteristic

For input pulses shorter than 20 ns pulse width (the grey area) the driver does not guarantee that the input pulse will be transferred to the output, depending on the device the input pulse might go through and generate an output pulse or it might not go through and therefore not generating an output pulse. For input pulses with pulse width smaller than 30 ns the output pulse is kept to 30 ns, then the response will be linear (shifted by the propagation delay). This is diagram is illustrative only with typical value. Actual value and pulse width distortion is subject to process variation. Output pulse width could in some case be shortened or extended to prevent retoggling. See propagation delay parameter footnote.

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Table 8 Table 2 Output pulse width vs input pulse width

Input pulse width	Output pulse width
Smaller than 20 ns	• In the case the driver is capable to transfer the pulse, the output pulse width is 30 ns • In case the driver is not capable of responding the output pulse is 0 ns
Between 20 ns and 30 ns	• The output pulse width is 30 ns
Above 30 ns	• The output pulse width is equal to input pulse width

6.7 Bootstrap capacitor design

The bootstrap capacitor is used to power the floating driver of the high side MOSFET. Therefore it has to provide the surge current and the charge to turn on the high side MOSFET. Normally a criteria to choose the minimum necessary boot capacitor is based on the gate charge of the high side and allowed ripple voltage across the boot capacitor, according to the following formula:

$$C_{BOOTmin} \geq \frac{Q_G}{\Delta V} \quad (2)$$

Where Q_G is the gate charge of the high side MOSFET and ΔV is the desired ripple voltage. Normally a rule of thumb for the ripple voltage is to have it smaller than 10% than the bootstrap voltage. This is a simplified formula which does not consider the leakage current of the floating driver, the bootstrap diode forward voltage but it is correct for most of the applications.

There is also an upper limit in the selection of the capacitor since a too big capacitor would lead to higher charging time which could result in startup issues due to the UVLO triggering. This problem can arise if the switching frequency is very high and therefore the time to charge the bootstrap is too short. For this kind of issues there is not a clear formula to apply, but some generic rules can be considered compatible with the $C_{BOOTmin}$ calculation:

- The higher the switching frequency the smaller should be the bootstrap capacitor
- The higher the MOSFET $RDS_{(ON)}$ the smaller should be the bootstrap capacitor
- The higher the V_{DD} the smaller should be the bootstrap capacitor (considering a fixed ripple voltage percentage)

6.8 Anti-shoot through protection

In order to prevent conditions where the high side MOSFET and the low side MOSFET are turned on at the same time an anti-shoot through logic is implemented with an addition of 3 ns deadtime. In other words the first input detected high, for instance HI will set the HO output high, meanwhile the LI will be inhibited until the HI input will not expire, then LI signal will be passed with additional 3 ns deadtime safety.

This logic prevents the HI and LI to be driven by the same signal. In this case the internal logic will select the “first” pulse coming in (depending on the specific parasitic of the device, the selection of the “first” signal might change) and inhibit the “second”. This logic is not suitable for driving parallel MOSFET with HO and LO.

6.9 Layout recommendations

The combination of the driver and MOSFETs forms the power trains of the converter. The relative location on the PCB of those two components together with the input capacitor is essential to reach high level of performance. The parasitic inductances of the PCB and of the power devices’ packaging (both upper and lower MOSFETs) can cause serious efficiency degradation due to dynamic effects. Careful layout can help minimize such unwanted effects. The following advices are meant to lead to an optimized layout:

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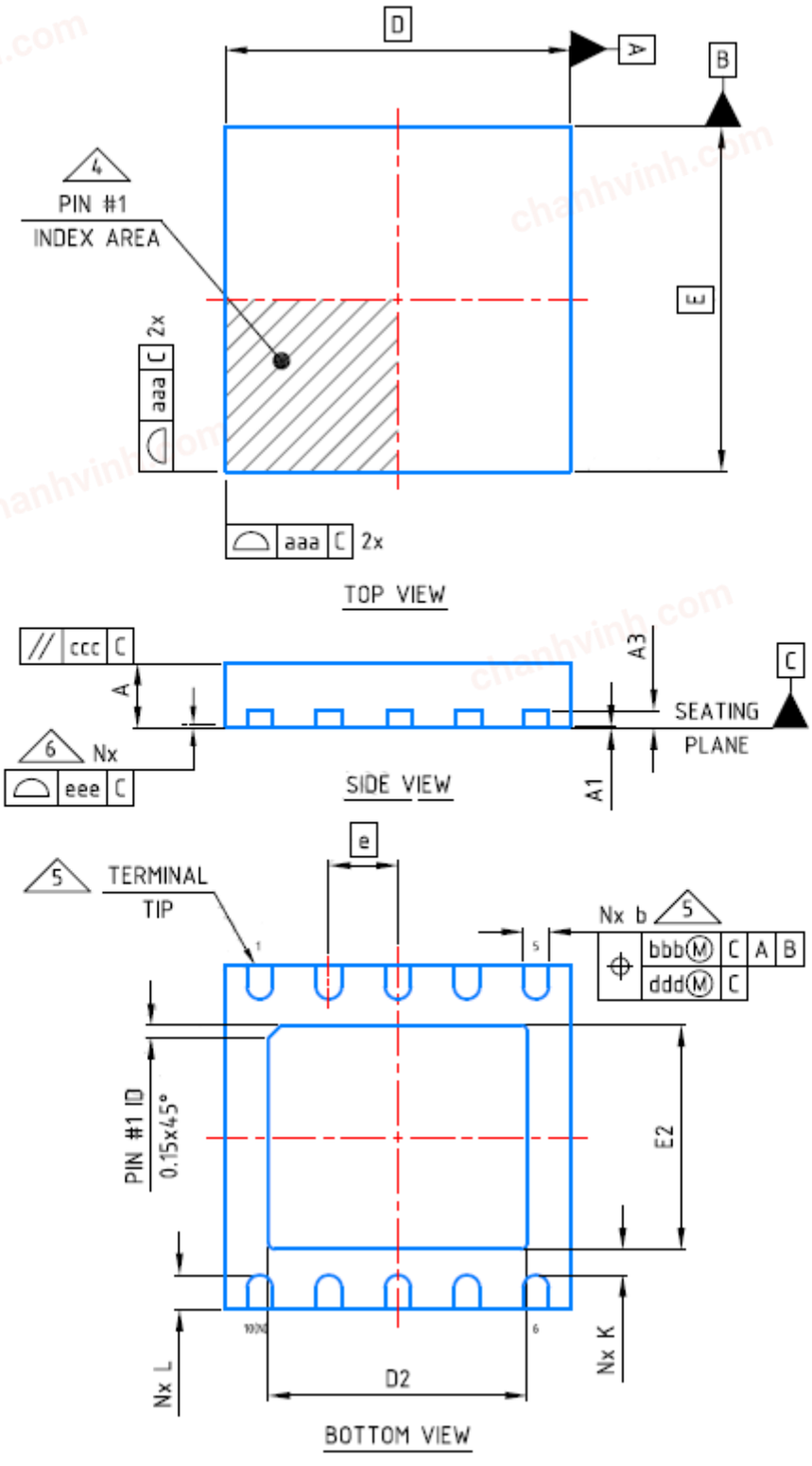
6 Functional description

1. Keep decoupling loops (VDD-GND and HB-HS) as short as possible
2. Minimize trace inductance, especially on low impedance lines. All power traces (HO, HS, LO, PGND, VDD) should be short and wide, as much as possible
3. The HS node should also be short and wide. Minimize the distance between the HS node and both the high side MOSFET source and the low side MOSFET drain to avoid efficiency losses minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible
4. To optimize heat spreading, copper should be placed directly underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried copper plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes for heat spreading allows the IC to achieve its full thermal potential

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7 Package information

7.1 Outline dimensions



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7 Package information

Dimension Table				
Thickness / Symbol	W			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref.	---	
b	0.25	0.30	0.35	5
D	4.00 BSC			
E	4.00 BSC			
e	0.80 BSC			
D2	2.85	3.00	3.10	
E2	2.45	2.60	2.70	
K	0.20	---	---	
L	0.30	0.40	0.50	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	10			3
ND	5			7
NOTES	1, 2			
LF DWG. NO.	CSM7/13/2016-001			

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.

2. All dimensions are in millimeters.

3. N is the total number of terminals.

4. The location of the marked terminal #1 identifier is within the hatched area.

5. Dimension b applies to the metallized terminal and is measured from 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.

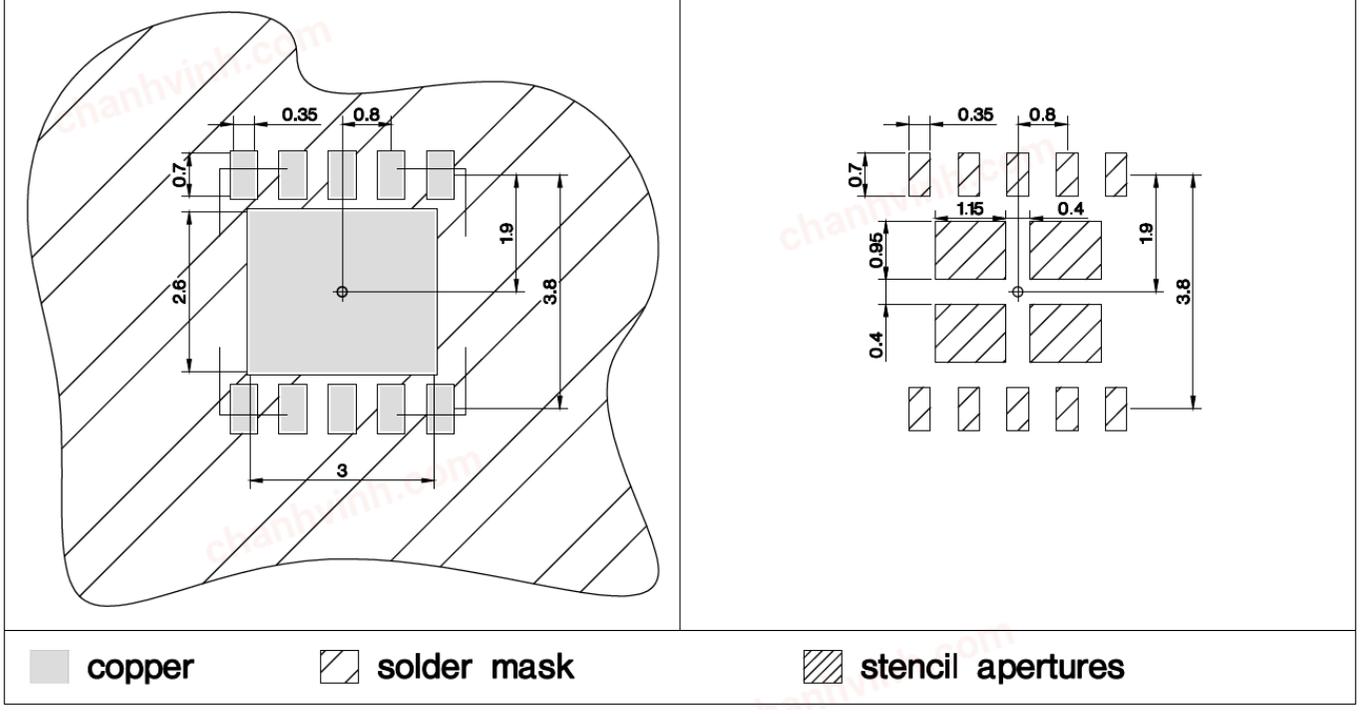
6. Coplanarity applies to the terminals and all other bottom surface metallization.

7. ND refers to the maximum number of terminals on D side.

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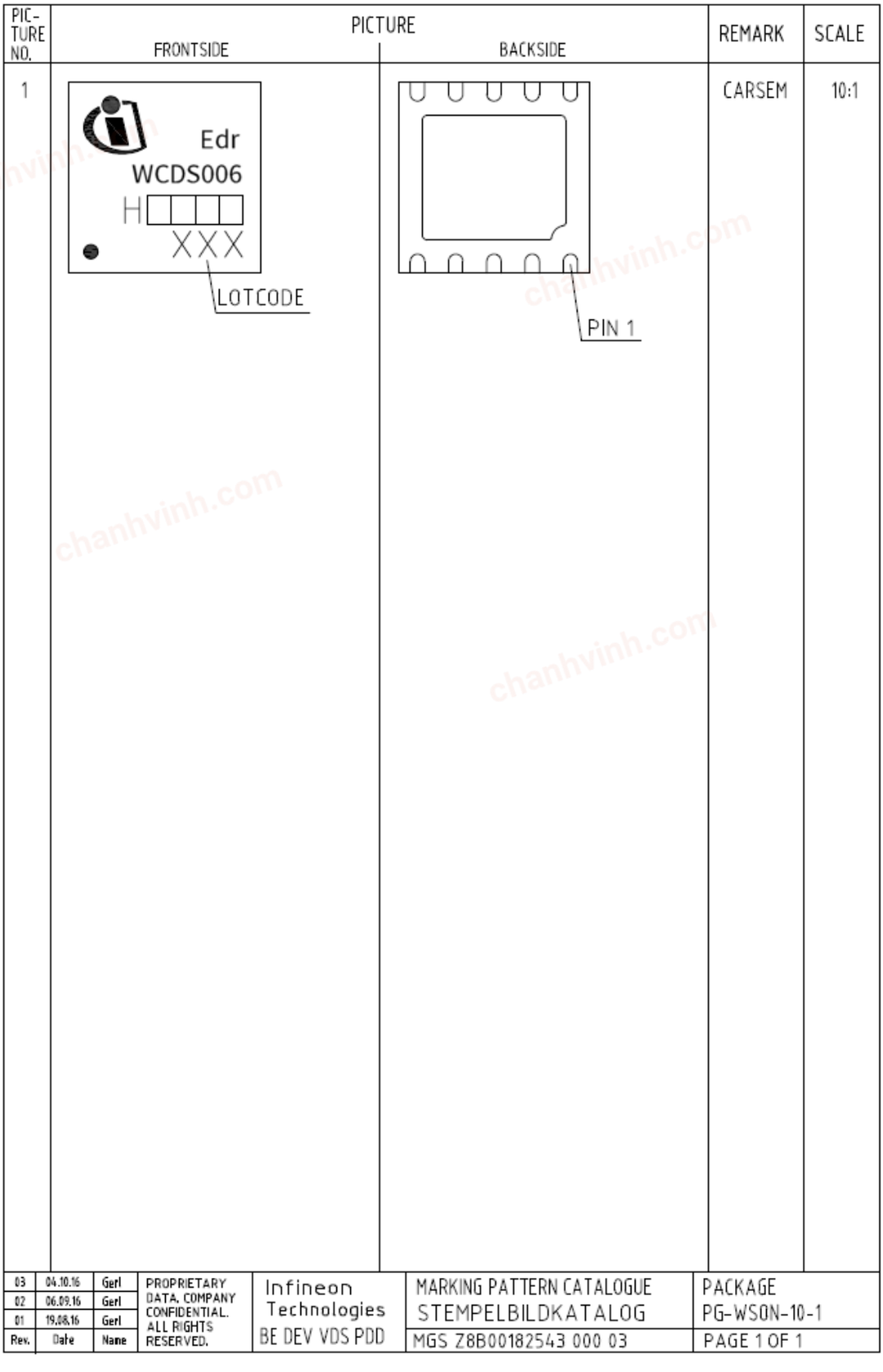
7.2 Boardpads and apertures

PG-WSON-10-1: Boardpads & Apertures



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7.3 Marking code



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8 References

1. Infineon, *Understanding the transient detector*, Infineon Technologies AG, Neubiberg 2020

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Revision history

Document version	Date of release	Description of changes
V2.2	2020-05-28	• Update of typical value of *DELM* in ***Dynamic electrical characteristics*** • ***Typical characteristics*** added
V2.1	2020-04-22	• Update to new template
V2.0	2019-09-17	• Initial release

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Edition 2020-05-28

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-ykn1580889052252

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