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Low Dropout Linear Voltage Regulator

TLS850D0TE

TLS850D0TEV50

TLS850D0TEV33

Linear Voltage Regulator

Data Sheet

Rev. 1.0, 2016-10-07

Automotive Power

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1 Overview

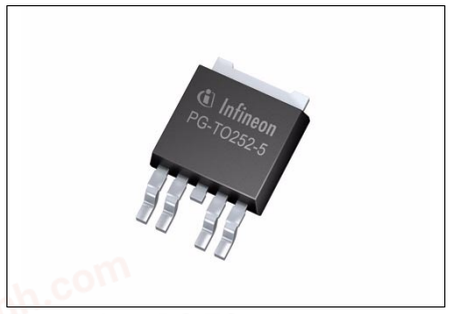


Figure 1 PG-TO252-5

Features

- Wide Input Voltage Range from 3.0 V to 40 V
- Fixed Output Voltage 5 V or 3.3 V
- Output Voltage Precision ≤ ±2 %
- Output Current Capability up to 500 mA
- Ultra Low Current Consumption typ. 40 µA
- Very Low Dropout Voltage typ. 70 mV @100 mA
- Stable with Ceramic Output Capacitor of 1 µF
- Delayed Reset at Power-On: 16.5 ms
- Enable, Undervoltage Reset, Overtemperature Shutdown
- Output Current Limitation
- Wide Temperature Range
- Green Product (RoHS compliant)
- AEC Qualified

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Functional Description

The TLS850D0TE is a high performance very low dropout linear voltage regulator for 5 V (TLS850D0V50) or 3.3 V (TLS850D0V33) supply in a PG-TO252-5 package.

With an input voltage range of 3 V to 40 V and very low quiescent of only 40 µA, these regulators are perfectly suitable for automotive or any other supply systems connected to the battery permanently. The TLS850D0TE provides an output voltage accuracy of 2 % and a maximum output current up to 500 mA.

The new loop concept combines fast regulation and very good stability while requiring only one small ceramic capacitor of 1 µF at the output. At currents below 100 mA the device will have a very low typical dropout voltage of only 70 mV (for 5 V device) and 80 mV (for 3.3 V device). The operating range starts already at input voltages of only 3 V (extended operating range). This makes the TLS850D0TE also suitable to supply automotive systems that need to operate during cranking condition.

The device can be switched on and off by the Enable feature as described in **Chapter 5.5**.

The output voltage is supervised by the Reset feature, including Undervoltage Reset and delayed Reset at Power-On, more details can be found in **Chapter 5.7**.

Internal protection features like output current limitation and overtemperature shutdown are implemented to protect the device against immediate damage due to failures like output short circuit to GND, over-current and over-temperatures.

Choosing External Components

An input capacitor C_I is recommended to compensate line influences. The output capacitor C_Q is necessary for the stability of the regulating circuit. TLS850D0TE is designed to be also stable with low ESR ceramic capacitors.

Type	Package	Marking
TLS850D0TEV50	PG-TO252-5	850D0V50
TLS850D0TEV33	PG-TO252-5	850D0V33

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2 Block Diagram

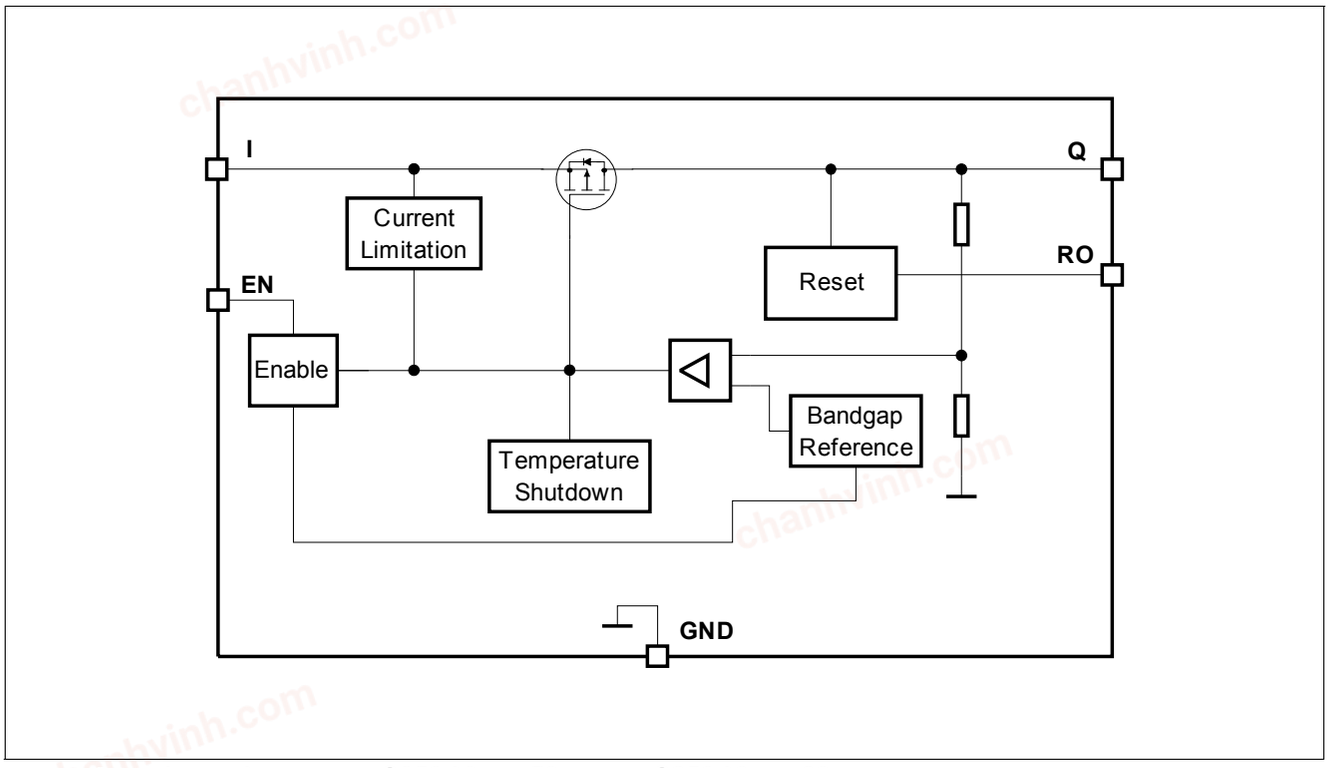


Figure 2 Block Diagram TLS850D0TEV50 and TLS850D0TEV33

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3 Pin Configuration

3.1 Pin Assignment TLS850D0TEV50 and TLS850D0TEV33

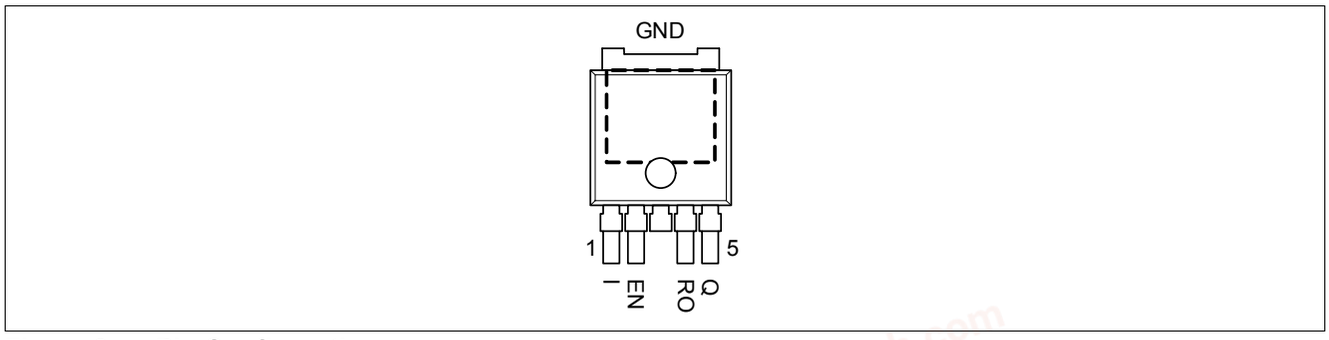


Figure 3 Pin Configuration

3.2 Pin Definitions and Functions TLS850D0TEV50 and TLS850D0TEV33

Pin	Symbol	Function
1	I	**Input** It is recommended to place a small ceramic capacitor (e.g. 100 nF) to GND, close to the IC terminals, in order to compensate line influences. See also **Chapter 6.2.1**
2	EN	**Enable** (integrated pull-down resistor) Enable the IC with high level input signal; Disable the IC with low level input signal;
3	GND	**Ground**
4	RO	**Reset Output** (intergrated pull-up resistor to Q) Open collector output; Leave open if the reset function is not needed
5	Q	**Output Voltage** Connect output capacitor C_Q to GND close to the IC's terminals, respecting the values specified for its capacitance and ESR in **"Functional Range" on Page 8**
Heat Slug	GND	**Heat Slug** Connect to GND Connect to heatsink area;

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4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input I, Enable EN							
Voltage	V_I, V_{EN}	-0.3	–	45	V	–	P_4.1.1
Output Q, Reset Output RO							
Voltage	V_Q, V_{RO}	-0.3	–	7	V	–	P_4.1.3
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.7
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.8
ESD Absorption							
ESD Susceptibility to GND	V_{ESD}	-2	–	2	kV	2) HBM	P_4.1.9
ESD Susceptibility to GND	V_{ESD}	-500	–	500	V	3) CDM	P_4.1.10
ESD Susceptibility Pin 1, 5 (corner pins) to GND	$V_{ESD1,5}$	-750	–	750	V	3) CDM	P_4.1.13

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Note:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

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4.2 Functional Range

Table 2 Functional Range

T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage Range	V_I	$V_{Q,nom}$ + V_{dr}	–	40	V	1) –	P_4.2.1
Extended Input Voltage Range	$V_{I,ext}$	3.0	–	40	V	2) –	P_4.2.3
Enable Voltage Range	V_{EN}	0	–	40	V	–	P_4.2.5
Output Capacitor's Requirements for Stability	C_Q	1	–	–	µF	3)4) –	P_4.2.6
ESR	$ESR(C_Q)$	–	–	100	Ω	3) –	P_4.2.7
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.9

1) Output current is limited internaly and depends on the input voltage, see Electrical Characteristics for more details.
2) When V_I is between $V_{I,ext,min}$ and $V_{Q,nom}$ + V_{dr}, V_Q = V_I - V_{dr}. When V_I is below $V_{I,ext,min}$, V_Q can drop down to 0 V.
3) Not subject to production test, specified by design.
4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

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4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Package Version PG-TO252-5							
Junction to Case	R_{thJC}	–	3	–	K/W	1) –	P_4.3.11
Junction to Ambient	R_{thJA}	–	26	–	K/W	1)2) 2s2p board	P_4.3.12
Junction to Ambient	R_{thJA}	–	109	–	K/W	1)3) 1s0p board, footprint only	P_4.3.13
Junction to Ambient	R_{thJA}	–	51	–	K/W	1)3) 1s0p board, 300 mm^2 heatsink area on PCB	P_4.3.14
Junction to Ambient	R_{thJA}	–	40	–	K/W	1)3) 1s0p board, 600 mm^2 heatsink area on PCB	P_4.3.15

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

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5 Block Description and Electrical Characteristics

5.1 Voltage Regulation

The output voltage V_Q is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and the pass transistor is driven accordingly.

The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the internal circuit design. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor (ESR) requirements given in **"Functional Range" on Page 8** have to be maintained. For details, also see the typical performance graph **"Output Capacitor Series Resistor ESR(CQ) versus Output Current IQ" on Page 15**. As the output capacitor also has to buffer load steps, it should be sized according to the application's needs.

An input capacitor C_I is recommended to compensate line influences. In order to block influences like pulses and HF distortion at input side, an additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the component's terminals.

In order to prevent overshoots during start-up, a smooth ramp up function is implemented. This ensures almost no output voltage overshoots during start-up, mostly independent from load and output capacitance.

Whenever the load current exceeds the specified limit, e.g. in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuit) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC's lifetime.

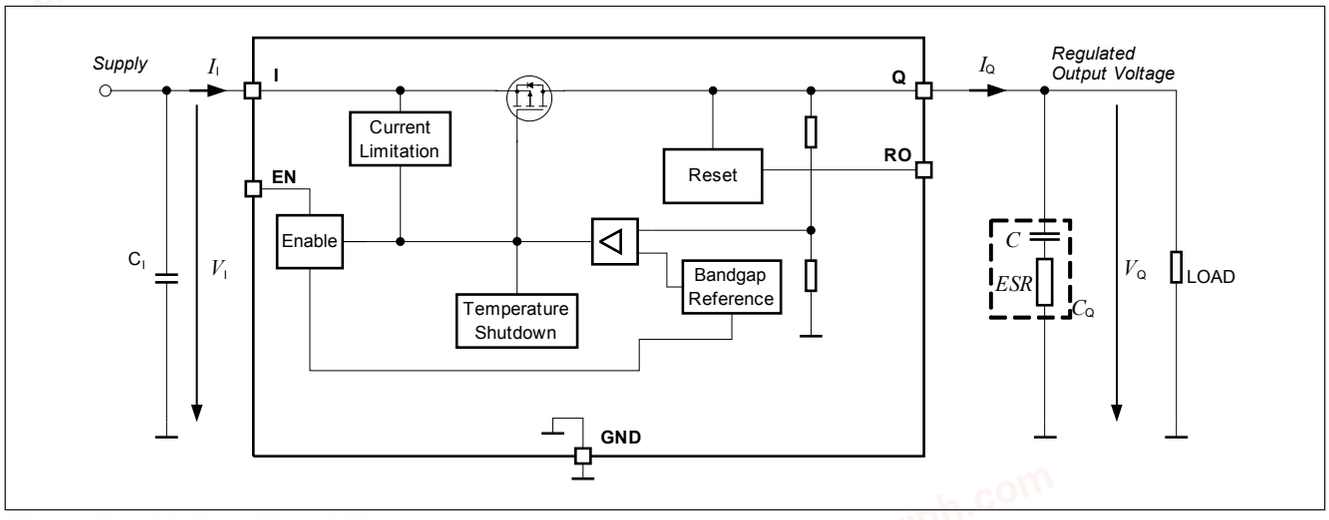


Figure 4 Voltage Regulation

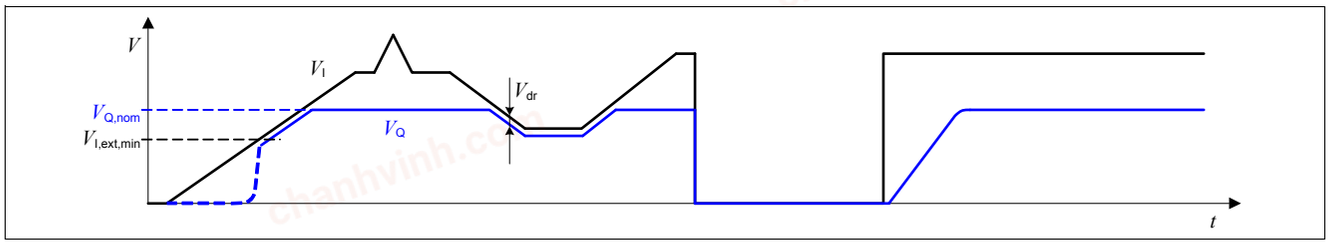


Figure 5 Output Voltage vs. Input Voltage

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Table 4 Electrical Characteristics Voltage Regulator 5 V version

T_j = -40 °C to +150 °C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage Precision	V_Q	4.9	5.0	5.1	V	0.05 mA < I_Q < 500 mA 5.95 V < V_I < 28 V	P_5.1.3
Output Voltage Precision	V_Q	4.9	5.0	5.1	V	0.05 mA < I_Q < 200 mA 5.44 V < V_I < 40 V	P_5.1.4
Output Voltage Start-up slew rate	dV_Q/dt	3.0	7.5	18	V/ms	V_I > 18 V/ms C_Q = 1 µF 0.5 V < V_Q < 4.5 V	P_5.1.7
Output Current Limitation	$I_{Q,max}$	501	650	1100	mA	0 V < V_Q < 4.8 V	P_5.1.9
Load Regulation steady-state	$\Delta V_{Q,load}$	-20	-1.5	5	mV	I_Q = 0.05 mA to 500 mA V_I = 6 V	P_5.1.11
Line Regulation steady-state	$\Delta V_{Q,line}$	-20	0	20	mV	V_I = 8 V to 32 V I_Q = 5 mA	P_5.1.13
Dropout Voltage V_{dr} = V_I - V_Q	V_{dr}	–	175	425	mV	1) I_Q = 250 mA	P_5.1.16
Dropout Voltage V_{dr} = V_I - V_Q	V_{dr}	–	70	170	mV	1) I_Q = 100 mA	P_5.1.17
Power Supply Ripple Rejection	$PSRR$	–	59	–	dB	2) f_{ripple} = 100 Hz V_{ripple} = 0.5 Vpp	P_5.1.18
Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	°C	2) T_j increasing	P_5.1.19
Overtemperature Shutdown Threshold Hysteresis	$T_{j,sdh}$	–	15	–	K	2) T_j decreasing	P_5.1.20

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5V

2) Not subject to production test, specified by design

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Table 5 Electrical Characteristics Voltage Regulator 3.3 V version

T_j = -40 °C to +150 °C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage Precision	V_Q	3.23	3.3	3.37	V	0.05 mA < I_Q < 500 mA 4.23 V < V_I < 28 V	P_5.1.23
Output Voltage Precision	V_Q	3.23	3.3	3.37	V	0.05 mA < I_Q < 200 mA 3.72 V < V_I < 40 V	P_5.1.24
Output Voltage Start-up slew rate	dV_Q/dt	3.0	7.5	18	V/ms	V_I > 18 V/ms C_Q = 1 µF 0.33 V < V_Q < 2.97 V	P_5.1.27
Output Current Limitation	$I_{Q,max}$	501	650	1100	mA	0 V < V_Q < 3.1 V	P_5.1.29
Load Regulation steady-state	$\Delta V_{Q,load}$	-20	-1.5	5	mV	I_Q = 0.05 mA to 500 mA V_I = 6 V	P_5.1.31
Line Regulation steady-state	$\Delta V_{Q,line}$	-15	0	15	mV	V_I = 8 V to 32 V I_Q = 5 mA	P_5.1.33
Dropout Voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	200	430	mV	1) I_Q = 250 mA	P_5.1.36
Dropout Voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	80	175	mV	1) I_Q = 100 mA	P_5.1.37
Power Supply Ripple Rejection	$PSRR$	–	63	–	dB	2) f_{ripple} = 100 Hz V_{ripple} = 0.5 Vpp	P_5.1.38
Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	°C	2) T_j increasing	P_5.1.39
Overtemperature Shutdown Threshold Hysteresis	$T_{j,sdh}$	–	15	–	K	2) T_j decreasing	P_5.1.40

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5V

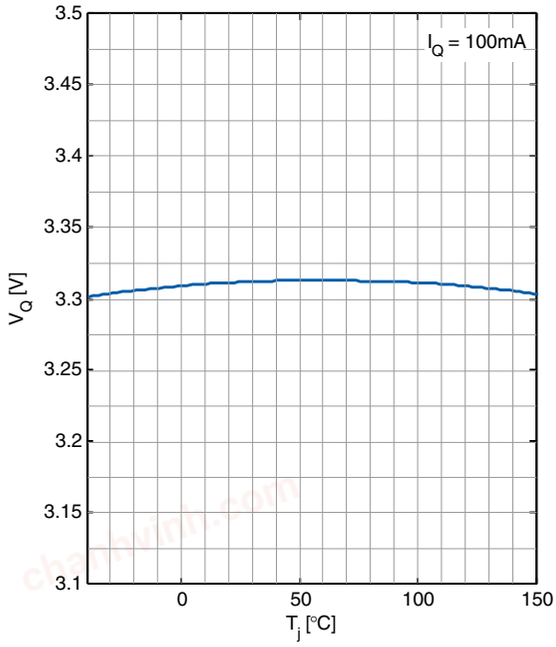
2) Not subject to production test, specified by design

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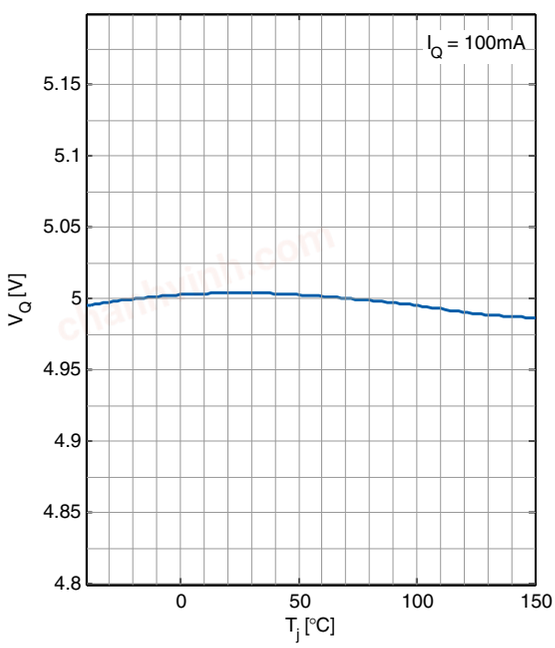
5.2 Typical Performance Characteristics Voltage Regulator

Typical Performance Characteristics

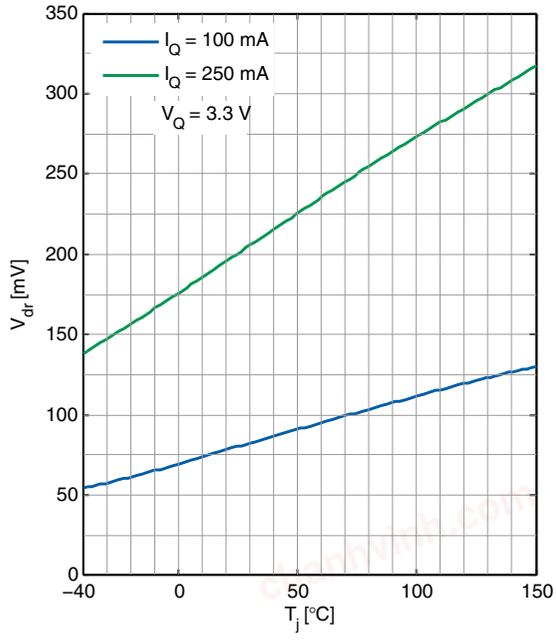
Output Voltage V_Q versus Junction Temperature T_j (3.3 V version)



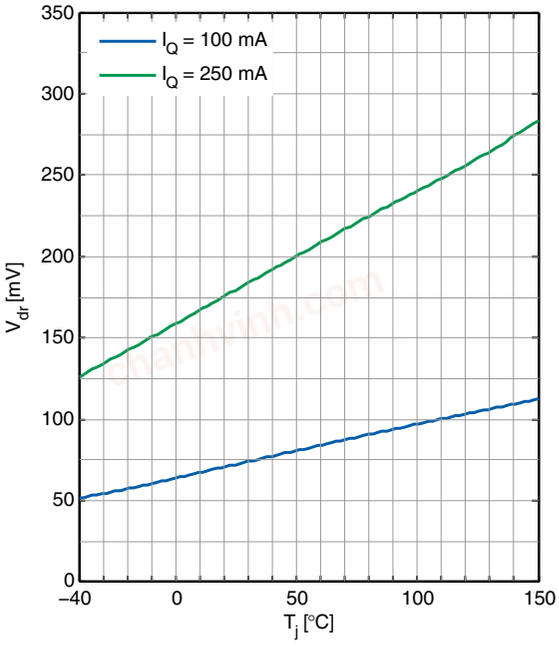
Output Voltage V_Q versus Junction Temperature T_j (5 V version)



Dropout Voltage V_{dr} versus Junction Temperature T_j (3.3 V version)

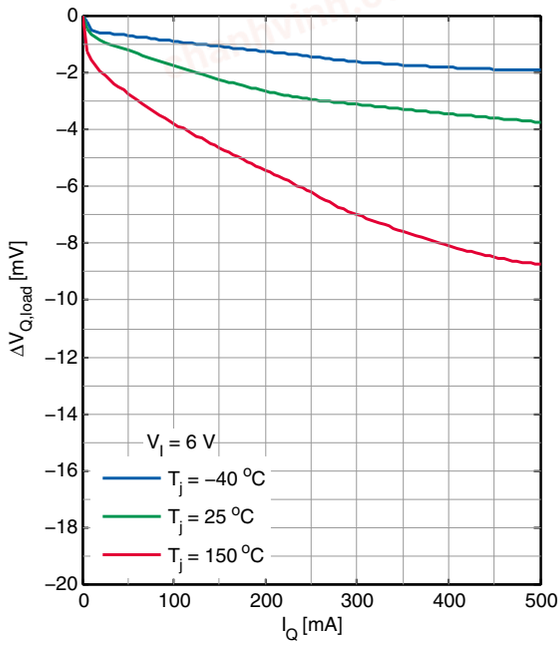


Dropout Voltage V_{dr} versus Junction Temperature T_j (5 V version)

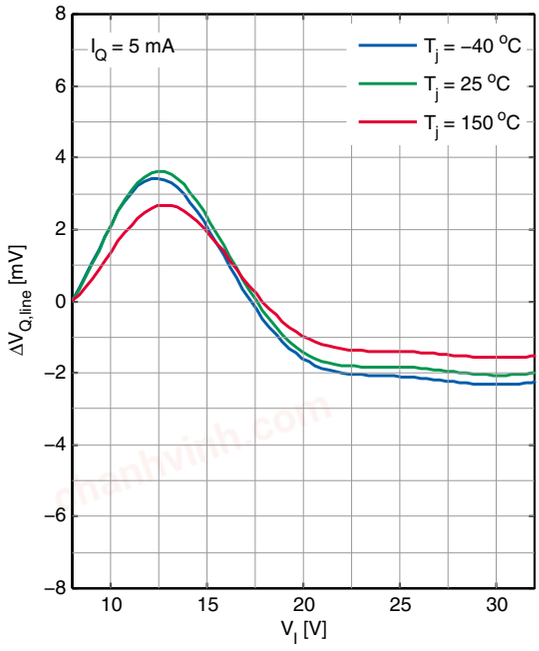


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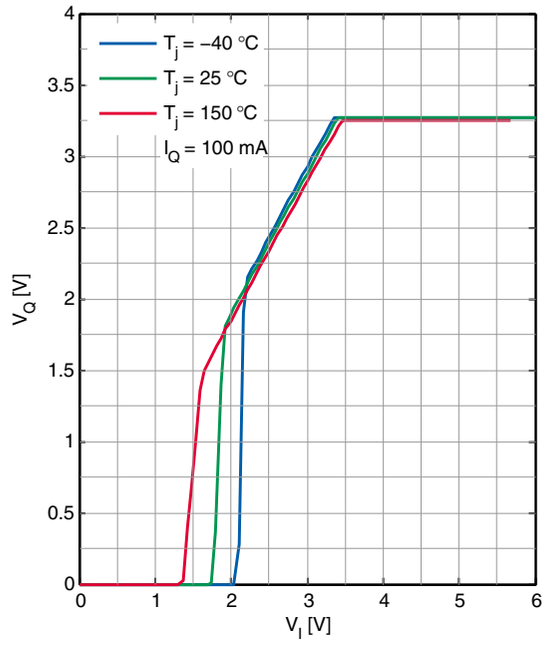
Load Regulation $\Delta V_{Q,load}$ versus Output Current Change I_Q



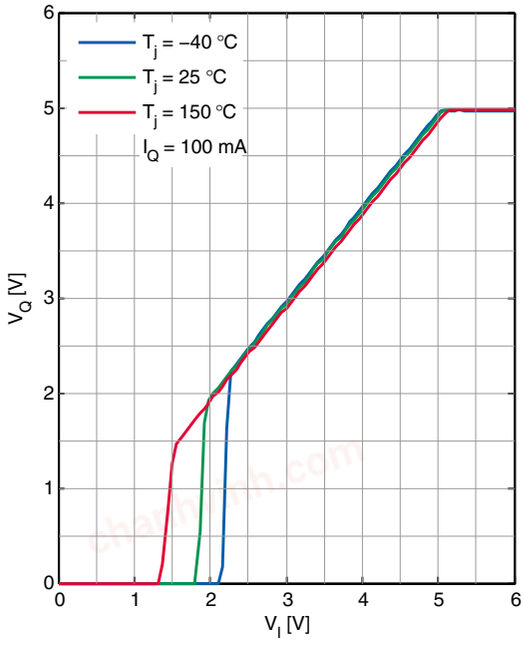
Line Regulation $\Delta V_{Q,line}$ versus Input Voltage V_I



Output Voltage V_Q versus Input Voltage V_I (3.3 V version)

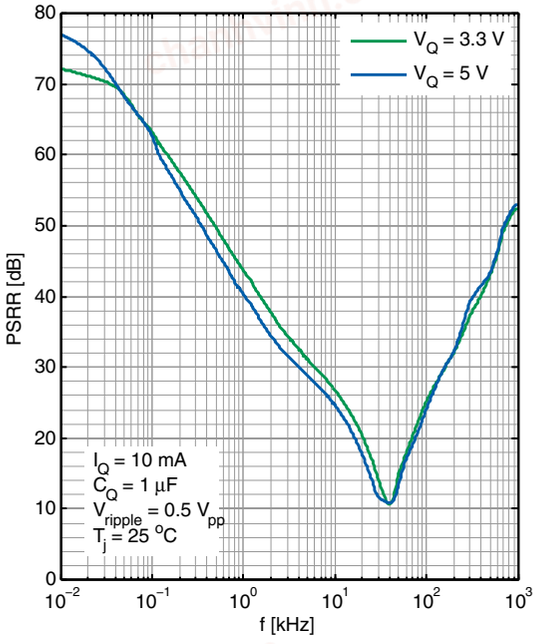


Output Voltage V_Q versus Input Voltage V_I (5 V version)

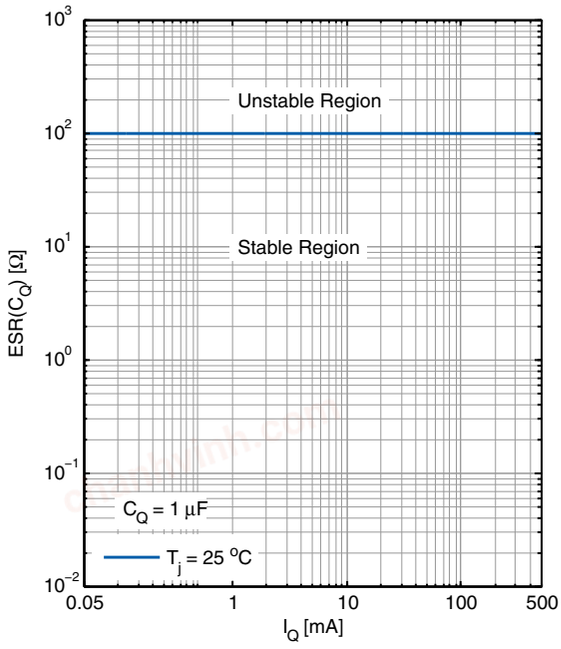


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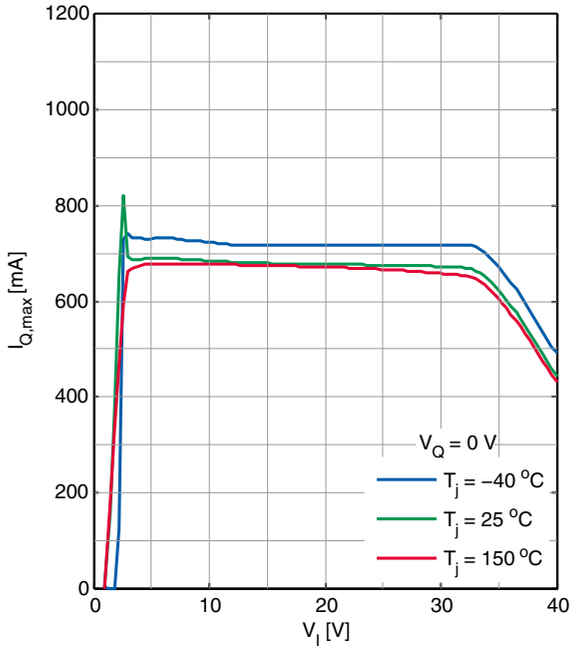
Power Supply Ripple Rejection $PSRR$ versus ripple frequency f



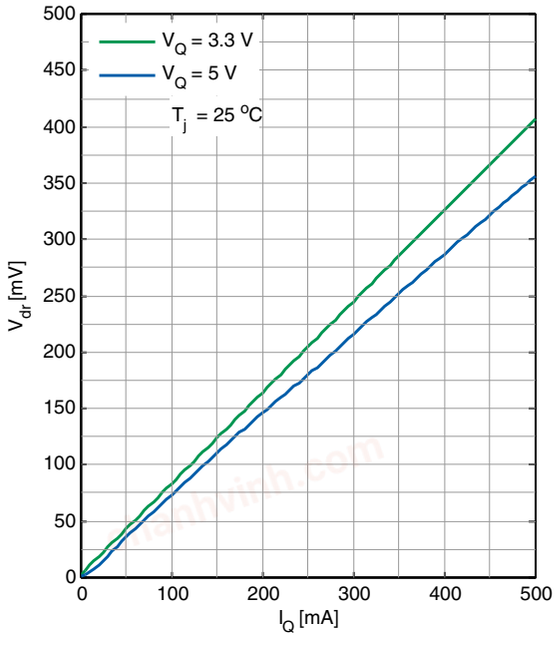
Output Capacitor Series Resistor $ESR(C_Q)$ versus Output Current I_Q



Maximum Output Current I_Q versus Input Voltage V_I



Dropout Voltage V_{dr} versus Output Current I_Q



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5.3 Current Consumption

Table 6 Electrical Characteristics Current Consumption

T_j = -40 °C to +150 °C, V_I = 13.5 V (unless otherwise specified)
Typical values are given at T_j = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption $I_q = I_I$	$I_{q,off}$	–	1.3	5	µA	V_{EN} = 0 V; T_j < 105 °C	P_5.3.1
Current Consumption $I_q = I_I$	$I_{q,off}$	–	–	8	µA	V_{EN} = 0.4 V; T_j < 125 °C	P_5.3.3
Current Consumption $I_q = I_I - I_Q$	I_q	–	40	52	µA	I_Q = 0.05 mA T_j = 25 °C	P_5.3.4
Current Consumption $I_q = I_I - I_Q$	I_q	–	62	77	µA	I_Q = 0.05 mA T_j < 125 °C	P_5.3.7
Current Consumption $I_q = I_I - I_Q$	I_q	–	62	82	µA	[1] I_Q = 500 mA T_j < 125 °C	P_5.3.11

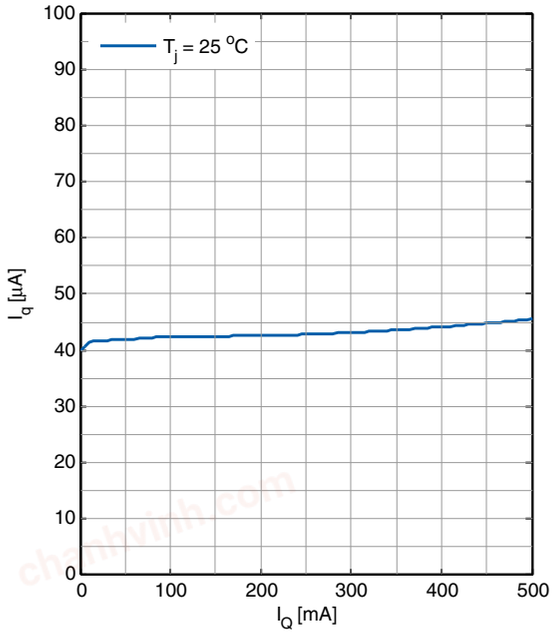
1) Not subject to production test, specified by design

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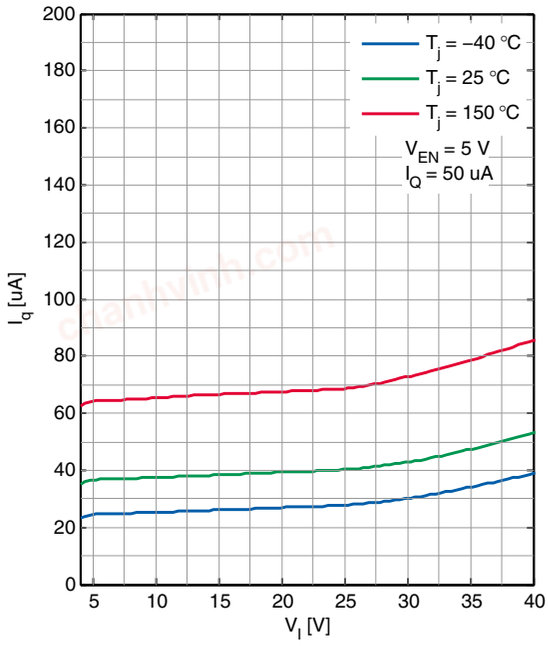
5.4 Typical Performance Characteristics Current Consumption

Typical Performance Characteristics

Current Consumption I_q versus Output Current I_Q



Current Consumption I_q versus Input Voltage V_I



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5.5 Enable

The TLS850D0TE can be switched on and off by the Enable feature: Connect a HIGH level as specified below (e.g. the battery voltage) to pin EN to enable the device; connect a LOW level as specified below (e.g. GND) to shut it down. The enable has a built in hysteresis to avoid toggling between ON/OFF state, if signals with slow slopes are applied to the EN input.

Table 7 Electrical Characteristics Enable

T_j = -40 °C to +150 °C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

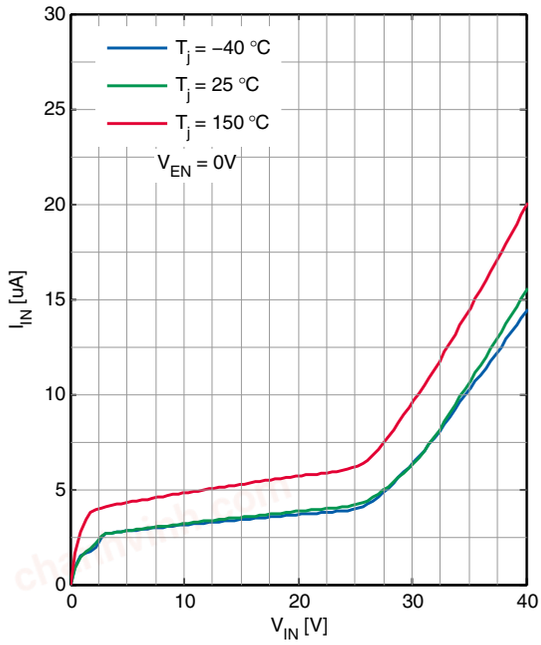
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
High Level Input Voltage	$V_{EN,H}$	2	–	–	V	V_Q settled	P_5.5.1
Low Level Input Voltage	$V_{EN,L}$	–	–	0.8	V	V_Q ≤ 0.1 V	P_5.5.2
Enable Threshold Hysteresis	$V_{EN,Hy}$	100	–	–	mV	–	P_5.5.3
High Level Input Current	$I_{EN,H}$	–	–	3.5	µA	V_{EN} = 3.3 V	P_5.5.4
High Level Input Current	$I_{EN,H}$	–	–	22	µA	V_{EN} ≤ 18 V	P_5.5.6
Enable internal pull-down resistor	R_{EN}	0.95	1.5	2.6	MΩ	–	P_5.5.7

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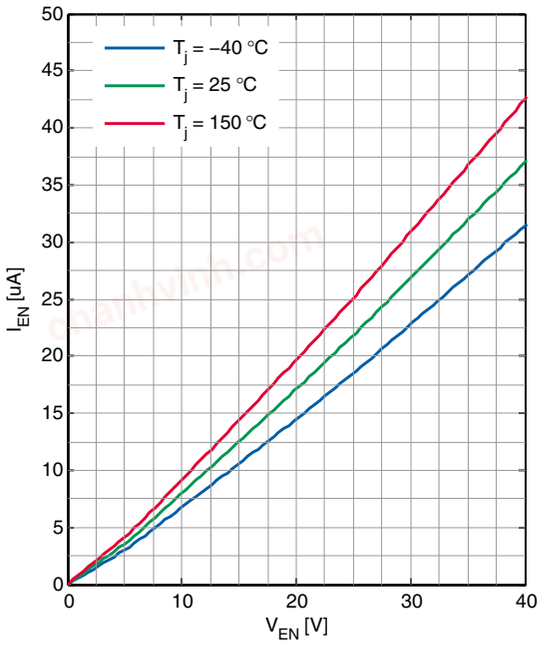
5.6 Typical Performance Characteristics Enable

Typical Performance Characteristics

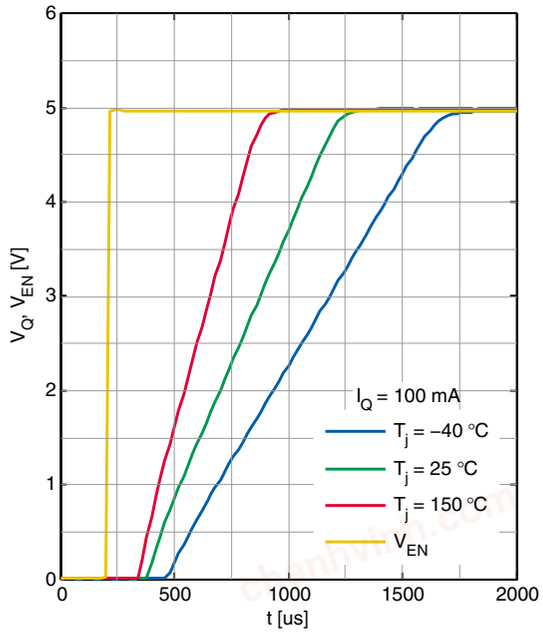
Input Current I_{IN} versus Input Voltage V_{IN} (condition: V_{EN} = 0 V)



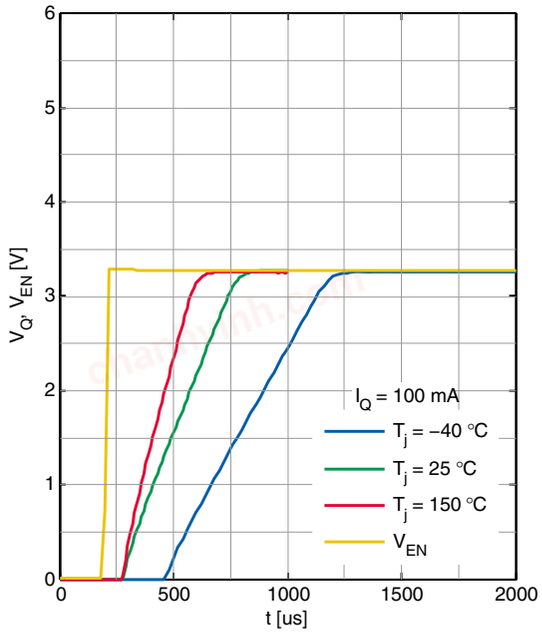
Enabled Input Current I_{EN} versus Enabled Input Voltage V_{EN}



Output Voltage V_Q versus time (EN switched ON, 5 V version)



Output Voltage V_Q versus time (EN switched ON, 3.3 V version)



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5.7 Reset

The TLS850D0TE's output voltage is supervised by the Reset feature, including Undervoltage Reset and delayed Reset at Power-On.

The Undervoltage Reset function sets the pin RO to LOW, in case V_Q is falling for any reason below the Reset Threshold $V_{RT,low}$.

When the regulator is powered on, the pin RO is held at LOW for the duration of the Power-On Reset Delay Time t_{rd}.

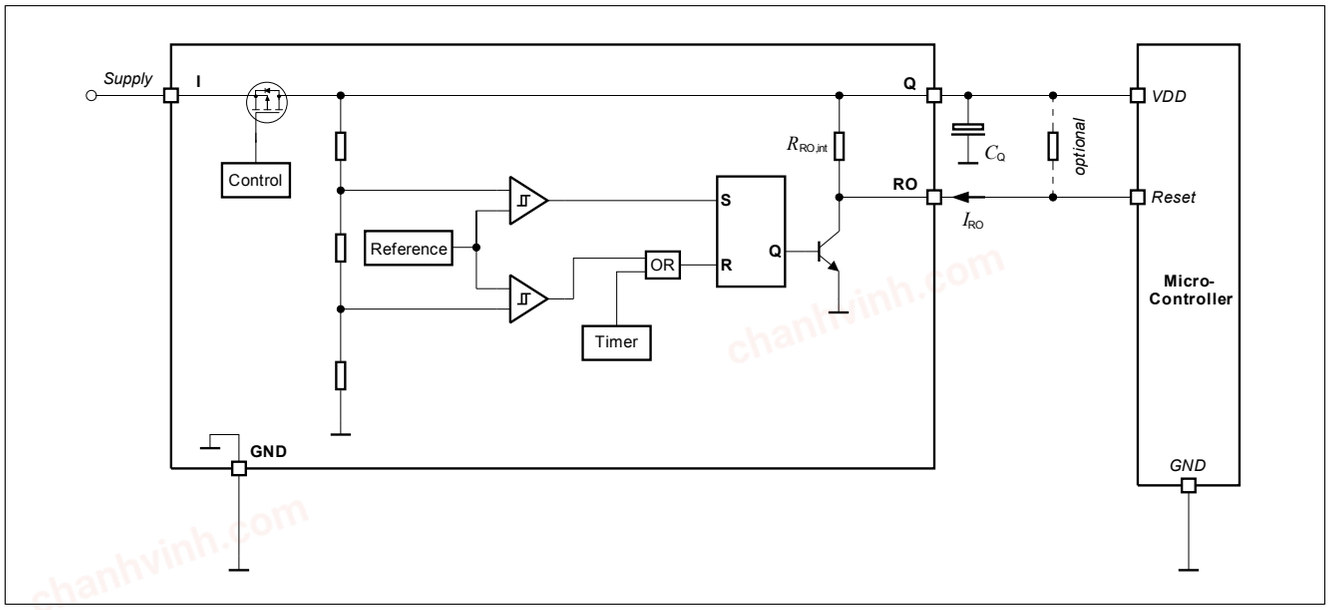


Figure 6 Block Diagram Reset Circuit

Reset Delay Time

The Reset Delay Time t_{rd} is fix defined according to **Table 8**.

Table 8 Reset DelayTime

Reset delay timing	t_{rd}
fix	16.5 ms

Power-On Reset Delay Time

The power-on reset delay time is defined by the parameter t_{rd} and allows a microcontroller and oscillator to start up. This delay time is the time period from exceeding the upper reset switching threshold $V_{RT,high}$ until the reset is released by switching the reset output "RO" from "LOW" to "HIGH".

Undervoltage Reset Delay Time

Unlike the power-on reset delay time, the undervoltage reset delay time is defined by the parameter t_{rd} and considers an output undervoltage event where the output voltage V_Q trigger the $V_{RT,low}$ threshold.

Reset Blanking Time

The reset blanking time $t_{rr,blank}$ avoids that short undervoltage spikes trigger an unwanted reset "low" signal.

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Reset Reaction Time

In case the output voltage of the regulator drops below the output undervoltage lower reset threshold $V_{RT,low}$, the reset output “RO” is set to low, after the delay of the internal reset reaction time $t_{rr,int}$. The reset blanking time $t_{rr,blank}$ is part of the reset reaction time $t_{rr,int}$.

Reset Output “RO”

The reset output “RO” is an open collector output with an integrated pull-up resistor. In case a lower-ohmic “RO” signal is desired, an external pull-up resistor can be connected to the output “Q”. Since the maximum “RO” sink current is limited, the minimum value of the optional external resistor “$R_{RO,ext}$” is given in **Table “Reset Output RO” on Page 22**.

Reset Output “RO” Low for VQ ≥ 1 V

In case of an undervoltage reset condition reset output “RO” is held “low” for V_Q ≥ 1 V, even if the input “I” is not supplied and the voltage V_I drops below 1 V. This is achieved by supplying the reset circuit from the output capacitor.

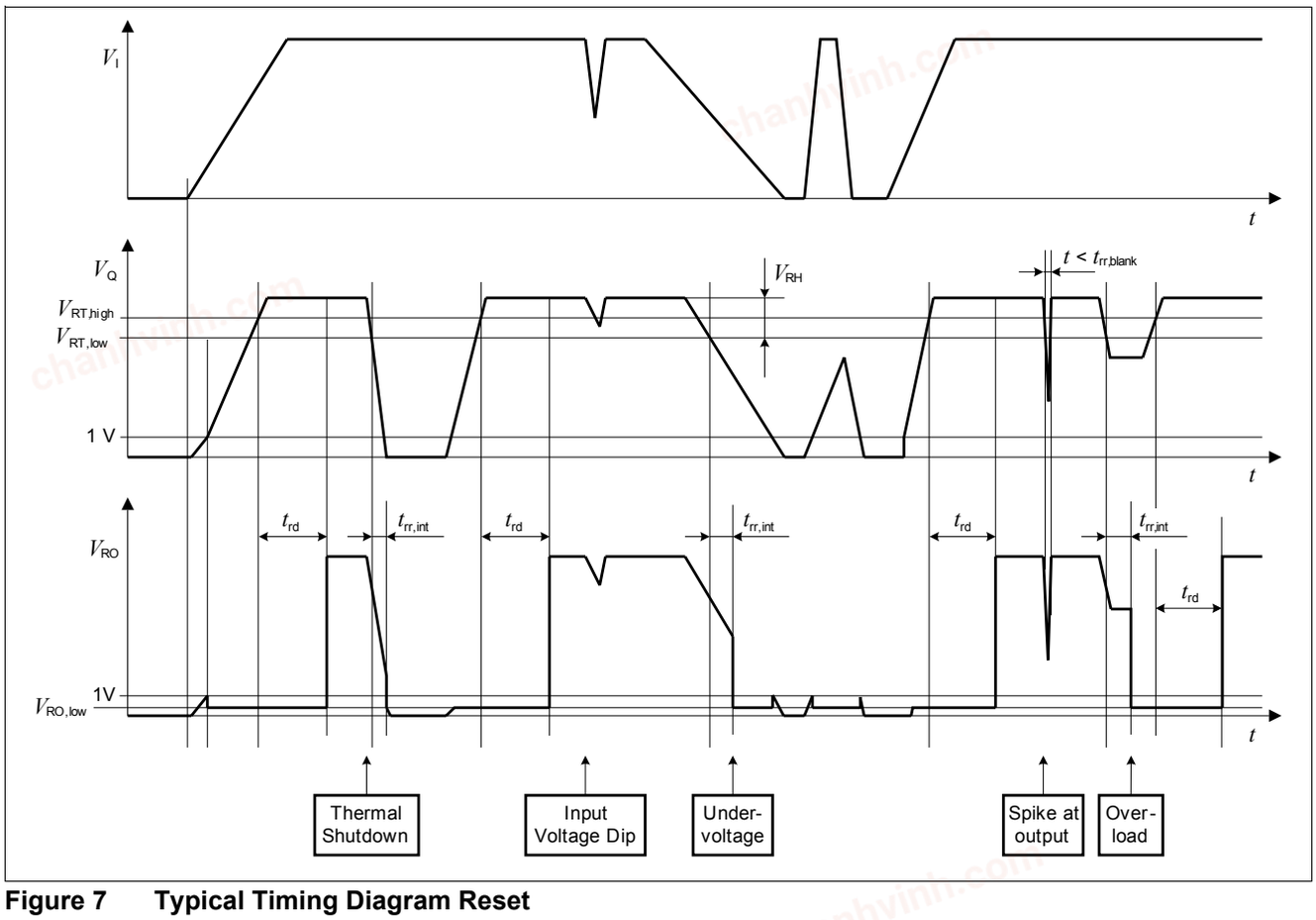


Figure 7 Typical Timing Diagram Reset

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Table 9 Electrical Characteristics Reset

T_j = -40 °C to +150 °C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Undervoltage Reset 5V Version only							
Output Undervoltage Reset Upper Switching Threshold	$V_{RT,high}$	4.6	4.7	4.8	V	V_Q increasing	P_5.7.1
Output Undervoltage Reset Lower Switching Threshold - Default	$V_{RT,low}$	4.5	4.6	4.7	V	V_Q decreasing	P_5.7.2
Output Undervoltage Reset Switching Hysteresis	$V_{RT,hy}$	60	100	–	mV	–	P_5.7.3
Output Undervoltage Reset Headroom V_Q - V_{RT}	V_{RH}	200	400	–	mV	–	P_5.7.4
Output Undervoltage Reset 3V3 Version only							
Output Undervoltage Reset Upper Switching Threshold	$V_{RT,high}$	3.08	3.15	3.22	V	V_Q increasing	P_5.7.5
Output Undervoltage Reset Lower Switching Threshold - Default	$V_{RT,low}$	3.0	3.05	3.13	V	V_Q decreasing	P_5.7.6
Output Undervoltage Reset Switching Hysteresis	$V_{RT,hy}$	60	100	–	mV	–	P_5.7.7
Output Undervoltage Reset Headroom V_Q - V_{RT}	V_{RH}	100	250	–	mV	–	P_5.7.8
Reset Output RO							
Reset Output Low Voltage	$V_{RO,low}$	–	0.2	0.4	V	1 V ≤ V_Q ≤ V_{RT}; R_{RO} ≥ 5.1 kΩ	P_5.7.40
Reset Output Internal Pull-Up Resistor	$R_{RO,int}$	13	20	36	kΩ	internally connected to Q	P_5.7.41
Reset Output External Pull-up Resistor to V_Q	$R_{RO,ext}$	5.1	–	–	kΩ	1 V ≤ V_Q ≤ V_{RT} ; V_{RO} ≤ 0.4 V	P_5.7.42
Reset Delay Timing							
Reset Delay Time	t_{rd}	13.2	16.5	19.8	ms	Fixed Timing	P_5.7.44
Reset blanking time	$t_{rr,blank}$	–	6	–	µs	1) for $V_{Q,nom}$ = 3.3 V	P_5.7.22
Reset blanking time	$t_{rr,blank}$	–	7	–	µs	2) for $V_{Q,nom}$ = 5 V	P_5.7.46
Internal Reset Reaction Time	$t_{rr,int}$	–	7	20	µs	for $V_{Q,nom}$ = 3.3 V	P_5.7.23
Internal Reset Reaction Time	$t_{rr,int}$	–	10	33	µs	for $V_{Q,nom}$ = 5 V	P_5.7.36

1) Not subject to production test, specified by design.

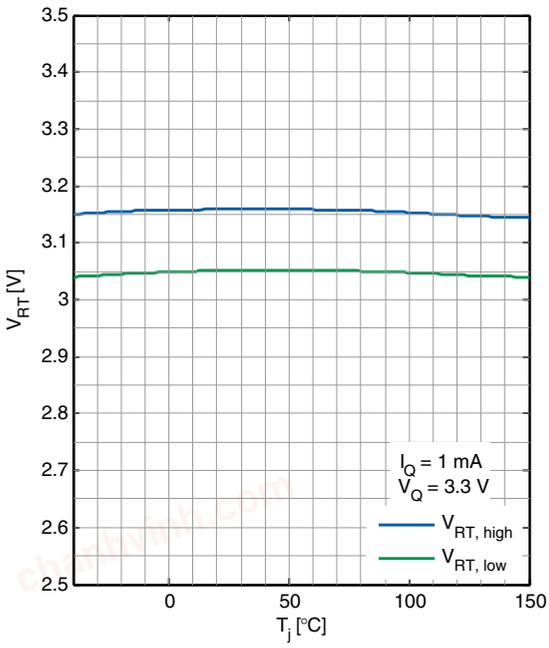
2) Not subject to production test, specified by design.

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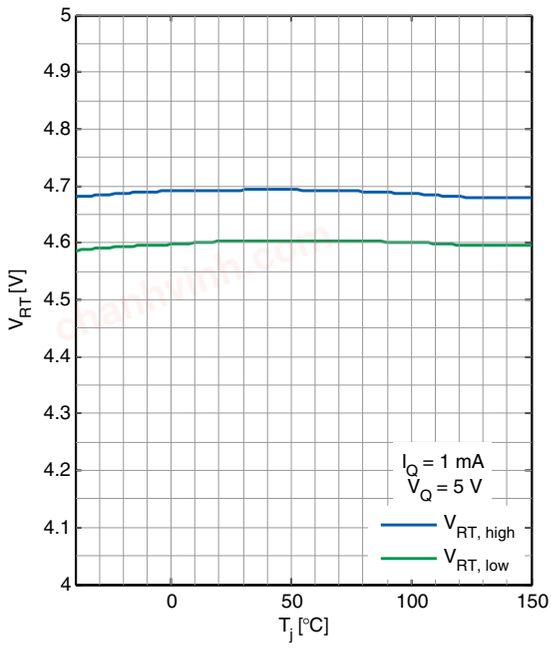
5.8 Typical Performance Characteristics Reset

Typical Performance Characteristics

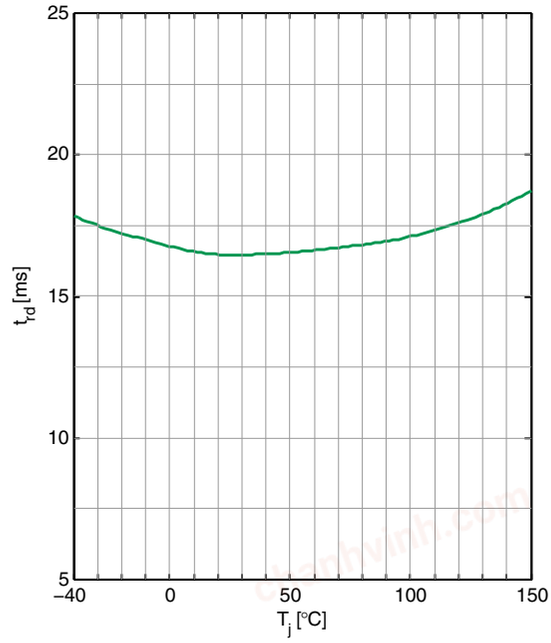
Undervoltage Reset Threshold V_{RT} versus Junction Temperature T_j (3.3 V version)



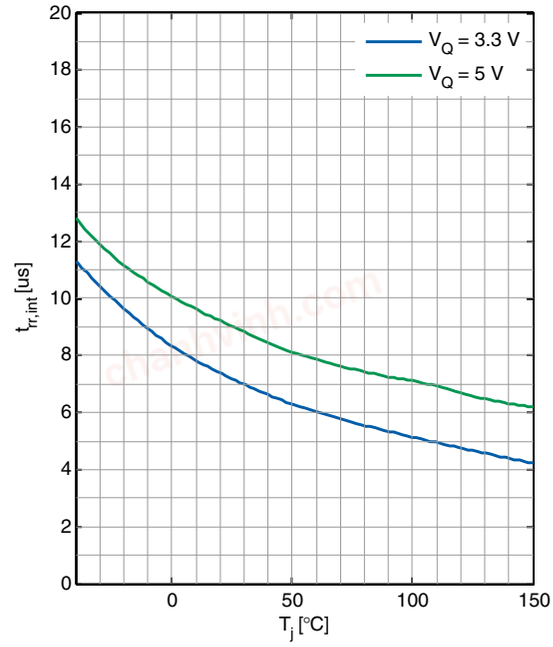
Undervoltage Reset Threshold V_{RT} versus Junction Temperature T_j (5 V version)



Power On Reset Delay Time t_{rd} versus Junction Temperature T_j



Internal Reset Reaction Time $t_{rr,int}$ versus Junction Temperature T_j



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6 Application Information

6.1 Application Diagram

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

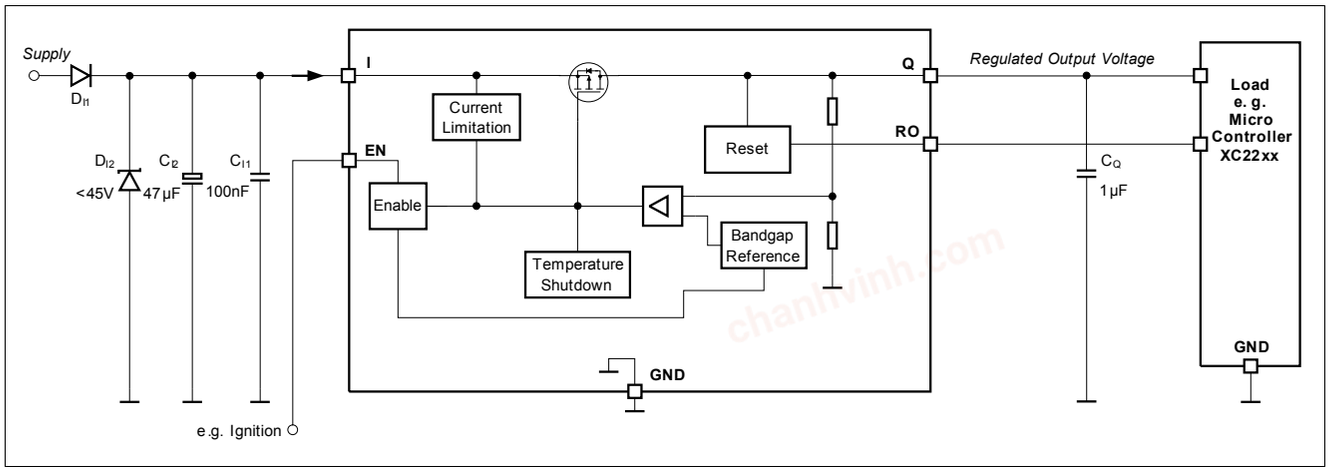


Figure 8 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

6.2 Selection of External Components

6.2.1 Input Pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

6.2.2 Output Pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **“Functional Range” on Page 8**. The graph **“Output Capacitor Series Resistor ESR(CQ) versus Output Current IQ” on Page 15** shows the stable operation range of the device.

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TLS850D0TE is designed to be also stable with low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

6.3 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (1)$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **"Thermal Resistance" on Page 9**.

Example

Application conditions:

V_I = 13.5 V

V_Q = 5 V

I_Q = 175 mA

T_a = 85 °C

Calculation of $R_{thJA,max}$:

$P_D = (V_I – V_Q) \times I_Q + V_I \times I_q$ ($V_I \times I_q$ can be neglected because of very low I_q)

= (13.5 V – 5 V) × 175 mA

= 1.487 W

$R_{thJA,max} = (T_{j,max} – T_a) / P_D$

= (150 °C – 85 °C) / 1.487 W = 43.71 K/W

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As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 43.71 K/W. According to **“Thermal Resistance” on Page 9**, at least 600 mm^2 heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used to ensure a proper cooling for the TLS850D0TE in package.

6.4 Reverse Polarity Protection

TLS850D0TE is not self protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is needed. The absolute maximum ratings of the device as specified in **“Absolute Maximum Ratings” on Page 7** must be kept.

6.5 Further Application Information

- For further information you may contact **http://www.infineon.com/**

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7 Package Outlines

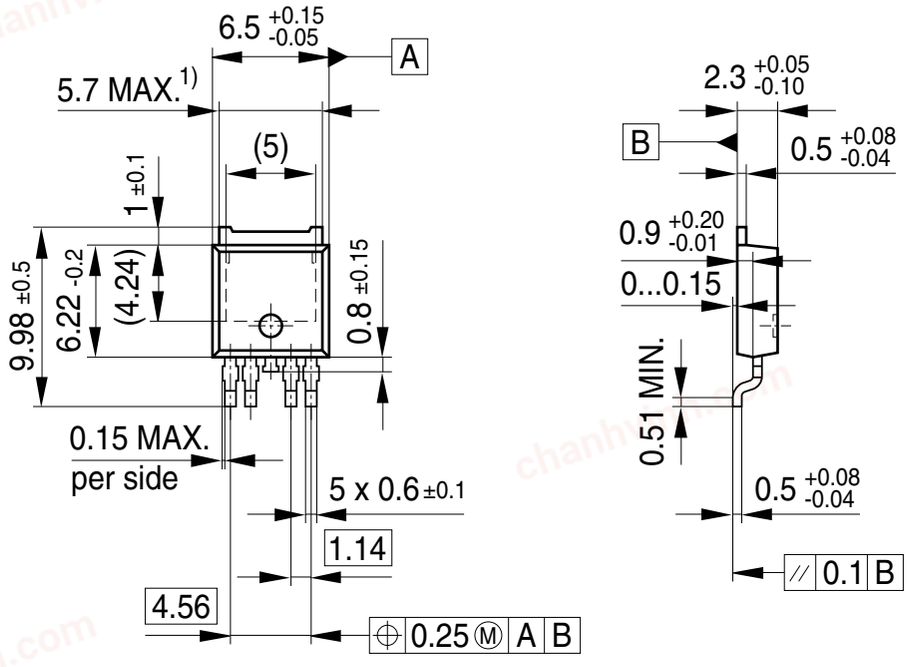


Figure 9 PG-TO252-5

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

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8 Revision History

Revision	Date	Changes
1.0	2016-10-07	Data Sheet - Initial version

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