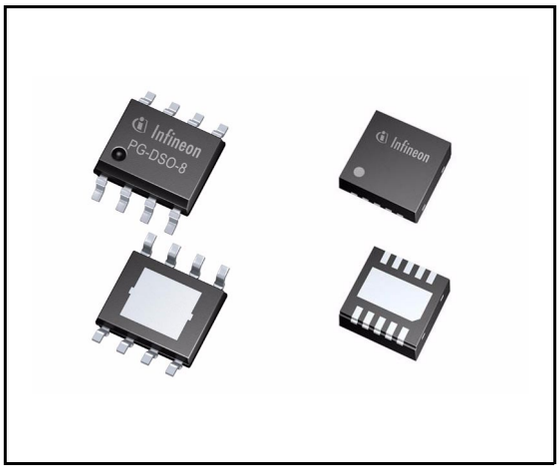
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OPTIREG™ Linear TLS115D0

High Precision Voltage Tracker

AEC Qualified

RoHS



Features

- 150 mA current capability
- Very high accuracy voltage tracking
- Output voltage adjustable down to 2.0 V
- Stable with ceramic output capacitors
- Very low dropout voltage
- Very low current consumption in OFF mode
- Power Good output indicates overvoltage and undervoltage
- Internally controlled soft start
- Wide input voltage range: -16 V ≤ V_{IN} ≤ 45 V
- Wide temperature range: -40°C ≤ T_j ≤ 150°C
- Short circuit protected output (to GND and to battery)
- Reverse polarity protected input
- Overtemperature protection
- Green Product (RoHS compliant)
- AEC Qualified

Applications

- Automotive sensor supply
- Protected sensor supply for off-board sensors
- Secondary voltage supply in automotive ECU
- High-precision voltage tracking
- Precision voltage replication
- Power switch for off-board load

Description

The OPTIREG™ Linear TLS115D0 is a monolithic integrated low-dropout voltage tracking regulator with high accuracy in small PG-DSO-8 exposed pad and PG-TSON-10 packages. The TLS115D0 is designed to supply off-board systems, for example sensors in powertrain management systems under the severe conditions of automotive applications. Therefore, the TLS115D0 is equipped with protection functions against reverse polarity and against short circuit to GND and battery.

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Up to a supply voltage of 45 V and output currents up to 150 mA, the output voltage follows the reference voltage that is applied to the ADJ input with very high accuracy. The required minimum reference voltage at ADJ is 2.0 V.

Type	Package	Marking
TLS115D0EJ	PG-DSO-8 EP	115D0
TLS115D0LD	PG-TSON-10	115D0

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1 Block diagram

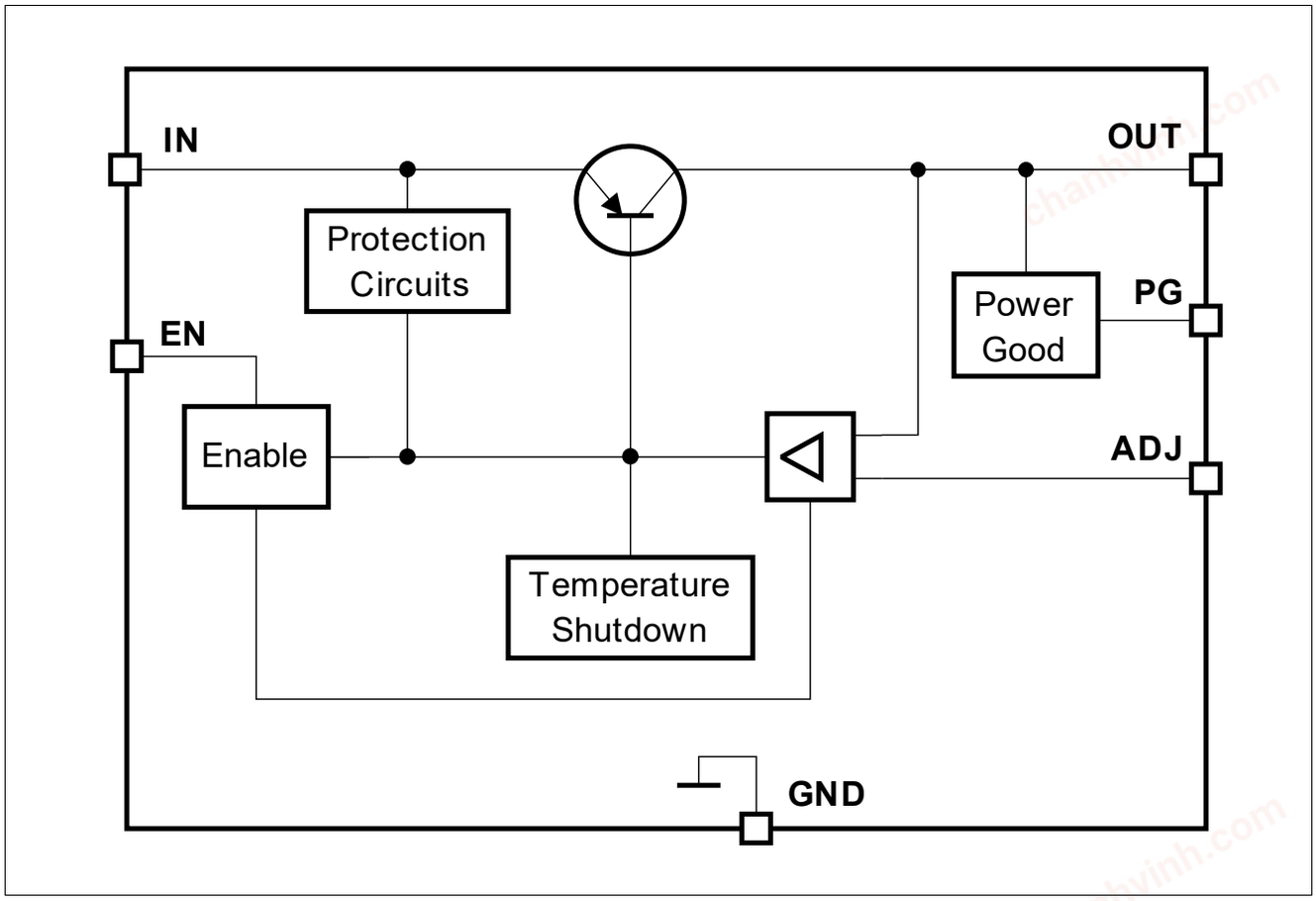


Figure 1 TLS115D0 block diagram

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2 Pin configuration

2.1 Pin assignment TLS115D0EJ in PG-DSO-8 EP package

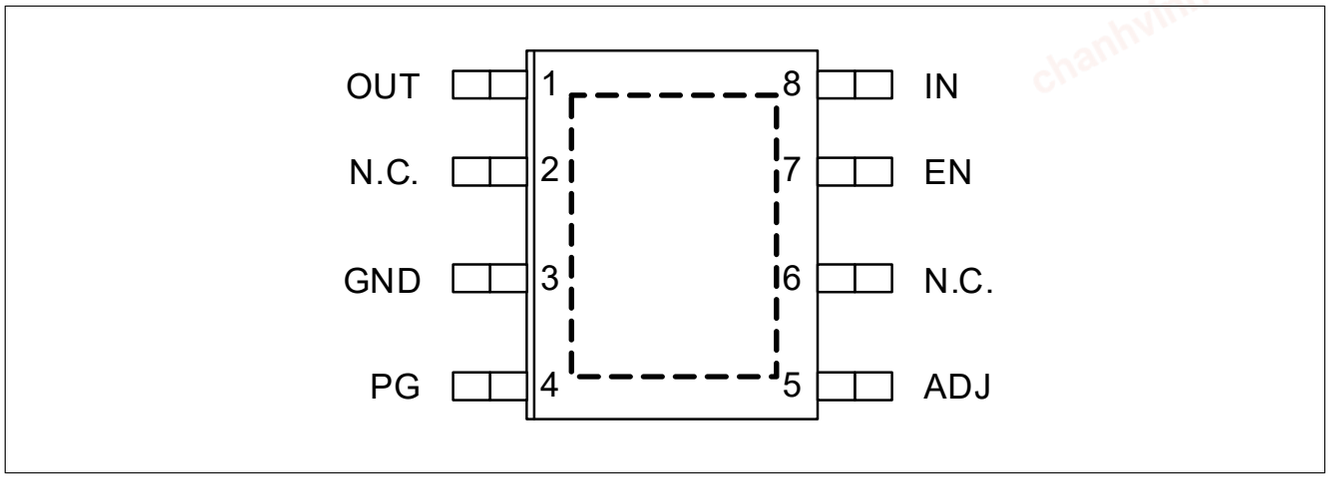


Figure 2 TLS115D0EJ pin Configuration

2.2 Pin definitions and functions TLS115D0EJ in PG-DSO-8 EP package

Pin	Symbol	Function
1	OUT	**Tracker output** 150 mA output current capability Connect to GND with a capacitor close to the pins, respecting capacitance and ESR requirements given in **Table 2 Functional range**.
2	N.C.	**Not connected**
3	GND	**Ground**
4	PG	**Power Good** Open collector output. Connect via a pull-up resistor to a positive voltage rail. A “low” signal indicates a fault condition of the tracker output.
5	ADJ	**Adjust** Connect to the reference voltage
6	N.C.	Not Connected
7	EN	**Enable input** “High” signal: enables the tracker “Low” signal: disables the tracker If the enable function is not required, then connect EN to IN.
8	IN	**Input** It is recommended to connect a small ceramic capacitor to GND close to the pins in order to compensate line influence.
Pad	–	Exposed Pad Connect to GND

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2.3 Pin assignment TLS115D0LD in PG-TSON-10 package

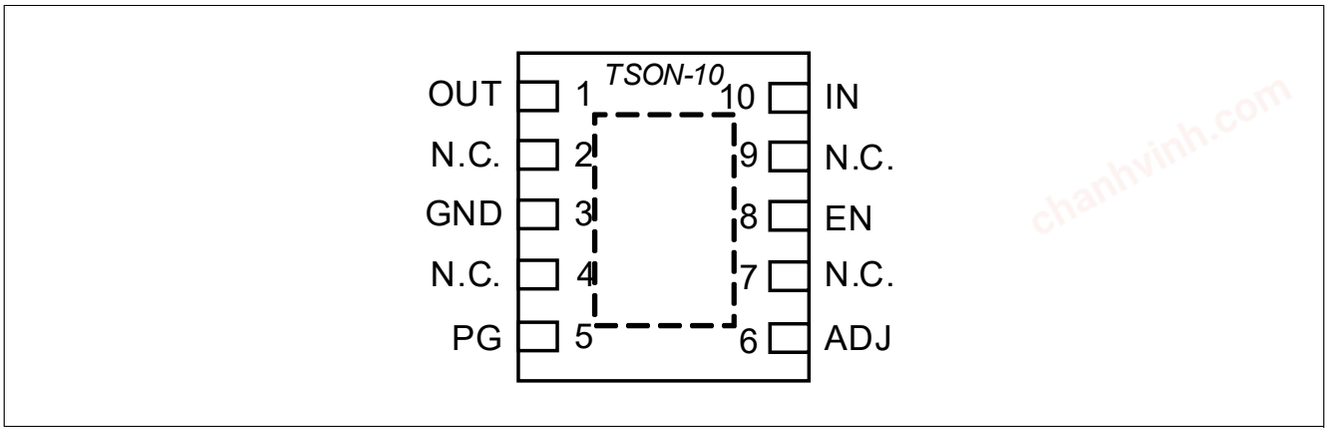


Figure 3 TLS115D0LD pin configuration

2.4 Pin definitions and functions TLS115D0LD in PG-TSON-10 package

Pin	Symbol	Function
1	OUT	**Tracker output** 150 mA output current capability Connect to GND with a capacitor close to the pins, respecting capacitance and ESR requirements given in **Table 2 Functional range**.
3	GND	**Ground**
5	PG	**Power Good** Open collector output. Connect via a pull-up resistor to a positive voltage rail. A “low” signal indicates a fault condition of the tracker output.
6	ADJ	**Adjust** Connect to the reference voltage
8	EN	**Enable input** “High” signal: enables the tracker “Low” signal: disables the tracker If the enable function is not required, then connect EN to IN.
10	IN	**Input** It is recommended to connect a small ceramic capacitor to GND close to the pins in order to compensate line influence.
2, 4, 7, 9	N.C.	**Not connected**
Pad	–	Exposed Pad Connect to GND

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3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input IN							
Voltage	V_{IN}	-16	–	45	V	–	P_3.1.1
Enable EN							
Voltage	V_{EN}	-16	–	45	V	–	P_3.1.2
Adjust ADJ							
Voltage	V_{ADJ}	-16	–	45	V	–	P_3.1.3
Output OUT							
Voltage	V_{OUT}	-5	–	45	V	–	P_3.1.4
Input Output Voltage Difference							
Voltage	V_{IN}-V_{OUT}	-30	–	45	V	–	P_3.1.5
Power Good PG							
Voltage	V_{PG}	-0.3	–	7	V	–	P_3.1.6
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_3.1.7
Storage temperature	T_{stg}	-55	–	150	°C	–	P_3.1.8
ESD Absorption							
ESD susceptibility to GND	$V_{ESD,HBM}$	-4	–	4	kV	Human Body Model (HBM)[2)]	P_3.1.9
ESD susceptibility to GND	$V_{ESD,CDM}$	-1	–	1	kV	Charge Device Model (CDM)[3)]	P_3.1.10
ESD susceptibility to GND	$V_{ESD,CDM}$	-1	–	1	kV	Charge Device Model (CDM) at corner pins[3)]	P_3.1.11

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

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3.2 Functional range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_{IN}	4	–	45	V	–	P_3.2.1
Adjust input voltage range (voltage tracking range)	V_{ADJ}	2	–	14	V	–	P_3.2.2
Output capacitor	C_{OUT}	1	–	–	µF	–[1)2)]	P_3.2.3
Output capacitor's Equivalent Series Resistance	ESR (C_{OUT})	–	–	5	Ω	–[2)]	P_3.2.4
Junction temperature	T_j	-40	–	150	°C	–[2)]	P_3.2.5

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
2) Not subject to production test, specified by design.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal resistance TLS115D0EJ in PG-DSO-8 EP package

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case[1)]	R_{thJC}	–	18	–	K/W	–	P_3.3.1
Junction to pin	R_{thJP}	–	85	–	K/W	–	P_3.3.2
Junction to ambient	R_{thJA}	–	50	–	K/W	2s2p board[2)]	P_3.3.3
Junction to ambient	R_{thJA}	–	157	–	K/W	1s0p board, footprint only[3)]	P_3.3.4
Junction to ambient	R_{thJA}	–	77	–	K/W	1s0p board, 300 mm² heatsink area on PCB[3)]	P_3.3.5
Junction to Ambient	R_{thJA}	–	63	–	K/W	1s0p board, 600 mm² heatsink area on PCB[3)]	P_3.3.6

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70 µm Cu).

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Table 4 Thermal resistance TLS115D0LD in PG-TSON-10 package

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case[1)]	R_{thJC}	–	17	–	K/W	–	P_3.3.7
Junction to pin	R_{thJP}	–	96	–	K/W	–	P_3.3.8
Junction to ambient	R_{thJA}	–	67	–	K/W	2s2p board[2)]	P_3.3.9
Junction to ambient	R_{thJA}	–	194	–	K/W	1s0p board, footprint only[3)]	P_3.3.10
Junction to ambient	R_{thJA}	–	82	–	K/W	1s0p board, 300 mm^2 heatsink area on PCB[3)]	P_3.3.11
Junction to ambient	R_{thJA}	–	68	–	K/W	1s0p board, 600 mm^2 heatsink area on PCB[3)]	P_3.3.12

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70 µm Cu).

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4 Block description and electrical characteristics

4.1 Tracking regulator

The regulator controls the output voltage V_{OUT} by comparing it to the voltage applied to the ADJ pin and driving a PNP pass transistor accordingly. The stability of the control loop depends on:

- the output capacitor C_{OUT}
- load current
- chip temperature
- the poles and zeroes in the frequency response of the circuit consisting of TLS115D0 and the load

An input capacitor C_{IN} is strongly recommended for buffering the line influence.

To ensure stable operation, the output capacitor's capacitance and its equivalent series resistance *ESR* requirements given in the table **"Functional range" on Page 8** must be maintained. For details see also the typical performance graph **"Output capacitor ESR(COUT) vs. output current IOUT" on Page 14**. The output capacitor must be sized suitably to buffer load transients.

Connect each capacitor close to the pins.

Protection circuitry prevents the TLS115D0 itself as well as the application from destruction in case of catastrophic events. These safeguards contain:

- output current limitation
- reverse polarity protection
- thermal shutdown

In order to protect the pass element and the package from excessive power dissipation the TLS115D0 reduces the maximum output current at high input voltage.

The TLS115D0 allows a negative supply voltage. However, in reverse polarity condition several low currents flowing into the TLS115D0 increase junction temperature. Thermal design must consider this effect, because in reverse polarity condition the overtemperature protection circuit does not operate.

The overtemperature protection circuit prevents immediate destruction of the TLS115D0 in certain fault conditions (for example a permanent short circuit at output) by switching off the power stage. After the chip cools down, the regulator restarts. If the fault is not removed, then this leads to an oscillatory behavior of the output voltage. Please note, that a junction temperature above 150°C is outside the maximum ratings and reduces the lifetime of the TLS115D0.

Table 5 Electrical characteristics tracking regulator

V_{IN} = 13.5 V, 2.0 V ≤ V_{ADJ} ≤ 14 V, V_{EN} ≥ 2.0 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Tracking output							
Output voltage tracking accuracy $\Delta V_{OUT} = V_{ADJ} - V_{OUT}$	ΔV_{OUT}	-5	–	5	mV	5.5 V ≤ V_{IN} ≤ 22 V; 0.1 mA ≤ I_{OUT} ≤ 150 mA; 2 V ≤ V_{ADJ} ≤ V_{IN} - 1 V	P_4.1.1

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Table 5 Electrical characteristics tracking regulator (cont'd)

V_{IN} = 13.5 V, 2.0 V ≤ V_{ADJ} ≤ 14 V, V_{EN} ≥ 2.0 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage tracking accuracy $\Delta V_{OUT} = V_{ADJ} - V_{OUT}$	ΔV_{OUT}	-5	–	5	mV	5.5 V ≤ V_{IN} ≤ 32 V; 0.1 mA ≤ I_{OUT} ≤ 70 mA; 2 V ≤ V_{ADJ} ≤ V_{IN} - 1 V	P_4.1.2
Load regulation steady-state	$\Delta V_{OUT,load}$	-4	-0.1	–	mV	I_{OUT} = 0.1 mA to 150 mA; V_{ADJ} = 5 V	P_4.1.3
Line regulation steady-state	$\Delta V_{OUT,line}$	–	0.1	4	mV	V_{IN} = 5.5 V to 32 V; I_{OUT} = 10 mA; V_{ADJ} = 5 V	P_4.1.4
Power supply ripple rejection[1]	*PSRR*	–	85	–	dB	f_{ripple} = 100 Hz; V_{ripple} = 1 Vpp; I_{OUT} = 10 mA; C_{OUT} = 10 µF, ceramic type	P_4.1.5
Output current limitation	$I_{OUT,max}$	151	350	500	mA	V_{OUT} = V_{ADJ} - 0.1 V; V_{ADJ} = 5 V	P_4.1.6
Reverse current	$I_{OUT,rev}$	-3.5	-1.7	–	mA	V_{IN} = 0 V; V_{OUT} = 16 V; V_{ADJ} = 5 V	P_4.1.9
Reverse current at negative input voltage	$I_{IN,rev}$	-4	-2	–	mA	V_{IN} = -16 V; V_{OUT} = 0 V; V_{ADJ} = 5 V	P_4.1.10
Dropout voltage[2] $V_{dr} = V_{IN} - V_{OUT}$	V_{dr}	–	250	500	mV	I_{OUT} = 150 mA; V_{ADJ} = 5 V[2]	P_4.1.11
Overtemperature protection							
Overtemperature shutdown threshold	$T_{j,sd}$	–	175	–	°C	T_j increasing due to power dissipation generated by the IC	P_4.1.15
Overtemperature shutdown threshold hysteresis	$\Delta T_{j,sdh}$	–	15	–	K		P_4.1.16

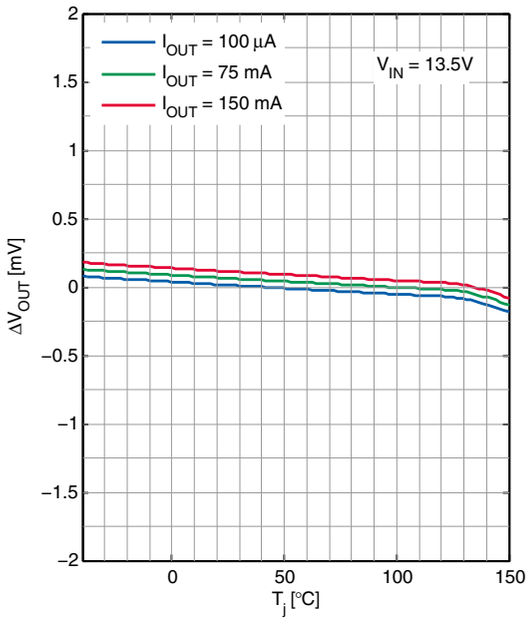
1) Not subject to production test, specified by design

2) Measured when the output voltage V_{OUT} has dropped 100 mV from the nominal value obtained at V_{IN} = 13.5V

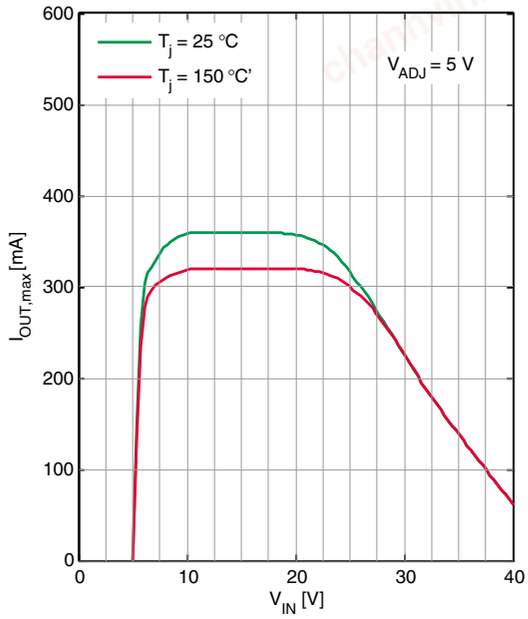
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4.2 Typical performance characteristics tracking regulator

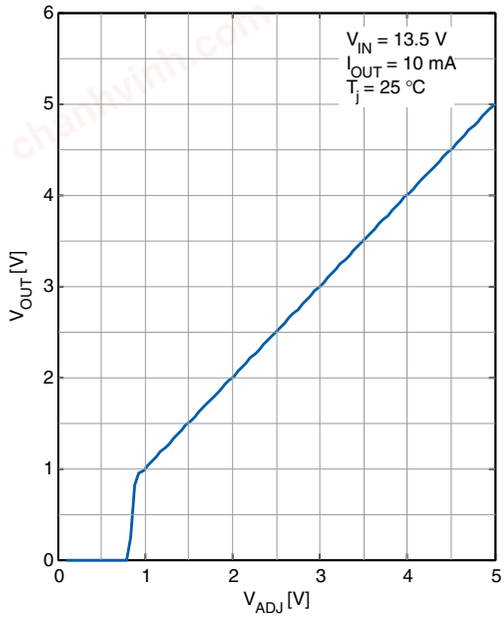
Tracking accuracy ΔV_{OUT} vs. junction temperature T_j



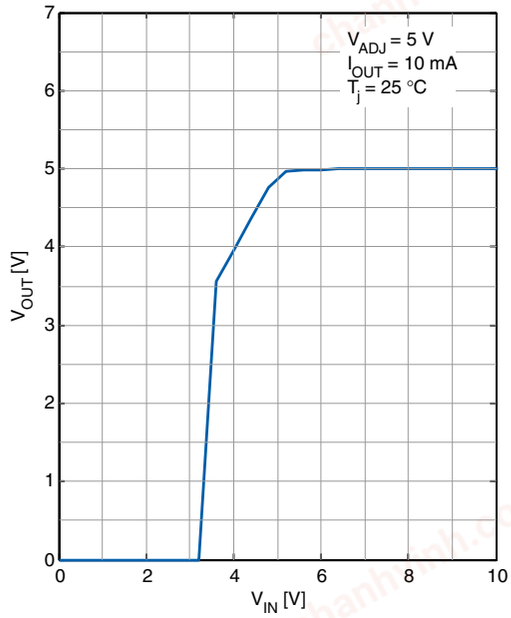
Output current limitation $I_{OUT,max}$ vs. input voltage V_{IN}



Output voltage V_{OUT} vs. adjust voltage V_{ADJ}



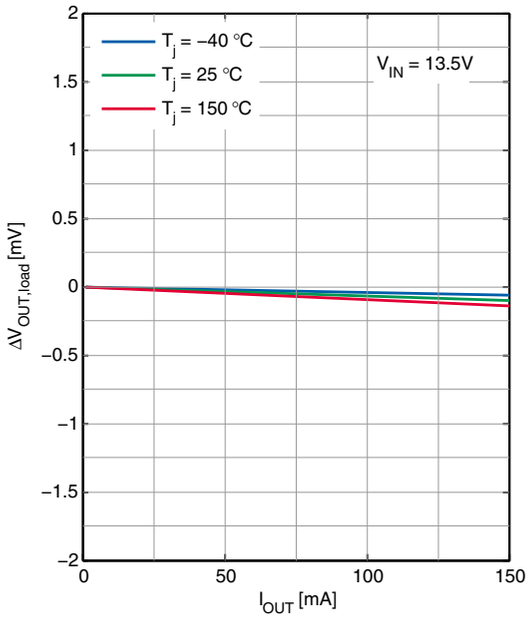
Output voltage V_{OUT} vs. input voltage V_{IN}



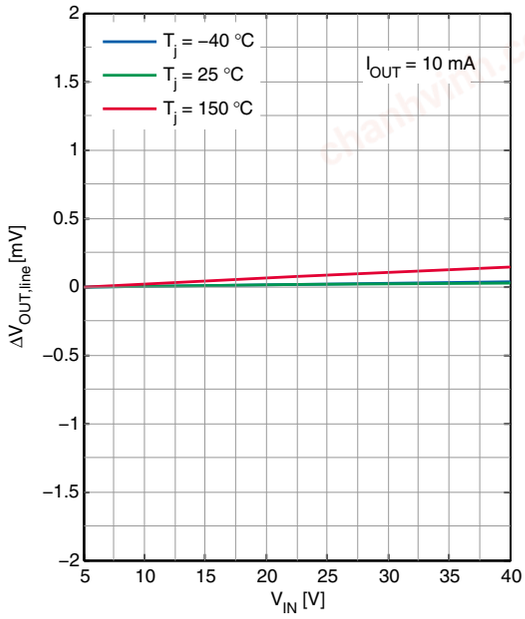
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Block description and electrical characteristics

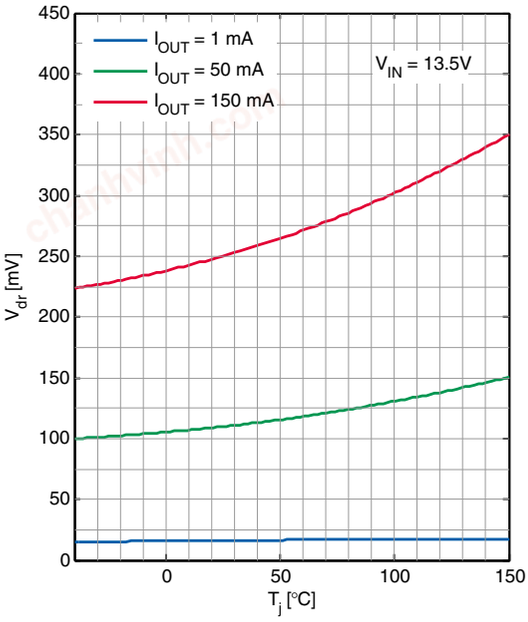
Load regulation $\Delta V_{OUT,load}$ vs. output current I_{OUT}



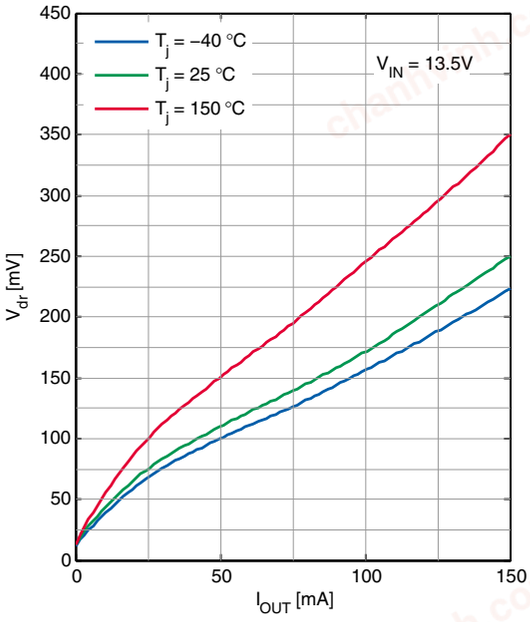
Line regulation $\Delta V_{OUT,line}$ vs. input voltage V_{IN}



Dropout voltage V_{dr} vs. junction temperature T_j



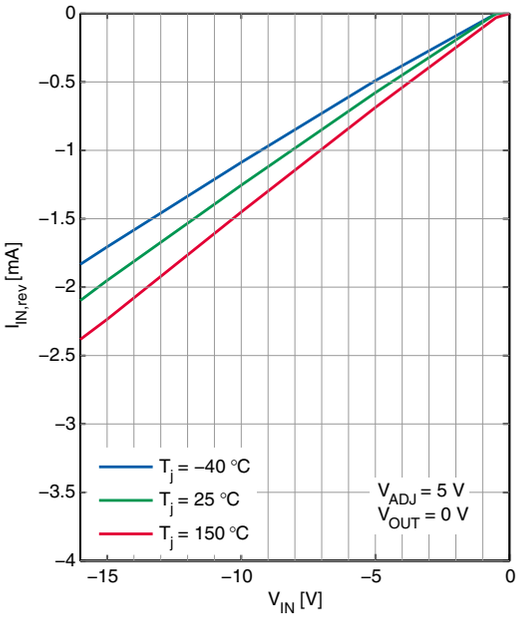
Dropout voltage V_{dr} vs. output current I_{OUT}



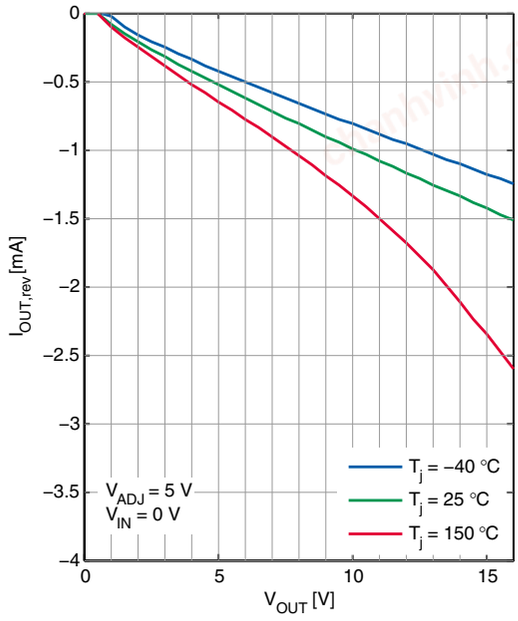
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Block description and electrical characteristics

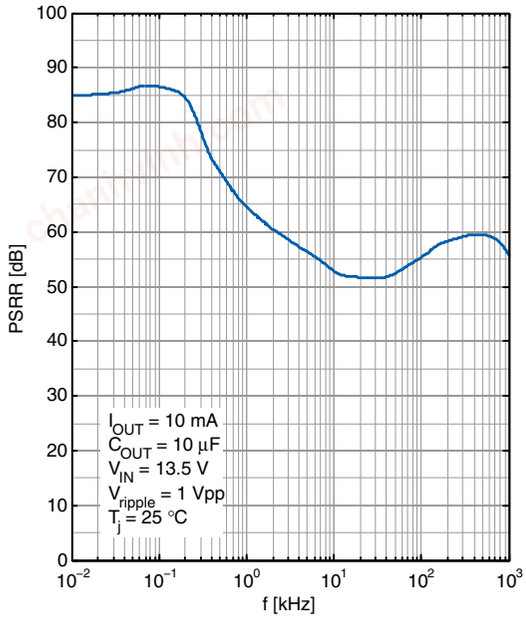
Reverse current $I_{IN,rev}$ vs. input voltage V_{IN}



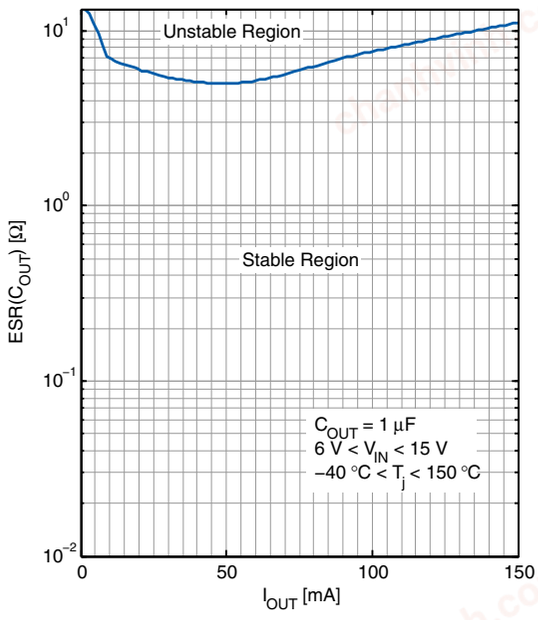
Reverse current $I_{OUT,rev}$ vs. output voltage V_{OUT}



Power supply ripple rejection *PSRR* vs. ripple frequency f_r



Output capacitor *ESR*(C_{OUT}) vs. output current I_{OUT}



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4.3 Current consumption

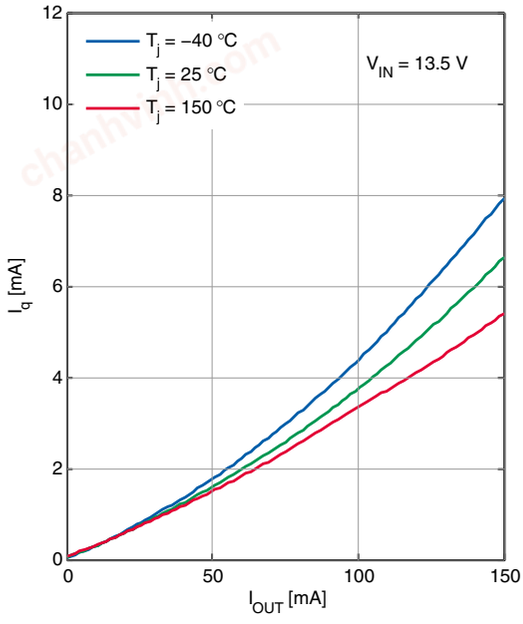
Table 6 Electrical characteristics current consumption

V_{IN} = 13.5 V, 2.0 V ≤ V_{ADJ} ≤ 14 V, V_{EN} ≥ 2.0 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

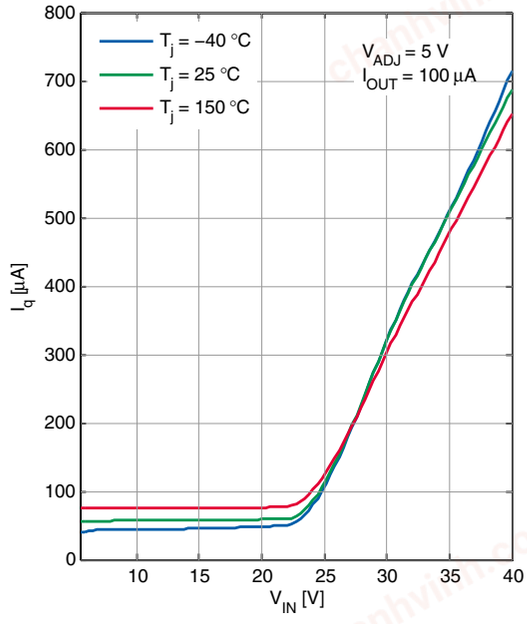
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption Stand-by mode $I_{q,off} = I_{IN}$	$I_{q,off}$	–	0.1	5	µA	V_{EN} ≤ 0.4 V; T_j ≤ 125°C	P_4.3.1
Current consumption $I_q = I_{IN} - I_{OUT}$	I_q	–	55	90	µA	I_{OUT} ≤ 0.1 mA; V_{ADJ} = 5 V; T_j ≤ 125 °C	P_4.3.2
Current consumption $I_q = I_{IN} - I_{OUT}$	I_q	–	7	14	mA	I_{OUT} ≤ 150 mA; V_{ADJ} = 5 V	P_4.3.3

4.4 Typical performance characteristics current consumption

Current consumption I_q vs. output current I_{OUT}



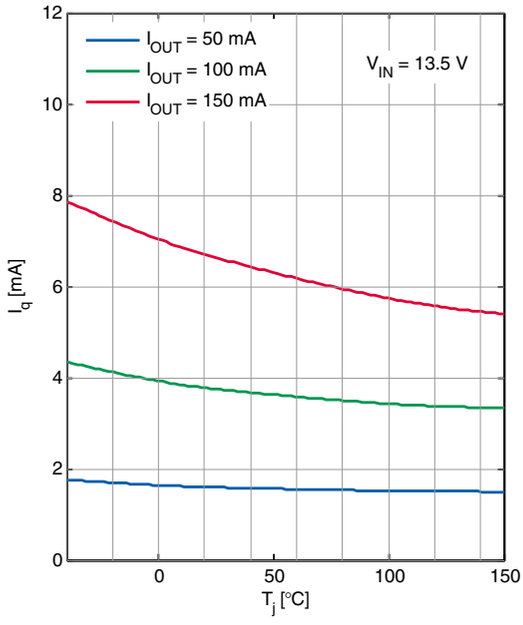
Current consumption I_q vs. input voltage V_{IN}



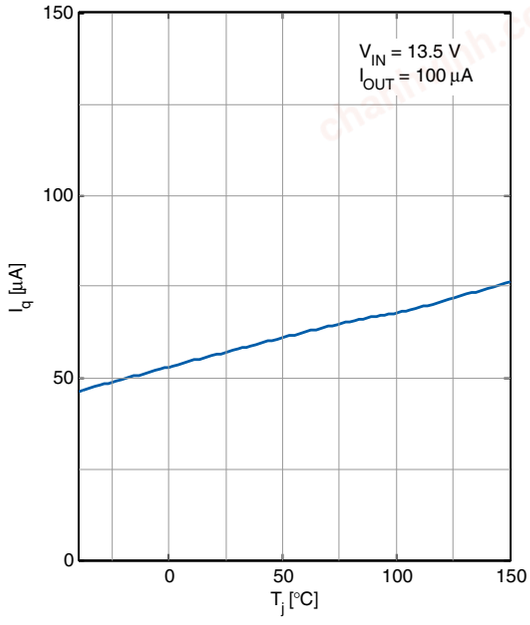
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Block description and electrical characteristics

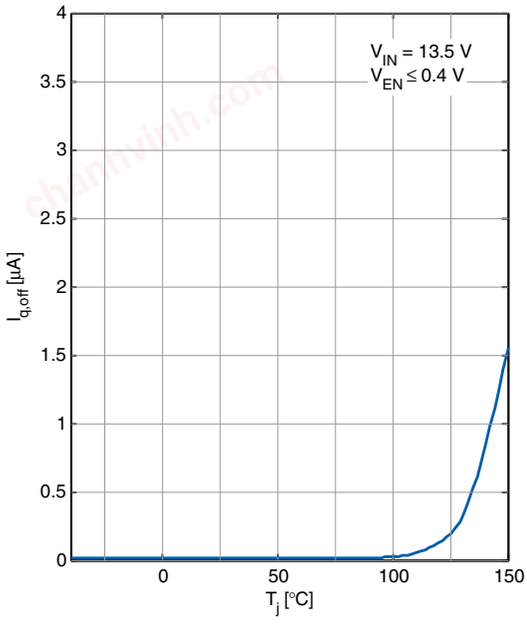
Current consumption I_q vs. junction temperature T_j



Current consumption I_q vs. junction temperature T_j (I_{OUT} low)



Current consumption in OFF mode $I_{q,off}$ vs. junction temperature T_j



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4.5 Enable input

In order to minimize the quiescent current, the TLS115D0 can be switched to stand-by mode by setting the corresponding enable input “EN” to “low”.

If the EN pin is not connected, then the “low” level from the internal pull-down resistor switches off the regulator.

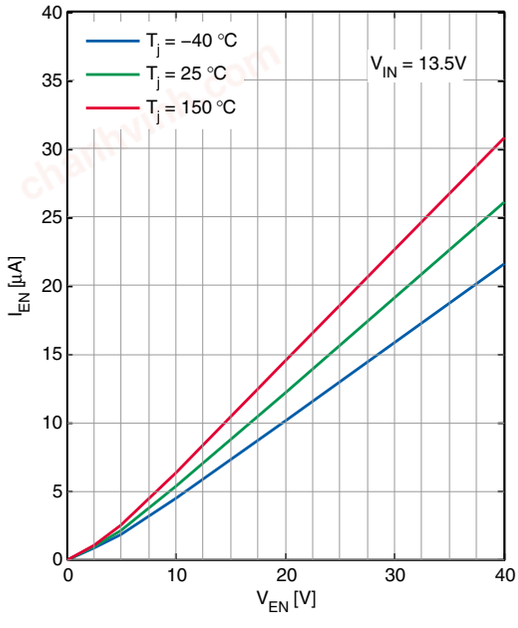
Table 7 Electrical characteristics Enable input

V_{IN} = 13.5 V, 2.0 V ≤ V_{ADJ} ≤ 14 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable off voltage range	$V_{EN,off}$	–	–	0.8	V	V_{OUT} = 0 V, I_{OUT} ≤ 5 µA, T_j ≤ 125°C	P_4.5.1
Enable on voltage range	$V_{EN,on}$	2	–	–	V	V_{OUT} settled	P_4.5.2
Enable input current	I_{EN}	–	2	4	µA	V_{EN} = 5 V	P_4.5.3

4.6 Typical performance characteristics Enable input

**Enable input current I_{EN} vs.
Enable input voltage V_{EN}**



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4.7 Adjust input

The Adjust input must be connected to the reference voltage, which is tracked.

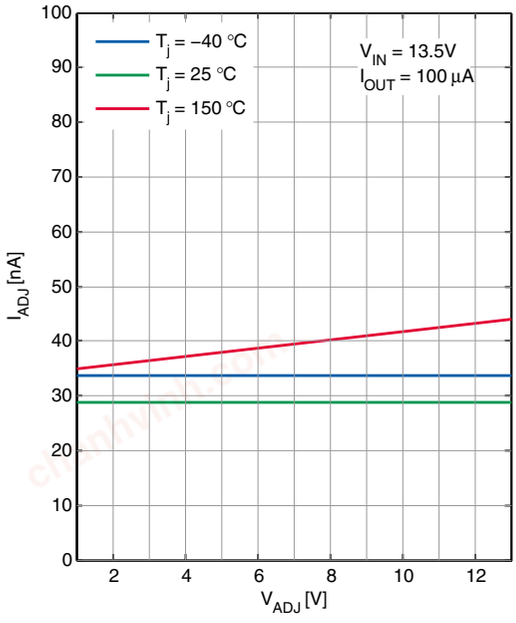
Table 8 Electrical characteristics Adjust input

V_{IN} = 13.5 V, 2.0 V ≤ V_{ADJ} ≤ 14 V, V_{EN} ≥ 2.0 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

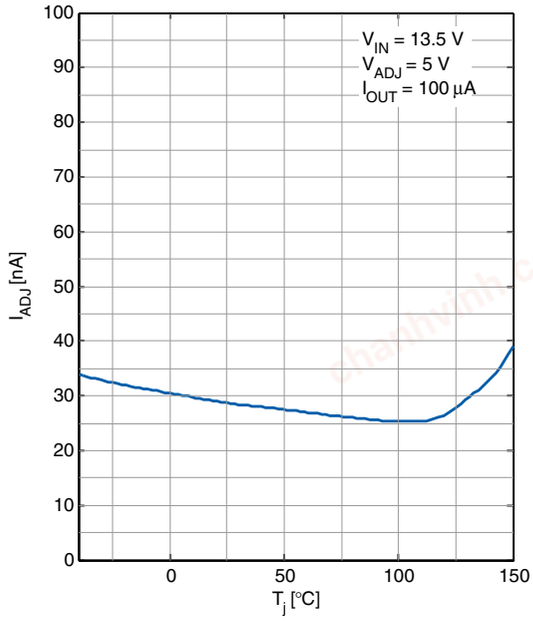
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Adjust input current	I_{ADJ}	–	0.03	1	µA	V_{ADJ} = 5 V	P_4.7.1

4.8 Typical performance characteristics Adjust input

Adjust input current I_{ADJ} vs. Adjust input voltage V_{ADJ}



Adjust input current I_{ADJ} vs. junction temperature T_j



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4.9 Power Good output

The Power Good output PG indicates an overvoltage or undervoltage condition of the tracker output. For this the TLS115D0 compares the output voltage V_{OUT} to the reference voltage V_{ADJ}. Variations of the output voltage beyond the Power Good switching thresholds are indicated by a “low” signal at the Power Good output PG. Transients shorter than the Power Good reaction time $t_{PG,r}$ do not trigger the Power Good output.

The Power Good output PG is an open collector output that requires a pull-up resisitor to a positive voltage rail. The pull-up voltage must not exceed the absolute maximum ratings of Power Good PG (see **“Absolute maximum ratings” on Page 7**).

Table 9 Electrical characteristics Power Good output

V_{IN} = 13.5 V, 2.0 V ≤ V_{ADJ} ≤ 14 V, V_{EN} ≥ 2.0 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Good switching threshold, undervoltage	$V_{OUT,UV}$	V_{ADJ} - 120	V_{ADJ} - 70	V_{ADJ} - 50	mV	V_{OUT} decreasing, $V_{IN} \geq V_{ADJ}$ + 150 mV	P_4.9.1
Power Good switching threshold, overvoltage	$V_{OUT,OV}$	V_{ADJ} + 50	V_{ADJ} + 70	V_{ADJ} + 120	mV	V_{OUT} increasing, $V_{IN} \geq V_{ADJ}$ + 150 mV	P_4.9.2
Power Good reaction time	$t_{PG,r}$	10	15	30	µs	–	P_4.9.3
Power Good output low voltage	$V_{PG,low}$	–	0.2	0.4	V	$V_{IN} \geq 4$ V, $I_{PG,ext} \leq 1.8$ mA	P_4.9.4
Power Good output external input current	$I_{PG,ext}$	–	–	1.8	mA	$V_{PG} \leq 0.4$ V	P_4.9.5
Power Good output leakage current	$I_{PG,leak}$	–	0	2	µA	$V_{OUT} = V_{ADJ}$, $V_{PG} = 5$ V	P_4.9.6

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5 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

5.1 Application diagram

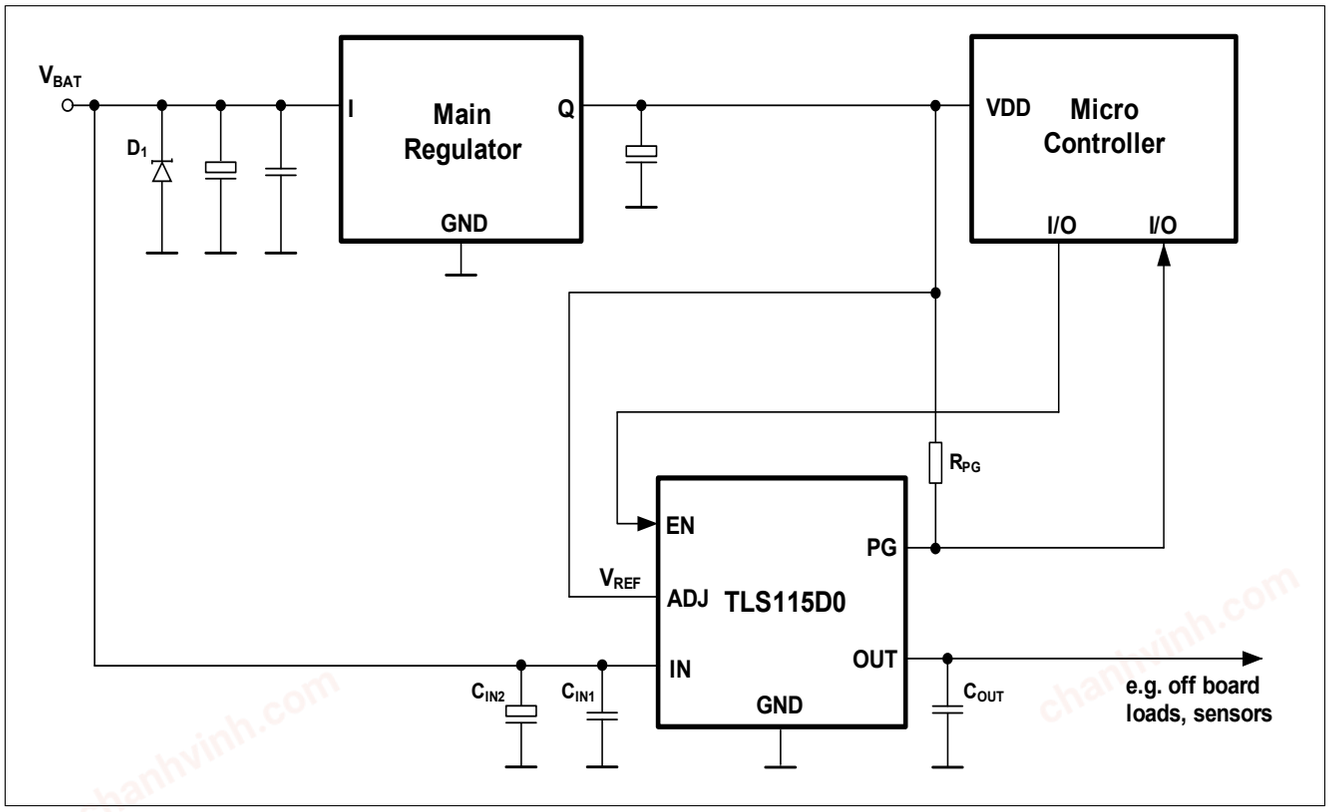


Figure 4 TLS115D0 application circuit

5.2 Selection of external components

5.2.1 Input pin

Figure 4 shows the typical input circuitry for a voltage tracking regulator. The following external components at the input are recommended in case of possible external disturbance.

A ceramic capacitor C_{IN1} (100 nF to 470 nF) at the input filters high frequency disturbance imposed by the line, such as ISO pulses 3a/b. Place C_{IN1} very close to the input pin of the voltage tracking regulator on the PCB.

An aluminum electrolytic capacitor C_{IN2} (10 µF to 470 µF) at the input smoothens high energy pulses, such as ISO pulse 2a. Place C_{IN2} close to the input pin of the voltage tracking regulator on the PCB.

An accordingly sized overvoltage suppressor diode D_1 suppresses high voltage beyond the maximum ratings of the circuit components and protects the devices from damage due to overvoltage.

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5.2.2 Output pin

An output capacitor C_{OUT} is mandatory for the stability of the voltage tracking regulator. The requirements for C_{OUT} are described in the table **"Functional range" on Page 8**. The graph **"Output capacitor ESR(COUT) vs. output current IOUT" on Page 14** shows the stable operation range of the TLS115D0.

For automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

Place C_{OUT} on the same side of the PCB as the regulator itself and as close as possible to both the tracker output pin and GND pin.

In case of rapid transients of input voltage or load current, C_{OUT} must be dimensioned properly to ensure the output stability in the application.

5.2.3 Adjust pin

Figure 4 shows a typical Adjust circuitry for a voltage tracking regulator. Typically the Adjust Pin is connected to a fixed voltage reference that the regulator tracks. In the example of the application diagram ADJ is connected to the supply voltage of a microcontroller. The voltage reference can also be adjusted by a voltage divider.

5.2.4 Power Good pin

The Power Good output is an open collector output, which requires a pull-up resistor to a positive voltage rail. The pull-up voltage must not exceed the maximum ratings of the Power Good PG shown in **"Absolute maximum ratings" on Page 7**. In **Figure 4** the supply voltage VDD of a microcontroller is used as pull-up voltage for example.

To limit the external input current according to the requirement (see **"Power Good output" on Page 19**), the resistor must be sized depending on the pull-up voltage.

5.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_q \quad (5.1)$$

with

- P_D: continuous power dissipation
- V_{IN}: input voltage
- V_{OUT}: output voltage
- I_{OUT}: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,\,max} = \frac{T_{j,\,max} - T_a}{P_D} \quad (5.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

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Application information

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **“Thermal resistance” on Page 8**.

Example

Application conditions:

V_{IN} = 13.5 V

V_{OUT} = V_{ADJ} = 5 V

I_{OUT} = 100 mA

T_a = 75°C

Calculation of $R_{thJA,max}$:

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_q$

= (13.5V – 5V) x 100 mA + 13.5 V x 3.5 mA

= 0.897 W

$R_{thJA,max} = (T_{j,max} - T_a) / P_D$

= (150°C – 75°C) / 0.897 W

= 83.61 K/W

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 83.61 K/W. According to **“Thermal resistance” on Page 8**, at least 300 mm² heatsink area is required on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

5.4 Further application information

- For further information you may contact **http://www.infineon.com/**

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6 Package outlines

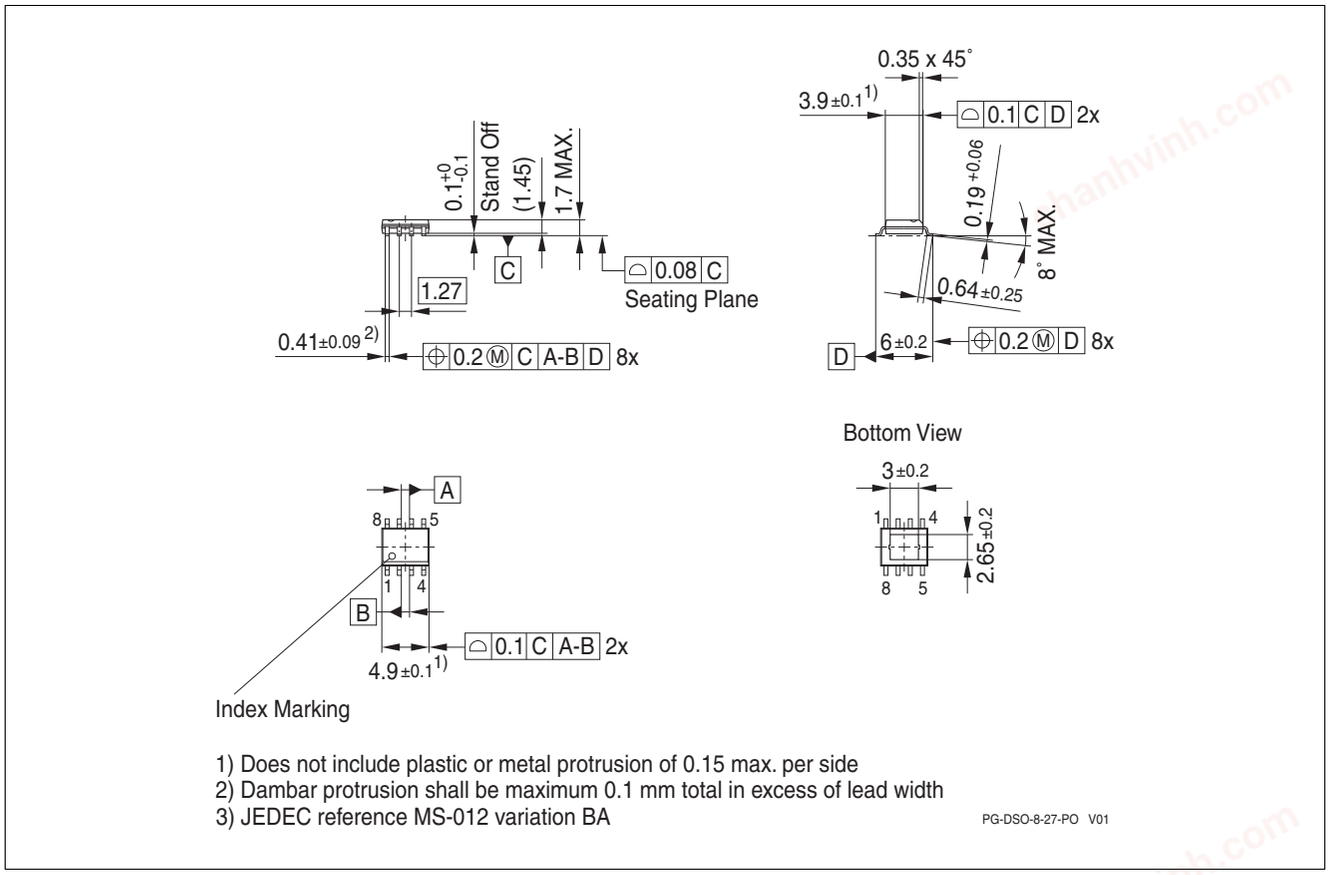


Figure 5 PG-DSO-8 EP

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Package outlines

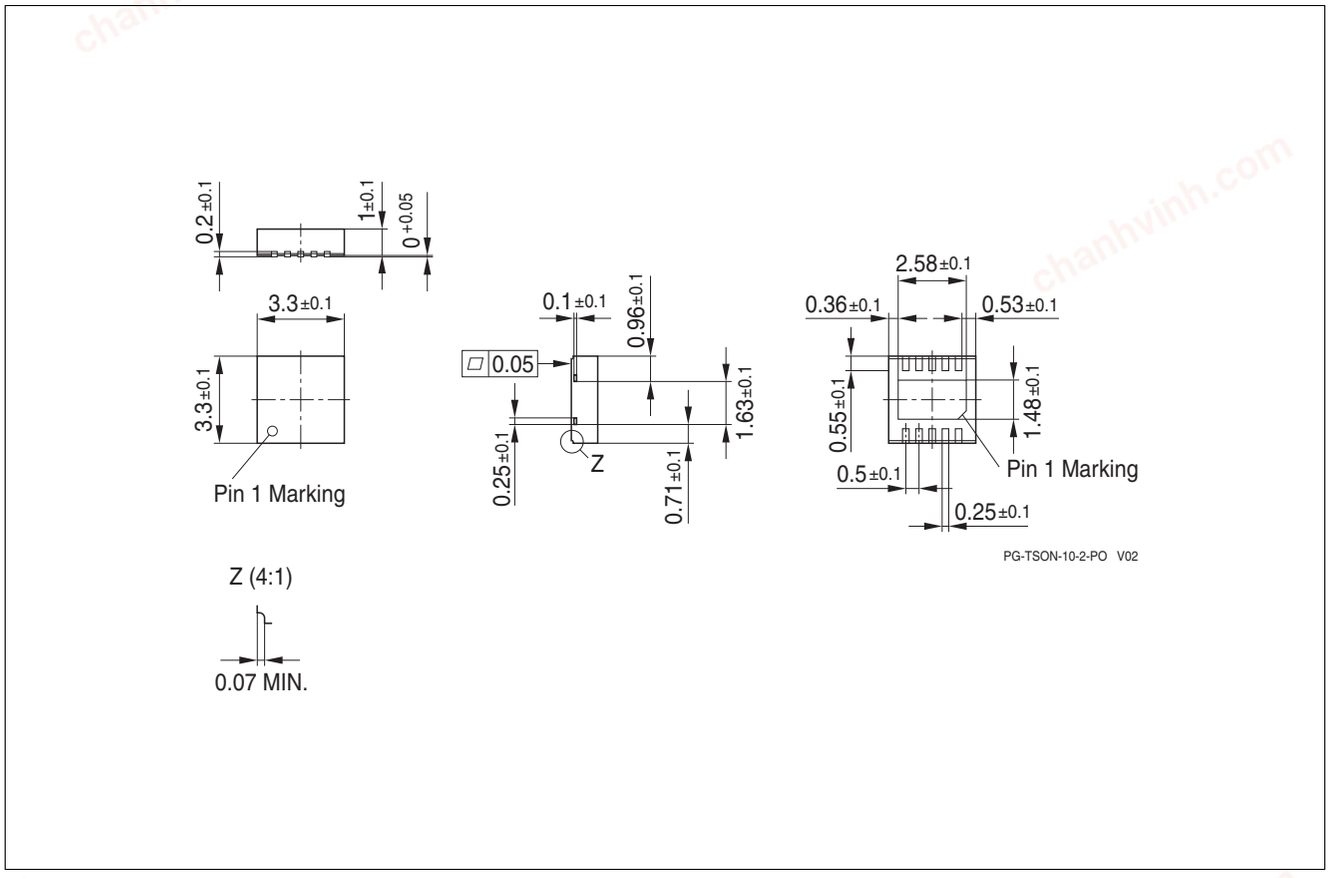


Figure 6 PG-TSON-10

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

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7 Revision history

Revision	Date	Changes
1.10	2020-03-19	Data Sheet - updated - Maximum rating for the input output voltage difference added - Editorial changes
1.00	2016-10-13	Data Sheet - Initial Version

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