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TLF1963

Low Dropout Linear Voltage Post Regulator

TLF1963TB
TLF1963TE

Data Sheet

Rev. 1.0, 2012-11-08

Automotive Power

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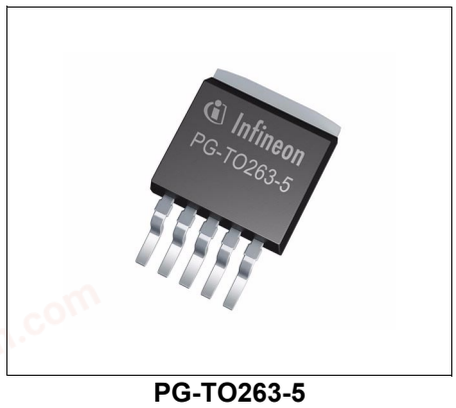
8 Revision History . . . 23

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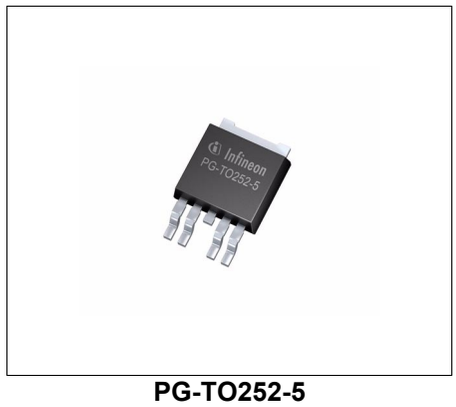
Low Dropout Linear Voltage Post Regulator **TLF1963**

AEC Qualified RoHS

1 Overview



PG-TO263-5



PG-TO252-5

Features

- Adjustable Output Voltage
- Output Voltage Tolerance at small loads of ±1.5 %
- Output Current Capability up to 1.5 A
- Very Low Dropout Voltage of 340 mV
- Extended Operating Range Starting at 1.7 V
- Low Noise of typ. 40 μV_{RMS} (10 Hz to 100 kHz)
- Small Output Capacitor for Stability 10 µF
- Suitable for Ceramic Output Capacitors
- Enable Functionality
- Overtemperature Shutdown
- Reverse Polarity Protection
- Output Current Limitation
- Wide Temperature Range From -40 °C up to 150 °C
- Suitable for use in automotive electronics as Post Regulator
- Green Product (RoHS compliant)
- AEC Qualified

Functional Description

TLF1963 is a low dropout voltage regulator available in PG-TO263-5 and PG-TO252-5 SMD package. The IC regulates an input voltage V_I in the range of 2.5 V < V_I < 20 V to an adjustable output voltage of 1.21 V < $V_{Q,nom}$ < V_I - V_{dr}. The device is capable to supply loads up to 1.5 A. The regulator can be enabled and disabled via the Enable input. The integrated output current limitation and the overtemperature shutdown will protect the device against failures like output short circuit to GND, overcurrent and overtemperature.

The TLF1963 provides the ideal solution for systems requiring several supply voltages. With its adjust feature the regulator can provide all supply voltages between 1.21 V and the available input voltage, this offers a high flexibility to the system designer.

Choosing External Components

The input capacitor C_I is necessary for compensating line influences. The output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values specified in **“Functional Range” on Page 8** within the whole operating temperature range.

Type	Package	Marking
TLF1963TB	PG-TO263-5	T1963V
TLF1963TE	PG-TO252-5	T1963V

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2 Block Diagram

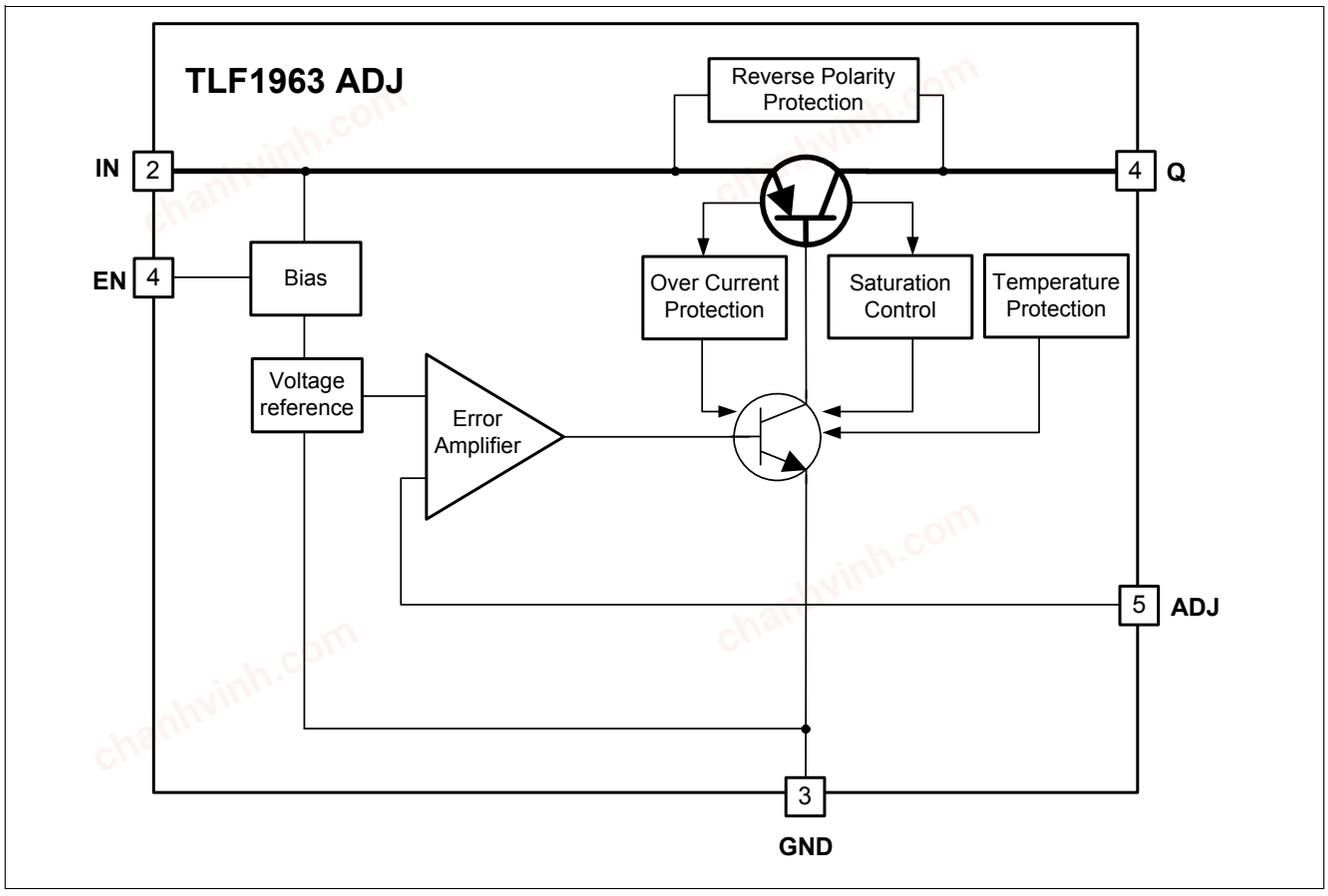


Figure 1 Block Diagram

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3 Pin Configuration

3.1 Pin Assignment TLF1963TB

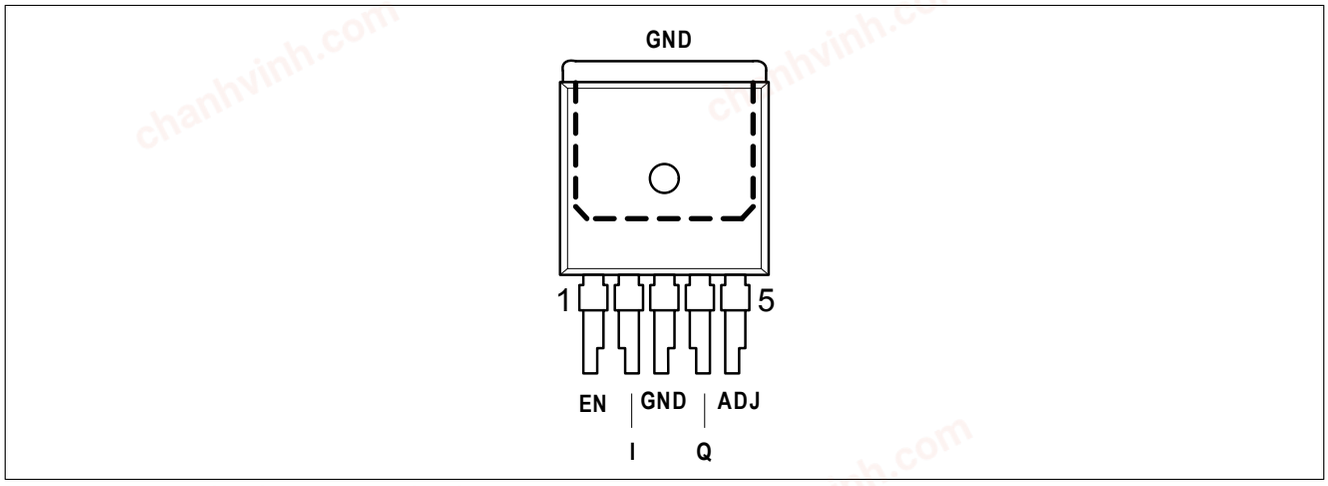


Figure 2 Pin Configuration PG-TO263-5

3.2 Pin Definitions and Functions TLF1963TB

Pin	Symbol	Function
1	EN	**Enable;** A low signal disables the IC. A high signal switches it on. Connect to the input I, if enable functionality is not required.
2	I	**Input voltage;** IC supply. For compensating line influences, a capacitor close to the IC pins is recommended.
3	GND	**Ground**
4	Q	**Output voltage;** Connect a capacitor between Q and GND close to the IC terminals, respecting the values given for its capacitance C_Q and ESR given in the table **“Functional Range” on Page 8**
5	ADJ	**Adjust Input;** Connect an external voltage divider from Q to GND to determine the output voltage. By connecting the output pin Q directly to the adjust pin ADJ without resistors an ouput voltage equal to the reference voltage V_{ADJ} = 1.21 V is determined.
TAB	GND	**Ground**

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3.3 Pin Assignment TLF1963TE

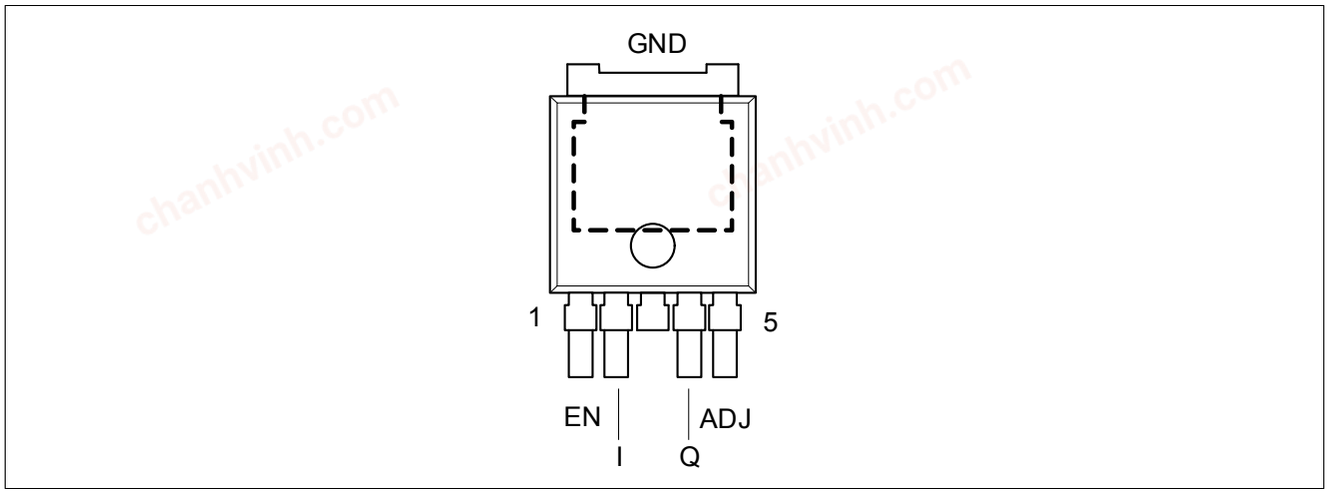


Figure 3 Pin Configuration PG-TO252-5

3.4 Pin Definitions and Functions TLF1963TE

Pin	Symbol	Function
1	EN	**Enable;** A low signal disables the IC. A high signal switches it on. Connect to the input I, if enable functionality is not required.
2	I	**Input voltage;** IC supply. For compensating line influences, a capacitor close to the IC pins is recommended.
3	GND	**Ground**
4	Q	**Output voltage;** Connect a capacitor between Q and GND close to the IC terminals, respecting the values given for its capacitance C_Q and ESR given in the table **“Functional Range” on Page 8**
5	ADJ	**Adjust Input;** Connect an external voltage divider from Q to GND to determine the output voltage. By connecting the output pin Q directly to the adjust pin ADJ without resistors an ouput voltage equal to the reference voltage V_{ADJ} = 1.21 V is determined.
TAB	GND	**Ground**

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4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Input, Enable						
4.1.1	Voltage	V_I, V_{EN}	-20	20	V	–
Adjust						
4.1.2	Voltage	V_{ADJ}	-7	7	V	–
Output						
4.1.3	Voltage	V_Q	-20	20	V	–
Temperatures						
4.1.4	Junction Temperature	T_j	-40	150	°C	–
4.1.5	Storage Temperature	T_{stg}	-50	150	°C	–
ESD Susceptibility						
4.1.6	ESD Resistivity	V_{ESD}	-2	2	kV	HBM[2)]
4.1.7	ESD Resistivity	V_{ESD}	-750	750	V	CDM[3)]

1) Not subject to production test, specified by design.

2) ESD HBM Test according AEC-Q100-002 - JESD22-A114 (1.5 kOhm, 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

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4.2 Functional Range

Table 2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input voltage	V_I	2.5	20	V	–
4.2.2	Output Capacitor's Requirements for Stability	C_Q	10	–	µF	–[1]
		$ESR(C_Q)$	–	3	Ω	–[2]
4.2.3	Junction temperature	T_j	-40	150	°C	

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at f = 10 kHz

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Package PG-TO263-5							
4.3.1	Junction to Case[1]	R_{thJC}	–	0.84	–	K/W	measured to heat slug
4.3.2	Junction to Ambient[1]	R_{thJA}	–	19	–	K/W	[2]
4.3.3			–	64	–	K/W	footprint only[3]
4.3.4			–	36	–	K/W	300 mm² heatsink area[3]
4.3.5			–	29	–	K/W	600 mm² heatsink area[3]
Package PG-TO252-5							
4.3.6	Junction to Case[1]	R_{thJC}	–	0.78	–	K/W	measured to heat slug
4.3.7	Junction to Ambient[1]	R_{thJA}	–	24	–	K/W	[2]
4.3.8			–	95	–	K/W	footprint only[3]
4.3.9			–	50	–	K/W	300 mm² heatsink area[3]
4.3.10			–	38	–	K/W	600 mm² heatsink area[3]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70 µm Cu).

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5 Electrical Characteristics

5.1 Electrical Characteristics Voltage Regulator

Table 4 Electrical Characteristics:

V_I = 2.5 V - 20 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing out of the pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Min. Input Voltage [1) 2)]	$V_{I,min}$	–	1.7	–	V	I_Q = 0.5 A; T_j = 25 °C
5.1.2		$V_{I,min}$	–	2.1	2.5	V	I_Q = 1.5 A
5.1.3	Adjustable Pin Voltage [1) 3)]	V_{ADJ}	1.192	1.21	1.228	V	V_I = 2.21 to 20 V; I_Q = 1 mA; T_j = 25 °C
5.1.4			1.174	1.21	1.246	V	I_Q = 1 mA to 1.5 A
5.1.5	Line regulation [1)]	$\Delta V_{Q,line}$	–	1.0	3	mV	V_I = 2.21 to 20 V; I_Q = 1 mA
5.1.6	Load regulation [1)]	$\Delta V_{Q,load}$	–	2	8	mV	I_Q = 1 mA to 1.5 A; V_I = 2.5 V; T_j = 25 °C
5.1.7			–	–	12	mV	I_Q = 1 mA to 1.5 A; V_I = 2.5 V
5.1.8	Dropout voltage [2) 4) 5)] $V_I = V_{Q,nom}$	V_{dr}	–	0.01	0.03	V	I_Q = 1 mA; T_j = 25 °C
5.1.9			–	–	0.04	V	I_Q = 1 mA
5.1.10			–	0.03	0.05	V	I_Q = 100 mA; T_j = 25 °C
5.1.11			–	–	0.09	V	I_Q = 100 mA
5.1.12			–	0.13	0.25	V	I_Q = 500 mA; T_j = 25 °C
5.1.13			–	–	0.27	V	I_Q = 500 mA
5.1.14			–	0.34	0.45	V	I_Q = 1.5 A; T_j = 25 °C
5.1.15			–	–	0.55	V	I_Q = 1.5 A
5.1.16	GND Pin Current [4) 6)] $V_I = V_{Q,nom}$ + 1 V	I_q	–	1.0	1.5	mA	I_Q = 0 mA
5.1.17			–	1.1	1.7	mA	I_Q = 1 mA
5.1.18			–	3.8	5.0	mA	I_Q = 100 mA
5.1.19			–	15	22	mA	I_Q = 500 mA
5.1.20			–	80	130	mA	I_Q = 1.5 A
5.1.21	Output Voltage Noise	$V_{Q,noise}$	–	40	–	μV_{RMS}	C_Q = 10 µF; I_Q = 1.5 A; BW = 10 Hz to 100 kHz
5.1.22	ADJ Pin Bias Current [1) 7)]	I_{ADJ}	–	1	2	µA	–
5.1.23	Enable Threshold	$V_{EN,LH}$	–	1.4	2	V	V_Q = Off to On
5.1.24		$V_{EN,HL}$	0.8	1.3	–	V	V_Q = On to Off
5.1.25	EN Pin current [8)]	I_{EN}	–	0	0.2	µA	V_{EN} = 0 V
5.1.26			–	2.5	20	µA	$V_{EN} \leq$ 20 V

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Table 4 Electrical Characteristics: (cont'd)

V_I = 2.5 V - 20 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing out of the pin (unless otherwise specified)

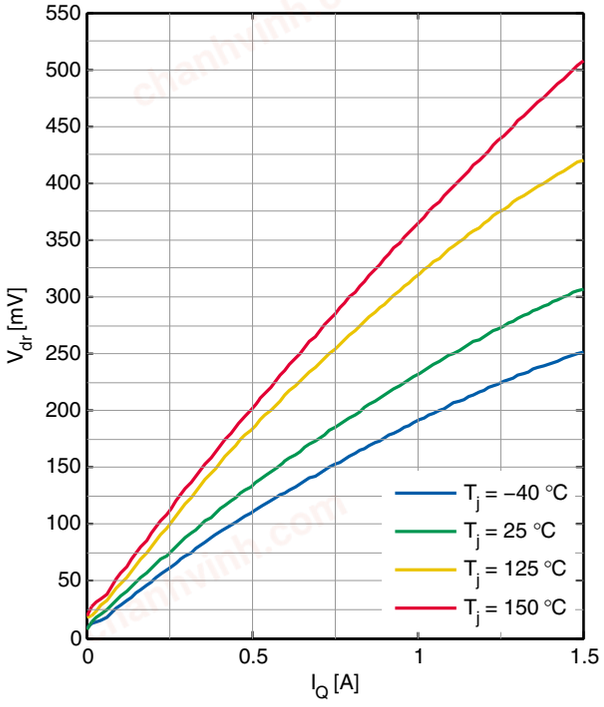
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.27	Quiescent Current in Shutdown [9]	$I_{q,off}$	–	0.01	1	µA	V_I = 6 V; V_{EN} = 0 V; $T_j \leq$ 85 °C
5.1.28	Power Supply ripple rejection [10]	*PSRR*	55	67	–	dB	T_j = 25 °C; f_r = 120 Hz; I_Q = 0.75 A; V_I - V_Q = 1.5 V; V_r = 0.5 V_{pp}
5.1.29	Output current limitation	I_Q	–	2	–	A	T_j = 25 °C; V_I = 7 V; V_Q = 0 V
5.1.30		I_Q	1.6	–	–	A	V_I = $V_{Q,nom}$ + 1 V; dV_Q = -0.1 V
5.1.31	Input Reverse Leakage Current	$I_{I,rev}$	–	–	2	mA	V_I = -20 V; V_Q = 0 V
5.1.32	Reverse Output Current [11]	$I_{Q,rev}$	–	300	600	µA	T_j = 25 °C; V_Q = 1.21 V; V_I < 1.21 V
5.1.33			–	–	1	mA	V_Q = 1.21 V; V_I < 1.21 V

1) The TLF1963 is tested and specified for these conditions with the ADJ pin connected to the Q pin.
2) For TLF1963 dropout voltage will be limited by the minimum input voltage specification under some output voltage/load conditions.
3) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.
4) To satisfy requirements for minimum input voltage, the TLF1963 is tested and specified for these conditions with an external resistor divider (two 4.12 kΩ resistors) for an output voltage of 2.4 V. The external resistor divider will add a 300 µA DC load on the output.
5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: $V_I - V_{dr}$
6) GND pin current is tested with V_I = $V_{Q,nom}$ + 1 V and a current source load.
7) ADJ pin bias current flows into the ADJ pin.
8) EN pin current flows into the EN pin.
9) Specified by design, tested at T_{amb} = 25 °C
10) Not subject to production test, specified by design.
11) Reverse output current is tested with the IN pin grounded and the Q pin forced to the rated output voltage. This current flows into the Q pin and out the GND pin

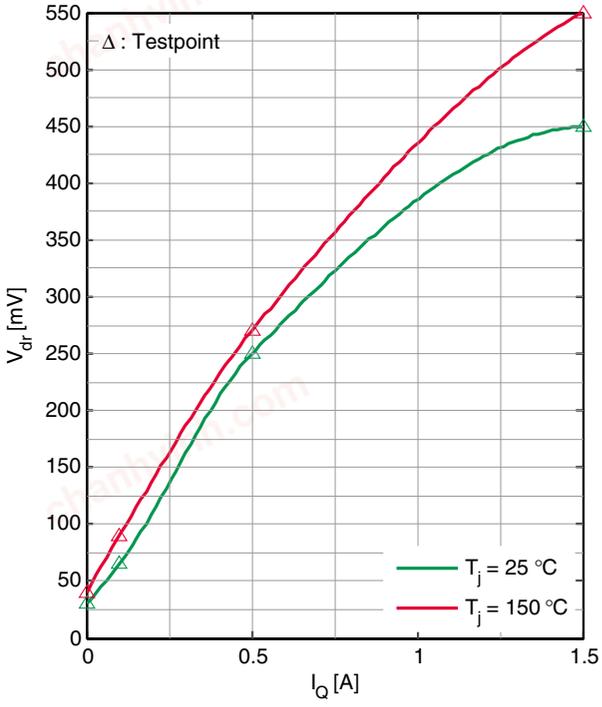
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5.2 Typical Performance Characteristics

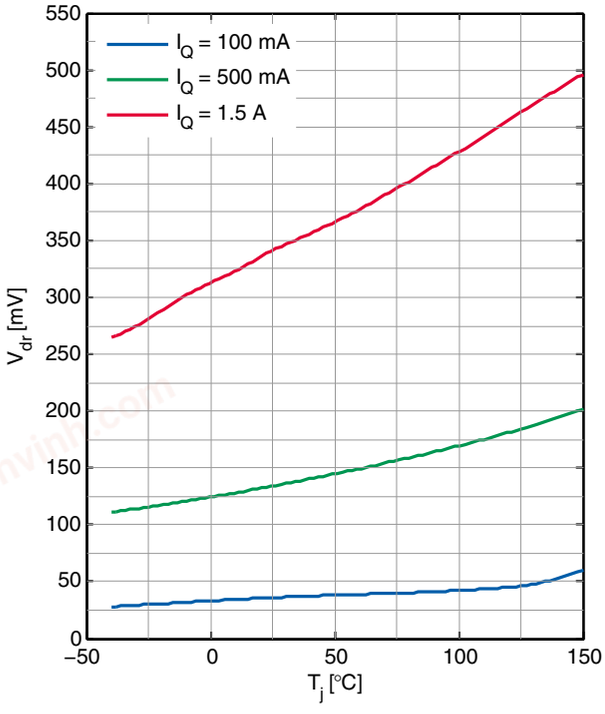
Dropout Voltage V_{DR} versus Output Current I_Q



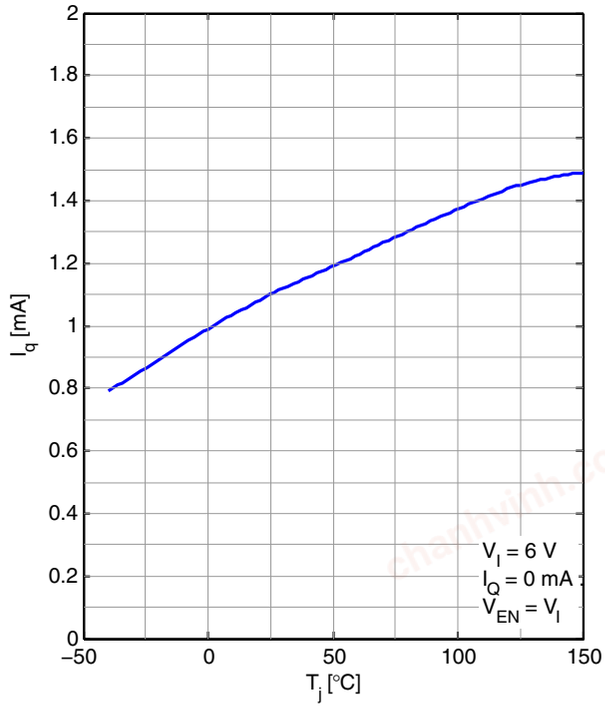
Guaranteed Dropout Voltage V_{dr} versus Output Current I_Q



Dropout Voltage V_{dr} versus Temperature T_j

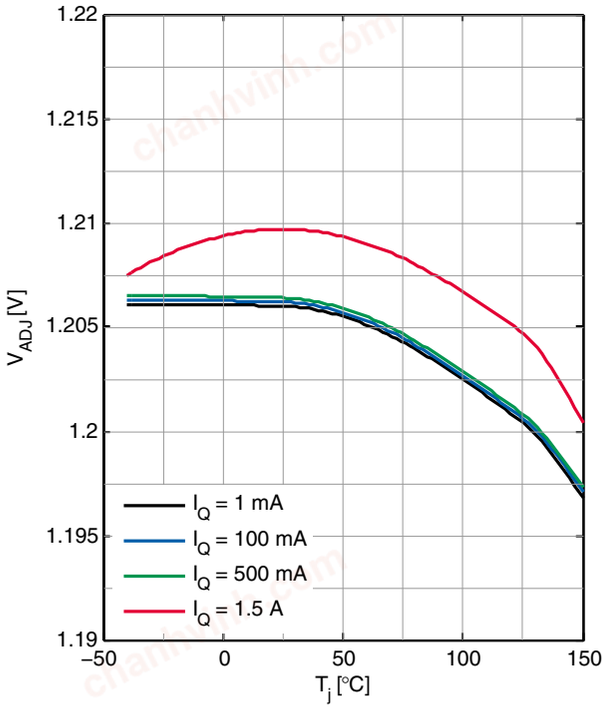


Quiescent Current I_q versus Temperature T_j

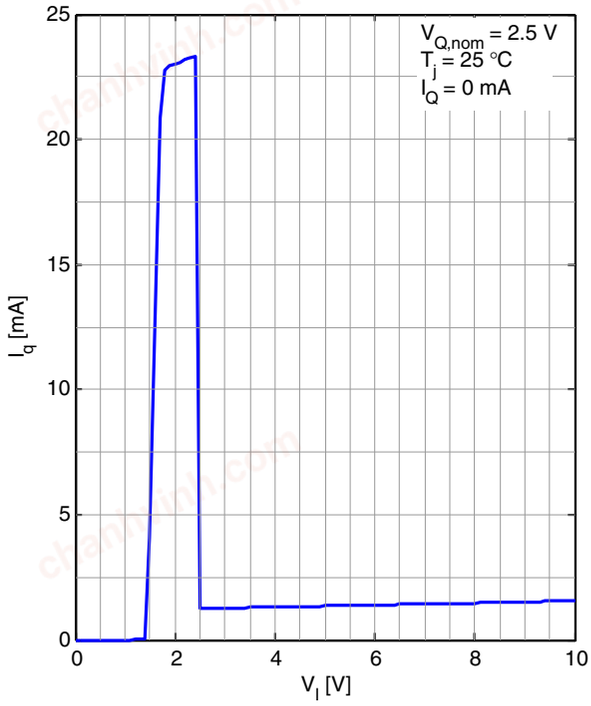


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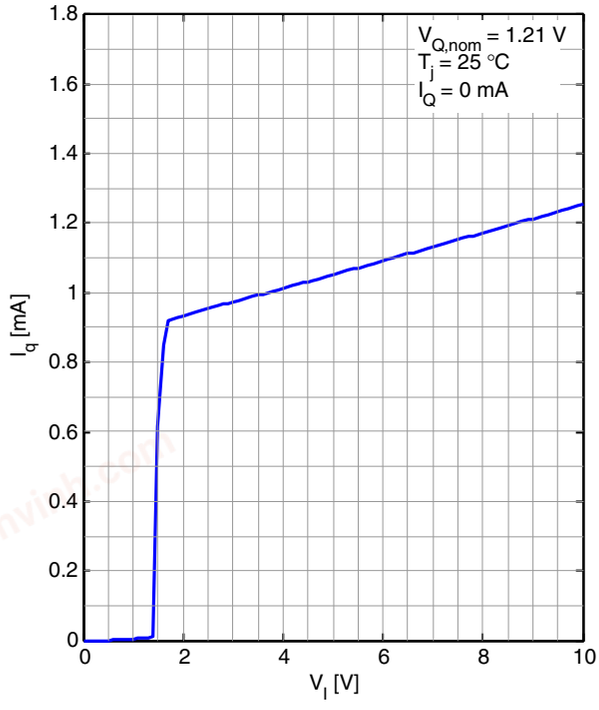
Adjustable Voltage V_{ADJ} versus Temperature T_j



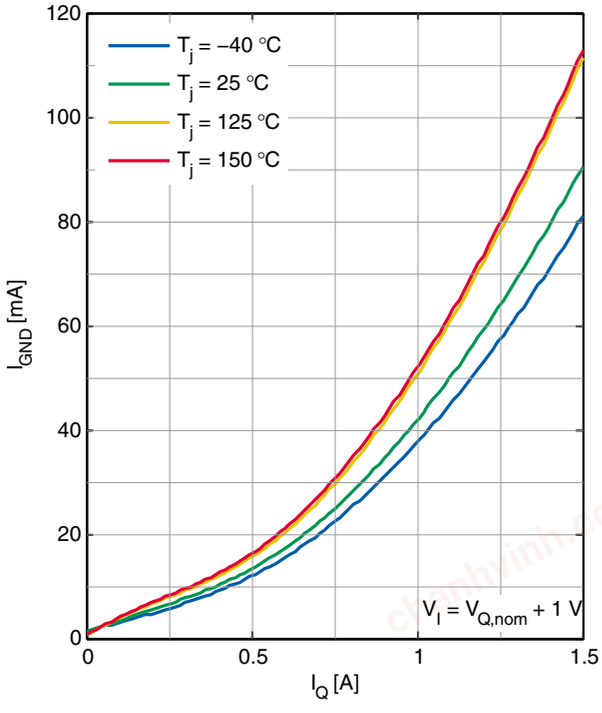
Quiescent Current I_q versus Input Voltage V_I ($V_{Q,nom}$ = 2.5 V)



Quiescent Current I_q versus Input Voltage V_I ($V_{Q,nom}$ = 1.21 V)

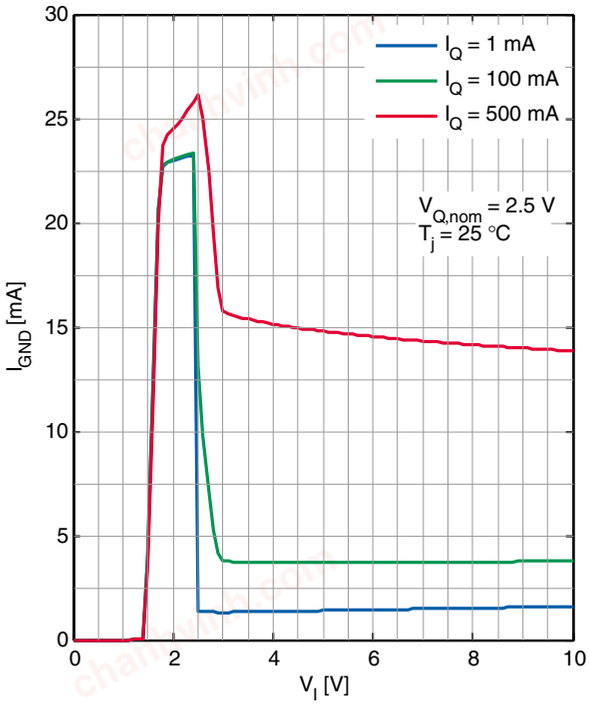


GND Pin Current I_{GND} versus Output Current I_Q

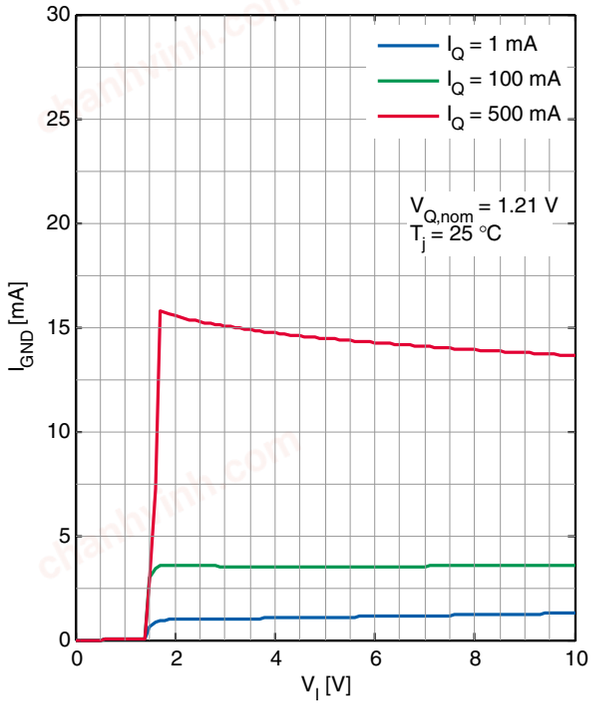


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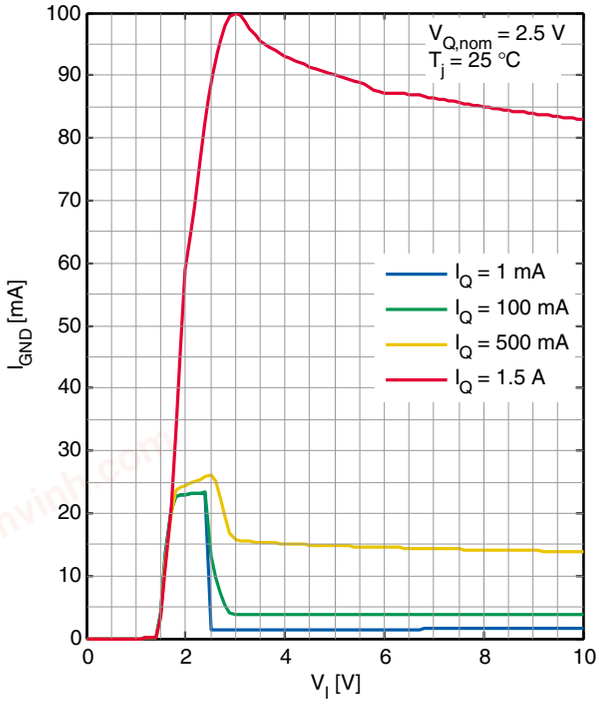
GND Pin Current I_{GND} versus Input Voltage V_I ($V_{Q,nom}$ = 2.5 V)



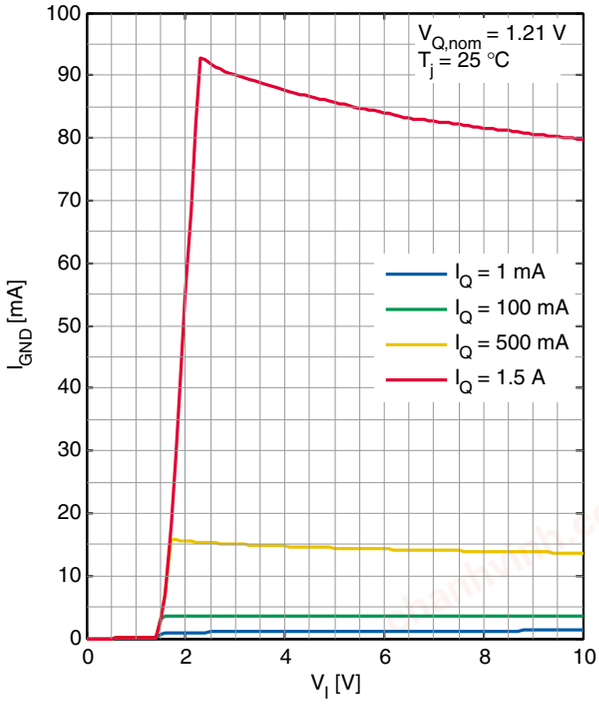
GND Pin Current I_{GND} versus Input Voltage V_I ($V_{Q,nom}$ = 1.21 V)



GND Pin Current I_{GND} versus Input Voltage V_I ($V_{Q,nom}$ = 2.5 V)

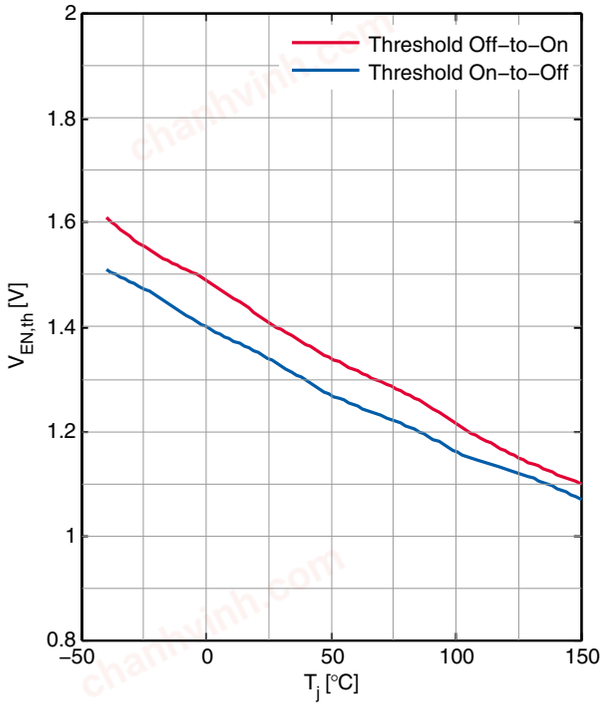


GND Pin Current I_{GND} versus Input Voltage V_I ($V_{Q,nom}$ = 1.21 V)

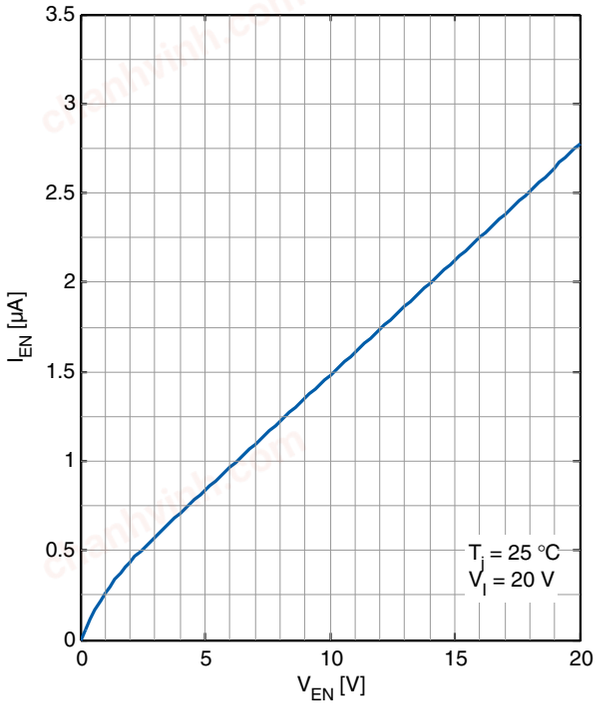


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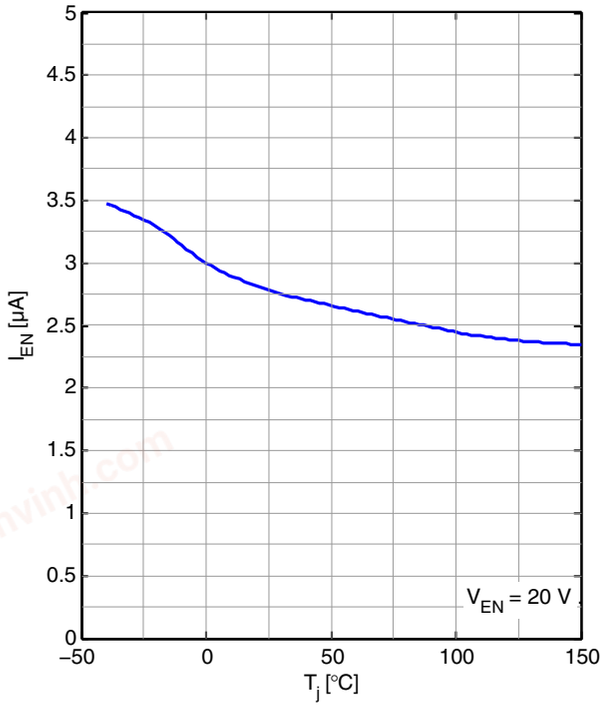
EN Pin Thresholds $V_{EN,th}$ versus Temperature T_j



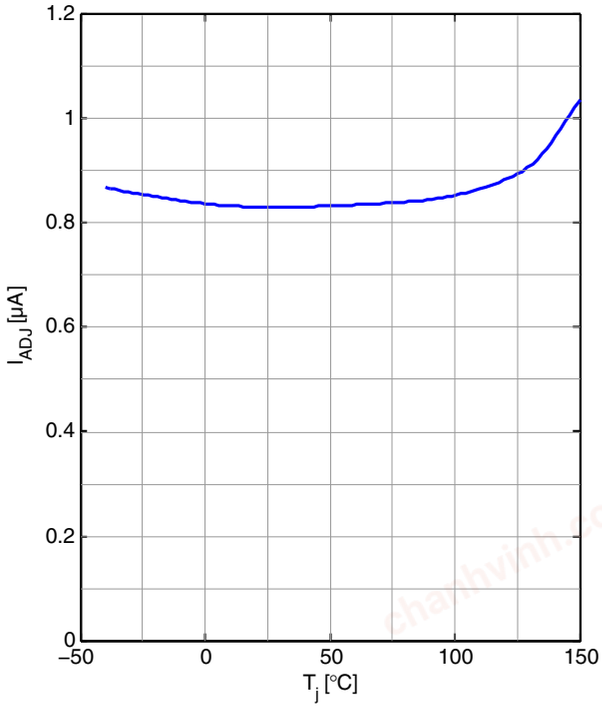
EN Pin Input Current I_{EN} versus EN Pin Voltage V_{EN}



EN Pin Input Current I_{EN} versus Temperature T_j

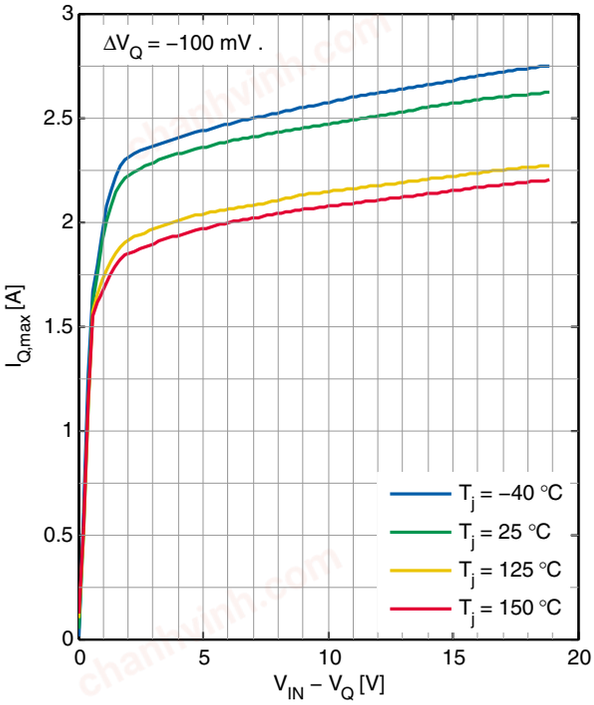


Adjustable Pin Bias Current I_{ADJ} versus Temperature T_j

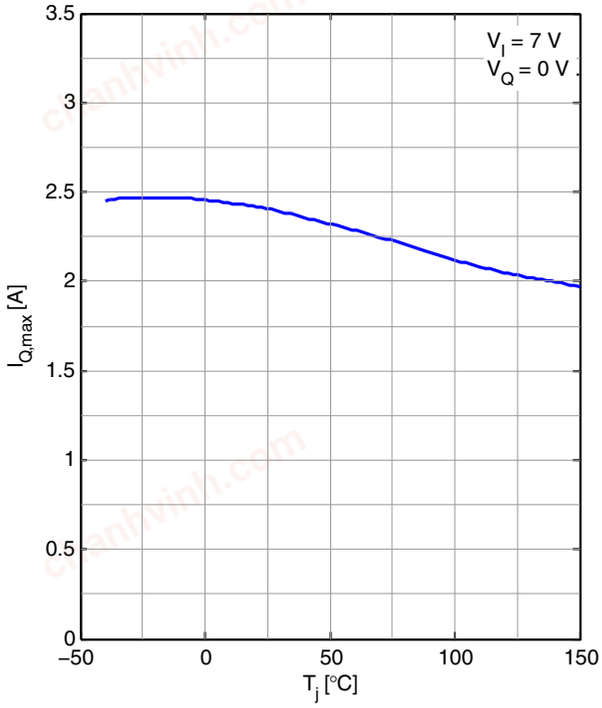


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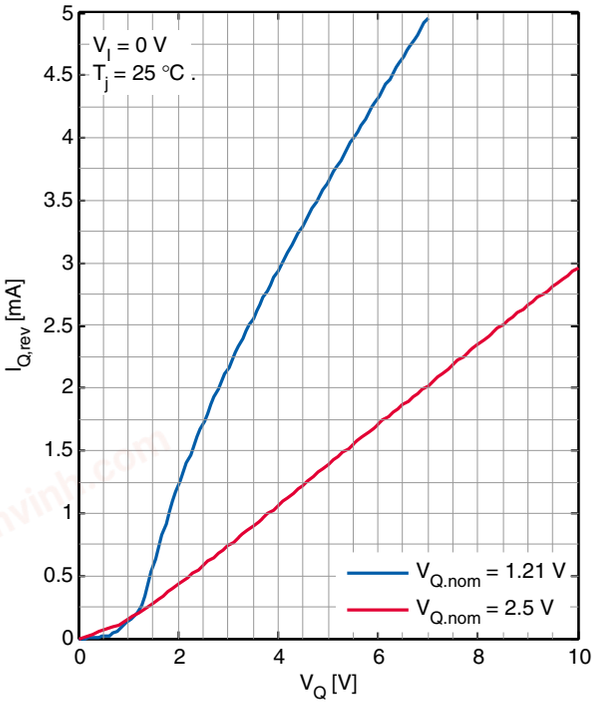
Current Limit $I_{Q,max}$ versus Input / Output Differential V_{IN} - V_Q



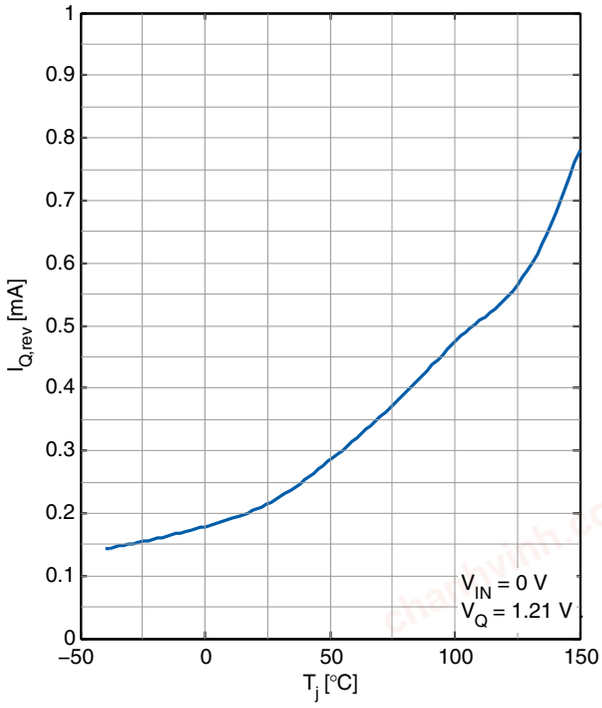
Current Limit $I_{Q,max}$ versus Temperature T_j



Reverse Output Current $I_{Q,rev}$ versus Output Voltage V_Q

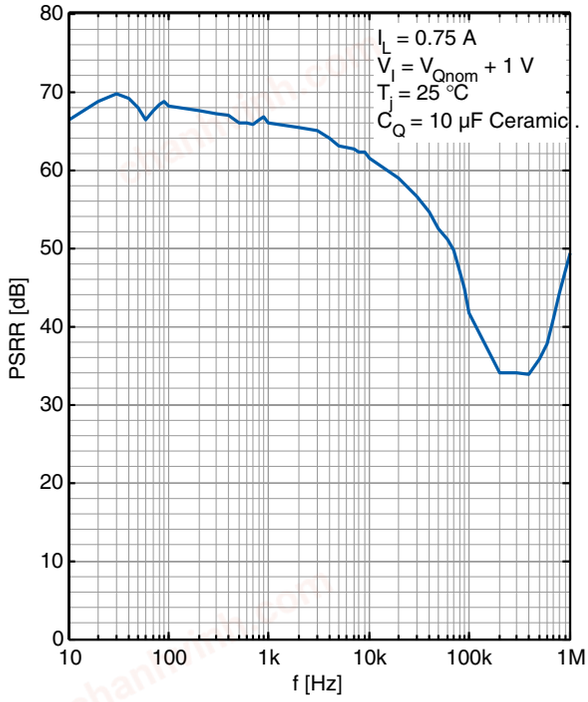


Reverse Output Current $I_{Q,rev}$ versus Temperature T_j

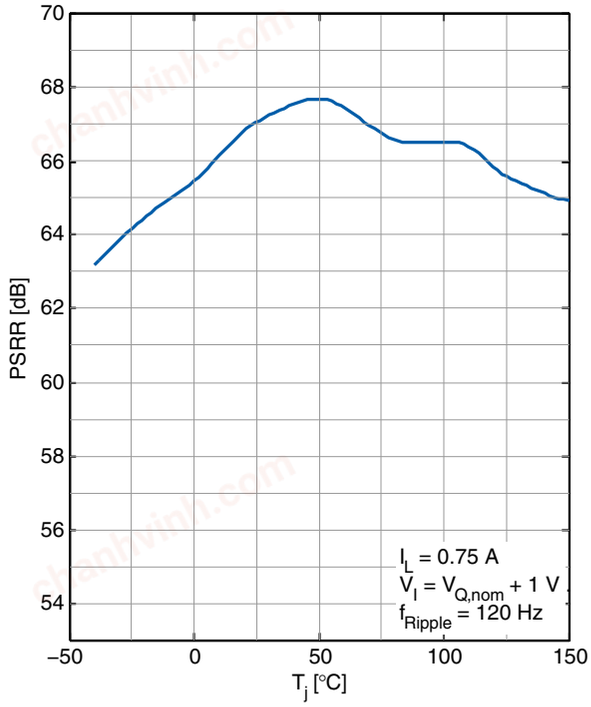


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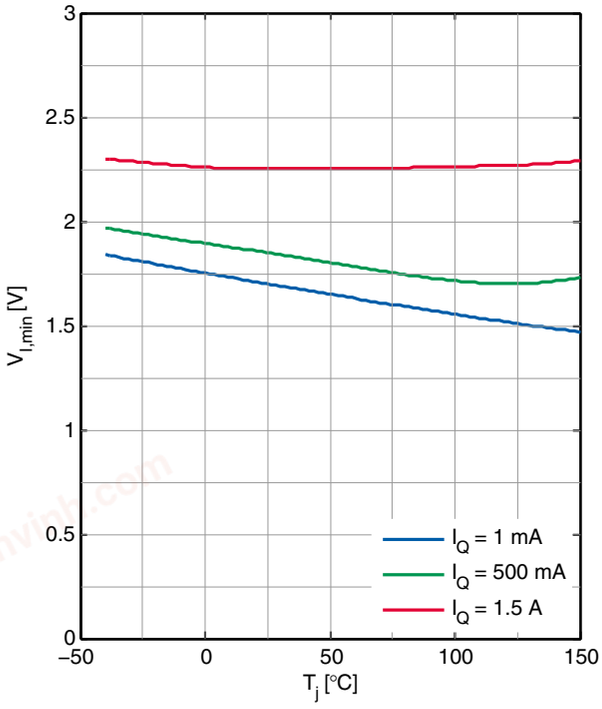
Ripple Rejection PSRR versus Frequency f



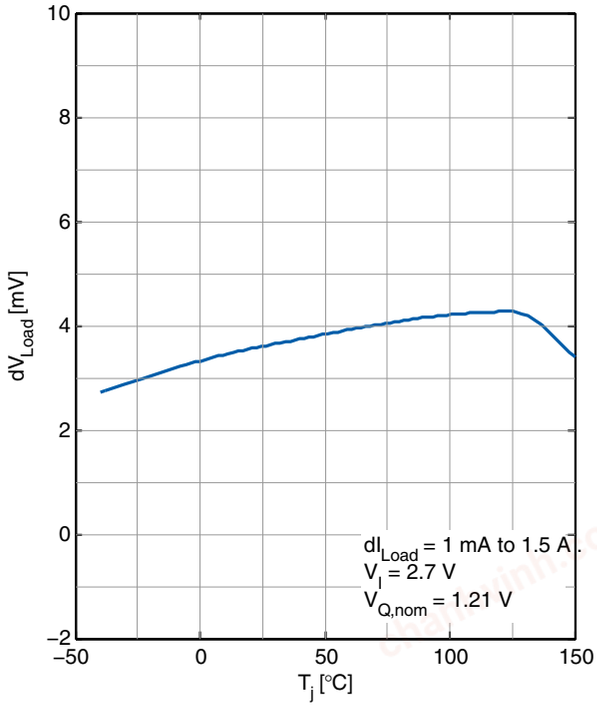
Ripple Rejection PSRR versus Temperature T_j



Minimum Input Voltage $V_{I,min}$ versus Temperature T_j

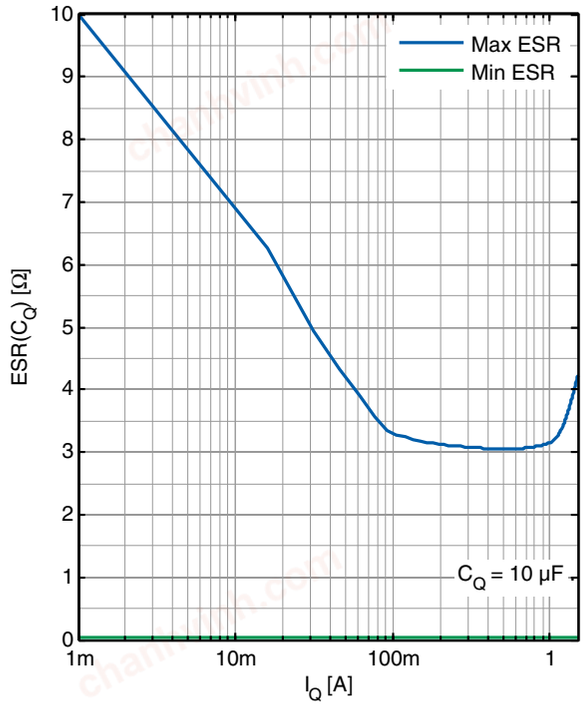


Load Regulation dV_{Load} versus Temperature T_j



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Equivalent Series Resistance $ESR(C_Q)$ vs Load Current I_Q



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6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

The TLF1963 is an 1.5 A low dropout regulator optimized for fast transient response. The device is capable of supplying 1.5 A at a very low dropout voltage up to a Junction Temperature of 150 °C. The low operating quiescent current of 1 mA drops to less than 1 µA in case the device is disabled. In addition to the low quiescent current, the TLF1963 incorporates several protection features which make them ideal for use in battery-powered systems. The device is protected against both reverse input and reverse output voltages.

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

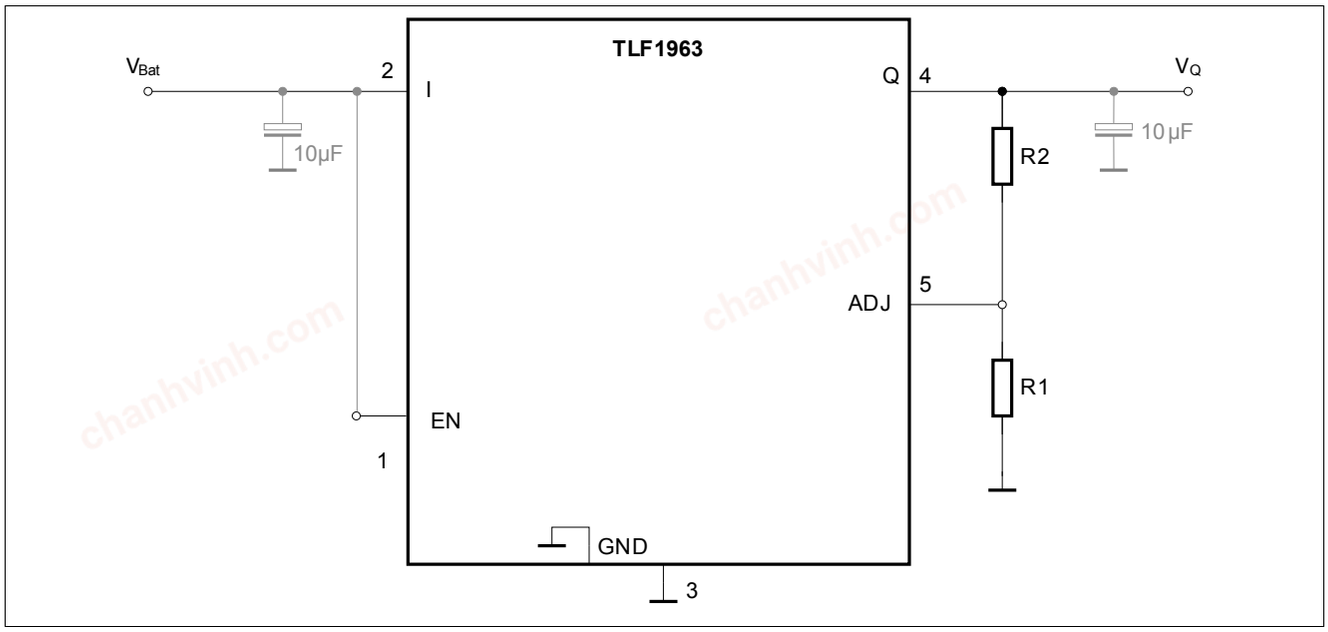


Figure 4 Application Diagram

6.1 Adjustable Operation

The TLF1963 has an output voltage range of 1.21 V to V_I - V_{dr} < 20 V. The output voltage is set by the ratio of two external resistors as shown in **Figure 4**. The device serves the output to maintain the voltage at the ADJ pin at 1.21 V referenced to ground. The current in R1 is then equal to 1.21 V / R1 and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 1 µA at 25 °C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula in **Equation (1)**.

$$V_Q = V_{ADJ} \cdot \left(1 + \frac{R_2}{R_1}\right) + I_{ADJ} \cdot R_2 \quad (1)$$

V_{ADJ} = 1.21 V typical
I_{ADJ} = 1 µA at 25 °C

The value of R1 is recommended to be smaller than 12 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off and the divider current will be zero.

The adjustable device is mainly tested and specified with the ADJ pin connected to the Q pin for an output voltage of 1.21 V. Specifications for output voltages adjusted to greater values than 1.21V will be proportional to the ratio of the desired output voltage to 1.21 V.

For example, load regulation for an output current change of 1 mA to 1.5 A is $\Delta V_{Q,load}$ = 2 mV typical at $V_{Q,nom}$ = 1.21 V.

At $V_{Q,nom}$ = 5 V, load regulation is: $\Delta V_{Q,load,5V}$ = (5 V / 1.21 V)•(2 mV) = 8.3 mV

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6.2 Output Capacitance and Transient Response

The TLF1963 is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10 µF with an ESR in the range of 10 mΩ to 3 Ω is recommended to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes.

6.3 Overload Recovery

The TLF1963 has a safe operating area protection. The device protects itself by limiting the output current to a maximum and prevent it self against destruction due to overload or short circuits conditions. In this cases the current is limited and the resulting output voltage decreases according to the load down to 0V in a short circuit condition.
The TLF1963 can supply the application for all input voltages between 2.5 V up to 20V with currents up to 1.5 A. Of course it needs to be ensured, that the junction temperature stays within the operating range up to 150 °C. For startup conditions with a high load current the TLF1963 is able to start up properly without exeeding the safe operating area. Even imediatly after removal of a short circuit failure case the device is able to start if the load current is very high. The characteristic of the current limitation can by seen in the typical perfomance graphs on Page 15.

6.4 Output Voltage Noise

The TLF1963 has been designed to provide low output voltage noise over the 10 Hz to 100 kHz bandwidth while operating at full load. Output voltage noise is typically 40 μV_{RMS} over this frequency bandwidth. For higher output voltages (generated by using a resistor divider), the output voltage noise will be gained up accordingly.

Higher values of output voltage noise may be measured when care is not exercised with regards to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TLF1963. Power supply ripple rejection must also be considered, because the TLF1963 does not have unlimited power supply ripple rejection and will pass a small portion of the input noise through to the output.

6.5 Protection Features

The TLF1963 has several protection features which makes him ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages and reverse output voltages.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 150 °C.

The input of the device will withstand reverse voltages of 20 V. Current flow out of the device will be limited to less than 2 mA in case of an input voltage of -20 V at the Input and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the TLF1963 can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20 V. The output will act like an open circuit, no current will flow out of the pin. If the input is powered by a voltage source, the output will source the short-circuit current of the device and will protect itself by thermal limiting. In this case, grounding the EN pin will turn off the device and stop the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the ADJ pin will act like an open circuit when pulled below ground and like a resistor (typically 4 kΩ) in series with a diode when pulled above ground.

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7 V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.21 V reference when the output is forced to

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20 V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5 mA when the ADJ pin is at 7 V. The 13 V difference between Q and ADJ pins divided by the 5 mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6 kΩ.

6.6 Further Application Information

- For further information you may contact **http://www.infineon.com/**

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7 Package Outlines

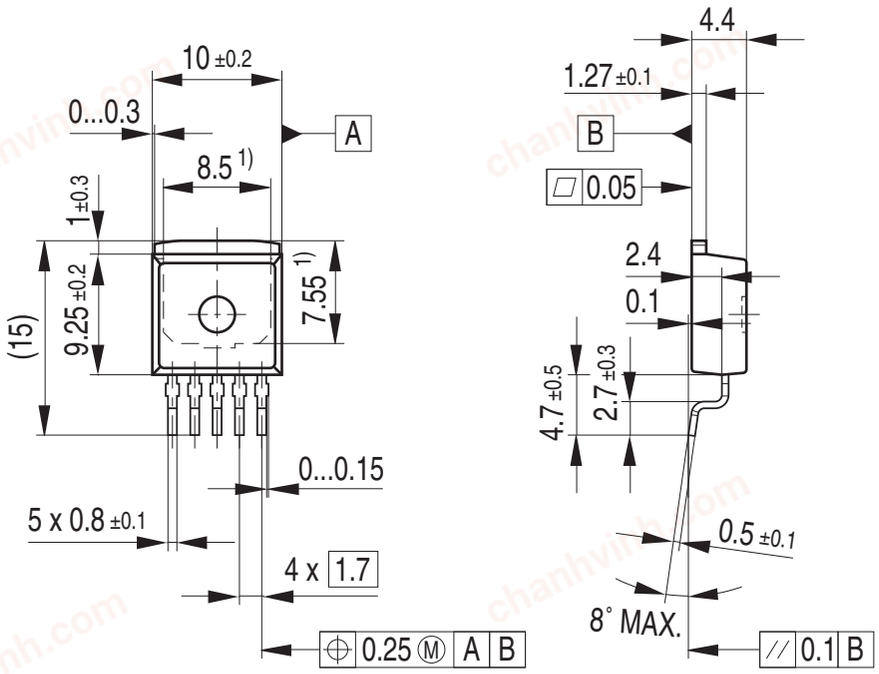


Figure 5 PG-TO263-5 SMD Package

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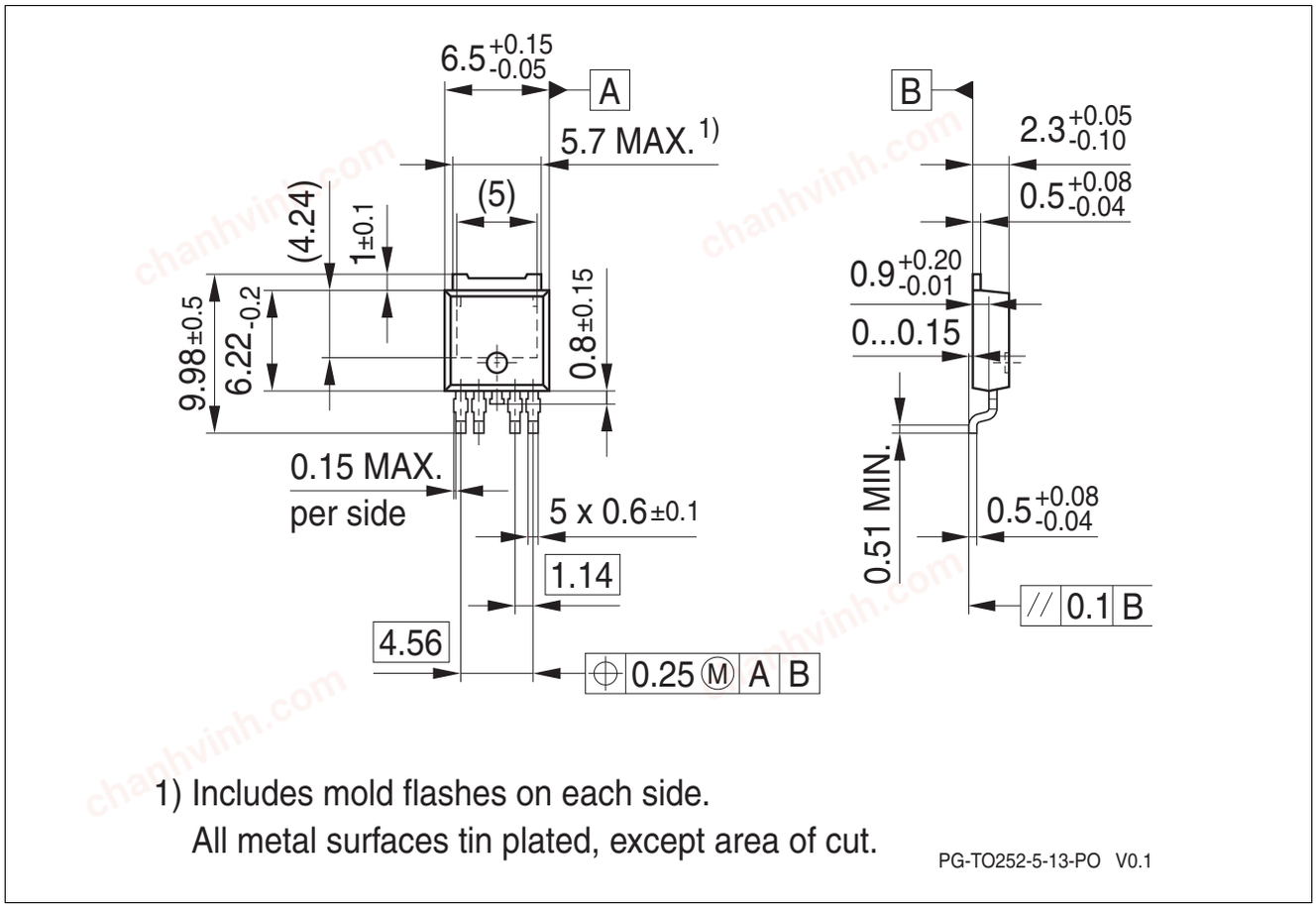


Figure 6 PG-TO252-5 SMD Package

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

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8 Revision History

Revision	Date	Changes
1.0	2012-11-08	Initial Version of Data Sheet

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