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TLE9842QX

Microcontroller with LIN and Power Switches for Automotive Applications

AEC Qualified RoHS



VQFN-48-31

1 Overview

Features

- 32-bit Arm® Cortex®*-M0 Core
  - up to 25 MHz clock frequency
  - one clock per machine cycle architecture
  - single cycle multiplier
- On-chip memory
  - 36 KB Flash (including EEPROM)
  - 4 KB EEPROM (emulated in Flash)
  - 768 bytes 100 Time Programmable Memory (100TP)
  - 2 KB RAM
  - Boot ROM for startup firmware and Flash routines
- On-chip OSC
- 2 Low-Side Switches incl. PWM functionality, can be used e.g. as relay driver
- 1 High-Side Switch with cyclic sense option and PWM functionality, e.g. for supplying LEDs or switch panels (min. 150 mA)
- 4 High Voltage Monitor Input pins for wake-up and with cyclic sense with analog measurement option
- 10 General-purpose I/O Ports (GPIO)
- 6 Analog input Ports
- 10-Bit A/D Converter with 6 analog inputs + VBAT_SENSE + VS + 4 high voltage monitoring inputs
- 8-Bit A/D Converter with 7 inputs for voltage and temperature supervision
- Measurement unit with 12 channels together with the onboard 10-Bit A/D converter and data post processing
- 16-Bit timers - GPT12, Timer 2 and Timer 21
- Capture/compare unit for PWM signal generation (CCU6)

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Type	Package	Marking
TLE9842QX	VQFN-48-31	TLE9842QX

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Overview

- 2 full duplex serial interfaces (UART1, UART2), UART1 with LIN support
- 2 synchronous serial channels (SSC1, SSC2)
- On-chip debug support via 2-wire SWD
- LIN Bootstrap loader to program the Flash via LIN (LIN BSL)
- 1 LIN 2.2 transceiver
- Single power supply from 3.0 V to 28 V
- Low-dropout voltage regulators (LDO)
- 5 V voltage supply VDDEXT for external loads (e.g. Hall-sensor)
- Core logic supply at 1.5 V
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes:
  - Micro Controller Unit slow-down mode
  - Sleep Mode with cyclic sense option
  - Cyclic wake-up during Sleep Mode
  - Stop Mode with cyclic sense option
- Power-on and undervoltage/brownout reset generator
- Overtemperature protection
- Short circuit protection for all voltage regulators and actuators (High Side, Low Side)
- Loss of clock detection with fail safe mode for power switches
- Temperature Range T_J: -40°C up to 150°C
- Package VQFN-48-31 with LTI feature
- Green package (RoHS compliant)
- AEC Qualified

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2 Block Diagram

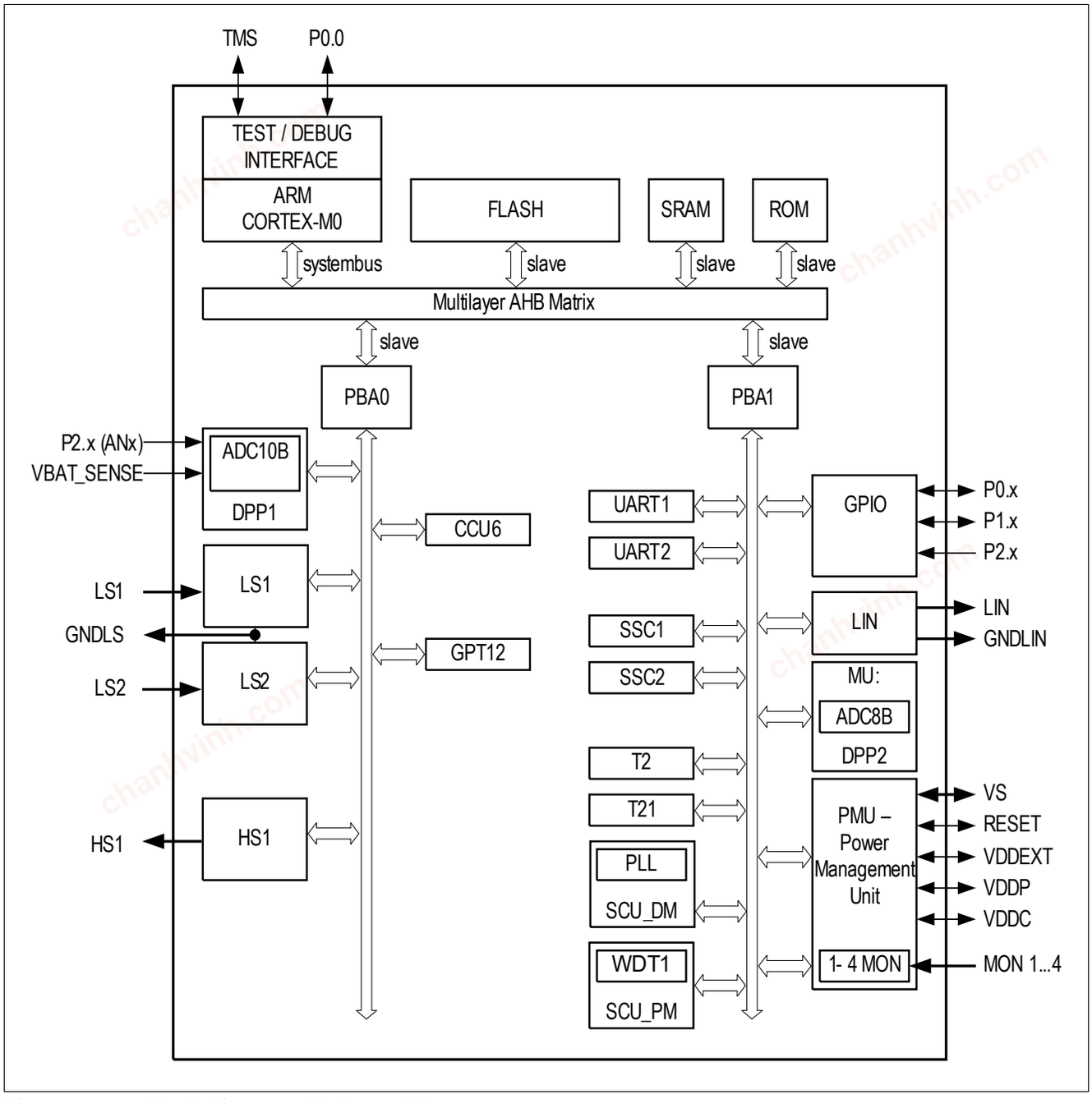


Figure 1 Block Diagram, TLE9842QX

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3 Device Pinout and Pin Configuration

3.1 Device Pinout

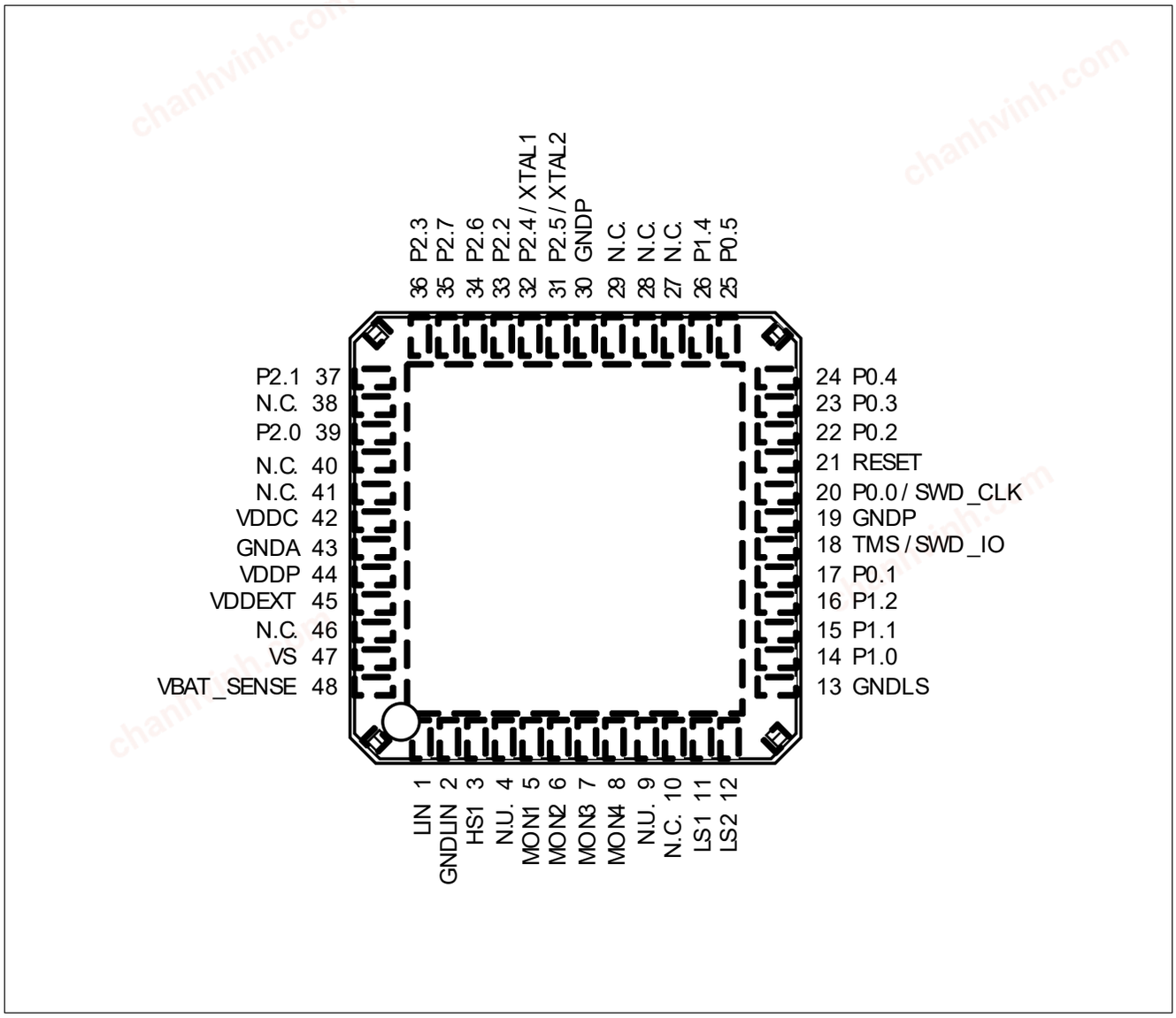


Figure 2 Device Pinout, TLE9842QX

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3.2 Pin Configuration

After reset, all pins are configured as input (except supply and LIN pins) with one of the following settings:

- Pull-up enabled only (PU)
- Pull-down enabled only (PD)
- Input with both pull-up and pull-down disabled (I)
- Output with output stage deactivated = high impedance state (Hi-Z)

The functions and default states of the TLE9842QX external pins are provided in the following table.

Type: indicates the pin type.

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

Not all alternate functions listed, see **Chapter 14**.

Table 1 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State	Function
P0				**Port 0** Port 0 is an 6-Bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.
P0.0	20	I/O	I/PU	SWD_CLK Serial Wire Debug Clock GPIO General Purpose IO Alternate function mapping see **Table 7**
P0.1	17	I/O	I/PU	GPIO General Purpose IO Alternate function mapping see **Table 7**
P0.2	22	I/O	I/PD	GPIO General Purpose IO Alternate function mapping see **Table 7**
P0.3	23	I/O	I/PU	GPIO General Purpose IO Alternate function mapping see **Table 7**
P0.4	24	I/O	I/PU	GPIO General Purpose IO Alternate function mapping see **Table 7**
P0.5	25	I/O	I/PU	GPIO General Purpose IO Alternate function mapping see **Table 7**
P1				**Port 1** Port 1 is an 4-Bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.
P1.0	14	I/O	I	GPIO General Purpose IO Alternate function mapping see **Table 8**
P1.1	15	I/O	I	GPIO General Purpose IO Alternate function mapping see **Table 8**
P1.2	16	I/O	I	GPIO General Purpose IO Alternate function mapping see **Table 8**

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Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P1.4	26	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 8**
P2				**Port 2** Port 2 is an 8-Bit general purpose input-only port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.	
P2.0	39	I	I	AN0	ADC1 analog input channel 12 Alternate function mapping see **Table 9**
P2.1	37	I	I	AN1	ADC1 analog input channel 7 Alternate function mapping see **Table 9**
P2.2	33	I	I	AN2	ADC1 analog input channel 8 Alternate function mapping see **Table 9**
P2.3	36	I	I	AN3	ADC1 analog input channel 9 Alternate function mapping see **Table 9**
P2.4	32	I	I	XTAL1[1)]	Alternate function mapping see **Table 9** External oscillator input
P2.5	31	I O	I Hi-Z	XTAL2[1)]	Alternate function mapping see **Table 9** External oscillator output
P2.6	34	I	I	AN6	ADC1 analog input channel 10 Alternate function mapping see **Table 9**
P2.7	35	I	I	AN7	ADC1 analog input channel 11 Alternate function mapping see **Table 9**
Power Supply					
VS	47	P	–	Battery supply input	
VDDP	44	P	–	I/O port supply (5.0 V). Do not connect external loads. For buffer and bypass capacitors	
VDDC	42	P	–	Core supply (1.5 V during Active Mode, reduced voltage during Stop Mode). Do not connect external loads. For buffer/bypass capacitor	
VDDEXT	45	P	–	External voltage supply output (5.0 V, 20 mA)	
GNDLS	13	P	–	Low-side ground LS1, LS2	
GNDP	19, 30	P	–	Core supply ground	
GNDA	43	P	–	Analog supply ground	
GNDLIN	2	P	–	LIN ground	
Monitor Inputs					
MON1	5	I	I	High Voltage Monitor Input 1	
MON2	6	I	I	High Voltage Monitor Input 2	
MON3	7	I	I	High Voltage Monitor Input 3	
MON4	8	I	I	High Voltage Monitor Input 4	
High-Side Switch / Low-Side Switch Outputs					

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Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
LS1	11	O	Hi-Z	Low-Side switch output 1
LS2	12	O	Hi-Z	Low-Side Switch output 2
HS1	3	O	Hi-Z	High-Side Switch output 1
LIN Interface				
LIN	1	I/O	PU	LIN bus interface input/output
Others				
TMS	18	I	I/PD	TMS Test mode select input SWD_IO Serial Wire Debug input/output
RESET	21	I/O	I/O/PU	Reset input/output, not available during Sleep Mode
VBAT_SENSE	48	I	I	Battery supply voltage sense input
N.C.	10, 27, 28, 29, 38, 40, 41, 46	–	–	Not connected, can be connected to GND
N.U.	4, 9	–	–	Not Used; see **Chapter 27.2**
EP	–	–	–	Exposed Pad, connect to GND

1) configurable by user

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4 Modes of Operation

This highly integrated circuit contains analog and digital functional blocks. For system and interface control an embedded 32-Bit Cortex®-M0 microcontroller is included. For internal and external power supply purposes, on-chip low drop-out regulators are existent. An internal oscillator (no external components necessary) provides a cost effective and suitable clock in particular for LIN slave nodes. As communication interface, a LIN transceiver and several High Voltage Monitor Inputs with adjustable threshold and filters are available. Furthermore oneHigh-Sides Switche (e.g. for driving LEDs or powering of switches), two low-side switches (e.g. for relays) and several general purpose input/outputs (GPIO) with pulse-width modulation (PWM) capabilities are available.

The Micro Controller Unit supervision and system protection including reset feature is controlled by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support terminal 30 connected automotive applications. A wake-up from the power saving mode is possible via a LIN bus message, via the monitoring inputs or repetitive with a programmable time period (cyclic wake-up).

The integrated circuit is available in a package with 0.5 mm pitch and is designed to withstand the challenging conditions of automotive applications.

The TLE9842QX has several operational modes mainly to support low power consumption requirements. The low power modes and state transitions are depicted in **Figure 3** below.

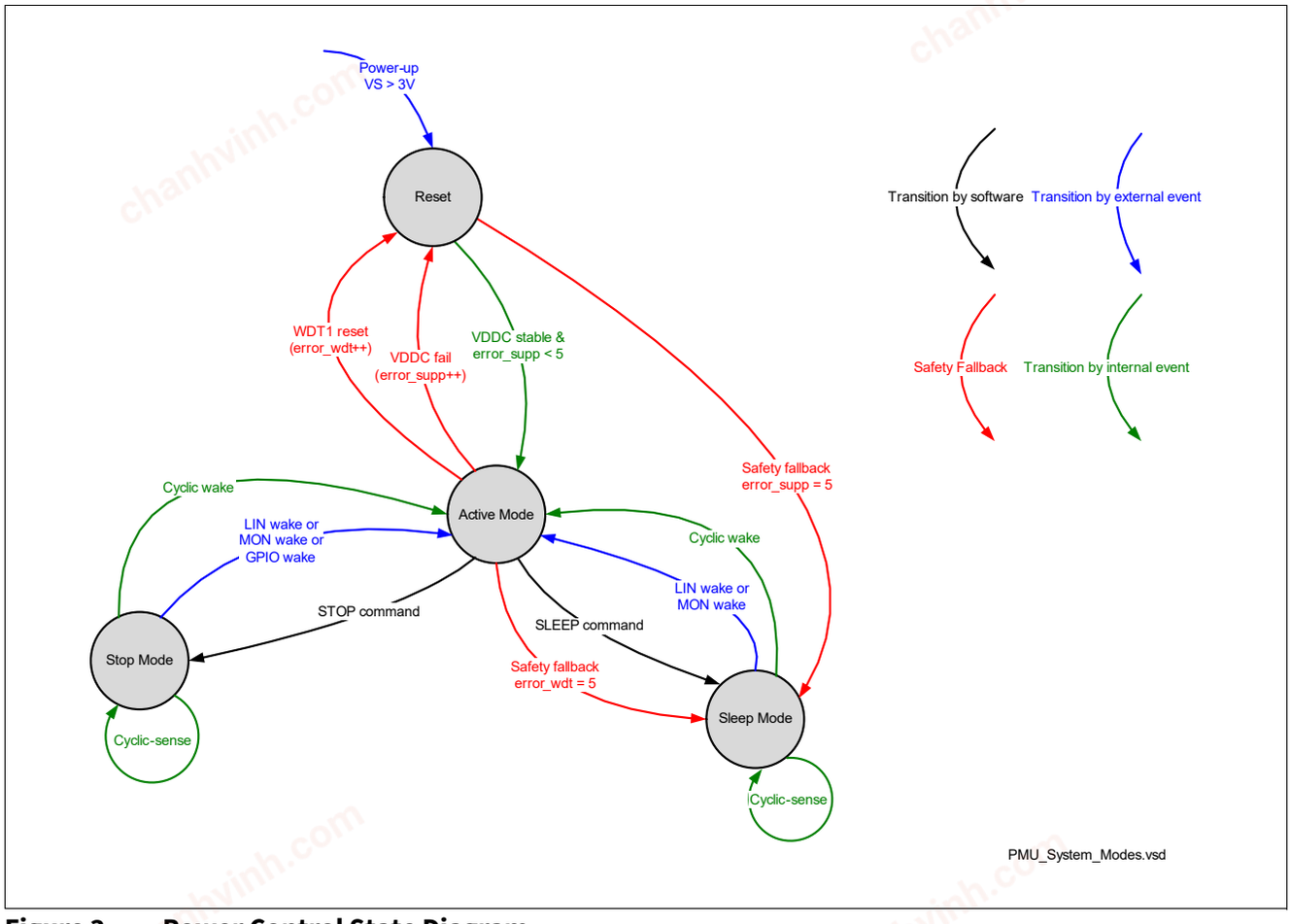


Figure 3 Power Control State Diagram

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Modes of Operation

Reset Mode

The Reset Mode is a transition mode e.g. during power-up of the device after a power-on reset. In this mode the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the Active Mode is entered. In case the watchdog timer WDT1 fails for more than four times, a fail-safe transition to the Sleep Mode is done.

Active Mode

In Active Mode all modules are activated and the TLE9842QX is fully operational.

Stop Mode

The Stop Mode is one out of two major low power modes. The transition to the low power modes is done by setting the respective Bits in the mode control register. In Stop Mode the embedded microcontroller is still powered allowing faster wake-up reaction times, but not clocked. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pins or the respective 5V GPIOs.

Sleep Mode

The Sleep Mode is a major low-power mode. The transition to the low-power modes is done by setting the respective Bits in the Micro Controller Unit mode control register. The sleep time is configurable. In Sleep Mode the embedded microcontroller power supply is deactivated, allowing the lowest system power consumption, but the wake-up time is longer compared to the Stop Mode. In this mode a 64 bit wide buffer for data storage is available. A wake-up from this mode is possible by LIN bus activity or the High Voltage Monitor Input pins and cyclic wake. A wake-up from Sleep Mode behaves similar to a power-on reset. While changing into Sleep Mode, no incoming wake-requests are lost (i.e. no dead-time). It is possible to enter sleep-mode even with LIN dominant.

Cyclic Wake-up Mode

The cyclic wake-up mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic wake-up mode is done by first setting the respective Bits in the mode control register followed by the SLEEP or STOP command. Additional to the cyclic wake-up behavior (wake-up after a programmable time period), the wake-up sources of the normal Stop Mode and Sleep Mode are available.

Cyclic Sense Mode

The cyclic sense mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic sense mode is done by first setting the respective Bits in the mode control register followed by the STOP or SLEEP command. In cyclic sense mode the High-Side Switch can be switched on periodically for biasing some switches for example. The wake-up condition is configurable, when the sense result of defined monitor inputs at a window of interest changed compared to the previous wake-up period or reached a defined state respectively. In this case the Active Mode is entered immediately.

The following table shows the possible power mode configurations of each major module or function respectively.

Table 2 Power Mode Configurations

Module/function	Active Mode	Sleep Mode	Stop Mode	Comment
VPRE, VDDP, VDDC	ON	OFF	ON	–
VDDEXT	ON/OFF	OFF	cyclic ON/OFF	–
HSx	ON/OFF	cyclic ON/OFF	cyclic ON/OFF	cyclic sense

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Table 2 Power Mode Configurations (cont'd)

Module/function	Active Mode	Sleep Mode	Stop Mode	Comment
LSx	ON/OFF	OFF	OFF	–
LIN TRx	ON/OFF	wake-up only / OFF	wake-up only/ OFF	–
MONx (wake-up)	n.a.	disabled/static/ cyclic	disabled/static/ cyclic	cyclic: combined with HS=on
MONx (measurement)	ON/OFF	OFF	OFF	available on all channels
VS sense	ON/OFF brownout detection	brownout detection	brownout detection	brownout det. done in PCU
VBAT_SENSE	ON/OFF	OFF	OFF	–
GPIO 5V	ON	OFF	ON	–
WDT1	ON	OFF	OFF	–
CYCLIC WAKE	n.a.	cyclic wake-up/ cyclic sense/OFF	cyclic wake-up/ cyclic sense/OFF	cyclic sense with HS; wake-up needs MC for enter Sleep Mode again
Measurement	ON[1)]	OFF	OFF	–
Micro Controller Unit	ON/slow-down/STOP	OFF	OFF	–
CLOCK GEN (MC)	ON	OFF	OFF	–
LP_CLK (f_{LP_CLK})	ON	OFF	OFF	WDT1
LP_CLK2 (f_{LP_CLK2})	ON	ON	ON	for cyclic wake-up

1) May not be switched off due to safety reasons

Wake-up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. It is ensured, that no wake-up event is lost.

As default wake-up sources, MON inputs and cyclic wake are activated after power-on reset, LIN is disabled as wake-up source by default.

Wake-up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for each monitor input individually.

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5 Power Management Unit (PMU)

5.1 Features

- System modes control (startup, sleep, stop and active)
- Power management (cyclic wake)
- Control of system voltage regulators with diagnosis (overload, short, overvoltage)
- Fail safe mode detection and operation in case of system errors (watchdog fail)
- Wake-up sources configuration and management (LIN, MON, GPIOs)
- System error logging

5.2 Introduction

The purpose of the power management unit is to ensure the fail safe behavior of the system IC. Therefore the power management unit controls all system modes including the corresponding transitions. The power management unit is responsible for generating all needed voltage supplies for the embedded MCU (VDDC, VDDP) and the external supply (VDDEXT). Additionally, the PMU provides well defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functionalities especially the reset behavior of the embedded MCU. All these functions are controlled by finite state machines. The system master functionality of the PMU requires the generation of an independent logic supply and system clock. Therefore the PMU has a module internal logic supply and system clock which works independently of the MCU clock.

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5.2.1 Block Diagram

The following figure shows the structure of the Power Management Unit. **Table 3** describes the submodules more detailed.

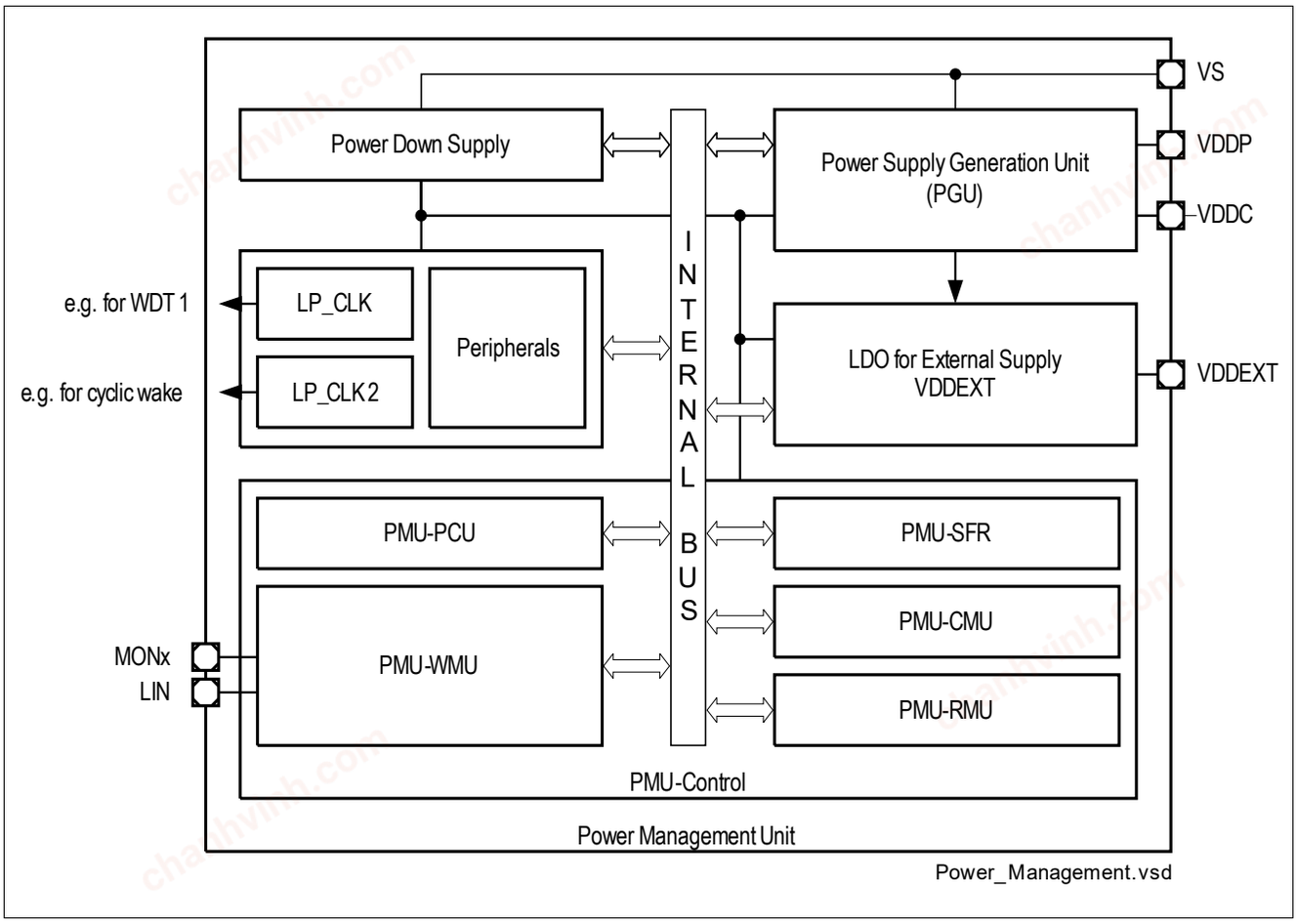


Figure 4 Power Management Unit Block Diagram

Table 3 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent Supply Voltage Generation for PMU	This supply is dedicated to the PMU to ensure an independent operation from generated power supplies (VDDP, VDDC).
LP_CLK (= f_{LP_CLK})	- Clock Source for all PMU submodules - Backup Clock Source for System - Clock Source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL Clock failure and as independent clock source for WDT1.
LP_CLK2 (= f_{LP_CLK2})	Clock Source for PMU	This ultra low power oscillator generates the clock for the PMU in Stop Mode and in the cyclic modes.
Peripherals	Peripheral Blocks of PMU	These blocks include the analog peripherals to ensure a stable and fail safe PMU startup and operation (bandgap, bias).

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Table 3 Description of PMU Submodules (cont'd)

Mod. Name	Modules	Functions
Power Supply Generation Unit (PGU)	Voltage regulators for VDDP and VDDC	This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC).
VDDEXT	Voltage regulator for VDDEXT to supply external modules (e.g. Sensors)	This voltage regulator is a dedicated supply for external modules.
PMU-SFR	All PMU relevant Extended Special Function Registers	This module contains all PMU relevant registers, which are needed to control and monitor the PMU.
PMU-PCU	Power Control Unit of the PMU	This block is responsible for controlling all power related actions within the PGU Module.It also contains all regulator related diagnosis like under- and overvoltage detection, overcurrent and short circuit diagnoses.
PMU-WMU	Wake-up Management Unit of the PMU	This block is responsible for controlling all Wake-up related actions within the PMU Module.
PMU-CMU	Cyclic Management Unit of the PMU	This block is responsible for controlling all actions within cyclic mode.
PMU-RMU	Reset Management Unit of the PMU	This block generates resets triggered by the PMU like undervoltage or short circuit reset, and passes all resets to the relevant modules and their register. A reset status register with every reset source is available.

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5.2.2 PMU Modes Overview

The following state diagram shows the available modes of the device.

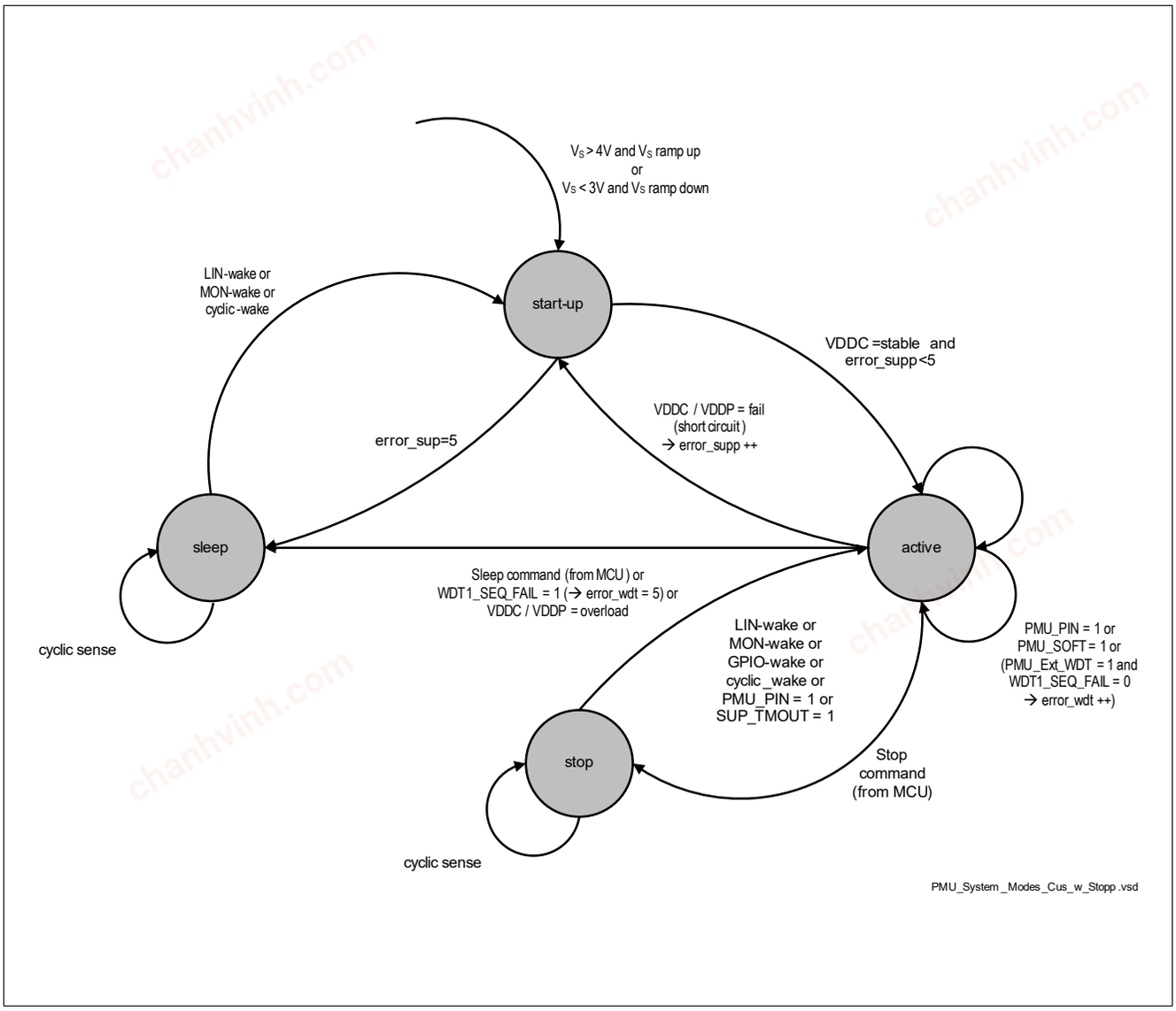


Figure 5 Power Management Unit System Modes

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5.3 Power Supply Generation (PGU)

5.3.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which provides the pad supply for the parallel port pins and other 5 V analog functions (e.g. LIN Transceiver).

Features

- 5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with Reset (Undervoltage Reset, V_{DDPUV})
- Overtemperature shutdown with MCU signalling (Interrupt)
- Pre-Regulator for VDDC Regulator
- GPIO Supply
- Pull Down Current Source at the output for Sleep Mode only (typ.5 mA)

The output capacitor C_{VDDP} is mandatory to ensure a proper regulator functionality.

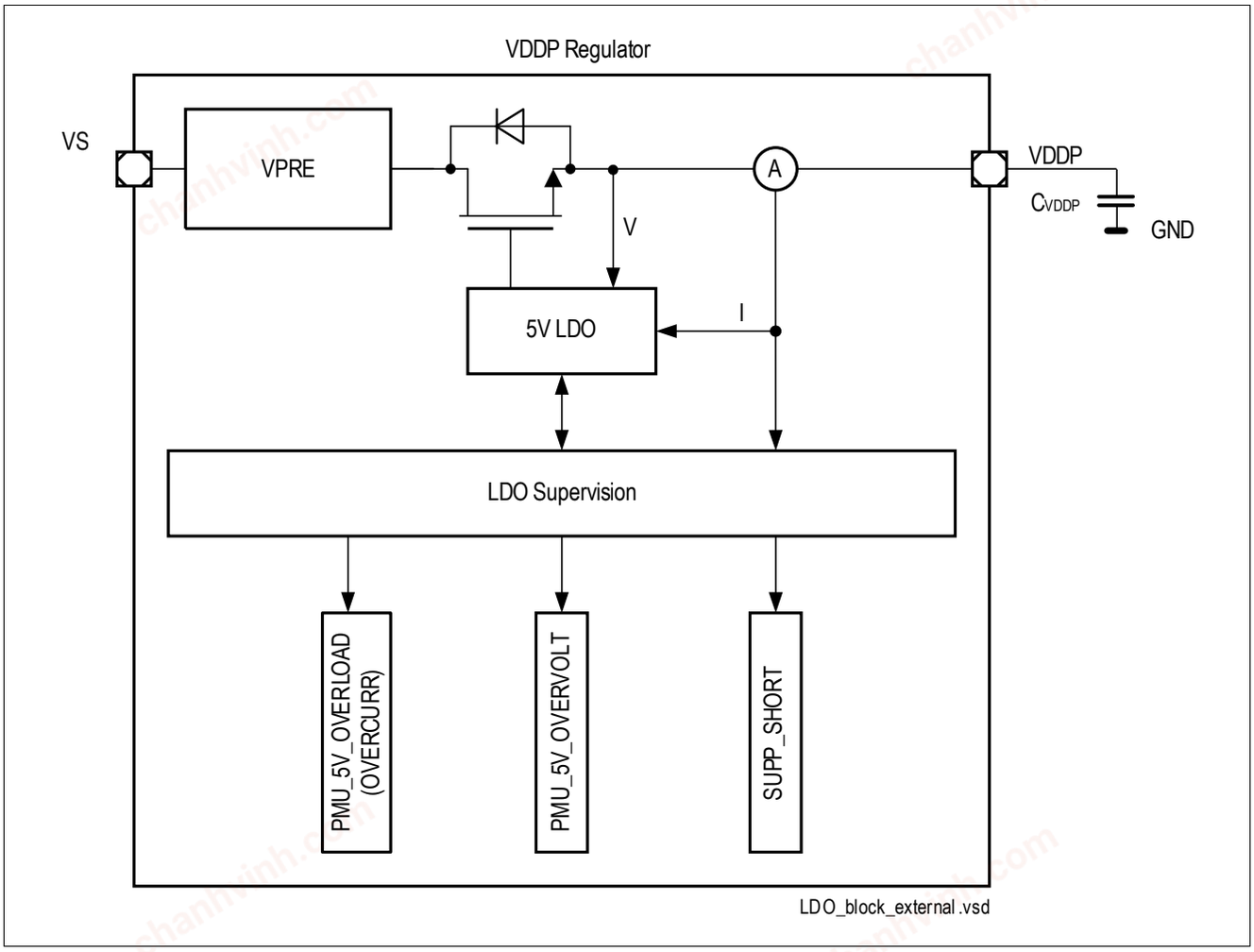


Figure 6 Module Block Diagram of VDDP Voltage Regulator

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5.3.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which provides the supply for the microcontroller core, digital peripherals and other chip internal analog 1.5 V functions (e.g. ADC).

Features

- 1.5 V low-drop voltage regulator
- Overcurrent monitoring and Shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with reset
- Overtemperature Shutdown with MCU signalling (Interrupt)
- Pull Down Current Source at the output for Sleep Mode only (typ. 100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

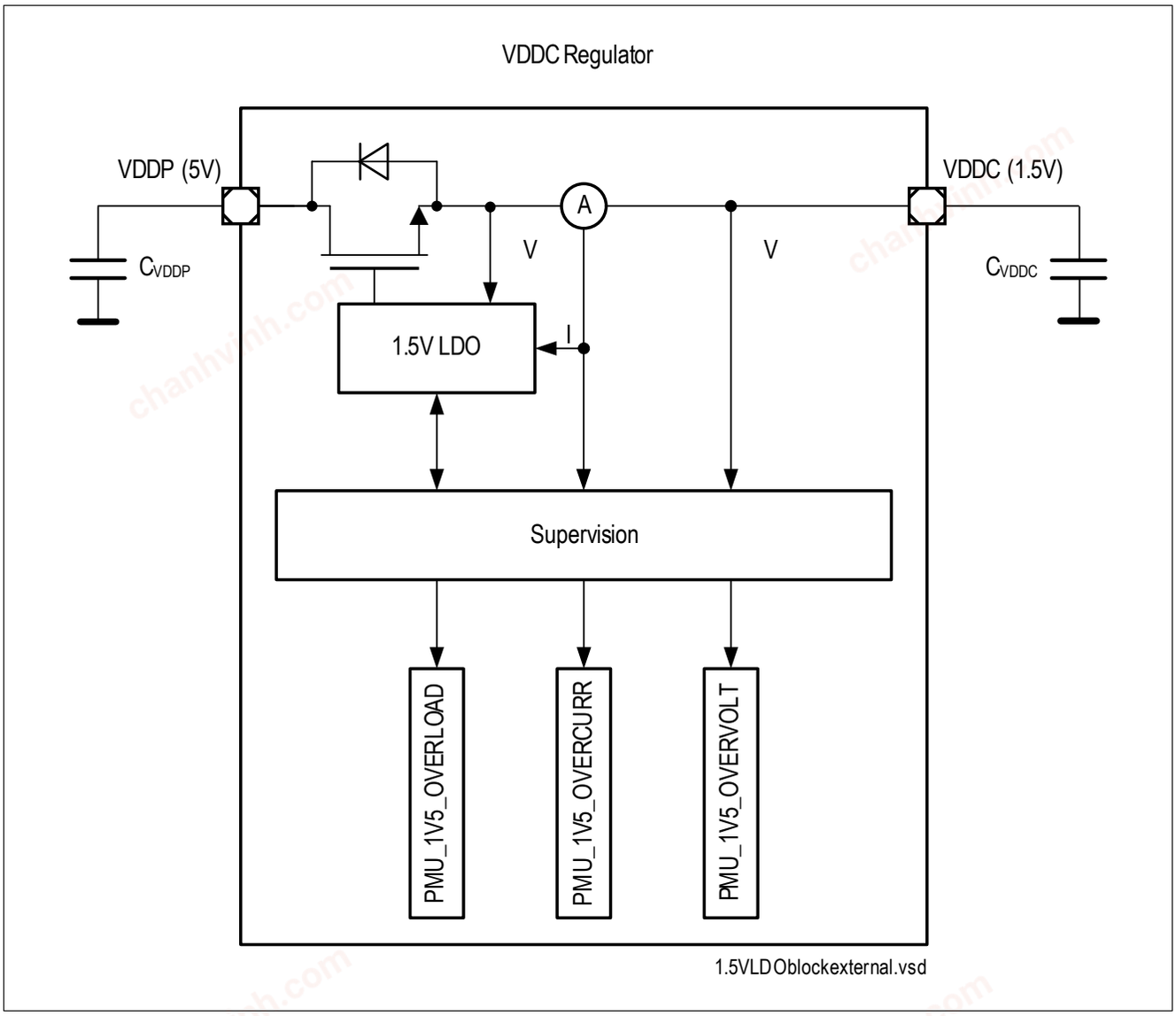


Figure 7 Module Block Diagram of VDDC Voltage Regulator

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5.3.3 External Voltage Regulator 5.0V (VDDEXT)

This module represents the 5 V voltage regulator, which serves as a supply for external circuits. It can be used e.g. to supply an external sensor, LEDs or potentiometers.

Features

- Switchable (by software) +5 V, low-drop voltage regulator
- Switch-on undervoltage blanking time in order to drive small capacitive loads
- Intrinsic current limitation
- Undervoltage monitoring and shutdown with MCU signalling (Interrupt)
- Overtemperature Shutdown with MCU signalling (Interrupt)
- Pull Down Current Source at the output for Sleep Mode only (typ. 100 µA)
- Cyclic sense option together with GPIOs
- Low current mode available to ensure reduced stop mode current consumption. In this mode current capability is reduced to I_{VDDEXT_LCM}

The output capacitor C_{VDDEXT} is mandatory to ensure a proper regulator functionality.

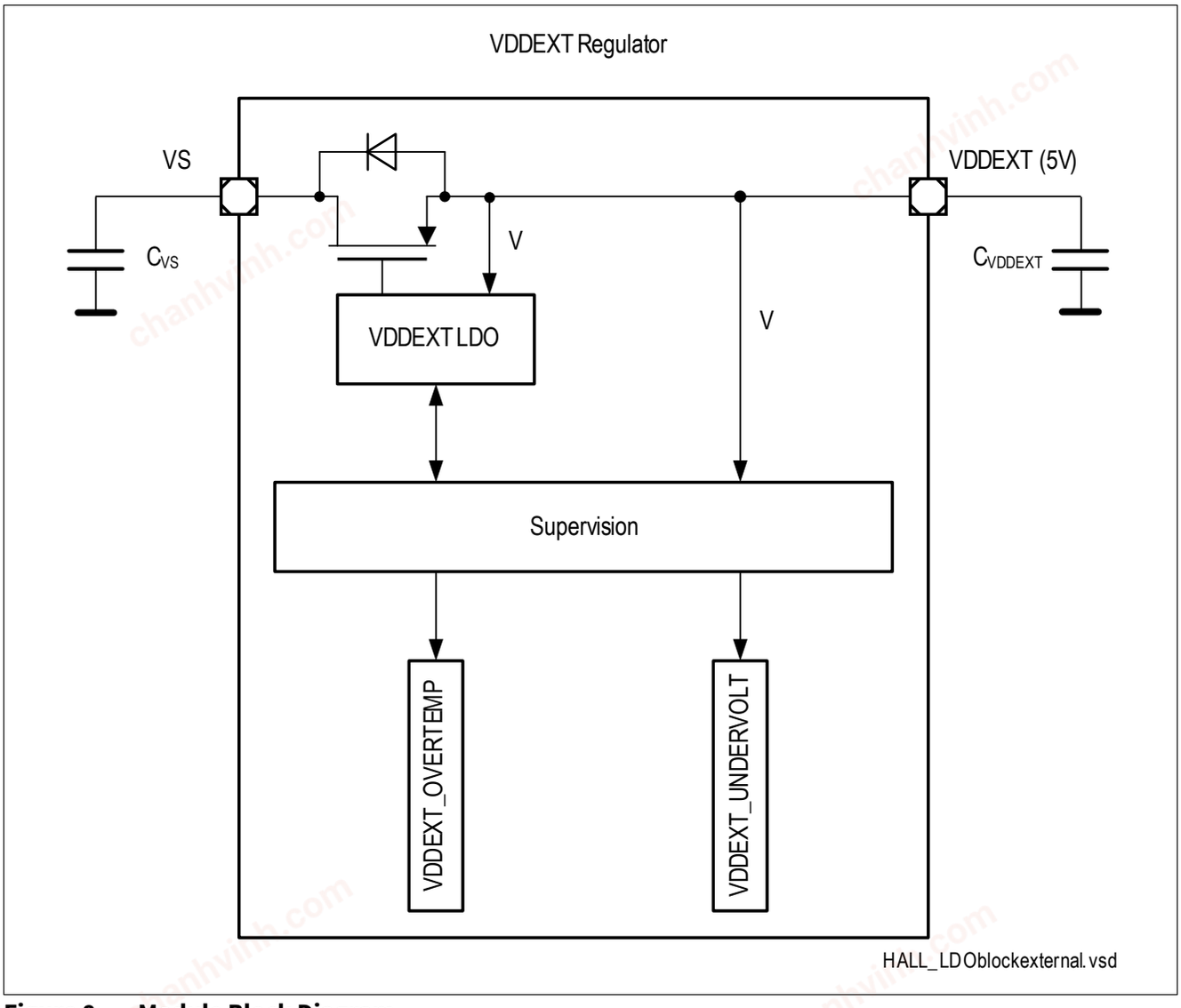


Figure 8 Module Block Diagram

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5.3.4 Power-on Reset Concept

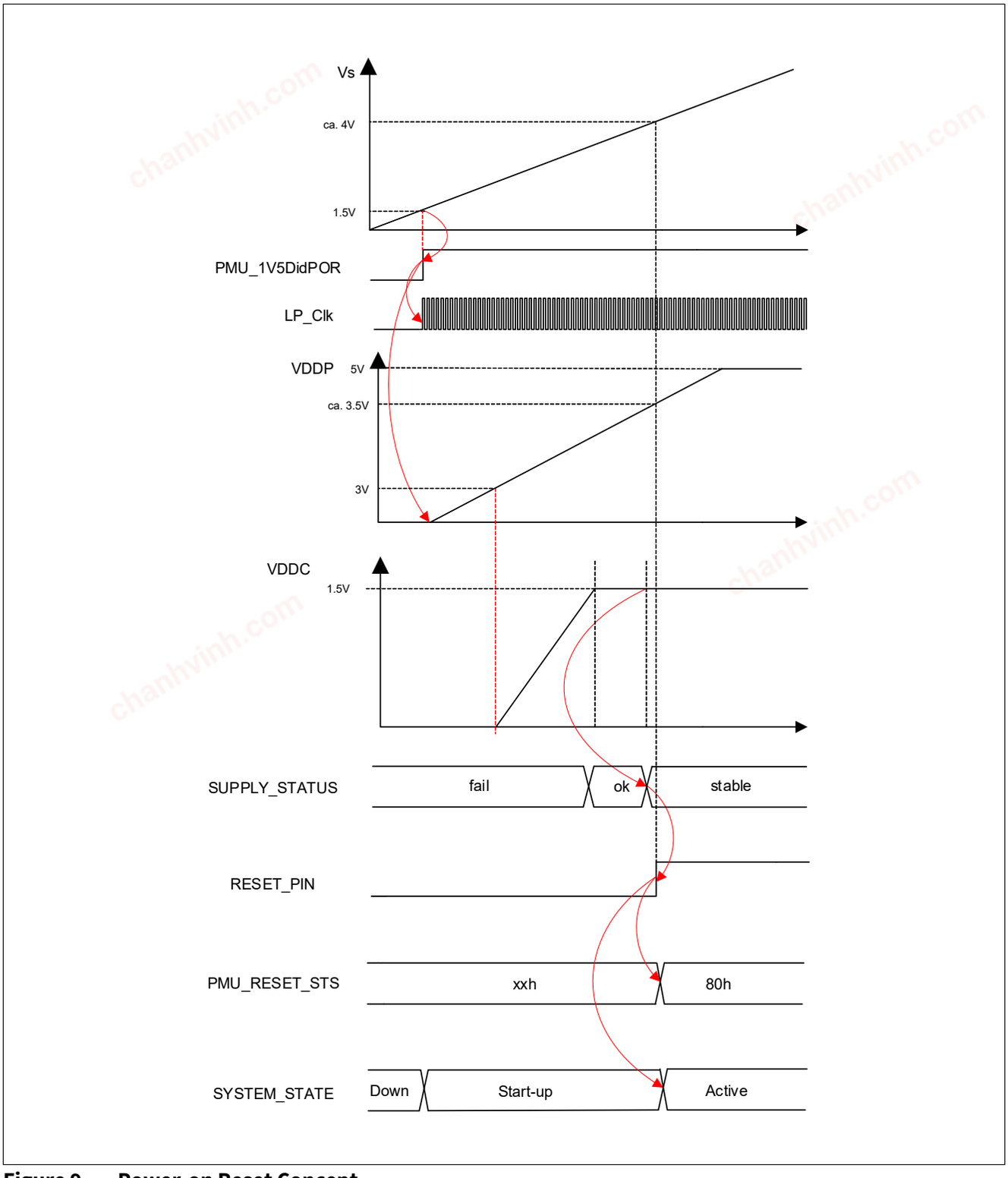


Figure 9 Power-on Reset Concept

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6 System Control Unit - Digital Modules (SCU-DM)

6.1 Features

- Flexible clock configuration features
- Reset management of all system resets
- System modes control for all power modes (active, power down, sleep)
- Interrupt enabling for many system peripherals
- General purpose input output control
- Debug mode control of system peripherals

6.2 Introduction

The System Control Unit (SCU) supports all central control tasks in the TLE9842QX. The SCU is made up of the following sub-modules:

- Clock System and Control (CGU)
- Reset Control (RCU)
- Power Management (PCU)
- Interrupt Management (ICU)
- General Port Control
- Flexible Peripheral Management
- Module Suspend Control
- Error Detection and Correction in Data Memory
- Miscellaneous Control
- Register Mapping

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6.2.1 Block Diagram

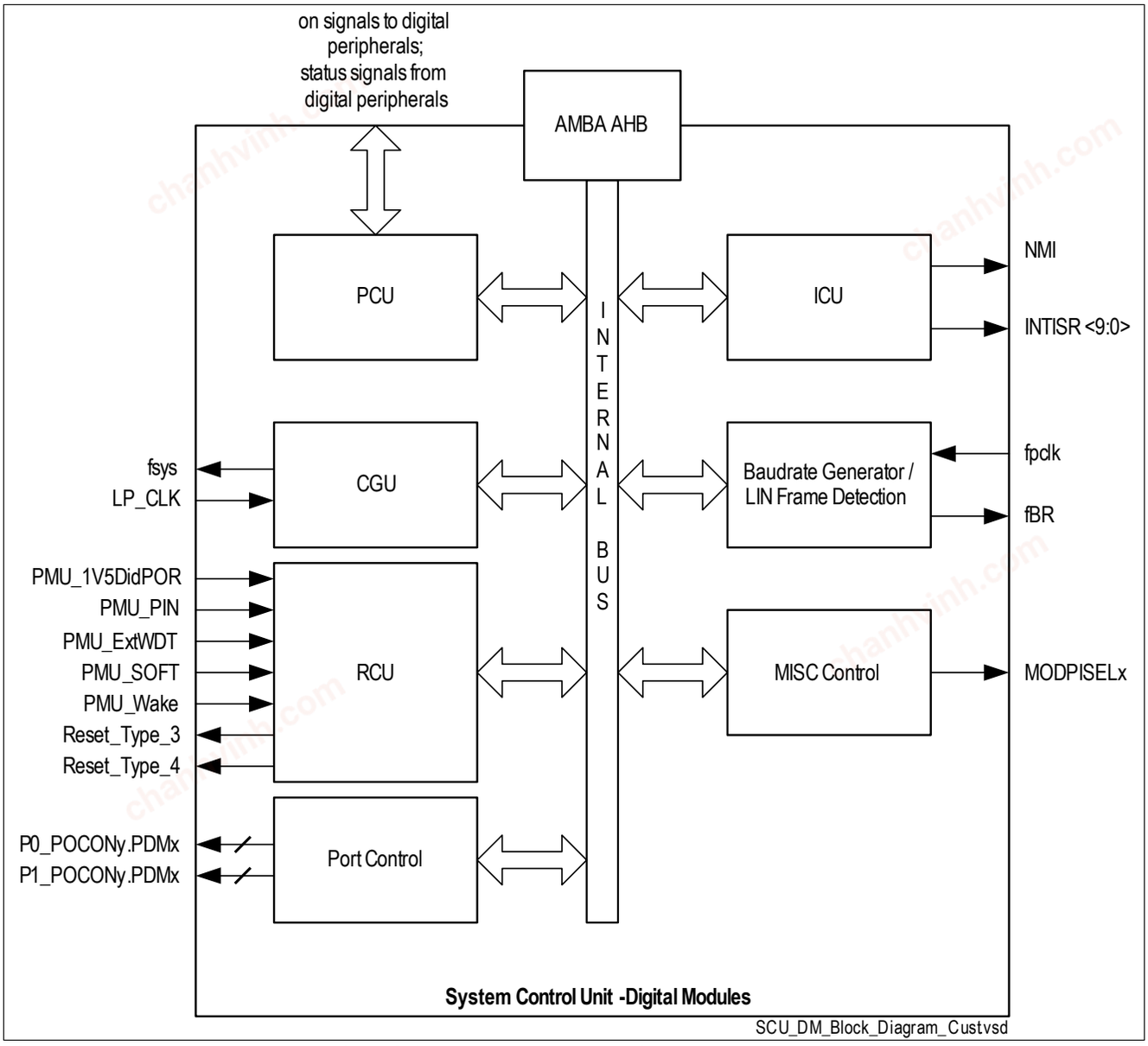


Figure 10 System Control Unit - Digital Modules Block Diagram

IO description of SCU_DM:

- CGU:
  - f_{sys}; system clock
  - LP_CLK; low-power backup clock
- RCU:
  - 1V5DidPOR; Undervoltage reset of power down supply
  - PMU_PIN; Reset generated by reset pin
  - PMU_ExtWDT; WDT1 reset
  - PMU_SOFT; Software reset
  - PMU_Wake; Stop Mode exit with reset

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  - Reset_Type_3; Peripheral reset (contains all resets)
  - Reset_Type_4; Peripheral reset (without SOFT)
- Baudrate generator:
  - f_{BR}; Baudrate clock for UART
- Port Control:
  - P0_POCONy.PDMx; driver strength control
  - P1_POCONy.PDMx; driver strength control
- MISC:
  - MODPISELx; Mode selection registers for UART (source selection) and Timer (trigger or count selection)

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6.3 Clock Generation Unit

The Clock Generation Unit (CGU) provides a flexible clock generation for TLE9842QX. During user program execution the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore the power consumption can be adapted to the actual application state.

The CGU in the TLE9842QX consists of one oscillator circuit (OSC_HP), a Phase-Locked Loop (PLL) module including an internal oscillator (OSC_PLL) and a Clock Control Unit (CCU). The CGU can convert a low-frequency input/external clock signal to a high-frequency internal clock.

The system clock f_{SYS} is generated out of the following selectable clocks:

- PLL clock output f_{PLL}
- Direct clock from oscillator OSC_HP f_{OSC}
- Direct output of internal Oscillator f_{INTOSC}
- Low precision clock f_{LP_CLK} (HW-enabled for startup after reset and during power-down wake-up sequence)

The following sections describe the different parts of the CGU.

6.3.1 Low Precision Clock

The clock source LP_CLK is a low-precision RC oscillator (LP-OSC, see f_{LP_CLK}) that is enabled by hardware as an independent clock source for the TLE9842QX startup after reset and during the power-down wake-up sequence. There is no user configuration possible on f_{LP_CLK}.

6.3.2 High Precision Oscillator Circuit (OSC_HP)

The high precision oscillator circuit, designed to work with both an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as input, and XTAL2 as output.

Figure 11 shows the recommended external circuitries for both operating modes, External Crystal Mode and External Input Clock Mode.

6.3.2.1 External Input Clock Mode

When supplying the clock signal directly, not using an external crystal and bypassing the oscillator, the input frequency needs to be within the range of 4 MHz to 24 MHz if the PLL VCO part is used.

When using an external clock signal it must be connected to XTAL1. XTAL2 is left open (unconnected).

6.3.2.2 External Crystal Mode

When using an external crystal, its frequency can be within the range of 4 MHz to 6 MHz. An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It consists normally of the two load capacitances C1 and C2, for some crystals a series damping resistor might be necessary. The exact values and related operating range are dependent on the crystal and have to be determined and optimized together with the crystal vendor using the negative resistance method. As starting point for the evaluation, the following load cap values may be used:

Table 4 External CAP Capacitors

Fundamental Mode Crystal Frequency (approx., MHz)	Load Caps C_1, C_2 (pF)
4	33
5	22
6	18

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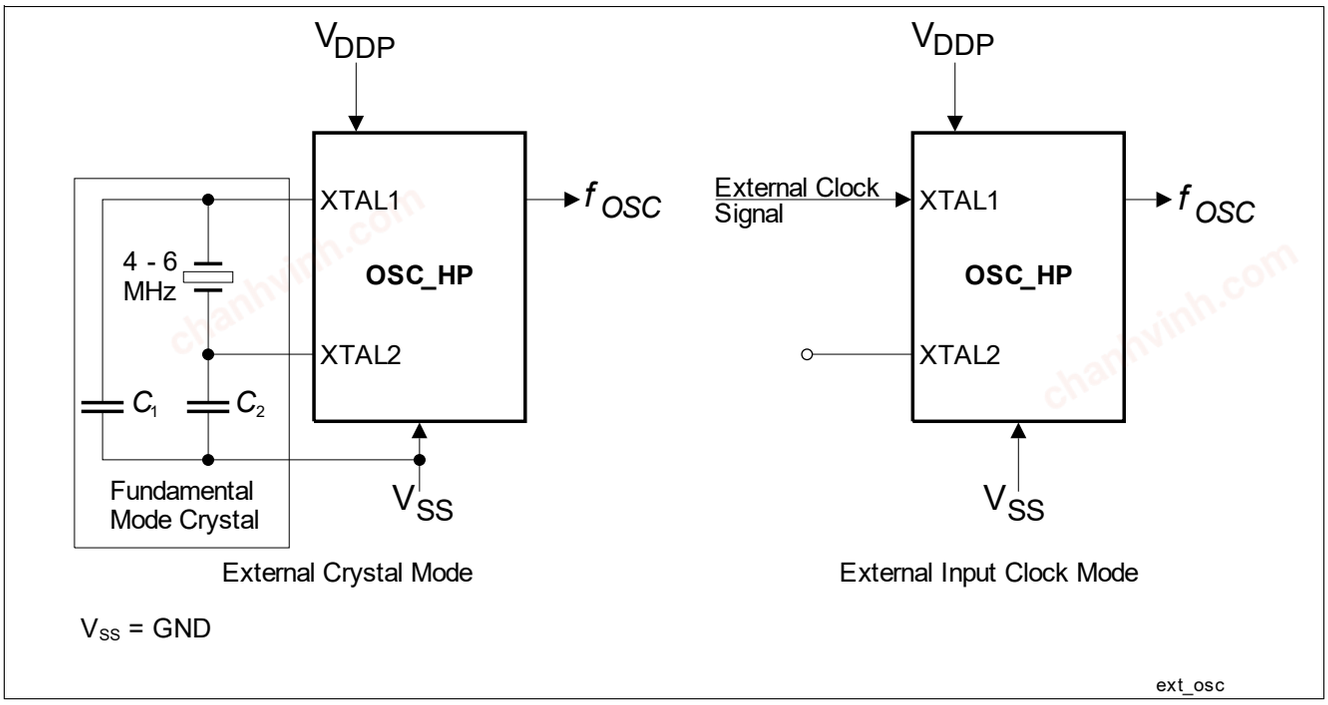


Figure 11 TLE9842QX External Circuitry for the OSC_HP

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6.3.3 Clock Control Unit

The Clock Control Unit (CCU) receives the clock from the PLL f_{PLL}, the external input clock f_{OSC}, the internal input clock f_{INTOSC}, or the low-precision input clock f_{LP_CLK}. The system frequency is derived from one of these clock sources.

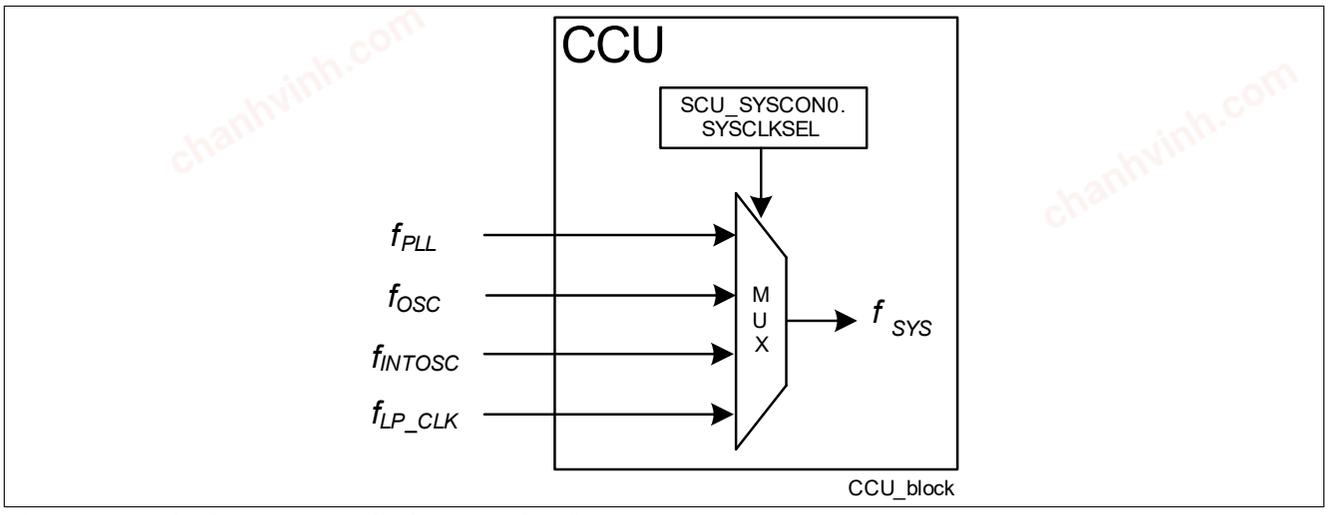


Figure 12 Clock Inputs to Clock Control Unit

The CCU generates all necessary clock signals within the microcontroller from the system clock. It consists of:

- Clock slow down circuitry
- Centralized enable/disable circuit for clock control

In normal running mode, the main module frequencies (synchronous unless otherwise stated) are as follows:

- System frequency, f_{SYS} = up to 25 MHz (measurement interface clock MI_CLK is derived from this clock)
- CPU clock (CCLK, SCLK) = up to 25 MHz (divide-down of NVM access clock)
- NVM access clock (NVMACCCLK) = up to 25 MHz
- Peripheral clock (PCLK, PCLK2, NVMCLK) = up to 25 MHz (equals CPU clock; must be same or higher)

Some peripherals are clocked by PCLK, others clocked by PCLK2 and the NVM is clocked by both NVMCLK and NVMACCCLK. During normal running mode, PCLK = PCLK2 = NVMCLK = CCLK. On wake-up from power-down mode, PCLK2 is restored similarly like NVMCLK, whereas PCLK is restored only after PLL is locked.

For optimized NVM access (read/write) with reduced wait state(s) and with respect to system requirements on CPU operational frequency, bit field NVMCLKFAC is provided for setting the frequency factor between the NVM access clock NVMACCCLK and the CPU clock CCLK.

For the slow down mode, the operating frequency is reduced using the slow down circuitry with clock divider setting at the bit field CLKREL. Bit field CLKREL is only effective when slow down mode is enabled via SFR bit PMCON0.SD bit. Note that the slow down setting of bit field CLKREL correspondingly reduces the NVMACCCLK clock. Slow down setting does not influence the erase and write cycles for the NVM.

Peripherals UART1, UART2, T2 and T21 and are not influenced by CLKREL and either not by NVMCLKFAC, to allow functional LIN communication in slow down mode.

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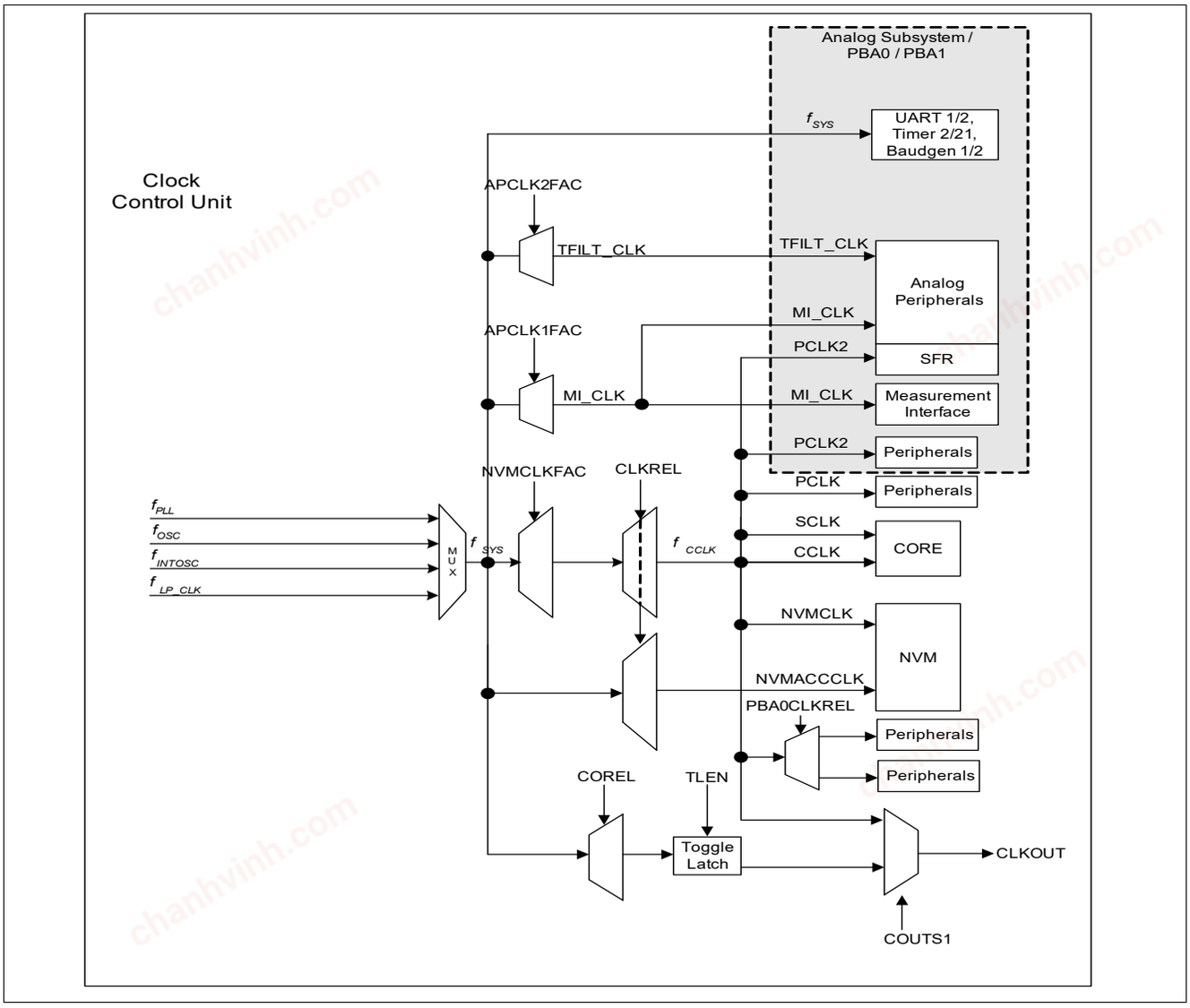


Figure 13 Clock Generation from f_{sys}; CLKOUT Generation

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7 System Control Unit - Power Modules (SCU-PM)

7.1 Description of the Power Modules System Control Unit

The System Control Unit of the power modules consists of the following sub-modules:

- Clock Watchdog Unit (CWU): supervision of all power modules relevant clocks with NMI signalling.
- Interrupt Control Unit (ICU): all system relevant interrupt flags and status flags.
- Power Control Unit (PCU): takes over control when device enters and exits Sleep and Stop Mode.
- External Watchdog (WDT1): independent system watchdog to monitor system activity

7.2 Introduction

7.2.1 Block Diagram

The System Control Unit of the power modules consists of the sub-modules in the figure shown below:

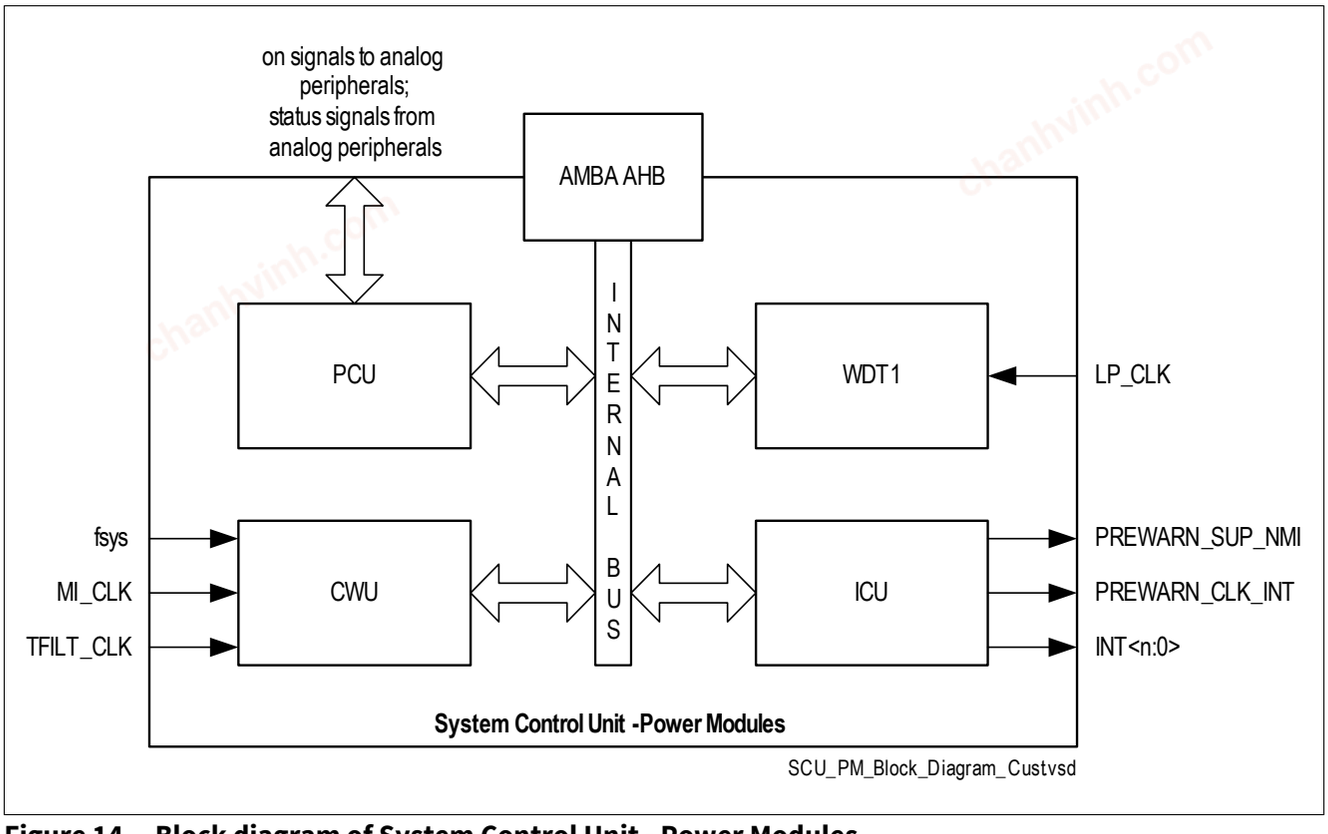


Figure 14 Block diagram of System Control Unit - Power Modules

IO description of SCU_PM:

CWU (Clock Watchdog Unit)

- check of f_{sys} = system frequency: output of PLL
- check of MI_CLK = measurement interface clock (analog clock): derived out of f_{sys} by division factors 1/2/3/4

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- check of TFILT_CLK = clock used for digital filters: derived out of f_{sys} by configurable division factors

ICU (Interrupt Control Unit)

- PREWARN_SUP_NMI = generation of Prewarn-Supply NMI
- PREWARN_CLK_INT = generation of Prewarn-Clock Watchdog NMI
- INT = generation of MISC interrupts

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8 Arm® Cortex®-M0 Core

8.1 Features

The key features of the Cortex®-M0 implemented are listed below.

Processor Core. A low gate count core, with low latency interrupt processing:

- Thumb® + Thumb-2® Instruction Set
- Banked stack pointer (SP) only
- Handler and thread modes
- Thumb and debug states
- Interruptible-continued instructions LDM/STM, Push/Pop for low interrupt latency
- Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
- Arm® architecture v6-M Style
- ARM®v6 unaligned accesses
- Systick (typ. 1ms)

Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing:

- External interrupts, configurable from 1 to 24
- 7 interrupt priority registers for levels from 0 up to 192 in steps of 64
- Dynamic repriorization of interrupts
- Priority grouping. This enables selection of pre-empting interrupt levels and non pre-empting interrupt levels
- Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

Bus interfaces

- Advanced High-performance Bus-Lite (AHB-Lite) interfaces

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8.2 Introduction

The Arm® Cortex®-M0 processor is a leading 32-bit processor and provides a high-performance and cost-optimized platform for a broad range of applications including microcontrollers, automotive body systems and industrial control systems. Like the other Cortex®-family processors, the Cortex®-M0 processor implements the Thumb®-2 instruction set architecture. With the optimized feature set the Cortex®-M0 delivers 32-bit performance in an application space that is usually associated with 8- and 16-bit microcontrollers.

8.2.1 Block Diagram

Figure 15 shows the functional blocks of the Cortex®-M0.

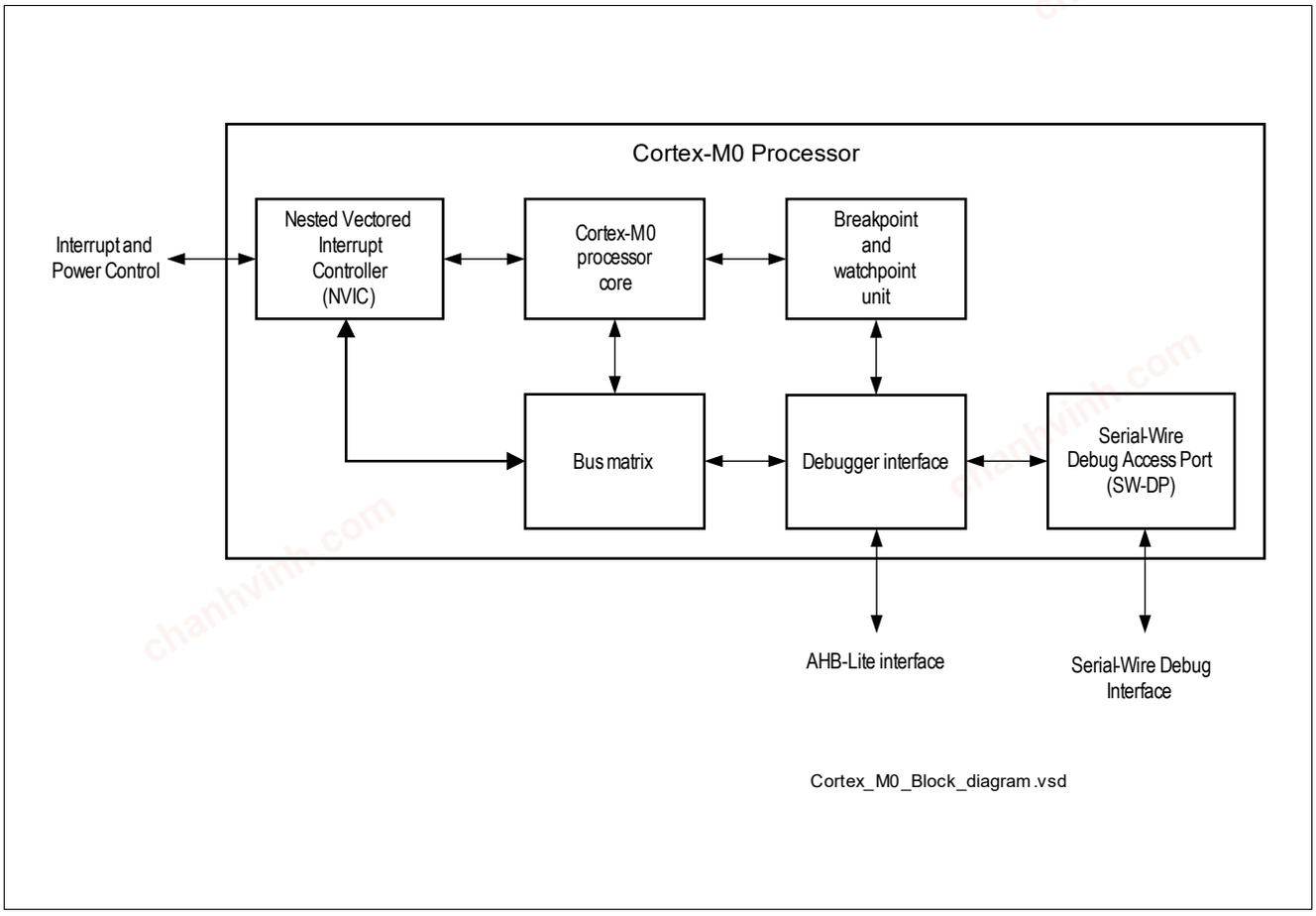


Figure 15 Cortex®-M0 Block Diagram

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9 Address Space Organization

The embedded Cortex®-M0 MCU offers the following address space organization:

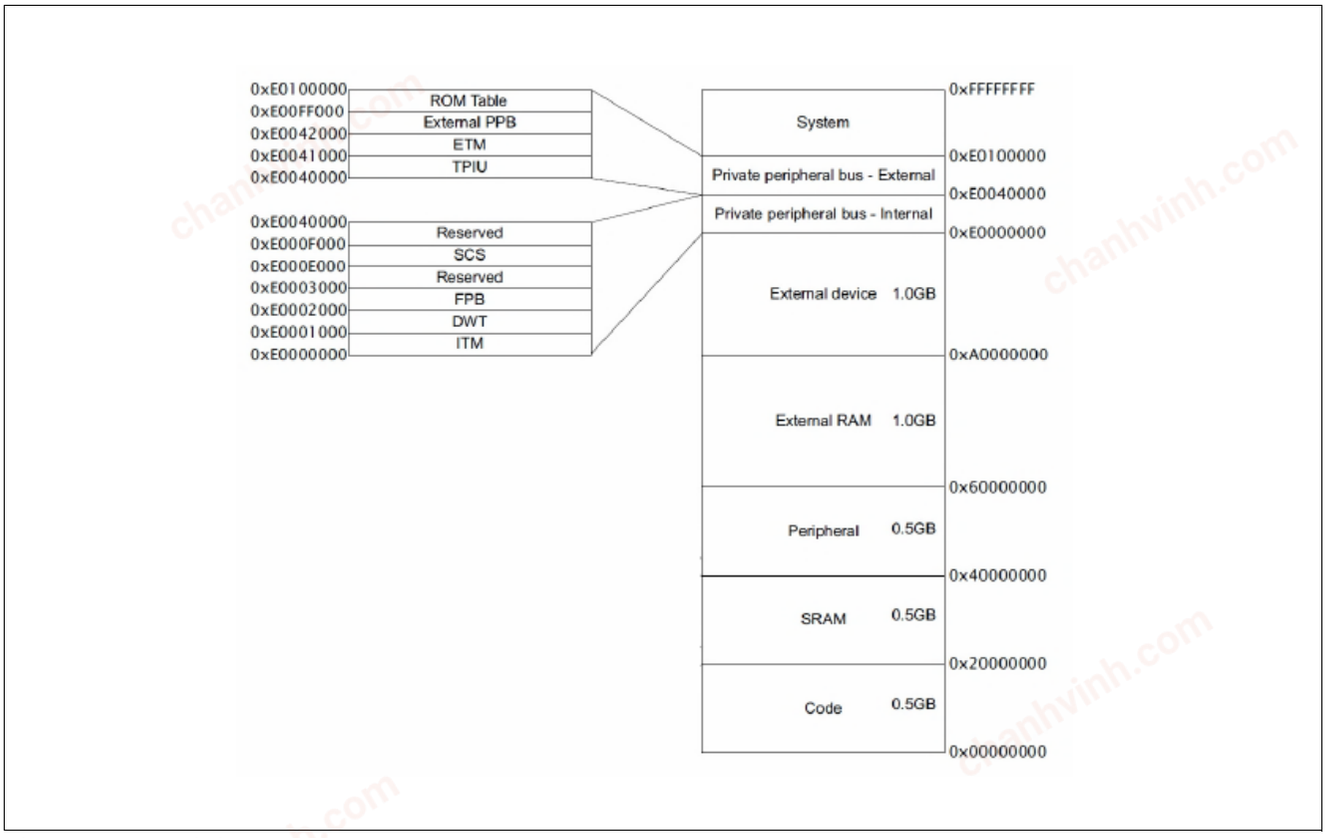


Figure 16 Original Cortex®-M0 Memory Map

The TLE9842QX manipulates operands in the following memory spaces:

- 36 KByte of Flash memory in code space
- 24 KB Boot ROM memory in code space (used for boot code and IP storage)
- 2 KB RAM memory in code space and data space (RAM can be read/written as program memory or external data memory)
- Special function registers (SFRs) in peripheral linear address space, up to 0.5 GBytes

The figure below shows the detailed address alignment of TLE9842QX:

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Address Space Organization

The on-chip memory modules available in the TLE9842QX are:

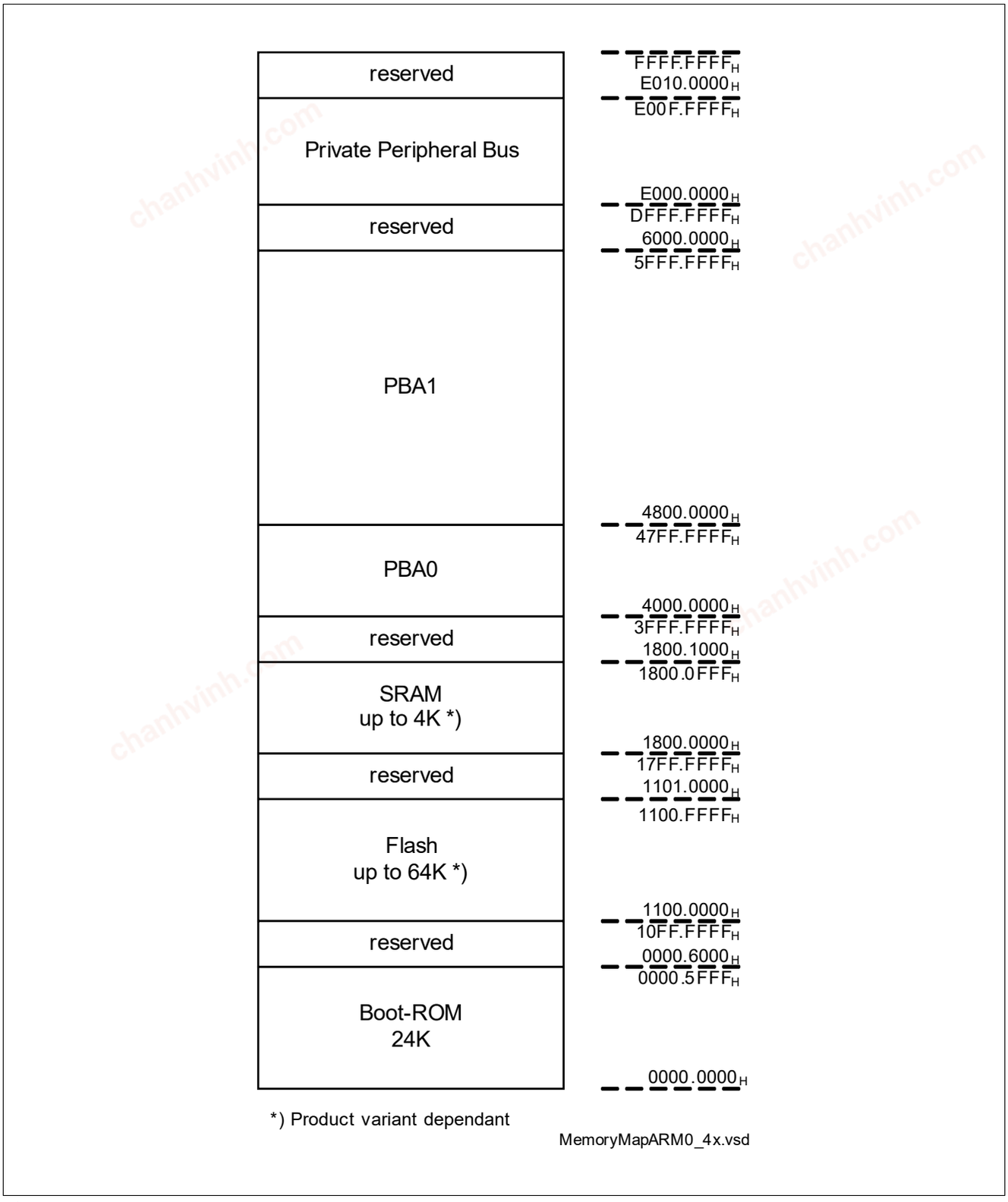


Figure 17 TLE9842QX Memory Map

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10 Memory Control Unit

10.1 Features

- Provides Memory access to ROM, RAM, NVM, Config Sector through AHB-Lite Interface
- MBIST for RAM
- MBIST for ROM
- NVM Configuration with Special Function Registers through AHB-Lite Interface
- Hardware Memory Protection Logic

10.2 Introduction

10.2.1 Block Diagram

The Memory Control Unit is divided in the following sub-modules:

- NVM Memory module (embedded Flash Memory)
- RAM memory module
- BootROM memory module
- Memory protection Unit (MPU) module

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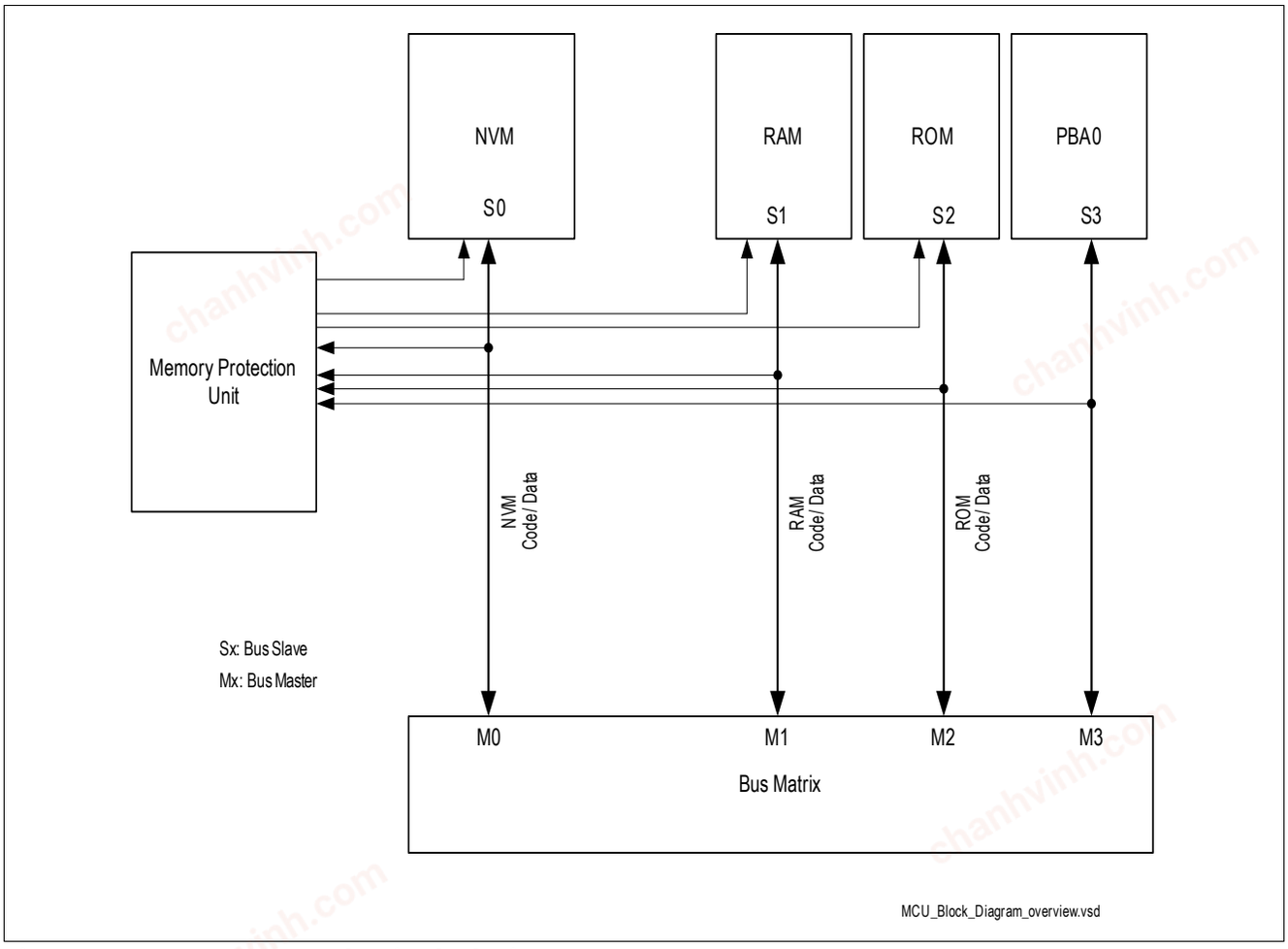


Figure 18 Memory Control Unit Block View

Functional Features for RAM

- 2 KB RAM
- Error correction code (ECC) for detection of single bit and double bit errors and dynamic correction of single bit errors
- Single byte access

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11 NVM Module (Flash Memory)

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data.

Features

- In-System Programming via LIN (Flash mode) and SWD
- Error Correction Code (ECC) for detection of single Bit and double Bit errors and dynamic correction of single Bit errors on Data Block (Double words, 64 bits).
- Interrupt and signaling of double bit error by NMI, address of double bit error readable by FW API user routine.
- Possibility of checking single bit error occurrence by ROM routines
- Program width of 128 Byte (page)
- Minimum erase width of 128 Byte (page)
- Integrated hardware support for EEPROM emulation
- 8 Byte read access
- Physical read access time: typ. 75 ns
- Code read access acceleration integrated; read buffer
- Page program time: typ. 3 ms
- Programming time for 64KB via Debug Interface: < 1800 ms (typ.)
- Page erase (128 bytes) and sector erase (4K bytes) time: typ. 4ms
- 3 separate keys for data area, program area and BSL area
- Password protection for three configurable program flash areas, three separate keys for data, program and BSL
- Security option to protect read out via debug interface in application run mode. NVM protection mode available, which can be enabled/disabled with password
- Write/erase access to 100TP (e.g. option bytes) is possible via the debug interface

Note: The user has to ensure that no flash operations which change the content of the flash get interrupted at any time.

The clock for the NVM is supplied with the system frequency f_{sys}. Integrated firmware routines are provided to ease NVM, and other operations including EEPROM emulation.

The TLE9842QX NVM module provides physical implementation of the memory module as well as needed complementary features and interface towards the core.

The module provides proper access to the memory through 2 AHB-Lite interfaces: a 8-bit data interface for NVM internal register access and a 32-bit data interface for code/data access both multiplexed on Cortex®-M0 system bus.

The TLE9842QX NVM module consists of the memory cell array and all the control circuits and registers needed to access the array itself. The 64 Kbyte data module is mapped in the Cortex®-M0 code address range 11000000H - 1100FFFFH while the dedicated SFRs are mapped in the Cortex®-M0 system address range 58004000H - 58007FFFH.

Access of NVM module is granted through the AMBA matrix block that forwards to the memory modules AHB-Lite interfaces the requests generated by the masters according to the defined priority policy.

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11.1 Definitions

This section defines the nomenclature and some abbreviations. The used flash memory is a non-volatile memory (“NVM”) based on a floating gate one-transistor cell. It is called “non-volatile” because the memory content is kept when the memory power supply is shut off.

11.1.1 General Definitions

Logical and Physical States

Erasing

The erased state of a cell is ´1´. Forcing an NVM cell to this state is called erasing. Erasing is possible with a granularity of a page (see below).

Writing

The written state of a cell is ´0´. Forcing an NVM cell to this state is called writing. Each bit can be individually written.

Programming

The combination of erasing and writing is called ‘programming’. Programming often means also writing a previously erased page.

The wording ‘write’ or ‘writing’ are also used for accessing special function registers and the assembly buffer. The meaning depends therefore on the context.

The above listed processes have certain limitations:

Retention: This is the time during which the data of a flash cell can be read reliably. The retention time is a statistical figure that depends on the operating conditions of the flash array (temperature profile) and the accesses to the flash array. With an increasing number of program/erase cycles (see endurance) the retention is lowered. Drain and gate disturbs decrease data retention as well.

Endurance: As described above, the data retention is reduced with an increasing number of program/erase cycles. A flash cell incurs one cycle whenever its page or sector is erased. This number is called “endurance”. As said for the retention, it is a statistical figure that depend on operating conditions and the use of the flash cells and on the required quality level.

Drain Disturb: Because of using a so called “one-transistor” flash cell each program access disturbs all pages of the same sector slightly. Over long these “drain disturbs” make 0 and 1 values indistinguishable and thus provoke read errors. This effect is again interrelated with the retention. A cell that incurred a high number of drain disturbs will have a lower retention. The physical sectors of the flash array are isolated from each other. So pages of a different sector do not incur a drain disturb. this effect must be therefore considered when the page erase feature is used or when re-programming an ready programmed page (implicitly causing an erase of the page before writing the new data).

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Data Portions

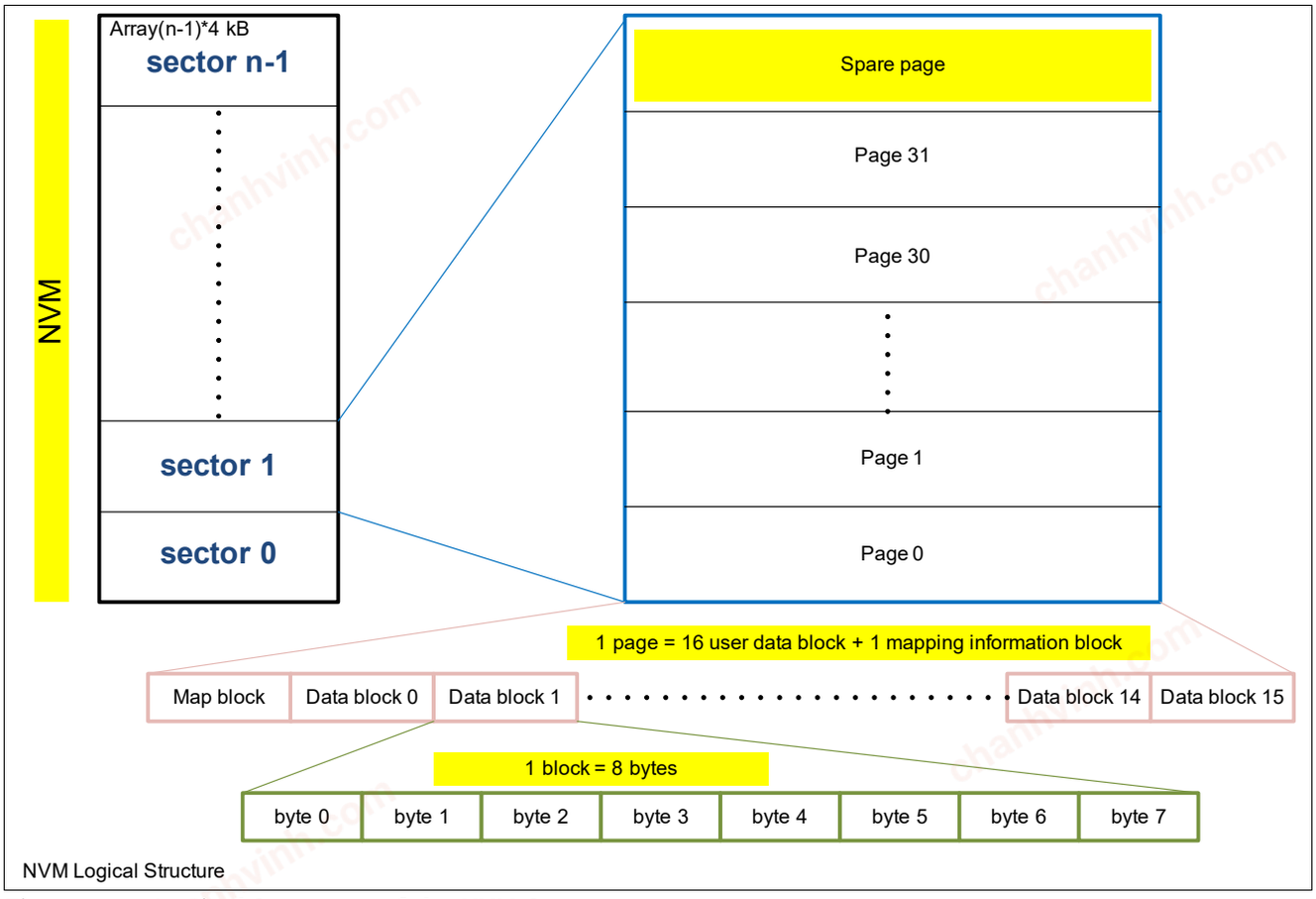


Figure 19 Logical Structure of the NVM Core

Doubleword

A doubleword consists of 64 bits. A doubleword represents the data size that is read from or written to the NVM core module within one access cycle.

Block

A block consists of one doubleword and its associated ECC data (64 bit data and 8 bit ECC). A block represents the smallest data portion that can be changed in the assembly buffer. Since the ECC protects 64 bits, when a byte is written to the assembly buffer automatically an NVM internal read of the complete block is triggered, the byte and the ECC are updated and the complete block is written back to the assembly buffer.

Mapblock

A map block consists of a module specific number of ECC -protected bits that hold the necessary information to map a physical page to a logical page.

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Page

A page consists of 16 blocks and one map block.

Spare Page

A spare page is an additional page in a sector used in each programming routine to allow tearing-safe programming.

Sector

A sector consists of 32 logical and 33 physical pages.

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12 Interrupt System

12.1 Features

- Up to 24 interrupt nodes for on-chip peripherals
- Up to 8 NMI nodes for critical system events
- Maximum flexibility for all 24 interrupt nodes

12.2 Introduction

12.2.1 Overview

The TLE9842QX supports 24 interrupt vectors with 4 priority levels. 22 of these interrupt vectors are assigned to the on-chip peripherals: GPT12, SSC1, SSC2, CCU6, Low-Side Switch, High-Side Switch and A/D Converter are each assigned to one dedicated interrupt vector; while UART1 and Timer2 or UART2, External Interrupt 2 and Timer21 share interrupt vectors. Two vectors are dedicated for External Interrupt 0 and 1.

Table 5 Interrupt Vector Table

Service Request	Node ID	Description
GPT1	0	GPT1 Interrupt
GPT2	1	GPT2 Interrupt
MU	2	MU interrupt / ADC2, VBG interrupt
ADC1	3	ADC10 Bit interrupt
CCU0	4	CCU6 node 0 interrupt
CCU1	5	CCU6 node 1 interrupt
CCU2	6	CCU6 node 2 interrupt
CCU3	7	CCU6 node 3 interrupt
SSC1	8	SSC1 interrupt (receive, transmit, error)
SSC2	9	SSC2 interrupt (receive, transmit, error)
UART1	10	UART1 (ASC-LIN) interrupt (receive, transmit), t2, linsync1, LIN
UART2	11	UART2 interrupt (receive, transmit), t21, External interrupt (EINT2)
EXINT0	12	External interrupt (EINT0)
EXINT1	13	External interrupt (EINT1)
WAKEUP	14	Wakeup interupt (generated by a wakeup event)
rfu	15	Reserved for future use
rfu	16	Reserved for future use
LS1	17	Low Side 1 Interrupt
LS2	18	Low Side 2 Interrupt
HS1	19	High Side 1 Interrupt
rfu	20	Reserved for future use

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Table 5 Interrupt Vector Table (cont'd)

Service Request	Node ID	Description
rfu	21	Reserved for future use
MONx	22	MONx Interrupt
Port 2.x	23	Port 2.x - DPP1

Table 6 NMI Interrupt Table

Service Request	Node	Description
PLL NMI	NMI	PLL Loss-of-Lock
NVM Operation Complete NMI	NMI	NVM Operation Complete
Overtemperature NMI	NMI	System Overtemperature
Oscillator Watchdog NMI	NMI	Oscillator Watchdog and MI_CLK Watchdog Timer Overflow
NVM Map Error NMI	NMI	NVM Map Error
ECC Error NMI	NMI	RAM / NVM Uncorrectable ECC Error
Supply Prewarning NMI	NMI	Supply Prewarning

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13 Watchdog Timer (WDT1)

13.1 Features

In Active Mode, the WDT1 acts as a windowed watchdog timer, which provides a highly reliable and safe way to recover from software or hardware failures.

The WDT1 is always enabled in Active Mode. In Sleep Mode, Stop Mode and Debug Mode the WDT1 is disabled.

Functional Features

- Watchdog Timer is operating with a from the system clock (f_{SYS}) independent clock source (f_{LP_CLK})
- Windowed Watchdog Timer with programmable timing (16, 32, 48, …, 1008ms period) in Active Mode
- Long open window (200 ms) after power-up, reset, wake-up
- Short open window (30 ms) to facilitate Flash programming
- System safety shutdown to Sleep Mode after 5 missed WDT1 services
- Watchdog is disabled in Debug Mode
- Watchdog cannot be deactivated in Normal Mode
- Watchdog reset is stored in reset status register

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13.2 Introduction

The behavior of the Watchdog Timer in Active Mode is depicted in **Figure 20**.

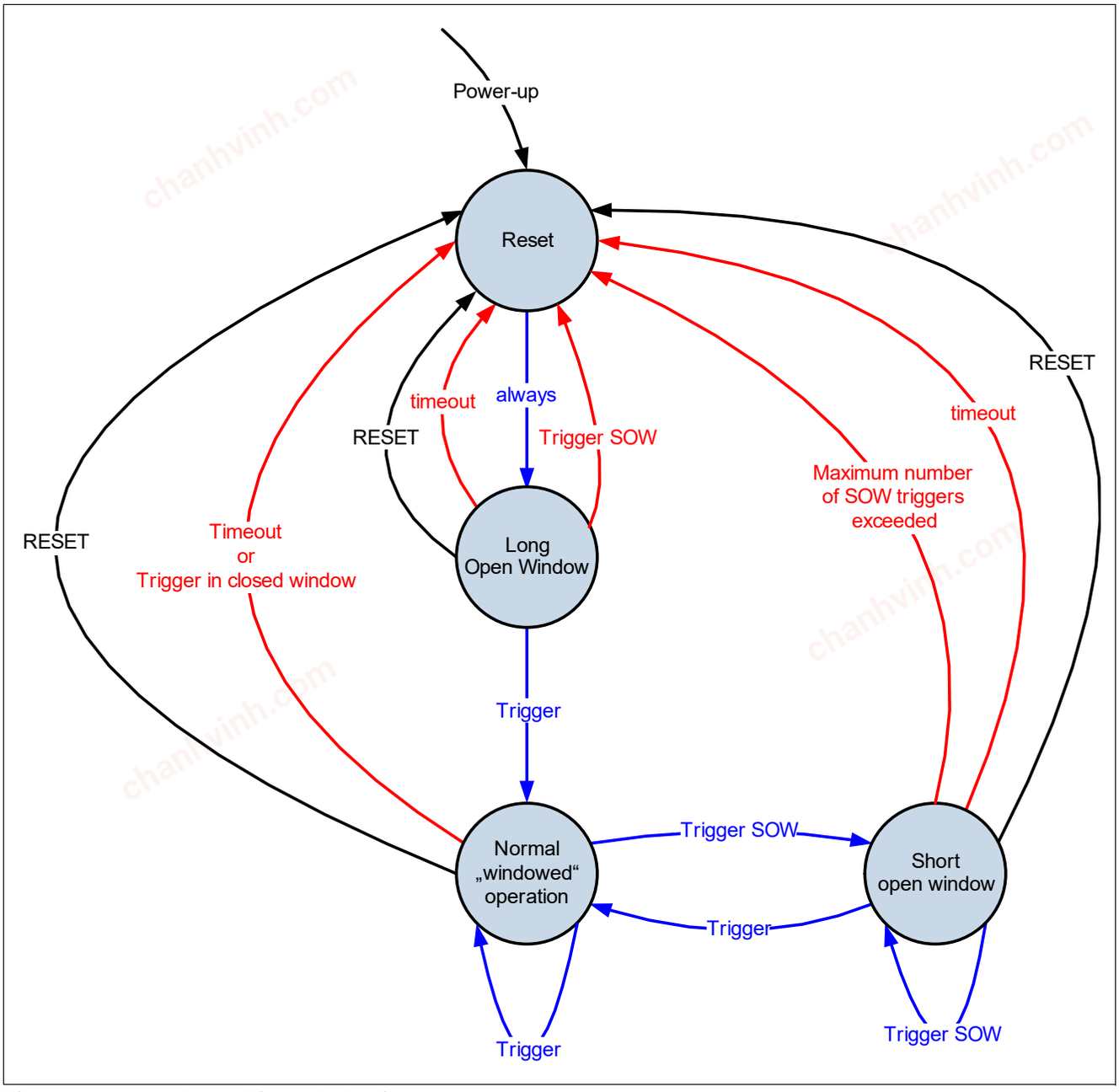


Figure 20 Watchdog Timer Behavior

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14 GPIO Ports and Peripheral I/O

The TLE9842QX has 18 port pins organized into three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. On Port 2 (P2) analog inputs are shared with general purpose input.

14.1 Features

- 10 GPIOs (P0.x & P1.x), 6 analog inputs (P2.x) and two additional analog inputs shared with a XTAL feature (P2.4, P2.5).
- Strong pull-up at Reset-pin and Hall-inputs (except P2.x)

Bidirectional Port Features (P0, P1)

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Analog Port Features (P2)

- Configurable pull-up/pull-down devices
- Transfer of data through digital inputs
- Alternate inputs for on-chip peripherals

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14.2 Introduction

14.2.1 Port 0 and Port 1

Figure 21 shows the block diagram of an TLE9842QX bidirectional port pin. Each port pin is equipped with a number of control and data bits, thus enabling very flexible usage of the pin.

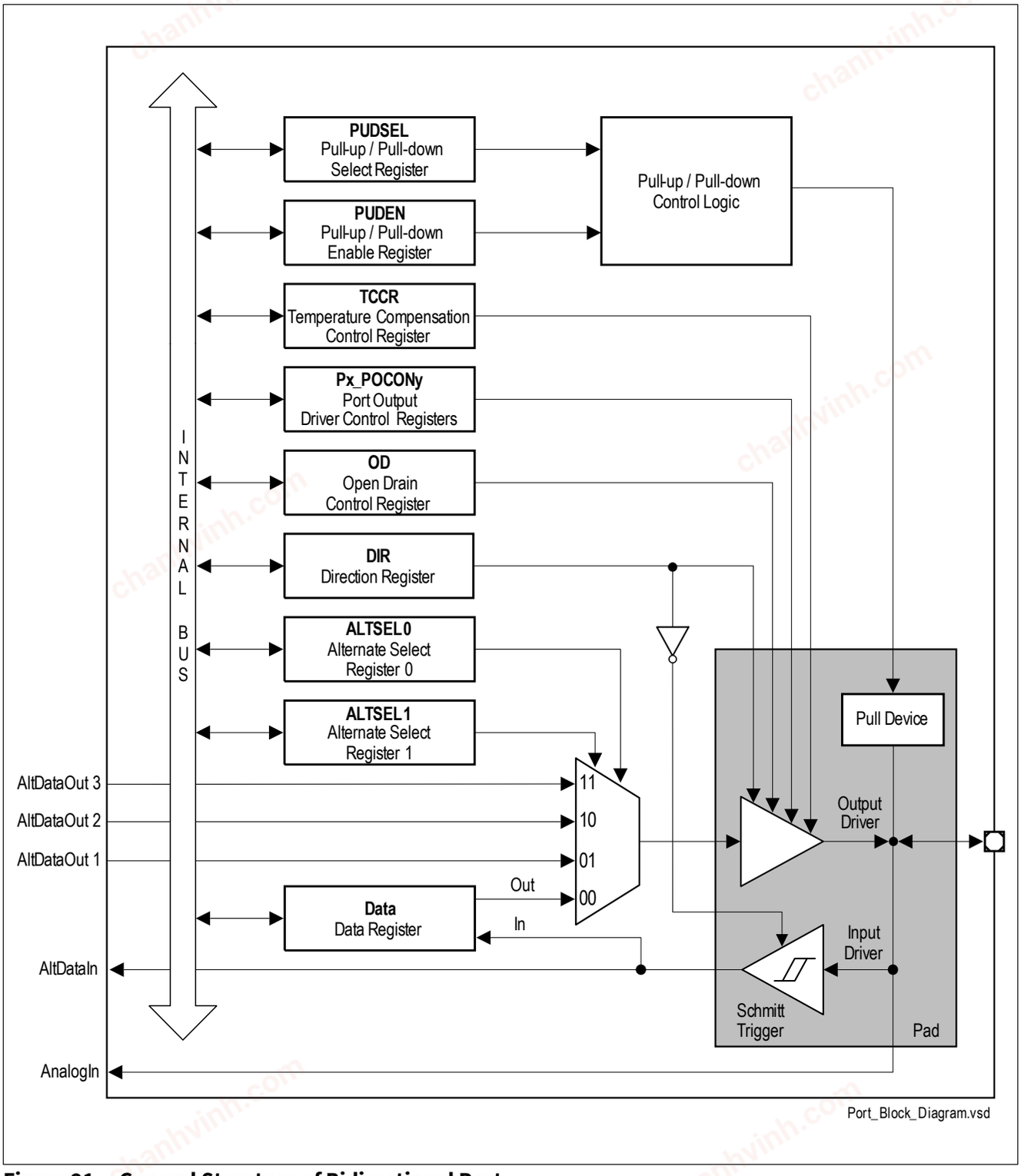


Figure 21 General Structure of Bidirectional Port

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14.2.2 Port 2

Figure 22 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt-Trigger device and can be read via the register P2_DATA. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register P2_PUDSEL selects whether a pull-up or the pull-down device is activated while register P2_PUDEN enables or disables the pull device. The analog input (AnalogIn) bypasses the digital circuitry and Schmitt-Trigger device for direct feed-through to the ADC input channel.

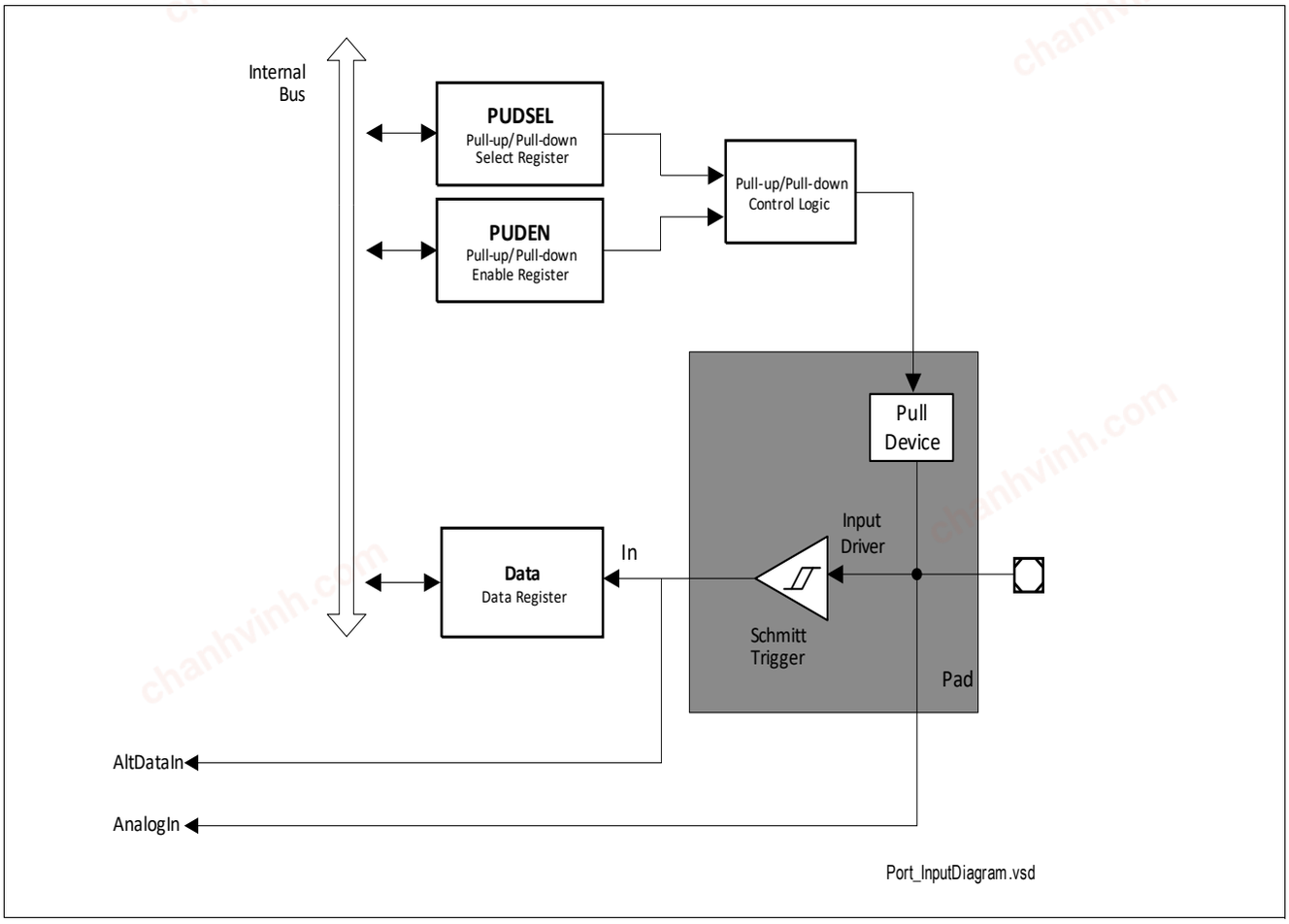


Figure 22 General Structure of Input Port

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14.3 TLE9842QX Port Implementation Details

14.3.1 Port 0

14.3.1.1 Port 0 Functions

Port 0 alternate function mapping according **Table 7**

Table 7 Port 0 Input/Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.0	Input	GPI	P0_DATA.P0	
		INP1	T12HR_0	CCU6
		INP2	T4INA	GPT12
		INP3	T2_0	Timer 2
		INP4	SWD_CLK	SWD
		INP5	EXINT2_3	SCU
	Output	GPO	P0_DATA.P0	
		ALT1	T3OUT_0	GPT12
		ALT2	EXF21_0	Timer 21
		ALT3	UART2_RXDO	UART2
P0.1	Input	GPI	P0_DATA.P1	
		INP1	T13HR_0	CCU6
		INP2	UART1_RXD	UART1
		INP3	T2EX_1	Timer 2
		INP4	T21_0	Timer 21
		INP5	EXINT0_3	SCU
		INP6	T4INC	GPT12
		INP7	CAPINA	GPT12
		INP8	SSC12_S_SCK	SSC1/2
		INP9	CC62_0	CCU6
	Output	GPO	P0_DATA.P1	
		ALT1	T6OUT_0	GPT12
		ALT2	CC62_0	CCU6
		ALT3	SSC12_M_SCK	SSC1/2

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Table 7 Port 0 Input/Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.2	Input	GPI	P0_DATA.P2	
		INP1	T2EUDA	GPT12
		INP2	CTRAP_0	CCU6
		INP3	SSC12_M_MRST	SSC1/2
		INP4	T21EX_0	Timer 21
		INP5	EXINT1_3	SCU
	Output	GPO	P0_DATA.P2	
		ALT1	SSC12_S_MRST	SSC1/2
		ALT2	UART1_TXD	UART1
		ALT3	EXF2_0	Timer 2
P0.3	Input	GPI	P0_DATA.P3	
		INP1	SSC1_S_SCK	SSC1
		INP2	T4EUDA	GPT12
		INP3	CAPINB	GPT12
		INP4	EXINT1_2	SCU
		INP5	T3EUDD	GPT12
		INP6	CCPOS0_1	CCU6
	Output	GPO	P0_DATA.P3	
		ALT1	SSC1_M_SCK	SSC1
		ALT2	T6OFL	GPT12
		ALT3	T6OUT_1	GPT12
P0.4	Input	GPI	P0_DATA.P4	
		INP1	SSC1_S_MTSR	SSC1
		INP2	CC60_0	CCU6
		INP3	T21_2	Timer 21
		INP4	EXINT2_2	SCU
		INP5	T3EUDA	GPT12
		INP6	CCPOS1_1	CCU6
	Output	GPO	P0_DATA.P4	
		ALT1	SSC1_M_MTSR	SSC1
		ALT2	CC60_0	CCU6
		ALT3	CLKOUT_0	SCU

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Table 7 Port 0 Input/Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.5	Input	GPI	P0_DATA.P5	
		INP1	SSC1_M_MRST	SSC1
		INP2	EXINT0_0	SCU
		INP3	T21EX_2	Timer 21
		INP4	T5INA	GPT12
		INP5	CCPOS2_1	CCU6
	Output	GPO	P0_DATA.P5	
		ALT1	SSC1_S_MRST	SSC1
		ALT2	COUT60_0	CCU6
		ALT3	LIN_RXD	LIN

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14.3.2 Port 1

14.3.2.1 Port 1 Functions

Port 1alternate function mapping according **Table 8**

Table 8 Port 1 Input / Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.0	Input	GPI	P1_DATA.P0	
		INP1	T3INC	GPT12
		INP2	CC61_0	CCU6
		INP3	SSC2_S_SCK	SSC2
		INP4	T4EUDB	GPT12
	Output	GPO	P1_DATA.P0	
		ALT1	SSC2_M_SCK	SSC2
		ALT2	CC61_0	CCU6
		ALT3	UART2_TXD	UART2
P1.1	Input	GPI	P1_DATA.P1	
		INP1	T6EUDA	GPT12
		INP2	T5INB	GPT12
		INP3	T3EUDC	GPT12
		INP4	SSC2_S_MTSR	SSC2
		INP5	T21EX_3	Timer 21
		INP6	UART2_RXD	UART2
	Output	GPO	P1_DATA.P1	
		ALT1	SSC2_M_MTSR	SSC2
		ALT2	COUT61_0	CCU6
		ALT3	EXF21_1	Timer 21
P1.2	Input	GPI	P1_DATA.P2	
		INP1	EXINT0_1	SCU
		INP2	T21_1	Timer 21
		INP3	T2INA	GPT12
		INP4	SSC2_M_MRST	SSC2
		INP5	CCPOS2_2	CCU6
	Output	GPO	P1_DATA.P2	
		ALT1	SSC2_S_MRST	SSC2
		ALT2	COUT63_0	CCU6
		ALT3	T3OUT_1	GPT12

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Table 8 Port 1 Input / Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.4	Input	GPI	P1_DATA.P4	
		INP1	EXINT2_1	SCU
		INP2	T21EX_1	Timer 21
		INP3	T2INB	GPT12
		INP4	T5EUDA	GPT12
		INP5	SSC12_S_MTSR	SSC1/2
		INP6	CCPOS1_2	CCU6
	Output	GPO	P1_DATA.P4	
		ALT1	CLKOUT_1	SCU
		ALT2	COUT62_0	CCU6
		ALT3	SSC12_M_MTSR	SSC1/2

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14.3.3 Port 2

14.3.3.1 Port 2 Functions

Port 2 alternate function mapping according **Table 9**

Table 9 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.0	Input	GPI	P2_DATA.P0	
		INP1	EXINT1_1	SCU
		INP2	CCPOS0_2	CCU6
		INP3	T5EUDB	GPT12
		ANALOG	AN0	ADC
P2.1	Input	GPI	P2_DATA.P1	
		INP1	CCPOS0_0	CCU6
		INP2	EXINT1_0	SCU
		INP3	T12HR_1	CCU6
		INP4	CC61_1	CCU6
		ANALOG	AN1	ADC
P2.2	Input	GPI	P2_DATA.P2	
		INP1	T6EUDB	GPT12
		INP2	T2EX_0	Timer 2
		INP3	T12HR_2	CCU6
		ANALOG	AN2	ADC
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	EXINT0_2	SCU
		INP3	CTRAP_1	CCU6
		INP4	T3IND	GPT12
		INP5	CC60_1	CCU6
		ANALOG	AN3	ADC
P2.4	Input	GPI	P2_DATA.P4	
		INP1	T2EUDB	GPT12
		INP2	T2_2	Timer 2
		INP3	T2EX_2	Timer 2
		INP4	CCPOS0_3	CCU6
		INP5	CTRAP_2	CCU6
		IN	XTAL (in)[1)]	XTAL

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Table 9 Port 2 Input Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.5	Input / Output	GPI	P2_DATA.P5	
		INP1	T3EUDB	GPT12
		INP2	T4EUDC	GPT12
		INP3	T2_1	Timer 2
		INP4	LIN_TXD	LIN
		INP5	CCPOS1_3	CCU6
		OUT	XTAL (out)[1)]	XTAL
P2.6	Input	GPI	P2_DATA.P6	
		INP1	T4EUDD	GPT12
		INP2	T2EX_3	Timer 2
		INP3	CCPOS2_3	CCU6
		INP4	T13HR_2	CCU6
		ANALOG	AN6	ADC
P2.7	Input	GPI	P2_DATA.P7	
		INP1	CCPOS2_0	CCU6
		INP2	EXINT2_0	SCU
		INP3	T13HR_1	CCU6
		INP4	CC62_1	CCU6
		ANALOG	AN7	ADC

1) configurable by user

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15 General Purpose Timer Units (GPT12)

15.1 Features

15.1.1 Features Block GPT1

The following list summarizes the supported features:

- f_{GPT}/4 maximum resolution
- 3 independent timers/counters
- Timers/counters can be concatenated
- 4 operating modes:
  - Timer Mode
  - Gated Timer Mode
  - Counter Mode
  - Incremental Interface Mode
- Reload and Capture functionality
- Shared interrupt: Node 0

15.1.2 Features Block GPT2

The following list summarizes the supported features:

- f_{GPT}/2 maximum resolution
- 2 independent timers/counters
- Timers/counters can be concatenated
- 3 operating modes:
  - Timer Mode
  - Gated Timer Mode
  - Counter Mode
- Extended capture/reload functions via 16-bit capture/reload register CAPREL
- Shared interrupt: Node 1

15.2 Introduction

The General Purpose Timer Unit blocks GPT1 and GPT2 have very flexible multifunctional timer structures which may be used for timing, event counting, pulse width measurement, pulse generation, frequency multiplication, and other purposes.

They incorporate five 16-bit timers that are grouped into the two timer blocks GPT1 and GPT2. Each timer in each block may operate independently in a number of different modes such as Gated timer or Counter Mode, or may be concatenated with another timer of the same block.

Each block has alternate input/output functions and specific interrupts associated with it. Input signals can be selected from several sources by register PISEL.

The GPT module is clocked with clock f_{GPT}. f_{GPT} is a clock derived from f_{SYS}.

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15.2.1 Block Diagram GPT1

Block GPT1 contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{GPT}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer.

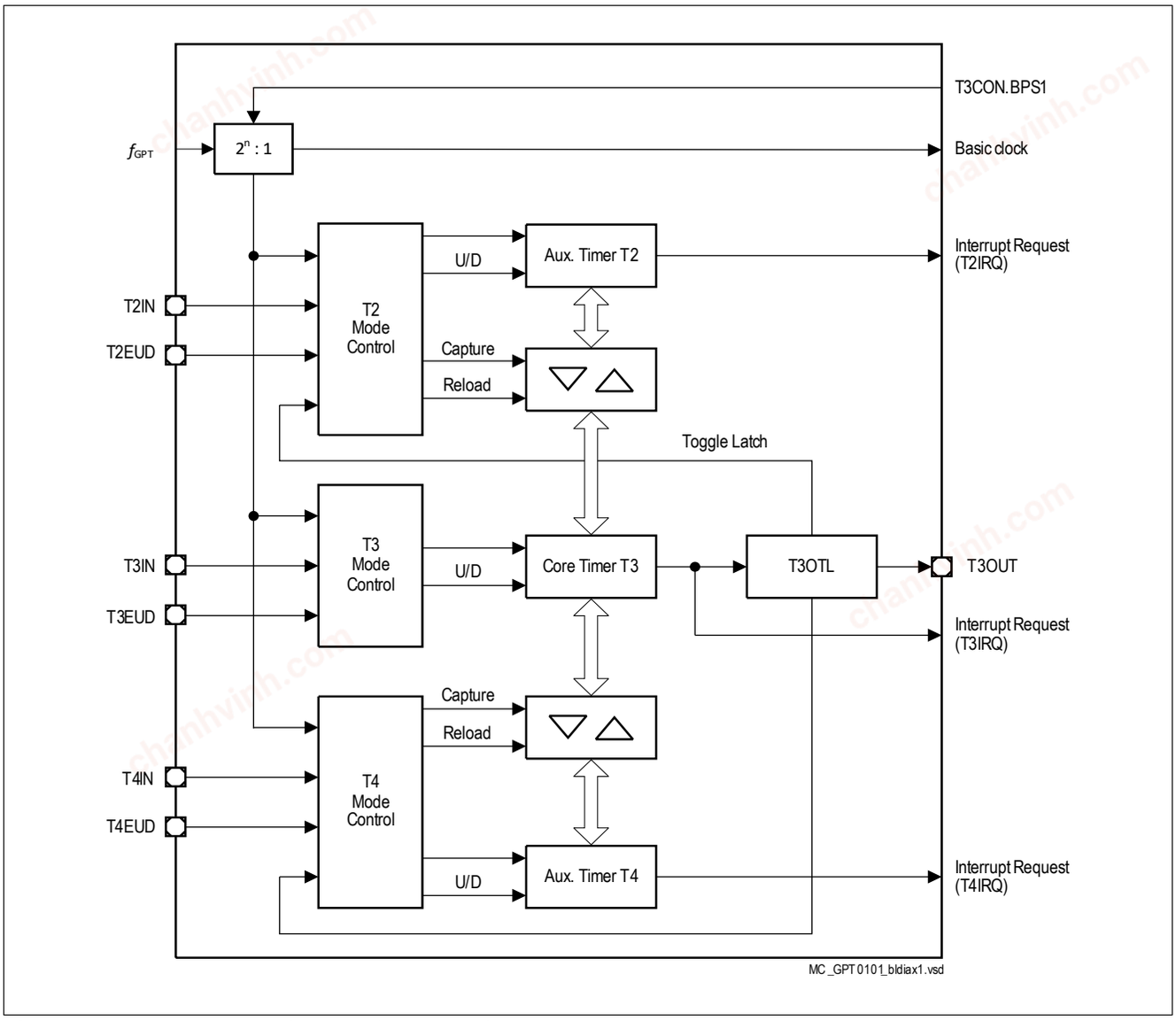


Figure 23 GPT1 Block Diagram (n = 2 … 5)

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15.2.2 Block Diagram GPT2

Block GPT2 contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{GPT}/2$. An additional Capture/Reload register (CAPREL) supports capture and reload operation with extended functionality.

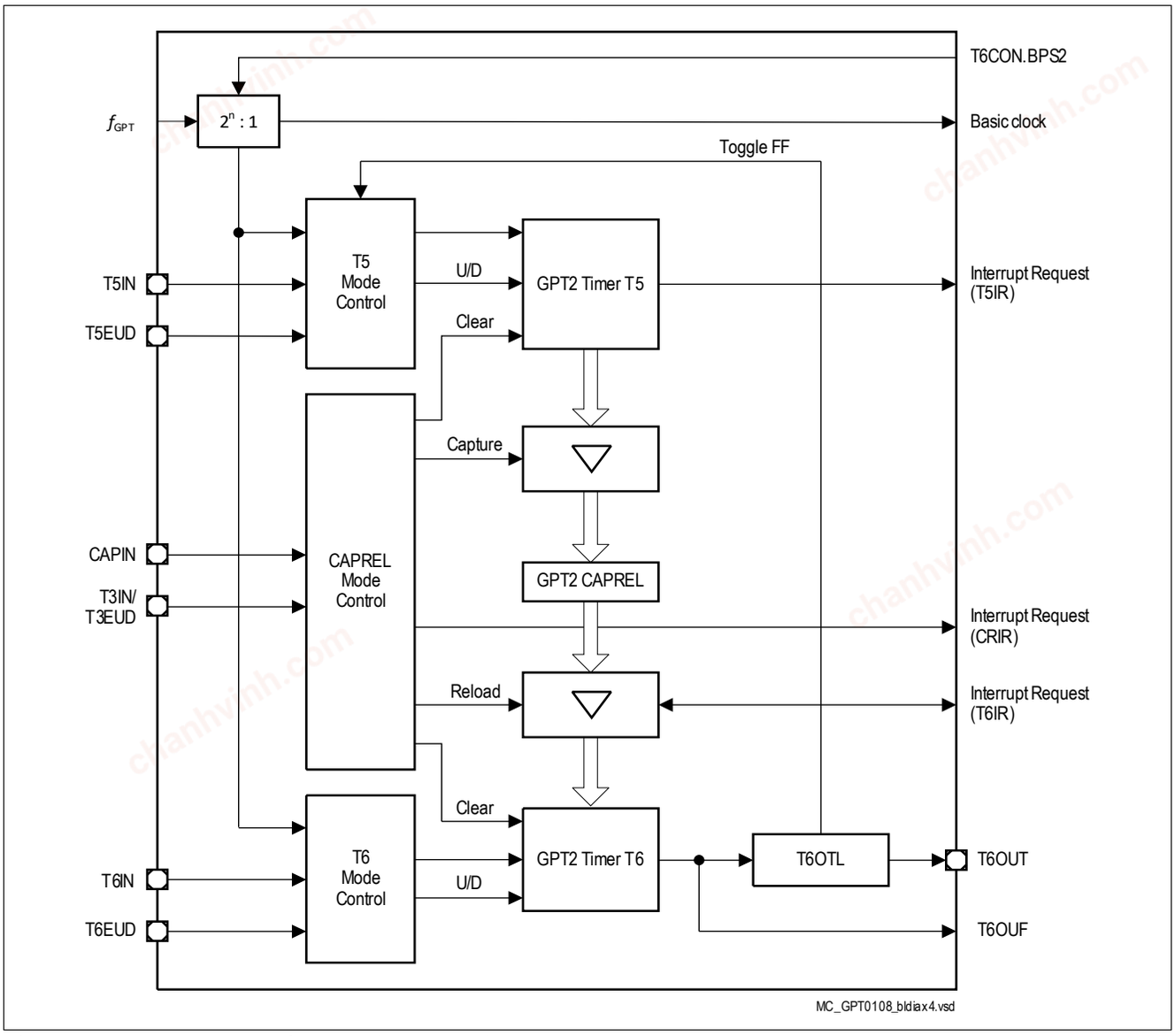


Figure 24 GPT2 Block Diagram (n = 1 ... 4)

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16 Timer2 and Timer21

16.1 Features

- 16-bit auto-reload mode
  - selectable up or down counting
- One channel 16-bit capture mode
- Baud-rate generator for U(S)ART

16.2 Introduction

Two functionally identical timers are implemented: Timer 2 and 21. The description refers to Timer 2 only, but applies to Timer 21 as well.

The timer modules are general purpose 16-bit timer. Timer 2 can function as a timer or counter in each of its modes. As a timer, it counts with an input clock of $f_{sys}/12$ (if prescaler is disabled). As a counter, Timer 2 counts 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is $f_{sys}/24$ (if prescaler is disabled).

16.2.1 Timer2 and Timer21 Modes Overview

Table 10 Timer2 and Timer21 Modes

Mode	Description
Auto-reload	**Up/Down Count Disabled** • Count up only • Start counting from 16-Bit reload value, overflow at $FFFF_H$ • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmable reload value in register RC2 • Interrupt is generated with reload events.

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Table 10 Timer2 and Timer21 Modes (cont'd)

Mode	Description
Auto-reload	**Up/Down Count Enabled** • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up – Start counting from 16-Bit reload value, overflow at $FFFF_H$ – Reload event triggered by overflow condition – Programmable reload value in register RC2 • Count down – Start counting from $FFFF_H$, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at $FFFF_H$
Channel capture	• Count up only • Start counting from 0000_H, overflow at $FFFF_H$ • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generate with reload or capture event

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17 Capture/Compare Unit 6 (CCU6)

17.1 Feature Set Overview

This section gives an overview over the different building blocks and their main features.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for High Side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Multiple interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

Additional Specific Functions

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

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17.2 Introduction

The CCU6 unit is made up of a Timer T12 Block with three capture/compare channels and a Timer T13 Block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive AC-motors or inverters.

A rich set of status bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide means for efficient software-control.

Note: The capture/compare module itself is named CCU6 (capture/compare unit 6). A capture/compare channel inside this module is named CC6x.

17.2.1 Block Diagram

The Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

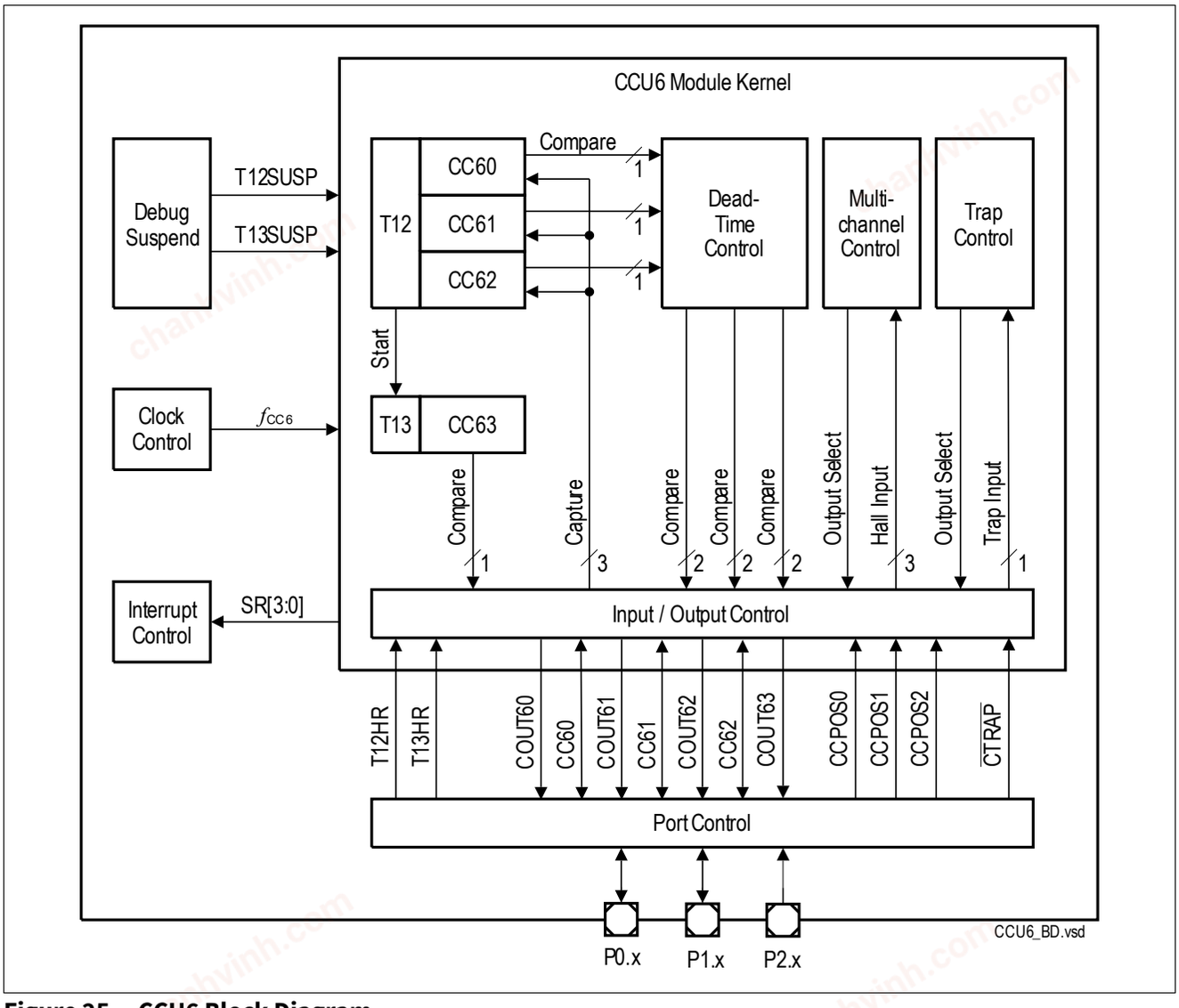


Figure 25 CCU6 Block Diagram

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18 UART1/UART2

18.1 Features

- Full-duplex asynchronous modes
  - 8-Bit or 9-Bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered (1 Byte)
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates, e.g. 9.6kBaud, 19.2kBaud, 115.2kBaud, 125kBaud, 250kBaud, 500kBaud
- Hardware logic for break and sync byte detection
- for UART1: LIN support: connected to timer channel for synchronization to LIN baud rate

In all modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in the modes by the incoming start bit if REN = 1.

The serial interface also provides interrupt requests when transmission or reception of the frames has been completed. The corresponding interrupt request flags are TI or RI, respectively. If the serial interrupt is not used (i.e., serial interrupt not enabled), TI and RI can also be used for polling the serial interface.

18.2 Introduction

The UART1/UART2 provide a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. They are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, the previous byte will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

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18.2.1 Block Diagram

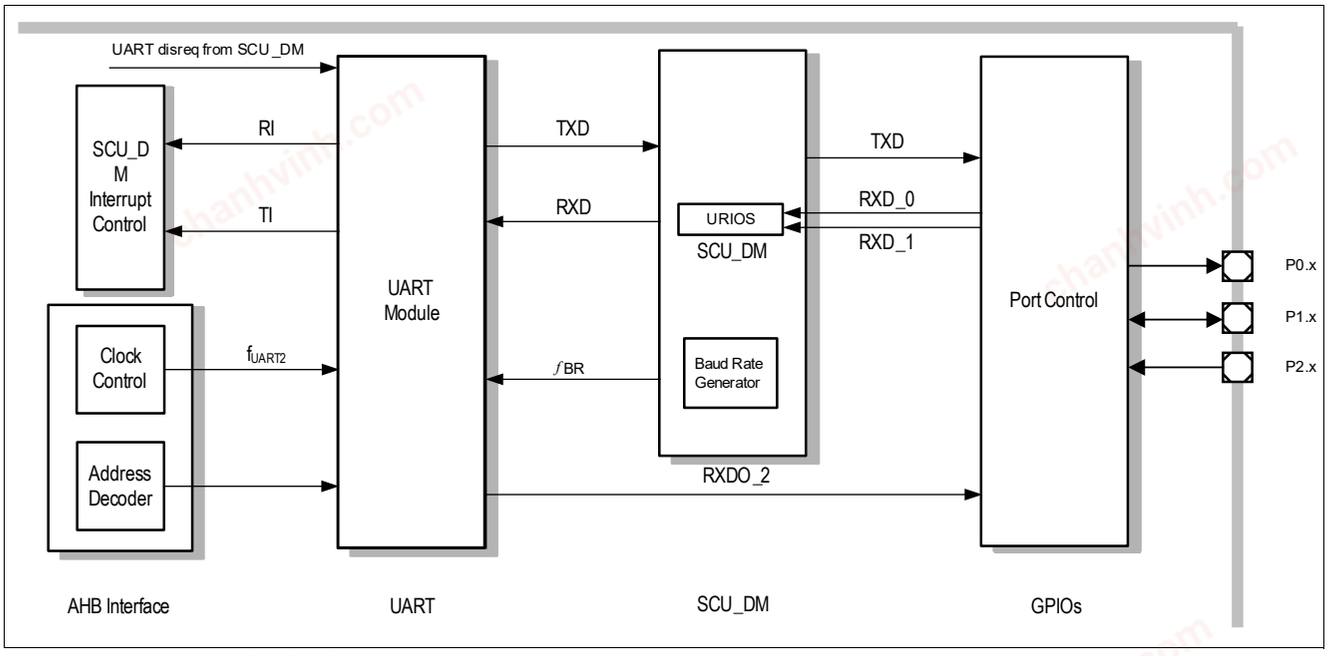


Figure 26 UART Block Diagram

18.3 UART Modes

The UART1/UART2 can be used in four different modes. In mode 0, it operates as an 8-Bit shift register. In mode 1, it operates as an 8-Bit serial port. In modes 2 and 3, it operates as a 9-Bit serial port. The only difference between mode 2 and mode 3 is the baud rate, which is fixed in mode 2 but variable in mode 3. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator.

The different modes are selected by setting bits SM0 and SM1 to their corresponding values, as shown in **Table 11**.

Mode 1 example: 8 data bits, 1 start bit, 1 stop bit, no parity selection, 16 times oversampled (majority decision of bits 6, 7, 8), receive & transmit register double buffered, Tx/Rx IRQ(s).

Table 11 UART Modes

SM0	SM1	Operating Mode	Baud Rate
0	0	Mode 0: 8-Bit shift register	$f_{sys}/2$
0	1	Mode 1: 8-Bit shift UART	Variable
1	0	Mode 2: 9-Bit shift UART	$f_{sys}/64$ or $f_{sys}/32$
1	1	Mode 3: 9-Bit shift UART	Variable

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19 LIN Transceiver

19.1 Features

General Functional Features

- Compliant to LIN2.2 Standard, backward compatible to LIN1.3, LIN2.0 and LIN 2.1
- Compliant to SAE J2602 (Slew Rate, Receiver hysteresis)

Special Features

- Measurement of LIN Master baudrate via Timer 2
- LIN can be used as Input/Output with SFR bits.
- TxD Timeout Feature (optional, on by default)
- Overcurrent limitation and overtemperature protection
- LIN module fully resettable via global enable bit

Operation Modes Features

- LIN Sleep Mode (LSLM)
- LIN Receive-Only Mode (LROM)
- LIN Normal Mode (LNM)
- High Voltage Input / Output Mode (LHVIO)

Slope Modes Features

- Normal Slope Mode (20 kbit/s)
- Low Slope Mode (10.4 kbit/s)
- Fast Slope Mode (62.5 kbit/s)
- Flash Mode (115 kbit/s, 250 kbit/s)

Wake-Up Features

- LIN Bus wake-up. The wake-up happens on the falling edge of the LIN signal, to allow wake-up and decoding of the same frame. It is possible to enter the sleep mode also with LIN dominant (e.g. caused by LIN shorted to GND).

19.2 Introduction

The LIN Module is a transceiver for the Local Interconnect Network (LIN) compliant to the LIN2.2 Standard, backward compatible to LIN1.3, LIN2.0 and LIN2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kBaud and 20 kBaud. Additionally baud rates up to 62.5 kBaud are implemented.

The LIN Module offers several different operation modes, including a LIN Sleep Mode and the LIN Normal Mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a Flash Mode up to 115 kBaud is implemented. This Flash

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Mode can be used for data transfer under special conditions for up to 250 kbit/s (in production environment, point-to-point communication with reduced wire length and limited supply voltage).

19.2.1 Block Diagram

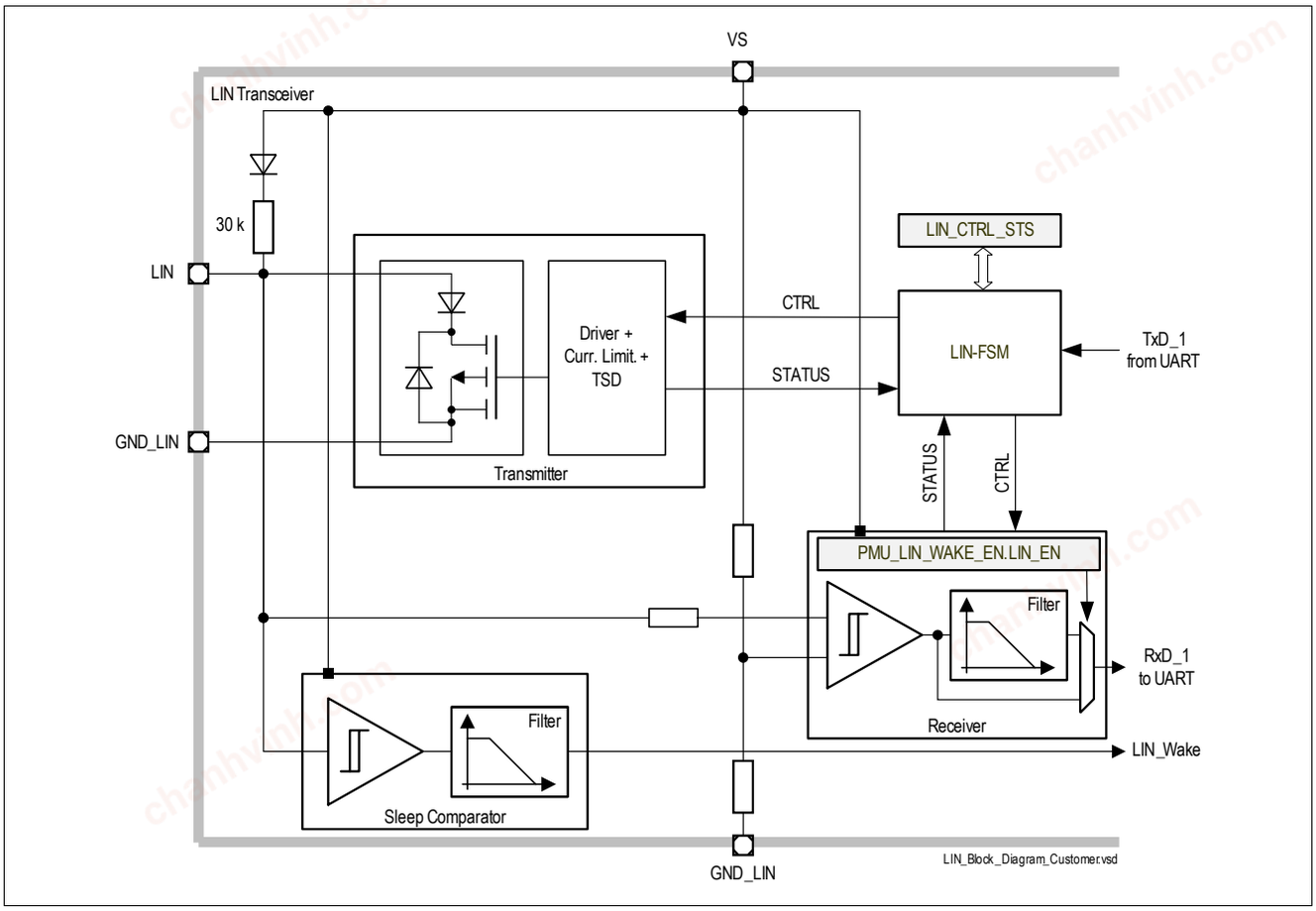


Figure 27 LIN Transceiver Block Diagram

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20 High-Speed Synchronous Serial Interface SSC1/SSC2

20.1 Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive double buffered
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: Least Significant Bit (LSB) or Most Significant Bit (MSB) shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate, e.g. 250kBaud - 8MBaud
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
  - On a transfer complete condition
- Port direction selection, see **Chapter 14**

20.2 Introduction

The High-Speed Synchronous Serial Interface (SSC) supports both full-duplex and half-duplex serial synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-Bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (MasterTransmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

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20.2.1 Block Diagram

Figure 28 shows all functional relevant interfaces associated with the SSC Kernel.

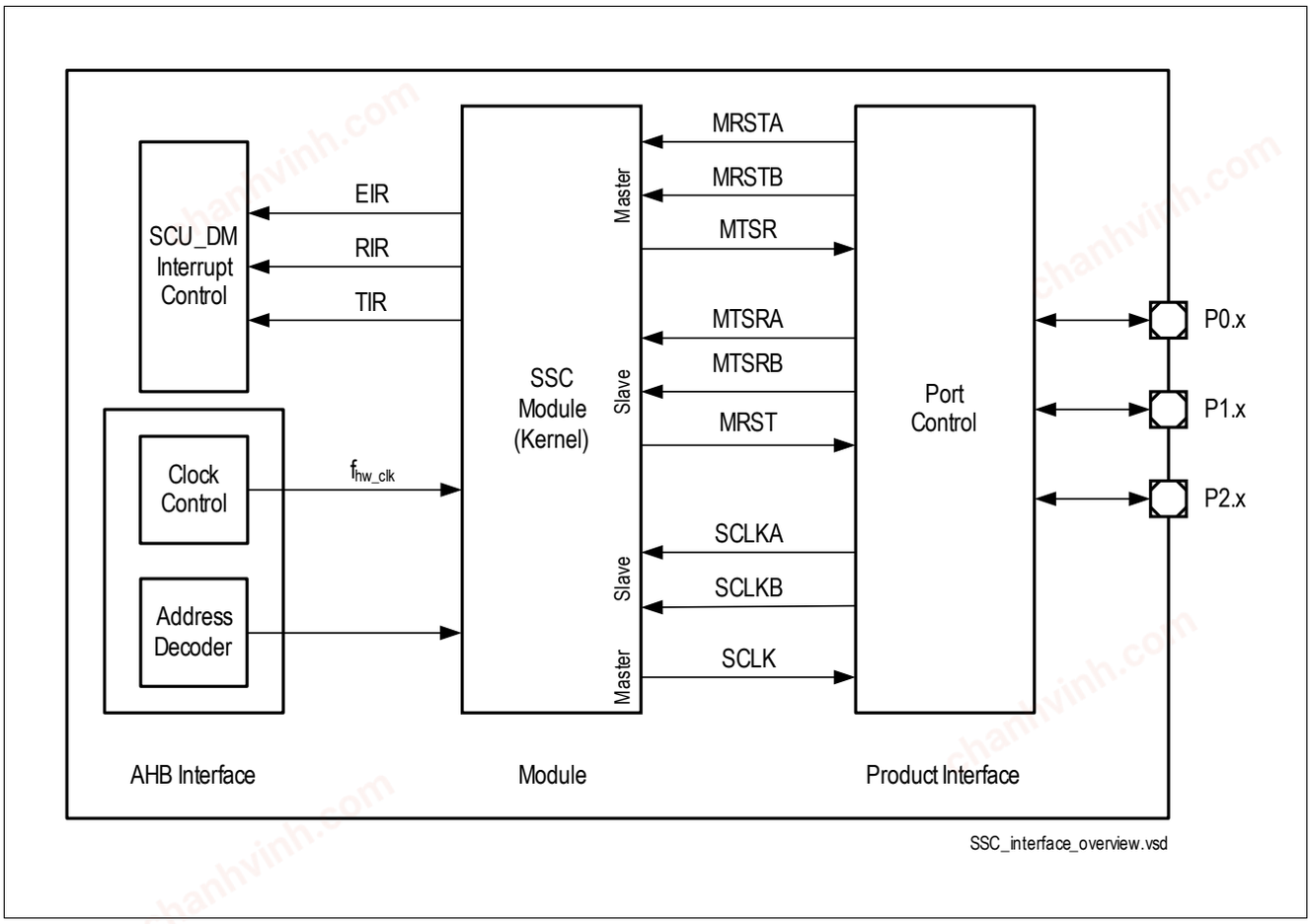


Figure 28 SSC Interface Diagram

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21 Measurement Unit

21.1 Features

- 1 x 10 Bit ADC with 13 Inputs including attenuator allowing measurement of high voltage input signals
- Supply Voltage Attenuators with attenuation of **VBAT_SENSE**, **VS, MONx**, **P2.x**.
- 1 x 8 Bit ADC with 7 Inputs including attenuator allowing measurement of high voltage input signals
- Supply Voltage Attenuators with attenuation of **VS, VDDEXT, VDDP**, **VBG, VDDC, TSENSE_LS, TSENSE_CENTRAL**.
- VBG monitoring of 8 Bit ADC to support functional safety requirements.
- Temperature Sensor for monitoring the chip temperature and Low Side module temperature.
- Supplement Block with Reference Voltage Generation, Bias Current Generation, Voltage Buffer for NVM Reference Voltage, Voltage Buffer for Analog Module Reference Voltage and Test Interface.

21.2 Introduction

The measurement unit is a functional unit that comprises the following associated sub-modules:

Table 12 Measurement functions and associated modules

Module Name	Modules	Functions
Central Functions Unit	Bandgap reference circuit + current reference circuit	The bandgap-reference sub-module provides two reference voltages 1. an accurate reference voltage for the 10-bit and 8-bit ADCs. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage arising e.g. from crosstalk or ground voltage shift. 2. the reference voltage for the NVM module
10 Bit ADC (ADC1)	10-bit ADC module with 13 multiplexed analog inputs	VBAT_SENSE, VS and MONx measurement. Six (5V) analog inputs from Port 2.x
8 Bit ADC (ADC2)	8-bit ADC module with 7 multiplexed inputs	VS/VDDEXT/VDDP/VBG/VDDC/TSENSE_LS and TSENSE_CENTRAL measurement.
Temperature Sensor	Temperature sensor readout amplifier with two multiplexed ΔVbe-sensing elements	Generates outputs voltage which is a linear function of the local chip (Tj) temperature.
Measurement Core Module	Digital signal processing and ADC control unit	1. Generates the control signal for the 8-bit ADC 2 and the synchronous clock for the switched capacitor circuits (temperature sensor) 2. Performs digital signal processing functions and provides status outputs for interrupt generation.

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21.2.1 Block Diagram

The Structure of the Measurement Functions Module is shown in the following figure.

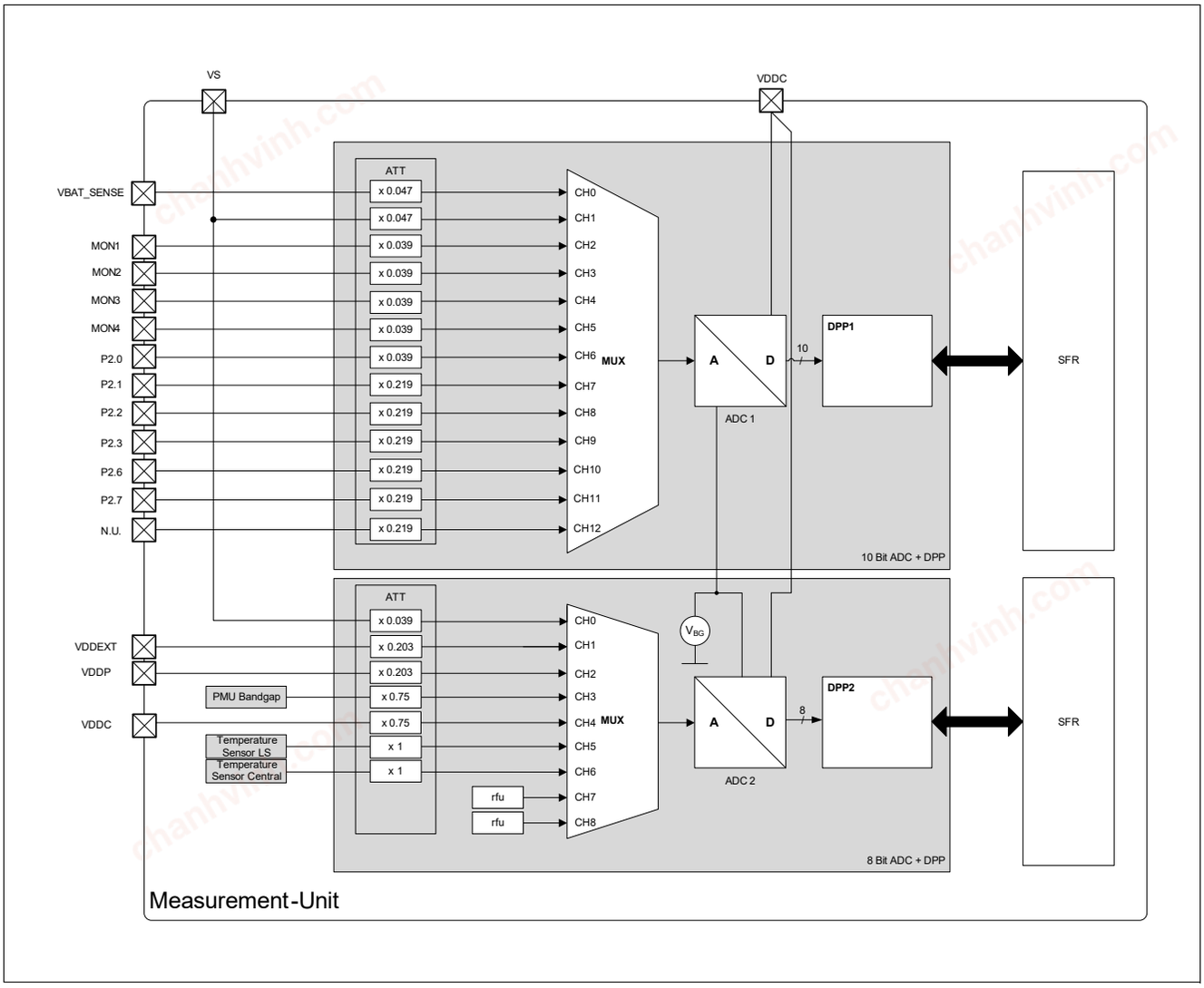


Figure 29 TLE9842QX Measurement Unit-Overview

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22 Measurement Core Module (incl. ADC2)

22.1 Features

- 7 individually programmable channels split into two groups of user configurable and non user configurable
- Individually programmable channel prioritization scheme for measurement unit
- Two independent filter stages with programmable low-pass and time filter characteristics for each channel
- Two channel configurations:
  - Programmable upper- and lower trigger thresholds comprising a fully programmable hysteresis
  - Two individually programmable trigger thresholds with limit hysteresis settings
- Individually programmable interrupts and status for all channel thresholds
- Operation down to reset threshold of entire system

22.2 Introduction

The basic function of this block is the digital postprocessing of several analog digitized measurement signals by means of filtering level comparison and interrupt generation. The measurement postprocessing block is built of seven identical channel units attached to the outputs of the 7-channel 8-bit ADC (ADC2). It processes seven channels, where the channel sequence and prioritization is programmable within a wide range.

22.2.1 Block Diagram

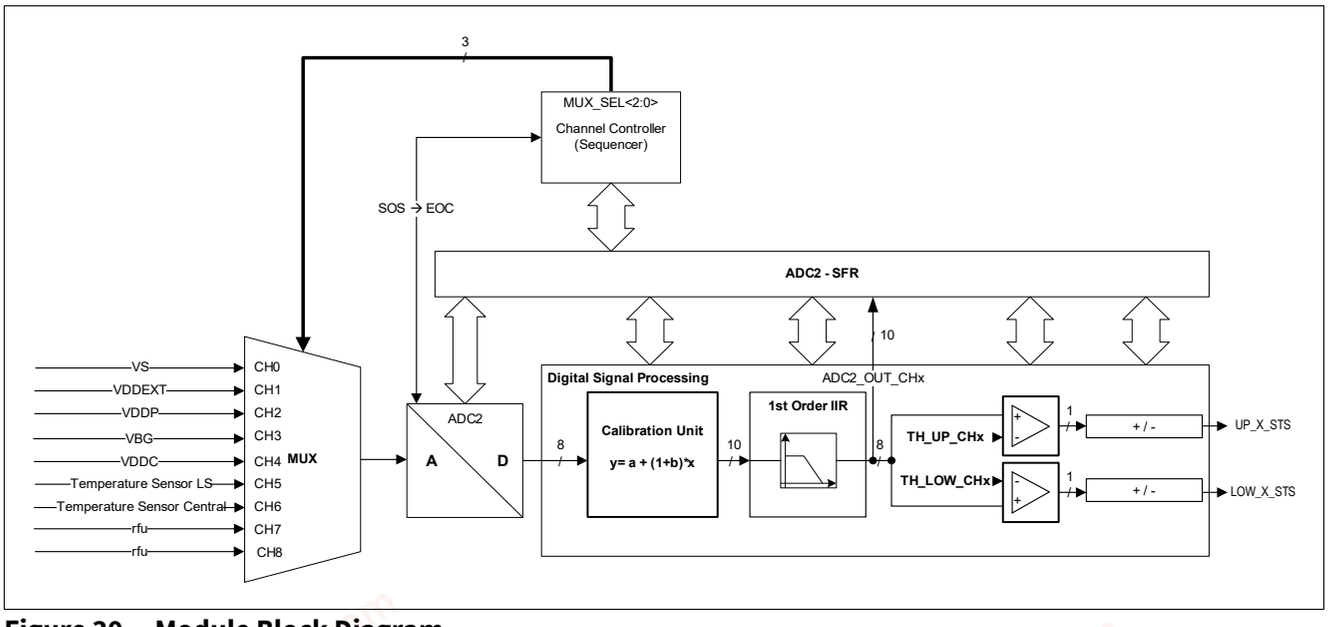


Figure 30 Module Block Diagram

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23 10-Bit Analog Digital Converter (ADC1)

23.1 Features

The basic function of this block is the digital postprocessing of several analog digitized measurement signals by means of filtering, level comparison and interrupt generation. The measurement postprocessing block is built of twelve identical channel units attached to the outputs of the 13-channel 10-bit ADC. It processes twelve channels, where the channel sequence and prioritization is programmable within a wide range.

Functional Features

- 10 Bit SAR ADC with conversion time of 17 clock cycles
- Programmable clock divider for sequencer and ADC
- 12 individually programmable channels (ch0..ch11):
  - 6 HV Channels: VS, VBAT_SENSE, MON1...MON4
  - 6 LV Channels: P2.1, P2.2, P2.3, P2.6, P2.7, P2.0
- All channels are fully calibrated and user configurable
- Individually programmable channel prioritization scheme for digital postprocessing (dpp)
- Two independent filter stages with programmable low-pass and time filter characteristics for each channel
- Two channel configurations:
  - Programmable upper- and lower trigger thresholds comprising a fully programmable hysteresis
  - Two individually programmable trigger thresholds with limit hysteresis settings
- Individually programmable upper threshold and lower threshold interrupts and status for all channel thresholds
- ADC reference completely integrated

Note: In case the MONx should be evaluated by the ADC1, it is recommended to add 6.8nF capacitors close to the MONx pin of the device, in order to build an external RC filter to limit the bandwidth of the input signal.

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23.2 Introduction

23.2.1 Block Diagram

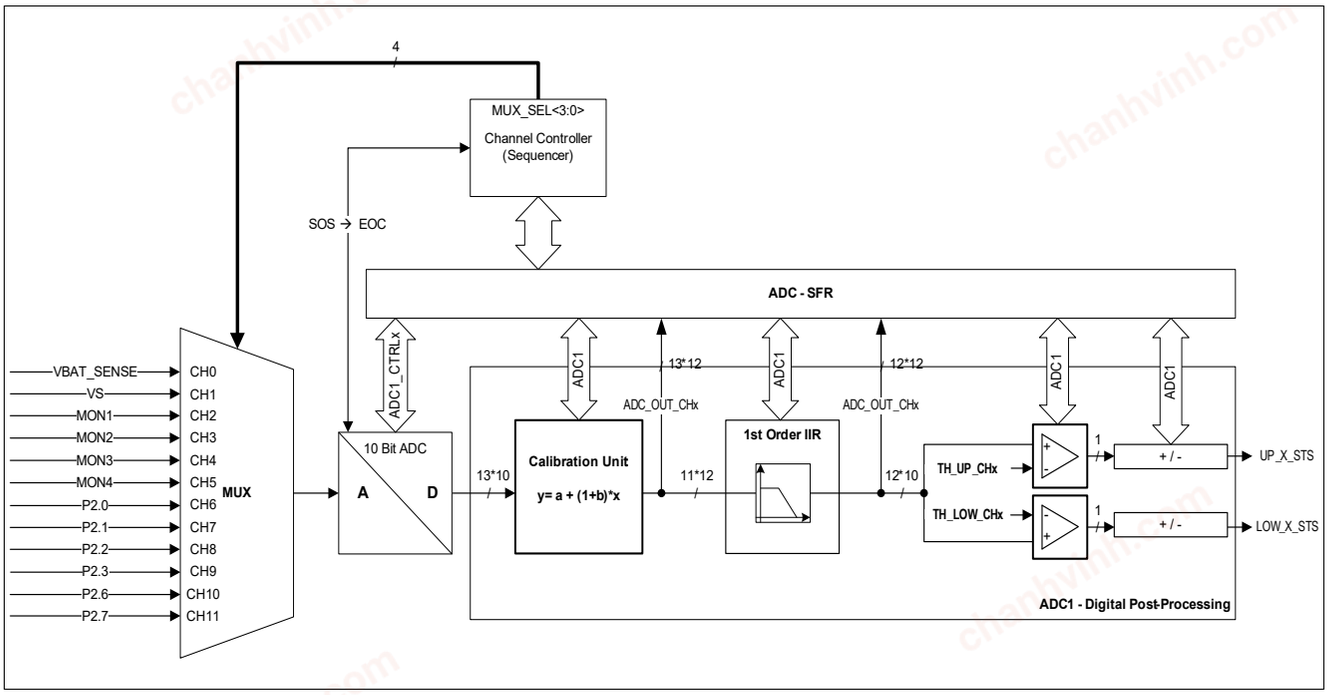


Figure 31 Module Block Diagram

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24 High-Voltage Monitor Input

24.1 Features

Features

- 4 High-voltage inputs with VS/2 threshold voltage
- Wake capability for system stop mode and system sleep mode
- Edge sensitive wake-up feature configurable for transitions from low to high, high to low or both directions
- MON inputs can also be evaluated with ADC in Active Mode, using adjustable threshold values (see also **Chapter 23**).
- Selectable pull-up and pull-down current sources available

24.2 Introduction

This module is dedicated to monitor external voltage levels above or below a specified threshold. Each MONx pin can further be used to detect a wake-up event by detecting a level change by crossing the selected threshold. This applies to any power mode. Further more each MONx pin can be sampled by the ADC as analog input.

24.2.1 Block Diagram

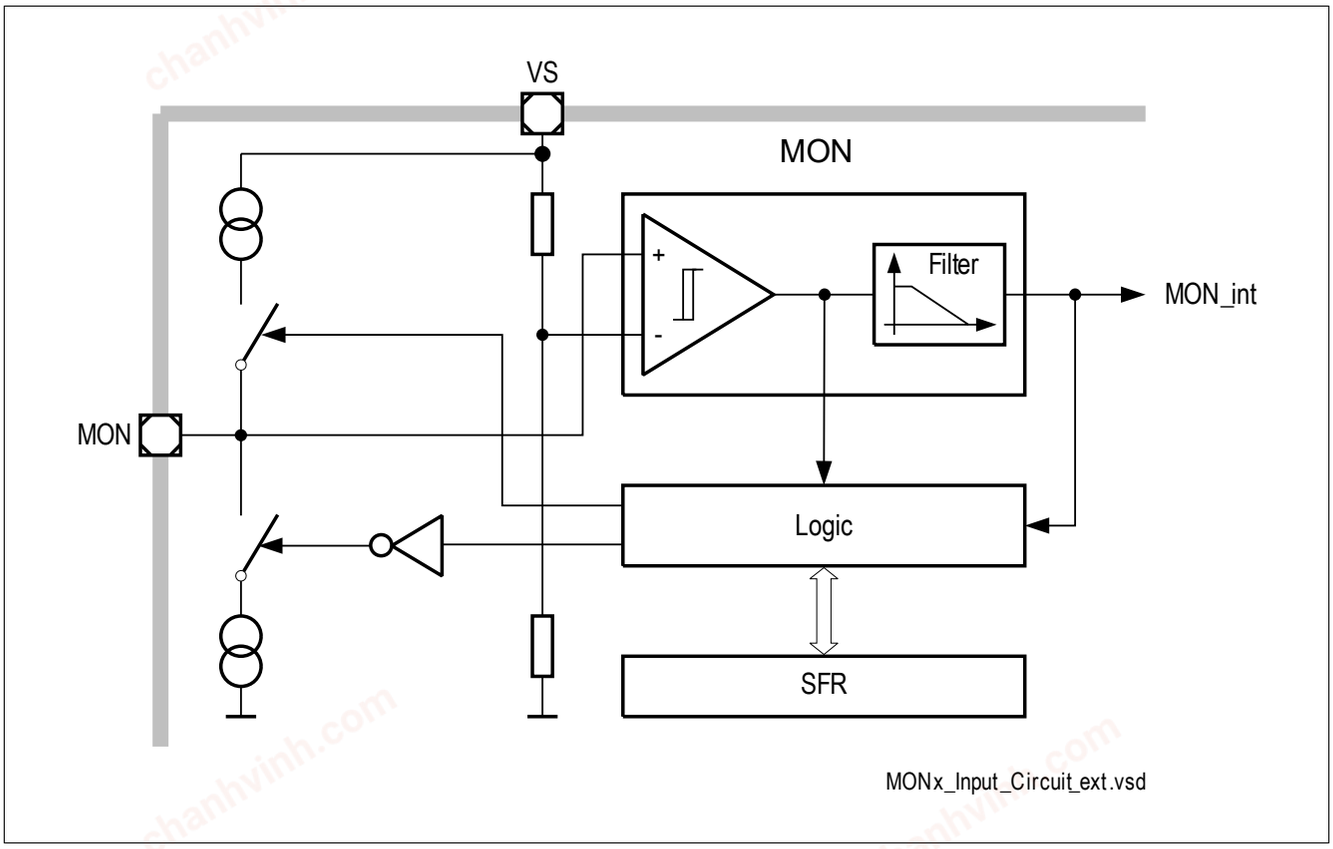


Figure 32 Monitoring Input Block Diagram

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25 High-Side Switch

25.1 Features

The high-side switch is optimized for driving resistive loads. Only small line inductance are allowed. Typical applications are single or multiple LEDs of a dashboard, switch illumination or other loads that require a high-side switch.

A cyclic switch activation during Sleep Mode or Stop Mode of the system is also available.

Functional Features

- Multi-purpose high-side switch for resistive load connections (only small line inductances are allowed)
- Overcurrent limitation
- Overcurrent detection with thresholds: 25 mA, 50 mA, 100 mA, 150 mA and automatic shutdown
- Overtemperature detection and automatic shutdown
- Open load detection in on mode with open load current of max. 1.5 mA.
- Interrupt signalling of overcurrent, overtemperature and open load condition
- Cyclic switch activation in Sleep Mode and Stop Mode with cyclic sense support and reduced driver capability: max. 40 mA
- PWM capability up to 25 kHz
- Internal connection to System-PWM Generator (CCU6)
- Slew rate control for low EMI characteristic

Applications hints

- The voltage at HSx must not exceed the supply voltage by more than 0.3V to prevent a reverse current from HSx to VS.

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25.2 Introduction

25.2.1 Block Diagram

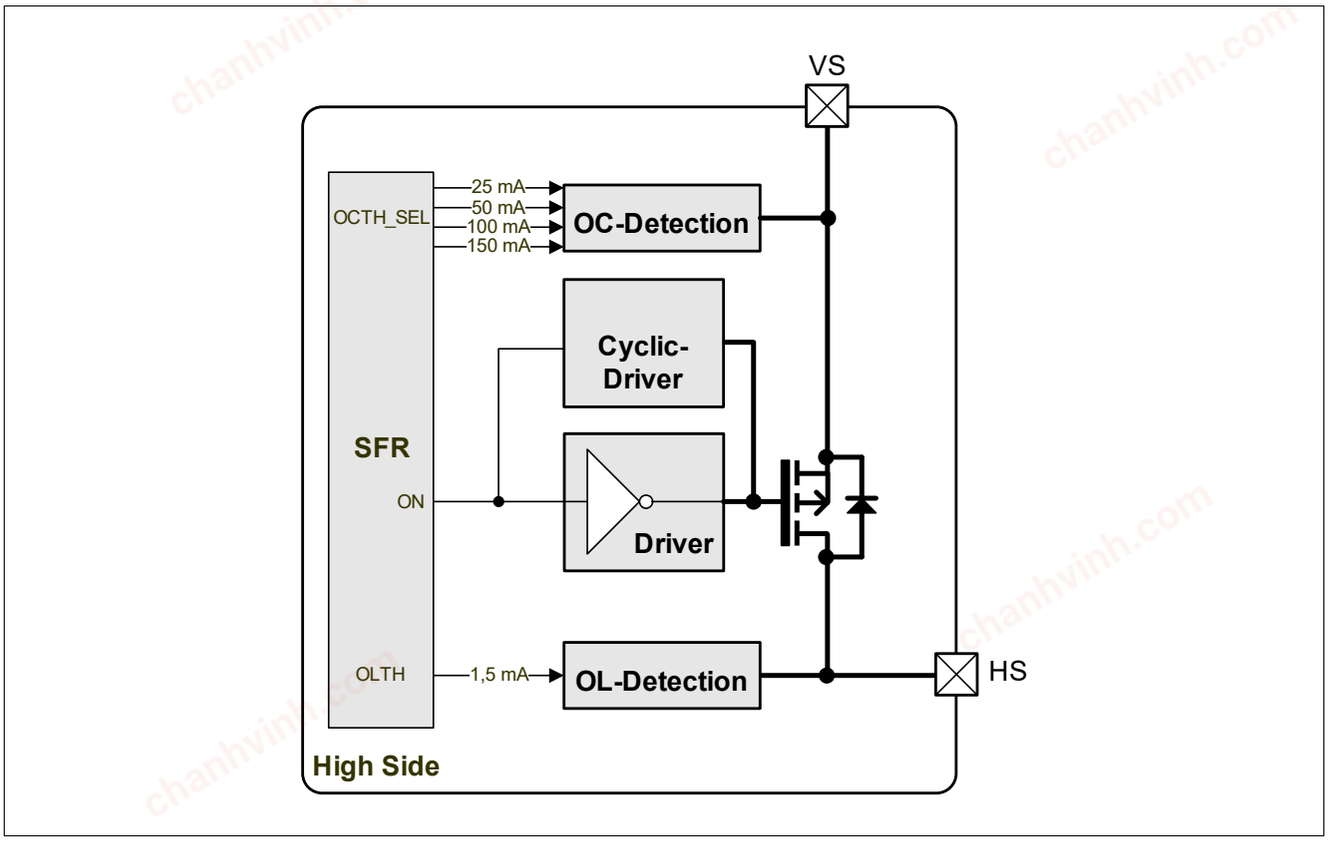


Figure 33 High-Side Module Block Diagram (incl. subblocks)

25.2.2 General

The high-side switch can generally be controlled in three different ways:

- In Normal mode the output stage is fully controllable through the **SFR** Registers **HSx_CTRL**. Protection functions as overcurrent, overtemperature and open load detection are available.
- The PWM Mode can also be enabled by a **HSx_CTRL - SFR** bit. The PWM configuration has to be done in the corresponding PWM Module. All protection functions are also available in this mode. The maximum PWM frequency must not exceed 25 kHz (disabled slew rate control only).
- The high-side switch provides also the possibility of cyclic switch activation in all low power modes (Sleep Mode and Stop Mode). In this configuration it has limited functionality with limited current capability. Diagnostic functions are not available in this mode.

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26 Low-Side Switch

26.1 Features

The general purpose low-side switch is optimized to control an on-board relay. The low-side switch provides embedded protection functions including overcurrent and overtemperature detection. The module is designed for on-board connections.

Measures for standard ESD (HBM) and EMC robustness are implemented.

Functional Features

- Multi purpose low-side switch optimized for driving relays:
  - simple relay driver
  - PWM relay driver
- Integrated clamping for usage as a simple relay driver
- overcurrent detection and automatic shutdown
- overtemperature detection and automatic shutdown
- interrupt signalling of overcurrent and overtemperature condition
- open load detection with interrupt signalling
- PWM capability up to 25 kHz (for inductive loads with external clamping circuitry only!)
- Selectable PWM source: dedicated CCU6 channels
- Current drive capability up to min. 270 mA

Applications hints

- It is not recommended to use the switch in PWM Mode without external free wheeling diode.

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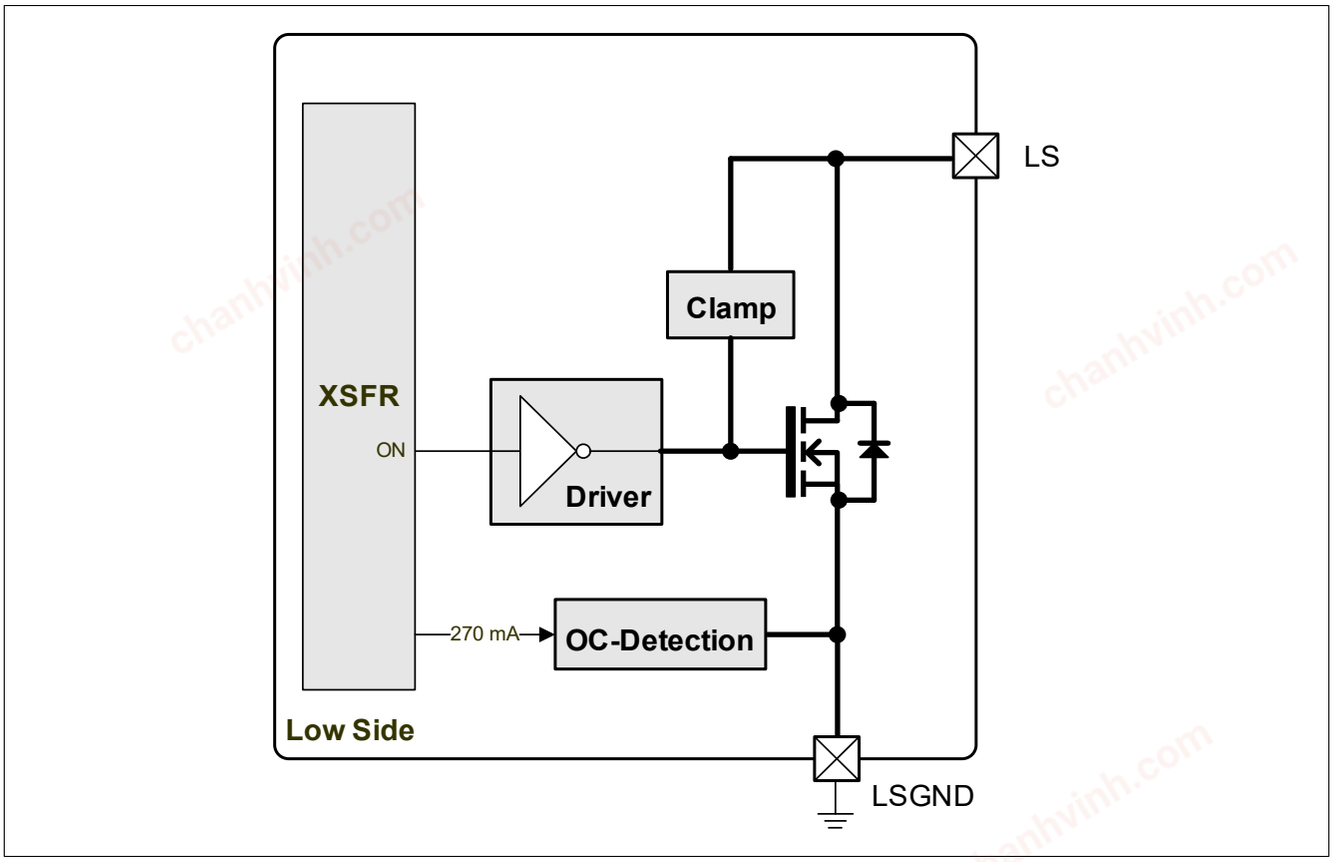


Figure 34 Module Block Diagram

26.2 Functional Description

The low-side switches can generally be controlled in two different ways:

- In normal mode the output stage is fully controllable through the **SFR** Registers **LSx_CTRL**. Protection functions as overcurrent and overtemperature are available.
- The PWM Mode can also be enabled by a **LSx_CTRL - SFR** bit. The PWM configuration has to be done in the corresponding PWM Module (CCU6). All protection functions are also available in this mode. The maximum PWM frequency must not exceed 25 kHz (fast slew rate only).

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27 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

27.1 Relay Window Lift Application diagram

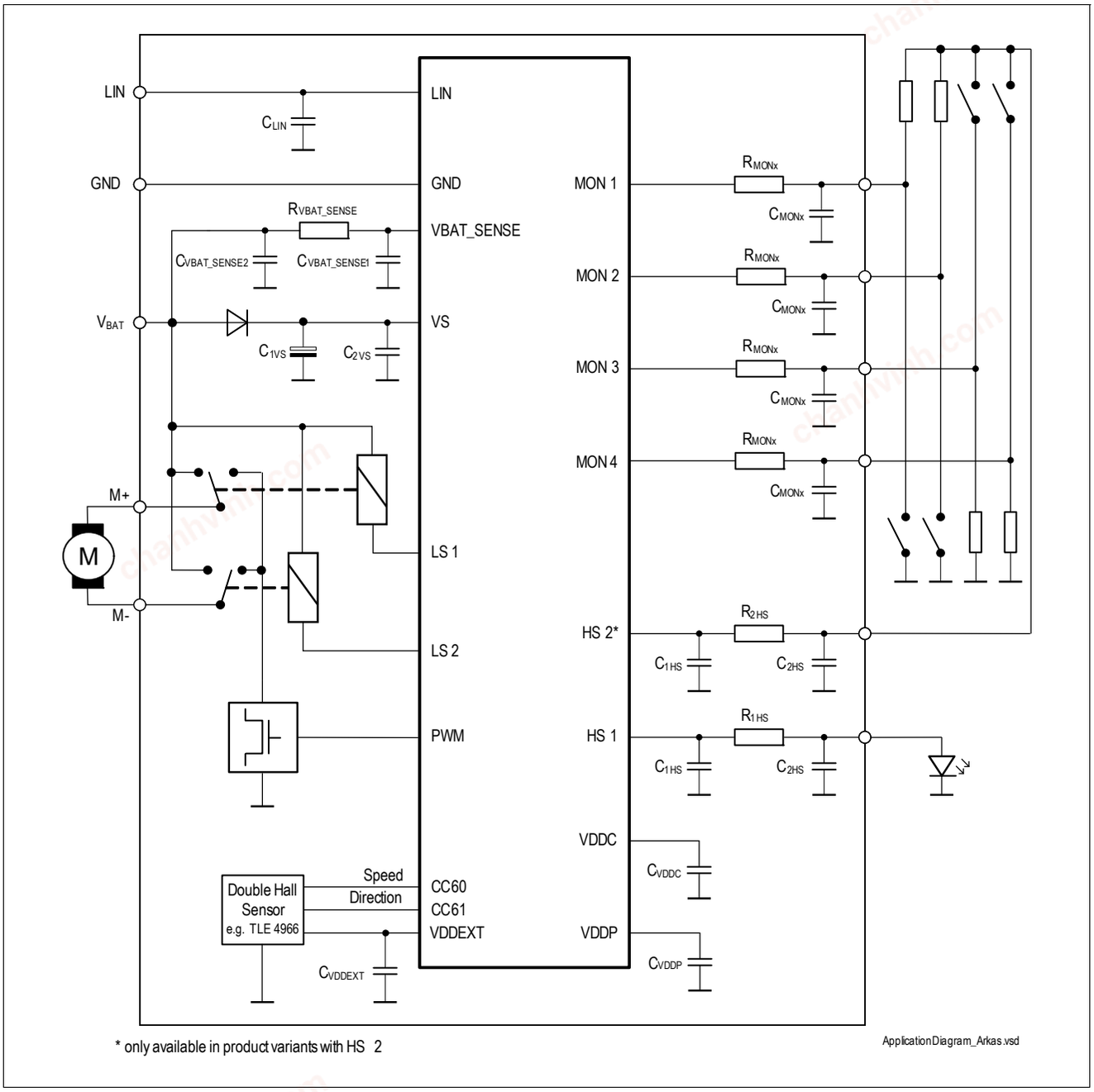


Figure 35 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the actual application.

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Table 13 External Component (BOM)

Symbol	Function	Component
C_{1VS}	Capacitor 1 at VS pin	22 µF[1)]
C_{2VS}	Capacitor 2 at VS pin	100 nF[2)3)]
C_{VDDEXT}	Capacitor at VDDEXT pin	330 nF[2)]
C_{VDDC}	Capacitor at VDDC pin	100 nF[2)3)] + 330 nF[2)]
C_{VDDP}	Capacitor at VDDP pin	470 nF[2)3)] + 470 nF[2)]
R_{MONx}	Resistor at MONx pin	3.9 kΩ
C_{MONx}	Capacitor at MONx connector	6.8 nF[4)]
R_{VBAT_SENSE}	Resistor at VBAT_SENSE pin	3.9 kΩ
C_{VBAT_SENSE1}	Capacitor 1at VBAT_SENSE pin	10 nF[2)]
C_{VBAT_SENSE2}	Capacitor 2 at VBAT_SENSE connector	6.8 nF[4)]
C_{LIN}	Capacitor at LIN pin	220 pF
R_{1HS}	Resistor at HS pin for LED	e.g. 2.7kΩ
R_{2HS}	Resistor at HS pin	160 Ω[5)]
C_{1HS}	Capacitor at HS pin	6.8nF[2)]
C_{2HS}	Capacitor at HS connector	33nF[4)]

1) to be dimensioned according to application requirements
2) to reduce the effect of fast voltage transients of Vs, these capacitors should be placed close to the device pin
3) ceramic capacitor
4) for ESD GUN
5) optional, for short to battery protection, calculated for 24V (jump start)

27.2 Connection of N.C. / N.U. pins

The device contains several N.C. (not connected, no bond wire) and N.U. (not used, but bonded) pins.

Table 14 Recommendation for connecting N.C. / N.U. pins

type	pin number	recommendation 1	recommendation 2	comment
N.C.	27, 28, 29, 38, 40, 41	GND		
N.C.	10, 46	open	GND	neighboring high-voltage pins
N.U.	4	VS	open	
N.U.	9	GND		

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27.3 Connection of unused pins

Table 15 shows recommendations how to connect pins, in case they are not needed by the application.

Table 15 Recommendation for connecting unused pins

type	pin number	recommendation 1 (if unused)	recommendation 2 (if unused)
LIN	1	open	
HS1	3	VS	open
MON	5, 6, 7, 8	GND	open + configure internal PU/PD
LS1, LS2	11, 12	GNDLS	open
GPIO	14, 15, 16, 17, 20, 22, 23, 24, 25, 26, 33, 34, 35, 36, 37, 39	GND	external PU/PD or open + configure internal PU/PD
TMS	18	GND	
Reset	21	open	
P2/XTAL out	31	open	
P2/XTAL in	32	GND	
VDDEXT	45	open	
VBAT_SENSE	48	VS	

27.4 Connection of P0.2 for SWD debug mode

To enter the SWD debug mode, P0.2 needs to be 0 at the rising edge of the reset signal.

P0.2 has an internal pulldown, so it just needs to be ensured that there is no external 1 at P0.2 when the debug mode is entered.

27.5 Connection of TMS

For the debug mode, the TMS pin needs to be 1 at the rising edge of the reset signal. This is controlled by the debugger. The TMS pin has an internal PD.

To avoid the device entering the debug mode unintendedly in the final application, adding an external pull-down additionally is recommended.

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27.6 ESD Immunity According to IEC61000-4-2

*Note: Tests for ESD robustness according to IEC61000-4-2 “gun test” (150pF, 330Ω) were performed. The results and test condition are available in a test report. The achieved values for the test are listed in **Table 16** below.*

Table 16 ESD “Gun Test”

Performed Test	Result	Unit	Remarks
ESD at pin LIN, versus GND	≥6	kV	[1)]positive pulse
ESD at pin LIN, versus GND	≤ -6	kV	[1)]negative pulse
ESD at pin VS, VBAT_SENSE, MONx, HS, versus GND	≥6	kV	[1)]positive pulse
ESD at pin VS, VBAT_SENSE, MONx, HS, versus GND	≤ -6	kV	[1)]negative pulse

1) ESD susceptibility “ESD GUN”, tested by external test house (IBEE Zwickau, EMC Test report Nr. 11-01-16), according to "LIN Conformance Test Specification Package for LIN 2.1, October 10th, 2008" and "Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Application – AUDI, BMW, Daimler, Porsche, Volkswagen – Revision 1.3 / 2012"

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28 Electrical Characteristics

This chapter includes all relevant Electrical Characteristics of the product TLE9842QX.

28.1 General Characteristics

28.1.1 Absolute Maximum Ratings

Table 17 Absolute Maximum Ratings[1)]

T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages Supply Pins							
VS voltage	$V_{S,max}$	-0.3	–	40	V	Load dump	P_1.1.1
VDDP voltage	$V_{DDP,max}$	-0.3	–	5.5	V	–	P_1.1.2
VDDEXT voltage	$V_{DDEXT,max}$	-0.3	–	V_S +0.3	V	–	P_1.1.3
VDDC voltage	$V_{DDC,max}$	-0.3	–	1.6	V	–	P_1.1.4
Voltages High Voltage Pins							
Voltage at VBAT_SENSE pin	$V_{BAT_SENSE,max}$	-28	–	40	V	[2)]–	P_1.1.5
Voltage at HS pin	$V_{HS,max}$	-0.3	–	V_S +0.3	V	–	P_1.1.6
Voltage at LIN pin	$V_{LIN,max}$	-28	–	40	V	–	P_1.1.7
Voltage at MON_x pins	$V_{MON,max}$	-28	–	40	V	[2)]	P_1.1.8
Voltage at LS pin	$V_{LS,max}$	-0.3	–	40	V	Internal clamping structure > 40V	P_1.1.9
Voltages GPIOs							
Voltage on port pin P0.x, P1.x, P2.x, TMS and RESET	$V_{IO,max}$	-0.3	–	V_{DDP} +0.3	V	$V_{IN} < V_{DDPmax}$	P_1.1.10
Currents							
Injection current in Sleep Mode on P0.x, P1.x, P2.x, TMS and RESET	I_{xx}	–	–	5	mA	maximum allowed injection current on single pin or sum of pins in Sleep Mode and unpowered device	P_1.1.11
Injection current on HS	I_{XLO}	–	–	150	mA	current flowing into HS pin (back supply in case of short to battery)	P_1.1.12

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Table 17 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output current on LS	I_{LS}	-300	–	–	mA	current flowing out of LS pin, e.g. reverse polarity event (defined in LV124) or ISO Pulse event (defined in ISO 7637-2)	P_1.1.13
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_1.1.14
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_1.1.15
ESD Susceptibility							
ESD Susceptibility **HBM** all pins	V_{ESD1}	-2	–	2	kV	JEDEC HBM[3)]	P_1.1.16
ESD Susceptibility **HBM** pins LIN vs. LINGND	V_{ESD3}	-6	–	6	kV	JEDEC HBM[3)]	P_1.1.17
ESD Susceptibility **CDM**	V_{ESD_CDM}	–500	–	500	V	Charged device model, acc. JEDEC JESD22-C101	P_1.1.18
ESD Susceptibility **CDM** pins 1, 12, 13, 24, 25, 36, 37, 48 (corner pins)	V_{ESD_CDM}	–750	–	750	V	Charged device model, acc. JEDEC JESD22-C101	P_1.1.19

1) Not subject to production test, specified by design.
2) for -28V, external 3.9kΩ resistor is required to limit output current.
3) ESD susceptibility, "JEDEC HBM" according to ANSI/ESDA/JEDEC JS001 (1.5kΩ, 100pF).

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

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28.1.2 Functional Range

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Table 18 Functional Range

T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage in Active Mode	V_{S_AM}	5.5	–	28	V	–	P_1.2.1
Extended Supply voltage in Active Mode - Range 1	$V_{S_AM_extend_1}$	28	–	40	V	Functional with parameter deviation[1]	P_1.2.12
Extended Supply voltage in Active Mode with reduced functionality (Microcontroller / Flash with full operation) - Range 2	$V_{S_AM_extend_2}$	3.0	–	5.5	V	Functional with parameter deviation[2]	P_1.2.2
Specified Supply voltage for LIN Transceiver - Active Mode	$V_{S_AM_LIN}$	5.5	–	18	V	Parameter Specification	P_1.2.3
Extended Supply voltage for LIN Transceiver - Active Mode	$V_{S_AM_LIN_extend}$	4.8	–	28	V	Functional with parameter deviation	P_1.2.4
Extended Supply voltage for LIN & Monitoring Input (MON) - Stop & Sleep Mode	$V_{S_SSM_LIN_MON_extend}$	3.6	–	5.5	V	Wakeup functionality ensured	P_1.2.13
Min. Supply voltage in Stop Mode	$V_{S_Stopmin}$	3.0	–	–	V	–	P_1.2.5
Min. Supply voltage in Sleep Mode	$V_{S_Sleepmin}$	3.0	–	–	V	–	P_1.2.6
Supply Voltage transients slew rate	dV_S/dt	-5	–	5	V/µs	[3]	P_1.2.7
Output current on any GPIO	I_{OH}, I_{OL}	-10	–	10	mA	[3]	P_1.2.8
Output sum current for all GPIO pins	$I_{GPIO,sum}$	-50	–	50	mA	[3]	P_1.2.9
Operating frequency	f_{sys} [4]	5	–	25	MHz	[3]	P_1.2.10
Junction Temperature	T_j	-40	–	150	°C	–	P_1.2.11

1) This operation voltage range is only allowed for a short duration: $t_{max} \leq 400$ ms.
2) Hall-Supply, ADC, SPI, UART, NVM, RAM, CPU fully functional and in spec down to 3V VS. Actuators (HS, LS) in VS range from 3V < VS < 5.5V functional but some parameters can be out of spec
3) Not subject to production test, specified by design.
4) Function not specified when limits are exceeded.

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28.1.3 Current Consumption

Table 19 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption @VS pin							
Current Consumption in Active Mode	$I_{Vs_freduced}$	–	–	15	mA	fsys = 10 MHz V_s= 13.5V all digital modules enabled and functional, ADCs converting in sequencer mode, PLL running, no loads on GPIOs, VDDEXT off, LIN in recessive state (no communication), HSx & LSx enabled but off[1)]	P_1.3.1
Current Consumption in Active Mode	I_{Vs}	–	14	18	mA	fsys = 25 MHz V_s= 13.5V all digital modules enabled and functional, ADCs converting in sequencer mode, PLL running, no loads on GPIOs, VDDEXT off, LIN in recessive state (no communication), HSx & LSx enabled but off	P_1.3.22
Current consumption in Sleep Mode	I_{Sleep}	–	–	15	µA	System in Sleep Mode, microcontroller not powered, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND: T_J = -40°C to 25°C; V_s = 13.5V	P_1.3.2
Current consumption in Sleep Mode (extended Temperature Range)	$I_{Sleep(T_extend)}$	–	–	25	µA	System in Sleep Mode, microcontroller not powered, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND: T_J = 25°C to 85°C; V_s = 13.5V	P_1.3.3

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Table 19 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in Sleep Mode (extended Voltage and Temperature Range)	$I_{Sleep(V_T_extend)}$	–	–	30	µA	System in Sleep Mode, microcontroller not powered, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND: T_J = -40°C to 85°C; V_s = 5.5V to 18V	P_1.3.4
Current consumption in Sleep Mode (extended Voltage and Temperature Range 2)	$I_{Sleep(V_T_extend2)}$	–	–	40	µA	System in Sleep Mode, microcontroller not powered, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND: T_J = -40°C to 85°C; V_s = 3V to 28V	P_1.3.7
Current consumption in Sleep Mode with cyclic wake	I_{Cyclic}	–	–	15	µA	T_J = -40°C to 25°C; V_s = 13.5V during sleep period	P_1.3.5
Current consumption in Sleep Mode with cyclic wake (extended Temperature Range)	$I_{Cyclic(T_extend)}$	–	–	30	µA	T_J = 25°C to 85°C; V_s = 13.5V; during sleep period	P_1.3.6
Current consumption in Stop Mode	I_{Stop}	–	65	115	µA	System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND; T_J = -40°C to 85°C	P_1.3.19

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Table 19 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in Stop Mode	$I_{Stop_V_extend}$	–	3.5	4.0	mA	System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND; T_J = -40°C to 85°C; V_s = 3V	P_1.3.21
Current consumption in Stop Mode with cyclic sense	I_{Stop_CS}	–	70	125	µA	System in Stop Mode (during stop period), microcontroller not clocked, Wake capable via LIN and MON; VDDEXT off; High Side off; GPIOs open (no loads) or connected to GND or VDDP; T_J = -40°C to 85°C; V_s = 5.5V to 28V	P_1.3.20

1) Not subject to production test, specified by design

28.1.4 Thermal Resistance

Table 20 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	$R_{th(JC)}$	–	6	–	K/W	1) measured to Exposed Pad	P_1.4.1
Junction to Ambient	$R_{th(JA)}$	–	33	–	K/W	2)	P_1.4.2

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board . Board: 76.2x114.3x1.5mm^3 with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm2 cooling area on the bottom layer (70µm).

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28.1.5 Timing Characteristics

The transition times between the system modes are specified here. Generally the timings are defined from the time when the corresponding Bits in register PMCON0 are set until the sequence is terminated.

Table 21 System Timing[1)]

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Wake-up over battery	t_{start}	–	–	1	ms	Battery ramp-up till MCU reset is released; Vs > 3V and RESET = ’1’	P_1.5.1
Sleep-Exit	$t_{sleep\ -\ exit}$	–	–	1	ms	rising/falling edge of any wake-up signal (LIN, MON) till MCU software running	P_1.5.2
Sleep-Entry	$t_{sleep\ -\ entry}$	–	–	330	µs	2)	P_1.5.3

1) Not subject to production test, specified by design.
2) Wake events during Sleep-Entry are stored and lead to wake-up after Sleep Mode is reached.

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28.2 Power Management Unit (PMU)

This chapter includes all electrical characteristics of the Power Management Unit

28.2.1 PMU Input Voltage VS

Table 22 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Required decoupling capacitance	C_{VS1}	0.1	–	–	µF	1) ESR < 1Ω	P_2.1.12
Required buffer capacitance for stability (load jumps)	C_{VS2}	10	–	–	µF	2)	P_2.1.13

1) only min. value is tested.

2) Not subject to production test, specified by design.

28.2.2 PMU I/O Supply Parameters VDDP

Table 23 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Specified Output Current	I_{VDDP}	0	–	50	mA	2)	P_2.1.1
Required decoupling capacitance	C_{VDDP1}	0.47	–	–	µF	3)4) ESR < 1Ω	P_2.1.2
Required buffer capacitance for stability (load jumps)	C_{VDDP2}	0.47	–	1	µF	4)5)	P_2.1.3
Output Voltage including line and load regulation @ Active Mode	V_{DDPOUT}	4.9	5.0	5.1	V	6) I_{load} < 90mA;Vs > 5.5V	P_2.1.4
Output Voltage including line and load regulation @ Stop Mode	$V_{DDPOUTSTOP}$	4.5	5.0	5.25	V	6) I_{load} is only internal;Vs > 5.5V	P_2.1.5
Output Drop	$Vs_{V\ DDPout}$	–	50	+400	mV	7) I_{VDDP} = 50mA; V_S = 3V;	P_2.1.6
Load Regulation	$V_{VDDPLOR}$	-50	–	50	mV	2 ... 90mA; C = C_{VDDP1}+C_{VDDP2}	P_2.1.7
Line Regulation	$V_{VDDPLIR}$	-50	–	50	mV	V_s= 5.5 ... 28V	P_2.1.8
Over Voltage Detection	V_{DDPOV}	5.14	–	5.4	V	V_s > 5.5V; Overvoltage leads to SUPPLY_NMI	P_2.1.9

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Table 23 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Under Voltage Reset	V_{DDPUV}	2.55	2.7	2.8	V	–	P_2.1.10
Over Current Diagnostic	I_{VDDPOC}	90	–	200	mA	current including VDDC current consumption	P_2.1.11

1) currents used in this table are positive but flowing out the pin VDDP
2) Specified output current for port supply and additional other external loads connected to VDDP, excluding on-chip current consumption.
3) only min. value is tested.
4) the total capacitance on VDDP must not exceed 2,2 µF
5) Not subject to production test, specified by design.
6) Load current includes internal supply.
7) Output drop for I_{VDDP} plus internal supply

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28.2.3 PMU Core Supply Parameters VDDC

Table 24 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Required decoupling capacitance	C_{VDDC1}	0.1	–	–	µF	1) ESR < 1Ω	P_2.2.1
Required buffer capacitance for stability (load jumps)	C_{VDDC2}	0.33	–	1	µF	2)	P_2.2.2
Output Voltage including line regulation @ Active Mode/Stop Mode	V_{DDCOUT}	1.44	1.5	1.56	V	I_{load} < 40mA; with setting of VDDC output voltage to 1.5V in Stop Mode	P_2.2.3
Load Regulation	V_{DDCLOR}	-50	–	50	mV	2 ... 40mA; C = C_{VDDC1}+C_{VDDC2}	P_2.2.4
Line Regulation	V_{DDCLIR}	-25	–	25	mV	V_s= 5.5 ... 28V	P_2.2.5
Over Voltage Detection	V_{DDCOV}	1.58	–	1.68	V	Overvoltage leads to SUPPLY_NMI	P_2.2.6
Under Voltage Reset	V_{DDVUV}	1.10	–	1.19	V	–	P_2.2.7
Over Current Diagnostic	I_{VDDCOC}	40	–	80	mA	–	P_2.2.8

1) only min. value is tested.

2) Not subject to production test, specified by design.

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28.2.4 VDDEXT Voltage Regulator 5.0V

Table 25 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VDDEXT Regulator Active Mode							
Specified Output Current	I_{VDDEXT}	0	–	20	mA	current flowing out of pin VDDEXT	P_2.3.1
Required decoupling capacitance	$C_{VDDEXT1}$	330	–	1000	nF	2) ESR < 1 Ω	P_2.3.2
Required buffer capacitance for stability (load jumps)	$C_{VDDEXT2}$	100	–	1000	nF	3)	P_2.3.3
Output Voltage including line and load regulation	V_{DDEXT}	4.9	5.0	5.1	V	I_{load} < 20mA;Vs ≥ 5.5V	P_2.3.4
Output Drop	V_s-V_{DDEXT}		50	+400	mV	I_{load} < 20mA; 3V < V_s < 5.0V	P_2.3.5
Load Regulation	$V_{DDEXTLOR}$	-80	–	20	mV	0.01 ... 20mA; C = $C_{VDDEXT1}$+$C_{VDDEXT2}$; V_s≥ 5.5V	P_2.3.6
Line Regulation	$V_{VDDEXTLIR}$	-50	–	50	mV	V_s= 5.5 ... 28V	P_2.3.7
Power Supply Ripple Rejection	$P_{SSRVDDEXT}$	50	–	–	dB	3) V_s= 13.5V; f=0 ... 1KHz; Vr=2Vpp; 0 ... 20mA	P_2.3.8
Under Voltage Shutdown	$V_{VDDEXTUV}$	1.55	1.9	2.2	V	4)	P_2.3.9
Over Current Limitation	$I_{VDDEXTOC}$	100	250	380	mA	3)	P_2.3.10
VDDEXT output discharge resistance	R_{VDDEXT_DISCHG}	16	20	24	kΩ	–	P_2.3.11
VDDEXT Regulator Low Current Mode							
Specified Output Current	I_{VDDEXT_LCM}	0	–	5	mA	–	P_2.3.28
Output Voltage including line and load regulation - Load 1	V_{DDEXT_LCM1}	4.6	5.0	5.1	V	I_{load} ≤ 5mA;Vs ≥ 5.5V	P_2.3.29
Output Drop - Load 1	V_s-V_{DDEXT_LCM1}		50	+300	mV	I_{load} ≤ 5mA; 3V < V_s ≤ 5V; C = $C_{VDDEXT1}$+$C_{VDDEXT2}$	P_2.3.30
Load Regulation - Load 1	$V_{DDEXTLOR_LCM1}$	-250	–	250	mV	0 ... 5mA; C = $C_{VDDEXT1}$+$C_{VDDEXT2}$; V_s≥ 5.5V	P_2.3.31

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Table 25 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Line Regulation - Load 1	$V_{VDDEXTLIR_LCM1}$	-300	–	300	mV	I_{load} ≤ 5mA; V_s= 5.5 ... 28V	P_2.3.32
Power Supply Ripple Rejection	$P_{SSRVDDEXT_LCM}$	50	–	–	dB	3) V_s= 13.5V; f=0 ... 1KHz; Vr=2Vpp; 0 ... 5mA	P_2.3.33

1) currents used in this table are positive but flowing out the pin VDDEXT
2) only min. value is tested.
3) Not subject to production test, specified by design.
4) When condition is met, the Bit VDDEXT_CTRL.VDDEXT_UV_IS will be set.

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28.2.5 VPRE Voltage Regulator (PMU Subblock) Parameters

The PMU VPRE Regulator acts as a supply of VDDP and VDDC voltage regulators.

Table 26 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Specified Output Current	I_{VPRE}	–	–	90	mA	1)	P_2.4.1

1) Not subject to production test, specified by design.

28.2.5.1 Load Sharing of VPRE Regulator

The figure below shows the load sharing concept of VPRE regulator.

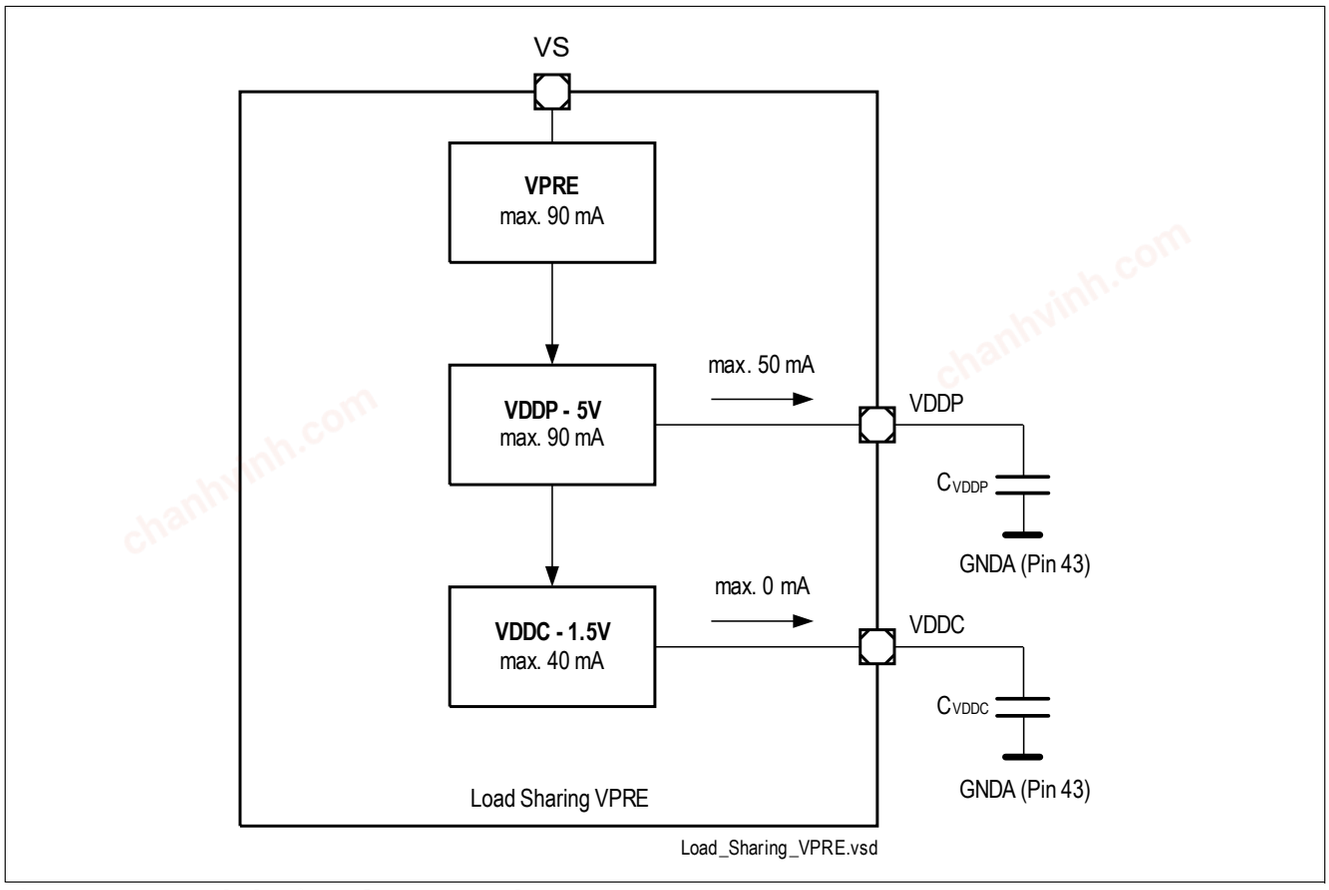


Figure 36 Load Sharing of VPRE Regulator

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28.2.6 Power Down Voltage Regulator (PMU Subblock) Parameters

The PMU Power Down voltage regulator consists of two subblocks:

- Power Down Pre regulator: VDD5VPD
- Power Down Core regulator: VDD1V5_PD (Supply used for GPUDATAxy registers)

Both regulators are used as purely internal supplies. The following table contains all relevant parameter:

Table 27 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power-On Reset Threshold	$V_{DD1V5_PD_RSTTH}$	1.2	–	1.5	V	1) I_{load} = internal load connected to VDD1V5_PD	P_2.5.1

1) Not subject to production test, specified by design

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28.3 System Clocks

28.3.1 Electrical Characteristics Oscillators and PLL

Table 28 Electrical Characteristics System Clocks

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PMU Oscillators (Power Management Unit)							
Frequency of LP_CLK	f_{LP_CLK}	17	20	23	MHz	this clock is used at startup and can be used in case the PLL fails	P_3.1.1
Frequency of LP_CLK2	f_{LP_CLK2}	70	100	130	kHz	this clock is used for cyclic wake	P_3.1.2
CGU Oscillator (Clock Generation Unit Microcontroller)							
Short term frequency deviation[1)]	f_{TRIMST}	-0.4%	–	+0.4%	MHz	within any 100 ms, e.g. after synchronization to a LIN frame (includes PLL accumulated jitter value).Assuption: T_j is varying < 30°C.	P_3.1.3
Absolute accuracy	$f_{TRIMABSA}$	-1.49%	–	+1.49%	MHz	Including temperature& lifetime drift and supply variation	P_3.1.4
CGU-OSC Start-up time	t_{OSC}	–	–	10	µs	[2)] startup time OSC from Sleep Mode, power supply stable	P_3.1.5
PLL (Clock Generation Unit Microcontroller) [2)]							
VCO reference frequency range	f_{REF}	0.8	1	1.25	MHz	–	P_3.1.25
VCO frequency (tuning) range	f_{VCO}	75	–	160	MHz	–	P_3.1.21
Input frequency range	f_{OSC}	4	–	6	MHz	see also specified limits for f_{VCO} and f_{REF} resulting in restrictions for possible N divider settings	P_3.1.6
XTAL1 input freq. range	f_{OSCHP}	4	–	6	MHz	see also specified limits for f_{VCO} and f_{REF} resulting in restrictions for possible N divider settings	P_3.1.23

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Table 28 Electrical Characteristics System Clocks (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output freq. range	f_{PLL}	15	–	40	MHz	see also specified limits for f_{VCO} and f_{REF} resulting in restrictions for possible N divider settings	P_3.1.7
Free-running frequency	$f_{VCOfree}$	–	34	–	MHz	–	P_3.1.24
Input clock high/low time	$t_{high/low}$	10	–	–	ns	–	P_3.1.8
Peak period jitter	t_{jp}	-500	–	500	ps	for K=2; this parameter value is only valid with the combination of an external quartz oscillator (e.g. 5 MHz)	P_3.1.9
Accumulated jitter with external oscillator	jacc_ext	–	–	5	ns	for K=2; this parameter value is only valid with the combination of an external quartz oscillator (e.g. 5 MHz).	P_3.1.10
Lock-in time	t_L	–	–	260	µs	this parameter represents the duration from module power-on to assertion of lock signal	P_3.1.11

1) The typical oscillator frequency is 40 MHz
2) Not subject to production test, specified by design.

28.3.2 External Clock Parameters XTAL1, XTAL2

Table 29 Functional Range

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range limits for signal on XTAL1	V_{IX1_SR}	-1.7 + V_{DDC}	–	1.7	V	[2)]	P_3.2.1
Input voltage (amplitude) on XTAL1	V_{AX1_SR}	0.3 x V_{DDC}	–	–	V	[3)] Peak-to-peak voltage	P_3.2.2
XTAL1 input current	I_{IL}	–	–	±20	µA	0 V < V_{IN} < V_{DDI}	P_3.2.3
Oscillator frequency	f_{OSC}	4	–	6	MHz	Clock signal	P_3.2.4

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Table 29 Functional Range (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Oscillator frequency	f_{OSC}	4	–	6	MHz	Crystal or Resonator	P_3.2.5
High time	t_{1_VCOBYP}	6	–	–	ns	4)5)	P_3.2.6
Low time	t_{2_VCOBYP}	6	–	–	ns	4)5)	P_3.2.7
Rise time	t_{3_VCOBYP}	–	8	8	ns	4)5)	P_3.2.8
Fall time	t_{4_VCOBYP}	–	8	8	ns	4)5)	P_3.2.9
High time	t_{1_PLLNM}	12	–	–	ns	5)6)	P_3.2.10
Low time	t_{2_PLLNM}	12	–	–	ns	5)6)	P_3.2.11
Rise time	t_{3_PLLNM}	–	7	7	ns	5)6)	P_3.2.12
Fall time	t_{4_PLLNM}	–	7	7	ns	5)6)	P_3.2.13

1) Not subject to production test, specified by design.
2) Overload conditions must not occur on pin XTAL1.
3) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.
4) this performance is only valid for Prescaler Mode (VCO Bypass mode).
5) tested with rectangular signal with $V_{IN_Low} = 0V$ to $V_{IN_High} = V_{DDC}$
6) this performance is only valid for PLL Normal Mode.

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28.4 Flash Parameters

This chapter includes the parameters for the 36 KByte embedded flash module.

28.4.1 Flash Characteristics

Table 30 Flash Characteristics[1)]

V_S = 5.5 V to 28 V,, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 Byte page	t_{PR}	–	3[2)]	3.5	ms	3V < V_S < 28V	P_4.1.1
Erase time per sector/page	t_{ER}	–	4[2)]	4.5	ms	3V < V_S < 28V	P_4.1.2
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles	P_4.1.3
Data retention time	t_{RET}	50	–	–	years	1,000 erase / program cycles T_j = 30°C[3)]	P_4.1.4
Flash erase endurance for user sectors	N_{ER}	30	–	–	kcycles	Data retention time 5 years	P_4.1.5
Flash erase endurance for security pages[4)]	N_{SEC}	10	–	–	cycles	Data retention time 20 years	P_4.1.6
Drain disturb limit	N_{DD}	32	–	–	kcycles	[5)]	P_4.1.7

1) Not subject for production test, specified by design.
2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. The requirement is only relevant for extremely low system frequencies.
3) Derived by extrapolation of lifetime tests.
4) Temperature: 25 °C
5) This parameter limits the number of subsequent programming operations within a physical sector without a given page in this sector being (re-)programmed. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated. For data sectors the integrated EEPROM emulation firmware routines handle this limit automatically, for wordline erases in code sectors (without EEPROM emulation) it is recommended to execute a software based refresh, which may make use of the integrated random number generator NVMBRNG to statistically start a refresh.

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28.5 Parallel Ports (GPIO)

28.5.1 Description of Keep and Force Current

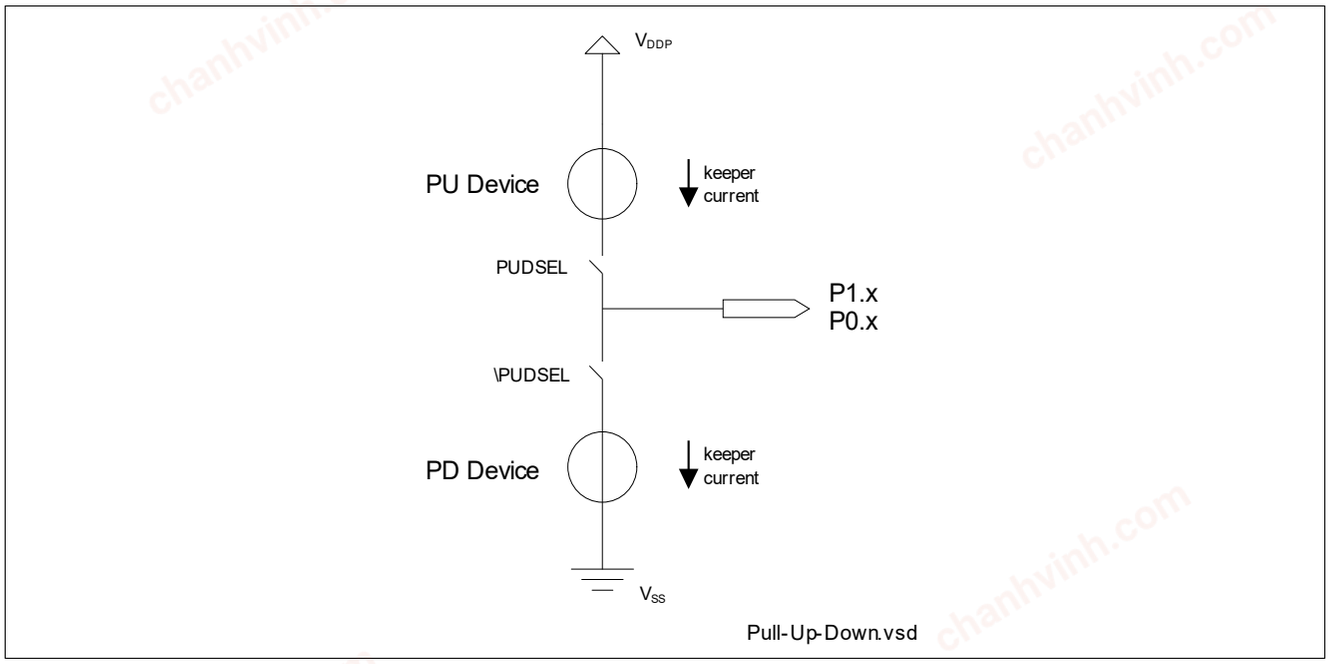


Figure 37 Pull-Up/Down Device

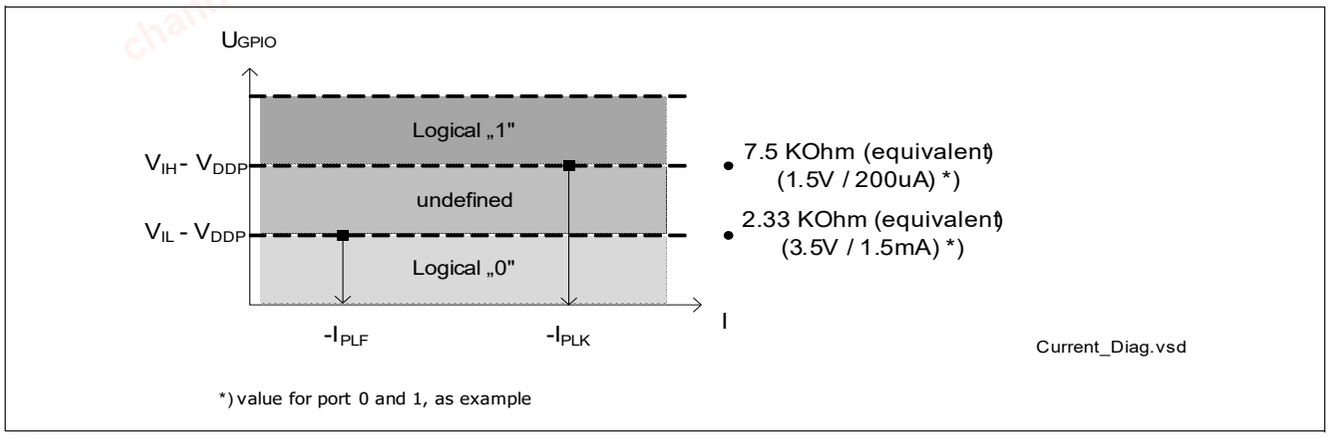


Figure 38 Pull-Up Keep and Forced Current

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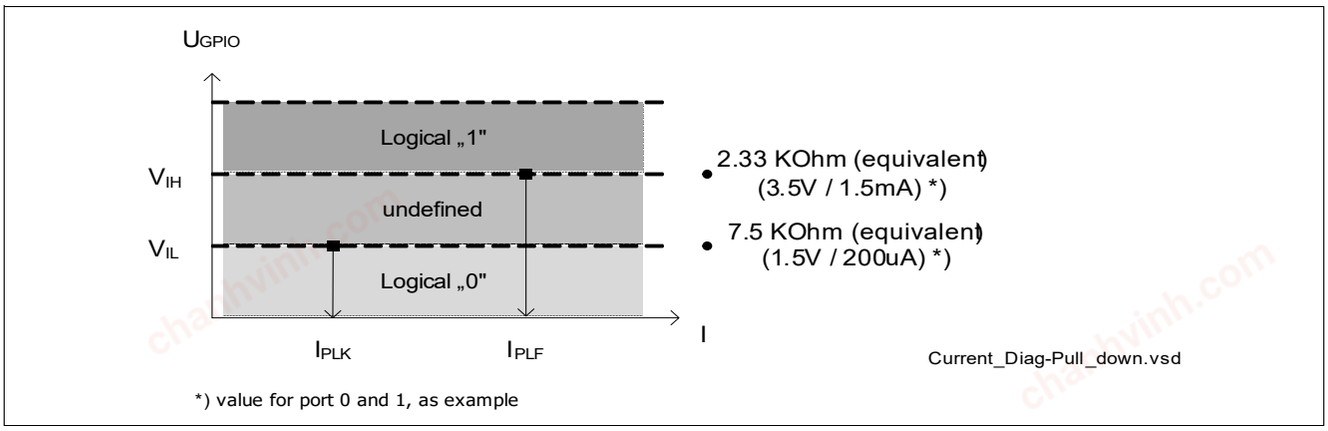


Figure 39 Pull-Down Keep and Force Current

28.5.2 DC Parameters Port 0, Port 1, TMS, Reset

Table 31 DC Characteristics Port0, Port1

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	1) 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.1
Input low voltage	V_{IL_extend}	-0.3	0.42 x V_{DDP}	–	V	2) 2.6V ≤ V_{DDP} < 4.5V	P_5.2.14
Input high voltage	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	1) 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.2
Input high voltage	V_{IH_extend}	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	2) 2.6V ≤ V_{DDP} < 4.5V	P_5.2.15
Input Hysteresis	HYS	0.11 x V_{DDP}	–	–	V	2) 4.5V ≤ V_{DDP} ≤ 5.5V; Series resistance = 0 Ω	P_5.2.3
Input Hysteresis	HYS_{extend}	–	0.09 x V_{DDP}	–	V	2) 2.6V ≤ V_{DDP} < 4.5V; Series resistance = 0 Ω	P_5.2.16
Output low voltage	V_{OL}	–	–	1.0	V	3) 4) I_{OL} ≤ I_{OLmax}	P_5.2.4
Output low voltage	V_{OL}	–	–	0.4	V	3) 5) I_{OL} ≤ I_{OLnom}	P_5.2.5
Output high voltage	V_{OH}	V_{DDP} - 1.0	–	–	V	3) 4) I_{OH} ≥ I_{OHmax}	P_5.2.6
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	3) 5) I_{OH} ≥ I_{OHnom}	P_5.2.7
Input leakage current	I_{OZ2}	-5	–	+5	µA	6) T_J ≤ 85°C, 0.45 V < V_{IN} < V_{DDP}	P_5.2.8

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Table 31 DC Characteristics Port0, Port1 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input leakage current	I_{OZ2}	-15	–	+15	µA	$T_J \le 150°C$, $0.45\ V < V_{IN} < V_{DDP}$	P_5.2.9
Pull level keep current[7]	I_{PLK}	–	–	±200	µA	[8] $V_{PIN} \ge V_{IH}$ (up) $V_{PIN} \le V_{IL}$ (dn)	P_5.2.10
Pull level force current[7]	I_{PLF}	±1.5	–	–	mA	[8] $V_{PIN} \ge V_{IL}$ (up) $V_{PIN} \le V_{IH}$ (dn)	P_5.2.11
Pin capacitance	C_{IO}	–	–	10	pF	[2]	P_5.2.12
Reset Pin Timing							
Reset Pin Input Filter Time	T_{filt_RESET}	–	5	–	µs	[9]	P_5.2.13

1) Tested at V_{DDP} = 5V, specified for 2.55V < V_{DDP} < 5.1V.
2) Not subject to production test, specified by design.
3) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.
4) Tested at 2.55V < V_{DDP} < 5.1V, I_{OL} = 4mA, I_{OH} = -4mA, specified for 2.7V < V_{DDP} < 5.1V.
5) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}→*GND*, V_{OH}→V_{DDP}). Tested at 2.55V < V_{DDP} < 5.1V, I_{OL} = 1mA, I_{OH} = -1mA.
6) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
$I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
$I_{OZ} = I_{OZtempmax}$ - (1.6 × DV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.
7) Negative current is representing pullup; positive current is representing pulldown
8) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \ge V_{IH}$ for a pull-up; $V_{PIN} \le V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \le V_{IL}$ for a pull-up; $V_{PIN} \ge V_{IH}$ for a pull-down.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
9) This filter time and its variation is derived from the time base $t_{LP_CLK} = 1 / f_{LP_CLK}$.

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

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Table 32 Current Limits for Port Output Drivers[1)]

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , - I_{OHmax})		Output Current (I_{OLnom} , - I_{OHnom})		Number
	VDDP ≥ 4.5V	2.55V<VDDP < 4.5V	VDDP ≥ 4.5V	2.55V<VDDP < 4.5V	
Strong Driver	5 mA	3 mA	1.6 mA	1.0 mA	P_5.2.20
Medium Driver	3 mA	1.8 mA	1.0 mA	0.8 mA	P_5.2.21
Weak Driver	0.5 mA	0.3 mA	0.25 mA	0.15 mA	P_5.2.22

1) Not subject to production test, specified by design.

28.5.3 DC Parameters Port 2

These parameters apply to the IO voltage range, 2.55 V ≤ V_{DDP} ≤ 5.5 V.

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 33 DC Characteristics Port 2

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL_P2}	-0.3	–	0.3 x V_{DDP}	V	1) 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.3.1
Input low voltage	$V_{IL_P2_extend}$	-0.3	0.42 x V_{DDP}	–	V	2) 2.6V ≤ V_{DDP} < 4.5V	P_5.3.8
Input high voltage	V_{IH_P2}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	1) 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.3.2
Input high voltage	$V_{IH_P2_extend}$	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	2) 2.6V ≤ V_{DDP} < 4.5V	P_5.3.9
Input Hysteresis	HYS_{P2}	0.11 x V_{DDP}	–	–	V	2) 4.5V ≤ V_{DDP} ≤ 5.5V; Series resistance = 0 Ω	P_5.3.3
Input Hysteresis	HYS_{P2_extend}	–	0.09 x V_{DDP}	–	V	2) 2.6V ≤ V_{DDP} < 4.5V; Series resistance = 0 Ω	P_5.3.10
Input leakage current	I_{OZ1_P2}	-400	–	+400	nA	4.5V ≤ V_{DDP} ≤ 5.5V T_J ≤ 85°C, 0 V < V_{IN} < V_{DDP}	P_5.3.4
Input leakage current (extended temperature range)	$I_{OZ1_P2_T_extend}$	-1	–	+1	uA	2.6V ≤ V_{DDP} < 4.5V T_J ≤ 150°C, 0 V < V_{IN} < V_{DDP}	P_5.3.11

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Table 33 DC Characteristics Port 2 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Pull level keep current[4]	I_{PLK_P2}	–	–	±30	µA	[3] $V_{PIN} \geq V_{IH}$ (up) $V_{PIN} \leq V_{IL}$ (dn)	P_5.3.5
Pull level force current[4]	I_{PLF_P2}	±750	–	–	µA	[3] $V_{PIN} \leq V_{IL}$ (up) $V_{PIN} \geq V_{IH}$ (dn)	P_5.3.6
Pin capacitance (digital inputs/outputs)	C_{IO_P2}	–	–	10	pF	[2]	P_5.3.7

1) Tested at V_{DDP} = 5V, specified for 4.9V < V_{DDP} < 5.1V.
2) Not subject to production test, specified by design.
3) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pull-up; $V_{PIN} \leq V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pull-up; $V_{PIN} \geq V_{IH}$ for a pull-down.
4) Negative current is representing pullup; positive current is representing pulldown

28.5.4 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the TLE9842QX. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Table 34 Operating Condition Parameters

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital core supply voltage	V_{DDC}	1.35	–	1.6	V	Full active mode	P_5.4.1
Digital supply voltage for IO pads	V_{DDP}	2.55	5.0	5.5	V	[1]	P_5.4.2
Digital ground voltage	V_{SS}	0	–	0	V	Reference voltage	P_5.4.3
Overload current	I_{OV}	- 5.0	–	5.0	mA	Per IO pin[2)3)]	P_5.4.4
Overload current	I_{OV}	- 2.0	–	5.0	mA	Per analog input pin[2)3)]	P_5.4.5
Overload positive current coupling factor for analog inputs[4]	K_{OVA}	–	1.0×10^{-6}	1.0×10^{-4}	–	$I_{OV} > 0$[3]	P_5.4.6
Overload negative current coupling factor for analog inputs	K_{OVA}	–	2.5×10^{-4}	1.5×10^{-3}	–	$I_{OV} < 0$[3]	P_5.4.7

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Table 34 Operating Condition Parameters (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overload positive current coupling factor for digital I/O pins	K_{OVD}	–	1.0 x 10^{-4}	5.0 x 10^{-3}	–	$I_{OV} > 0$ [3]	P_5.4.8
Overload negative current coupling factor for digital I/O pins	K_{OVD}	–	1.0 x 10^{-2}	3.0 x 10^{-2}	–	$I_{OV} < 0$ [3]	P_5.4.9
Absolute sum of overload currents	$\Sigma\lvert I_{OV}\rvert$	–	–	80	mA	[3]	P_5.4.10

1) Performance of pad drivers, A/D Converter, and Flash module depends on V_{DDP}.
If the external supply voltage V_{DDP} becomes lower than the specified operating range, a power reset must be generated. Otherwise, the core supply voltage V_{DDI} may rise above its specified operating range due to parasitic effects.
This power reset can be generated by the on-chip SWD. If the SWD is disabled the power reset must be generated by activating the $\overline{\text{PORST}}$ input

2) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application.
Overload conditions must not occur on pin XTAL1 (powered by V_{DDIM}).

3) Not subject to production test, specified by design.

4) An overload current (I_{OV}) through a pin injects an error current (I_{INJ}) into the adjacent pins. This error current adds to that pin's leakage current (I_{OZ}). The value of the error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is reversed from the polarity of the overload current that produces it.
The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

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28.6 LIN Transceiver

28.6.1 Electrical Characteristics

Table 35 Electrical Characteristics LIN Transceiver

V_s = 5.5V to 18V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bus Receiver Interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 x V_S	V	SAE J2602	P_6.1.1
Receiver dominant state	V_{BUSdom}	-27	–	0.4 × V_S	V	LIN Spec 2.2 (Par. 17)	P_6.1.2
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 x V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	P_6.1.3
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 × V_S	V	[1] LIN Spec 2.2 (Par. 18)	P_6.1.4
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	[2] LIN Spec 2.2 (Par. 19)	P_6.1.5
Receiver hysteresis	V_{HYS}	0.07 × V_S	0.12 × V_S	0.175 × V_S	V	[3] LIN Spec 2.2 (Par. 20)	P_6.1.6
Wake-up threshold voltage	$V_{BUS,wk}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_6.1.7
Dominant time for bus wake-up	$t_{WK,bus}$	30	–	150	µs	including analog and digital filter time. Digital filter time can be adjusted by PMU.CNF_WAKE_FILTER	P_6.1.8
Bus Transmitter Interface							
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level	P_6.1.9
Bus short circuit current	$I_{BUS,sc}$	40	100	150	mA	Current Limitation for driver dominant state driver on V_{BUS} = 18 V; LIN Spec 2.2 (Par. 12)	P_6.1.10
Leakage current	$I_{BUS_NO_GND}$	-1000	-450	0	µA	V_S = 0 V; V_{BUS} = -12 V; LIN Spec 2.2 (Par. 15)	P_6.1.11
Leakage current	$I_{BUS_NO_BAT}$	–	10	20	µA	V_S = 0 V; V_{BUS} = 18 V; LIN Spec 2.2 (Par. 16)	P_6.1.12
Leakage current	$I_{BUS_PAS_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN Spec 2.2 (Par. 13)	P_6.1.13

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Table 35 Electrical Characteristics LIN Transceiver (cont'd)

V_s = 5.5V to 18V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Leakage current	$I_{BUS_PAS_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; LIN Spec 2.2 (Par. 14)	P_6.1.14
Bus pull-up resistance	R_{BUS}	20	30	47	kΩ	Normal mode LIN Spec 2.2 (Par. 26), also present in Sleep mode	P_6.1.15
AC Characteristics - Transceiver Normal Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.16
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.17
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; LIN Spec 2.2 (Par. 32)	P_6.1.18
Duty cycle D1 Normal Slope Mode (for worst case at 20 kbit/s)	t_{duty1}	0.396	–	–		[4] duty cycle 1 $TH_{Rec}(max) = 0.744 \times V_S$; $TH_{Dom}(max) = 0.581 \times V_S$; t_{bit} = 50 µs; $D1 = t_{bus_rec(min)} / 2 \times t_{bit}$; LIN Spec 2.2 (Par. 27)	P_6.1.19
Duty cycle D2 Normal Slope Mode (for worst case at 20 kbit/s)	t_{duty2}	–	–	0.581		[4] duty cycle 2 $TH_{Rec}(min) = 0.422 \times V_S$; $TH_{Dom}(min) = 0.284 \times V_S$; t_{bit} = 50 µs; $D2 = t_{bus_rec(max)} / 2 \times t_{bit}$; LIN Spec 2.2 (Par. 28)	P_6.1.20
AC Characteristics - Transceiver Low Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.21
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.22
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; LIN Spec 2.2 (Par. 32)	P_6.1.23

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Table 35 Electrical Characteristics LIN Transceiver (cont'd)

V_S = 5.5V to 18V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D3 (for worst case at 10,4 kbit/s)	t_{duty1}	0.417	–	–		[4] duty cycle 3 $TH_{Rec}(max) = 0.778 \times V_S$; $TH_{Dom}(max) = 0.616 \times V_S$; $t_{bit} = 96\ \mu s$; $D3 = t_{bus_rec(min)} / 2 \times t_{bit}$; LIN Spec 2.2 (Par. 29)	P_6.1.24
Duty cycle D4 (for worst case at 10,4 kbit/s)	t_{duty2}	–	–	0.590		[4] duty cycle 4 $TH_{Rec}(min) = 0.389 \times V_S$; $TH_{Dom}(min) = 0.251 \times V_S$; $t_{bit} = 96\ \mu s$; $D4 = t_{bus_rec(max)} / 2 \times t_{bit}$; LIN Spec 2.2 (Par. 30)	P_6.1.25
AC Characteristics - Transceiver Fast Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	–	P_6.1.26
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	–	P_6.1.27
Receiver delay symmetry-extended supply voltage range	$t_{sym,R}$	-2.0	–	2.0	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$;	P_6.1.42
Duty cycle D5 (used for 62,5 kbit/s)	t_{duty1}	0.395	–	–		[4] duty cycle 5 $TH_{Rec}(max) = 0.744 \times V_S$; $TH_{Dom}(max) = 0.581 \times V_S$; $t_{bit} = 16\mu s$; $D5 = t_{bus_rec(min)} / 2 \times t_{bit}$;	P_6.1.29
Duty cycle D6 (used for 62,5 kbit/s)	t_{duty2}	–	–	0.581		[4] duty cycle 6 $TH_{Rec}(min) = 0.422 \times V_S$; $TH_{Dom}(min) = 0.284 \times V_S$; $t_{bit} = 16\ \mu s$; $D6 = t_{bus_rec(max)} / 2 \times t_{bit}$;	P_6.1.30
AC Characteristics - Flash Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	0.5	6	µs	–	P_6.1.31
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	0.5	6	µs	–	P_6.1.32
Receiver delay symmetry	$t_{sym,R}$	-1.0	–	2.0	µs	$t_{sym,R} = t_{d(L),R} - t_{d(\wedge H),R}$;	P_6.1.44

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Table 35 Electrical Characteristics LIN Transceiver (cont'd)

V_s = 5.5V to 18V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D7 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry (used for 250 kbit/s programming)	t_{duty1}	0.395	–	–		5)duty cycle D7 $TH_{Rec}(max) = 0.744 \times V_S$; $TH_{Dom}(max) = 0.581 \times V_S$; $t_{bit} = 8.7$ µs; D7 = $t_{bus_rec(min)} / 2 \times t_{bit}$;	P_6.1.34
Duty cycle D8 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry (used for 250 kbit/s programming)	t_{duty2}	–	–	0.578		5)duty cycle D8 $TH_{Rec}(min) = 0.422 \times V_S$; $TH_{Dom}(min) = 0.284 \times V_S$; $t_{bit} = 8.7$ µs; D8 = $t_{bus_rec(max)} / 2 \times t_{bit}$;	P_6.1.35
LIN input capacity	C_{LIN_IN}	–	15	30	pF	6)	P_6.1.36
TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V	P_6.1.37
Thermal Shutdown (Junction Temperature)							
Thermal shutdown temp.	T_{jSD}	160	180	200	°C	6)	P_6.1.38
Thermal shutdown hyst.	ΔT	–	10	–	K	6)	P_6.1.39

1) Maximum limit specified by design.
2) $V_{BUS_CNT} = (V_{th_dom} + V_{th\ rec})/2$
3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$
4) Bus load concerning LIN Spec 2.2:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
5) Bus load
   Load 1 = 1 nF / 500 Ω = C_{BUS} / R_{BUS}
6) Not subject to production test, specified by design.

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28.7 High-Speed Synchronous Serial Interface

28.7.1 SSC Timing

The table below provides the SSC timing in the TLE9842QX.

Table 36 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	1) 2 * T_{SSC}	–	–		2) V_{DDP} > 2.7 V	P_7.1.1
MTSR delay from SCLK	t_1	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.2
MRST setup to SCLK	t_2	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.3
MRST hold from SCLK	t_3	15	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.4

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. If f_{CPU} = 20 MHz, t_0 = 100 ns. T_{CPU} is the CPU clock period.
2) Not subject to production test, specified by design.

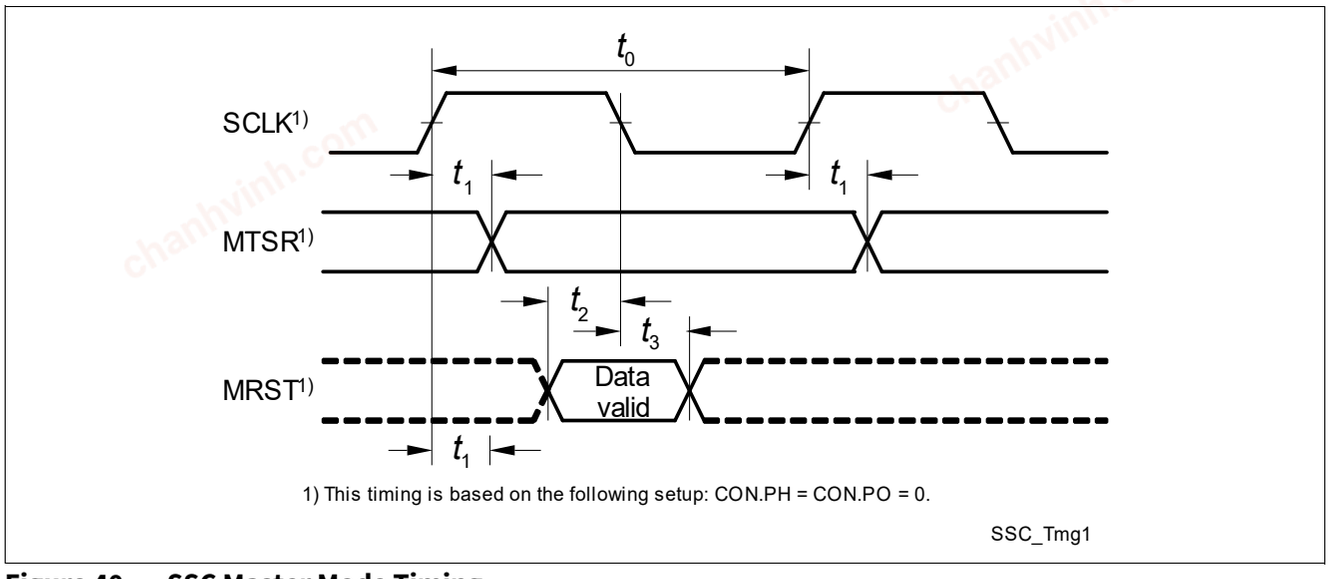


Figure 40 SSC Master Mode Timing

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28.8 Measurement Unit

28.8.1 Electrical Characteristics

Table 37 Supply Voltage Signal Conditioning

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ADC1 - Battery / Supply Voltage Measurement V_{BAT_SENSE} / V_S							
Input to output voltage attenuation: V_{BAT_SENSE} / V_S	ATT_{VBAT_SENSE} , ATT_{VS}	–	0.047	–		–	P_8.1.10
Nominal operating input voltage range V_{BAT_SENSE} / V_S	$V_{BAT_SENSE,range}$, $V_{S,range}$	0	–	25.77	V	2) Max. value corresponds to typ. ADC full scale input;	P_8.1.11
Accuracy of V_{BAT_SENSE} / V_S after calibration - with IIR filter	$\Delta V_{BAT_SENSE_IIR}$, V_{S_IIR}	-200	–	200	mV	V_s= 5.5V to 18V, T_j = -40..125°C, f_{ADCI} = f_{sys_max} ADC1_FILTCOEFF0_11.CHx = 11’b.	P_8.1.12
Accuracy of V_{BAT_SENSE} / V_S after calibration	ΔV_{BAT_SENSE}, V_S	-300	–	300	mV	V_s= 5.5V to 18V, T_j = -40..125°C, f_{ADCI} = f_{sys_max}.	P_8.1.36
ADC1 - Monitoring Input Voltage Measurement V_{MONx}							
Input to output voltage attenuation: VMONx	ATT_{VMONx}	–	0.039	–		–	P_8.1.13
Nominal operating input voltage range VMONx	$V_{MONx,range}$	0	–	31.05	V	2) Max. value corresponds to typ. ADC full scale input;	P_8.1.14
Accuracy of V_{MONx} sense after calibration - with IIR filter	ΔV_{MONx_IIR}	-241	–	241	mV	V_s= 5.5V to 18V, T_j = -40..125°C, f_{ADCI} = f_{sys_max} ADC1_FILTCOEFF0_11.CHx = 11’b.	P_8.1.33
Accuracy of V_{MONx} sense after calibration - Reduced Operating Range - with IIR filter	$\Delta V_{MONx_ROR_IIR}$	-170	–	170	mV	2) V_s= 5.5V to 18V, T_j = -40..125°C, $V_{MONx,range}$= 0V to 12V, f_{ADCI} = f_{sys_max}, ADC1_FILTCOEFF0_11.CHx = 11’b.	P_8.1.20

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Table 37 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Accuracy of V_{MONx} sense after calibration	ΔV_{MONx}	-361	–	361	mV	2) V_s= 5.5V to 18V, T_j = -40..125°C, $f_{ADCI} = f_{sys_max}$.	P_8.1.37
ADC1 - Port 2.x Voltage Measurement $V_{2.x}$							
Input to output voltage attenuation: VPort2.x	$ATT_{2.x}$	–	0.219	–		–	P_8.1.15
Nominal operating input voltage range VPort2.x	$V_{Port2.x,range}$	0	–	5.53 1)	V	2) Max. value corresponds to typ. ADC full scale input;	P_8.1.16
Accuracy of $V_{Port2.x}$ sense after calibration - with IIR filter	$\Delta V_{Port2.x_IIR}$	-43	–	43	mV	V_s= 5.5V to 18V, T_j = -40..125°C, $f_{ADCI} = f_{sys_max}$ ADC1_FILTCOEFF0_11.CHx = 11'b.	P_8.1.34
Accuracy of $V_{Port2.x}$ sense after calibration	$\Delta V_{Port2.x}$	-67	–	67	mV	V_s= 5.5V to 18V, T_j = -40..125°C, $f_{ADCI} = f_{sys_max}$.	P_8.1.38
ADC2 - Supply Voltage Measurement V_S							
Input to output voltage attenuation: V_S	ATT_{VS_ADC2}	–	0.039	–		–	P_8.1.1
Nominal operating input voltage range V_S	$V_{S,ADC2}$	3	–	31.05	V	2) Max. value corresponds to typ. ADC full scale input; 3V < V_S < 28V	P_8.1.2
Accuracy of V_S after calibration	$\Delta V_{S,ADC2}$	-270	–	270	mV	V_s= 5.5V to 18V, T_j = -40..125°C	P_8.1.3
ADC2 - VDDEXT Voltage Measurement V_{DDEXT}							
Input to output voltage attenuation: VDDEXT	ATT_{VDDEXT}	–	0.203	–		–	P_8.1.17
Nominal operating input voltage range VDDEXT	$V_{DDEXT,range}$	0	–	5.96	V	2) Max. value corresponds to typ. ADC full scale input;	P_8.1.18
ADC2 - Pad Supply Voltage Measurement V_{VDDP}							
Input-to-output voltage attenuation: VDDP	ATT_{VDDP}	–	0.203	–		–	P_8.1.4

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Table 37 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating input voltage range VDDP	$V_{DDP,range}$	0	–	5.96	V	2) Max. value corresponds to typ. ADC full scale input;	P_8.1.5
ADC2 - Reference Voltage Measurement V_{BG}							
Input-to-output voltage attenuation: VBG	ATT_{VBG}	–	0.75	–		–	P_8.1.6
Nominal operating input voltage range VBG	$V_{BG,range}$	0.8	–	VDDC - 0.1V	V	2) Max. value corresponds to typ. ADC full scale input;	P_8.1.7
Value of ADC2-V_{BG} measurement after calibration	V_{BG_PMU}	0.90	1.0	1.1	V	–	P_8.1.39
ADC2 - Core supply Voltage Measurement V_{DDC}							
Input-to-output voltage attenuation: VDDC	ATT_{VDDC}	–	0.75	–		–	P_8.1.8
Nominal operating input voltage range VDDC	$V_{DDC,range}$	0.6	–	VDDC + 0.1V	V	2) Max. value corresponds to typ. ADC full scale input;	P_8.1.9

1) This typical theoretical full scale is not reached as the internal ESD Clamping Structure limits the voltage to max. 5.2V.
2) Not subject to production test, specified by design.

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28.8.2 Central Temperature Sensor Module

28.8.2.1 Electrical Characteristics

Table 38 Electrical Characteristics Temperature Sensor Module

V_S = 5.5 V to 28 V, , T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage V_{TEMP} at T_0=0°C (273 K)[2]	a	–	0.628	–	V	T_0=0°C (273 K)	P_8.2.1
Temperature sensitivity b [2]	b	–	2.31	–	mV/K		P_8.2.2
Accuracy_1	Acc_1	-10	–	10	°C	[1] -40°C < T_j < 85°C	P_8.2.3
Accuracy_2	Acc_2	-15	–	15	°C	125°C < T_j < 175°C	P_8.2.4
Accuracy_3	Acc_3	-5	–	5	°C	[2] 85°C < T_j < 125°C	P_8.2.5

1) Accuracy with reference to on-chip temperature calibration measurement.
2) Not subject to production test, specified by design.

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28.9 ADC1 (10-Bit)

28.9.1 ADC1 Reference Voltage

Table 39 DC Specifications

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reference Voltage	V_{BG}	-1%	1.211	+1%	V	–	P_9.1.10
Temperature Drift	ΔV_{BG}	-1%		+1%	V	–	P_9.1.11

28.9.2 Electrical Characteristics ADC1 (10-Bit)

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 40 A/D Converter Characteristics

V_S = 5.5 V to 28 V, , T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Analog clock frequency	f_{ADCI}	5	–	40	MHz	1)	P_9.2.1
DNL error	EA_{DNL}	–	–	± 2	LSB	2)	P_9.2.8
INL error	EA_{INL}	–	–	± 3	LSB	–	P_9.2.9
Gain error	EA_{GAIN}	–	–	± 1.2	% of FSR 3)	4)calibrated; Gain Error is calibrated by implemented calibration unit	P_9.2.10
Offset error	EA_{OFF}	–	–	± 2.5	LSB	4)calibrated; Offset Error is calibrated by implemented calibration unit	P_9.2.11
Total unadjusted error	EA_{TUE}	–	–	± 10	LSB	already calibrated	P_9.2.33

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Table 40 A/D Converter Characteristics (cont'd)

V_S = 5.5 V to 28 V, , T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input referred noise	V_{Noise_LSB}	–	–	1.5	LSB rms	4) T_j = 25°C; this value is determined out of 4 consecutive measurements which are averaged.	P_9.2.34
Cross-coupling Attenuation between LV Channels	EA_{CCOUP}	–	±1	± 2	LSB	4) –	P_9.2.12
Input capacitance of a HV analog input	C_{AINT_HVI}	–	–	200	fF	4)	P_9.2.13
Input capacitance of a LV analog input	C_{AINT_LVI}	–	–	200	fF	4)	P_9.2.19

1) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.
2) this parameter is measured with disabled hardware calibration
3) this Gain error is calibrated by IFX end of line
4) Not subject to production test

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28.10 High-Voltage Monitoring Input

28.10.1 Electrical Characteristics

Table 41 Electrical Characteristics Monitoring Input

V_S = 5.5 V to 28 V; T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
MON Input Pin characteristics							
Wake-up/monitoring threshold voltage	V_{MONth}	0.4*V_s	0.5*V_s	0.6*V_s	V	without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s);	P_10.1.1
Threshold hysteresis	$V_{MONth,hys}$	0.015* V_s	0.06*V_s	0.10*V_s	V	in all modes; without external serial resistor R_s (with R_s:dV = $I_{PD/PU}$ * R_s); 5.5 V < V_S < 18 V	P_10.1.2
Threshold hysteresis-extended supply voltage range	$V_{MONth,hys_VS_extended}$	0.02*V_s	0.06*V_s	0.12*V_s	V	in all modes; without external serial resistor R_s (with R_s:dV = $I_{PD/PU}$ * R_s); 18 V < V_S < 28 V	P_10.1.7
Pull-up current	$I_{PU, MON}$	-20	-10	-5	µA	0.6*V_s;	P_10.1.3
Pull-down current	$I_{PD, MON}$	5	10	20	µA	0.4*V_s;	P_10.1.4
Input leakage current	$I_{LK,MON}$	-2	–	2	µA	0 V < V_{MON_IN} < 28 V	P_10.1.5
Timing							
Wake-up filter time	$t_{FT,MON}$	-	20	-	µs	1)	P_10.1.6

1) With pull-up, pull down current disabled.

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28.11 High Side Switches

28.11.1 Electrical Characteristics

Table 42 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWM frequency of HS with Slew Rate Control	$f_{PWM_W_SR}$	0	–	10	kHz	1) Frequency must be configured in the PWM Generator	P_11.1.1
PWM frequency of HS without Slew Rate Control	f_{PWM_W/O_SR}	0	–	25 2)	kHz	1) Frequency must be configured in the PWM Generator	P_11.1.2
Output HS							
ON-State Resistance	R_{ON}	2	10	18	Ω	5.5 V < V_S < 28V, Ids=100mA, T_j = 25 °C	P_11.1.3
Output leakage Current	$I_{leakage}$	–	–	2	µA	Output OFF 0 V < V_{XLO} < V_S; T_j ≤ 150 °C	P_11.1.4
Output Slew Rate (rising) with slow Slew Rate setting (Slew Rate 1)	SR_{raise_SR1}	1	–	10	V/µs	20% to 80% of V_S V_S = 9 to 18V R_L =300Ω 1)	P_11.1.5
Output Slew Rate (falling) with slow Slew Rate setting (Slew Rate 1)	SR_{fall_SR1}	-10	–	-1	V/µs	80% to 20% of V_S V_S = 9 to 18V R_L =300Ω 1)	P_11.1.6
Output Slew Rate (rising) with fast Slew Rate setting (Slew Rate 2)	SR_{raise_SR2}	18.0	–	55.0	V/µs	20% to 80% of V_S V_S = 9 to 18V R_L =300Ω 1)	P_11.1.7
Output Slew Rate (falling) with fast Slew Rate setting (Slew Rate 2)	SR_{fall_SR2}	-43.4	–	-12.5	V/µs	80% to 20% of V_S V_S = 9 to 18V R_L =300Ω 1)	P_11.1.8
Turn ON Delay time (Slew Rate 1)	$t_{IN\text{-}HS_SR1}$	–	–	4.5	µs	ON = 1 to 20% of V_S R_L =300Ω	P_11.1.9
Turn ON time (Slew Rate 1)	t_{ON_SR1}	1	–	15	µs	V_S = 9 to 18V HS_ON=1 to 80% of V_S R_L =300Ω T_j =25°C	P_11.1.10

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Table 42 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Turn OFF time (Slew Rate 1)	t_{OFF_SR1}	1	–	15	µs	V_S = 9 to 18V HS_ON= 0 to 20% of V_S R_L =300Ω; T_j =25°C	P_11.1.11
Turn ON Delay time (Slew Rate 2)	$t_{IN\text{-}HS_SR2}$	–	–	1	µs	ON = 1 to 20% of V_S R_L =300Ω	P_11.1.55
Turn ON time (Slew Rate 2)	t_{ON_SR2}	–	–	3	µs	V_S = 9 to 18V HS_ON=1 to 80% of V_S R_L =300Ω T_j =25°C	P_11.1.56
Turn OFF time (Slew Rate 2)	t_{OFF_SR2}	–	–	3	µs	V_S = 9 to 18V HS_ON= 0 to 20% of V_S R_L =300Ω; T_j =25°C	P_11.1.57
Over-current detection							
Overcurrent threshold 0	I_{octh0}	26	42	60	mA	V_S = 13.5V HSx_OC_SEL =00	P_11.1.12
Overcurrent threshold 0 hysteresis	$I_{octh0,hyst}$	–	14	–	mA	[1] HSx_OC_SEL =00	P_11.1.13
Overcurrent threshold 1	I_{octh1}	51	60	80	mA	V_S = 13.5V HSx_OC_SEL =01	P_11.1.14
Overcurrent threshold 1 hysteresis	$I_{octh1,hyst}$	–	17	–	mA	[1] HSx_OC_SEL =01	P_11.1.15
Overcurrent threshold 2	I_{octh2}	101	123	150	mA	V_S = 13.5V HSx_OC_SEL =10	P_11.1.16
Overcurrent threshold 2 hysteresis	$I_{octh2,hyst}$	–	25	–	mA	[1] HSx_OC_SEL =10	P_11.1.17
Overcurrent threshold 3	I_{octh3}	151	176	210	mA	V_S = 13.5V HSx_OC_SEL =11	P_11.1.18
Overcurrent threshold 3 hysteresis	$I_{octh3,hyst}$	–	30	–	mA	[1] HSx_OC_SEL =11	P_11.1.19
Over-current shutdown response time	t_{ocft}	8	–	80	µs	[1] V_S = 13.5V, R_L =100Ω, HS_ON to OC_SD (including switch-on time)	P_11.1.20
ON-state open load detection							
Open load threshold	I_{OLONth}	0.46	1.32	2.2	mA	–	P_11.1.21
Hysteresis	$I_{OLONhys}$	35	155	300	µA	–	P_11.1.22

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Table 42 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Cyclic sense mode							
Current capability	$I_{HS\ max\ sleep_pd}$	40	–	–	mA	Sleep Mode / Stop Mode	P_11.1.23
ON-State Resistance	$R_{ON,static}$	–	–	40	Ω	Ids = 40mA,	P_11.1.24
Output Slew Rate (rising)	SR_{rise_cyc}	1	–	–	V/µs	20% to 80% of V_S V_S = 9 to 18V R_L =300Ω	P_11.1.25
Output Slew Rate (falling)	SR_{fal_cycl}	–	–	-1	V/µs	80% to 20% of V_S V_S = 9 to 18V R_L =300Ω	P_11.1.26
Delay Time CYCLIC_ON-HS	t_{IN_cyc}	–	–	2	µs	ON =1 to 20% of V_S RL=300Ω	P_11.1.27
Turn-ON time	t_{ON_cyc}	–	–	15	µs	V_S = 9 to 18V ON=1 to 80% R_L =300Ω	P_11.1.28
Turn-OFF time	t_{OFF_cyc}	–	–	15	µs	V_S = 9 to 18V ON=0 to 20% of V_S R_L =300Ω; T_j=25°C	P_11.1.29

1) Not subject to production test, specified by design.
2) this is an additional requirement which refers to a 47Ohm series resistor to charge an external power mos gate.

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28.12 Low Side Switches

28.12.1 Electrical Characteristics

Table 43 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWM Frequency of LS	f_{PWM}	–	–	25	kHz	1) R_L =270Ω	P_12.1.1
Overcurrent Limitation	I_{LSTyp}	270	300	330	mA		P_12.1.2
ON-State Resistance	R_{ON}	1	4	10	Ω	I_{ds} =100mA;	P_12.1.3
Leakage Current	$I_{leakage}$	–	–	2	µA	0 V < V_{LS} < V_S; T_j < 85°C	P_12.1.5
Turn ON Delay time, slow mode	t_{dOn-LS}	–	–	50	µs	2) LS_ON=1 to 0.9*Vs V_S=13.5V, R_L =270Ω	P_12.1.6
Turn ON Delay time, PWM mode	$t_{dOn,f-LS}$	–	–	0.5	µs	LS_ON=1 to 0.9*Vs V_S=13.5V, R_L =270Ω	P_12.1.7
Turn ON fall time, PWM mode	$t_{ONF,PWM}$	–	1	1.25	µs	V_{LS} 0.9*Vs to 0.1*Vs V_S=13.5V, R_L =270Ω	P_12.1.8
Turn ON fall time, slow mode	$t_{ONF,Slow}$	–	100	150	µs	2) V_{LS} 0.9*Vs to 0.1*Vs V_S=13.5V, R_L =270Ω	P_12.1.9
Turn OFF Delay time, slow mode	$t_{dOff-LS}$	–	–	50	µs	2) LS_ON=0 to 0.1*Vs V_S=13.5V, R_L =270Ω	P_12.1.10
Turn OFF Delay time, PWM mode	$t_{dOff,f-LS}$	–	–	2	µs	LS_ON=0 to 0.1*Vs V_S=13.5V, R_L =270Ω	P_12.1.11
Turn OFF Rise time, PWM mode	$t_{OFFR,PWM}$	–	1	1.25	µs	V_{LS} 0.1*Vs to 0.9*Vs; V_S=13.5V, R_L =270Ω	P_12.1.12
Turn OFF Rise time, slow mode	$t_{OFFR,Slow}$	–	100	150	µs	2) V_{LS} 0.1*Vs to 0.9*Vs; V_S=13.5V, R_L =270Ω	P_12.1.13
Minimum Duty Cycle Pulse Width variation	ton_{MIN}	1.5	2	3.5	µs	ton(dig) = 2µs1)	P_12.1.14
Typical (systematic) Pulse Width increase LS_ON to VLS	$d\,ton_{TYP}$	–	1.25	–	µs	ton(dig) = 2µs1)	P_12.1.15
Zener Clamp Voltage	V_{AZ}	–	50	–	V	values are valid at T_j = 25°C	P_12.1.16
Clamping Energy (repetitive)	E_{clamp}	–	–	2	mJ	1)3) 1.000.000 cycles, @ I_{max} = 90mA	P_12.1.17

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Table 43 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Clamping Energy	E_{clamp}	–	–	14	mJ	[1)3)] *10 cycles, Tstart* = 25°C, @ I_{max} = 230mA	P_12.1.18
Clamping Energy (single), hot	E_{clamp}	–	–	7	mJ	[1)3)] 10 cycles, *Tstart* = 85°C, @ I_{max} = 230mA	P_12.1.19

1) Not subject to production test, specified by design.
2) Static ON mode (no PWM)
3) valid for one low-side, not for both at the same time

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29 Package Outlines

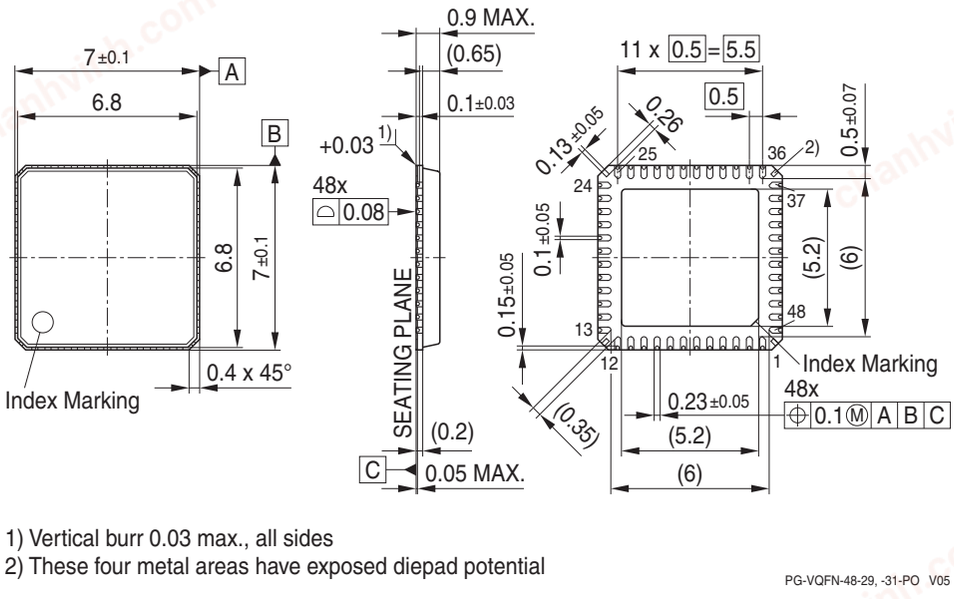


Figure 41 Package outline VQFN-48-31 (with LTI)

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.*
2. *Dimensions in mm.*

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30 Abbreviations

The following acronyms and terms are used within this document. List see in **Table 44**.

Table 44 Acronyms

Acronyms	Name
AHB	Arm® Advanced High-Performance Bus
CCU6	Capture Compare Unit 6
CGU	Clock Generation Unit
CLKMU	Clock Management Unit
CMU	Cyclic Management Unit
DPP	Data Post Processing
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input Output
HV	High Voltage
ICU	Interrupt Control Unit
LDO	Low DropOut voltage regulator
LIN	Local Interconnect Network
LSB	Least Significant Bit
LTI	Lead Tip Inspection
LV	Low Voltage
MCU	Microcontroller Unit
MF	Measurement Functions
MPU	Memory Protection Unit
MRST	Master Receive / Slave Transmit, corresponds to MISO in SPI
MSB	Most Significant Bit
MTSR	Master Transmit / Slave Receive, corresponds to MOSI in SPI
MU	Measurement Unit
NMI	Non Maskable Interrupt
NVIC	Nested Vector Interrupt Controller
OSC	Oscillator
OTP	One Time Programmable
PBA	Peripheral Bridge
PC	Program Counter
PCU	Power Control Unit
PD	Pull Down
PGU	Power supply Generation Unit
PLL	Phase Locked Loop
PMU	Power Management Unit
PPB	Private Peripheral Bus

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Abbreviations

Table 44 Acronyms (cont'd)

Acronyms	Name
PSW	Program Status Word
PU	Pull Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RCU	Reset Control Unit
rfu	reserved for future use
RMU	Reset Management Unit
ROM	Read Only Memory
SCU	System Control Unit
SOW	Short Open Window (for WDT1)
SPI	Serial Peripheral Interface
SSC	Synchronous Serial Channel
SWD	Arm® Serial Wire Debug
TCCR	Temperature Compensation Control Register
TMS	Test Mode Select
TSD	Thermal Shut Down
UART	Universal Asynchronous Receiver Transmitter
VBG	Voltage reference Band Gap
VCO	Voltage Controlled Oscillator
WDT1	Watchdog timer in SCU-PM (System Control Unit - Power Modules)
WMU	Wake-up Management Unit
100TP	100 Times Programmable

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31 Revision History

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Rev. 1.1, 2022-05-11	
	• **Table 1**: For VDDC changed value 0.9 V to reduced voltage Editorial changes: • Updated Arm® trademarks • **Figure 9**: Changed “PMU_RST_STS” to “PMU_RESET_STS” • **Chapter 11**: Added system address range “58004000H - 58007FFFH” • **Table 5**: Removed “wakeup” at nodes 12 and 22 • **Table 10**: Changed table title from “Port Registers” to “Timer2 and Timer21 Modes” • Moved the “Abbreviations” to the end of the datasheet • P_1.1.10: Removed footnote
Rev. 1.0, 2016-03-17	
	Initial revision

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