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# TLE9562QX

## DC Motor System IC



## 1 Overview

### Features

- Low-drop voltage regulator 5 V, 250 mA for main supply
- Four half-bridge gate drivers for external N-channel MOSFETs
- Adaptive MOSFET gate control:
  - Regulation of the MOSFET switching time
  - Reduced switching losses in PWM mode
  - High efficient constant gate charge
- Control of reverse battery protection MOSFET
- High-speed CAN transceiver supporting CAN FD communication up to 5 Mbit/s according to ISO11898-2:2016
- LIN Transceivers LIN2.2/SAE J2602 with programmable TXD time-out feature and LIN flash mode
- Fail Outputs for fail-safe signalization
- Configurable wake-up sources
- Four high-side outputs 7 Ω typ.
- Two PWM inputs
  - High-side and low-side PWM capable
  - Active free-wheeling
  - Up to 25 kHz PWM frequency
- 32 bit serial peripheral interface (SPI) with cyclic redundancy check (CRC)
- Very low quiescent current consumption in Stop Mode and Sleep Mode
- Periodic cyclic sense and cyclic wake in Normal Mode, Stop Mode and Sleep Mode
- Reset and interrupt output
- Drain-source monitoring and open-load detection
- Configurable time-out and window watchdog
- Overtemperature and short circuit protection features
- Leadless power package with support of optical lead tip inspection
- Green Product (RoHS compliant)

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Overview

## Potential applications

- Door module
- Power lift gate
- Power sliding doors
- Seat control module
- Seatbelt pretension
- Steering column lock
- Sunroof module

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

## Description

The TLE9562QX is a multifunctional system IC with integrated power supply, communication interfaces, multiple half-bridges and support features in an exposed pad PG-VQFN-48 power package. The device is designed for various motor control automotive applications.

To support these applications, the DC Motor System IC provides the main functions, such as a 5 V low-dropout voltage regulator one HS-CAN transceiver supporting CAN FD, one LIN transceiver, four half-bridges for DC motor control, and one 32 bit serial peripheral interface (SPI).

The device includes diagnostic and supervision features, such as drain-source monitoring and open-load detection, short circuit protection, configurable time-out and window watchdog, fail-safe output, as well as overtemperature protection.

| Type | Package | Marking |
|---|---|---|
| TLE9562QX | PG-VQFN-48 | TLE9562QX |

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# 2 Block Diagram

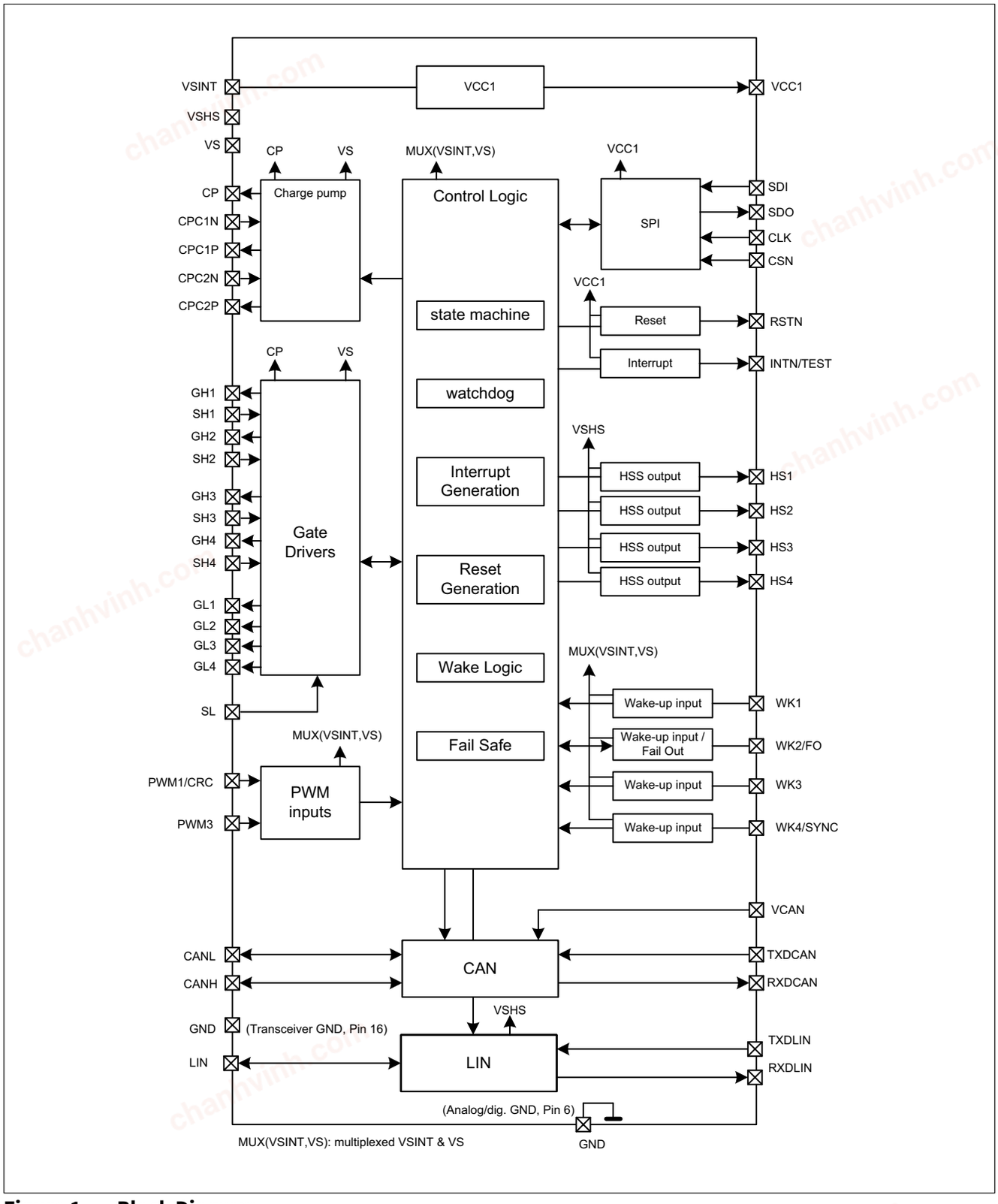



**Figure 1 Block Diagram**

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# 3 Pin Configuration

## 3.1 Pin Assignment

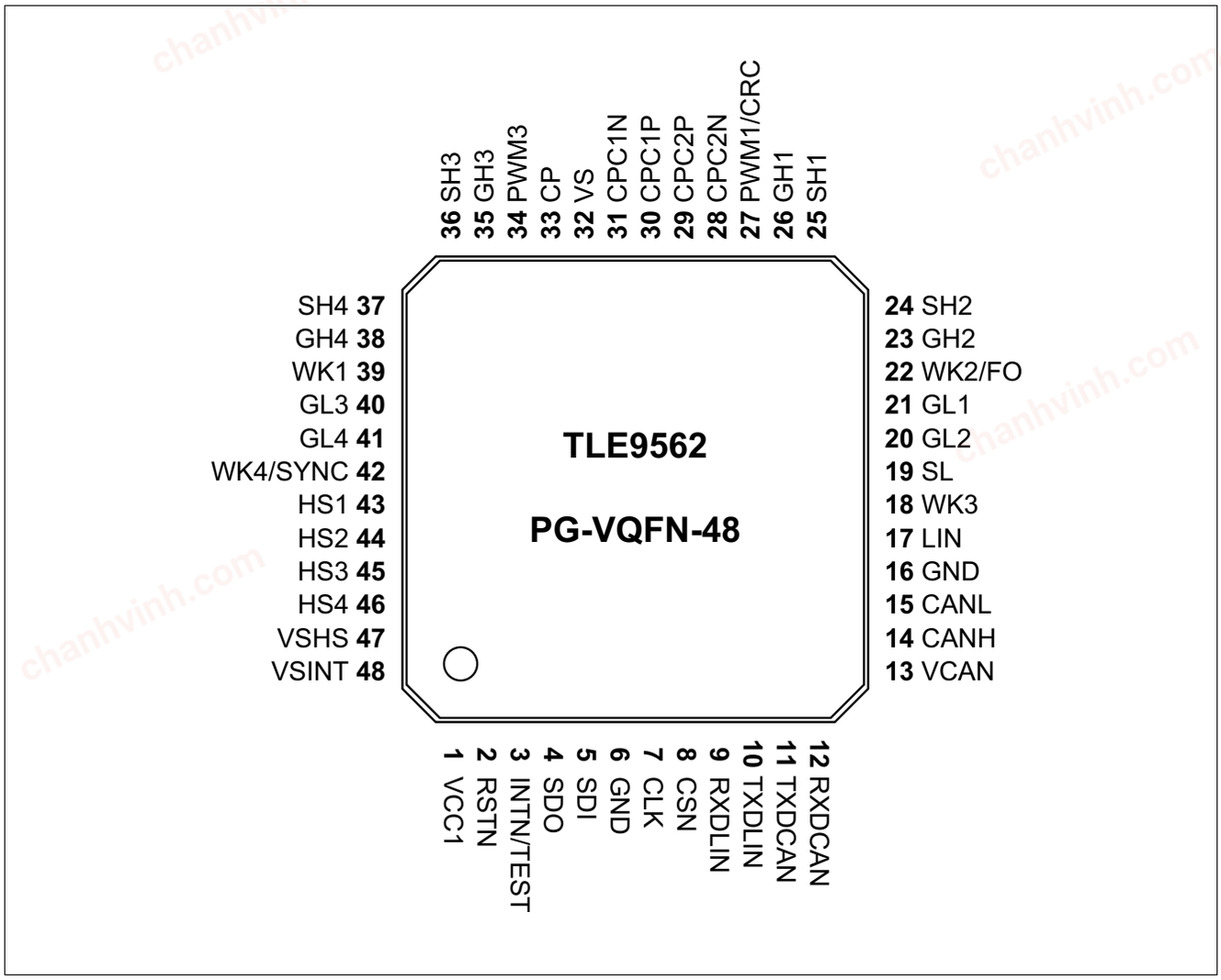



**Figure 2 Pin Configuration**

## 3.2 Pin Definitions and Functions

| Pin | Symbol | Function |
|---|---|---|
| 1 | VCC1 | **Voltage Regulator.** Output voltage 1 |
| 2 | RSTN | **Reset Output.** Active LOW, internally passive pull-up with open-drain output |
| 3 | INTN/TEST | **Interrupt Output.** Active LOW output, push-pull structure<br>**TEST.** Connect to GND (via pull-down) to activate Software Development Mode |
| 4 | SDO | **SPI Data Output to Microcontroller** (=MISO). Push-pull structure |
| 5 | SDI | **SPI Data Input from Microcontroller** (=MOSI). Internal pull-down |
| 6 | GND | **Ground.** Analog/digital ground |
| 7 | CLK | **SPI Clock Input.** Internal passive pull-down |

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## Pin Configuration

| Pin | Symbol | Function |
|---|---|---|
| 8 | CSN | **SPI Chip Select Not input.** Internal passive pull-up |
| 9 | RXDLIN | **Receive LIN.** Push-pull structure |
| 10 | TXDLIN | **Transmit LIN.** Internal passive pull-up |
| 11 | TXDCAN | **Transmit CAN.** Internal passive pull-up |
| 12 | RXDCAN | **Receive CAN.** Push-pull structure |
| 13 | VCAN | **HS-CAN Supply Input.** For internal HS-CAN cell needed for CAN Normal Mode |
| 14 | CANH | **CAN High Bus.** |
| 15 | CANL | **CAN Low Bus.** |
| 16 | GND | **Ground.** Transceiver ground (CAN, LIN) |
| 17 | LIN | **LIN Bus.** |
| 18 | WK3 | **Wake-up input 3.** |
| 19 | SL | **Source Low Side.** |
| 20 | GL2 | **Gate Low Side 2.** |
| 21 | GL1 | **Gate Low Side 1.** |
| 22 | WK2/FO | **Wake-up input 2 or Fail Safe Output.** |
| 23 | GH2 | **Gate High Side 2.** |
| 24 | SH2 | **Source High Side 2.** |
| 25 | SH1 | **Source High Side 1.** |
| 26 | GH1 | **Gate High Side 1.** |
| 27 | PWM1/CRC | **PWM input 1.** Internal passive pull-down<br>**CRC.** Connect to GND (via pull-down) to activate CRC functionality |
| 28 | CPC2N | **Negative connection to Charge Pump Capacitor 2.** |
| 29 | CPC2P | **Positive connection to Charge Pump Capacitor 2.** |
| 30 | CPC1P | **Positive connection to Charge Pump Capacitor 1.** |
| 31 | CPC1N | **Negative connection to Charge Pump Capacitor 1.** |
| 32 | VS | **Supply voltage for Bridge Drivers and Charge pump.** Connected to the battery voltage after reverse protection. |
| 33 | CP | **Charge Pump output voltage.** |
| 34 | PWM3 | **PWM input 3.** Internal passive pull-down |
| 35 | GH3 | **Gate High Side 3.** |
| 36 | SH3 | **Source High Side 3.** |
| 37 | SH4 | **Source High Side 4.** |
| 38 | GH4 | **Gate High Side 4.** |
| 39 | WK1 | **Wake-up input 1.** |
| 40 | GL3 | **Gate Low Side 3.** |
| 41 | GL4 | **Gate Low Side 4.** |
| 42 | WK4/SYNC | **Wake-up input 4/Sync.** |
| 43 | HS1 | **High Side output 1.** |
| 44 | HS2 | **High Side output 2.** |

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| Pin | Symbol | Function |
|---|---|---|
| 45 | HS3 | **High Side output 3.** |
| 46 | HS4 | **High Side output 4.** |
| 47 | VSHS | **Supply voltage for HSx and LIN.** Connected to the battery voltage after reverse protection |
| 48 | VSINT | **Voltage regulator and main supply voltage.** Connected to the battery voltage after reverse protection |
| Cooling Tab | GND | Cooling Tab - Exposed Die Pad; For cooling purposes only, do not use as an electrical ground[1)] |

1) The exposed die pad at the bottom of the package allows better power dissipation of heat from the device via the PCB. The exposed die pad is not connected to any active part of the IC. However, it should be connected to GND for the best EMC performance.

*Note: The GND pin as well as the Cooling Tab must be connected to one common GND potential.*

## 3.3 Hints for not functional pins

It must be ensured that the correct configurations are also selected, i.e. in case functions are not used that they are disabled via SPI. Unused pins should be handled as follows:

- **N.U.**: not used; internally bonded for testing purpose; leave open.
- **RSVD**: must be connected to GND.

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# 4 General Product Characteristics

## 4.1 Absolute Maximum Ratings

**Table 1 Absolute Maximum Ratings[1)]**

$T_j$ = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Voltages** | | | | | | | |
| Supply Voltage VS | $V_{S, max}$ | -0.3 | – | 28 | V | – | P_4.1.1 |
| Supply Voltage VS | $V_{S, max}$ | -0.3 | – | 40 | V | Load Dump | P_4.1.2 |
| Supply Voltage VSINT | $V_{SINT, max}$ | -0.3 | – | 28 | V | – | P_4.1.3 |
| Supply Voltage VSINT | $V_{SINT, max}$ | -0.3 | – | 40 | V | Load Dump | P_4.1.4 |
| Supply Voltage VSHS | $V_{SHS, max}$ | -0.3 | – | 28 | V | – | P_4.1.5 |
| Supply Voltage VSHS | $V_{SHS, max}$ | -0.3 | – | 40 | V | Load Dump | P_4.1.6 |
| Voltage Regulator 1 | $V_{CC1, max}$ | -0.3 | – | 5.5 | V | | P_4.1.7 |
| Charge Pump Output Pin (CP) | $V_{CP, max}$ | $V_S$ - 0.8 | – | $V_S$ + 17 | V | $I_{CP}$ > - 200 µA if CP is disabled | P_4.1.8 |
| CPC1P, CPC2P | $V_{CPCxP, max}$ | - 0.3 | – | $V_S$ + 17 | V | | P_4.1.38 |
| CPC1N, CPC2N | $V_{CPCxN, max}$ | - 0.3 | – | $V_S$ + 0.3 | V | | P_4.1.39 |
| Bridge Driver Gate High Side (GHx) | $V_{GHx, max}$ | -8.0 | – | 40 | V | – | P_4.1.11 |
| Bridge Driver Gate Low Side (GLx) | $V_{GLx, max}$ | -8.0 | – | 24 | V | – | P_4.1.12 |
| Voltage difference between GHx-SHx and between GLx-SLx | $V_{GS}$ | -0.3 | – | 16 | V | – | P_4.1.13 |
| Bridge Driver Source High (SHx) | $V_{SHx, max}$ | -8.0 | – | 40 | V | – | P_4.1.14 |
| Bridge Driver Source Low Side SL | $V_{SL, max}$ | -8.0 | – | 6.0 | V | – | P_4.1.15 |
| Wake Input WKx | $V_{WKx, max}$ | -0.3 | – | 40 | V | – | P_4.1.19 |
| High Side HSx | $V_{HSx, max}$ | -0.3 | – | $V_{SHS, max}$ + 0.3 | V | – | P_4.1.20 |
| LIN bus | $V_{LIN, max}$ | -27 | – | 40 | V | – | P_4.1.21 |
| CANH, CANL | $V_{BUS, max}$ | -27 | – | 40 | V | – | P_4.1.22 |
| PWM1/CRC, PWM3 Input Pins | $V_{PWM1-3, max}$ | -0.3 | – | 40 | V | – | P_4.1.23 |
| Logic Input Pins (CSN, CLK, SDI, TXDCAN, TXDLIN) | $V_{I, max}$ | -0.3 | – | $V_{CC1}$ + 0.3 | V | – | P_4.1.27 |

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**Table 1 Absolute Maximum Ratings[1)]** (cont'd)

$T_j$ = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Logic Output Pins (SDO, RSTN, INTN, RXDCAN, RXDLIN) | $V_{O, max}$ | -0.3 | – | $V_{CC1}$ + 0.3 | V | – | P_4.1.30 |
| VCAN Input Voltage | $V_{VCAN, max}$ | -0.3 | – | 5.5 | V | | P_4.1.31 |
| **Temperatures** | | | | | | | |
| Junction Temperature | $T_j$ | -40 | – | 150 | °C | – | P_4.1.32 |
| Storage Temperature | $T_{stg}$ | -55 | – | 150 | °C | – | P_4.1.33 |
| **ESD Susceptibility** | | | | | | | |
| ESD Resistivity | $V_{ESD,11}$ | -2 | – | 2 | kV | HBM[2)] | P_4.1.34 |
| ESD Resistivity to GND, CANH, CANL, LIN | $V_{ESD,12}$ | -8 | – | 8 | kV | HBM[2)3)] | P_4.1.35 |
| ESD Resistivity to GND | $V_{ESD,21}$ | -500 | – | 500 | V | CDM[4)] | P_4.1.36 |
| ESD Resistivity Pin 1, 12,13,24,25,36,37,48 (corner pins) to GND | $V_{ESD,22}$ | -750 | – | 750 | V | CDM[4)] | P_4.1.37 |

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).
3) For ESD "GUN" Resistivity (according to IEC61000-4-2 "gun test" (150 pF, 330 Ω)), is shown in Application Information and test report will be provided from IBEE.
4) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1.

**Notes**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

**Table 2 Functional Range[1)]**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Supply Voltage | $V_{SINT,func}$ | $V_{POR,f}$ | – | 28 | V | [2)] | P_4.2.1 |
| Bridge Supply Voltage | $V_{S,func}$ | 6.0 | – | 28 | V | – | P_4.2.2 |
| High Side Supply Voltage | $V_{SHS_HS,func}$ | 6.0 | – | 28 | V | [2)] | P_4.2.7 |
| LIN Bus Voltage | $V_{SHS_LIN,func}$ | 6 | – | 18 | V | [3)] | P_4.2.3 |
| CAN Supply Voltage | $V_{CAN,func}$ | 4.75 | – | 5.25 | V | – | P_4.2.4 |
| Junction Temperature | $T_j$ | -40 | – | 150 | °C | – | P_4.2.6 |

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1) Not subject to production test, specified by design.
2) Including Power-On Reset, Over- and Undervoltage Protection.
3) Parameter specification according to ISO 17987-4: rev 2016.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

### Device Behavior Outside of Specified Functional Range

- 28 V < **$V_{SINT,func}$** < 40 V: Device will still be functional including the state machine; the specified electrical characteristics might not be ensured anymore. The $V_{CC1}$ is working properly, however, a thermal shutdown might occur due to high power dissipation. HSx switches might be turned OFF depending on HSx_OV configurations. The specified SPI communication speed is ensured; the absolute maximum ratings are not violated, however the device is not intended for continuous operation of $V_{SINT}$ > 28 V and a thermal shutdown might occur due to high power dissipation. The device operation at high junction temperatures for long periods might reduce the operating life time.

  Note: 18 V < $V_{SHS}$ <28 V: The LIN transceiver is still functional. However, the communication might fail due to out-of-LIN-spec operation.

  Note: **$V_{SHS,UVD}$** < $V_{SHS}$ < 6 V: The LIN transceiver is still functional. However, the communication might fail due to out-of-LIN-spec operation.

  Note: $V_{CAN}$ < 4.75 V: The undervoltage bit will be set in the SPI register and the transmitter will be disabled as long as the UV condition is present.

  Note: 5.25 V < $V_{CAN}$ < 5.5 V: CAN transceiver still functional. However, the communication might fail due to out-of-spec operation.

- **$V_{POR,f}$** < $V_{SINT}$ < 5.5 V (given the fact that the device was powered up correctly before with $V_{SINT}$ > 5.5 V): Device will still be functional; the specified electrical characteristics might not be ensured anymore:
  - The voltage regulator will enter the low-drop operation mode.
  - A reset could be triggered depending on the Vrthx settings.
  - The LIN transmitter will be disabled if **$V_{SHS,UVD}$** is reached. .
  - HSx switch behavior will depend on the respective configuration:
    **HS_UV_SD_DIS** = ‘0’ (default): HSx will be turned OFF for $V_{SHS}$ < $V_{SHS,UVD}$ and will stay OFF.
    **HS_UV_SD_DIS** = ‘1’: HSx stays on as long as possible. An unwanted overcurrent shut down may occur. OC shut down bit set and the respective HSx switch will stay OFF.
  - If WK2/FO is configured as Fail Safe Output, FO outputs will remain ON if they were enabled before $V_{SINT}$ > 5.5 V.
  - The specified SPI communication speed is ensured.

*Note: **$V_{S,UV}$** < $V_S$ < 6.0 V: the charge pump might be deactivated due to a charge pump undervoltage detection, resulting in a turn-off of the external MOSFETs.*

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## 4.3 Thermal Resistance

**Table 3 Thermal Resistance[1)]**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to Soldering Point | $R_{th(JSP)}$ | – | 7.2 | – | K/W | Exposed Pad | P_4.3.1 |
| Junction to Ambient | $R_{th(JA)}$ | – | 27 | – | K/W | 2) | P_4.3.2 |

1) Not subject to production test, specified by design.

2) Specified $R_{th(JA)}$ value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board for a power dissipation of 1.5 W; the product (chip+package) was simulated on a 76.2 x 114.3 x 1.5 $mm^3$ with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm C); where applicable a thermal via array under the exposed pad contacted the first inner copper layer and 300 $mm^2$ cooling areas on the top layer and bottom layers (70 µm).

## 4.4 Current Consumption

**Table 4 Current Consumption**

Current consumption values are specified at $T_j$ = 25°C, $V_{SINT}$= $V_{SHS}$ = 13.5 V, all outputs open (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Normal Mode** | | | | | | | |
| Normal Mode current consumption | $I_{Normal}$ | – | 4.5 | 5.5 | mA | 1) $V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; CAN=LIN=CP=off | P_4.4.1 |
| **Stop Mode** | | | | | | | |
| Stop Mode current consumption (low active peak threshold) | $I_{Stop_1,25}$ | – | 50 | 65 | µA | 1)2) CAN=LIN=off; WKx=HSx=CP=off: Cyclic Wak./Sen.=off Watchdog = off; no load on $V_{CC1}$; **I_PEAK_TH** = $0_B$ | P_4.4.2 |
| Stop Mode current consumption (low active peak threshold) | $I_{Stop_1,85}$ | – | 55 | 80 | µA | 1)2)3) $T_j$ = 85°C; CAN=LIN=off; WKx=HSx=CP=off: Cyclic Wak./Sen.=off Watchdog = off; no load on $V_{CC1}$; **I_PEAK_TH** = $0_B$ | P_4.4.3 |
| Stop Mode current consumption (high active peak threshold) | $I_{Stop_2,25}$ | – | 70 | 95 | µA | 1)2) CAN=LIN=off; WKx=HSx=CP=off: Cyclic Wak./Sen.=off Watchdog = off; no load on $V_{CC1}$; **I_PEAK_TH** = $1_B$ | P_4.4.4 |

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**Table 4 Current Consumption** (cont'd)

Current consumption values are specified at $T_j$ = 25°C, $V_{SINT}$= $V_{SHS}$ = 13.5 V, all outputs open (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Stop Mode current consumption (high active peak threshold) | $I_{Stop_2,85}$ | – | 75 | 105 | µA | 1)2)3) $T_j$ = 85°C; CAN=LIN=off; Cyclic Wak./Sen.=off; Watchdog = off; no load on $V_{CC1}$; **I_PEAK_TH** = $1_B$ | P_4.4.5 |
| **Sleep Mode** | | | | | | | |
| Sleep Mode current consumption | $I_{Sleep,25}$ | – | 18 | 30 | µA | 1) CAN=LIN=off; WKx=HSx=CP=off: Cyclic Wak./Sen.= off | P_4.4.6 |
| Sleep Mode current consumption | $I_{Sleep,85}$ | – | 28 | 40 | µA | 1)3) $T_j$ = 85°C; CAN=LIN=off; WKx=HSx=CP=off: Cyclic Wak./Sen.=off | P_4.4.7 |
| **Feature Incremental Current Consumption** | | | | | | | |
| Current consumption for LIN module, recessive state | $I_{LIN,rec}$ | – | 1.0 | 1.2 | mA | 3)4) Normal/Stop Mode; LIN Normal Mode; $T_j$ = -40°C to +150°C; $V_{TXDLIN}$ = $V_{CC1}$; no RL on LIN | P_4.4.8 |
| Current consumption for LIN module, dominant state | $I_{LIN,dom}$ | – | 1.5 | 1.7 | mA | 3)4) Normal/Stop Mode; LIN Normal Mode; $T_j$ = -40°C to +150°C; $V_{TXDLIN}$ = GND; no RL on LIN | P_4.4.9 |
| Current consumption for LIN module, Receive Only Mode, Normal Mode | $I_{LIN,Rec_onlyN}$ | – | 0.1 | 0.2 | mA | 3)4) Normal Mode; LIN Receive Only Mode; $V_{TXDLIN}$ = $V_{CC1}$ no RL on LIN | P_4.4.10 |
| Current consumption for LIN wake capability | $I_{LIN,wake,25}$ | – | 0.2 | 2 | µA | 4) Stop/Sleep Mode; LIN wake capable; | P_4.4.11 |
| Current consumption for LIN wake capability | $I_{LIN,wake,85}$ | – | 2 | 3 | µA | 3)4) Stop/Sleep Mode; $T_j$ = 85°C; LIN wake capable; | P_4.4.12 |

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**Table 4 Current Consumption** (cont'd)

Current consumption values are specified at $T_j$ = 25°C, $V_{SINT}$= $V_{SHS}$ = 13.5 V, all outputs open (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Current consumption for CAN module, recessive state | $I_{CAN,rec}$ | – | 2 | 3.5 | mA | [1)3)] Normal/Stop Mode; CAN Normal Mode; $T_j$ = -40°C to +150°C; $V_{CC1}$ connected to $V_{CAN}$; $V_{TXDCAN}$ = $V_{CC1}$; no RL on CAN | P_4.4.13 |
| Current consumption for CAN module, dominant state | $I_{CAN,dom}$ | – | 3 | 5.0 | mA | [1)3)] Normal/Stop Mode; CAN Normal Mode; $T_j$ = -40°C to +150°C; $V_{CC1}$ connected to $V_{CAN}$; $V_{TXDCAN}$ = GND; no RL on CAN | P_4.4.14 |
| Current consumption for CAN module, Receive Only Mode, Normal Mode | $I_{CAN,Rec_onlyN}$ | – | 0.5 | 0.7 | mA | [1)3)] Normal Mode; CAN Receive Only Mode; $T_j$ = -40°C to +150°C; $V_{CC1}$ connected to $V_{CAN}$; $V_{TXDCAN}$ = $V_{CC1}$; no RL on CAN | P_4.4.15 |
| Current consumption for CAN module, Receive Only Mode, Stop Mode | $I_{CAN,Rec_only}$ | – | 1.4 | 1.5 | mA | [1)3)] Stop Mode; CAN Receive Only Mode; $T_j$ = -40°C to +150°C; $V_{CC1}$ connected to $V_{CAN}$; $V_{TXDCAN}$ = $V_{CC1}$; no RL on CAN | P_4.4.16 |
| Current consumption for CAN wake capability | $I_{CAN,wake,25}$ | – | 4.5 | 7 | µA | [5)] Sleep Mode; CAN wake capable; | P_4.4.17 |
| Current consumption for CAN wake capability | $I_{CAN,wake,85}$ | – | 8 | 10 | µA | [3)5)] Sleep Mode; $T_j$ = 85°C; CAN wake capable; WK = off; | P_4.4.18 |
| Current consumption for each WK input | $I_{WK,wake,25}$ | – | 0.2 | 2 | µA | [1)5)6)7)] Sleep Mode; WK wake capable; no activity on WK pin; | P_4.4.22 |
| Current consumption for each WK input | $I_{WK,wake,85}$ | – | 0.5 | 3 | µA | [1)3)5)6)7)] Sleep Mode; $T_j$ = 85°C; WK wake capable; no activity on WK pin; | P_4.4.23 |

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**Table 4 Current Consumption** (cont'd)

Current consumption values are specified at $T_j$ = 25°C, $V_{SINT}$= $V_{SHS}$ = 13.5 V, all outputs open (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Current consumption for first High-Side in Stop Mode | $I_{Stop,HS,25}$ | – | 250 | 375 | µA | 3)5)8)10)9) Stop Mode; HS with 100% duty cycle (no load); | P_4.4.24 |
| Current consumption for first High-Side in Stop Mode | $I_{Stop,HS,85}$ | – | 250 | 375 | µA | 3)5)8)10)9) Stop Mode; $T_j$ = 85°C; HS with 100% duty cycle (no load); | P_4.4.25 |
| Current consumption for cyclic sense function | $I_{Stop,CS25}$ | – | 20 | 26 | µA | 5)8)10)11) Stop Mode; WD = off; | P_4.4.26 |
| Current consumption for cyclic sense function | $I_{Stop,CS85}$ | – | 24 | 32 | µA | 3)5)8)10)11) Stop Mode; $T_j$ = 85°C; WD = off; | P_4.4.27 |
| Current consumption for watchdog active in Stop Mode | $I_{Stop,WD25}$ | – | 18 | 23 | µA | 3)12) Stop Mode; Watchdog running; | P_4.4.28 |
| Current consumption for watchdog active in Stop Mode | $I_{Stop,WD85}$ | – | 19 | 25 | µA | 3)12) Stop Mode; $T_j$ = 85°C; Watchdog running; | P_4.4.29 |
| Current consumption for active Fail Output FO | $I_{Stop,FO}$ | – | 350 | 600 | µA | 3)12) all modes; $T_j$ < 85°C; FO = on (no load); | P_4.4.30 |
| Current consumption in parking braking mode (LSx ON) | $I_{parking}$ | – | 10 | 14 | µA | 3)12) Stop Mode or Sleep Mode; $T_j$ < 85°C; **PARK_BRK_EN** = $1_B$ | P_4.4.32 |
| Current consumption Over voltage braking mode (LSx OFF) | $I_{OV,LS_OFF}$ | – | 7 | 10 | µA | 3)12) Stop Mode or Sleep Mode; $T_j$ < 85°C; **OV_BRK_EN** = $1_B$ | P_4.4.34 |
| Current consumption in VS for Charge Pump and Bridge Driver | $I_{CP,BD}$ | – | 30 | 40 | mA | Normal Mode; $T_j$ = -40°C to +150°C; **CPEN** = 1; All HB OFF | P_4.4.35 |

1) Measured at $V_{SINT}$.
2) If the load current on $V_{CC1}$ will exceed the configured $V_{CC1}$ active peak threshold, the current consumption will increase by typ. 2.9 mA to ensure optimum dynamic load behavior. See also **Chapter 6**.
3) Not subject to production test, specified by design.
4) Additional current will be drawn from VSHS.
5) Current consumption adders of features defined for Stop Mode also apply for Sleep Mode and vice versa. Wake input signals are stable (i.e. not toggling), cyclic wake/sense & watchdog are OFF (unless otherwise specified).
6) No pull-up or pull-down configuration selected.
7) The specified WKx current consumption adder for wake capability applies regardless how many WK inputs are activated.
8) Additional current will be drawn from $V_{SHS}$ and $V_{SINT}$.
9) Typical adder of additional high-side switch activation 200 µA.

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10) HSx used for cyclic sense, Timerx with 20ms period, 0.1 ms on-time, no load.
In general the current consumption adder for cyclic sense in Stop Mode can be calculated with below equation:
$I_{Stop,CS_typ}$ = 18 µA + ($I_{Stop,HS,25}$ x ton/TPer)
where the 18 uA is the base current consumption of the digital cyclic sense/wake functionality.
11) Also applies to cyclic wake but without adder from HS biasing contribution.
12) Additional current will be drawn from $V_{SINT}$.

## Notes

1. *There is no additional current consumption contribution in Normal Mode due to PWM generators or Timers.*
2. *The quiescent current consumption in Stop Mode and Sleep Mode will increase for $V_{SINT}$ < 9 V.*

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# 5 System Features

This chapter describes the system features and behavior of the TLE9562QX:

- State machine
- Device configuration
- State machine modes and mode transitions
- Wake-up features such as cyclic sense and cyclic wake

## 5.1 Short State Machine Description

The DC Motor System IC offers six operating modes:

- Init Mode: Power-up of the device and after a soft reset.
- Normal Mode: The main operating mode of the device.
- Stop Mode: The first-level power saving mode with the main voltage regulator VCC1 enabled.
- Sleep Mode: The second-level power saving mode with VCC1 disabled.
- Restart Mode: An intermediate mode after a wake event from Sleep Mode or Fail-Safe Mode or after a failure (e.g. WD failure, VCC1 under voltage reset) to bring the microcontroller into a defined state via a reset.
- Fail-Safe Mode: A safe-state mode after critical failures (e.g. Temperature shutdown) to bring the system into a safe state and to ensure a proper restart of the system.

A special mode, called Software Development Mode, is available during software development or debugging of the system. All above mentioned operating modes can be accessed in this mode. However, the watchdog is still running, but no reset to the microcontroller is applied. Watchdog failures are indicated over INTN pin instead.

However, the watchdog reset signaling can be reactivated again in Software Development Mode. The Watchdog will start always with the Long Open Windows (t_low).

The DC Motor System IC is controlled via a 32-bit SPI interface (refer to **Chapter 14** for detailed information). The configuration as well as the diagnosis is handled via the SPI.

The device offers various supervision features to support functional safety requirements. Refer to **Chapter 13** for more information.

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## 5.2 Device Configuration

Two features on the DC Motor System IC can be configured by hardware:

- The selection of the normal device operation or the Software Development Mode.
- Enabling/disabling the CRC on the SPI interface.

The configurations are done monitoring the follow pins:

- INTN/TEST
- PWM1/CRC

The hardware configuration can be done typically at device power-up, where the device is in Init Mode or (only in case of CRC setting) in Restart Mode.

### Software development Mode configuration detail

After the RSTN is released, the INTN/TEST pin is internally pulled HIGH with a weak pull-up resistor. Therefore the default configuration is the device in normal operation.

In order to configure the Software Development Mode, the following conditions have to be fulfilled:

- Init Mode from power-up
- VCC1>Vrtx
- **POR**=1
- RSTN = HIGH

The Software Development Mode is configured using the following scheme:

- Only one external pull-down on INTN/TEST pin followed by an arbitrary SPI command, the device latches the Software Development Mode.
- External pull-up or no pull-down on INTN/TEST pin enable the device in normal operation.
- To enter Software Development Mode, a pull-down resistor to GND might be used.

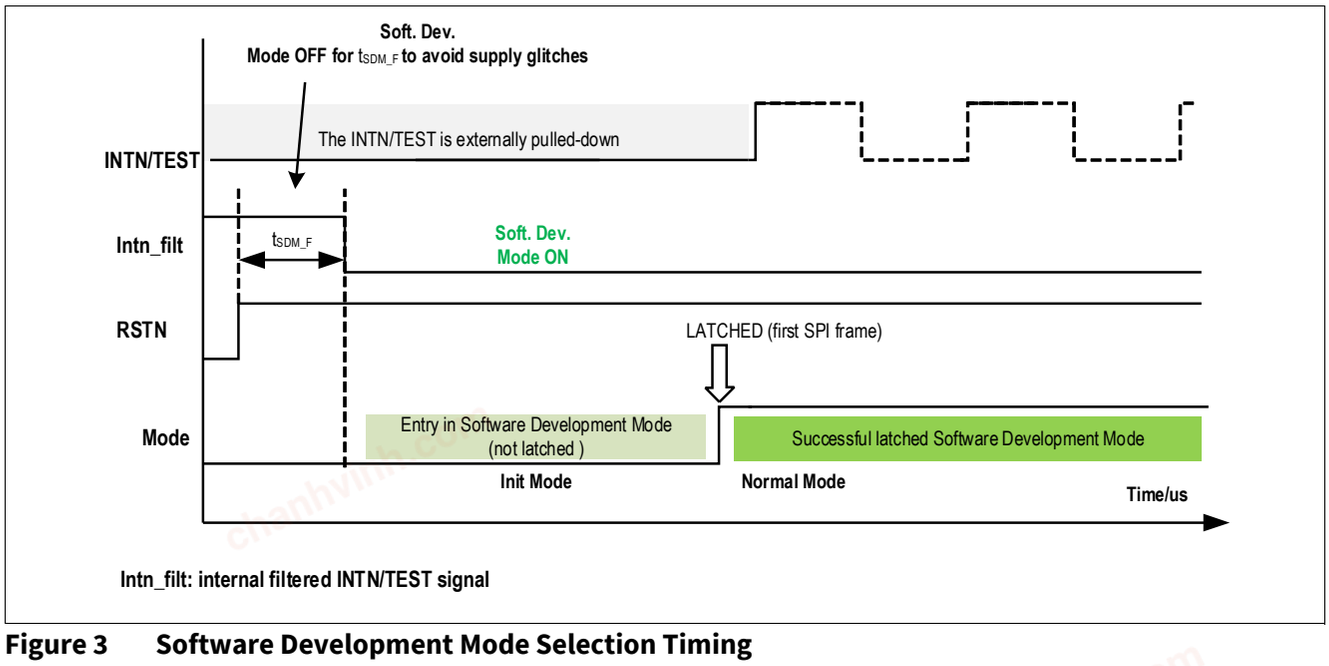



**Figure 3 Software Development Mode Selection Timing**

Intn_filt is a filtered signal from INTN/TEST, with the filter time $t_{SMD_F}$ (P_11.2.7). Intn_filt starts (at the rising edge if RSNT) wit the value 1.

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*Note: If during monitoring the INTN/TEST pin for Software Development Mode entry, the device changes the mode without SPI command, the device will not enter/stay in Software Development Mode.*

### CRC configuration detail

The CRC is configured using the following scheme:

- Pull-down on PWM1/CRC enable the CRC.
- No external components on PWM1/CRC disables the CRC.

In order to configure the CRC, the follow conditions have to be full filled:

- Init Mode (from power-up) or Restart Mode
- VCC1>Vrtx
- **POR**=1
- RSTN = LOW

The configuration selection is done during the reset delay time $t_{RD1}$ with a continuous filter time of $t_{CFG_F}$ and the configuration (depending on the voltage level at PWM1/CRC) is latched at the rising edge of RSTN.

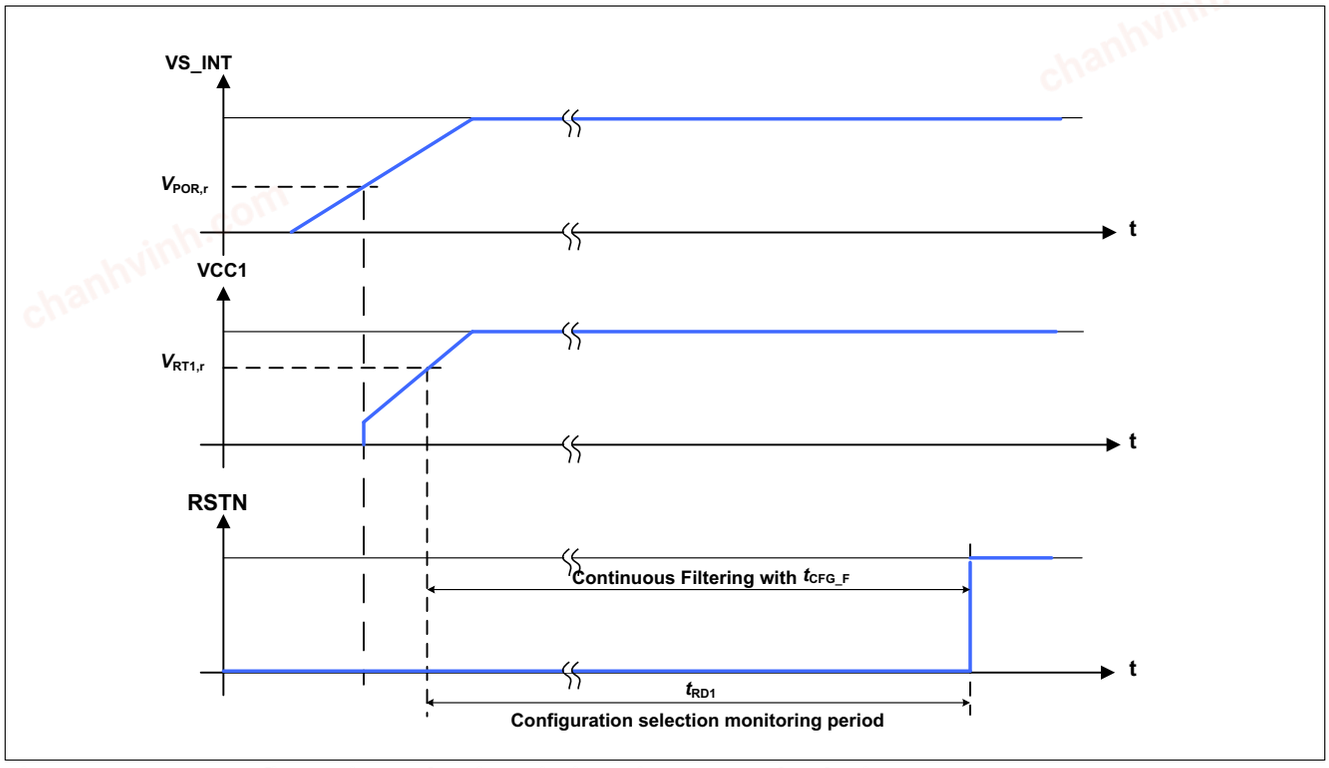



**Figure 4 CRC configuration Selection Timing Diagram at the device power-up.**

In case of mismatch between CRC setting between the device and µC (**CRC_STAT**), the device can accept two recovery SPI commands (static patterns).

The pattern 67AA AA0E$_H$ (addr + rw_bit = 67 ; data = AAAA ; CRC = 0E ) enables the CRC.

The pattern E7AA AAC3$_H$ (addr + rw_bit = E7 ; data = AAAA ; CRC = C3) disables the CRC.

The patterns shall be send only in Normal Mode.

For additional details about the CRC setting and configuration, refer also to **Chapter 14.3.1**.

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## 5.3 Block Description of State Machine

The state machine describes the different states of operation, the device may get into. The following figure shows the state machine flow diagram.

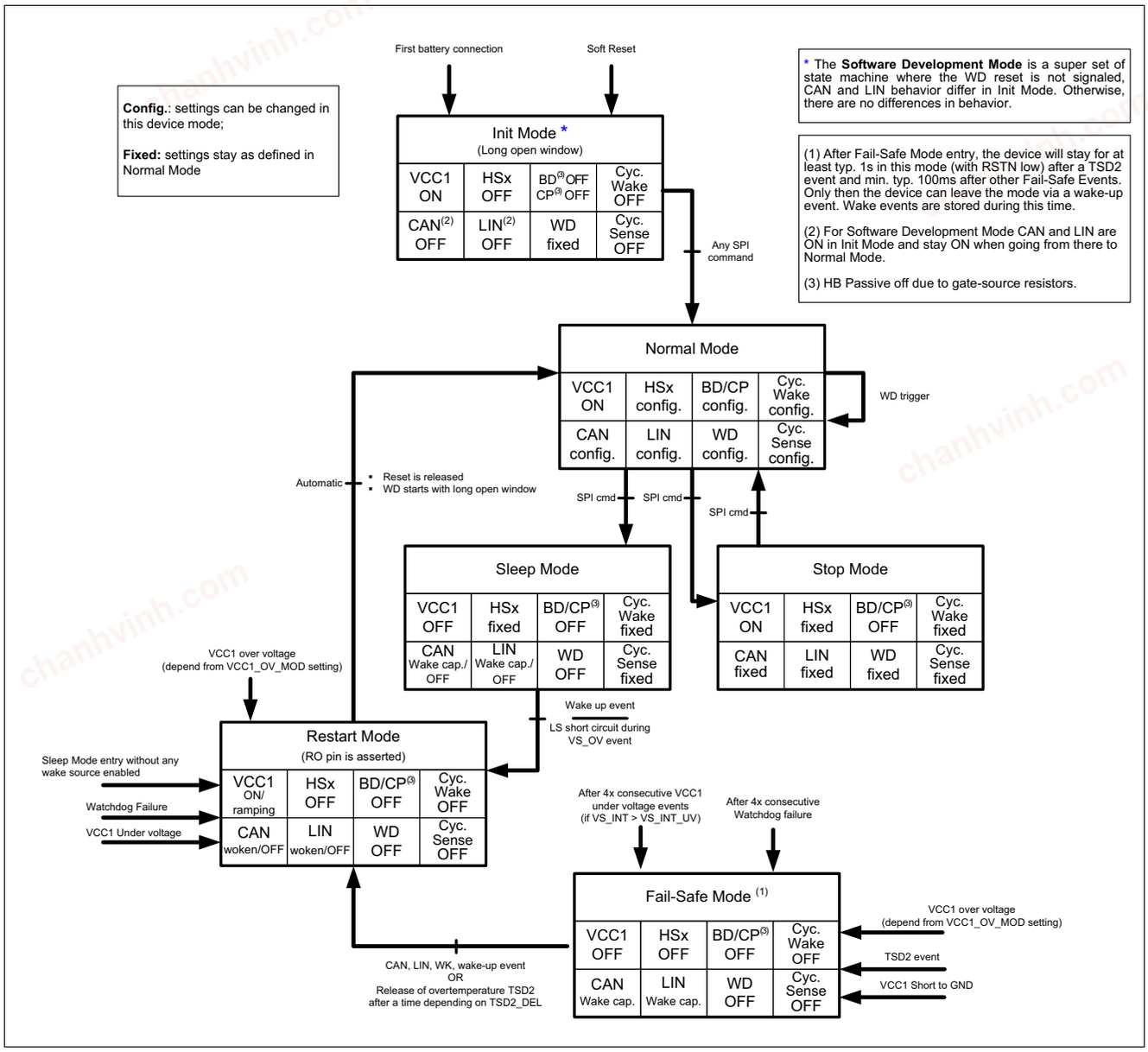



**Figure 5 State Diagram showing the operating modes**

**Description:**

- ON /OFF:= Indicate if the module is enabled or disabled either via SPI or from the device itself
- config:= Settings can be changed in this mode
- fixed:= Settings stay as defined in Normal Mode or Init Mode
- active/inactive:= Indicate if the device activates/deactivates one specific feature
- Wake capable:= Transceiver that is capable to detect one wake-up events
- woken:= Transceiver that has detected one wake-up event

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## 5.4 State Machine Modes Description

### 5.4.1 Init Mode

The device starts up in Init Mode after crossing the power-on reset $V_{POR,r}$ threshold (see also **Chapter 13.3**) and the watchdog will start with a long open window ($t_{LW}$) after RSTN is released (High level).

In Init Mode, the device waits for the microcontroller to finish its startup and initialization sequence.

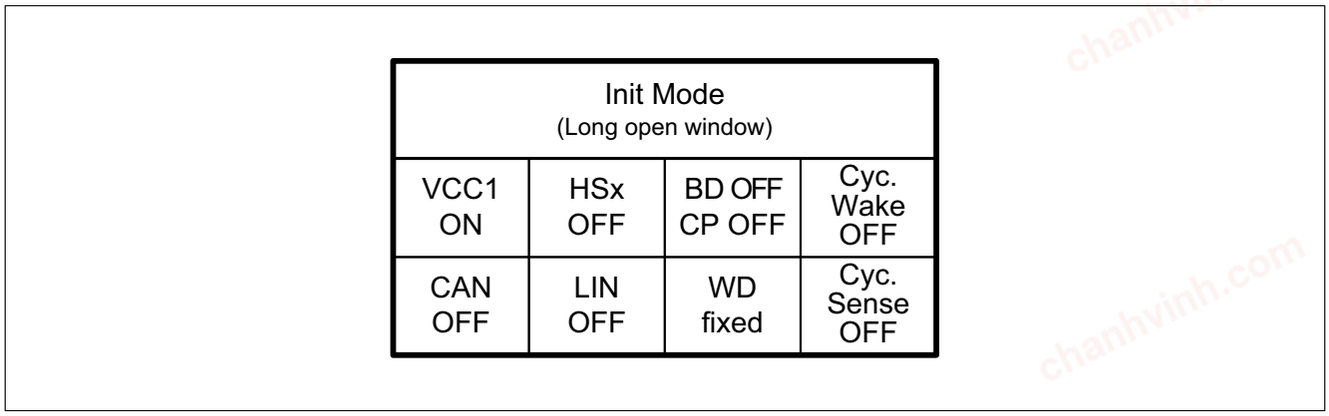



**Figure 6 Init Mode**

**Table 5 Init Mode Settings**

| Part/Function | Value | Description |
|---|---|---|
| VCC1 | ON | • The VCC1 is ON |
| WD | fixed | • Watchdog is fixed and set with a long open window ($t_{LW}$) |
| HSx | OFF | • All HSx are OFF |
| BD | OFF | • Bridge Drivers is OFF |
| CP | OFF | • Charge Pump is OFF |
| CAN | OFF | • CAN transceiver is OFF[1)] |
| LIN | OFF | • LIN transceiver is OFF [2)] |
| Cyc Sense | OFF | • Cycle Sense is OFF |
| Cyc Wake | OFF | • Cycle Wake is OFF |

1) Exception: The CAN transceiver is ON during Software Development Mode
2) Exception: The LIN transceiver is ON during Software Development Mode

### 5.4.2 Normal Mode

The Normal Mode is the standard operating mode for the device. The VCC1 is active and all features are configurable. Supervision and monitoring features are enabled.

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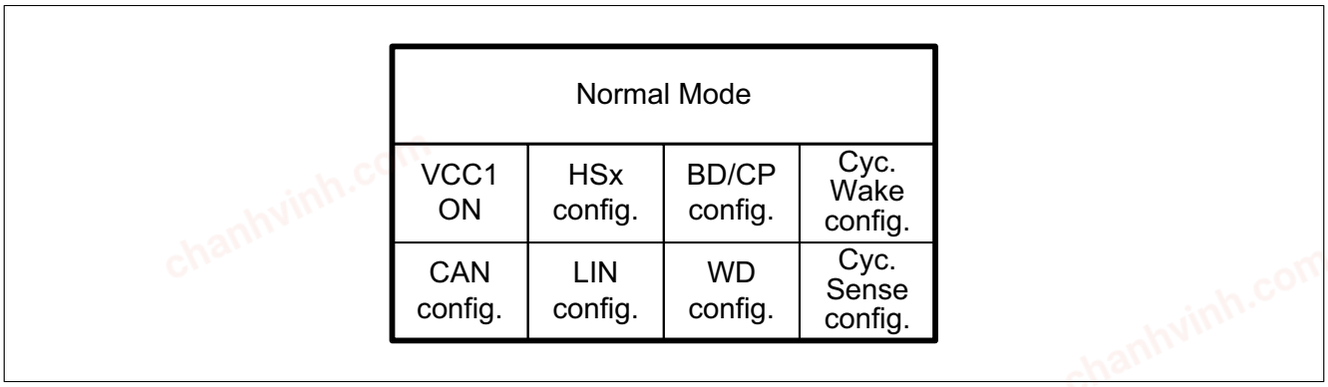



**Figure 7 Normal Mode**

**Table 6 Normal Mode Settings**

| Part/Function | Value | Description |
|---|---|---|
| VCC1 | ON | • VCC1 is active |
| WD | config | • Watchdog may be configured by SPI |
| HSx | config | • The High Side Switches may be configured and switched ON or OFF by SPI |
| BD/CP | config | • The Bridge Drivers and Charge Pump may be configured and switched ON or OFF by SPI |
| CAN | config | • CAN may be configurable and switched ON or OFF by SPI |
| LIN | config | • LIN may be configurable and switched ON or OFF by SPI |
| Cyc. Sense | config | • Cyclic sense may be configured with the HSx, WKx inputs and Timer1 or Timer2 or SYNC (WK4) |
| Cyc. Wake | config | • Cyclic wake can be configured with the Timer1 or Timer 2 |

### 5.4.3 Stop Mode

The Stop Mode is the first level technique to reduce the overall current consumption by setting the voltage regulator VCC1 into a low-power mode.

*Note: All settings have to be done before entering Stop Mode.*

In Stop Mode any kind of SPI WRITE commands are ignored and the **SPI_FAIL** bit is set, except for changing to Normal Mode, triggering a device Soft Reset, refreshing the watchdog as well as for reading and clearing the SPI status registers.

*Note: A wake-up event on CAN, LIN, WKx, Low-Side short circuit detection in parking braking mode or overvoltage brake detection, could generate an interrupt on pin INTN (based on INTN masking configuration; refer to **Chapter 11**) however, no change of the device mode will occur.*

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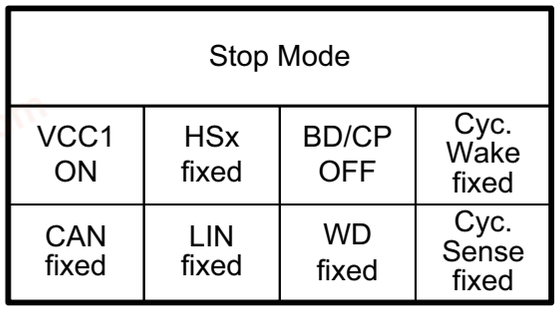



**Figure 8 Stop Mode**

**Table 7 Stop Mode Settings**

| Part/Function | Value | Description |
|---|---|---|
| VCC1 | ON | • VCC1 is ON |
| WD | fixed | • Watchdog is fixed as configured in Normal Mode |
| HSx | fixed | • HSx are fixed as configured in Normal Mode |
| BD/CP | OFF | • The Bridge Drivers and Charge Pump are OFF |
| CAN | fixed | • CAN fixed as configured in Normal Mode |
| LIN | fixed | • LIN fixed as configured in Normal Mode |
| Cyc. Sense | fixed | • Cyclic sense fixed as configured in Normal Mode |
| Cyc. Wake | fixed | • Cyclic wake is fixed as configured in Normal Mode |

*Note: In Stop Mode, it is possible to activate the Low-Side of Bridge Drivers (e.g. in case of parking braking mode or overvoltage brake detection). Refer to **Chapter 13.11** for additional details.*

### 5.4.4 Sleep Mode

The Sleep Mode is the second level technique to reduce the overall current consumption to a minimum needed to react on wake-up events or for the device to perform autonomous actions (e.g. cyclic sense).

*Note: All settings have to be done before entering Sleep Mode.*

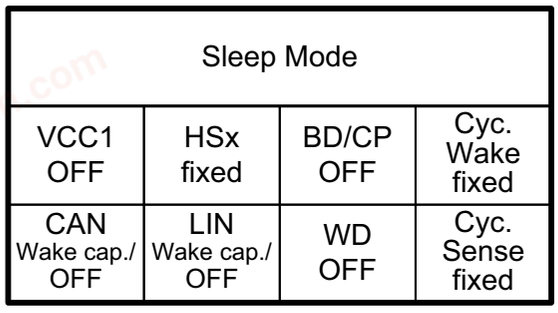



**Figure 9 Sleep Mode**

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**Table 8 Sleep Mode Settings**

| Part/Function | Value | Description |
|---|---|---|
| VCC1 | OFF | • VCC1 is OFF |
| WD | OFF | • Watchdog is OFF |
| HSx | fixed | • HSx are fixed as configured in Normal Mode |
| BD/CP | OFF | • The Bridge Drivers and Charge Pump are OFF |
| CAN | Wake Cap/ OFF | • CAN fixed as configured (Wake Capable or OFF) |
| LIN | Wake Cap/ OFF | • LIN fixed as configured (Wake Capable or OFF) |
| Cyc. Sense | fixed | • Cyclic sense fixed as configured in Normal Mode |
| Cyc. Wake | fixed | • Cyclic wake is fixed |

*Note: In Sleep Mode, it is possible to activate the Low-Side's of Bridge Drivers (e.g. in case of parking braking mode or overvoltage braking). Refer to **Chapter 13.11** for additional details.*

### 5.4.5 Restart Mode

The Restart Mode is a transition state where the RSNT pin is asserted.

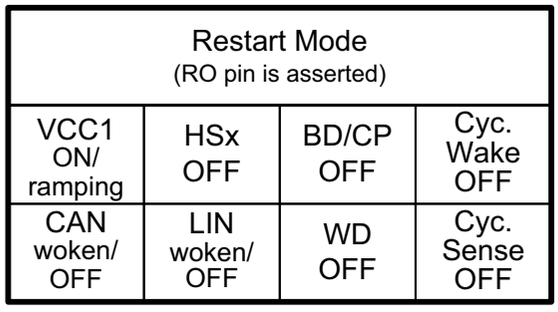



**Figure 10 Restart Mode**

**Table 9 Restart Mode Settings**

| Part/Function | Value | Description |
|---|---|---|
| VCC1 | ON/ ramping | • VCC1 is ON or ramping up |
| WD | OFF | • WD will be disabled if it was activated before |
| HSx | OFF | • HSx will be disabled if it was activated before |
| BD/CP | OFF | • The Bridge Drivers and Charge Pump are OFF |
| CAN | Woken/ wake capable/ OFF | • CAN may woken (in case of wake-up event on the Bus) or wake capable or OFF |

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**Table 9 Restart Mode Settings** (cont'd)

| Part/Function | Value | Description |
|---|---|---|
| LIN | Woken/ wake capable/ OFF | • LIN may woken (in case of wake-up event on the Bus) or wake capable or OFF |
| Cyc. Sense | OFF | • Cyclic sense will be disabled if it was activated before |
| Cyc. Wake | OFF | • Cyclic wake will be disabled if it was activated before |

## 5.4.6 Fail-Safe Mode

The purpose of this mode is to bring the system in a safe status after a failure condition by turning OFF the VCC1 supply and powering off the microcontroller. After a wake event the system is then able to restart again.

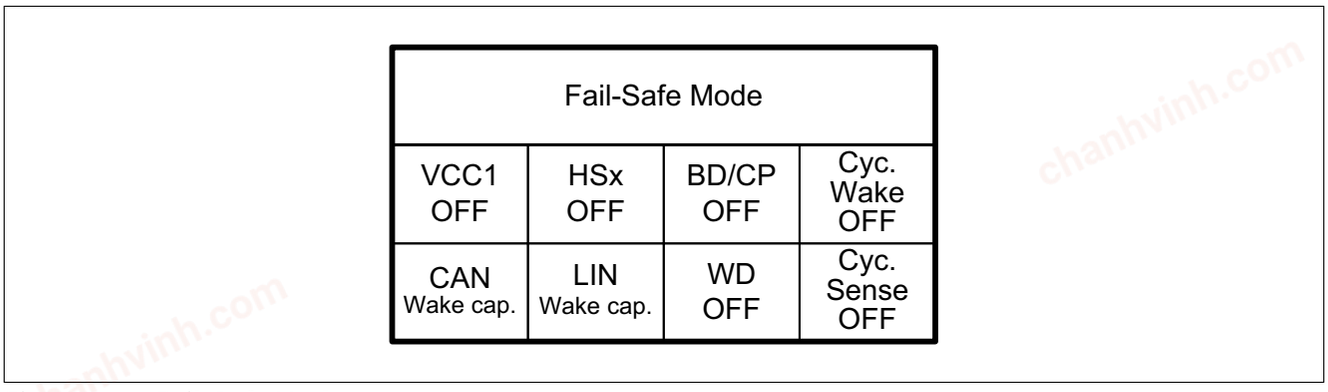



**Figure 11 Fail-Safe Mode**

**Table 10 Fail-Safe Mode Settings**

| Part/Function | Value | Description |
|---|---|---|
| VCC1 | OFF | • VCC1 is switched OFF |
| WD | OFF | • WD is switched OFF |
| HSx | OFF | • HSx are switched OFF |
| BD/CP | OFF | • The Bridge Drivers and Charge Pump are OFF |
| CAN | Wake Cap | • CAN is forced to be Wake capable |
| LIN | Wake Cap | • LIN is forced to be Wake capable |
| Cyc. Sense | OFF | • Cyclic sense is switched OFF |
| Cyc. Wake | OFF | • Cyclic wake is switched OFF |

**Note**

- In Fail-Safe Mode, the default wake sources CAN, LIN and WKx (if configured as wake inputs) are activated automatically and all wake event bits will be cleared.
- In case that WK2 is set as Fail Safe Output (FO), the WK2/FO is automatically activated.
- The Fail-Safe Mode will be maintained until a wake event on the default wake sources occurs. To avoid any fast toggling behavior a filter time of typ. 100ms ($t_{FS,min}$) is implemented. Wake events during this time will be stored and will automatically lead to entering Restart Mode after the filter time.
  In case of an VCC1 overtemperature shutdown (TSD2) the Restart Mode will be reached automatically after

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a filter time of typ. 1s ($t_{TSD2}$) without the need of a wake event once the device temperature has fallen below the TSD2 threshold.

- The parking braking mode is automatically disabled in Fail-Safe Mode.

### 5.4.7 Software Development Mode

The Software Development Mode is a dedicated device configuration especially useful for software development.

Compared to the default device user mode operation, this mode is a super set of the state machine. The device will start also in Init Mode and it is possible to use all the modes and functions with following differences:

- Restart Mode or Fail-Safe Mode (depending on the configuration) is not reached due to watchdog failure but the other reasons to enter these modes are still valid.
- CAN, LIN default value in Init Mode and entering Normal Mode from Init Mode is ON instead of OFF.

**Table 11 Normal Mode Settings (Software Development Mode active)**

| Part/Function | Default State | Description |
|---|---|---|
| VCC1 | ON | • VCC1 is active |
| WD | ON | • WD is on, but will not trigger transition to Fail-Safe Mode or Restart Mode |
| HSx | OFF | • The High Side Switches may be configured and switched ON or OFF by SPI |
| BD/CP | OFF | • The Bridge Drivers and Charge Pump may be configured and switched ON or OFF by SPI |
| CAN | ON | • CAN may be configurable and switched ON or OFF by SPI |
| LIN | ON | • LIN may be configurable and switched ON or OFF by SPI |
| Cyc. Sense | OFF | • Can be configured |
| Cyc. Wake | OFF | • Can be configured |

#### Software Development Mode entry

For timing and configuration details, refer to **Chapter 5.2**.

**Note**

- After Init Mode, the pull-up is released as the INTN/TEST pin acts as output then to drive the INTN signal.
- If the device enters Fail-Safe Mode due to VCC1 short circuit to GND during the Init Mode, the Software Development Mode will not be entered and can only be reached at the next power-up of the device after the VCC1 short circuit is removed.
- The absolute maximum ratings of the pin INTN must be observed. To increase the robustness of this pin during debugging or programming a series resistor between INTN and the connector can be added.

#### Watchdog in Software Development Mode

The Watchdog is enabled in Software Development Mode as default state. One INTN event is generated due to wrong watchdog trigger.

It is possible to deactivate the integrated Watchdog module using the **WD_SDM_DISABLE** bit. After disabling the Watchdog, no INTN events are generated and the **WD_FAIL** bit will also not be set anymore in case of a trigger failure. It is also possible only to mask / unmask the INTN event of the WD in Software Development Mode by using the bit **WD_SDM**. In case of unmasking, a WD trigger fail will only lead to **WD_FAIL** bit set.

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## 5.5 Transition Between States

This chapter describes the transition between the modes triggered by power-up, SPI commands or wake-up events.

### 5.5.1 Transition into Init Mode

The device goes into Init Mode in case of a power-up or after sending a soft-reset in Normal or Stop Mode.

**Prerequisites**:

- Power OFF
- Device in Normal Mode or Stop Mode with follow conditions:
  - VSINT > VPOR,r
  - RSTN High

**Triggering Events:**

- A Soft Reset command (**MODE** = '11'). All SPI registers will be changed to their respective Soft Reset values.

**Note**

- In case of Soft Reset command, a hardware RSTN event can be generated depending on the configuration. An external Reset will be generated in case of **SOFT_RESET_RO** = $0_B$ . In case of **SOFT_RESET_RO** = $1_B$, no RSTN hardware event is generated in case of Soft Reset.
- At power-up, the SPI bit **VCC1_UV** will not be set as long as VCC1 is below the VRT,x threshold and if VSINT is below the VSINT,UV threshold. The RSTN pin will be kept LOW as long as VCC1 is below the selected VRT1,r threshold. The reset delay counter will start after VRT1,r threshold is reached. After the first threshold crossing of VCC1 > $V_{RT1,R}$ and RSTN transition from low to high, all subsequent undervoltage events will lead to Restart Mode.
- Wake events are ignored during Init Mode and will be lost.
- The bit **VSINT_UV** will only be updated in Init Mode once RSTN resumes a high level.

### 5.5.2 Init Mode -> Normal Mode

This transition moves the device in the mode where all configurations are accessable via SPI command.

**Prerequisites:**

- VSINT > VPOR,r
- Init Mode
- RSTN High

**Triggering Events:**

- Any valid SPI command (from SPI protocol point of view) will bring the device to Normal Mode (i.e. any register can be written, cleared and read) during the long open window where the watchdog has to be triggered (refer also **Chapter 14.2**). The CRC is not taken into account for this transition.
- For example:
  - A SPI Sleep Mode command will still bring the device into Normal Mode. However, as this is an invalid state transition, the SPI bit **SPI_FAIL** is set.
  - Any invalid SPI command (from content point of view) will still bring the device into Normal Mode. The SPI bit **SPI_FAIL** is set.

**Note**

- It is recommended to use the first SPI command to trigger and to configure the watchdog.

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### 5.5.3 Normal Mode -> Stop Mode

This transition is intended as first measure to reduce the current consumption. All the device features needed in Stop Mode shall be configured in Normal Mode.

**Prerequisites:**

- VCC1>Vrtx
- Device in Normal Mode

**Triggering Events:**

- State transition is only initiated by specific SPI command.

**Note**

- An interrupt is triggered on the pin INTN when Stop Mode is entered and not all wake source signalization flags were cleared.
- If high-side switches are kept enabled during Stop Mode, then the device current consumption will increase.
- It is not possible to switch directly from Stop Mode to Sleep Mode. Doing so will also set the **SPI_FAIL** flag and will bring the device into Restart Mode.

### 5.5.4 Normal Mode -> Sleep Mode

This transition is intended to reduce as much as possible the current consumption keeping active only wake-up sources. All wake-up sources configurations shall be done in Normal Mode.

**Prerequisites:**

- VCC1>Vrtx
- Device in Normal Mode
- All wake source signalization flags were cleared (including the LSxDSOV_BRK bit)
- At least one wake-up source activated

**Triggering Events:**

- State transition is only initiated by specific SPI command.

**Note**

- If the HSx outputs are kept enabled during Sleep Mode, then the device current consumption will increase (see **Chapter 4.4**).
- The Cyclic Sense function will not work properly anymore in case of a failure event (e.g. overcurrent, over temperature, reset) because the configured HSx and Timers will be disabled.
- If **VCC1_UV** or **VCC1_OV** (with Config to go to Restart Mode) occurs at the border of the Sleep Mode entry: The device will go immeditaley into Restart Mode.
- If **TSD2** or **VCC1_OV** (with Config to go to Fail-Safe Mode) occurs at the border of the Sleep Mode entry: The device will enter immediately Fail-Safe Mode.
- As soon as the Sleep Mode command is sent, the Reset will go low.
- It is not possible to switch all wake sources off in Sleep Mode. Doing so will set the **SPI_FAIL** flag and will bring the device into Restart Mode.

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### 5.5.5 Stop Mode -> Normal Mode

This transition is intented to set the device in Normal Mode where all the device integrated features are availbale and configurable.

**Prerequisites:**

- VCC1>Vrtx
- Device in Stop Mode

**Triggering Events:**

- State transition is only initiated by SPI command.

**Note**

- None

### 5.5.6 Sleep Mode -> Restart Mode

This transition is the consequence of a detection of wake-up event by the device. This transition is used to ramp up VCC1 after a wake in a defined way.

**Prerequisites:**

- Device in Sleep Mode
- At least one wake-up source active

**Triggering Events:**

- A wake-up event on CAN, LIN, WKx, Cyclic Sense, Cyclic Wake.
- Bridge driver low-side short circuit detected during overvoltage braking or in parking braking mode.

**Note**

- It is not possible to switch off all wake sources in Sleep Mode. Doing so will set the **SPI_FAIL** flag and will bring the device into Restart Mode.
- RSTN is pulled low during Restart Mode.
- The Restart Mode entry is signalled in the SPI register **DEV_STAT**.
- The wake-up events are flaged in **WK_STAT** register or **DSOV** register.

### 5.5.7 Restart Mode -> Normal Mode

From Restart Mode, the device goes automatically to Normal Mode.

**Prerequisites:**

- Device in Sleep Mode or Fail-Safe Mode

**Triggering Events:**

- Automatic
- Reset is released

**Note**

- The watchdog timer will start with a long open window starting from the moment of the rising edge of RSTN and the watchdog period setting in the register **WD_CTRL** will be changed to the respective default value.

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### 5.5.8 Fail-Safe Mode -> Restart Mode

This transition is similar to device from Sleep Mode to Restart Mode and consequence of a detection of wake-up event by the device. This transition is used to ramp up VCC1 after a wake in a defined way.

**Prerequisites:**

- Device in Fail-Safe Mode

**Triggering Events:**

- A wake-up event on CAN, LIN, WKx, TSD2 (released over temperature TDS2 after $t_{TSD2}$).
- Bridge Driver Low Side short circuit detected during VS/VSINT overvoltage braking mode or in parking braking mode.

*Note: After leaving Fail-Safe Mode, the **FAILURE** bit in **DEV_STAT** register is set and needs to be cleared in order to release the FO pin.*

## 5.6 Reaction on Detected Faults

The device can react at some critical events either signalling the specific failure or changing the device mode. The chapter describes actions taken from the device in case of critical events in particular related the device mode change.

### 5.6.1 Stay in Current State

The following failures will not trigger any device mode changes, but will indicate the failures by an INTN event (depending from the Interrupt Masking) and in dedicated status registers:

- Failures on CAN
- Failures on LIN
- Failures in Bridge Driver and/or Charge Pump
- Failures on HSx

### 5.6.2 Transition into Restart Mode

The Restart Mode can be entered in case of failure as shown in following figure.

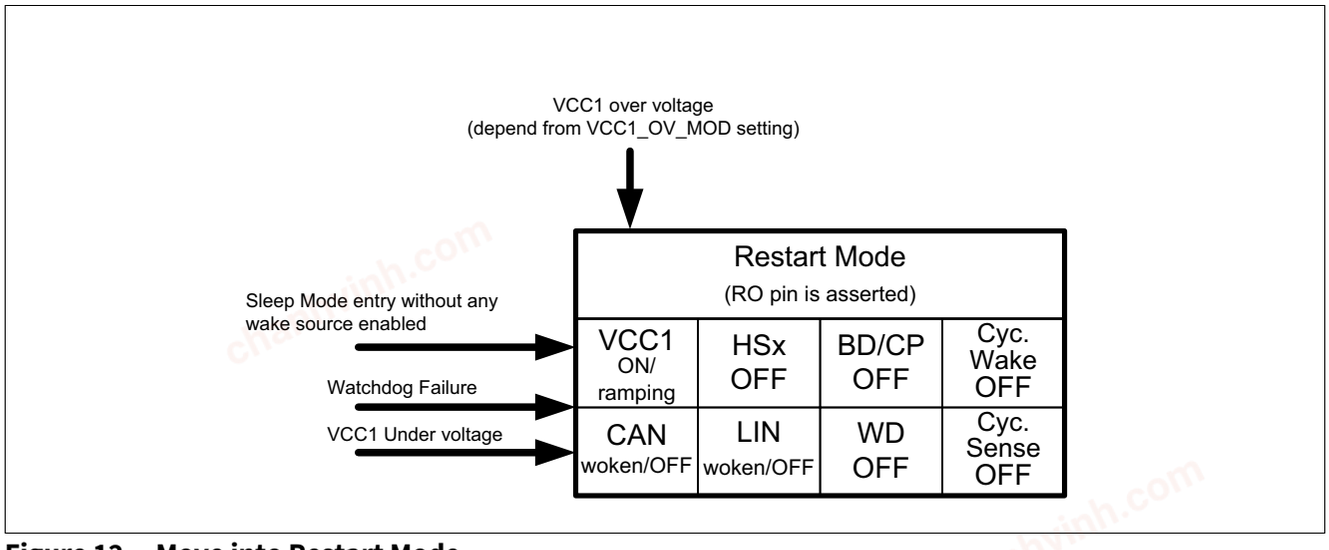



**Figure 12 Move into Restart Mode**

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### System Features

#### Prerequisites

- In case of wake-up event from Sleep Mode or Fail Safe Mode
- In case of Normal Mode
- In case of Stop Mode

#### Trigger Events

- VCC1 Undervoltage in case of Normal Mode or Stop Mode.
- Watchdog trigger failure in case of Normal Mode or Stop Mode.
- VCC1 Overvoltage (based on **VCC1_OV_MOD**) in case of Normal Mode or Stop Mode.
- Sleep Mode entry without any wake-up sources enabled in Normal Mode or Stop Mode.

#### Note

- None

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### 5.6.3 Transition into Fail-Safe Mode

The Fail-Safe Mode can be entered in case of critical event as shown in the following figure.

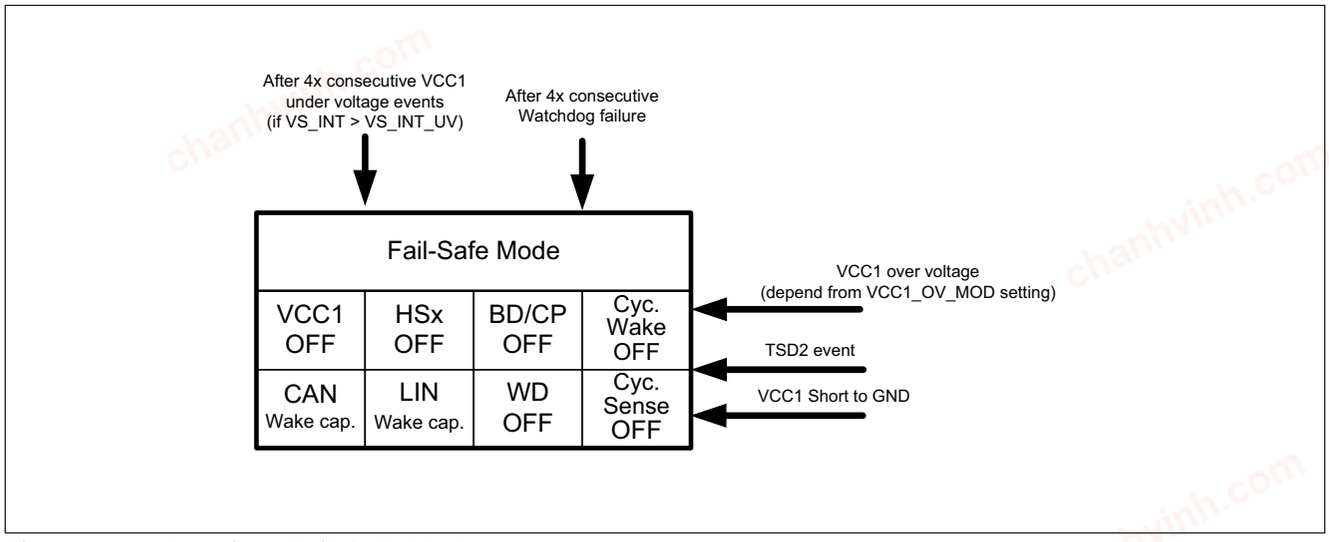



**Figure 13 Move into Fail-Safe Mode**

**Prerequisites:**

- Critical events on VCC1
- Watchdog trigger failures

**Trigger Events:**

- Device thermal shutdown (TSD2) (see also **Chapter 13.10.3**).
- VCC1 is shorted to GND (see also **Chapter 13.8**).
- VCC1 over voltage (based on **VCC1_OV_MOD**).
- 4 consecutive Watchdog trigger failure.
- 4 consecutive VCC1 under voltage events.

**Note**

- The FO/WK2 will be automatically activated if it was before configured as Fail Safe Output (FO).

## 5.7 Wake Features

Following wake sources are implemented in the device:

- Static Sense: WKx inputs are permanently active as wake sources.
- Cyclic Sense: WKx inputs only active during on-time of cyclic sense period. Internal timers are activating HSx during on-time for sensing the WKx inputs.
- Cyclic Wake: wake controlled by internal timers, wake inputs are not used for cyclic wake.
- CAN wake: Wake-up via Bus pattern (refer to **Chapter 8.2.4**).
- LIN wake: Wake-up via Bus messages (refer to **Chapter 9.2.4**).

*Note: Differences of 'cyclic sense' and 'cyclic wake':*
*In both cases a timer is active. With 'cyclic sense' one of the high-side drivers is switched on periodically and supplies some external circuits connected to the WK inputs. For the design, this means that the WK input states are only sampled at the end of the selected HS on-phase which is set*

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*by the corresponding SPI settings for GPIO HS and the timer. 'Cyclic wake' means that the timer is a wake source and thus generates periodic interrupts as long as it is enabled.*

### 5.7.1 Cyclic Sense

The cyclic sense feature is intended to reduce the quiescent current of the device and the application.
In the cyclic sense configuration, one high-side driver is switched on periodically controlled by **TIMER_CTRL** or WK4/SYNC pin. One high-side driver supplies external circuitries e.g. switches and/or resistor arrays, which are connected to one wake input WKx (see **Figure 14**). Any edge change of the WKx input signal during the on-time of the cyclic sense period causes a wake event. Depending on the device mode, either the INTN is pulled low (Normal Mode and Stop Mode) or the device is woken enabling the VCC1 (after Sleep Mode).

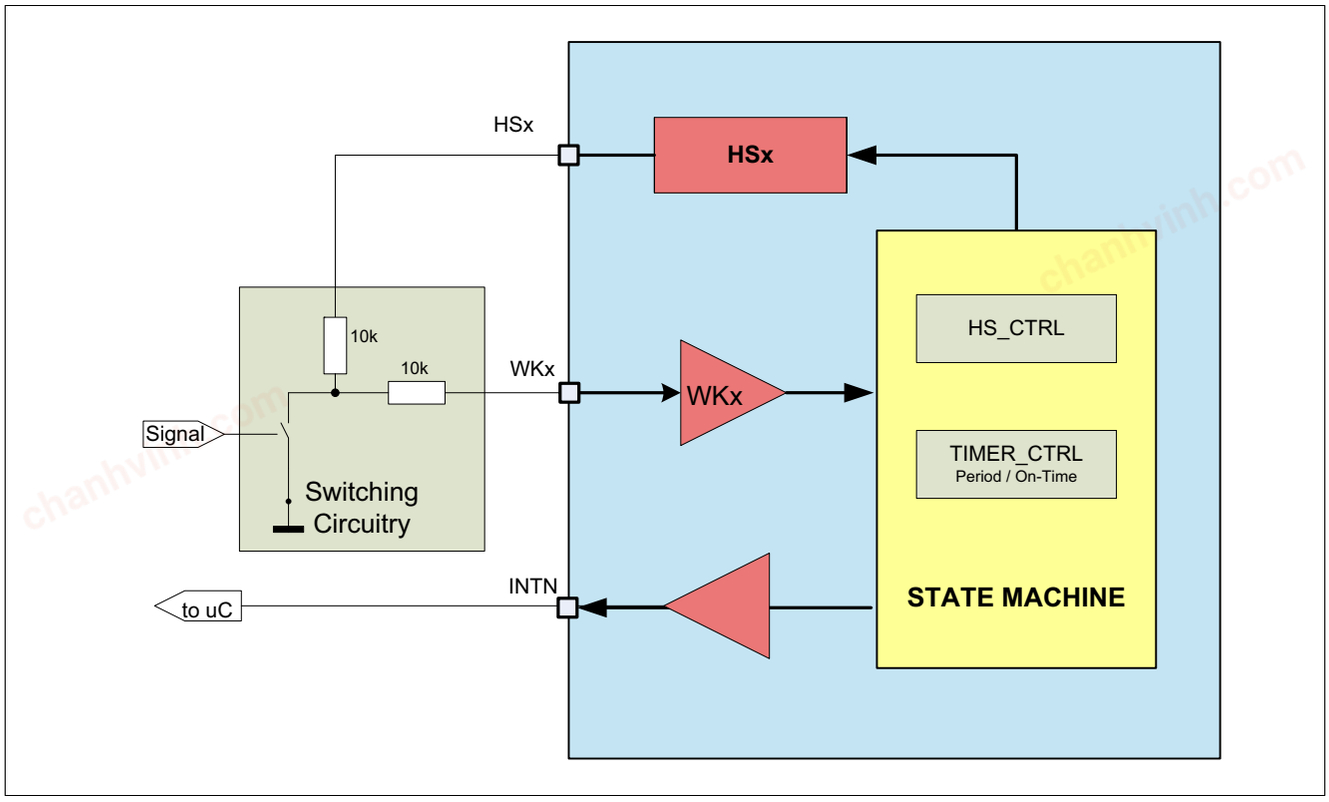



**Figure 14 Cyclic Sense Working Principle**

#### 5.7.1.1 Configuration and Operation of Cyclic Sense

The correct sequence to configure the cyclic sense is shown in **Figure 15**. All the configurations have to be performed before the on-time is set in the **TIMER_CTRL** registers. The settings “OFF / LOW” and “OFF / HIGH” define the voltage level of the respective HS driver before the start of the cyclic sense. The intention of this selection is to avoid an unintentional wake due to a voltage level change at the start of the cyclic sense.

Cyclic Sense will start as soon as the respective on-time has been selected independently from the assignment of the HS and filter configuration. The correct configuration sequence is as follows:

- Configure the initial level.
- Mapping of a Timer to the respective HSx outputs.
- Configuring the respective filter timing and WK pins.
- Configuring the timer period and on-time.

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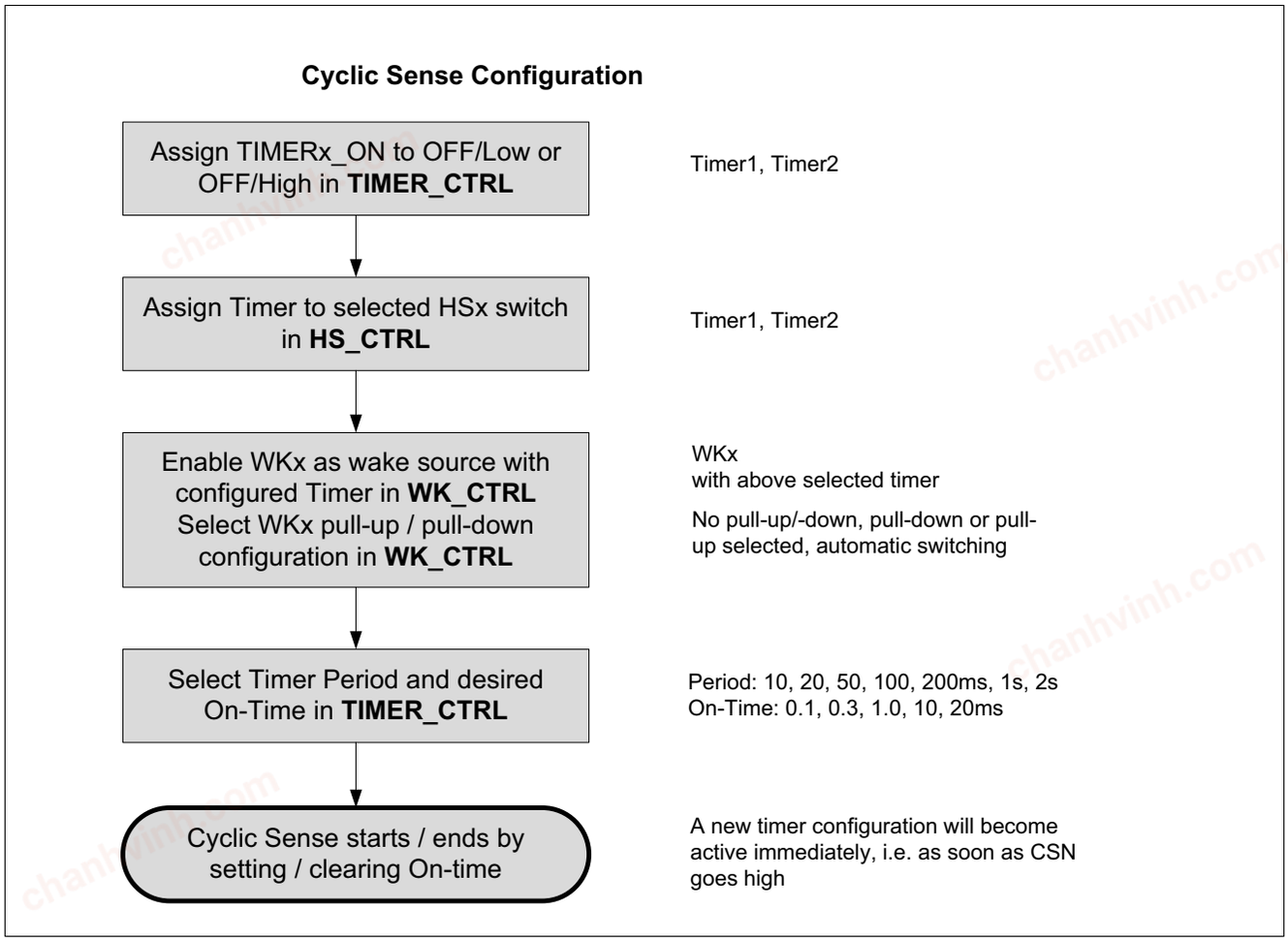



**Figure 15 Cyclic Sense: Configuration and Sequence**

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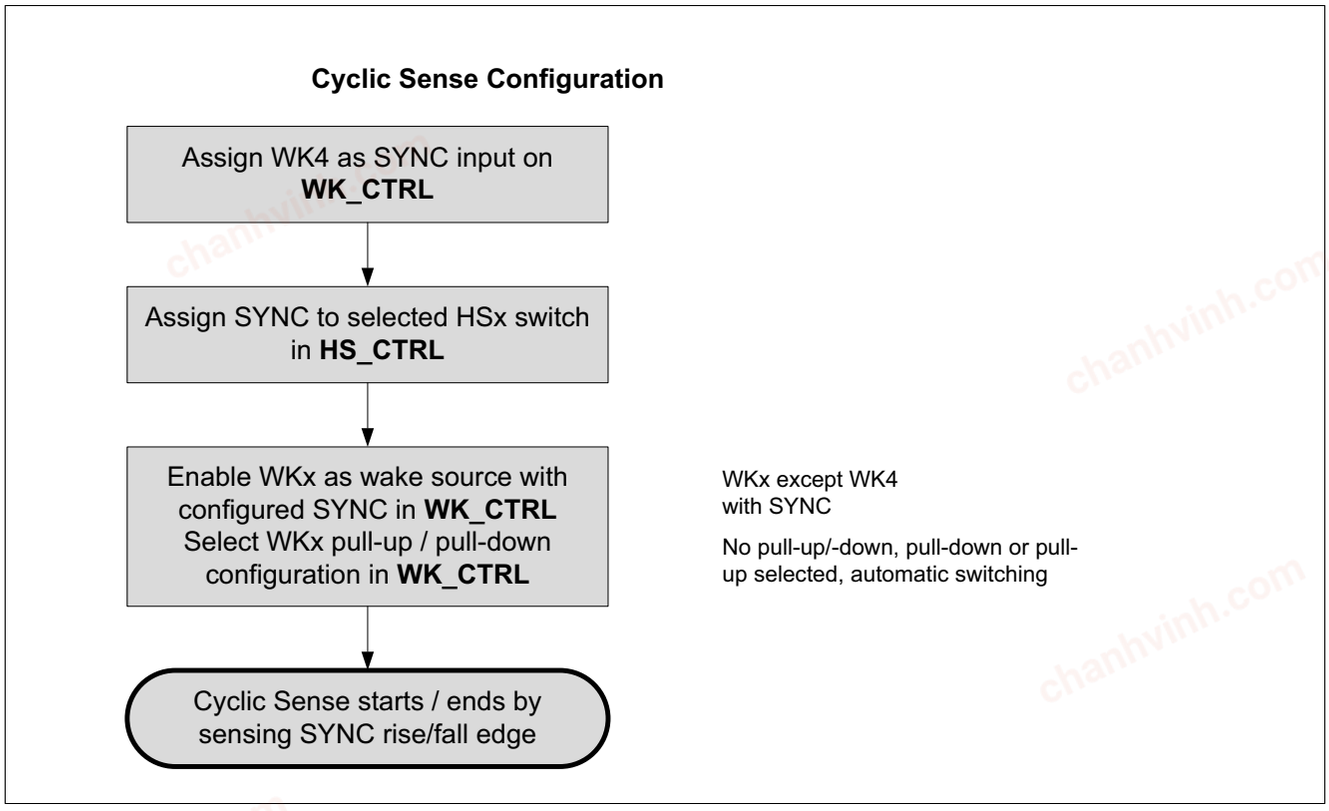



**Figure 16 Cyclic Sense: Configuration and Sequence in case of SYNC usage**

**Note**

- All configurations of period and on-time can be selected. However, recommended on-times for cyclic sense are 0.1ms, 0.3ms and 1ms for quiescent current saving reasons. The **SPI_FAIL** will be set if the on-time is longer than the period.
- If the sequence is not ensured before entering Sleep Mode, then the cyclic sense function might not work properly, e.g. an interrupt could be missed or an unintentional interrupt could be triggered. However, if cyclic sense is the only wake source and it is not configured properly, then Restart Mode will be entered immediately because no valid wake source was set.
- During the HSx on phase in cyclic-sensing, the WKx level is sampled only once (one sample point). In case, a level change will appear during HSx on phase, but before the sampling, as the sampling will happen at the end of the on time, the level change will not be detected and has to wait for the next sensing-cycle.

A wake event caused by cyclic-sensing will also set the corresponding bit WKx_WU.

During Cyclic Sense, **WK_LVL_STAT** is updated only with the sampled voltage levels of the WKx pin in Normal Mode or Stop Mode.

The functionality of the sampling and different scenarios are depicted in **Figure 17** to **Figure 19**. The behavior in Stop Mode and Sleep Mode is identical except that in Normal Mode and Stop Mode INTN will be triggered to signal a change of WKx input level and in Sleep Mode, VCC1 will power-up instead. A wake event will be triggered regardless if the bit WKx_WU is already set.

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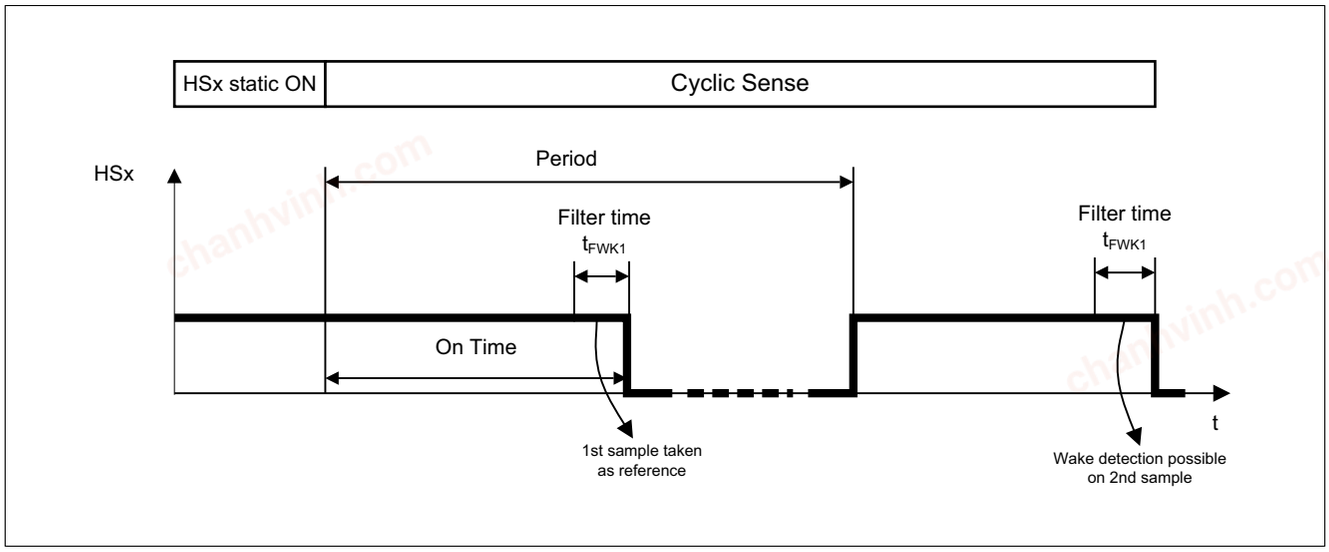



**Figure 17 Cyclic Sense Timing**

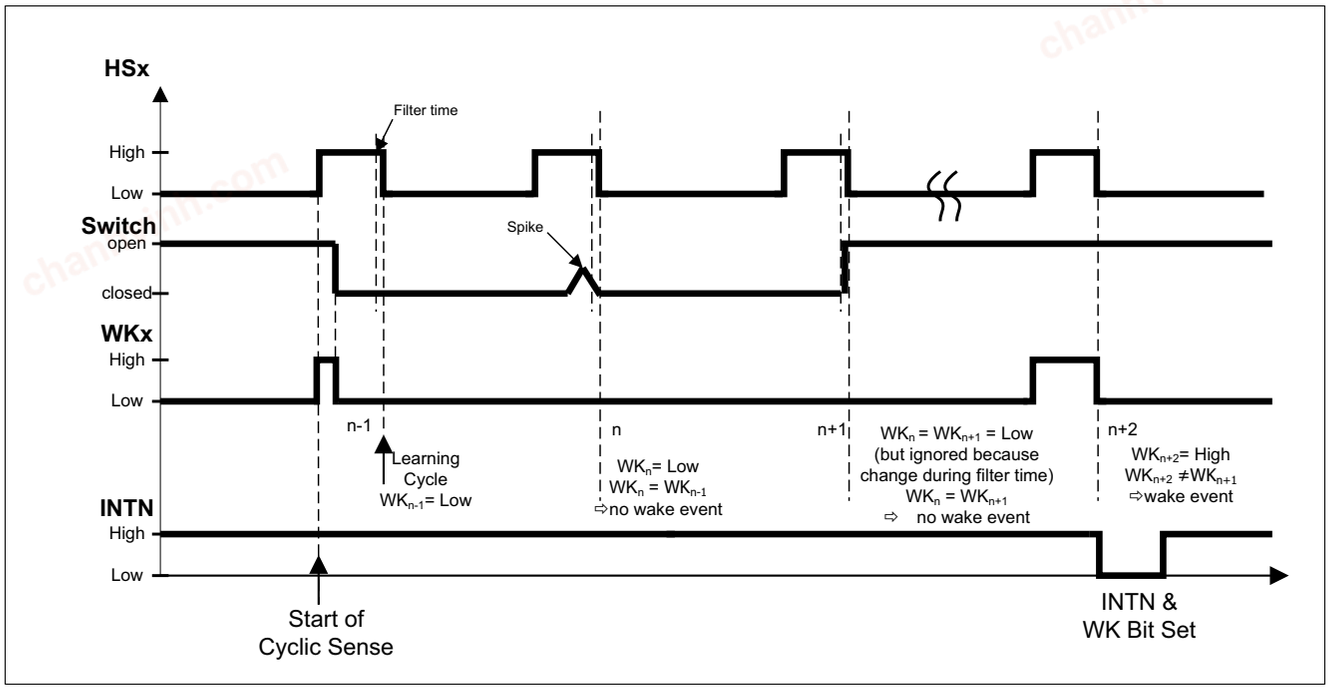



**Figure 18 Cyclic Sense Example Timing for Stop Mode, HSx starts LOW, GND based WKx input**

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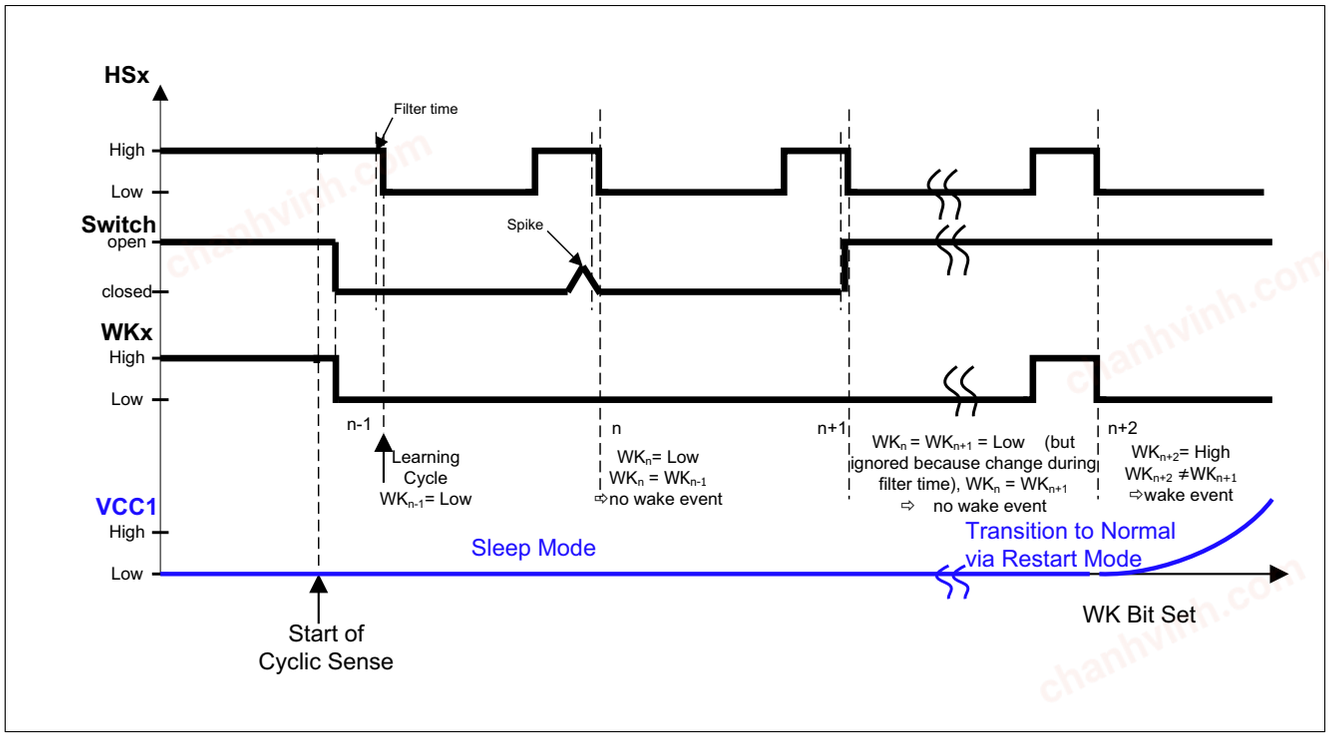



**Figure 19 Cyclic Sense Example Timing for Sleep Mode, HSx starts with ON, GND based WKx input**

The cyclic sense function will be disabled in case of following conditions:

- in case Fail-Safe Mode is entered, the HSx switch will be disabled and the WKx pin will be changed to static sensing. An unintended wake-up event could be triggered when the WKx input is changed to static sensing.
- In Normal Mode, Stop Mode, or Sleep Mode in case of an overcurrent, or overtemperature, or under- or overvoltage event, the respective HS switch will be disabled.

### 5.7.1.2 Cyclic Sense in Low-power Mode

If cyclic sense is intended for Stop Mode or Sleep Mode, it is necessary to activate cyclic sense in Normal Mode before going to the low-power mode. A wake event due to cyclic sense will set the bit WKx_WU. In Stop Mode a wake event will trigger an interrupt, in Sleep Mode the wake event will send the device via Restart Mode to Normal Mode.

Before returning to Sleep Mode, the wake status registers **WK_STAT** and **DSOV** must be cleared. Trying to go to Sleep Mode with uncleared wake flags will lead to a direct wake-up from Sleep Mode by going via Restart Mode to Normal Mode and triggering of RSTN.

## 5.7.2 Cyclic Wake

For the cyclic wake feature one timer is configured as internal wake-up source and will periodically trigger an interrupt on INTN in Normal Mode and Stop Mode. During Sleep Mode, the timer triggers and wakes up the device again. The device enters via Restart Mode the Normal Mode.

The correct sequence to configure the cyclic wake is shown in **Figure 20**. The sequence is as follows:

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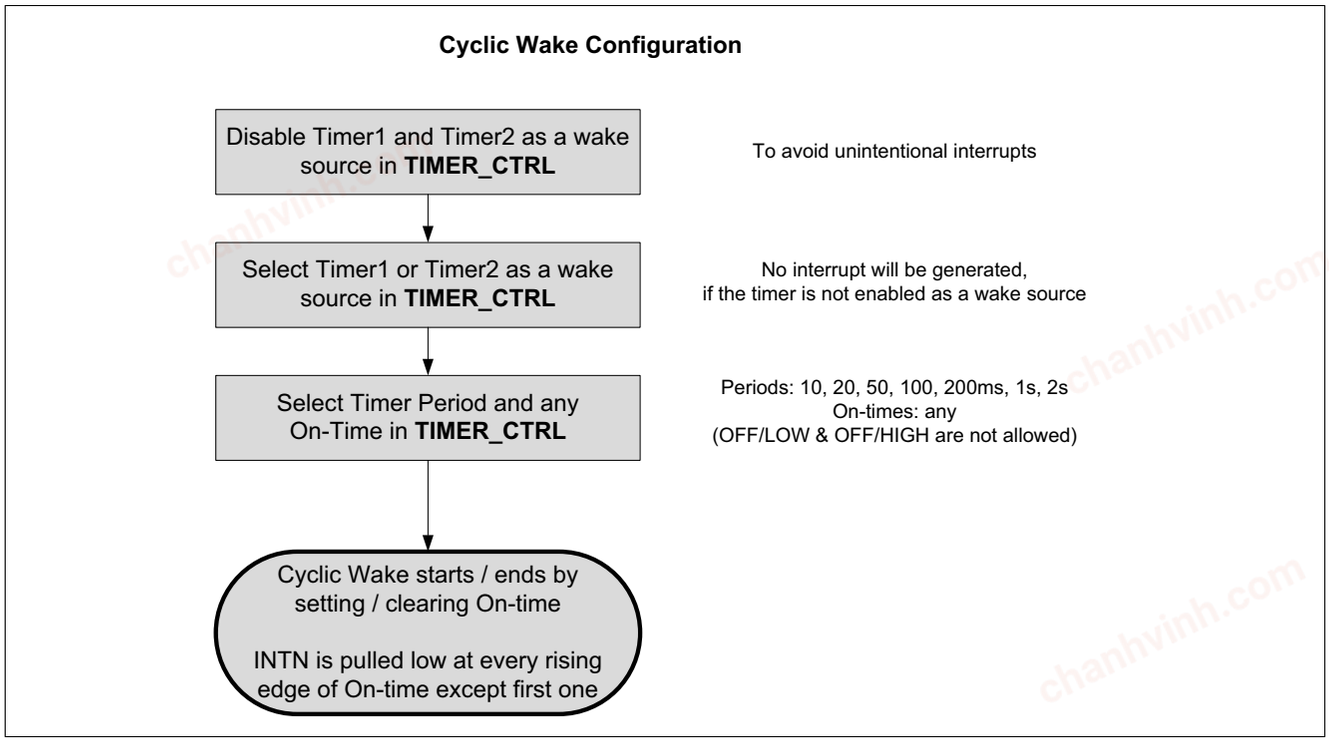



**Figure 20 Cyclic Wake: Configuration and Sequence**

*Note: The on-time is only used to enable the cyclic wake function regardless of the value of the on time, i.e. the on time value has no meaning to the cyclic wake function as long as it is not '000' or '110' or '111'.*

As in cyclic sense, the cyclic wake function will start as soon as the on-time is configured. An interrupt is generated for every start of the on-time except for the very first time when the timer is started.

### 5.7.3 Internal Timers

Two integrated timers can be used to control the below features:

- Cyclic Wake, i.e. to wake up the microcontroller periodically in Normal Mode, Stop Mode and Sleep Mode.
- Cyclic Sense, i.e. to perform cyclic sensing using the wake input WKx and the HSx by mapping the timer accordingly via the **HS_CTRL** register.

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## 5.8 VS Supply Multiplexing

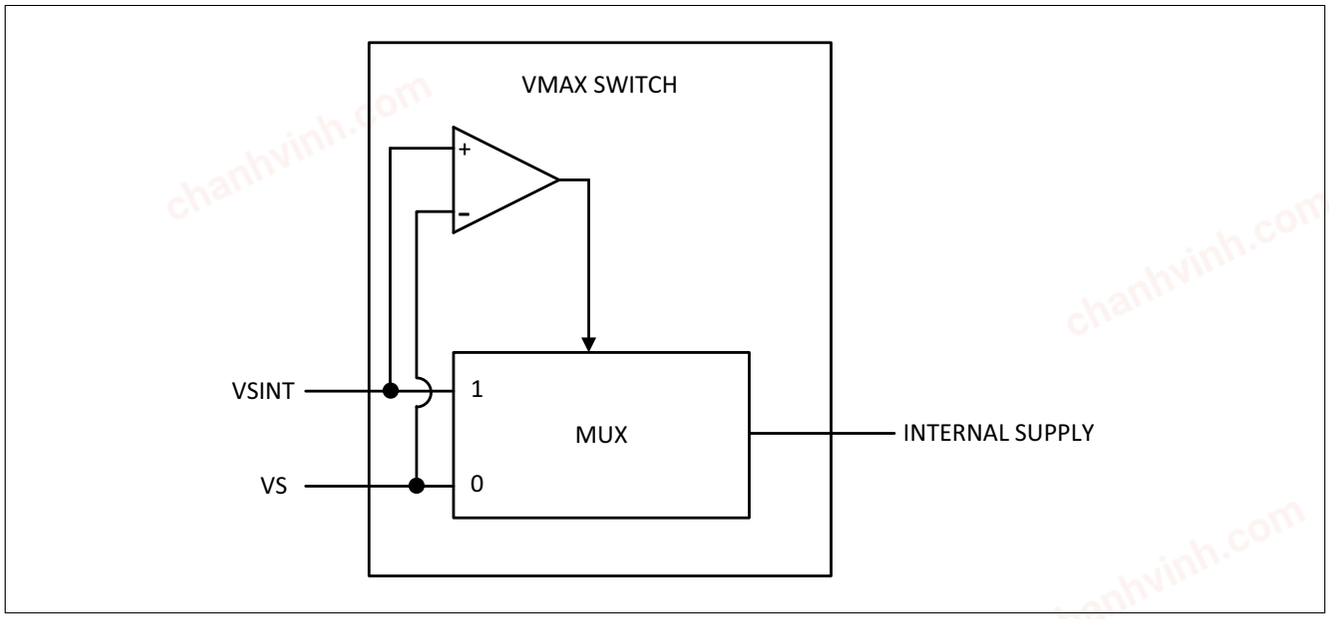



**Figure 21 VS Supply Multiplexing**

The internal supply voltage is multiplexed from VSINT and VS, choosing continuously the larger of both. In case of transient low VBAT, the buffered supply voltage takes over the internal supply, avoiding loss of power.

*Note: Only the internal digital logic of the device is supplied by the VMAX SWITCH. In case of a power loss of either VS or VSINT, the internal register values will not be lost.*

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# 6 Voltage Regulator 1

## 6.1 Block Description

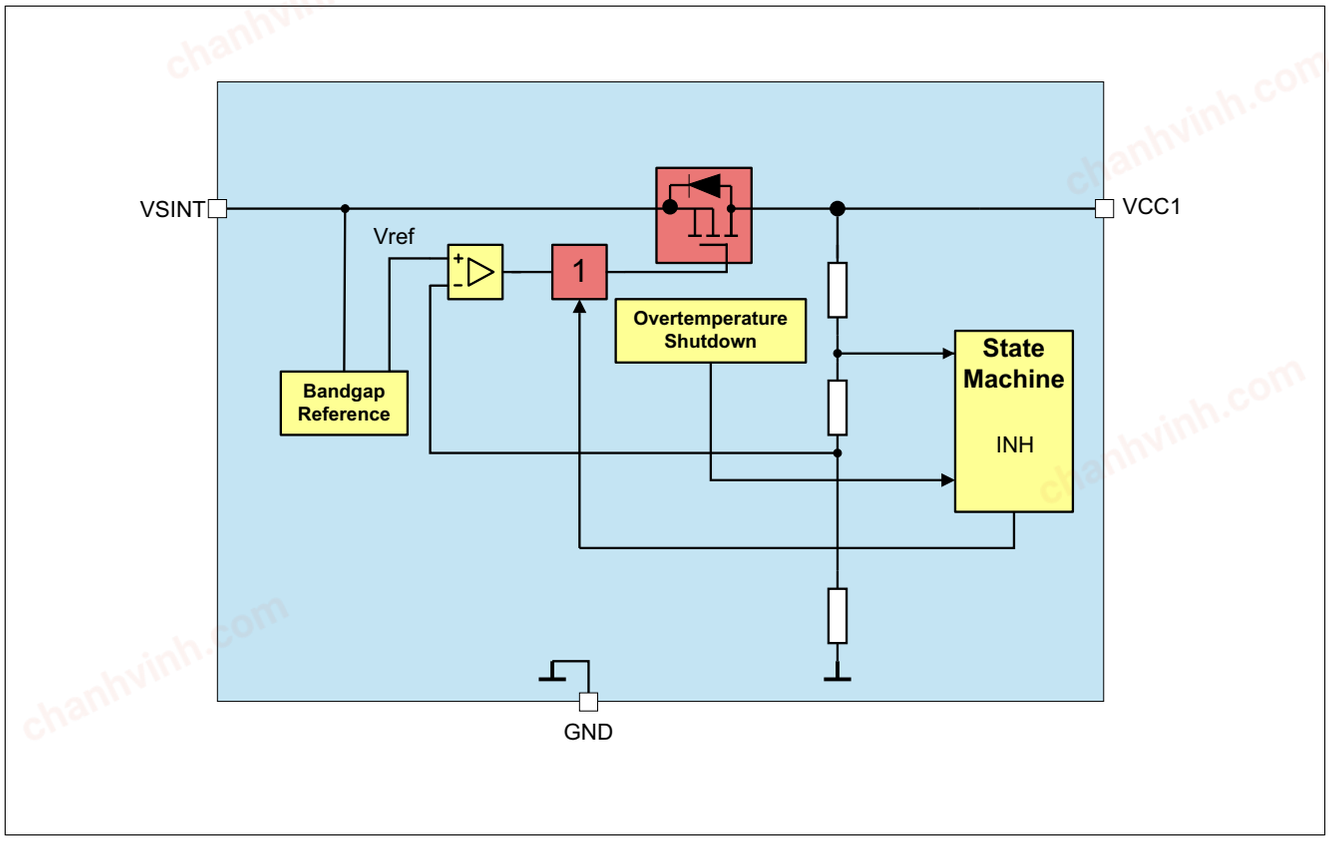



**Figure 22 Module Block Diagram**

### Functional Features

- 5 V low-drop voltage regulator.
- Undervoltage monitoring with adjustable reset level and VCC1 undervoltage prewarning (refer to **Chapter 13.7** and **Chapter 13.8** for more information).
- Short circuit detection and switch off with undervoltage fail threshold, device enters Fail-Safe Mode.
- Effective capacitance must be ≥ 1 µF at nominal voltage output for stability. A 2.2 µF ceramic capacitor (MLCC) is recommended for best transient response.
- Output current capability up to $I_{VCC1,lim}$.

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## 6.2 Functional Description

The Voltage Regulator 1 (=VCC1) is “ON” in Normal Mode and Stop Mode and is disabled in Sleep Mode and in Fail-Safe Mode. The regulator can provide an output current up to $I_{VCC1,lim}$.

For low-quiescent current reasons, the output voltage tolerance is decreased in Stop Mode because only the less accurate low-power mode regulator will be active for small loads. If the load current on VCC1 exceeds the selected threshold ($I_{VCC1,Ipeak1,r}$ or $I_{VCC1,Ipeak2,r}$) then the high-power mode regulator will be also activated to support an optimum dynamic load behavior. The current consumption will then increase (approx. 2.8 mA additional quiescent current). The device mode stays unchanged.
If the load current on VCC1 falls below the selected threshold ($I_{VCC1,Ipeak1,f}$ or $I_{VCC1,Ipeak2,f}$), then the low-quiescent current mode is resumed again by disabling the high-power mode regulator.
Both regulators (low-power mode and high-power mode) are active in Normal Mode.

Two different active peak thresholds can be selected via SPI:

- **I_PEAK_TH** = ‘0’(default): the lower VCC1 active peak threshold 1 is selected with lowest quiescent current consumption in Stop Mode.
- **I_PEAK_TH** = ‘1’: the higher VCC1 active peak threshold 2 is selected with an increased quiescent current consumption in Stop Mode.

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## 6.3 Electrical Characteristics

### Table 12 Electrical Characteristics

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Output Voltage including Line and Load Regulation | $V_{CC1,out1}$ | 4.9 | 5.0 | 5.1 | V | [1]Normal Mode; 10 µA < $I_{VCC1}$ < 150 mA; | P_6.3.1 |
| Output Voltage including Line and Load Regulation (Full Load Current Range) | $V_{CC1,out2}$ | 4.9 | 5.0 | 5.1 | V | [1]Normal Mode; 6 V < $V_{SINT}$ < 28 V; 10 µA < $I_{VCC1}$ < 250 mA | P_6.3.2 |
| Output Voltage including Line and Load Regulation (Higher Accuracy Rage) | $V_{CC1,out3}$ | 4.95 | – | 5.05 | V | [2]Normal Mode; 20 mA < $I_{VCC1}$ < 80 mA; 8 V < $V_{SINT}$ < 18 V; 25°C < $T_j$ < 150°C | P_6.3.3 |
| Output Voltage including Line and Load Regulation (low-power mode) | $V_{CC1,out4}$ | 4.9 | 5.05 | 5.2 | V | Stop Mode; 10 µA < $I_{VCC1}$ < $I_{VCC1,Ipeak}$ | P_6.3.4 |
| Output Drop Voltage | $V_{CC1,d1}$ | – | 200 | 400 | mV | $I_{VCC1}$ = 50 mA, $V_{SINT}$ = 5 V | P_6.3.9 |
| Output Drop Voltage | $V_{CC1,d2}$ | – | 300 | 500 | mV | $I_{VCC1}$ = 150 mA, $V_{SINT}$ = 5 V | P_6.3.10 |
| VCC1 Active Peak Threshold 1 (Transition threshold between low-power and high-power mode regulator) | $I_{VCC1,Ipeak1,r}$ | – | 3.25 | 5.0 | mA | [2] $I_{CC1}$ rising; $V_{SINT}$ = 13.5 V; **I_PEAK_TH** = '0' | P_6.3.17 |
| VCC1 Active Peak Threshold 1 (Transition threshold between high-power and low-power mode regulator) | $I_{VCC1,Ipeak1,f}$ | 1.2 | 1.7 | – | mA | [2] $I_{CC1}$ falling; $V_{SINT}$ = 13.5V; **I_PEAK_TH** = '0' | P_6.3.18 |
| VCC1 Active Peak Threshold 2 (Transition threshold between low-power and high-power mode regulator) | $I_{VCC1,Ipeak2,r}$ | 6 | – | 20 | mA | [2] $I_{CC1}$ rising; $V_{SINT}$ = 13.5 V; **I_PEAK_TH** = '1' | P_6.3.19 |
| VCC1 Active Peak Threshold 2 (Transition threshold between high-power and low-power mode regulator) | $I_{VCC1,Ipeak2,f}$ | 5 | – | 15 | mA | [2] $I_{CC1}$ falling; $V_{SINT}$ = 13.5V; **I_PEAK_TH** = '1' | P_6.3.20 |
| Overcurrent Limitation | $I_{VCC1,lim}$ | 260 | 360 | 500 | mA | current following out of pin, VCC1= 0V [2] | P_6.3.21 |

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**Table 12 Electrical Characteristics** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Minimum Output Capacitance for stability | $C_{VCC1,min}$ | 1[3] | – | – | µF | [2] | P_6.3.22 |
| Maximum Output Capacitance | $C_{VCC1,max}$ | – | – | 47 | µF | [2] | P_6.3.23 |

1) In Stop Mode, the specified output voltage tolerance applies when $I_{VCC1}$ has exceeded the selected active peak threshold ($I_{VCC1,Ipeak1,r}$ or $I_{VCC1,Ipeak2,r}$) but with increased current consumption.
2) Not subject to production test, specified by design.
3) Value is meant to be an effective value at rated output voltage level.

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# 7 High-Side Switch

## 7.1 Block Description

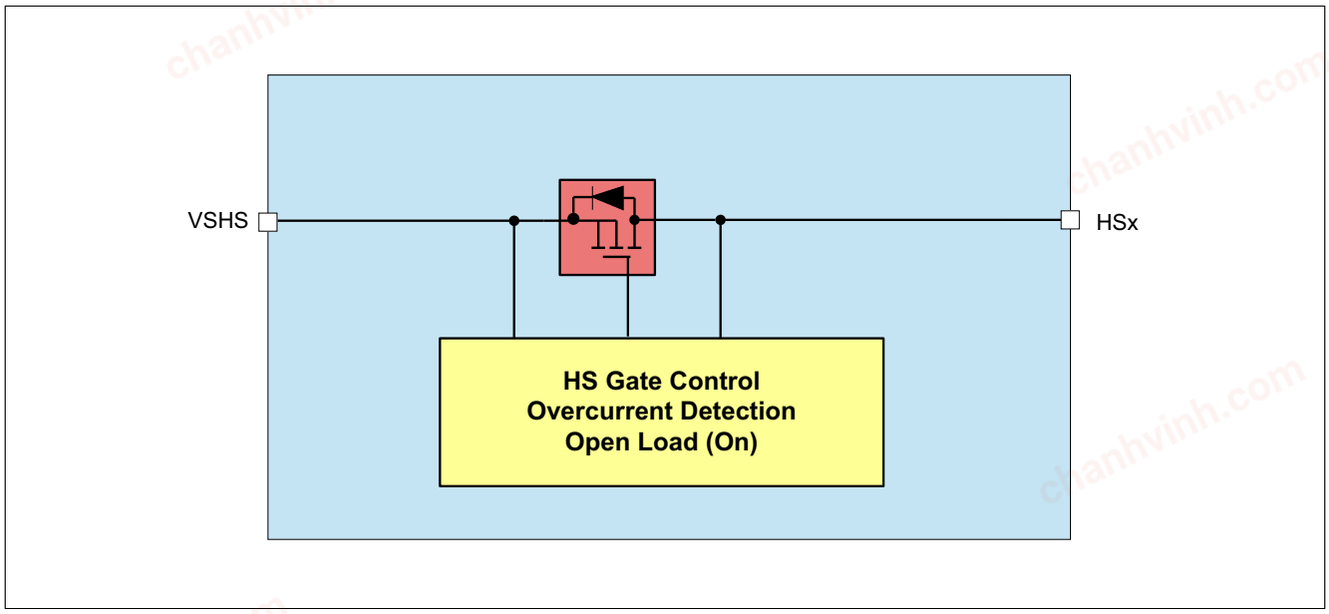



**Figure 23 High-Side Module Block Diagram**

**Features**

- All HSx supplied by VSHS
- Under voltage switch off configurable via SPI.
- Dedicated over voltage switch off per each HSx in Normal Mode- configurable via SPI.
- Overvoltage switch off in Stop Mode and Sleep Mode- configurable via SPI.
- Overcurrent detection and switch off.
- Open load detection in ON-state.
- PWM capability with internal or external timers configurable via SPI.
- Switch recovery after removal of OV or UV condition configurable via SPI.

## 7.2 Functional Description

The High-Side switches can be used for control of LEDs, as supply for the wake inputs and for other loads (except inductive load). The High-Side outputs can be controlled either directly via SPI by the integrated timers or by the integrated PWM generators or by external sync signal (using WK4/SYNC pin).

The high-side outputs are supplied by VSHS pin. The topology supports improved cranking condition behavior.

The configuration of the High-Sides (Permanent On, PWM, cyclic sense, etc.) drivers must be done in Normal Mode. The configuration is taken over in Stop Mode or Sleep Mode and cannot be modified. When entering Restart Mode or Fail-Safe Mode the HSx outputs are disabled.

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### 7.2.1 Under Voltage Switch Off

All HS drivers in on-state are switched off in case of under voltage on VSHS. The feature can be disabled by setting the SPI bit **HS_UV_SD_DIS** .

After release of under voltage condition, the HSx switch goes back to programmed state in which it was configured via SPI. This behavior is only valid if the bit **HS_UV_REC** is set. Otherwise the switches will stay off and the respective SPI control bits are cleared.
The under voltage is signaled in the bit **HS_UV**, no other error bits are set.

### 7.2.2 Over Voltage Switch Off

The HS drivers in on-state are switched off in case of over voltage on VSHS.. In Normal Mode the HSx can be kept in on-state above the VSHS overvoltage threshold if the HSx_OV_SDN_DIS bit is set.

In Stop Mode or Sleep Modes all HS drivers can be kept in on-state if **HS_OV_SDS_DIS** bit is set.

When the HSx are configured to switch off in case of over voltage condition, after release of over voltage condition, the HS switch goes back to programmed state in which it was configured via SPI. This behavior is only valid if the respective bit HSx_OV_REC is set. Otherwise the switch will stay off and the respective SPI control bits are cleared. This configuration is available for each HSx.
The over voltage is signaled in the bit **HS_OV**, no other error bits are set.

### 7.2.3 Over Current Detection and Switch Off

If the load current exceeds the over current shutdown threshold for a time longer then the over current shutdown filter time the output is switched off.

The over current condition and the switch off is signaled with the respective HSx_OC_OT bit in the register **HS_OL_OC_OT_STAT**. The HSx configuration is then reset to 000 by the device. To activate the High-Side again the HSx configuration has to be set to ON (001) or be programmed to a timer function. It is recommended to clear the over current bit before activation the High-Side switch, as the bits are not cleared automatically by the device.

### 7.2.4 Open Load Detection

Open load detection on the High-Side outputs is done during on state of the output. If the current in the activated output falls below the open load detection current threshold, the open load is detected and signaled via the respective bit HS1_OL, HS2_OL, HS3_OL, or HS4_OL in the register **HS_OL_OC_OT_STAT**. The High-Side output stays activated.. If the open load condition disappears the Open Load bit in the SPI can be cleared. The bits are not cleared automatically by the device.

### 7.2.5 PWM, Timer and SYNC Function

Each integrated HSx can be configured in different ways, in particular:

- Static OFF
- Static ON
- Timer 1
- Timer 2
- Internal generator PWM1
- Internal generator PWM2
- Internal generator PWM3
- Internal generator PWM4

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- SYNC (via WK4)

*Note: PWMx mentioned in this chapter refer to the internal PWM generators, which are configured by the registers **HS_CTRL** and **PWM_CTRL**. They can be used to control the internal high-side switches HSx.*

*Note: PWMx mentioned in this chapter **do not refer** to the PWMx pins. The PWMx pins are used for the PWM operation of the bridge drivers, to control the external MOSFETs.*

### Static configuration (ON/OFF)

This configuration set the HSx permanently ON or OFF. This configuration is available in Normal Mode, Stop Mode and Sleep Mode.

The configuration shall be done via SPI.

### Timer configuration (TIMER1 or TIMER2)

Two Timers are dedicated to control the ON phase of dedicated HS outputs.

The Timers are mapped to the dedicated HS outputs. Period and the duty cycle can be independently configured with via SPI.

### PWM configuration (PWM1..PWM4)

Several internal PWM generators are dedicated to generate a PWM signal on the HSx output, e.g. for brightness adjustment or compensation of supply voltage fluctuation. The PWM generators are mapped to the dedicated HS outputs, and the duty cycle can be independently configured with a 10-bit resolution via SPI (**PWM_CTRL**). Two different frequencies can be selected independently for every PWM generator in the register **PWM_CTRL**.

In order to assign and configure the PWMx to specific HSX, the follow steps have to be followed:

- Configure duty cycle and frequency for respective PWM generator in **PWM_CTRL**.
- Assign PWM generator to respective HS switch(es) in HSx_CTRL.
- The PWM generation will start right after the HSx is assigned to the PWM generator (**HS_CTRL**) .

*Note: The min. on-time during PWM is limited by the actual on- and off-time of the respective HS switch, e.g. the PWM setting '00 0000 0001' could not be realized.*

### SYNC configuration (using WK4)

Another possible configuration is to use the WK4 (set as SYNC pin) and mapped to one dedicated HSx output.

The configuration of the WK4/SYNC bit is done using the **WK_EN** bits. If the **WK_EN**=$10_B$ (SYNC selected), all bits in WK4 bank are ignored and wake-up capability on WK4 is not available.

Only after the WK4/SYNC configuration, the HSx can be configured for SYNC usage (HSx = $1000_B$).

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## 7.3 Electrical Characteristics

**Table 13 Electrical Characteristics**

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Output HS1, HS2, HS3, HS4** | | | | | | | |
| Static Drain-Source ON Resistance HSx | $R_{ON,HS25}$ | – | 7 | – | Ω | $I_{ds}$ = 60 mA, $T_j$ < 25°C | P_7.3.1 |
| Static Drain-Source ON Resistance HSx | $R_{ON,HS150}$ | – | 11.5 | 16 | Ω | $I_{ds}$ = 60 mA, $T_j$ < 150°C | P_7.3.2 |
| Leakage Current HSx / per channel | $I_{leak,HS}$ | – | – | 2 | µA | 1) 0 V < $V_{HSx}$ < $V_{S_HS}$; $T_j$ < 85°C | P_7.3.3 |
| Output Slew Rate (rising) | $SR_{raise,HS}$ | 0.8 | – | 2.5 | V/µs | 1) 20 to 80% $V_{SHS}$ = 6 to 18 V $R_L$ = 220 Ω | P_7.3.4 |
| Output Slew Rate (falling) | $SR_{fall,HS}$ | -2.5 | – | -0.8 | V/µs | 1) 80 to 20% $V_{SHS}$ = 6 to 18 V $R_L$ = 220 Ω | P_7.3.5 |
| Switch-on time HSx | $t_{ON,HS}$ | 3 | – | 30 | µs | CSN = HIGH to 0.8 × VSHS; $R_L$ = 220 Ω; $V_{SHS}$ = 6 to 18 V | P_7.3.6 |
| Switch-off time HSx | $t_{OFF,HS}$ | 3 | – | 30 | µs | CSN = HIGH to 0.2 × VSHS; $R_L$ = 220 Ω; $V_{SHS}$ = 6 to 18 V | P_7.3.7 |
| Short Circuit Shutdown Current | $I_{SD,HS}$ | 150 | 245 | 300 | mA | $V_{SHS}$ = 6 to 20 V | P_7.3.8 |
| Short Circuit Shutdown Filter Time | $t_{SD,HS}$ | 12 | 16 | 22 | µs | 2) | P_7.3.9 |
| Open Load Detection Current | $I_{OL,HS}$ | 0.4 | – | 2 | mA | hysteresis included | P_7.3.10 |
| Open Load Detection hysteresis | $I_{OL,HS,hys}$ | – | 0.45 | – | mA | 1) | P_7.3.11 |
| Open Load Detection Filter Time | $t_{OL,HS}$ | 160 | 220 | 270 | µs | 2) | P_7.3.12 |

1) Not subject to production test, specified by design.

2) Not subject to production test, tolerance defined by internal oscillator tolerance.

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# 8 High Speed CAN Transceiver

## 8.1 Block Description

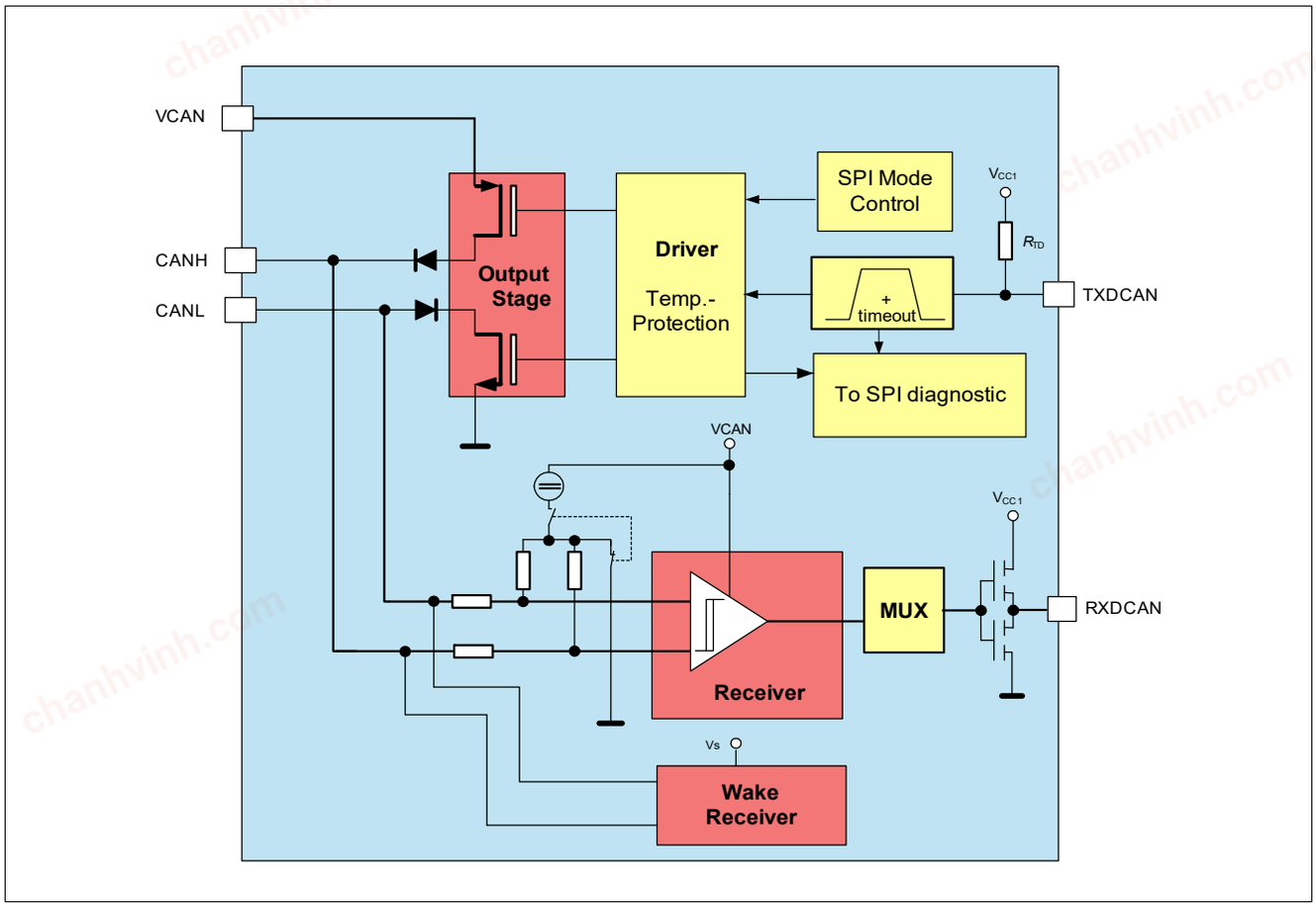



**Figure 24 Functional Block Diagram**

## 8.2 Functional Description

The Controller Area Network (CAN) transceiver part of the device provides High-Speed (HS) differential mode data transmission (up to 2 Mbaud/s) and reception in automotive and industrial applications. It works as an interface between the CAN protocol controller and the physical bus lines compatible to ISO11898-2:2016 and SAE J2284.

The CAN FD transceiver offers low-power modes to reduce current consumption. This supports networks with partially powered down nodes. To support software diagnostic functions, a CAN Receive Only Mode is implemented.

It is designed to provide excellent passive behavior when the transceiver is switched off (mixed networks, clamp 15/30 applications).

A wake-up from the CAN Wake Capable Mode is possible via a message on the bus. Thus, the microcontroller can be powered down or idled and is woken up by the CAN bus activities.

The CAN transceiver is designed to withstand the severe conditions of automotive applications and to support 12 V applications.

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The transceiver can also be configured to Wake Capable in order to save current and to ensure a safe transition from Normal Mode to Sleep Mode (to avoid loosing messages).

**Figure 25** shows the possible transceiver mode transition when changing the device mode.

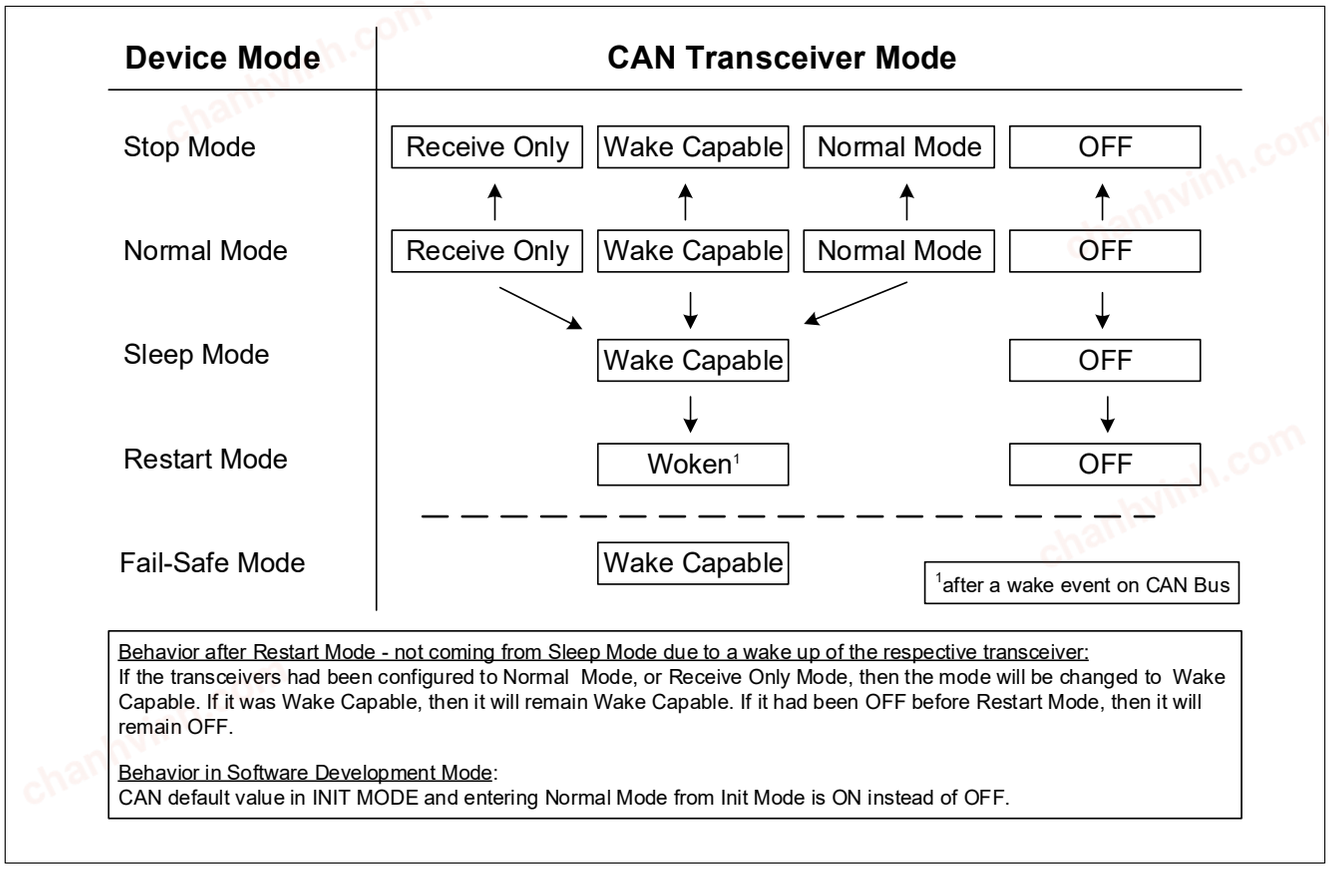



**Figure 25 CAN Mode Control Diagram**

### CAN FD Support

CAN FD stands for 'CAN with Flexible Data Rate'. It is based on the well established CAN protocol as specified in ISO11898-2:2016. CAN FD still uses the CAN bus arbitration method. The benefit is that the bit rate can be increased by switching to a shorter bit time at the end of the arbitration process and then to return to the longer bit time at the CRC delimiter, before the receivers transmit their acknowledge bits. See also **Figure 26**. In addition, the effective data rate is increased by allowing longer data fields. CAN FD allows the transmission of up to 64 data bytes compared to the 8 data bytes from the standard CAN.

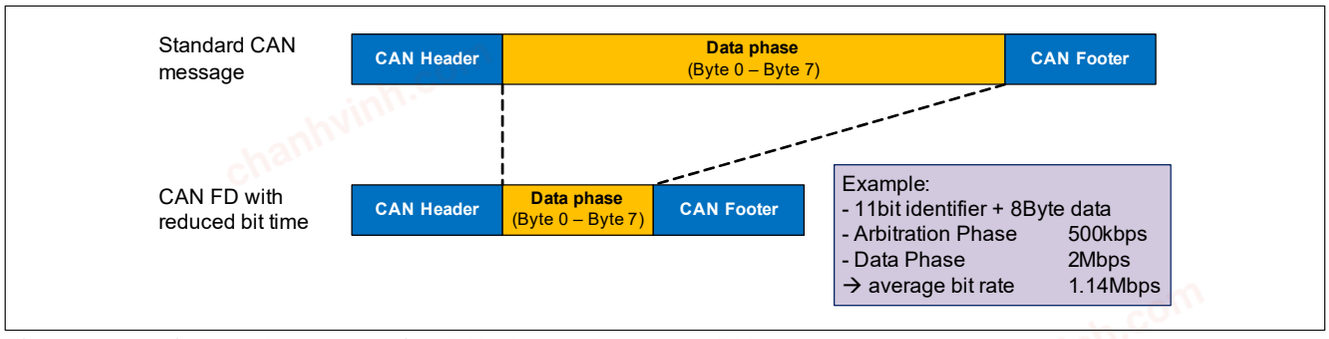



**Figure 26 Bit Rate Increase with CAN FD vs. Standard CAN**

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Not only the physical layer must support CAN FD but also the CAN controller. In case the CAN controller is not able to support CAN FD then the respective CAN node must at least tolerate CAN FD communication. This CAN FD tolerant mode is realized in the physical layer.

### 8.2.1 CAN OFF Mode

The CAN OFF Mode is the default mode after power-up of the device. It is available in all device modes and is intended to completely stop CAN activities or when CAN communication is not needed. In CAN OFF Mode, a wake-up event on the bus will be ignored.

### 8.2.2 CAN Normal Mode

The CAN Transceiver is enabled via SPI in Normal Mode. CAN Normal Mode is designed for normal data transmission/reception within the HS-CAN network. The mode is available in Normal Mode and in Stop Mode. The bus biasing is set to VCAN/2.

**Transmission**

The signal from the microcontroller is applied to the TXDCAN input of the device. The bus driver switches the CANH/L output stages to transfer this input signal to the CAN bus lines.

**Enabling sequence**

The CAN transceiver requires an enabling time $t_{CAN,EN}$ before a message can be sent on the bus. This means that the TXDCAN signal can only be pulled low after the enabling time. If this is not ensured, then the TXDCAN needs to be set back to high (=recessive) until the enabling time is completed. Only the next dominant bit will be transmitted on the bus. **Figure 27** shows different scenarios and explanations for CAN enabling.

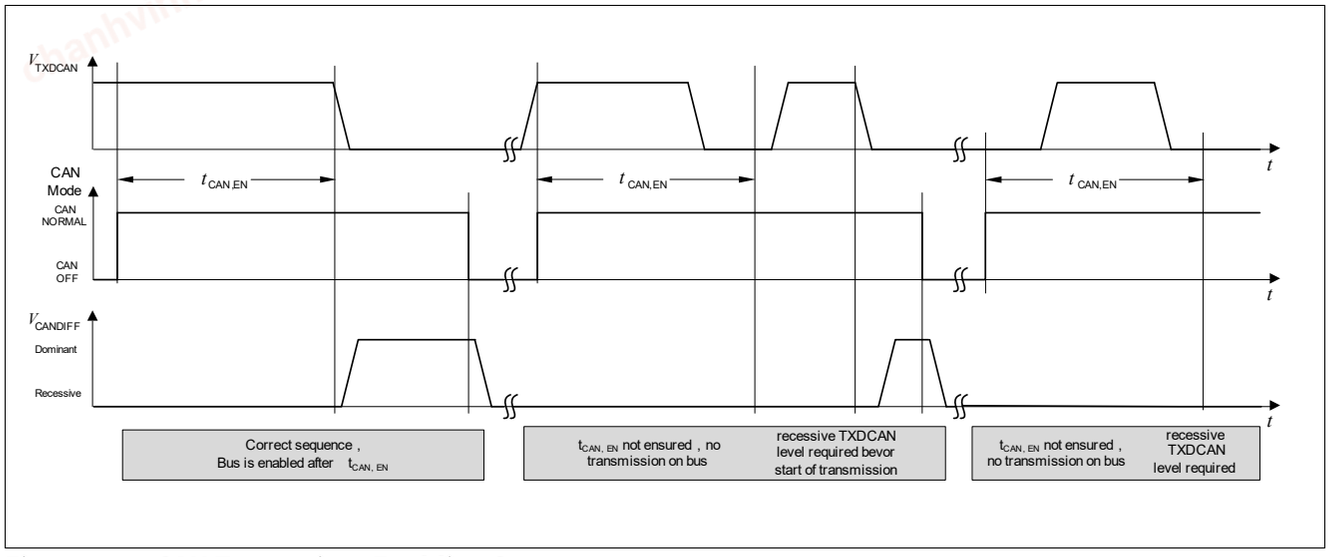



**Figure 27 CAN Transceiver Enabling Sequence**

**Reduced Electromagnetic Emission**

To reduce electromagnetic emissions (EME), the bus driver controls CANH/L slopes symmetrically.

**Reception**

Analog CAN bus signals are converted into digital signals at RXDCAN via the differential input receiver.

### 8.2.3 CAN Receive Only Mode

In CAN Receive Only Mode (RX only), the driver stage is de-activated but reception is still operational. This mode is accessible by an SPI command in Normal Mode and in Stop Mode.

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*Note: The transceiver is still properly working in CAN Receive Only Mode even if VCAN is not available because of an independent receiver supply.*

### 8.2.4 CAN Wake Capable Mode

This mode can be used in Stop Mode, Sleep Mode, Restart Mode and Normal Mode by programming via SPI and it is used to monitor bus activities. It is automatically accessed in Fail-Safe Mode. A wake-up signal on the bus results in a change of behavior of the device, as described in **Table 14**. As a signalization to the microcontroller, the RXDCAN pin is set low and will stay low until the CAN transceiver is changed to any other mode. After a wake-up event, the transceiver can be switched to CAN Normal Mode via SPI for bus communication.

As shown in **Figure 28**, a wake-up pattern (WUP) is signaled on the bus by two consecutive dominant bus levels for at least $t_{Wake1}$ (wake-up time) and less than $t_{Wake2}$, each separated by a recessive bus level of greater than $t_{Wake1}$ and shorter than $t_{Wake2}$.

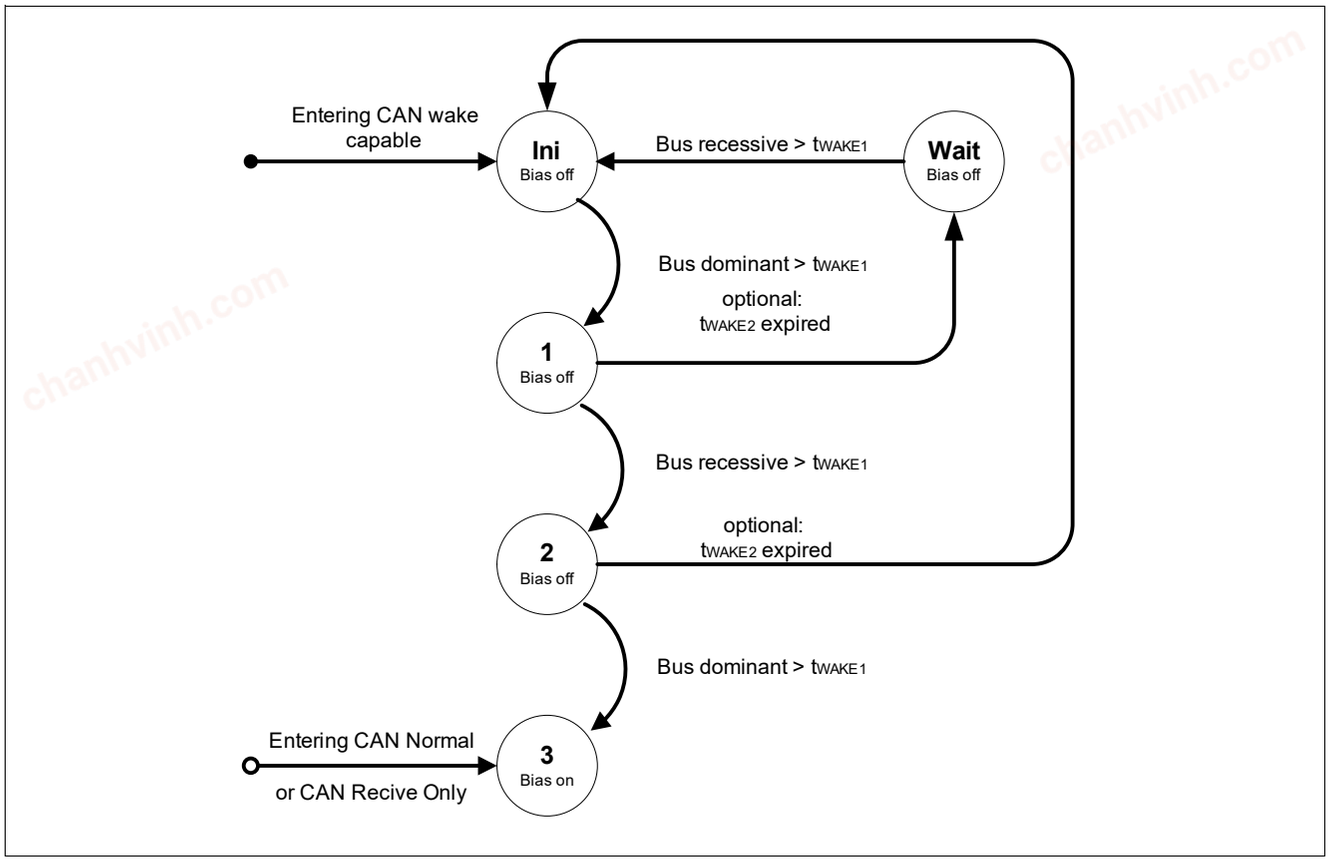



**Figure 28 CAN Wake-up Pattern Detection according to the Definition in ISO11898-2:2016**

**Rearming the Transceiver for Wake Capability**

After a BUS wake-up event, the transceiver is woken. However, the **CAN** transceiver mode bits will still show wake capable (=‘01’) so that the RXDCAN signal will be pulled low. There are two possibilities how the CAN transceiver’s wake capable mode is enabled again after a wake-up event:

- The CAN transceiver mode must be toggled, i.e. switched from CAN Wake Capable Mode to CAN Normal Mode, CAN Receive Only Mode or CAN OFF Mode, before switching to CAN Wake Capable Mode again.
- Rearming is done automatically when the device is changed to Stop Mode, Sleep Mode or Fail-Safe Mode to ensure wake-up capability.

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**Wake-Up in Stop Mode and Normal Mode**

In Stop Mode, if a wake-up is detected, it is always signaled by the INTN output and in the **WK_STAT** SPI register. It is also signaled by RXDCAN pulled to low. The same applies for the Normal Mode. The microcontroller should set the device from Stop Mode to Normal Mode, there is no automatic transition to Normal Mode.

For functional safety reasons, the watchdog will be automatically enabled in Stop Mode after a bus wake-up event in case it was disabled before (if bit **WD_EN_ WK_BUS** was configured to high before).

**Wake-Up in Sleep Mode**

Wake-up is possible via a CAN message. The wake-up automatically transfers the device into the Restart Mode and from there to Normal Mode the corresponding RXDCAN pin is set to low. The microcontroller is able to detect the low signal on RXDCAN and to read the wake source out of the **WK_STAT** register via SPI. No interrupt is generated when coming out of Sleep Mode. The microcontroller can now for example switch the CAN transceiver into CAN Normal Mode via SPI to start communication.

**Table 14 Action due to CAN Bus Wake-Up**

| Mode | Mode after Wake | VCC1 | INTN | RXDCAN |
|---|---|---|---|---|
| Normal Mode | Normal Mode | On | Low | Low |
| Stop Mode | Stop Mode | On | Low | Low |
| Sleep Mode | Restart Mode | Ramping Up | High | Low |
| Restart Mode | Restart Mode | On | High | Low |
| Fail-Safe Mode | Restart Mode | Ramping Up | High | Low |

### 8.2.5 CAN Bus termination

In accordance with the CAN configuration, four types of bus terminations are allow:

- CAN Normal Mode: VCAN/2 termination.
- CAN Receive Only Mode: VCAN/2 termination in case that VCAN is nominal supply. when VCAN UV is detected, the termination is 2.5 V.
- CAN Wake Capable Mode: GND termination: after wake-up, the termination is 2.5 V.
- CAN OFF Mode: no termination necessary (bus floating).

When entering CAN Wake Capable Mode the termination is only connected to GND after the t_silence time has expired.

### 8.2.6 TXD Time-out Feature

If the TXDCAN signal is dominant for a time $t > t_{TXDCAN_TO}$, in CAN Normal Mode, the TXDCAN time-out function deactivates the transmission of the signal at the bus setting the TXDCAN pin to recessive. This is implemented to prevent the bus from being blocked permanently due to an error. The transmitter is disabled and thus switched to recessive state. The CAN SPI control bits (**CAN** on **BUS_CTRL**) remain unchanged and the failure is stored in the SPI flag **CAN_FAIL**. The CAN transmitter stage is activated again after the dominant time-out condition is removed and the transceiver is automatically switched back to CAN Normal Mode.

### 8.2.7 Bus Dominant Clamping

If the CAN bus is dominant for a time $t > t_{BUS_CAN_TO}$, when CAN is configured as CAN Normal Mode or CAN Receive Only Mode, a bus dominant clamping is detected and the SPI bit **CAN_FAIL** is set. The transceiver configuration stays unchanged. In order to avoid that a bus dominant clamping is detected due to a TXD time-out the bus dominant clamping filter time $t_{BUS_CAN_TO} > t_{TXDCAN_TO}$.

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### 8.2.8 Undervoltage Detection

The voltage at the CAN supply pin is monitored in CAN Normal Mode and CAN Receive Only Mode. In case of VCAN undervoltage a signalization via SPI bit **VCAN_UV** is triggered and the TLE9562QX disables the transmitter stage. If the CAN supply reaches a higher level than the undervoltage detection threshold (VCAN > **VCAN_UV**), the transceiver is automatically switched back to CAN Normal Mode.

The undervoltage detection is enabled if the mode bit CAN_1 = '1', i.e. in CAN Normal or CAN Receive Only Mode. .

## 8.3 Electrical Characteristics

**Table 15 Electrical Characteristics**

$T_j$ = -40°C to +150°C; $V_{SINT}$ = 5.5 V to 28 V; $V_{CAN}$ = 4.75 V to 5.25 V; RL = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **CAN Bus Receiver** | | | | | | | |
| Differential Receiver Threshold Voltage, recessive to dominant edge | $V_{diff,rd_N}$ | – | 0.80 | 0.90 | V | $V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ $V_{CM}$(CAN) ≤ 12 V; CAN Normal Mode | P_8.3.1 |
| Differential Receiver Threshold Voltage, dominant to recessive edge | $V_{diff,dr_N}$ | 0.50 | 0.60 | – | V | $V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ $V_{CM}$(CAN) ≤ 12 V; CAN Normal Mode | P_8.3.2 |
| Dominant state differential input voltage range | $V_{diff_D_range}$ | 0.9 | – | 8.0 | V | $V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ VCM(CAN) ≤ +12 V; CAN Normal Mode | P_8.3.60 |
| Common Mode Range | CMR | -12 | – | 12 | V | 4) | P_8.3.3 |
| Recessive state differential input voltage range | $V_{diff_R_range}$ | -3.0 | – | 0.5 | V | $V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ VCM(CAN) ≤ +12 V; CAN Normal Mode | P_8.3.61 |
| Maximum Differential Bus Voltage | $V_{diff,max}$ | -5 | – | 10 | V | 4) | P_8.3.4 |
| CANH, CANL Input Resistance | $R_i$ | 20 | 40 | 50 | kΩ | CAN Normal / Wake Capable Mode; Recessive state -2V ≤ $V_{CANH/L}$ ≤ +7V | P_8.3.5 |
| Differential Input Resistance | $R_{diff}$ | 40 | 80 | 100 | kΩ | CAN Normal / Wake Capable Mode; Recessive state -2V ≤ $V_{CANH/L}$ ≤ +7V | P_8.3.6 |
| Input Resistance Deviation between CANH and CANL | $DR_i$ | -3 | – | 3 | % | 4)Recessive state $V_{CANH} = V_{CANL}$ = 5V | P_8.3.7 |

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**Table 15 Electrical Characteristics** (cont'd)

$T_j$ = -40°C to +150°C; $V_{SINT}$ = 5.5 V to 28 V; $V_{CAN}$ = 4.75 V to 5.25 V; RL = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Input Capacitance CANH, CANL versus GND | $C_{in}$ | – | 20 | 40 | pF | [1] $V_{TXDCAN}$ = 5 V | P_8.3.8 |
| Differential Input Capacitance | $C_{diff}$ | – | 10 | 20 | pF | [1] $V_{TXDCAN}$ = 5 V | P_8.3.9 |
| Wake-up Receiver Threshold Voltage, recessive to dominant edge | $V_{diff, rd_W}$ | – | 0.8 | 1.15 | V | -12 V ≤ $V_{CM}$(CAN) ≤ 12 V; CAN Wake Capable Mode | P_8.3.10 |
| Wake-up Receiver Dominant state differential input voltage range | $V_{diff,D_range_W}$ | 1.15 | – | 8.0 | V | -12 V ≤ $V_{CM}$(CAN) ≤ +12 V; CAN Wake Capable Mode | P_8.3.62 |
| Wake-up Receiver Threshold Voltage, dominant to recessive edge | $V_{diff, dr_W}$ | 0.4 | 0.7 | | V | -12 V ≤ $V_{CM}$(CAN) ≤ 12 V; CAN Wake Capable Mode | P_8.3.11 |
| Wake-up Receiver Recessive state differential input voltage range | $V_{diff,R_range_W}$ | -3.0 | – | 0.4 | V | -12 V ≤ $V_{CM}$(CAN) ≤ +12 V; CAN Wake Capable Mode | P_8.3.63 |
| **CAN Bus Transmitter** | | | | | | | |
| CANH/CANL Recessive Output Voltage (CAN Normal Mode) | $V_{CANL/H_NM}$ | 2.0 | – | 3.0 | V | CAN Normal Mode $V_{TXDCAN}$ = $V_{cc1}$; no load | P_8.3.12 |
| CANH/CANL Recessive Output Voltage (CAN Wake Capable Mode) | $V_{CANL/H_LP}$ | -0.1 | – | 0.1 | V | CAN Wake Capable Mode; $V_{TXDCAN}$ = $V_{cc1}$; no load | P_8.3.13 |
| CANH, CANL Recessive Output Voltage Difference $V_{diff}$ = $V_{CANH}$ - $V_{CANL}$ (CAN Normal Mode) | $V_{diff_r_N}$ | -500 | – | 50 | mV | CAN Normal Mode; $V_{TXDCAN}$ = $V_{cc1}$; no load | P_8.3.14 |
| CANH, CANL Recessive Output Voltage Difference $V_{diff}$ = $V_{CANH}$ - $V_{CANL}$ (CAN Wake Capable Mode) | $V_{diff_r_W}$ | -200 | – | 200 | mV | CAN Wake Capable Mode; $V_{TXDCAN}$ = $V_{cc1}$; no load | P_8.3.15 |
| CANL Dominant Output Voltage | $V_{CANL}$ | 0.5 | – | 2.25 | V | [4] CAN Normal Mode; $V_{TXDCAN}$ = 0 V; $V_{CAN}$ = 5 V; 50 Ω ≤ $R_L$ ≤ 65 Ω | P_8.3.16 |

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**Table 15 Electrical Characteristics** (cont'd)

$T_j$ = -40°C to +150°C; $V_{SINT}$ = 5.5 V to 28 V; $V_{CAN}$ = 4.75 V to 5.25 V; RL = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| CANH Dominant Output Voltage | $V_{CANH}$ | 2.75 | – | 4.5 | V | 4)CAN Normal Mode; $V_{TXDCAN}$ = 0 V; $V_{CAN}$ = 5 V; 50 Ω ≤ $R_L$ ≤ 65 Ω | P_8.3.17 |
| CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$ | $V_{diff_d_N}$ | 1.5 | 2.0 | 2.5 | V | 4)CAN Normal Mode; $V_{TXDCAN}$ = 0 V; $V_{CAN}$ = 5 V; 50 Ω ≤ $R_L$ ≤ 65 Ω | P_8.3.18 |
| CANH, CANL Dominant Output Voltage Difference (resistance during arbitration) $V_{diff} = V_{CANH} - V_{CANL}$ | $V_{diff_d_N}$ | 1.5 | – | 5.0 | V | 4)CAN Normal Mode; $V_{TXDCAN}$ = 0 V; $V_{CAN}$ = 5 V; $R_L$ = 2240 Ω | P_8.3.19 |
| CANH, CANL output voltage difference slope, recessive to dominant | $V_{diff_slope_rd}$ | – | – | 70 | V/us | 4)30% to 70% of measured differential bus voltage, $C_L$ = 100 pF, $R_L$ = 60 Ω | P_8.3.54 |
| CANH, CANL output voltage difference slope, dominant to recessive | $V_{diff_slope_dr}$ | – | – | 70 | V/us | 4)70% to 30% of measured differential bus voltage, $C_L$ = 100 pF, $R_L$ = 60 Ω | P_8.3.55 |
| Driver Symmetry $V_{SYM} = V_{CANH} + V_{CANL}$ | $V_{SYM}$ | 4.5 | – | 5.5 | V | 2)CAN Normal Mode; $V_{TXDCAN}$ = 0 V / 5 V; $V_{CAN}$ = 5 V; $C_{SPLIT}$ = 4.7 nF; 50 Ω ≤ $R_L$ ≤ 60 Ω; | P_8.3.21 |
| CANH Short Circuit Current | $I_{CANHsc}$ | -115 | -80 | -50 | mA | CAN Normal Mode; $V_{CANHshort}$ = -3 V | P_8.3.22 |
| CANL Short Circuit Current | $I_{CANLsc}$ | 50 | 80 | 115 | mA | CAN Normal Mode; $V_{CANLshort}$ = 18 V; | P_8.3.23 |
| Leakage Current | $I_{CANH,lk}$ $I_{CANL,lk}$ | – | 5 | 7.5 | µA | $V_S = V_{CAN}$ = 0 V; 0 V ≤ $V_{CANH,L}$ ≤ 5 V; 3)$R_{test}$ = 0 / 47kΩ | P_8.3.24 |
| **Receiver Output RXDCAN** | | | | | | | |
| High level Output Voltage | $V_{RXDCAN,H}$ | 0.8 × $V_{CC1}$ | – | – | V | CAN Normal Mode; $I_{RXDCAN}$ = -2 mA | P_8.3.26 |
| Low Level Output Voltage | $V_{RXDCAN,L}$ | – | – | 0.2 × $V_{cc1}$ | V | CAN Normal Mode; $I_{RXDCAN}$ = 2 mA | P_8.3.27 |

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**Table 15 Electrical Characteristics** (cont'd)

$T_j$ = -40°C to +150°C; $V_{SINT}$ = 5.5 V to 28 V; $V_{CAN}$ = 4.75 V to 5.25 V; RL = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Transmission Input TXDCAN** | | | | | | | |
| High Level Input Voltage Threshold | $V_{TXDCAN,H}$ | – | – | 0.7 × $V_{cc1}$ | V | CAN Normal Mode; recessive state | P_8.3.28 |
| Low Level Input Voltage Threshold | $V_{TXDCAN,L}$ | 0.3 × $V_{cc1}$ | – | – | V | CAN Normal Mode; dominant state | P_8.3.29 |
| TXDCAN Input Hysteresis | $V_{TXDCAN,hys}$ | – | 0.12 × $V_{cc1}$ | – | V | 4) | P_8.3.30 |
| TXDCAN Pull-up Resistance | $R_{TXDCAN}$ | 20 | 50 | 80 | kΩ | - | P_8.3.31 |
| TXDCAN input capacitance | $C_{TXDCAN}$ | – | 6 | 10 | pF | 4) | P_8.3.64 |
| CAN Transceiver Enabling Time | $t_{CAN,EN}$ | 8 | 12 | 18 | µs | 6) CSN = high to first valid transmitted TXDCAN dominant | P_8.3.32 |
| **Dynamic CAN-Transceiver Characteristics** | | | | | | | |
| Min. Dominant Time for Bus Wake-up | $t_{Wake1}$ | 0.5 | – | 1.8 | µs | -12 V ≤ $V_{CM}$(CAN) ≤ 12 V; CAN Wake Capable Mode | P_8.3.33 |
| Wake-up Time-out, Recessive Bus | $t_{Wake2}$ | 0.8 | – | 10 | ms | 6)CAN Wake Capable Mode | P_8.3.34 |
| Loop delay (recessive to dominant) | $t_{LOOP,f}$ | – | 150 | 255 | ns | 2)CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω; $V_{CAN}$ = 5 V; $C_{RXDCAN}$ = 15 pF | P_8.3.35 |
| Loop delay (dominant to recessive) | $t_{LOOP,r}$ | – | 150 | 255 | ns | 2)CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω; $V_{CAN}$ = 5 V; $C_{RXDCAN}$ = 15 pF | P_8.3.36 |
| Propagation Delay TXDCAN low to bus dominant | $t_{d(L),T}$ | – | 50 | 140 | ns | CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω; $V_{CAN}$ = 5 V | P_8.3.37 |
| Propagation Delay TXDCAN high to bus recessive | $t_{d(H),T}$ | – | 50 | 140 | ns | CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω; $V_{CAN}$ = 5 V | P_8.3.38 |

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**Table 15 Electrical Characteristics** (cont'd)

$T_j$ = -40°C to +150°C; $V_{SINT}$ = 5.5 V to 28 V; $V_{CAN}$ = 4.75 V to 5.25 V; RL = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Propagation Delay bus dominant to RXDCAN low | $t_{d(L),R}$ | – | 100 | – | ns | CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω; $V_{CAN}$ = 5 V; $C_{RXDCAN}$ = 15 pF | P_8.3.39 |
| Propagation Delay bus recessive to RXDCAN high | $t_{d(H),R}$ | – | 100 | – | ns | CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω; $V_{CAN}$ = 5 V; $C_{RXDCAN}$ = 15 pF | P_8.3.40 |
| Received Recessive bit width | $t_{bit(RXD)}$ | 400 | – | 550 | ns | CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω ; $V_{CAN}$ = 5 V; $C_{RXDCAN}$ = 15 pF; $t_{bit(TXD)}$ = 500 ns; Parameter definition in according to **Figure 30**. | P_8.3.42 |
| Transmitted Recessive bit width | $t_{bit(BUS)}$ | 435 | – | 530 | ns | CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω; $V_{CAN}$ = 5 V; $C_{RXDCAN}$ = 15 pF; $t_{bit(TXD)}$ = 500 ns; Parameter definition in according to **Figure 30**. | P_8.3.43 |
| Receiver timing symmetry[5)] | $\Delta t_{Rec}$ | -65 | – | 40 | ns | CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω; $V_{CAN}$ = 5 V; $C_{RXDCAN}$ = 15 pF; $t_{bit(TXD)}$ = 500 ns; Parameter definition in according to **Figure 30**. | P_8.3.44 |

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**Table 15 Electrical Characteristics** (cont'd)

$T_j$ = -40°C to +150°C; $V_{SINT}$ = 5.5 V to 28 V; $V_{CAN}$ = 4.75 V to 5.25 V; RL = 60 Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Received Recessive bit width | $t_{bit(RXD)}$ | 120 | – | 220 | ns | CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω ; $V_{CAN}$ = 5 V; $C_{RXDCAN}$ = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 30**. | P_8.3.45 |
| Transmitted Recessive bit width | $t_{bit(BUS)}$ | 155 | – | 210 | ns | CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω; $V_{CAN}$ = 5 V; $C_{RXDCAN}$ = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 30**. | P_8.3.46 |
| Receiver timing symmetry Δt Rec = t_bit(RXD) - t_bit(Bus) | $\Delta t_{Rec}$ | -45 | – | 15 | ns | CAN Normal Mode; $C_L$ = 100 pF; $R_L$ = 60 Ω; $V_{CAN}$ = 5 V; $C_{RXDCAN}$ = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 30**. | P_8.3.47 |
| TXDCAN Permanent Dominant Time-out | $t_{TXDCAN_TO}$ | 1.6 | 2.0 | 2.4 | ms | [6)]CAN Normal Mode | P_8.3.48 |
| BUS Permanent Dominant Time-out | $t_{BUS_CAN_TO}$ | 2.0 | 2.5 | 3.0 | ms | [6)]CAN Normal Mode | P_8.3.49 |
| Timeout for bus inactivity | $t_{SILENCE}$ | 0.6 | – | 1.2 | s | [6)] | P_8.3.50 |
| Bus Bias reaction time | $t_{Bias}$ | – | – | 250 | µs | [6)] | P_8.3.51 |

1) Not subject to production test, specified by design, S2P - Method; f = 10 MHz
2) $V_{SYM}$ shall be observed during dominant and recessive state and also during the transition dominant to recessive and vice versa while TXD is simulated by a square signal (50% duty cycle) with a frequency of up to 1 MHz (2MBit/s).
3) $R_{tests}$ between (Vs /VCAN) and 0V (GND).
4) Not subject to production test, specified by design.
5) $\Delta t_{Rec} = t_{bit(RXD)} - t_{bit(BUS)}$.
6) Not subject to production test, tolerance defined by internal oscillator tolerance.

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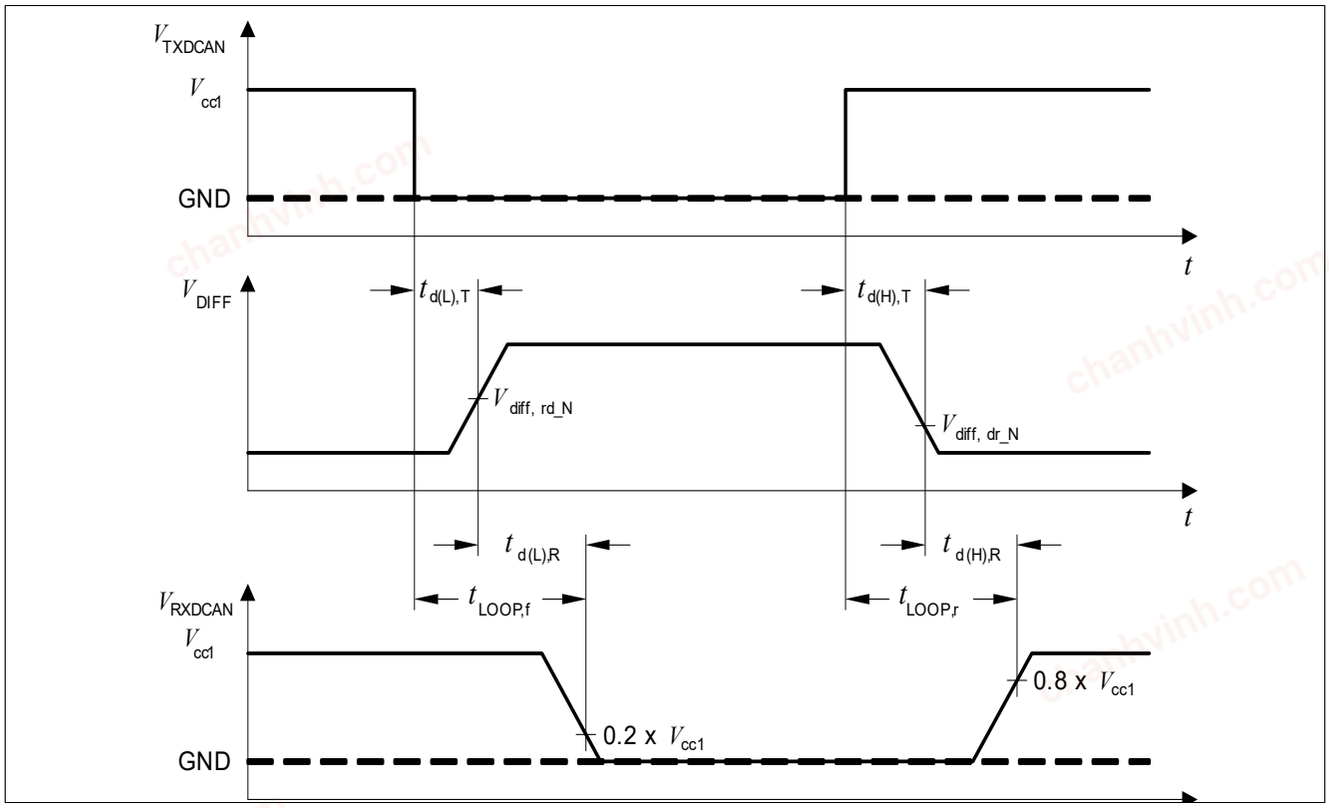



**Figure 29 Timing Diagrams for Dynamic Characteristics**

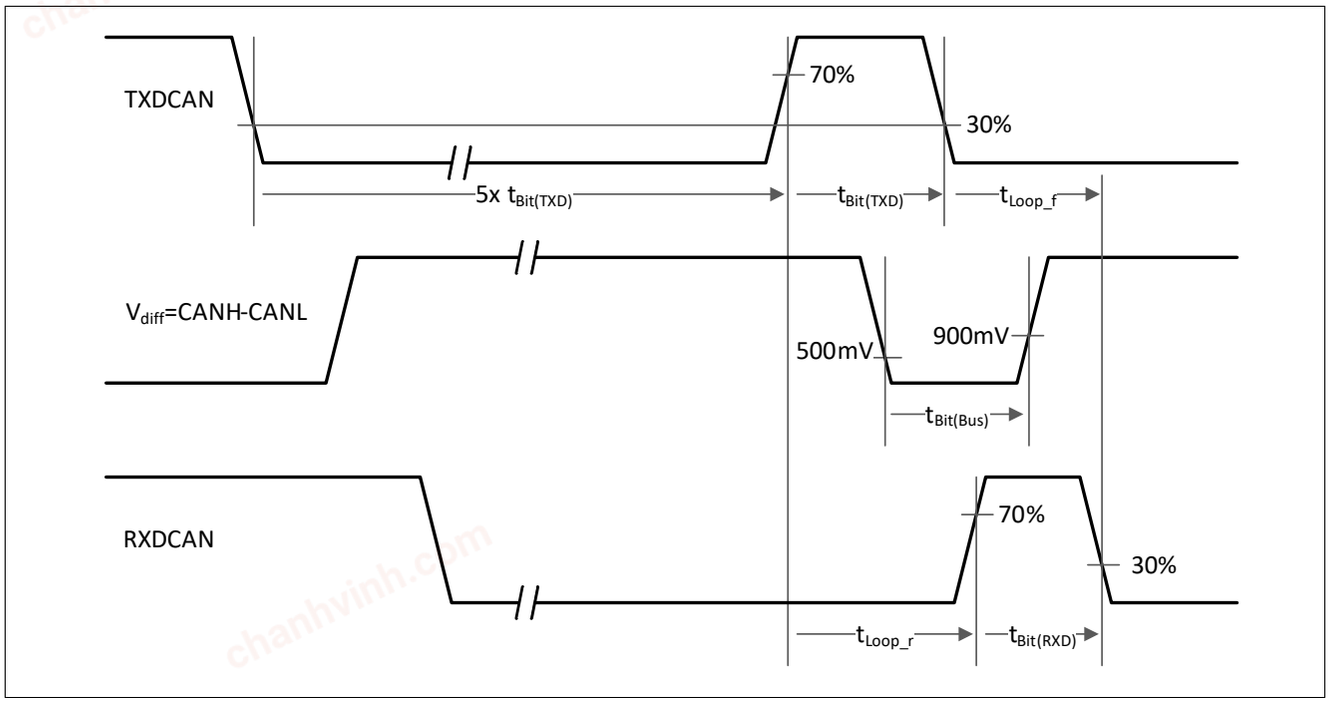



**Figure 30 From ISO11898-2:2016: tloop, tbit(TXD), tbit(Bus), tbit(RXD) definitions**

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# 9 LIN Transceiver

## 9.1 Block Description

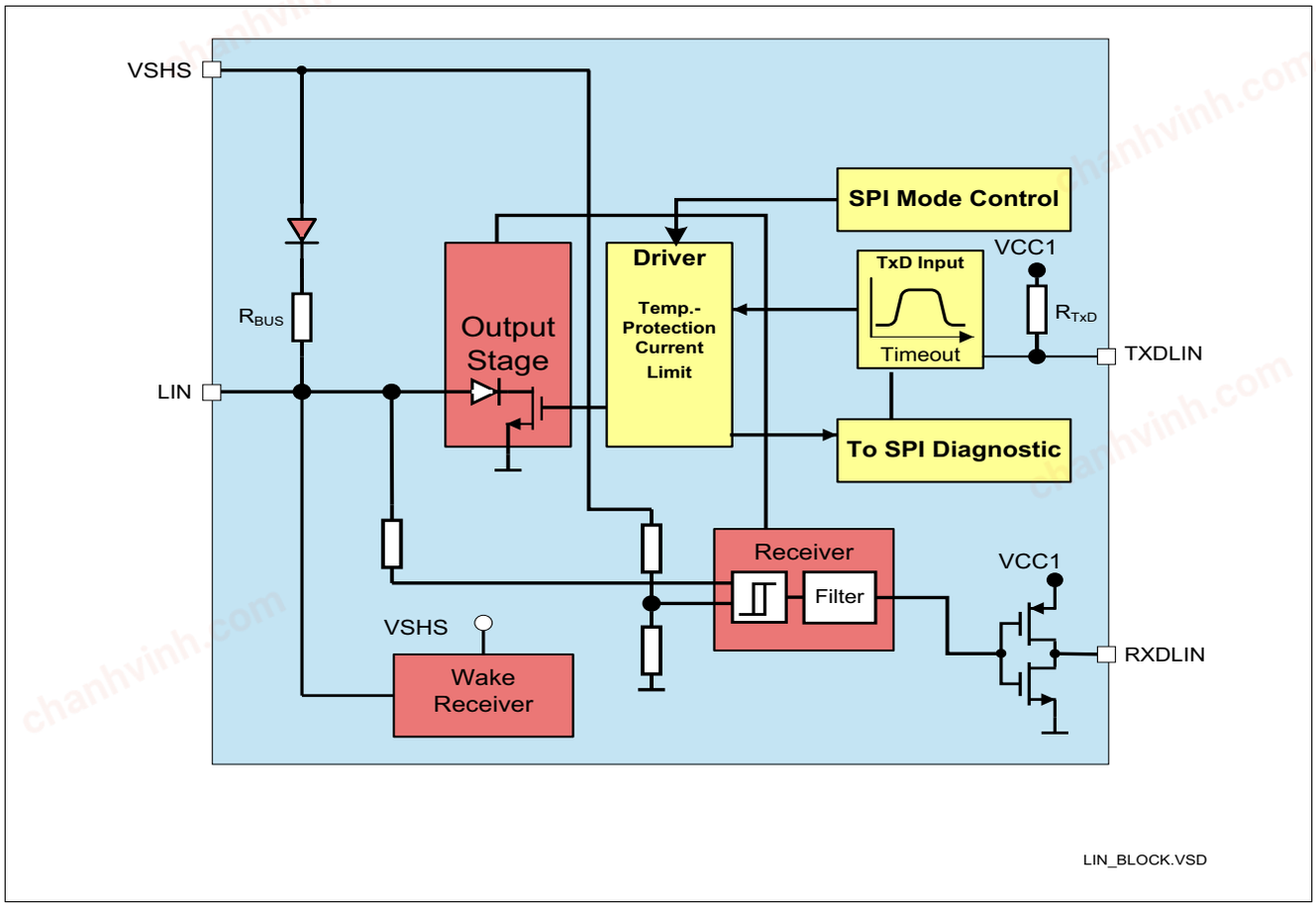



**Figure 31 Block Diagram**

### 9.1.1 LIN Specifications

The LIN network is standardized by international regulations.

The device is compliant to:

- ISO17987-4: rev. 2016
- SAE-J2602-2

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## 9.2 Functional Description

The LIN Bus is a single wire, bi-directional bus, used for in-vehicle networks. The LIN transceivers implemented inside the TLE9562QX are the interface between the microcontroller and the physical LIN Bus. The digital output data from the microcontroller are driven to the LIN bus via the TXDLIN pin on the TLE9562QX. The transmit data stream on the TXDLIN is converted to a LIN bus signal with optimized slew rate to minimize the EME level of the LIN network. The RXDLIN sends back the information from the LIN bus to the microcontroller. The receiver has an integrated filter network to suppress noise on the LIN Bus and to increase the EMI (Electro Magnetic Immunity) level of the transceiver.

Two logical states are possible on the LIN Bus according to the LIN specification.

Every LIN network consists of a master node and one or more slave nodes. To configure the TLE9562QX for master node applications, a resistor in the range of 1 kΩ and a reverse diode must be connected between the LIN bus and the power supply VSHS.

The different transceiver modes can be controlled via the SPI **LIN** bits.

**Figure 32** shows the possible transceiver mode transitions when changing the devicemode.

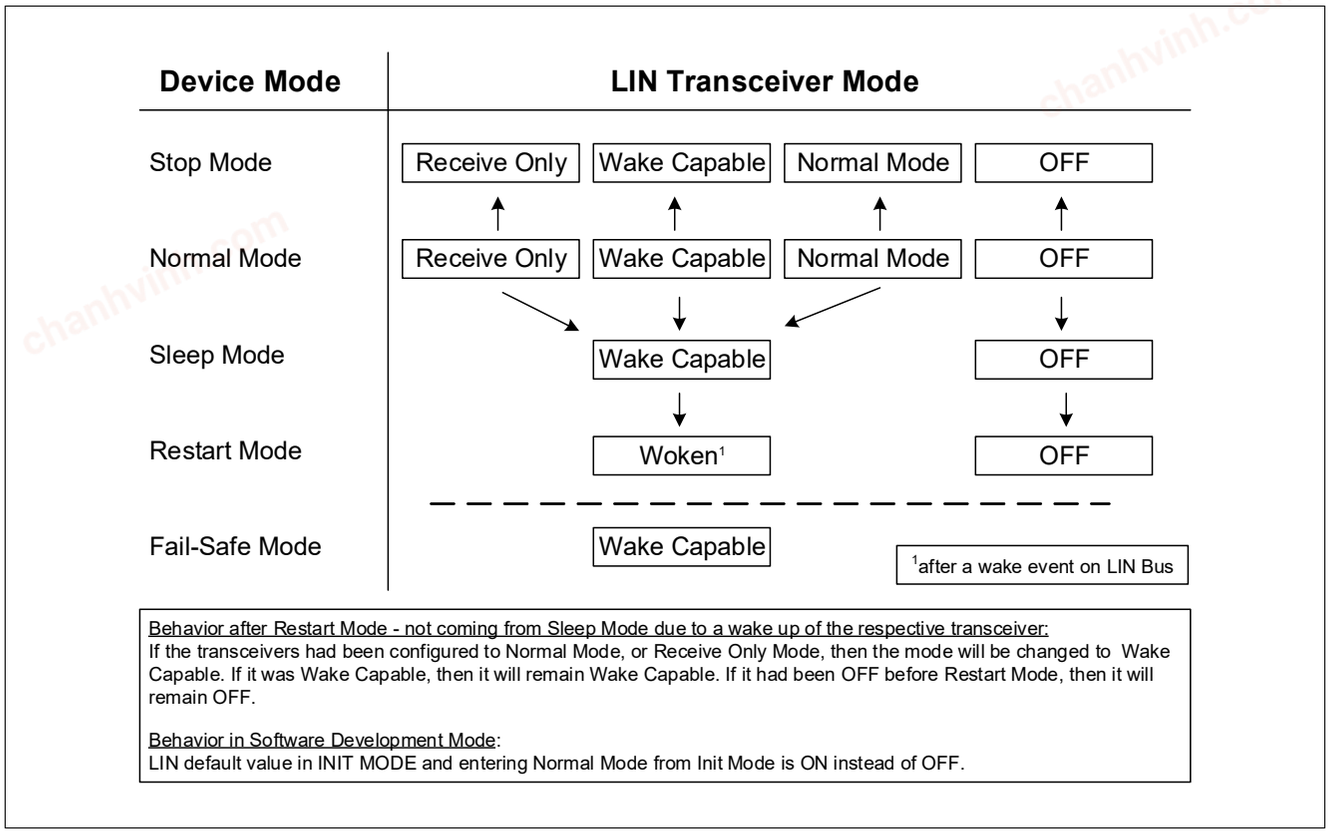



**Figure 32 LIN Mode Control Diagram**

### 9.2.1 LIN OFF Mode

The LIN OFF Mode is the default mode after power-up of the device. It is available in all device modes and is intended to completely stop LIN activities or when LIN communication is not needed. In LIN OFF Mode, a wake-up event on the bus will be ignored.

### 9.2.2 LIN Normal Mode

The LIN Transceiver is enabled via SPI in Normal Mode. LIN Normal Mode is designed for normal data transmission/reception within the LIN network. The mode is available in Normal Mode and in Stop Mode.

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### Transmission

The signal from the microcontroller is applied to the TXDLIN input of the device. The bus driver switches the LIN output stage to transfer this input signal to the LIN bus line.

### Enabling Sequence

The LIN transceiver requires an enabling time $t_{LIN,EN}$ before a message can be sent on the bus. This means that the TXDLIN signal can only be pulled LOW after the enabling time. If this is not ensured, then the TXDLIN needs to be set back to high (=recessive) until the enabling time is completed.

Only the next dominant bit will be transmitted on the bus.

**Figure 33** shows different scenarios and explanations for LIN enabling.

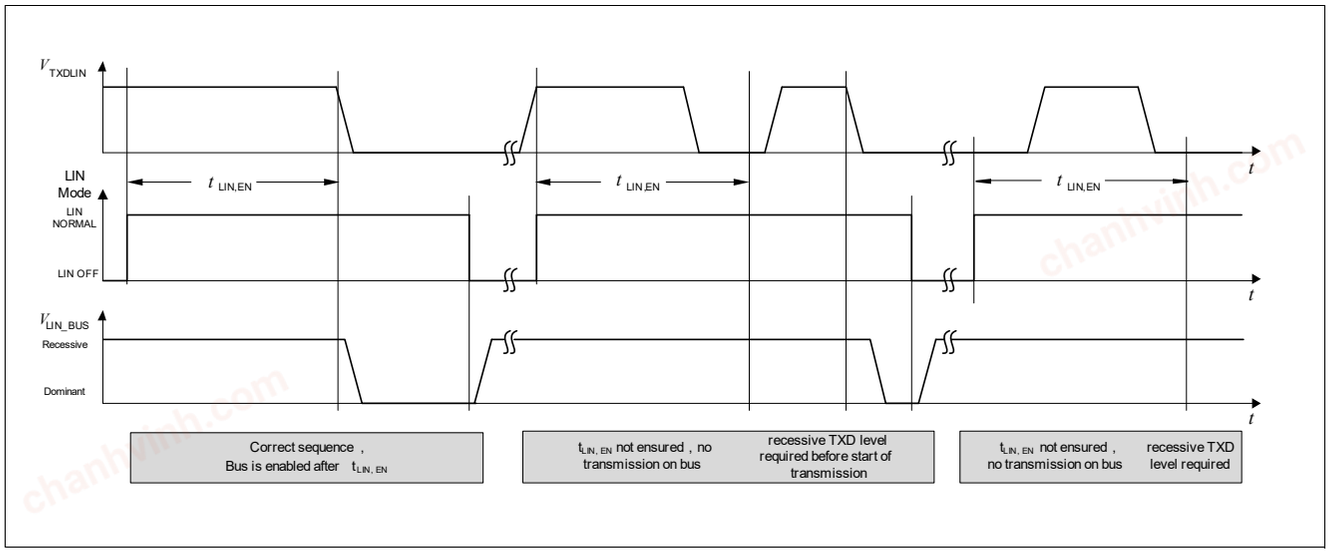



**Figure 33 LIN Transceiver Enabling Sequence**

### Reduced Electromagnetic Emission

To reduce electromagnetic emissions (EME), the bus driver controls LIN slopes symmetrically. The configuration of the different slopes is described in **Chapter 9.2.8**.

### Reception

Analog LIN bus signals are converted into digital signals at RXDLIN via the differential input receiver.

## 9.2.3 LIN Receive Only Mode

In LIN Receive Only Mode (RXD only), the driver stage is de-activated but reception is still possible. This mode is accessible by an SPI command and is available in Normal Mode and Stop Mode.

## 9.2.4 LIN Wake Capable Mode

This mode can be used in Stop Mode, Sleep Mode, Restart Mode and Normal Mode by programming via SPI and it is used to monitor bus activities. It is automatically accessed in Fail-Safe Mode. A wake up is detected, if a recessive to dominant transition on the LIN bus is followed by a dominant level of longer than $t_{WK,Bus}$ followed by a dominant to recessive transition. The dominant to recessive transition will cause a wake up of the LIN transceiver.

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A wake-up results in different behavior of the device, as described in below **Table 16**. As a signalization to the microcontroller, the RXDLIN pin is set LOW and will stay LOW until the LIN transceiver is changed to any other mode. After a wake-up event the transceiver can be switched to LIN Normal Mode for communication.

**Table 16 Action due to a LIN BUS Wake-up**

| Mode | Mode after Wake | VCC1 | INTN | RXDLIN |
|---|---|---|---|---|
| Normal Mode | Normal Mode | ON | LOW | LOW |
| Stop Mode | Stop Mode | ON | LOW | LOW |
| Sleep Mode | Restart Mode | Ramping Up | HIGH | LOW |
| Restart Mode | Restart Mode | ON | HIGH | LOW |
| Fail-Safe Mode | Restart Mode | Ramping up | HIGH | LOW |

#### Rearming the transceiver for wake capability

After a BUS wake-up event, the transceiver is woken. However, the **LIN** transceiver mode bits will still show wake capable (=‘01’) so that the RXDLIN signal will be pulled low.

There are two possibilities how the LIN transceiver’s wake capable mode is enabled again after a wake event:

- The LIN transceiver mode must be toggled, i.e. switched to LIN Normal Mode, LIN Receive Only Mode or LIN OFF Mode, before switching to LIN Wake Capable Mode again.
- Rearming is done automatically when the device is changed to Stop Mode, Sleep Mode or Fail-Safe Mode to ensure wake-up capability.

#### Wake-Up in Stop Mode and Normal Mode

In Stop Mode, if a wake-up is detected, it is signaled by the INTN output and in the **WK_STAT** SPI register. It is also signaled by RXDLIN put to LOW. The same applies for the Normal Mode. The microcontroller should set the device to Normal Mode, there is no automatic transition to Normal Mode.

For functional safety reasons, the watchdog will be automatically enabled in Stop Mode after a Bus wake event in case it was disabled before (if bit **WD_EN_ WK_BUS** was configured to HIGH before).

#### Wake-Up in Sleep Mode

One wake-up event on the LIN Bus from Sleep or Fail-Safe Mode automatically transfers the device into the Restart Mode and from there to Normal Mode. The corresponding RXD pin in set to LOW. The microcontroller is able to detect the low signal on RXD and to read the wake source out of the **WK_STAT** register via SPI. No interrupt is generated when coming out of Sleep or Fail-Safe Mode. The microcontroller can now switch the LIN transceiver into LIN Normal Mode via SPI to start communication.

### 9.2.5 TXD Time-out Feature

If the TXDLIN signal is dominant for the time $t > t_{TxD_LIN_TO}$, the TXD time-out function deactivates the LIN transmitter output stage temporarily. The transceiver remains in recessive state. The TXD time-out function prevents the LIN bus from being blocked by a permanent LOW signal on the TXDLIN pin, caused by a failure. The failure is stored in the SPI flag **LIN_FAIL**. The LIN transmitter stage is activated again after the dominant time-out condition is removed. The transceiver configuration stays unchanged.

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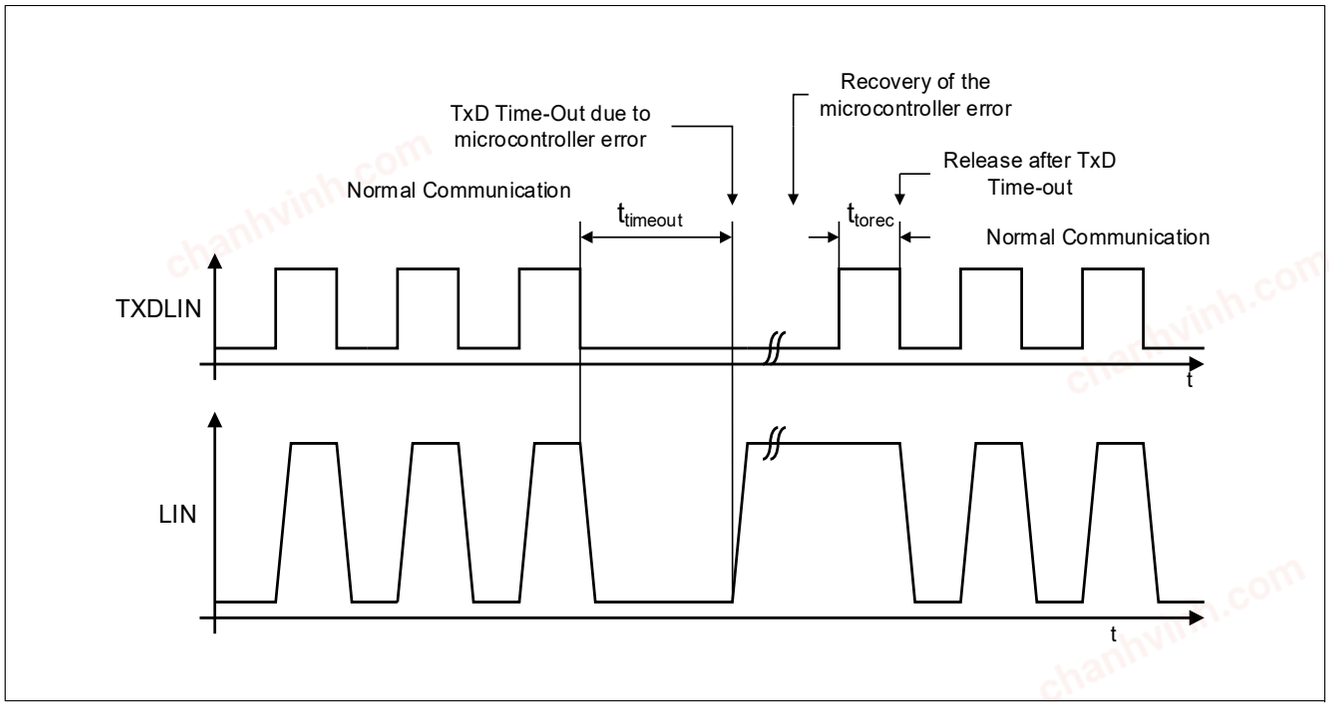



**Figure 34 TXD Time-Out Function**

### 9.2.6 Bus Dominant Clamping

If the LIN bus signal is dominant for a time $t > t_{BUS_LIN_TO}$ in LIN Normal Mode and LIN Receive Only Mode, then a bus dominant clamping is detected and the SPI bit **LIN_FAIL** is set. The transceiver configuration stays unchanged.

### 9.2.7 Under-Voltage Detection

In case the supply voltage is dropping below the VSHS undervoltage detection threshold (VSHS < $V_{SHS,UVD}$), the TLE9562QX disables the output and receiver stages. If the power supply reaches a higher level than the undervoltage detection threshold (VSHS> $V_{SHS,UVD}$), the TLE9562QX continues with normal operation. The transceiver configuration stays unchanged.

### 9.2.8 Slope Selection

The LIN transceiver offers a LIN Low-Slope Mode for 10.4 kBaud communication and a LIN Normal-Slope Mode for 20 kBaud communication. The only difference is the behavior of the transmitter. In LIN Low-Slope Mode, the transmitter uses a lower slew rate to further reduce the EME compared to Normal-Slope Mode. This complies with SAE J2602 requirements.By default, the device works in LIN Normal-Slope Mode. The selection of LIN Low-Slope Mode is done by an SPI bit **LIN_LSM** and will become effective as soon as CSN goes ‘HIGH’. Only the LIN Slope is changed. The selection is accessible in Normal Mode only.

### 9.2.9 Flash Programming via LIN

The device allows LIN flash programming, e.g. of another LIN Slave with a communication of up to 115 kBaud. This feature is enabled by de-activating the slope control mechanism via a SPI command (bit LIN_FLASH) and will become effective as soon as CSN goes ‘HIGH’. The SPI bit can be set in Normal Mode.

*Note: It is recommended to perform flash programming only at nominal supply voltage VSHS = 13.5 V to ensure stable data communication.*

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## 9.3 Electrical Characteristics

**Table 17 Electrical Characteristics**

$V_{SHS}$ = 5.5 V to 18 V, $T_j$ = -40°C to +150°C, RL = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Receiver Output (RXD pin)** | | | | | | | |
| HIGH Level Output Voltage | $V_{RXD,H}$ | 0.8 × $V_{CC1}$ | – | – | V | $I_{RXD}$ = -2 mA; $V_{Bus}$ = $V_{SHS}$ | P_9.3.1 |
| LOW Level Output Voltage | $V_{RXD,L}$ | – | – | 0.2 × $V_{CC1}$ | V | $I_{RXD}$ = 2 mA; $V_{Bus}$ = 0 V | P_9.3.2 |
| **Transmission Input (TXD pin)** | | | | | | | |
| HIGH Level Input Voltage | $V_{TXD,H}$ | – | – | 0.7 × $V_{CC1}$ | V | Recessive State | P_9.3.3 |
| TXD Input Hysteresis | $V_{TXD,hys}$ | – | 0.12 × $V_{CC1}$ | – | V | 1) | P_9.3.4 |
| LOW Level Input Voltage | $V_{TXD,L}$ | 0.3 × $V_{CC1}$ | – | – | V | Dominant State | P_9.3.5 |
| TXD Pull-up Resistance | $R_{TXD}$ | 20 | 40 | 80 | kΩ | $V_{TXD}$ = 0 V | P_9.3.6 |
| **LIN Bus Receiver (LIN Pin)** | | | | | | | |
| Receiver Threshold Voltage, Recessive to Dominant Edge | $V_{Bus,rd}$ | 0.4 × $V_{SHS}$ | 0.45 × $V_{SHS}$ | – | V | | P_9.3.7 |
| Receiver Dominant State | $V_{Bus,dom}$ | – | – | 0.4 × $V_{SHS}$ | V | LIN 2.2 Param. 17 | P_9.3.8 |
| Receiver Threshold Voltage, Dominant to Recessive Edge | $V_{Bus,dr}$ | – | 0.55 × $V_{SHS}$ | 0.60 × $V_{SHS}$ | V | | P_9.3.9 |
| Receiver Recessive State | $V_{Bus,rec}$ | 0.6 × $V_{SHS}$ | – | – | V | LIN 2.2 Param 18 | P_9.3.10 |
| Receiver Center Voltage | $V_{Bus,c}$ | 0.475 × $V_{SHS}$ | 0.5 × $V_{SHS}$ | 0.525 × $V_{SHS}$ | V | LIN 2.2 Param 19 6 V < $V_{SHS}$ < 18 V | P_9.3.11 |
| Receiver Hysteresis | $V_{Bus,hys}$ | 0.07 × $V_{SHS}$ | 0.1 × $V_{SHS}$ | 0.175 × $V_{SHS}$ | V | $V_{bus,hys}$ = $V_{bus,dr}$ - $V_{bus,rd}$ LIN 2.2 Param 20 | P_9.3.12 |
| Wake-up Threshold Voltage | $V_{Bus,wk}$ | 0.40 × $V_{SHS}$ | 0.5 × $V_{SHS}$ | 0.6 × $V_{SHS}$ | V | – | P_9.3.13 |
| Dominant Time for Bus Wake-up | $t_{WK,Bus}$ | 30 | – | 150 | µs | 2) | P_9.3.14 |

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**Table 17 Electrical Characteristics** (cont'd)

$V_{SHS}$ = 5.5 V to 18 V, $T_j$ = -40°C to +150°C, RL = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **LIN Bus Transmitter (LIN Pin)** | | | | | | | |
| Bus Serial Diode Voltage Drop | $V_{serdiode}$ | 0.4 | 0.7 | 1.0 | V | 1) $V_{TXD}$ = VCC1; LIN 2.2 Param 21 | P_9.3.15 |
| Bus Recessive Output Voltage | $V_{BUS,ro}$ | 0.8 × $V_{SHS}$ | – | $V_{SHS}$ | V | $V_{TXD}$ = HIGH Level | P_9.3.16 |
| Bus Short Circuit Current | $I_{BUS,sc}$ | 40 | 100 | 150 | mA | $V_{BUS}$ = 18 V; LIN 2.2 Param 12 | P_9.3.20 |
| Leakage Current Loss of Ground | $I_{BUS,lk1}$ | -1000 | -450 | 20 | µA | $V_{SHS}$ = 12 V = GND; 0 V < $V_{BUS}$ < 18 V; LIN 2.2 Param 15 | P_9.3.21 |
| Leakage Current Loss of Battery | $I_{BUS,lk2}$ | – | – | 20 | µA | $V_{SHS}$ = 0 V; $V_{BUS}$ = 18 V; LIN 2.2 Param 16 | P_9.3.22 |
| Leakage Current Driver Off | $I_{BUS,lk3}$ | -1 | – | – | mA | $V_{SHS}$ = 18 V; $V_{BUS}$ = 0 V; LIN 2.2 Param 13 | P_9.3.23 |
| Leakage Current Driver Off | $I_{BUS,lk4}$ | – | – | 20 | µA | $V_{SHS}$ = 8 V; $V_{BUS}$ = 18 V; LIN 2.2 Param 14 | P_9.3.24 |
| Bus Pull-up Resistance | $R_{BUS}$ | 20 | 30 | 47 | kΩ | Normal Mode LIN 2.2 Param 26 | P_9.3.25 |
| LIN Input Capacitance | $C_{BUS}$ | | 20 | 25 | pF | 1) | P_9.3.26 |
| Receiver propagation delay bus dominant to RXD LOW | $t_{d(L),R}$ | – | 1 | 6 | µs | $V_{CC}$ = 5 V; $C_{RXD}$ = 20 pF; LIN 2.2 Param 31 | P_9.3.27 |
| Receiver propagation delay bus recessive to RXD HIGH | $t_{d(H),R}$ | – | 1 | 6 | µs | $V_{CC}$ = 5 V; $C_{RXD}$ = 20 pF; LIN 2.2 Param 31 | P_9.3.28 |
| Receiver delay symmetry | $t_{sym,R}$ | -2 | – | 2 | µs | $t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$; LIN 2.2 Param 32 | P_9.3.29 |
| LIN Transceiver Enabling Time | $t_{LIN,EN}$ | 8 | 13 | 18 | µs | 2)CSN = HIGH to first valid transmitted TXD dominant | P_9.3.30 |
| Bus Dominant Time Out | $t_{BUS_LIN_TO}$ | – | 20 | – | ms | 1)2) | P_9.3.31 |
| TXD Dominant Time Out | $t_{TxD_LIN_TO}$ | – | 20 | – | ms | 1)2) $V_{TXD}$ = 0 V | P_9.3.32 |
| TXD Dominant Time Out Recovery Time | $t_{torec}$ | – | 10 | – | µs | 1)2) | P_9.3.33 |

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**Table 17 Electrical Characteristics** (cont'd)

$V_{SHS}$ = 5.5 V to 18 V, $T_j$ = -40°C to +150°C, RL = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Duty Cycle D1<br>(For worst case at 20 kbit/s)<br>LIN 2.2 Normal Slope | D1 | 0.396 | – | – | | [3] $TH_{Rec}(max) = 0.744 \times V_{SHS}$;<br>$TH_{Dom}(max) = 0.581 \times V_{SHS}$;<br>$V_{SHS}$ = 7.0 … 18 V;<br>$t_{bit}$ = 50 µs;<br>D1 = $t_{bus_rec(min)}/2\ t_{bit}$;<br>LIN 2.2 Param 27 | P_9.3.34 |
| Duty Cycle D2<br>(for worst case at 20 kbit/s)<br>LIN 2.2 Normal Slope | D2 | – | – | 0.581 | | [3] $TH_{Rec}(min.) = 0.422 \times V_{SHS}$;<br>$TH_{Dom}(min.) = 0.284 \times V_{SHS}$;<br>$V_{SHS}$ = 7.6 … 18 V;<br>$t_{bit}$ = 50 µs;<br>D2 = $t_{bus_rec(max)}/2\ t_{bit}$;<br>LIN 2.2 Param 28 | P_9.3.35 |
| Duty Cycle D3<br>(for worst case at 10.4 kbit/s)<br>SAE J2602 Low Slope | D3 | 0.417 | – | – | | [3] $TH_{Rec}(max) = 0.778 \times V_{SHS}$<br>$TH_{Dom}(max) = 0.616 \times V_{SHS}$;<br>$V_{SHS}$ = 7.0 … 18 V;<br>$t_{bit}$ = 96 µs;<br>D3 = $t_{bus_rec(min)}/2\ t_{bit}$;<br>LIN 2.2 Param 29 | P_9.3.36 |
| Duty Cycle D4<br>(for worst case at 10.4 kbit/s)<br>SAE J2602 Low Slope | D4 | – | – | 0.590 | | [3] $TH_{Rec}(min.) = 0.389 \times V_{SHS}$;<br>$TH_{Dom}(min.) = 0.251 \times V_{SHS}$;<br>$V_{SHS}$ = 7.6 … 18 V;<br>$t_{bit}$ = 96 µs;<br>D4 = $t_{bus_rec(max)}/2\ t_{bit}$;<br>LIN 2.2 Param 30 | P_9.3.37 |

1) Not subject to production test, specified by design.
2) Not subject to production test, tolerance defined by internal oscillator tolerance.
3) Bus load conditions concerning LIN Specification 2.2 $C_{LIN}$, $R_{LIN}$ = 1 nF, 1 kΩ / 6.8 nF, 660 Ω/ 10 nF, 500 Ω.

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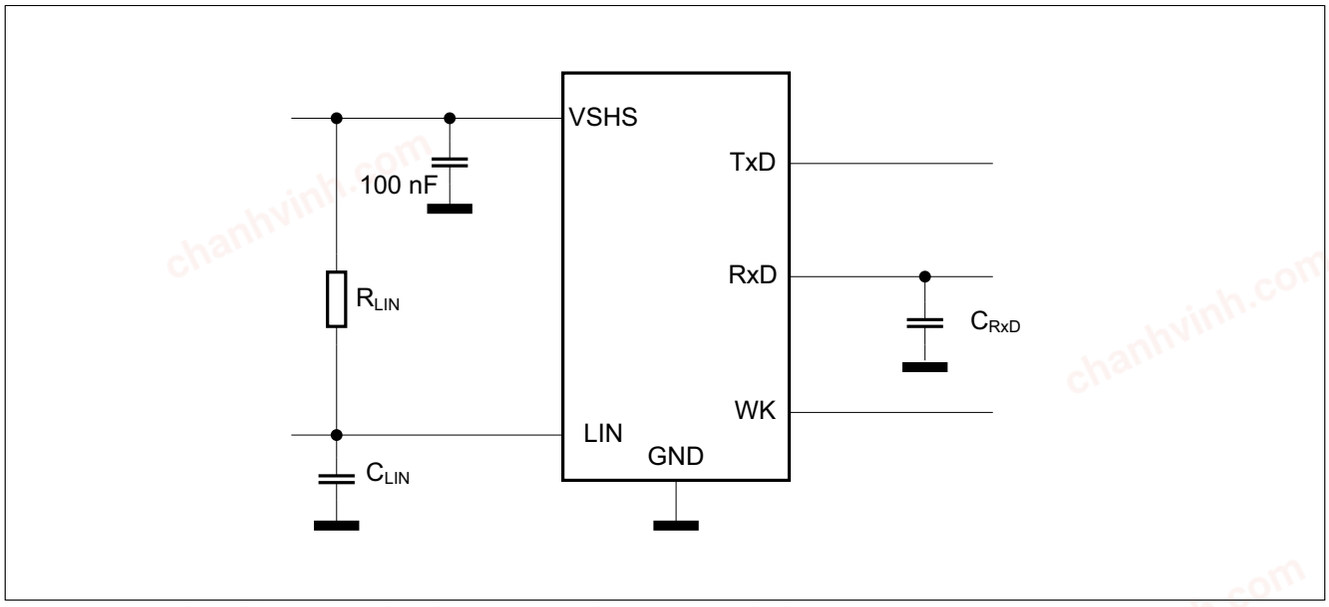



**Figure 35 Simplified Test Circuit for Dynamic Characteristics**

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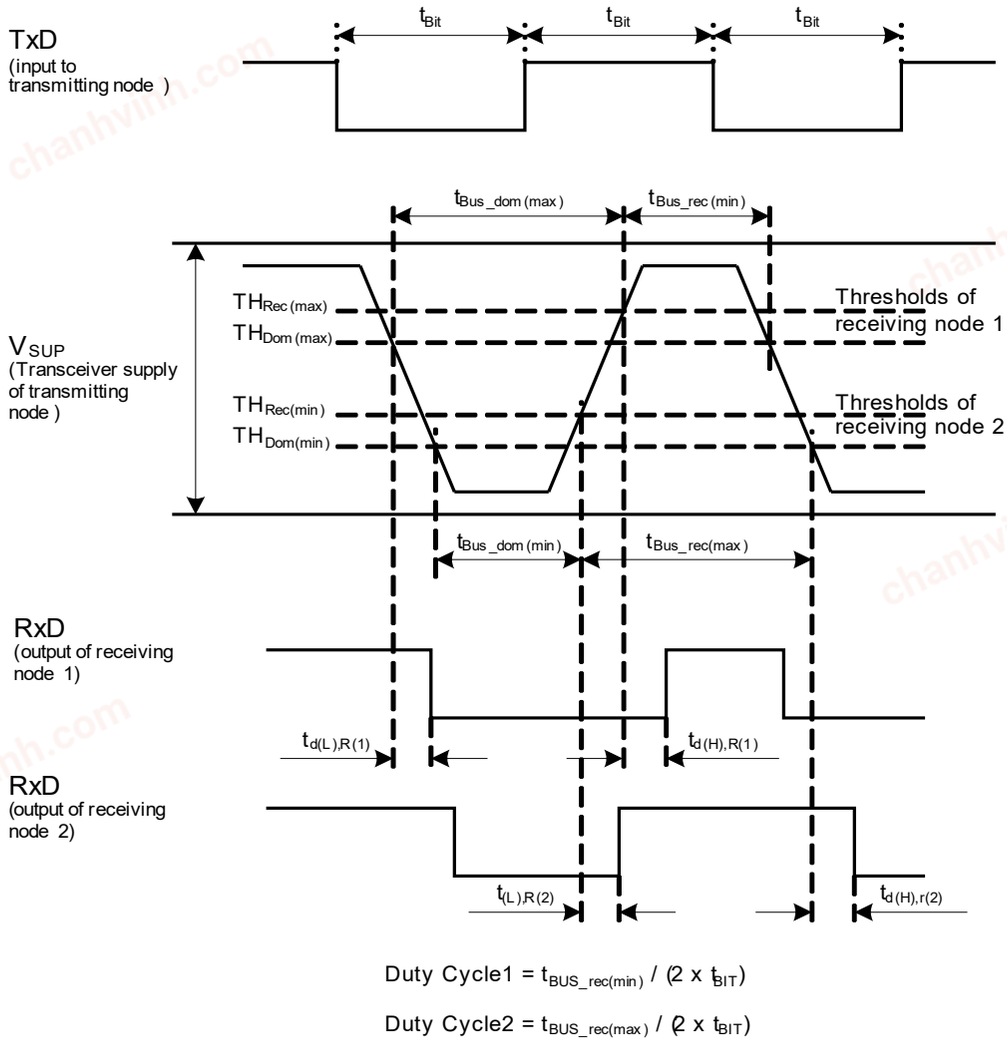



**Figure 36 Timing Diagram for Dynamic Characteristics**

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# 10 High-Voltage Wake Input

## 10.1 Block Description

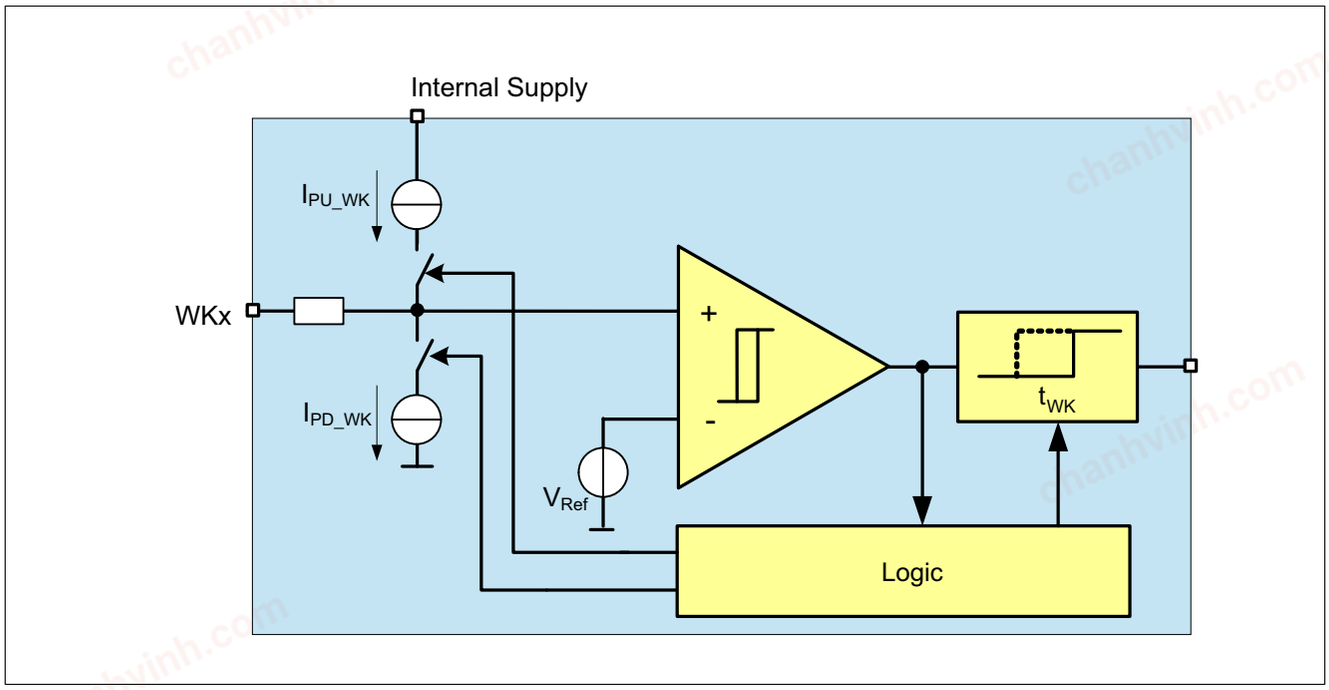



**Figure 37 Wake Input Block Diagram**

**Features**

- High-Voltage inputs with a 3 V (typ.) threshold voltage.
- Wake-up capability for power saving modes.
- Edge sensitive wake feature low to high and high to low.
- Pull-up and Pull-down current sources, configurable via SPI.
- Selectable configuration for static sense or cyclic sense.
- In Normal Mode and Stop Mode the level of the WKx pin can be read via SPI unless WK4 is configured as SYNC or WK2 is configured as FO.
- Synchronization with HSx via WK4 (for cyclic sense).
- Fail Safe Output configurability (only WK2).

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## 10.2 High-Voltage Wake Function

### 10.2.1 Functional Description

The wake inputs pin are edge-sensitive inputs with a switching threshold of typically 3 V. Both transitions, high to low and low to high, result in a signalization by the device. The signalization occurs either in triggering the interrupt in Normal Mode and Stop Mode or by a wake up of the device in Sleep Mode and Fail-Safe Mode.

Two different wake detection modes can be selected via SPI:

- Static sense: WK inputs are always active.
- Cyclic sense: WK inputs are only active for a certain time period (see **Chapter 5.7.1**).

A filter time tFWKx is implemented to avoid an unintentional wake-up due to transients or EMC disturbances in static sense configuration.

The filter time (tFWKx) is triggered by a level change crossing the switching threshold and a wake signal is recognized if the input level will not cross again the threshold during the selected filter time.

**Figure 38** shows a typical wake-up timing and filtering of transient pulses.

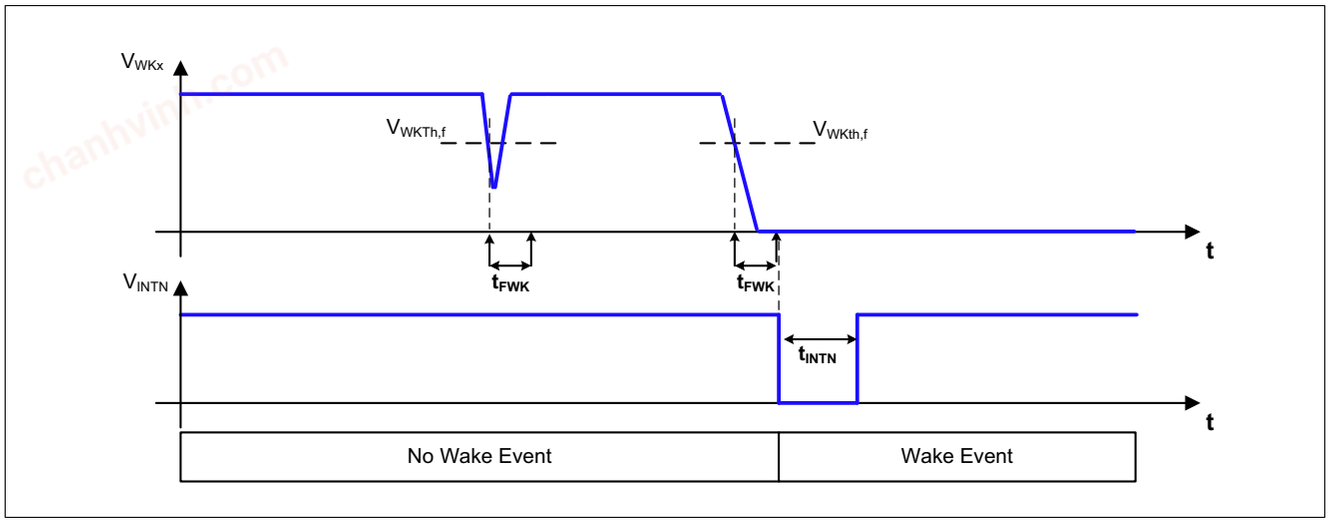



**Figure 38 Wake-up Filter Timing for Static Sense**

The wake-up capability for the WKx pin can be enabled or disabled via SPI command.

A wake event via the WKx pin can always be read in the register **WK_STAT**.

The actual voltage level of the WKx pin (low or high) can always be read in Normal Mode, Stop Mode and Init Mode in the register **WK_LVL_STAT**. During Cyclic Sense, the register shows the sampled levels of the respective WKx pin.

### 10.2.2 Wake Input Configuration

To ensure a defined and stable voltage levels at the internal comparator input it is possible to configure integrated current sources via the SPI register **WK_CTRL**.

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**Table 18 Pull-Up / Pull-Down Resistor**

| WKx_PUPD_1 | WKx_PUPD_0 | Current Sources | Note |
|---|---|---|---|
| 0 | 0 | no current source | WK input is floating if left open (default setting) |
| 0 | 1 | pull-down | WK input internally pulled to GND |
| 1 | 0 | pull-up | WK input internally pulled to internal 5V supply |
| 1 | 1 | Automatic switching | If a high level is detected at the WK input the pull-up source is activated, if low level is detected the pull down is activated. |

*Note: If a WK input is not used, the respective WK input must be tied to GND on board to avoid unintended floating state of the pin.*

One additional configuration is related the filter time of each Wake-up module. The bits **WK_FILT** permit to set the filter time in static sensing or in cyclic sensing.

*Note: When the device mode is changed to normal (from INIT), in case of static sense, if the WK pin is set, the WK_STAT register is set in this time (also the interrupt pin).*

### 10.2.3 Wake configuration for Cyclic Sense

The wake-up inputs can also be used for cyclical sensing signals during low-power modes. For this function the WKx input performs a cyclic sensing of the voltage level during the on-time of specific HSx.
A transition of the voltage level will trigger a wake-up event.
See also **Chapter 5.7.1** for more details.

### 10.2.4 Wake configuration for Synchronization

The WK4 pin can be configured as SYNC input for driving the HSx.

Prerequisite to configure the WK4 as SYNC input is that the WK4 has to be OFF.

The configuration of the WK4/SYNC bit is done using the **WK_EN** bits. if the **WK_EN**=$10_B$ (SYNC selected), all bits in WK4 bank are ignored and wake-up capability on WK4 is not available.

*Note: If WKx is the only wake source available and is configured with cyclic sense with SYNC (WKx_FILT = 100), trying to go to Sleep Mode is not possible (restart mode is entered) - because SYNC is driven by the microcontroller which is not supplied in Sleep Mode.*

### 10.2.5 Fail Safe Output Configuration

The WK2 is by default configured as Fail Safe Output. It is possible to configure the WK2/FO pin as wake-up source using the **WK2_FO** bit.

As soon as the bit **WK2_FO** is written (first SPI write access of bank 2 on **WK_CTRL**), the configuration can be changed only after a software reset or a new power-up sequence.

In case that the **WK2_FO** is locked, any attempt to configured again it will set the **SPI_FAIL**.

The Fail Output consists of a failure logic block and one LOW-side switch. In case of a failure, the FO output is activated and the SPI bit **FAILURE**, in the register **DEV_STAT**, is set.

The Failure Output is activated due to the following failure conditions:

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### High-Voltage Wake Input

- After four consecutive Watchdog Trigger failures.
- Thermal Shutdown **TSD2**.
- VCC1 short to GND.
- VCC1 overvoltage in case **VCC1_OV_MOD**=$11_B$.
- after four consecutive VCC1 undervoltage detection.

In order to deactivate the Fail Output, the failure conditions (e.g. TSD2) must not be present anymore and the bit **FAILURE** needs to be cleared via SPI command.

In case of Watchdog fail, the deactivation of the Fail Output is only allowed after a successful WD trigger, i.e. the **FAILURE** bit must be cleared.

*Note: The internally stored default value used for the wake-enabled configuration is 'low'. A level change will be signalized in the corresponding bits in **WK_STAT** in case the externally connected signal proceeds a rising or falling edge transition if the WK-enable is configured to high.*

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## 10.3 Electrical Characteristics

**Table 19 Electrical Characteristics**

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **WK1, WK2 ,WK3, WK4 Input Pin Characteristics** | | | | | | | |
| Wake-up/monitoring threshold voltage falling | $V_{WKx_th,f}$ | 2.5 | 3 | 3.5 | V | without external serial resistor $R_S$ | P_10.3.1 |
| Wake-up/monitoring threshold voltage rising | $V_{WKx_th,r}$ | 3 | 3.5 | 4 | V | without external serial resistor $R_S$ | P_10.3.2 |
| Threshold hysteresis | $V_{WKx_th,hys}$ | 0.4 | 0.6 | 0.85 | V | without external serial resistor $R_S$ | P_10.3.3 |
| WK pin Pull-up Current | $I_{PU_WKx}$ | -20 | -10 | -3 | µA | $V_{WKx}$ = 4 V | P_10.3.4 |
| WK pin Pull-down Current | $I_{PD_WKx}$ | 3 | 10 | 20 | µA | $V_{WKx}$ = 2.5 V | P_10.3.5 |
| Input leakage current | $I_{LK,Ix}$ | -2 | | 2 | µA | 0 V < $V_{WKx}$ < 40 V; Pull-up / Pull-down disabled | P_10.3.6 |
| **WK4 as SYNC input pin** | | | | | | | |
| LOW input voltage threshold | $WK4_{SYNC_th,L}$ | 0.3 × $V_{CC1}$ | - | - | V | | P_10.3.11 |
| HIGH input voltage threshold | $WK4_{SYNC_th,H}$ | - | - | 0.7 × $V_{CC1}$ | V | | P_10.3.12 |
| Pull-down resistance on WK/SYNC | $R_{SYNC}$ | 20 | 40 | 80 | kΩ | $V_{SYNC}$ = 1 V | P_10.3.13 |
| **WK2/FO as Fail Safe Output** | | | | | | | |
| FO low-side output voltage (active) | $V_{FO,L1}$ | – | 0.6 | 1 | V | WK2 configured as Fail-Safe Output; $I_{FO}$ = 4.0 mA | P_10.3.14 |
| FO input leakage current (all inactive) | $I_{FO,LK}$ | – | – | 2 | µA | V_FO = 28 V | P_10.3.15 |
| **Timing** | | | | | | | |
| Wake-up filter time 1 | $t_{FWK1}$ | 12 | 16 | 22 | µs | 1) | P_10.3.16 |
| Wake-up filter time 2 | $t_{FWK2}$ | 50 | 64 | 80 | µs | 1) | P_10.3.17 |

1) Not subject to production test, tolerance defined by internal oscillator tolerance.

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# 11 Interrupt Function

## 11.1 Block and Functional Description

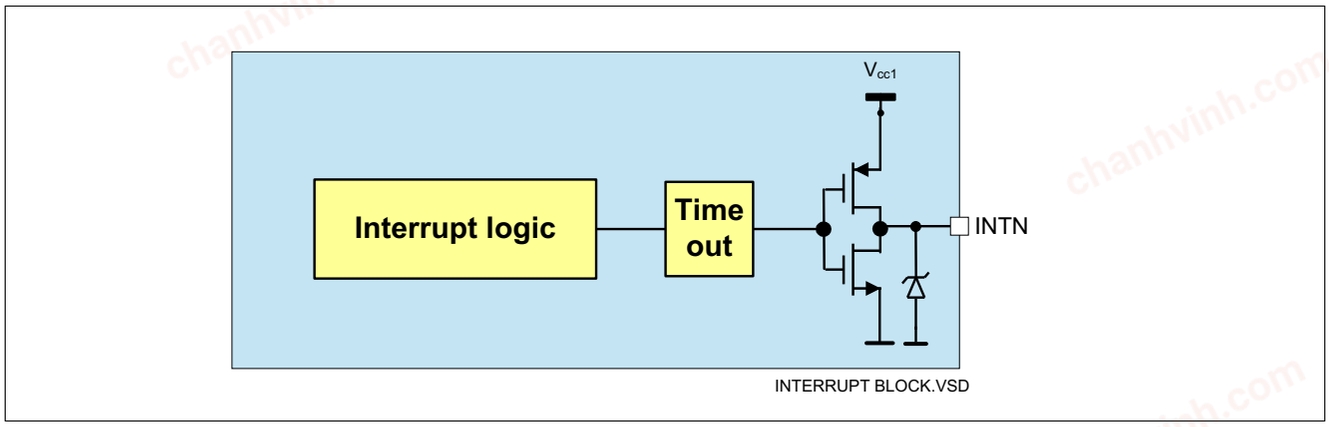



**Figure 39 Interrupt Block Diagram**

The interrupt is used to signalize special events in real time to the microcontroller. The interrupt block is designed as a push/pull output stage as shown in **Figure 39**. An interrupt is triggered and the INTN pin is pulled low (active low) for $t_{INTN}$ in Normal Mode and Stop Mode and it is released again once $t_{INTN}$ is expired. The minimum high-time of INTN between two consecutive interrupts is $t_{INTND}$. An interrupt does not cause a device mode change.

Two different interrupt generation methods are implemented:

- Interrupt Mask: One dedicated register (INT_MASK) is intended to enable or disable set of interrupt sources. The interrupt sources follow the SPI Status Information Field.
  In details:
  - SUPPLY_STAT: “OR” of all bits on SUP_STAT register except POR, VCC1_UV, VCC1_SC, VCC1_OV
  - TEMP_STAT: “OR” of all bits on THERM_STAT register except TSD2
  - BUS_STAT: “OR” of all bits on BUS_STAT register
  - HS_STAT: “OR” of all bits on HS_OL_OC_OT_STAT register
  - BD_STAT: “OR” of all bits on DSOV register
  - SPI_CRC_FAIL: or between SPI_FAIL and CRC_FAIL bits on DEV_STAT register.
- Wake-up events: all wake-up events stored in the wake status SPI register WK_STAT only in case the corresponding input was configured as wake-up source.
  The wake-up sources are:
  - via CAN (wake-up pattern or wake-up frame)
  - via LIN
  - via WK pins
  - via TIMERx (cyclic wake)
  - via LSx_DSOV_BRK if any of the brake-feature is enabled

The methods are both available at the same time.

*Note: The errors which will cause Restart or Fail-Safe Mode (VCC1_UV, VCC1_SC, VCC1_OV, TSD2) are the exceptions of an INTN generation. Also the bit POR will not generate interrupts. If the above*

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*mentioned bits are not cleared after the device is back in Normal Mode or Stop Mode, the INTN is periodically generated (Register based cyclic interrupt generation).*

*Note: Periodical interrupts are only generated by CRC fail and SPI fail from DEV_STAT register.*

*Note: During Restart Mode the SPI is blocked and the microcontroller is in reset. Therefore the INTN will not be in Restart Mode, which is the same behavior in Fail-Safe Mode or Sleep Mode.*

In addition to this behavior, INTN will be triggered when Stop Mode is entered and not all wake source bits were cleared in the WK_STAT register and also the LSx_DSOV_BRK bits in the DSOV register..

The SPI status registers are updated at every falling edge of the INTN pulse. All interrupt events are stored in the respective register until the register is cleared via SPI command. A second SPI read after reading out the respective status register is optional but recommended to verify that the interrupt event is not present anymore. The interrupt behavior is shown in **Figure 40**.

The INTN pin is also used during Init Mode to select the Software Development Mode entry. See **Chapter 5.2** for further information.

In case of pending INTN event (SPI Status registers are not cleared after INTN event), additional periodical INTN events are generated as shown in **Figure 41**.

The periodical INTN events generation can be disabled via SPI command using **INTN_CYC_EN** bit.

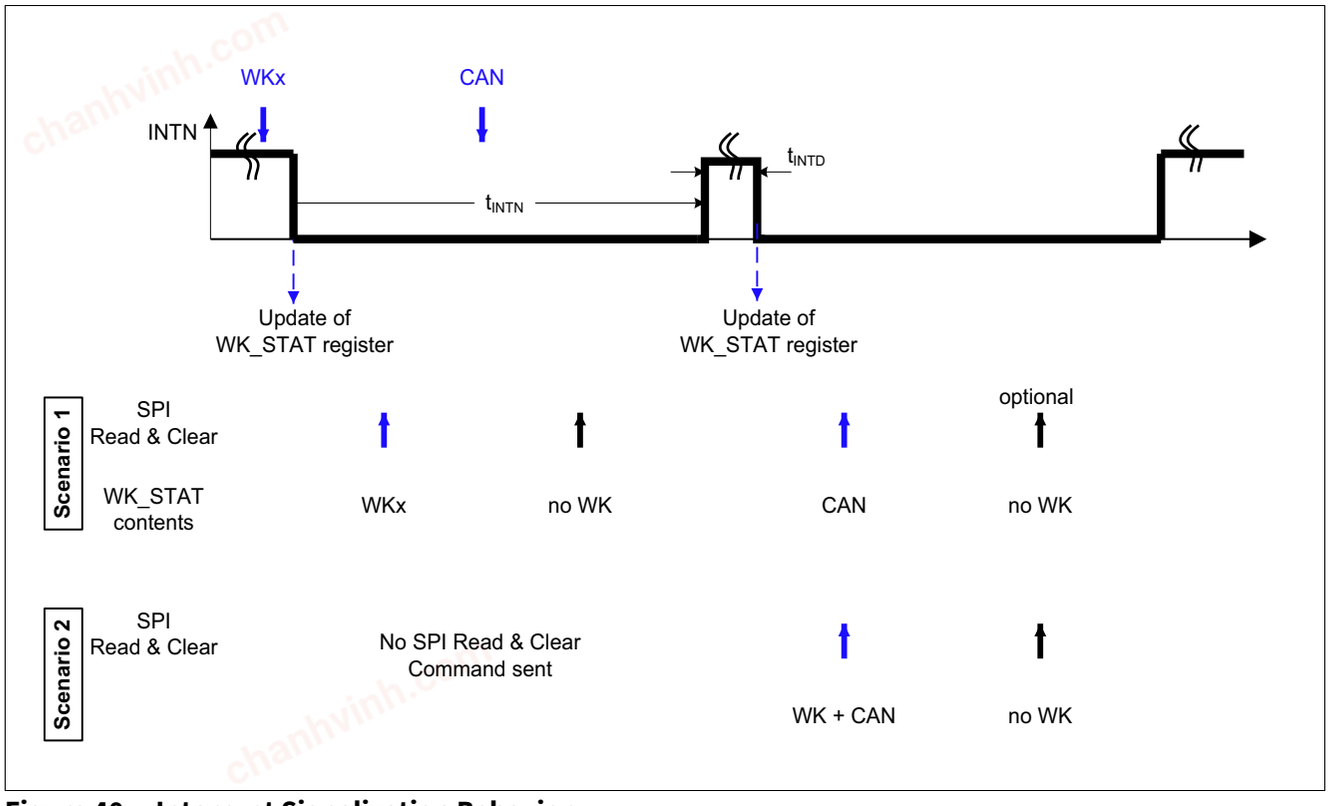



**Figure 40 Interrupt Signalization Behavior**

*Note: For two or more interrupt events at the same time, when INTN pin is low the same time, it will not start multiple toggling.*

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## Interrupt Function

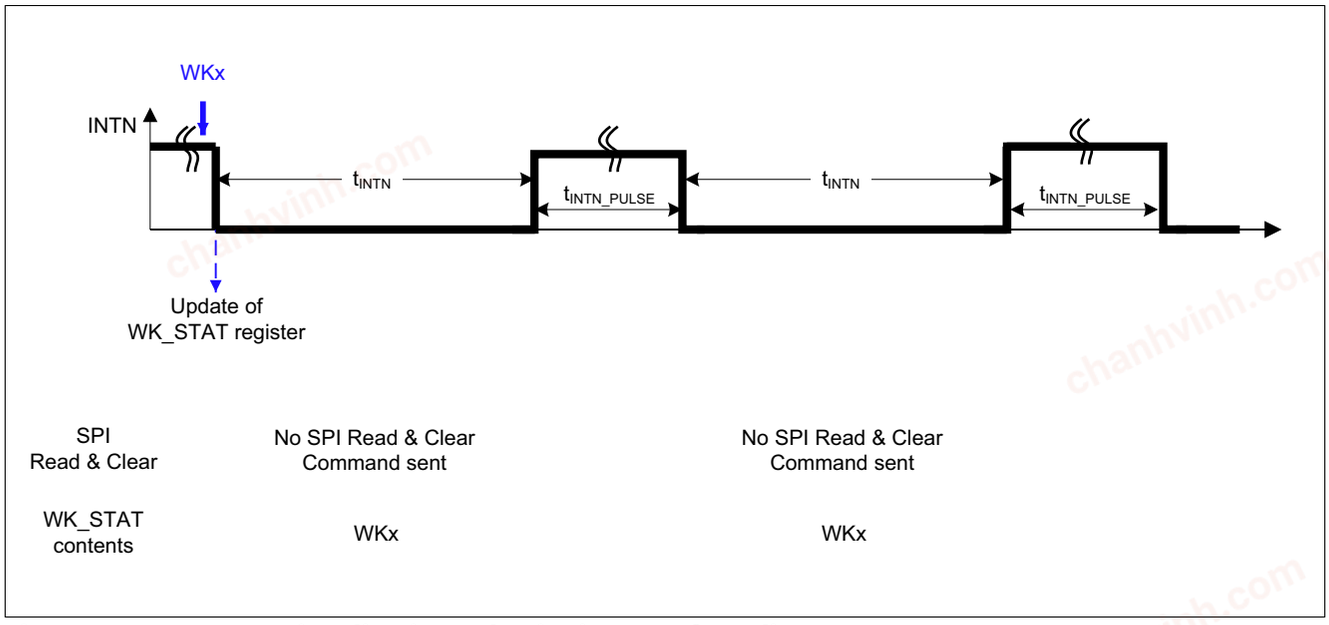



**Figure 41 Interrupt Signalization Behavior in case of pending INTN events**

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## 11.2 Electrical Characteristics

**Table 20 Electrical Characteristics**

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Interrupt Output; Pin INTN** | | | | | | | |
| INTN High Output Voltage | $V_{INTN,H}$ | 0.8 × $V_{CC1}$ | – | – | V | 1) $I_{INTN}$ = -2 mA; INTN = off | P_11.2.1 |
| INTN Low Output Voltage | $V_{INTN,L}$ | – | – | 0.2 × $V_{CC1}$ | V | 1) $I_{INTN}$ = 2mA; INTN = on | P_11.2.2 |
| INTN Pulse Width | $t_{INTN}$ | 80 | 100 | 120 | µs | 2) | P_11.2.3 |
| INTN Pulse Minimum Delay Time | $t_{INTND}$ | 80 | 100 | 120 | µs | 2) between consecutive pulses | P_11.2.4 |
| Pulse in case of pending INTN | $t_{INTN_PULSE}$ | 4 | 5 | 6 | ms | 2) between consecutive pulses | P_11.2.5 |
| **SDM Select; Pin INTN** | | | | | | | |
| Config Pull-up Resistance | $R_{SDM}$ | 30 | 60 | 100 | kΩ | $V_{INTN}$ = 5 V | P_11.2.6 |
| Config Select Filter Time | $t_{SDM_F}$ | 50 | 64 | 80 | µs | 2) | P_11.2.7 |

1) Output Voltage Value also determines device configuration during Init Mode.

2) Not subject to production test, tolerance defined by internal oscillator tolerance.

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# 12 Gate Drivers

The TLE9562QX integrates eight floating gate drivers capable of controlling a wide range of N-channel MOSFETs. They are configured as four high-sides an d four low-sides, building four half-bridges.

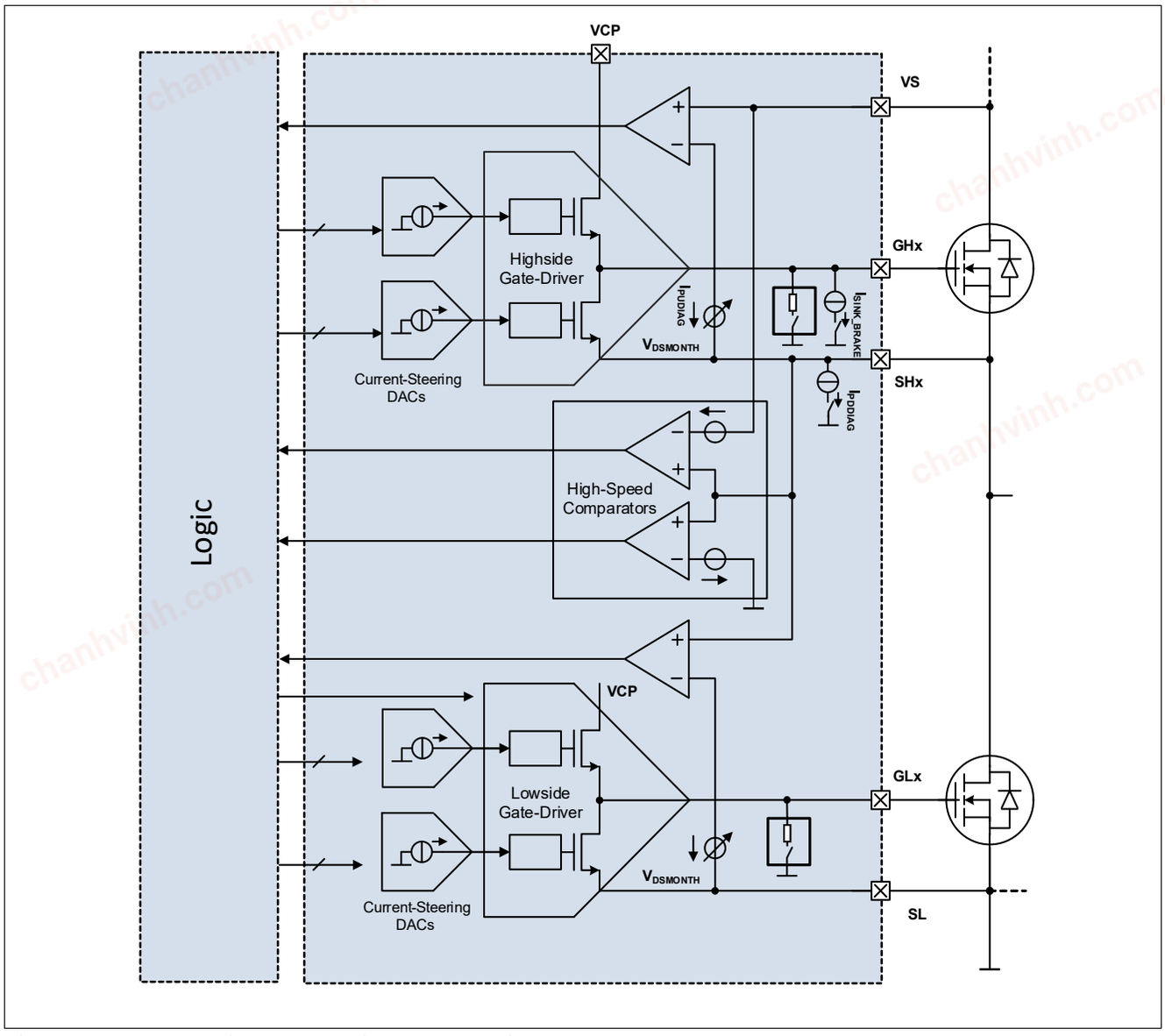



**Figure 42 Half-bridge gate driver - Block diagram**

This section describes the MOSFET control in static activation and during PWM operation.

*Note: PWMx mentioned in this chapter refer to the PWMx pins and signal used by the bridge driver to control the external MOSFETs.*

*Note: In this chapter PWMx **do not refer** to the internal PWM generators used to control the internal high-side switches HSx.*

## 12.1 MOSFET control

Depending on the configuration bits HBxMODE[1:0] (refer to **HBMODE**), **CPEN**, each high-side and low-side MOSFETs can be:

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- Kept off with the passive discharge.
- Kept off actively.
- Activated (statically, no PWM, HBx_PWM_EN = 0).
- Activated in PWM mode (HBx_PWM_EN = 1).

Refer to **Table 21** for details.

**Table 21 Half-bridge mode selection**

| CPEN | HBxMODE[1:0][1)] | Configuration of HSx/LSx[1)] |
|---|---|---|
| **CPEN** = 0 | Don’t care | All MOSFETs are kept off by the passive discharge |
| **CPEN** = 1 | $00_B$ | HBx MOSFETs are kept off by the passive discharge |
| **CPEN** = 1 | $01_B$ | LSx MOSFET is ON, HSx MOSFET is actively kept OFF |
| **CPEN** = 1 | $10_B$ | HSx MOSFET is ON, LSx MOSFET is actively kept OFF |
| **CPEN** = 1 | $11_B$ | LSx and HSx MOSFETs are actively kept OFF with IHOLD |

1) x = 1 … 4

## 12.2 Static activation

In this section, we consider the static activation of the high-side and low-side MOSFET of the half-bridge x: HBx_PWM_EN= 0 (in **ST_ICHG**) and **CPEN** = 1.

The low-side or high-side MOSFET of HBx is statically activated (no PWM) by setting HBxMODE[1:0] to respectively (0,1) or (1,0).

The configured active cross-current protection and the Drain-Source overvoltage blank times for the Half-Bridge x are noted $t_{HBxCCP\ ACTIVE}$ and $t_{HBxBLANK\ ACTIVE}$.
The charge and discharge currents applied to the static controlled Half-Bridge x are noted ICHGSTx (**ST_ICHG**).

IHARDOFF is the maximum current that the gate drivers can sink (100 mA typ.). This current is used to keep a MOSFET off, when the opposite MOSFET of the same half-bridge is being turned on. This feature reduces the risk of parasitic cross-current conduction.

ICHGSTx is the current sourced, respectively sunk, by the gate driver to turn-on the high-side x or low-side x. ICHGSTx is configured in the control register **ST_ICHG**.

**Table 22 Static charge and discharge currents**

| ICHGSTx[3:0] | Nom. charge current [mA] | Nom. discharge current [mA] | Max. deviation to typ. values |
|---|---|---|---|
| $0000_B$ | 0.5 ($I_{CHG0}$) | 0.5 ($I_{DCHG0}$) | +/- 60 % |
| $0001_B$ | 1.4 ($I_{CHG4}$) | 1.4 ($I_{DCHG4}$) | +/- 60 % |
| $0010_B$ | 3.1 ($I_{CHG8}$) | 3.1 ($I_{DCHG8}$) | +/- 55% |
| $0011_B$ | 5.7 ($I_{CHG12}$) | 5.7 ($I_{DCHG12}$) | +/- 40 % |
| $0100_B$ | 9.2 ($I_{CHG16}$) | 9.2 ($I_{DCHG16}$) | +/- 40 % |
| $0101_B$ | 13.7 ($I_{CHG20}$) | 13.5 ($I_{DCHG20}$) | +/- 40 % |

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**Table 22 Static charge and discharge currents** (cont'd)

| ICHGSTx[3:0] | Nom. charge current [mA] | Nom. discharge current [mA] | Max. deviation to typ. values |
|---|---|---|---|
| $0110_B$ | 19.2($I_{CHG24}$) | 18.8($I_{DCHG24}$) | +/- 40 % |
| $0111_B$ | 25.8 ($I_{CHG28}$) | 25.2 ($I_{DCHG28}$) | +/- 30 % |
| $1000_B$ | 32.8 ($I_{CHG32}$) | 32.2 ($I_{DCHG32}$) | +/- 30 % |
| $1001_B$ | 40.1 ($I_{CHG36}$) | 39.4 ($I_{DCHG36}$) | +/- 30 % |
| $1010_B$ | 47.8 ($I_{CHG40}$) | 47.0 ($I_{DCHG40}$) | +/- 30 % |
| $1011_B$ | 55.9 ($I_{CHG44}$) | 55.0 ($I_{DCHG44}$) | +/- 30 % |
| $1100_B$ | 64.3 ($I_{CHG48}$) | 63.2 ($I_{DCHG48}$) | +/- 30 % |
| $1101_B$ | 73.2 ($I_{CHG52}$) | 72.4 ($I_{DCHG52}$ | +/- 30 % |
| $1110_B$ | 82.7 ($I_{CHG56}$) | 82.1 ($I_{CHG56}$) | +/- 30 % |
| $1111_B$ | 92.7 ($I_{CHG60}$) | 92.2 ($I_{CHG60}$) | +/- 30 % |

IHOLD is the hold current used to keep the gate of the external MOSFETs in the desired state. This parameter is configurable with the IHOLD control bit in **GENCTRL**.

If the control bit IHOLD = 0:

- A MOSFET is kept ON with the current $I_{CHG19}$.
- A MOSFET is kept OFF with the current $I_{DCHG19}$.

If the control bit IHOLD = 1:

- A MOSFET is kept ON with the current $I_{CHG25}$.
- A MOSFET is kept OFF with the current $I_{CHG25}$.

### 12.2.1 Static activation of a high-side MOSFET

**Turn-on with cross-current protection**

If LSx is ON (HBxMODE[1:0] = $01_B$), before the activation of HSx (HBxMODE[1:0] = $10_B$) then the high-side MOSFET is turned on after a cross-current protection time (refer to **Figure 43**):

- After the CSN rising edge and for the duration $t_{HBxCCP\ ACTIVE}$ :
  - The high-side MOSFET is kept OFF with the current -ICHGSTx.
  - The gate of the low-side MOSFET is discharged with the current -ICHGSTx.
- At the end of $t_{HBxCCP\ ACTIVE}$ and for the duration $t_{HBxBLANK\ ACTIVE}$ + $t_{FVDS}$:
  - The gate of the high-side MOSFET is charged with the current ICHGSTx.
  - Low-side MOSFET is kept OFF with the current -IHARDOFF (hard off phase).
- At the end of $t_{FVDS}$:
  - The drive current of the high-side MOSFET is reduced to IHOLD.
  - The drive current of the low-side MOSFET is set to -IHOLD.

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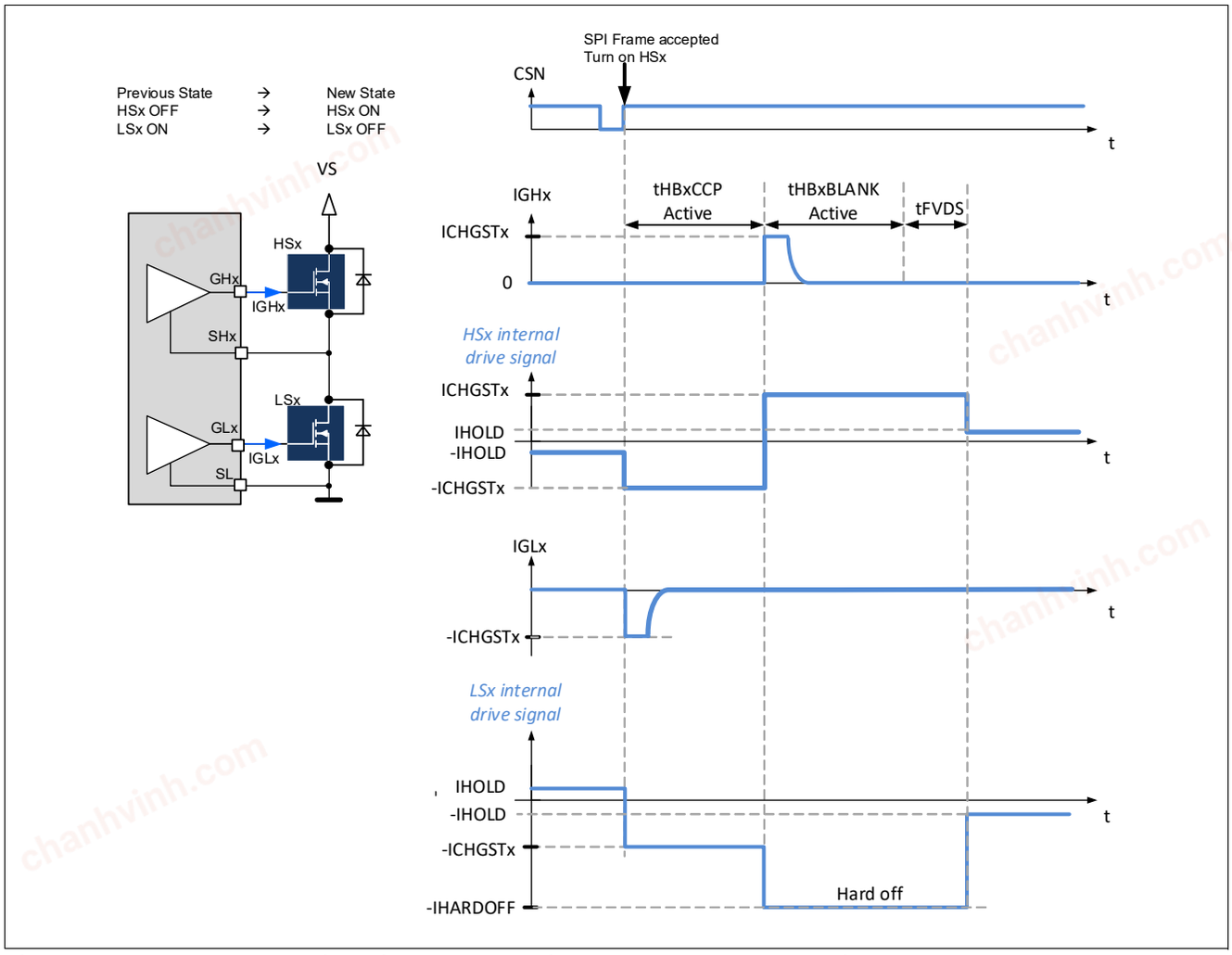



**Figure 43 Turn-on of a high-side MOSFET with cross-current protection**

*Note: The CSN rising edge must be synchronized with the device logic. Therefore SPI commands are executed with a delay of up to 3 µs after the CSN rising edge.*

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### Turn-on without cross-current protection

If LSx is OFF (HBxMODE[1:0] = $11_B$), before the activation of HSx (HBxMODE[1:0] = $10_B$), then the high-side MOSFET is turned on without cross-current protection (refer to **Figure 44**):

- right after the CSN rising edge and for a duration $t_{HBxBLANK\ ACTIVE} + t_{FVDS}$:
  - The gate of the high-side MOSFET is charged with the current ICHGSTx.
  - The low-side MOSFET is kept OFF with the current -IHARDOFF.
- At the end of $t_{FVDS}$:
  - The drive current of the high-side MOSFET is reduced to IHOLD.
  - The drive current of the low-side MOSFET is set to -IHOLD.

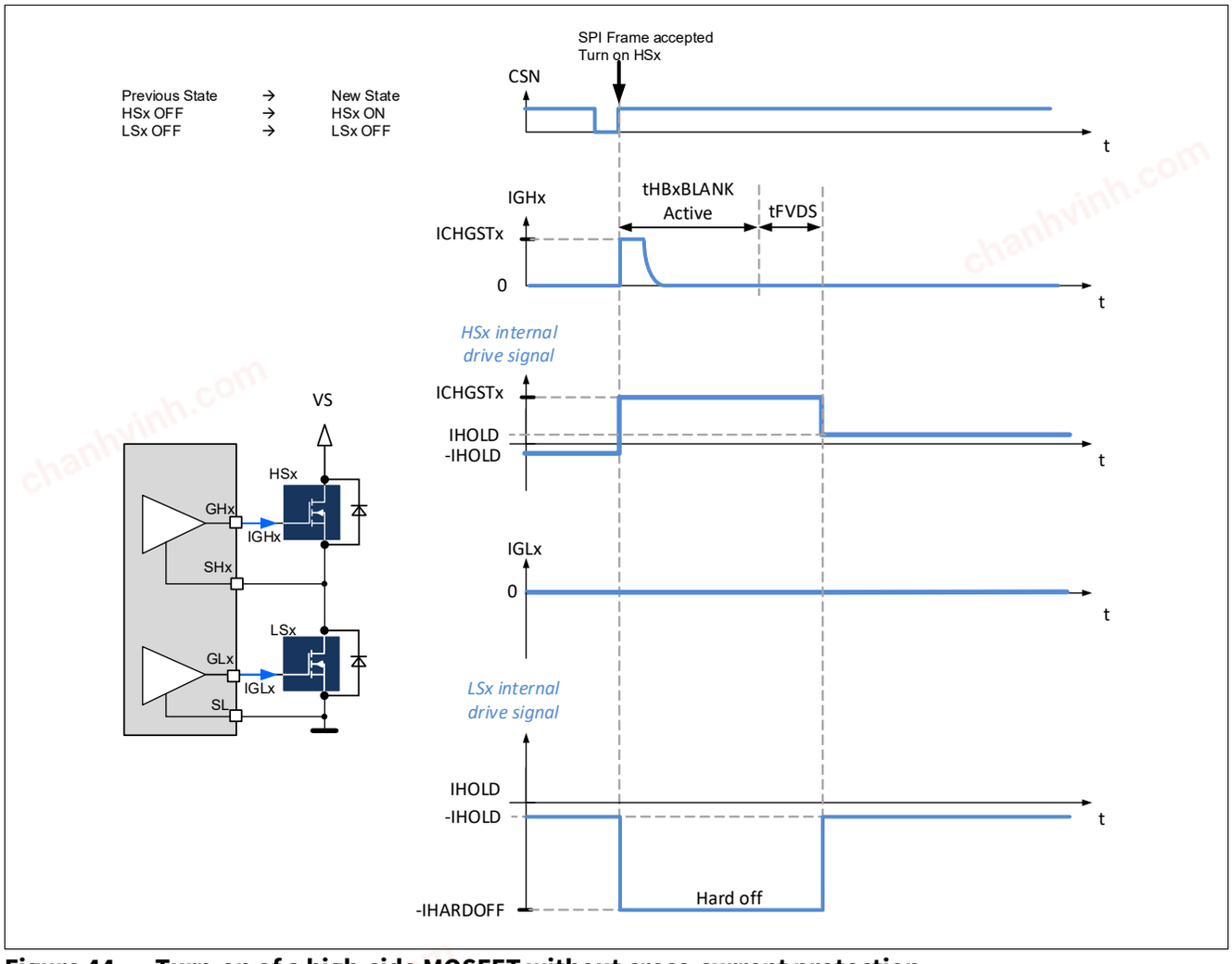



**Figure 44 Turn-on of a high-side MOSFET without cross-current protection**

*Note: The CSN rising edge must be synchronized with the device logic. Therefore SPI commands are executed with a delay of up to 3 µs after the CSN rising edge.*

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### 12.2.2 Static activation of a low-side MOSFET

The description of the static activation of a low-side x differs from the description of **Chapter 12.2.1** only by exchanging high-side x and low-side x.

### 12.2.3 Turn-off of the high-side and low-side MOSFETs of a half-bridge

When the TLE9562QX receives a SPI command to turn-off both the high-side and low-side MOSFETs of the half-bridge x (HBxMODE[1:0] = (0,0) or (1,1)):

- The gate of HSx and LSx are discharged with the current -ICHGSTx for the duration $t_{HBxCCP\ ACTIVE}$ (**Figure 45**).
- At the end of $t_{HBxCCP\ ACTIVE}$, the drive current of HSx and LSx are reduced to -IHOLD.

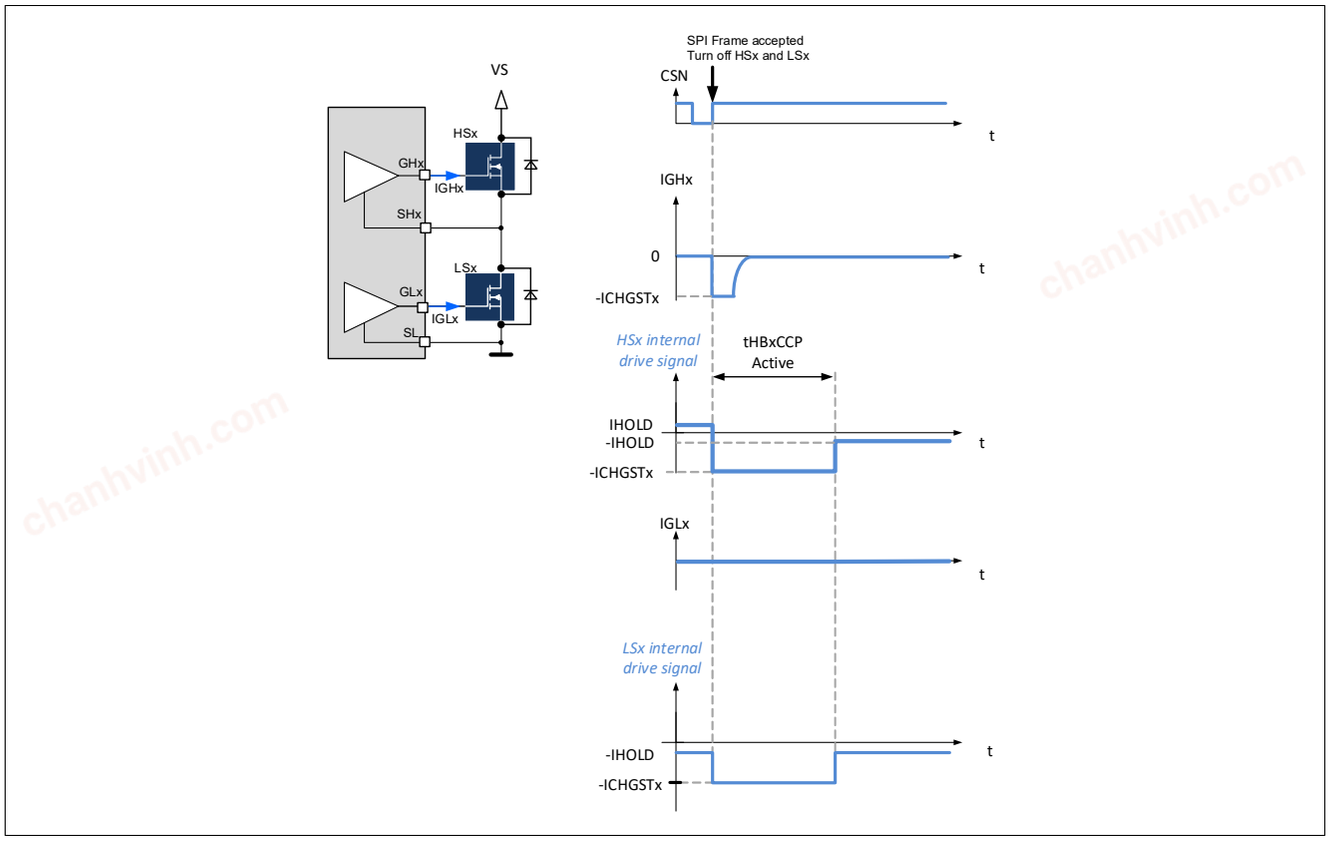



**Figure 45 Turn-off of the high-side and low-side MOSFETs of a half-bridge**

*Note: The CSN rising edge must be synchronized with the device logic. Therefore SPI commands are executed with a delay of up to 3 µs after the CSN rising edge.*

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## 12.3 PWM operation

The pins PWMx provide the PWM signal for each PWM channel.

Each half-bridge is activated in PWM mode by setting the corresponding HBx_PWM_EN bit (**HBMODE**).

### 12.3.1 Determination of the active and freewheeling MOSFET

If **EN_GEN_CHECK** = 1, right before each MOSFET activation, the device detects which MOSFET of the half-bridge is the active MOSFET and which MOSFET is the free-wheeling (FW) MOSFET (**Figure 46**):

- If VSHx > $V_{SHH}$ : The high-side MOSFET is the FW MOSFET and the low-side MOSFET is the active MOSFET.
- If VSHx < $V_{SHL}$: Then the low-side MOSFET is the FW MOSFET and the high-side MOSFET is the active MOSFET.
- If $V_{SHL}$ < VSHx < $V_{SHH}$: No clear distinction between the active FW MOSFET and the active MOSFET. The next MOSFET to be turned on is turned on as if it was the active MOSFET.
- No distinction between active MOSFET and FW MOSFET is possible (and the PWM MOSFET is considered as the active MOSFET), if:
  - the ON-time of the external PWM signal is shorter than tHBxCCP FW
  - the OFF-time of the external PWM signal is shorter than tHBxCCP Active

*Note: The PWM signal is applied to the MOSFET selected by HBxMODE[1:0], independently from the free-wheeling and the active MOSFET.*

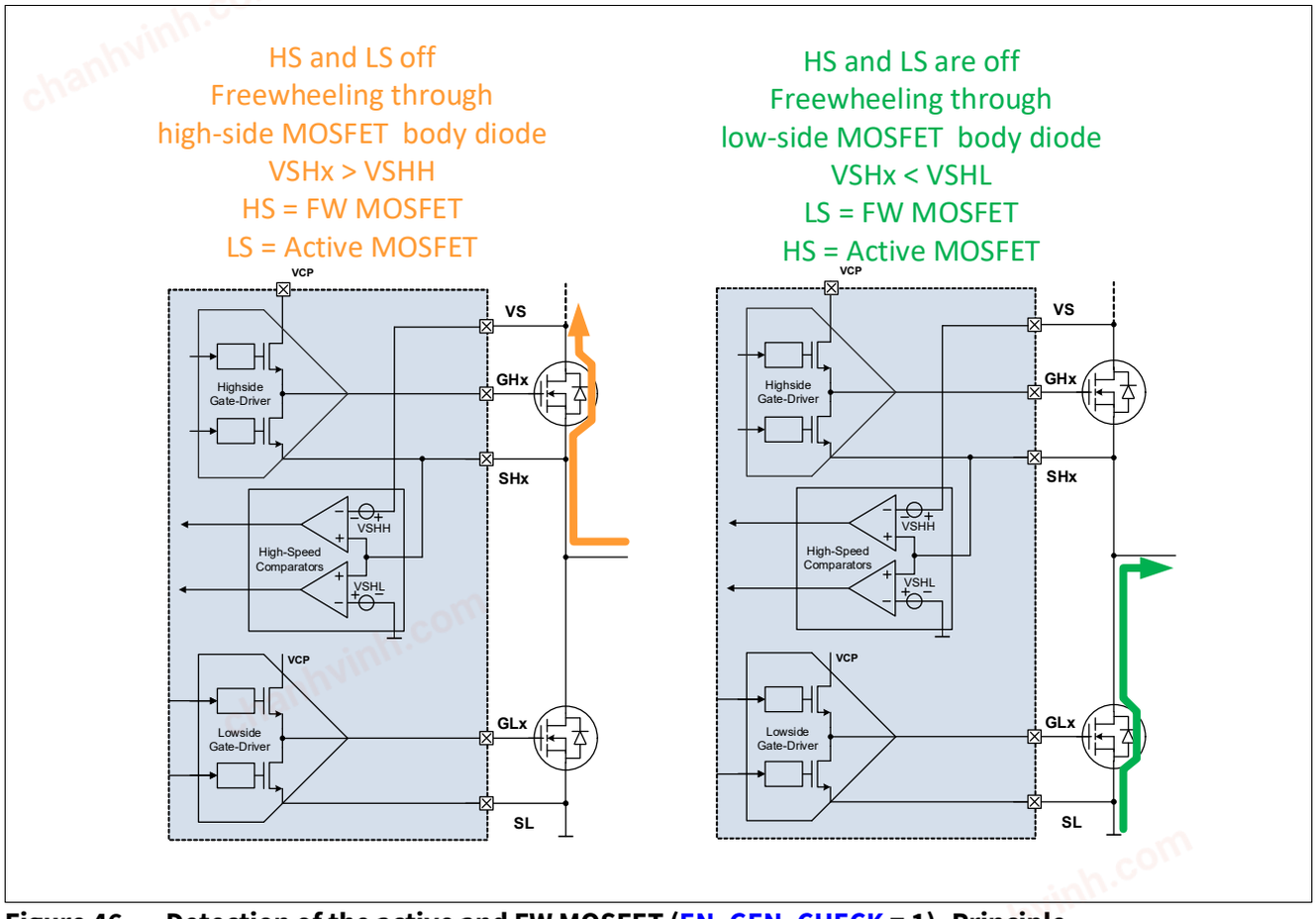



**Figure 46 Detection of the active and FW MOSFET (EN_GEN_CHECK = 1)- Principle**

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**Figure 47** and **Figure 48** show examples of free-wheeling and active MOSFET when the motor operates as load.

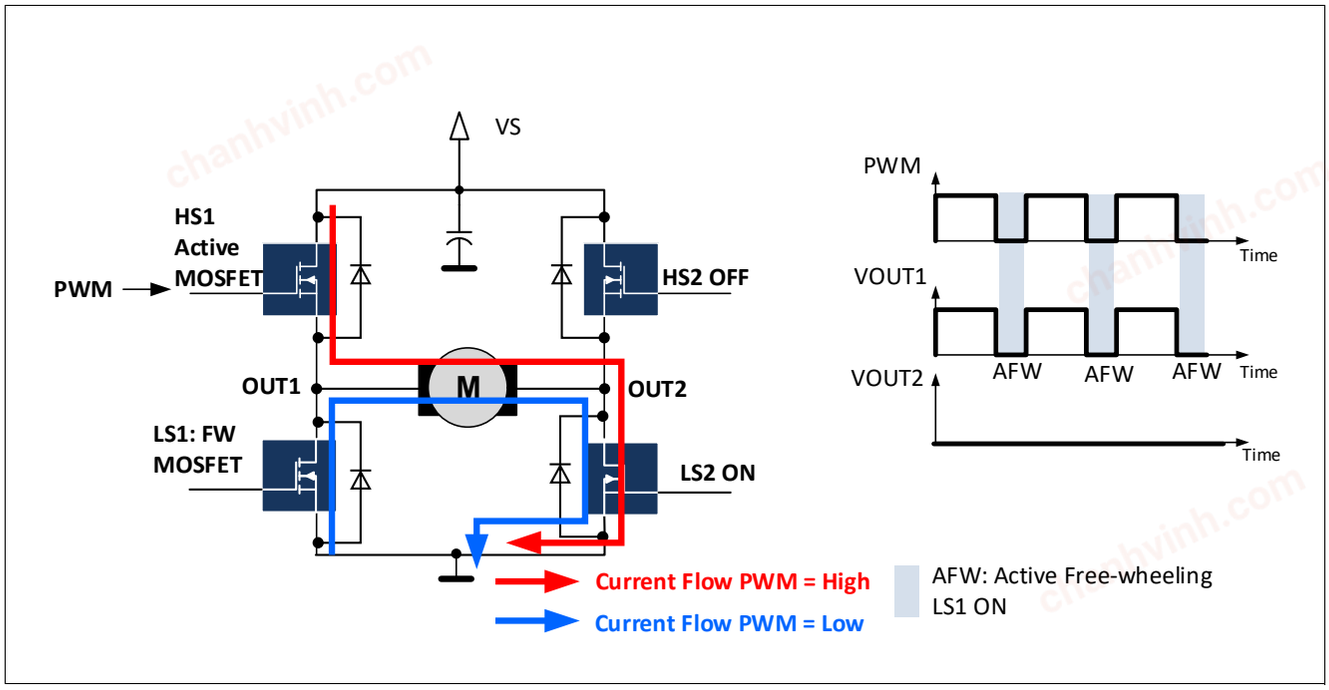



**Figure 47 Active freewheeling on HB1: AFW1 = 1, HB1_PWM_EN = 1. PWM applied to HS1 (HB1MODE[1:0] = $10_B$). The motor operates as load: HS1 is the active MOSFET, LS1 is the FW MOSFET.**

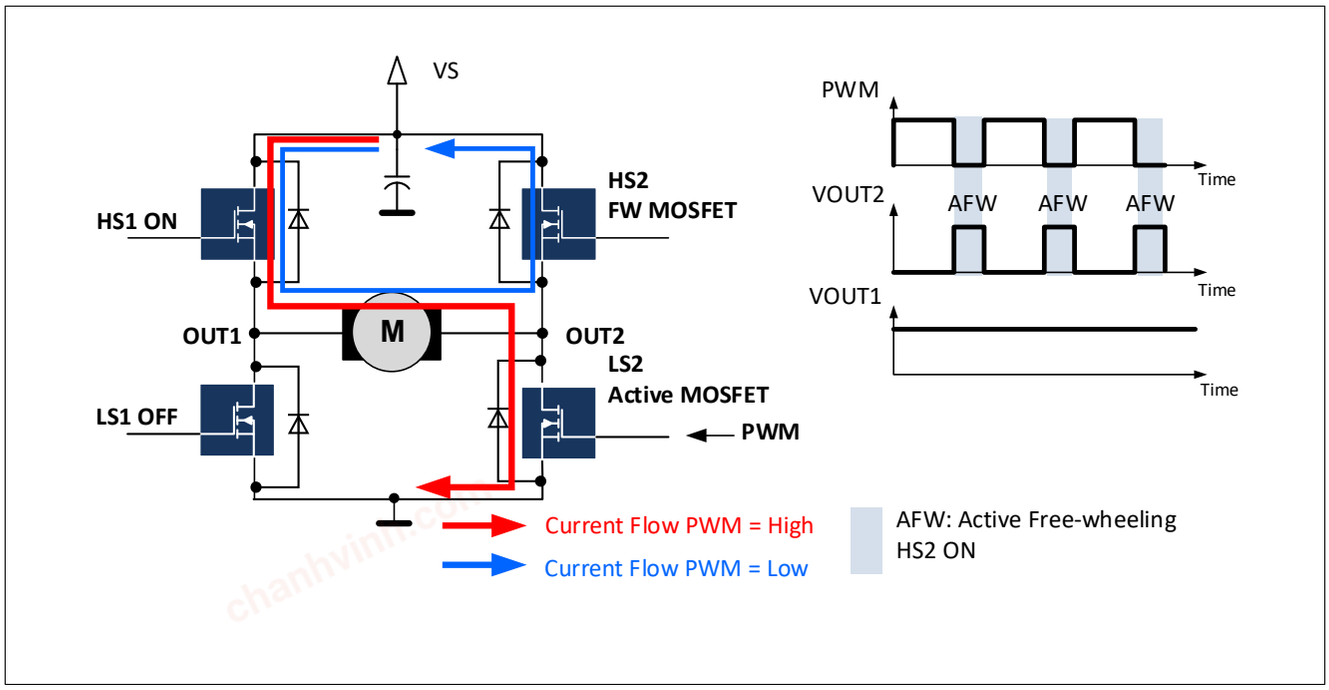



**Figure 48 Active freewheeling on HB2: AFW2 = 1, HB1_PWM_EN = 1. PWM applied to LS2 (HB2MODE[1:0] = $01_B$). The motor operates as load: LS2 is the active MOSFET, HS2 is the FW MOSFET.**

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**Figure 49** and **Figure 50** show examples of free-wheeling and active MOSFETs when the motor operates as generator.

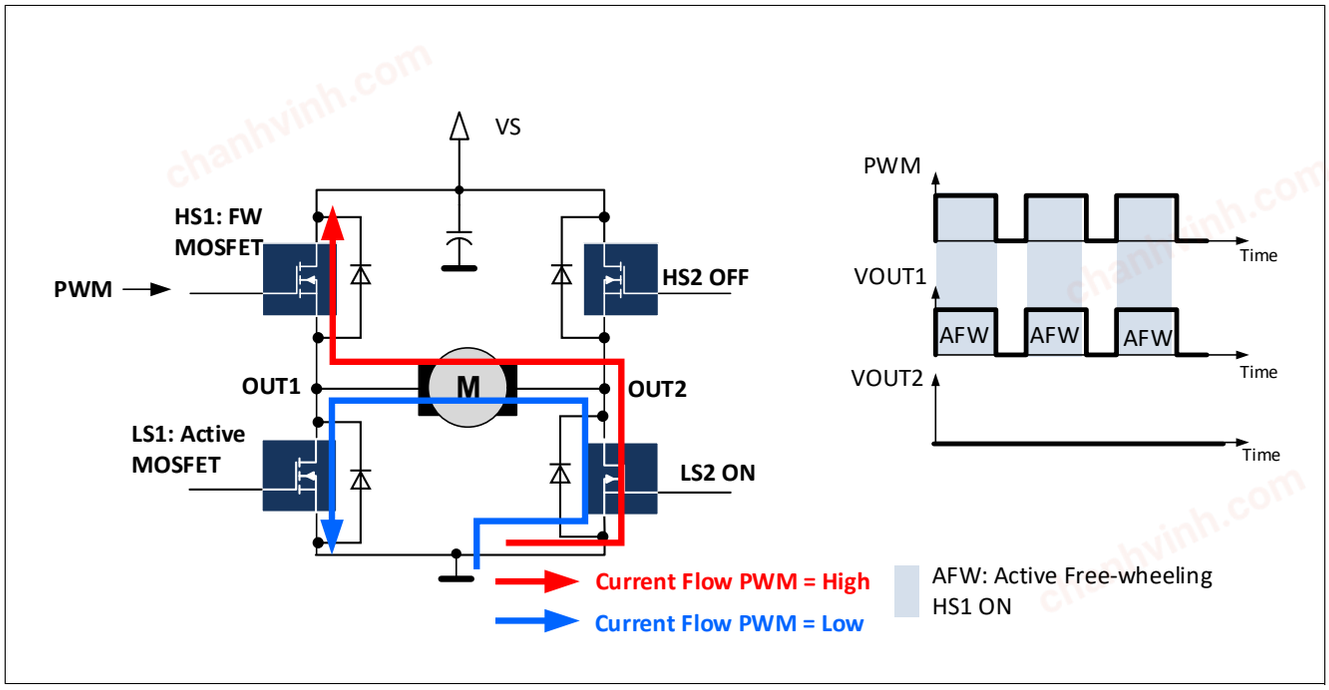



**Figure 49 Active freewheeling on HB1: AFW1 = 1, HB1_PWM_EN = 1. PWM applied to HS1 (HB1MODE[1:0] = $10_B$), EN_GEN_CHECK = 1.The motor operates as generator: LS1 is the active MOSFET, HS1 is the FW MOSFET.**

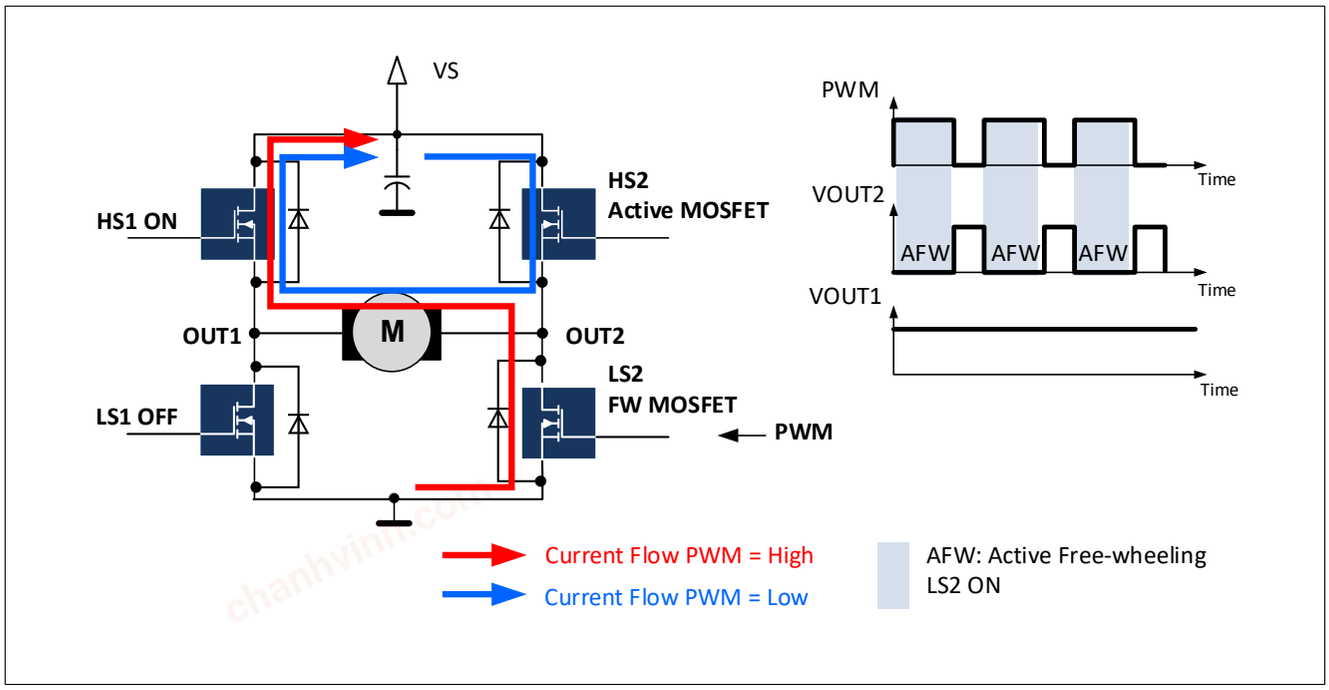



**Figure 50 Active freewheeling on HB2: AFW2 = 1, HB1_PWM_EN = 1. PWM applied to LS2 (HB2MODE[1:0] = $01_B$), EN_GEN_CHECK = 1. The motor operates as generator: HS2 is the active MOSFET, LS2 is the FW MOSFET.**

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### 12.3.2 Configurations in PWM mode

The following sections describe the different control schemes in PWM mode.

**Active gate control (AGC)**

The control scheme during the pre-charge and pre-discharge phases are configured by the control bits AGC[1:0]:

- Adaptive gate control (AGC[1:0] = (1,0) or (1,1), **GENCTRL**): in this mode a pre-charge current and a pre-discharge current are applied to the gate of the active MOSFET. These currents are used to regulate the turn-on and turn-off delays to the respective target values. Refer to **Chapter 12.3.4**.
- No adaptive gate control (AGC[1;0] = (0,0)): in this mode, the pre-charge and pre-discharge phases (of the active MOSFET) are deactivated. Refer to **Chapter 12.3.5**.
- No adaptive gate control (AGC[1;0] = (0,1)). In this mode:
  - During the pre-charge phase, the gate of the active MOSFET is charged with the configured current IPCHGINIT (**HB_PCHG_INIT**).
  - During the pre-discharge phase, the gate of the active MOSFET is discharged with the configured current IPDCHGINIT (**HB_PCHG_INIT**).

*Note: It is recommended to configure tPCHGx < tHBxBLANK Active and tPDCHGx < tHBxCCP Active (Refer to **TPRECHG** and **CCP_BLK**) independently from the AGC settings.*

**Active free-wheeling (AFW)**

The active free-wheeling is activated for HBx if the AFWx and HBx_PWM_EN (**HBMODE**) are set to 1 to reduce the power dissipation of the free-wheeling MOSFET. If an active MOSFET is OFF, the opposite MOSFET of the same half-bridge is actively turned on. See examples of high-side and low-side PWM operation in **Figure 47** and **Figure 48**.

If AFWx = 1, a cross-current protection time is applied to HBx (set by **CCP_BLK**) during the PWM operation.

If AFWx = 0, no cross current protection is applied to HBx during the PWM operation.

AFWx can be changed either when HBx is in high impedance or when one of the HBx MOSFETs is on:

- In motor mode :
  - If AFWx is changed from 1 to 0: then the new value of AFWx is read and latched at the end to tCCP FW which follows the PWM rising edge.
  - If AFWx is changed from 0 to 1: then the new value of AFWx is read and latched at the PWM rising edge.
- In generator mode (**EN_GEN_CHECK** = 1): If AFWx is changed from 0 to 1 or from 1 to 0, then the new value of AFWx is read and latched at the end to tCCP active which follows a PWM rising edge.

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### Post-charge

A post-charge is initiated if **POCHGDIS** is set to 0 (**GENCTRL**) to reach the minimum MOSFET Rdson.

- **POCHGDIS** = 0: The post-charge phase is initiated at the end of the turn-on of the active MOSFET. The charge current is increased by one current step at every bridge driver clock cycle (**BDFREQ**) to ICHGMAXx.
- **POCHGDIS** = 1: The post-charge phase is disabled. The charge current is kept to ICHGx.

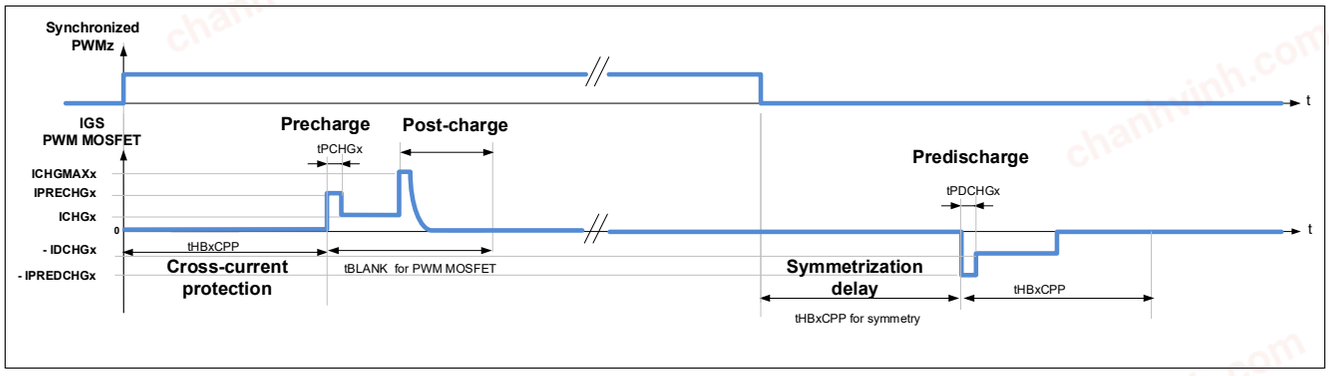



**Figure 51 PWM overview - AGC = $10_B$ or $11_B$, POCHGDIS=0, AFWx = 1**

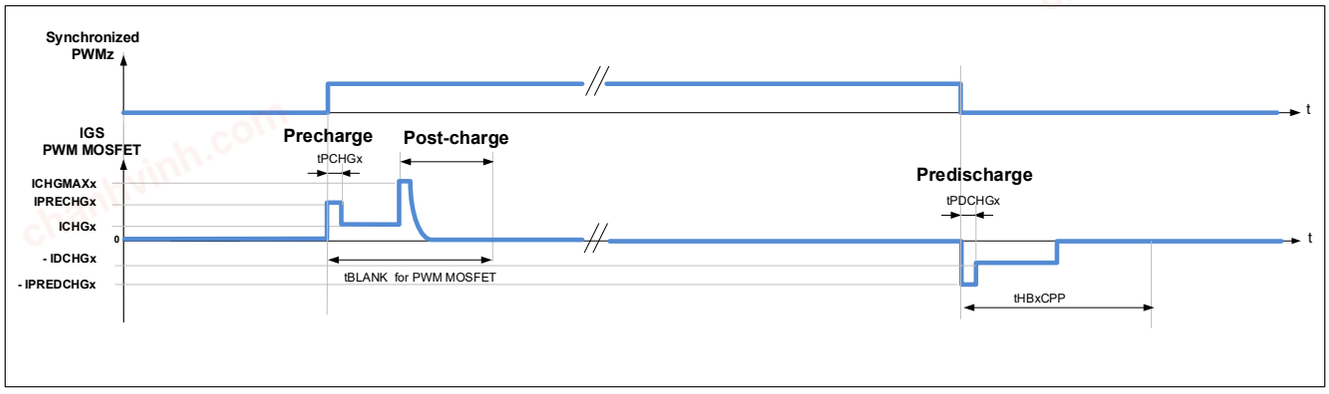



**Figure 52 PWM overview - AGC = $10_B$ or $11_B$, POCHGDIS=0, AFWx = 0**

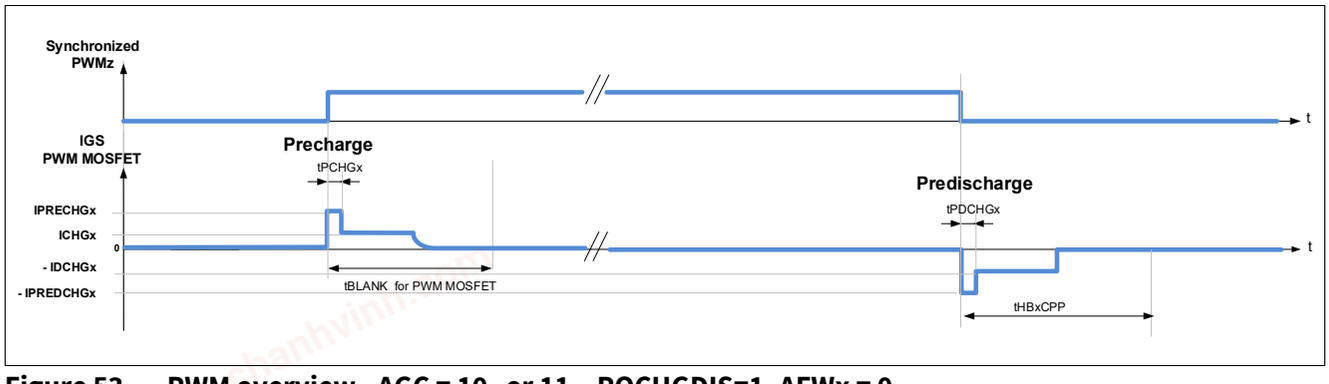



**Figure 53 PWM overview - AGC = $10_B$ or $11_B$, POCHGDIS=1, AFWx = 0**

## 12.3.3 PWM mapping

The PWM inputs can be mapped by different half-bridges by setting the configuration bits PWM12MAP and PWM34MAP in **GENCTRL**.

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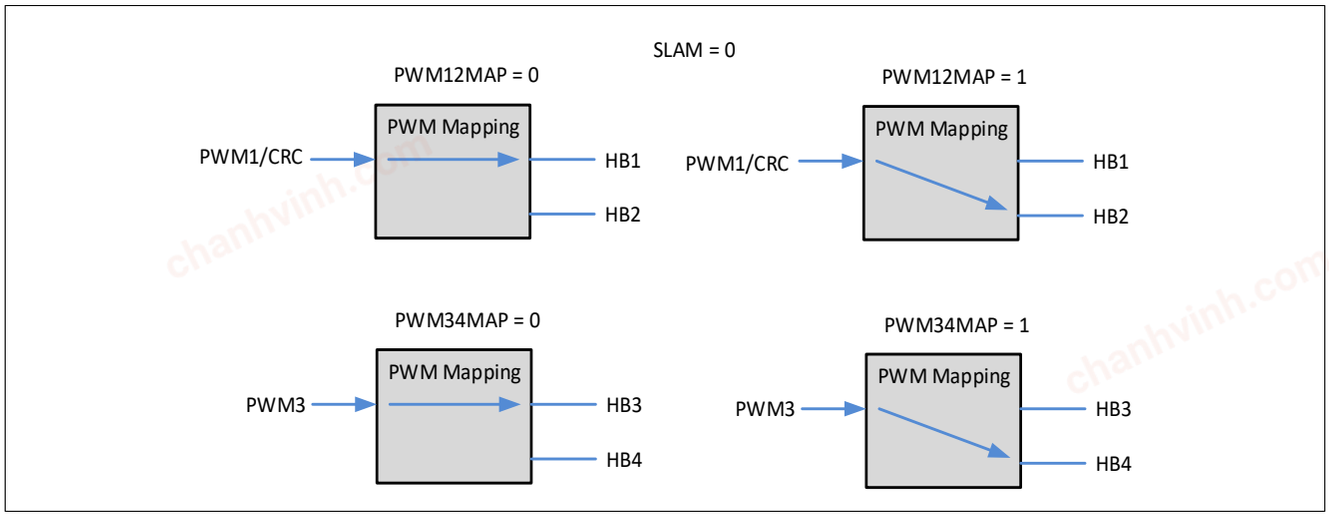



**Figure 54 PWM input mapping TLE9562QXC**

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### 12.3.4 PWM operation with adaptive gate control

This section describes the MOSFETs control during high-side or low-side PWM operation when the adaptive gate control is enabled (AGC[1:0] = (1,0) or (1,1), **GENCTRL**).

Assumption: A high-side or low-side MOSFET is mapped to the PWM input PWMz.

The TLE9562QX adapts the pre-charge current, respectively the pre-discharge current, in order to match the effective turn-on delay ($t_{DON}$) and turn-off delay ($t_{DOFF}$) to the configured values.

The configured turn-on and turn-off delays of the respective PWM MOSFETs are set by the registers **TDON_HB_CTRL** and **TDOFF_HB_CTRL**.

The effective turn-on and turn-off delays of the respective PWM MOSFETs are read out from the status registers EFF_TDON_OFFx.

**Table 23 Abbreviations for adaptive turn-on and turn-off phases in PWM configuration**

| Abbreviation | Definition |
|---|---|
| Suffix x | Related to the half-bridge x. |
| Suffix z | Related to the PWM input z. |
| VGS_HSx | Gate-Source voltage of high-side MOSFET x. |
| IGS_HSx | Gate current of high-side MOSFET x.<br>IGS_HSx is positive when the current flows out of GHx. |
| VGS_LSx | Gate-Source voltage of low-side MOSFET x. |
| IGS_LSx | Gate current of low-side MOSFET x.<br>IGS_LSx is positive when the current flows out of GLx. |
| tPWM_SYNCH | Synchronization delay between external and internal PWM signal. |
| tHBxCCP ACTIVE | Active cross-current protection time of HBx. See control register **CCP_BLK**. |
| tHBxBLANK ACTIVE | Active Drain-source overvoltage blank time of HBx. See control register and **CCP_BLK**. |
| tHBxCCP FW | Freewheeling cross-current protection time of HBx. See control register **CCP_BLK**. |
| tHBxBLANK FW | Freewheeling drain-source overvoltage blank time of HBx. See control register and **CCP_BLK**. |
| PWMz | External PWM signal applied to the input pin PWMz. |
| ICHGMAXx | Maximum drive current of the half-bridge x during the pre-charge and pre-discharge phases. See control register **HB_ICHG_MAX**.<br>IPRECHGx and IPREDCHGx are limited to ICHGMAXx. |
| IPRECHGx | Pre-charge current sourced by the gate driver to the active MOSFET of the half-bridge x during tPCHGx (**TPRECHG**).<br>Internal and self-adaptive parameter (if AGC[1:0] = (1,0) or (1,1), **GENCTRL**).<br>IPRECHGx is clamped between $I_{CHG0}$ (0.5 mA typ.) and ICHGMAXx. |
| IPCHGINITx | Initial value of IPRECHGx. Refer to **HB_PCHG_INIT**. |
| IPREDCHGx | Pre-discharge-current sunk by the gate driver mapped to the half-bridge x during tPDCHGx.<br>Internal and self-adaptive parameter (if AGC[1:0] = (1,0) or (1,1), **GENCTRL**).<br>IPREDCHGx is clamped between $I_{DCHG0}$ (0.5 mA typ.) and ICHGMAXx. |
| IPDCHGINITx | Initial value of IPREDCHGx. Refer to **HB_PCHG_INIT**. |

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**Table 23 Abbreviations for adaptive turn-on and turn-off phases in PWM configuration** (cont'd)

| Abbreviation | Definition |
|---|---|
| ICHGx | Current sourced by the gate driver to the active MOSFET of the half-bridge x during the charge phase. See control register **HB_ICHG**. |
| IDCHGx | Current sunk by the gate driver to turn-off the active MOSFET of the half-bridge x during the discharge phase. See control register **HB_ICHG**. |
| ICHGFWx | Current sourced or sunk by the gate driver to turn on / turn off the freewheeling MOSFET of the half-bridge x. See control register **HB_ICHG**. |
| tPCHGx | Duration of the pre-charge phase of half-bridge x.<br>tPCHGx is configurable by SPI. See control register **TPRECHG**. |
| tPDCHGx | Duration of the pre-discharge phase of half-bridge x.<br>tPDCHGx is configurable by SPI. See control register **TPRECHG**. |
| tDONx | Turn-on delay of the active MOSFET of HBx. |
| tDOFFx | Turn-off delay of the active MOSFET of HBx. |
| IHOLD | Hold current sourced or sunk by the gate driver to keep the MOSFET in the desired state. See **IHOLD** control bit in **GENCTRL**. |
| IHARDOFF | IHARDOFF is the maximum current that the gate drivers can sink. It corresponds to the discharge current when IDCHGx[5:0] = $63_D$ (100 mA typ.). |
| TFVDS | Drain-Source overvoltage filter time. See **LS_VDS**. |

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### 12.3.4.1 High-side PWM with adaptive gate control, motor operating as load

The following section describes the MOSFET control when the PWM signal is applied to the high-side MOSFET of one half-bridge while the motor operates as a load.

Assumption: the PWM input z is mapped to the high-side MOSFET of the half-bridge x.

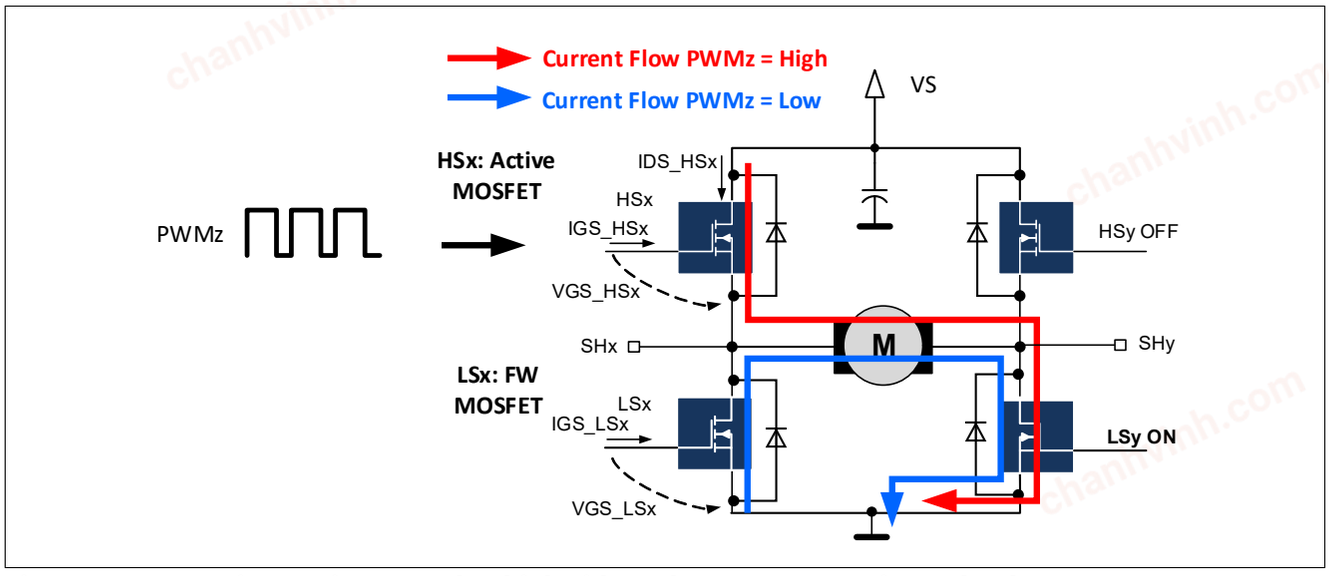



**Figure 55 PWM input z is mapped to high-side x, the motor operating as load**

#### 12.3.4.1.1 High-side PWM with adaptive gate control and active free-wheeling

This section describes the MOSFETs control scheme applied to HBx with active free-wheeling (AFWx = 1).

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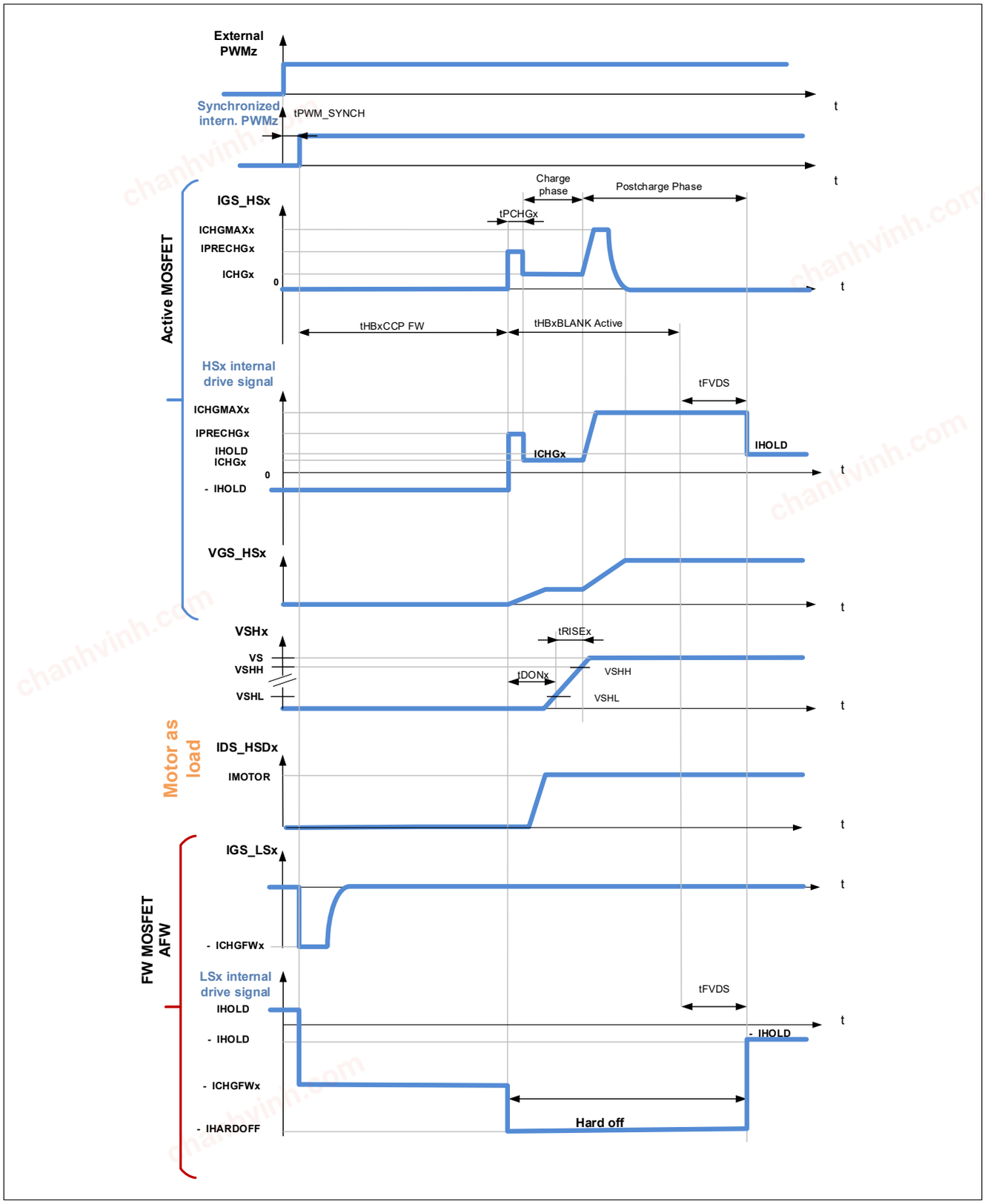



**Figure 56 Adaptive turn-on with high-side PWM, AGC[1:0] = (1,0) or (1,1), AFWx=1, POCHGDIS=0, motor operating as load**

### Adaptive turn-on during high-side PWM

The turn-on of the high-side MOSFET is done in four phases (Refer to **Figure 56**):

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1. **Cross-current protection phase**: The cross-current protection tHBxCCP FW starts at the rising edge of PWMz. During tHBxCCP FW, the low-side MOSFET x is turned off with the discharge current - ICHGFWx, while the high-side MOSFET x is kept off.
2. **Pre-charge:** [1]Once tHBxCCP FW has elapsed, the gate of the high-side MOSFET x is pre-charged with the current IPRECHGx for a duration tPCHGx. IPRECHGx[2] is an internal parameter, which is self-adaptive (see next phase).
3. **Charge:** After tPCHGx, the charge current is decreased from IPRECHGx down to ICHGx. The effective tDONx[3] is measured and compared to the configured tDONx for the automatic adaptation of IPRECHGx (see **Adaptive control of pre-charge current**). The charge phase ends up when $V_{SHx}$ reaches $V_{SHH}$ (typically $V_S$ - 2.25 V)
4. **Post-charge:** After the charge phase, the control signal for the charge current of HSx is increased by one current step at every bridge driver clock cycle (**BDFREQ**) to ICHGMAXx until the end of tFVDS.

### Adaptive control of pre-charge current

Refer to **Chapter 12.3.6** for information on the pre-discharge currents.

The pre-charge current IPRECHGx is a self-adaptive parameter if AGC[1:0] = (1,0) or (1,1) (see **GENCTRL**). It is applied during tPCHGx (see **TPRECHG**). The TLE9562QX adapts the IPRECHGx to match the effective tDONx to the configured value.

IPRECHGx is clamped between $I_{CHG0}$ (0.5 mA typ.) and ICHGMAXx (**HB_ICHG_MAX**).

IPRECHGx is initialized to Min(IPCHGINITx,ICHGMAXx) when the TLE9562QX receives an SPI command setting HBx_PWM_EN to 1 (see **HBMODE**). IPCHGINITx is set by the register **HB_PCHG_INIT**.

The following adaptive schemes can be selected.

AGCFILT = 0: No filter is applied:

- If the effective tDONx is longer than the configured tDONx, then IPRECHGx is increased during the next pre-charge phase.
- If the effective tDONx is shorter than the configured tDONx, then IPRECHGx is decreased during the next pre-charge phase.
- The pre-charge current is increased or decreased by one, respectively by two current steps (**Chapter 12.3.6**) if the control bit IPCHGADT in the control register **GENCTRL** is set to 0 respectively 1.

AGCFILT = 1: A filter is applied:

- If the effective tDONx **of the last two PWM cycles** are longer than the configured tDONx, then IPRECHGx is increased during the next pre-charge phase.
- If the effective tDONx **of the last two PWM cycles** are shorter than the configured tDONx, then IPRECHGx is decreased during the next pre-charge phase.
- The pre-charge current is increased or decreased by one, respectively by two current steps (**Chapter 12.3.6**) if the control bit IPCHGADT in the control register **GENCTRL** is set to 0 respectively 1.
- If none of the two cases are applicable, then IPRECHGx is unchanged during the next pre-charge phase.

1) For a correct operation, it is recommended to configure tPCHGx < tHBxBLANK Active.
2) IPRECHGx is clamped between ICHGMAXx and $I_{CHG0}$.
3) The effective tDON can be read out. Refer to **EFF_TDON_OFF1**, **EFF_TDON_OFF2**, **EFF_TDON_OFF3**, **EFF_TDON_OFF4**.

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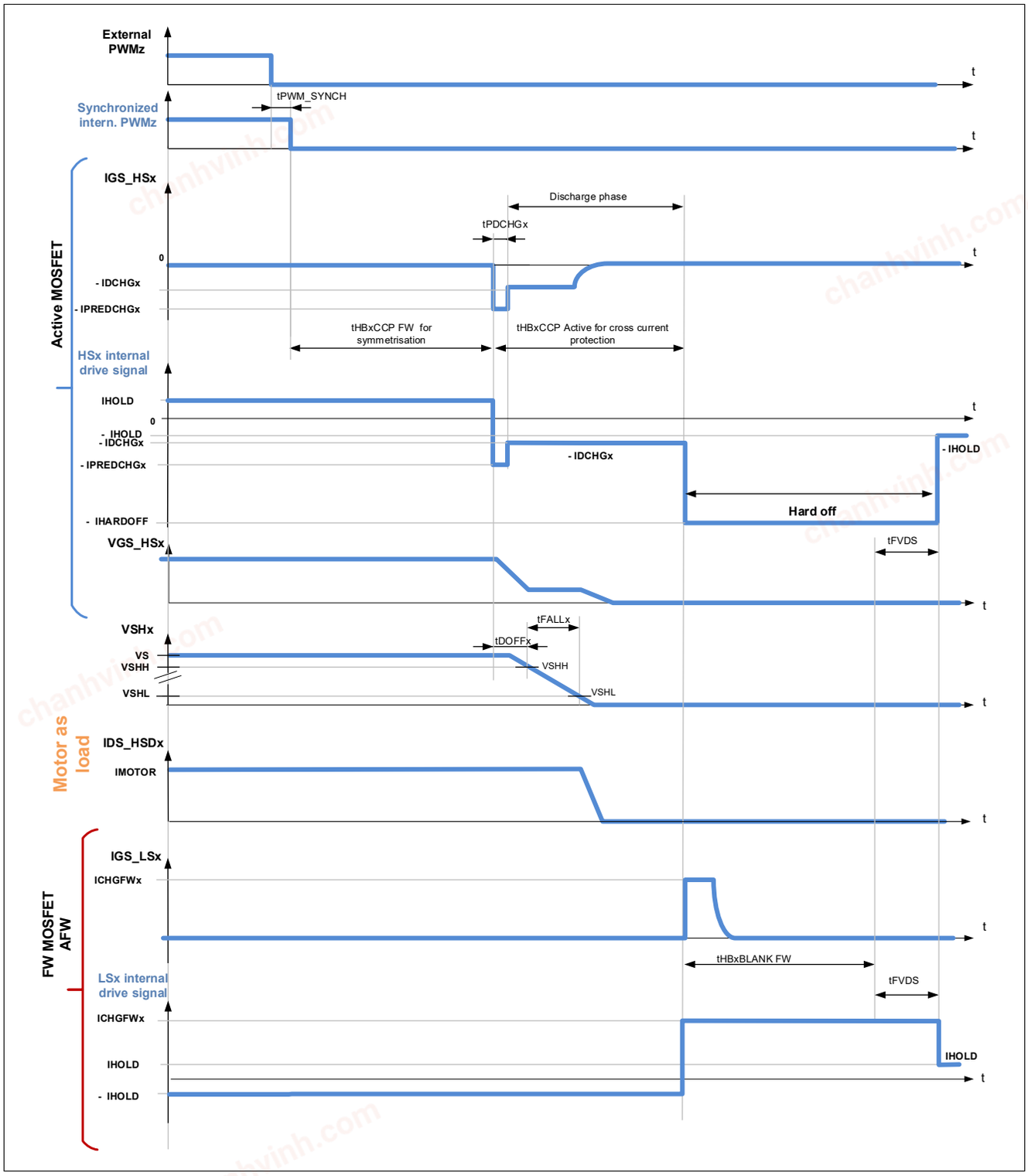



**Figure 57 Adaptive turn-off with high-side PWM, AGC[1:0] = (1,0) or (1,1), AFWx=1, motor operating as load**

### Adaptive turn-off during high-side PWM

The turn-off of the high-side MOSFET is done in four phases (Refer to **Figure 57**):

1. **Turn-off delay time for symmetrization** of the PWM signal: The turn-off of HSx is delayed by tHBxCCP FW after the falling edge of PWMz, in order to compensate the distortion caused by the cross-current protection time at turn-on.

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2. **Pre-discharge:** [1]once tHBxCCP FW for symmetrization has elapsed, the gate of the high-side MOSFET x is pre-discharged with the current - IPREDCHGx for a duration tDPCHGx. IPREDCHGx is a device internal parameter, which is self-adaptive (See next phase).
3. **Discharge:** After tPREDCHGx, the pre-discharge current is decreased in absolute value from IPREDCHGx[2] down to IDCHGx. The effective tDOFF[3] is measured and compared to the configured tDOFFx for the automatic adaptation of IPREDCHGx (see **Adaptive control of pre-discharge current**). The discharge phase ends up at expiration of tHBxCCP active for cross-current protection.
4. **Cross-current protection phase:** The cross-current protection is concurrent to the pre-discharge and discharge of the high-side MOSFET. The cross-current protection phase starts when the turn-off delay for symmetrization ends up. It has the duration tHBxCCP active . During tHBxCCP active, the low-side MOSFETx is kept OFF. When tHBxCCP active has elapsed, the gate of the low-side MOSFET x is charged with the current ICHGFWx until the end of tFVDS, provided that $V_{SHx} < V_{SHL}$.

### Adaptive control of pre-discharge current

Refer to **Chapter 12.3.6** for information on the pre-discharge currents.

The pre-discharge current IPREDCHGx is a self-adaptive parameter if AGC[1:0] = (1,0) or (1,1) (see **GENCTRL**). The TLE9562QX adapts the IPREDCHGx to match the measured $t_{DOFFx}$ to the configured value.

IPREDCHGx is clamped between $I_{DCHG0}$ (0.5 mA typ.) and ICHGMAXx (see **HB_ICHG_MAX**).

IPREDCHGx is initialized to Min(IPDCHGINITx, ICHGMAXx) when the TLE9562QX receives a SPI command setting HBx_PWM_EN to 1 (see **HBMODE**). IPDCHGINITx is set by the register **HB_PCHG_INIT**.

The pre-discharge current is increased or decreased by one, respectively by two current steps (**Chapter 12.3.6**) if the control bit IPCHGADT in the control register **GENCTRL** is set to 0 respectively 1.

The following adaptive schemes can be selected:

AGCFILT = 0: No filter is applied.

- If the effective tDOFFx is longer than the configured tDOFFx, then IPREDCHGx is increased during the next pre-discharge phase.
- If the effective tDOFFx is shorter than the configured tDOFFx, then IPREDCHGx is decreased during the next pre-discharge phase.
- The pre-charge current is increased or decreased by one, respectively by two current steps (**Chapter 12.3.6**) if the control bit IPCHGADT in the control register **GENCTRL**is set to 0 respectively 1.

AGCFILT = 1:

- If the effective tDOFFx **of the last two PWM cycles** are longer than the configured tDOFFx, then IPREDCHGx is increased during the next pre-discharge phase.
- If the effective tDOFFx **of the last two PWM cycles** are shorter than the configured tDOFFx, then IPREDCHGx is decreased during the next pre-discharge phase.
- If none of the two cases are applicable, then IPRECHGx is unchanged during the next pre-discharge phase.

1) For a correct operation, it is required to configure tPDCHGx < tHBxCCPActive.
2) IPREDCHGx is clamped between ICHGMAXx and $I_{DCHG0}$.
3) The effective tDOFF can be read out.

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- The pre-discharge current is increased or decreased by one, respectively by two current steps if the control bit IPCHGADT is set to 0 respectively 1.

#### 12.3.4.1.2 High-side PWM with adaptive gate control and passive free-wheeling

This section describes the MOSFETs control scheme with passive free-wheeling (AFWx = 0, **HBMODE**).

In contrast to the active free-wheeling, if AFWx =0, only the PWM MOSFET can be turned on, while the complementary MOSFET is always kept off.

**Turn-on of the PWM MOSFET, AFWx = 0**

If AFWx = 0, the cross-current protection time at the rising edge of the synchronized PWM signal is omitted in contrast to the active free-wheeling. The pre-charge, the charge and the post-charge phases are identical to the control scheme with active free-wheeling. Refer to **Figure 58**.

**Turn-off of the PWM MOSFET, AFWx = 0**

If AFWx = 0, the cross-current protection time at the falling edge of the synchronized PWM signal is omitted in contrast to the active free-wheeling. The pre-discharge, the discharge and the post-charge phases are identical to the control scheme with active free-wheeling. Refer to **Figure 59**.

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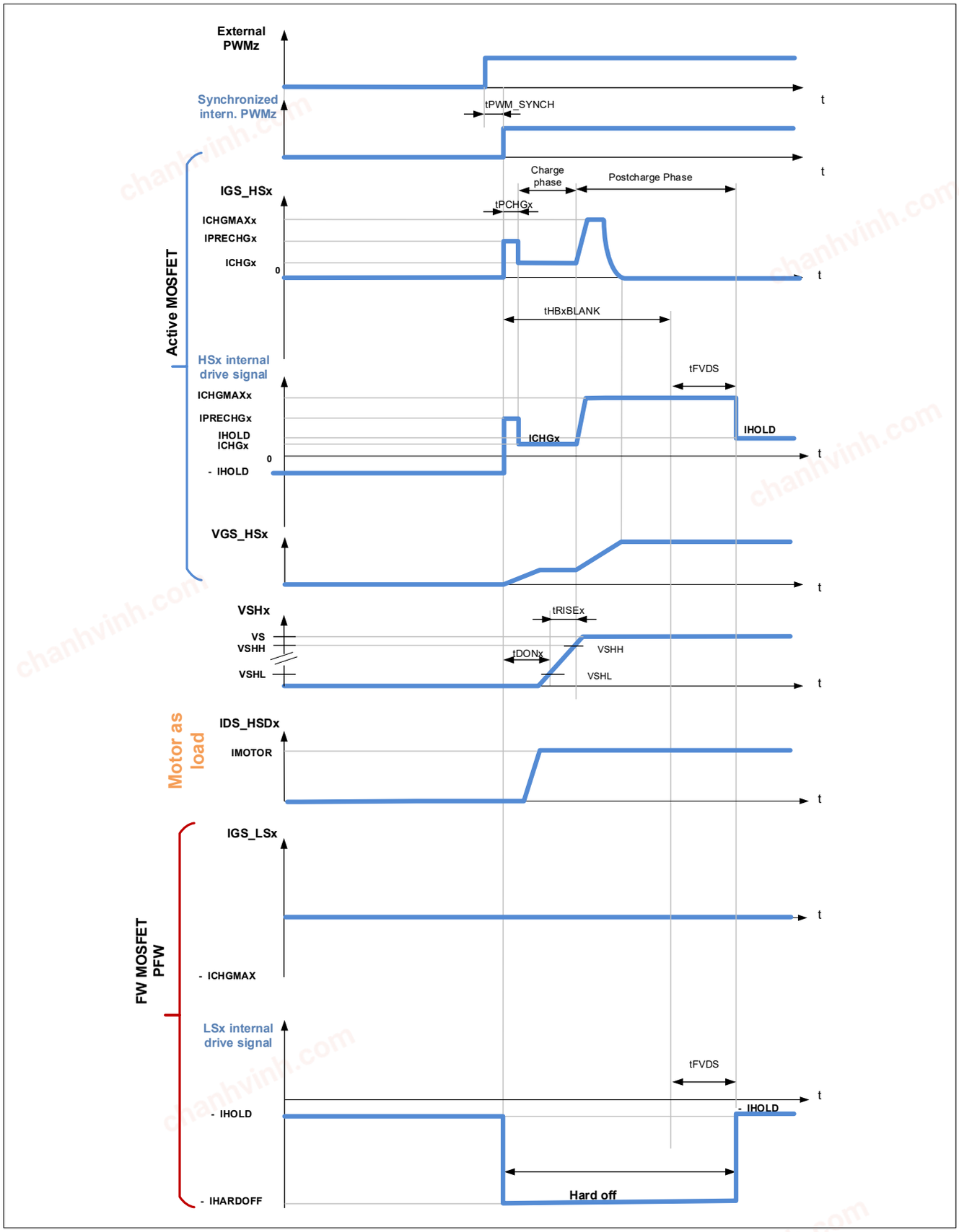



**Figure 58 Adaptive turn-on with high-side PWM, AGC[1:0] = (1,0) or (1,1), AFWx=0, POCHGDIS=0, motor operating as load**

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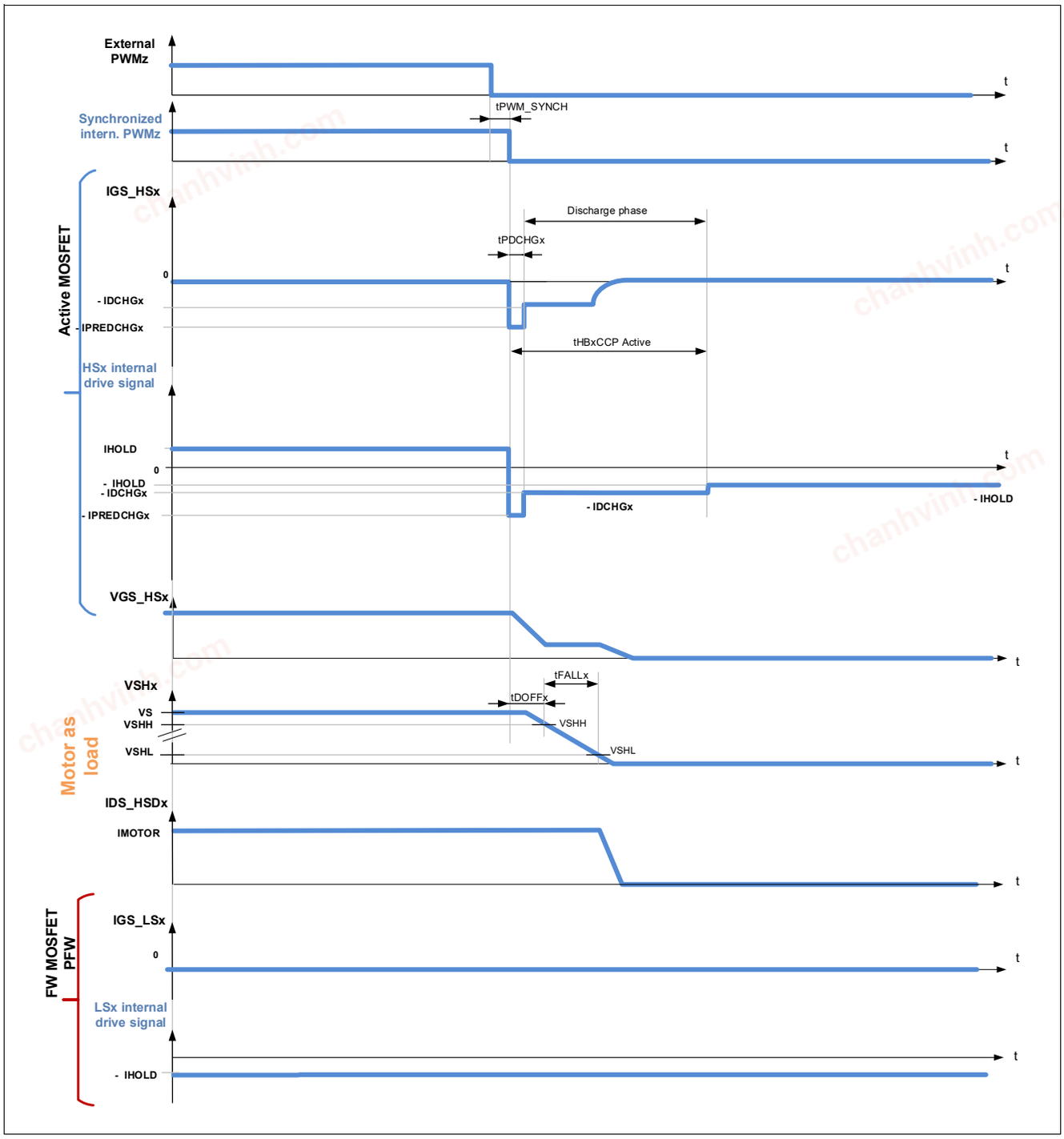



**Figure 59 Adaptive turn-off with high-side PWM, AGC[1:0] = (1,0) or (1,1), AFWx=0, motor operating as load**

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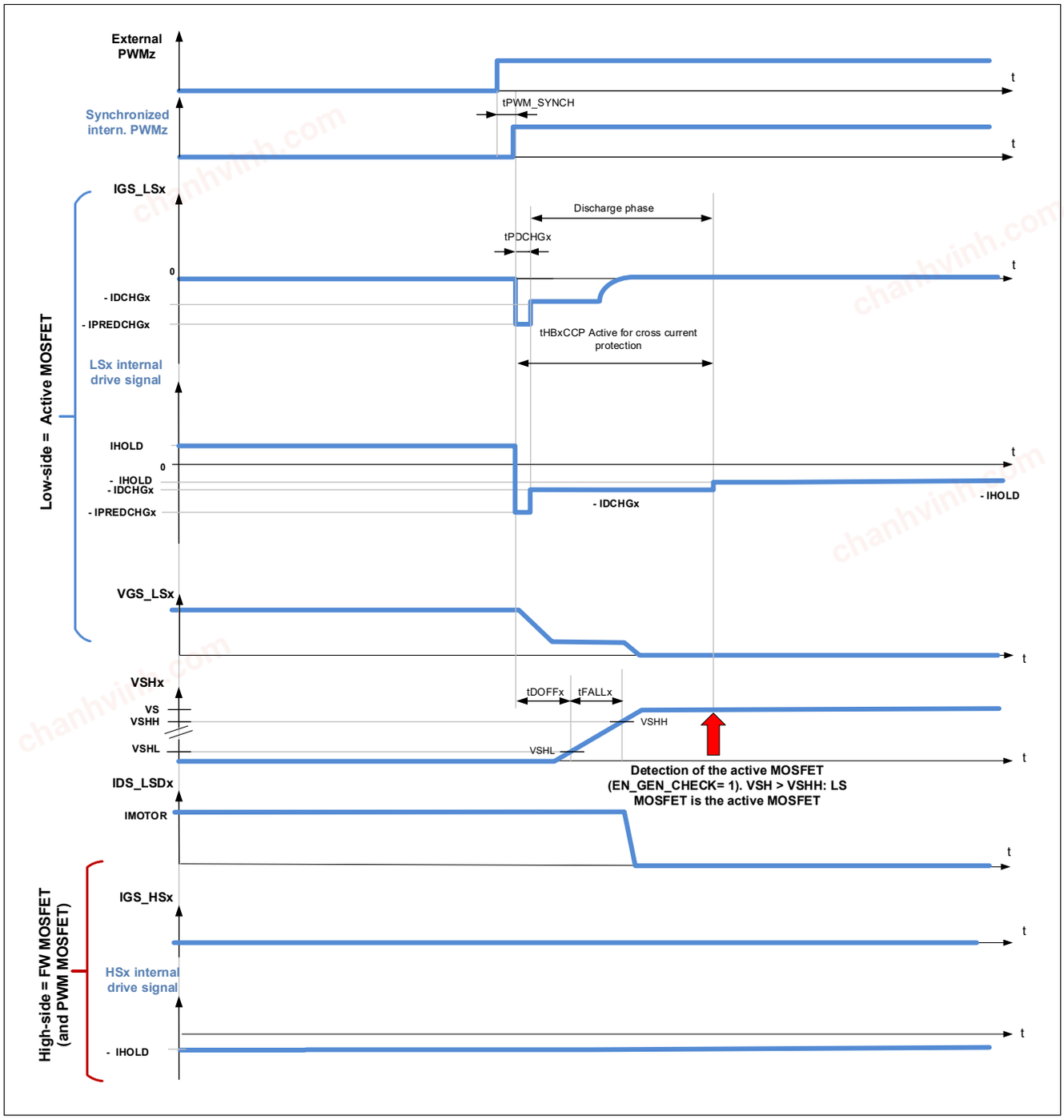



**Figure 60 PWM rising edge in generator mode with high-side PWM, adaptive gate control on, AGC[1:0] = (1,0) or (1,1), AFWx=0, POCHGDIS=0. EN_GEN_CHECK = 1. The PWM MOSFET is the FW MOSFET**

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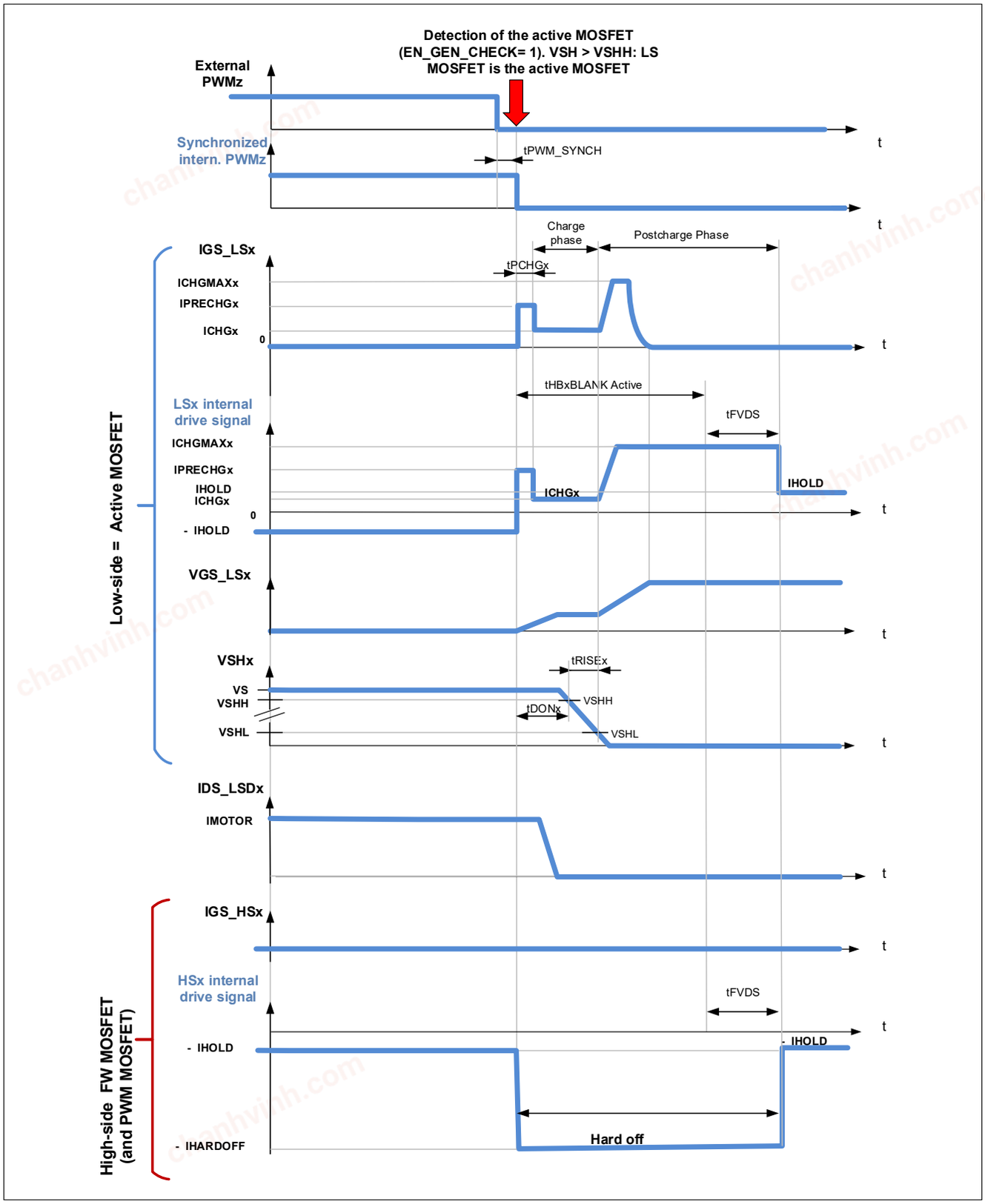



**Figure 61 PWM falling edge in generator mode with high-side PWM, adaptive gate control on, AGC[1:0] = (1,0) or (1,1), AFWx=0, POCHGDIS=0. EN_GEN_CHECK = 1. The PWM MOSFET is the FW MOSFET**

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### 12.3.4.2 Low-side PWM with adaptive gate control, motor operating as load

The following section describes the MOSFET control when the PWM signal is applied to the low-side MOSFET of one half-bridge.

Assumption: the PWM channel z is applied to the low-side MOSFET of the half-bridge x (**Figure 62**).

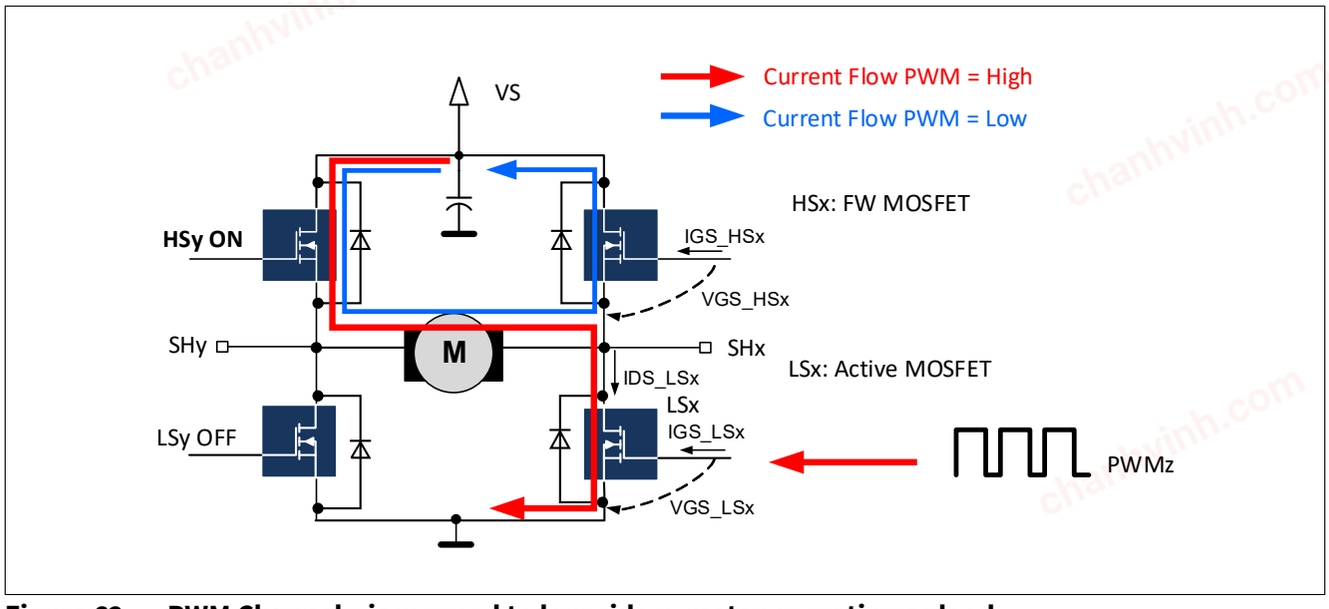



**Figure 62 PWM Channel z is mapped to low-side x, motor operating as load**

The description of the control of the PWM half-bridge differs from the description of **Chapter 12.3.4.1** only by exchanging high-side x and low-side x and thresholds $V_{SHH}$ and $V_{SHL}$.

### 12.3.4.3 High-side PWM with adaptive gate control, motor operating as generator

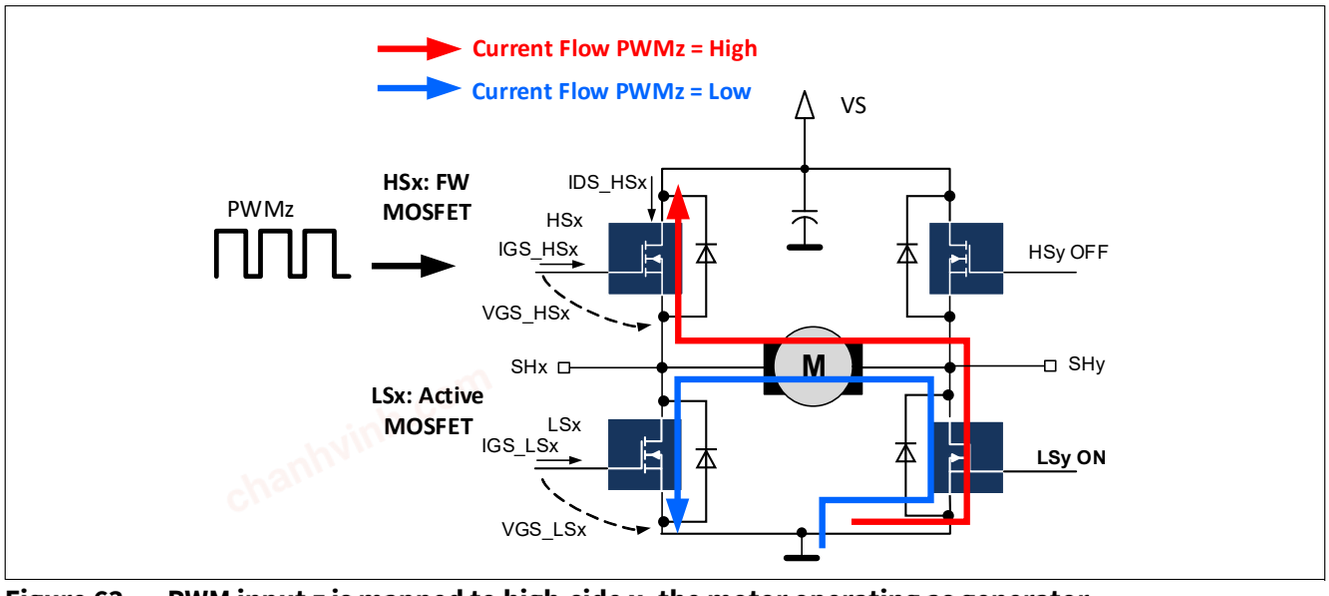



**Figure 63 PWM input z is mapped to high-side x, the motor operating as generator**

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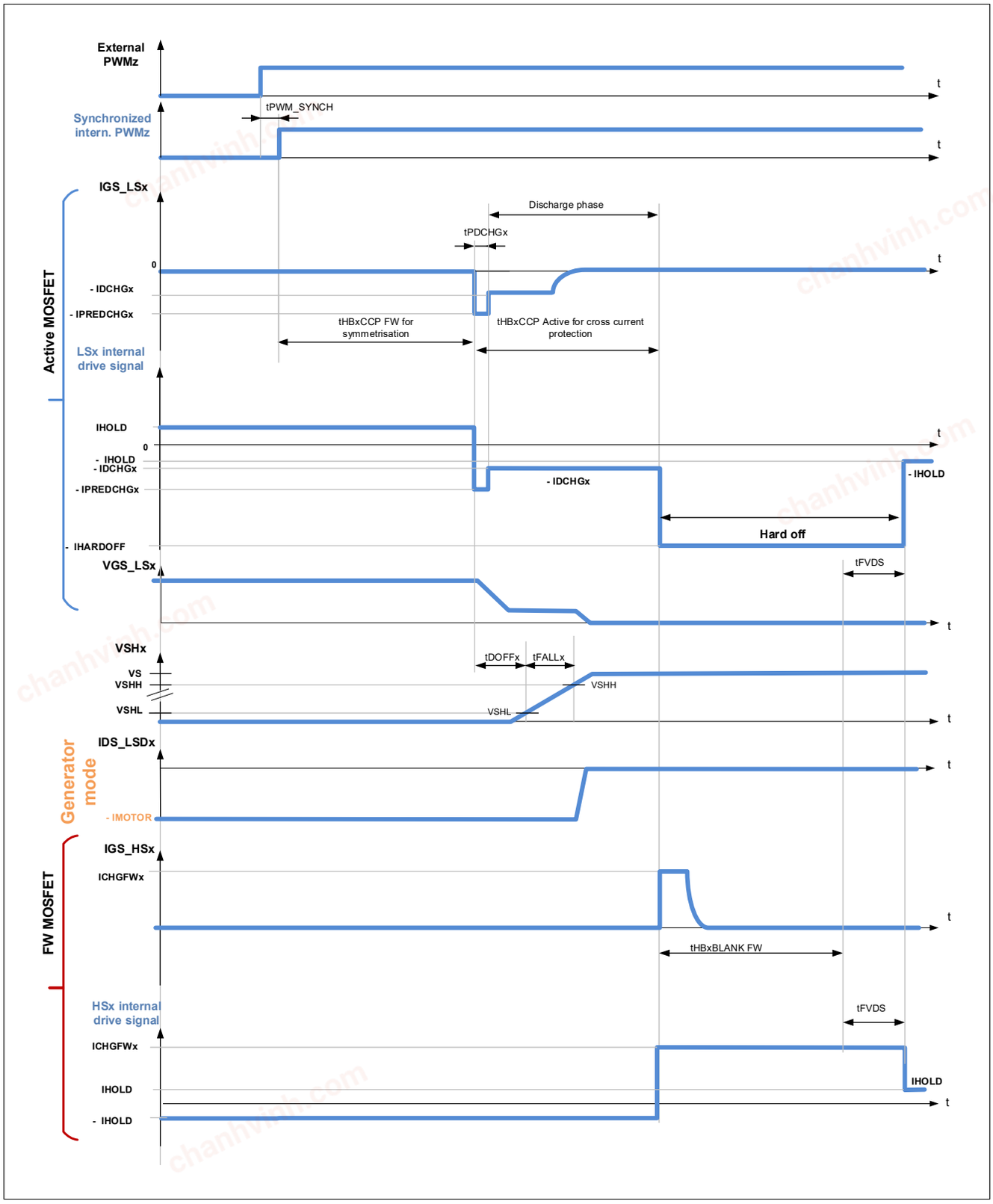



**Figure 64 Adaptive turn-on with high-side PWM, AGC[1:0] = (1,0) or (1,1), AFWx=1, motor operating as generator**

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### 12.3.4.4 Low-side PWM with adaptive gate control, motor operating as generator

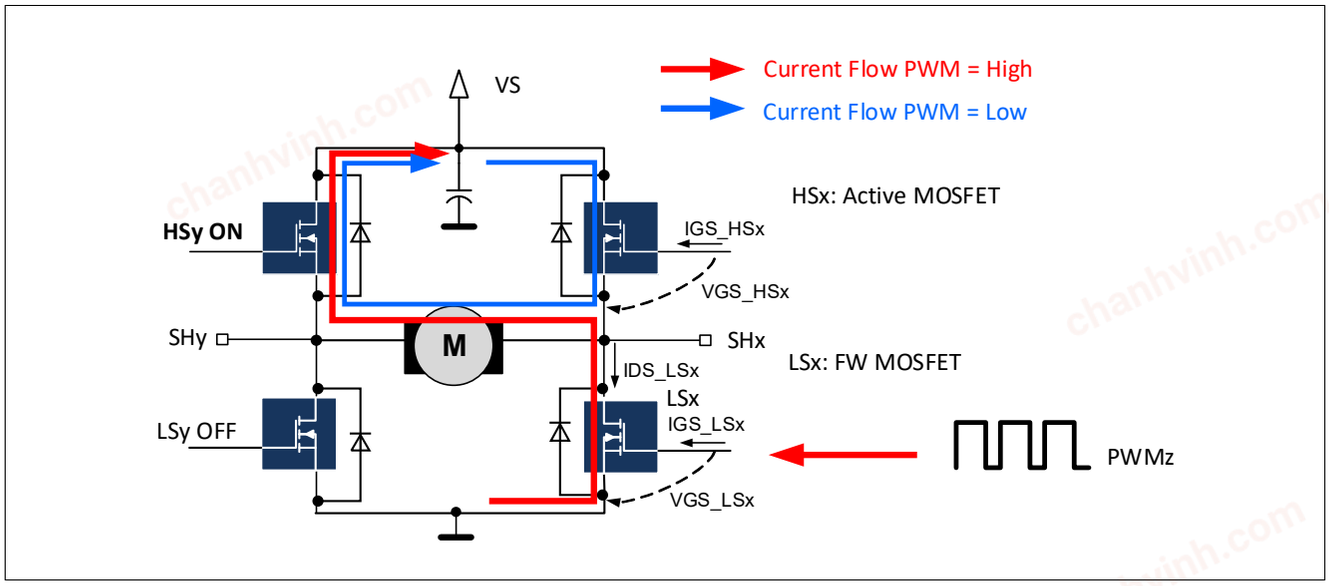



**Figure 65 PWM input z is mapped to low-side x, the motor operating as generator**

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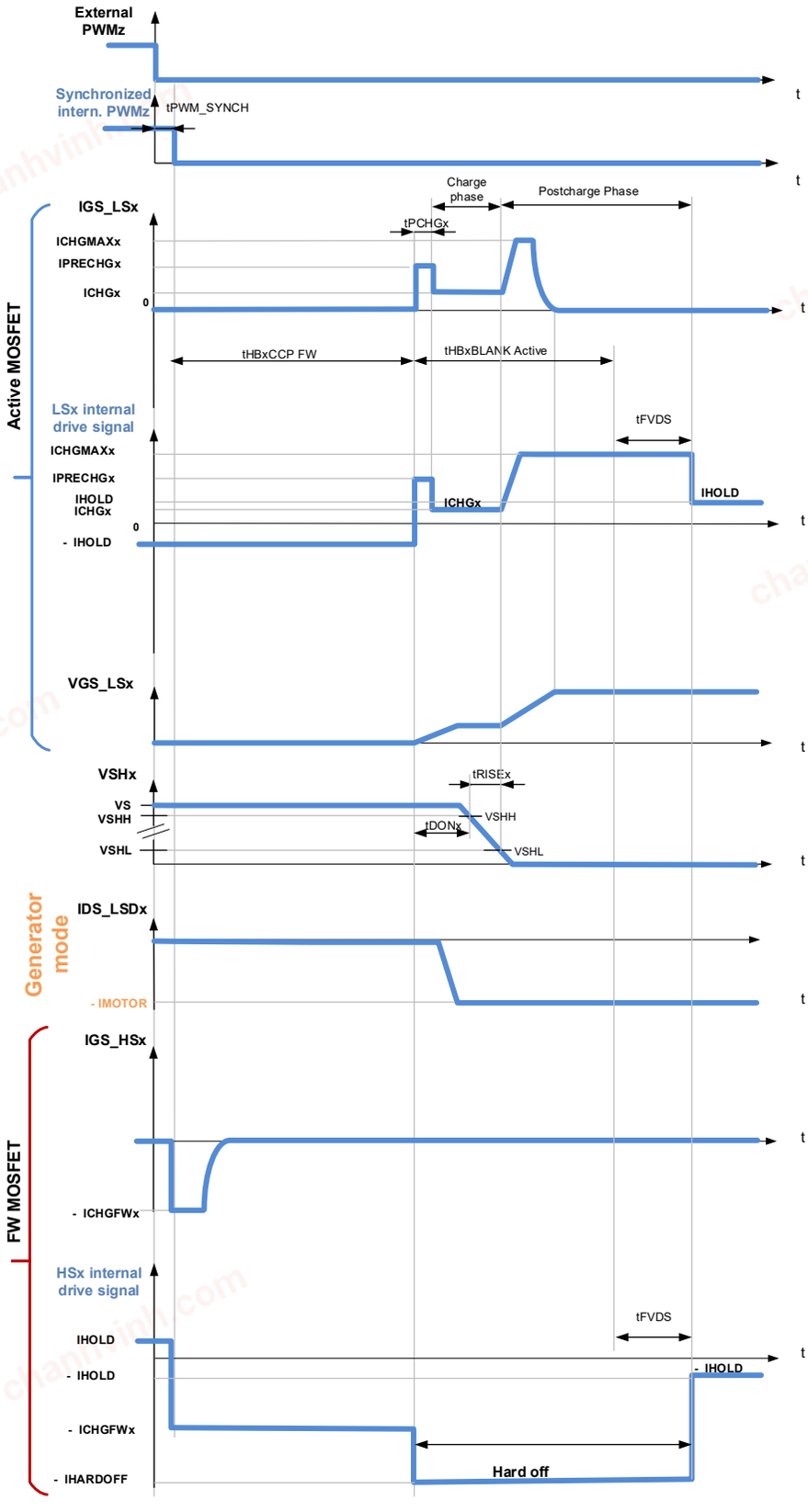



**Figure 66 Adaptive turn-off with high-side PWM, AGC[1:0] = (1,0) or (1,1), AFWx=1, motor operating as generator and EN_GEN_CHECK = 1**

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### 12.3.4.5 Status bits for regulation of turn-on and turn-off delay times

The control bits TDREGx (**TDREG**) indicate if tDONx and tDOFFx of the half-bridge x, using the adaptive control scheme (**AGC** = $10_B$ or $11_B$), are in regulation.

The half-bridge x is considered in regulation if one of the following conditions is met:

- Condition 1: The effective turn-on and turn-off delays are equal to the configured delays for at least eight cumulative PWM cycle (HBx tDON counter ≥ 8 and HBx tDOFF counter ≥ 8). For each PWM cycle
  - if tDONxEFF[1] = TDONx[2]: HBx tDON counter is incremented
  - if tDONxEFF[1] ≠ TDONx[2]: HBx tDON counter is decremented
  - if tDOFFxEFF[1] = TDOFFx[3]: HBx tDOFF counter is incremented
  - if tDOFFxEFF [1] ≠ TDOFFx[3]: HBx tDOFF counter is decremented
- Condition 2: The error between the effective delays ((tDONxEFF-TDONx) and(tDOFFxEFF-TDOFFx )) changes its sign three times consecutively

### 12.3.4.6 Time modulation of pre-charge and pre-discharge times

If **DEEP_ADAP** =0:

- one single precharge current is applied during tPCHGx to regulate TDON
- one single precharge current is applied during tPDCHGx to regulate TDOFF

If **DEEP_ADAP** = 1 (“deep adaptation” or “time modulation”) it is possible to:

- to divide the precharge phase in two parts, during which two different precharge currents can be applied
- to divide the predischarge phase in two parts, during which two different precharge currents can be applied

**Figure 67** describes the principle of the time modulation applied to the precharge phase. The same principle is also applied for the regulation of the pre-discharge phase.

1) Refer to **EFF_TDON_OFF1**, **EFF_TDON_OFF2**, **EFF_TDON_OFF3**, **EFF_TDON_OFF4**
2) Refer to **TDON_HB_CTRL**
3) Refer to **TDOFF_HB_CTRL**

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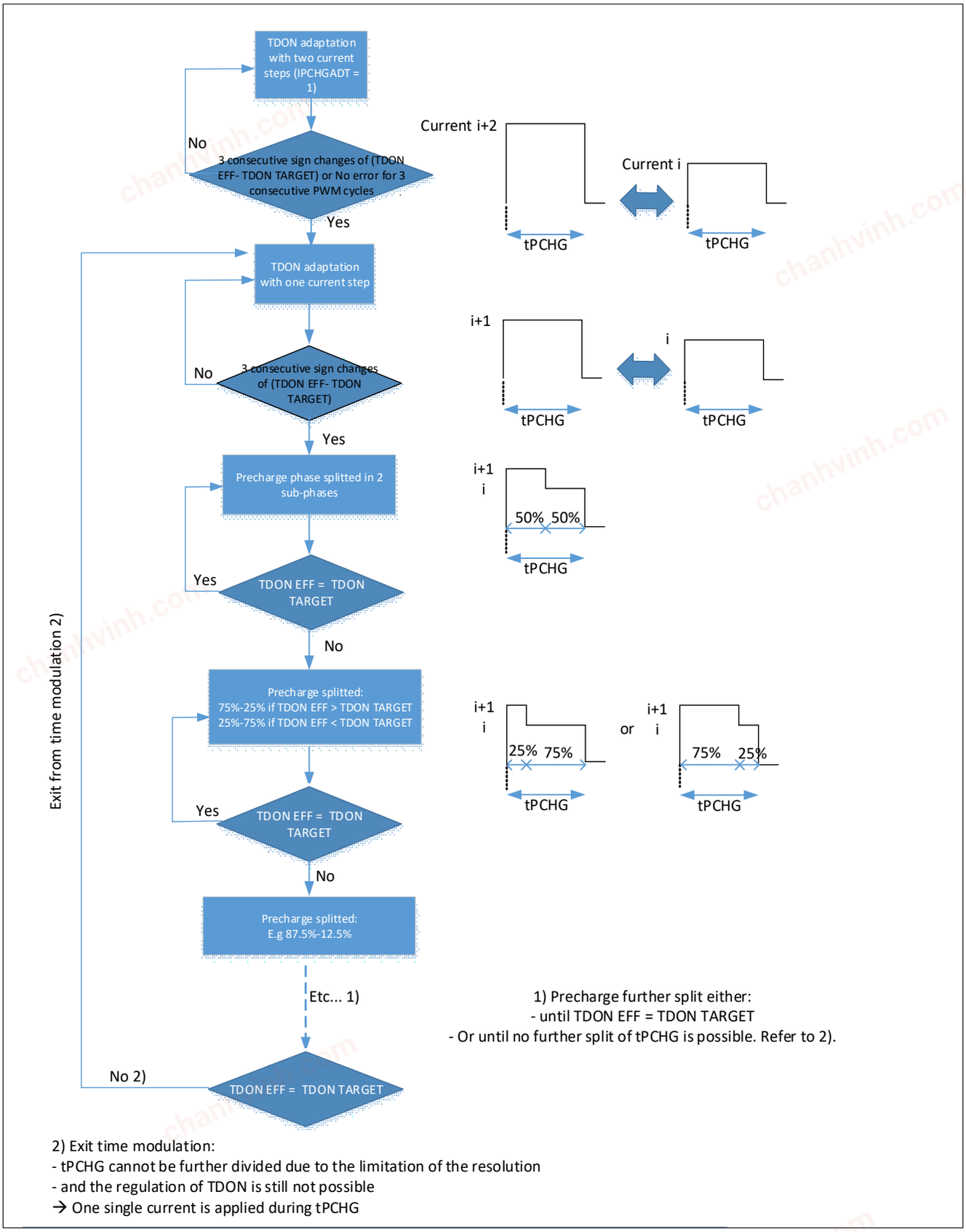



**Figure 67 Principle of the time modulation of the precharge phase, DEEP_ADAP = 1, AGC = $10_B$ or $11_B$**

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### 12.3.5 PWM operation without adaptive gate control

The adaptive gate control is disabled if AGC[1:0] is set to (0,0) or (0,1). The effective turn-on and turn -off delays of the PWM MOSFETs are not regulated. Two modes can be selected.

The target turn-on and turn-off delay times of PWM MOSFETs (configured in **TRISE_FALL1**, **TRISE_FALL2**, **TRISE_FALL3**, **TRISE_FALL4**) are no longer regulated. Nevertheless the status registers **EFF_TDON_OFF1**, **EFF_TDON_OFF2**, **EFF_TDON_OFF3**, **EFF_TDON_OFF4** still report the effective turn-on and turn-off times of the PWM MOSFET.

#### 12.3.5.1 AGC[1:0]=$00_B$

When AGC[1:0] = (0,0) (see **GENCTRL**), the control of the gate drivers in PWM mode differs from the description of **Chapter 12.3.4**, **PWM operation with adaptive gate control**, only by the suppression of the pre-charge and pre-discharge phases.

#### 12.3.5.2 AGC[1:0]=$01_B$

When **AGC** = (0,1) (see **GENCTRL**), then:

- During the pre-charge phase (tDCHGx) the gate of the PWM MOSFET mapped to the PWM input z is charged with the current IPCHGINITx (**HB_PCHG_INIT**).
- During the pre-discharge phase (tPDCHGx), the gate of the PWM MOSFET mapped to the PWM input z is discharged with the current -IPDCHGINITx (**HB_PCHG_INIT**).

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### 12.3.6 Gate driver current

Each gate driver is able to source and sink currents from 0.5 mA to 100 mA, with 64 steps according to **Figure 68** and **Figure 69**.

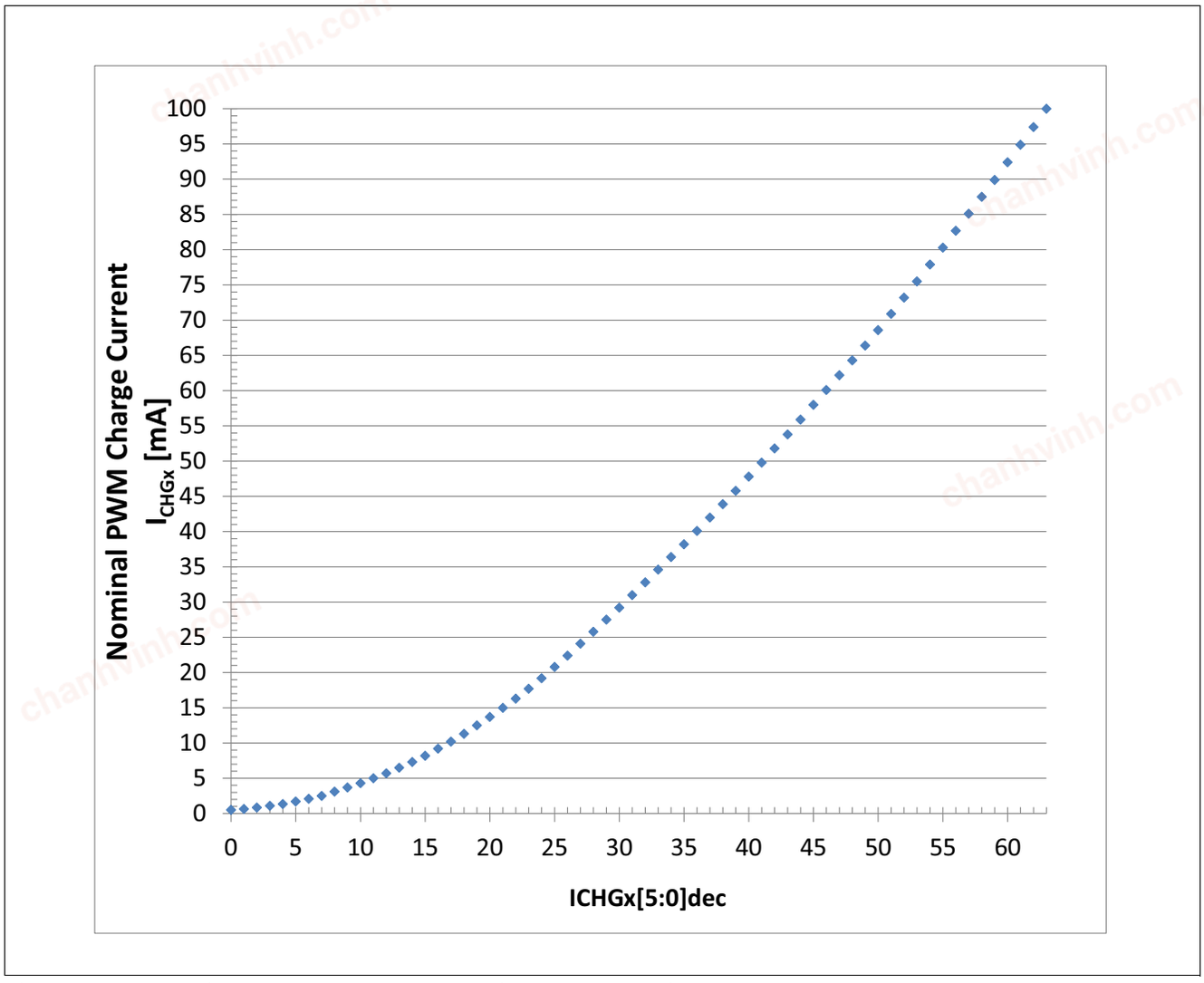



**Figure 68 Configurable charge currents in PWM operation**

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**Table 24 Charge currents in PWM operation, initial precharge current and freewheeling MOSFETs charge current**

| ICHGx[5:0], PCHGINIT[5:0] | Parameter name | Nom. charge current [mA] | Max. deviation to nominal values [%] |
|---|---|---|---|
| $000000_B$ | $I_{CHG0}$ | 0.5 | +/- 60% |
| $000001_B$ | $I_{CHG1}$ | 0.65 | +/- 60% |
| $000010_B$ | $I_{CHG2}$ | 0.85 | +/- 60% |
| $000011_B$ | $I_{CHG3}$ | 1.1 | +/- 60% |
| $000100_B$ | $I_{CHG4}$ | 1.35 | +/- 60% |
| $000101_B$ | $I_{CHG5}$ | 1.7 | +/- 60% |
| $000110_B$ | $I_{CHG6}$ | 2.1 | +/- 60% |
| $000111_B$ | $I_{CHG7}$ | 2.5 | +/- 60% |
| $001000_B$ | $I_{CHG8}$ | 3.1 | +/- 55% |
| $001001_B$ | $I_{CHG9}$ | 3.7 | +/- 55% |
| $001010_B$ | $I_{CHG10}$ | 4.3 | +/- 55% |
| $001011_B$ | $I_{CHG11}$ | 5.0 | +/- 55% |
| $001100_B$ | $I_{CHG12}$ | 5.7 | +/- 55% |
| $001101_B$ | $I_{CHG13}$ | 6.5 | +/- 55% |
| $001110_B$ | $I_{CHG14}$ | 7.3 | +/- 40% |
| $001111_B$ | $I_{CHG15}$ | 8.2 | +/- 40% |
| $010000_B$ | $I_{CHG16}$ | 9.2 | +/- 40 % |
| $010001_B$ | $I_{CHG17}$ | 10.2 | +/- 40 % |
| $010010_B$ | $I_{CHG18}$ | 11.3 | +/- 40% |
| $010011_B$ | $I_{CHG19}$ | 12.5 | +/- 40% |
| $010100_B$ | $I_{CHG20}$ | 13.7 | +/- 40% |
| $010101_B$ | $I_{CHG21}$ | 15 | +/- 40% |
| $010110_B$ | $I_{CHG22}$ | 16.3 | +/- 40% |
| $010111_B$ | $I_{CHG23}$ | 17.7 | +/- 40% |
| $011000_B$ | $I_{CHG24}$ | 19.2 | +/- 40% |
| $011001_B$ | $I_{CHG25}$ | 20.8 | +/- 40% |
| $011010_B$ | $I_{CHG26}$ | 22.4 | +/- 40% |
| $011011_B$ | $I_{CHG27}$ | 24.1 | +/- 40% |
| $011100_B$ | $I_{CHG28}$ | 25.8 | +/- 40% |
| $011101_B$ | $I_{CHG29}$ | 27.5 | +/- 40% |
| $011110_B$ | $I_{CHG30}$ | 29.2 | +/- 30% |
| $011111_B$ | $I_{CHG31}$ | 31 | +/- 30% |
| $100000_B$ | $I_{CHG32}$ | 32.8 | +/- 30% |
| $100001_B$ | $I_{CHG33}$ | 34.6 | +/- 30% |
| $100010_B$ | $I_{CHG34}$ | 36.4 | +/- 30% |
| $100011_B$ | $I_{CHG35}$ | 38.2 | +/- 30% |

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**Table 24 Charge currents in PWM operation, initial precharge current and freewheeling MOSFETs charge current** (cont'd)

| ICHGx[5:0], PCHGINIT[5:0] | Parameter name | Nom. charge current [mA] | Max. deviation to nominal values [%] |
|---|---|---|---|
| $100100_B$ | $I_{CHG36}$ | 40.1 | +/- 30% |
| $100101_B$ | $I_{CHG37}$ | 42 | +/- 30% |
| $100110_B$ | $I_{CHG38}$ | 43.9 | +/- 30% |
| $100111_B$ | $I_{CHG39}$ | 45.8 | +/- 30% |
| $101000_B$ | $I_{CHG40}$ | 47.8 | +/- 30% |
| $101001_B$ | $I_{CHG41}$ | 49.8 | +/- 30% |
| $101010_B$ | $I_{CHG42}$ | 51.8 | +/- 30% |
| $101011_B$ | $I_{CHG43}$ | 53.8 | +/- 30% |
| $101100_B$ | $I_{CHG44}$ | 55.9 | +/- 30% |
| $101101_B$ | $I_{CHG45}$ | 58 | +/- 30% |
| $101110_B$ | $I_{CHG46}$ | 60.1 | +/- 30% |
| $101111_B$ | $I_{CHG47}$ | 62.2 | +/- 30% |
| $110000_B$ | $I_{CHG48}$ | 64.3 | +/- 30% |
| $110001_B$ | $I_{CHG49}$ | 66.4 | +/- 30% |
| $110010_B$ | $I_{CHG50}$ | 68.6 | +/- 30% |
| $110011_B$ | $I_{CHG51}$ | 70.9 | +/- 30% |
| $110100_B$ | $I_{CHG52}$ | 73.2 | +/- 30% |
| $110101_B$ | $I_{CHG53}$ | 75.5 | +/- 30% |
| $110110_B$ | $I_{CHG54}$ | 77.9 | +/- 30% |
| $110111_B$ | $I_{CHG55}$ | 80.3 | +/- 30% |
| $111000_B$ | $I_{CHG56}$ | 82.7 | +/- 30% |
| $111001_B$ | $I_{CHG57}$ | 85.1 | +/- 30% |
| $111010_B$ | $I_{CHG58}$ | 87.5 | +/- 30% |
| $111011_B$ | $I_{CHG59}$ | 89.9 | +/- 30% |
| $111100_B$ | $I_{CHG60}$ | 92.4 | +/- 30% |
| $111101_B$ | $I_{CHG61}$ | 94.9 | +/- 30% |
| $111110_B$ | $I_{CHG62}$ | 97.4 | +/- 30% |
| $111111_B$ | $I_{CHG63}$ | 100 | +/- 30% |

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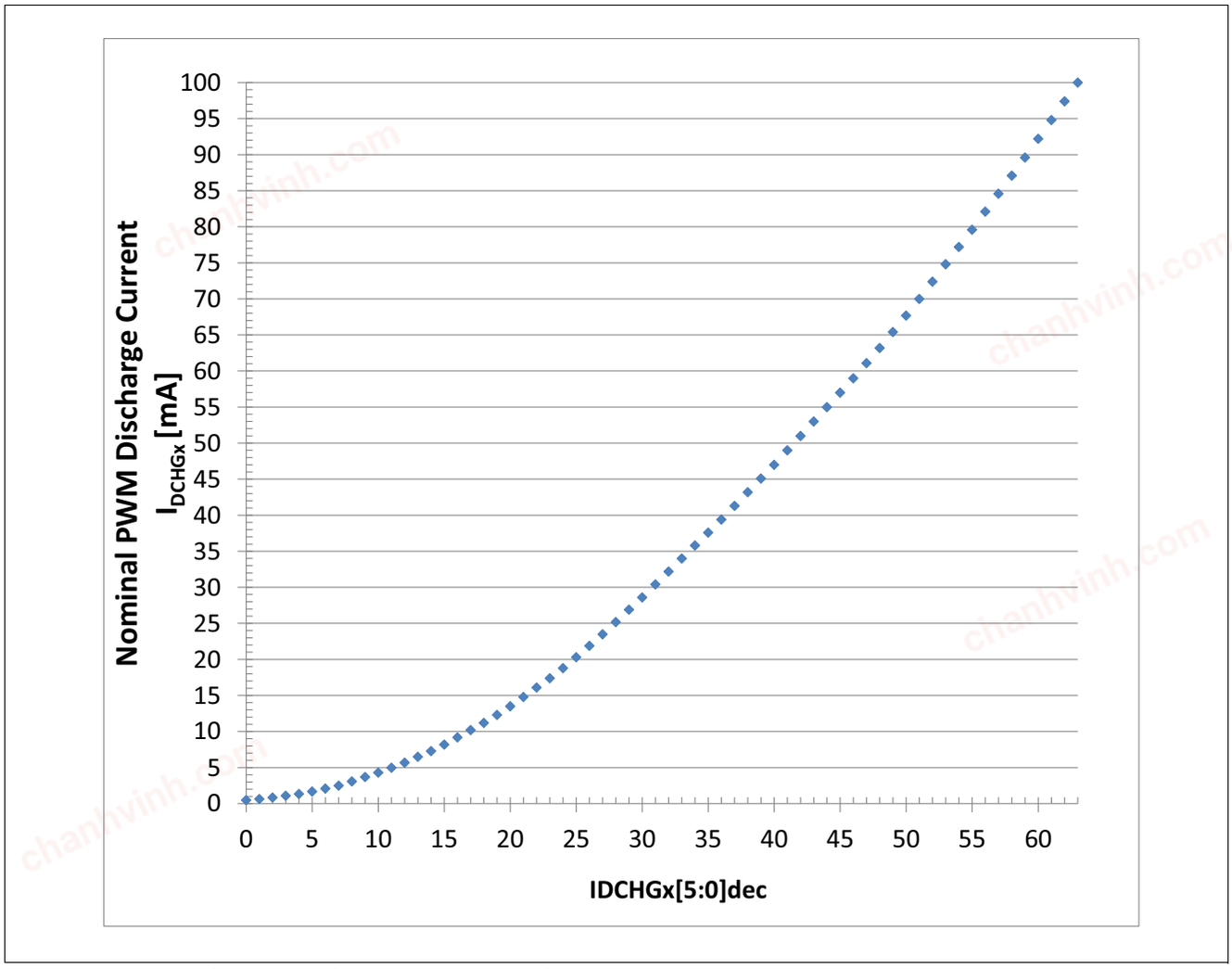



**Figure 69 Configurable discharge currents in PWM operation**

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**Table 25 Discharge currents in PWM operation, initial predischarge current and freewheeling MOSFETs discharge current**

| IDCHGx[5:0], PDCHGINIT[5:0] | Parameter name | Nom. discharge current [mA] | Max. deviation to nominal values [%] |
|---|---|---|---|
| $000000_B$ | $I_{DCHG0}$ | 0.5 | +/- 60% |
| $000001_B$ | $I_{DCHG1}$ | 0.65 | +/- 60% |
| $000010_B$ | $I_{DCHG2}$ | 0.85 | +/- 60% |
| $000011_B$ | $I_{DCHG3}$ | 1.1 | +/- 60% |
| $000100_B$ | $I_{DCHG4}$ | 1.35 | +/- 60% |
| $000101_B$ | $I_{DCHG5}$ | 1.7 | +/- 60% |
| $000110_B$ | $I_{DCHG6}$ | 2.1 | +/- 60% |
| $000111_B$ | $I_{DCHG7}$ | 2.5 | +/- 60% |
| $001000_B$ | $I_{DCHG8}$ | 3.1 | +/- 55% |
| $001001_B$ | $I_{DCHG9}$ | 3.7 | +/- 55% |
| $001010_B$ | $I_{DCHG10}$ | 4.3 | +/- 55% |
| $001011_B$ | $I_{DCHG11}$ | 5.0 | +/- 55% |
| $001100_B$ | $I_{DCHG12}$ | 5.7 | +/- 55% |
| $001101_B$ | $I_{DCHG13}$ | 6.5 | +/- 55% |
| $001110_B$ | $I_{DCHG14}$ | 7.3 | +/- 40% |
| $001111_B$ | $I_{DCHG15}$ | 8.2 | +/- 40% |
| $010000_B$ | $I_{DCHG16}$ | 9.2 | +/- 40% |
| $010001_B$ | $I_{DCHG17}$ | 10.2 | +/- 40% |
| $010010_B$ | $I_{DCHG18}$ | 11.2 | +/- 40% |
| $010011_B$ | $I_{DCHG19}$ | 12.3 | +/- 40% |
| $010100_B$ | $I_{DCHG20}$ | 13.5 | +/- 40% |
| $010101_B$ | $I_{DCHG21}$ | 14.8 | +/- 40% |
| $010110_B$ | $I_{DCHG22}$ | 16.1 | +/- 40% |
| $010111_B$ | $I_{DCHG23}$ | 17.4 | +/- 40% |
| $011000_B$ | $I_{DCHG24}$ | 18.8 | +/- 40% |
| $011001_B$ | $I_{DCHG25}$ | 20.3 | +/- 40% |
| $011010_B$ | $I_{DCHG26}$ | 21.9 | +/- 40% |
| $011011_B$ | $I_{DCHG27}$ | 23.5 | +/- 40% |
| $011100_B$ | $I_{DCHG28}$ | 25.2 | +/- 40% |
| $011101_B$ | $I_{DCHG29}$ | 26.9 | +/- 40% |
| $011110_B$ | $I_{DCHG30}$ | 28.6 | +/- 30% |
| $011111_B$ | $I_{DCHG31}$ | 30.4 | +/- 30% |
| $100000_B$ | $I_{DCHG32}$ | 32.2 | +/- 30% |
| $100001_B$ | $I_{DCHG33}$ | 34 | +/- 30% |
| $100010_B$ | $I_{DCHG34}$ | 35.8 | +/- 30% |
| $100011_B$ | $I_{DCHG35}$ | 37.6 | +/- 30% |

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**Table 25 Discharge currents in PWM operation, initial predischarge current and freewheeling MOSFETs discharge current** (cont'd)

| IDCHGx[5:0], PDCHGINIT[5:0] | Parameter name | Nom. discharge current [mA] | Max. deviation to nominal values [%] |
|---|---|---|---|
| $100100_B$ | $I_{DCHG36}$ | 39.4 | +/- 30 % |
| $100101_B$ | $I_{DCHG37}$ | 41.3 | +/- 30 % |
| $100110_B$ | $I_{DCHG38}$ | 43.2 | +/- 30 % |
| $100111_B$ | $I_{DCHG39}$ | 45.1 | +/- 30 % |
| $101000_B$ | $I_{DCHG40}$ | 47 | +/- 30 % |
| $101001_B$ | $I_{DCHG41}$ | 49 | +/- 30 % |
| $101010_B$ | $I_{DCHG42}$ | 51 | +/- 30 % |
| $101011_B$ | $I_{DCHG43}$ | 53 | +/- 30 % |
| $101100_B$ | $I_{DCHG44}$ | 55 | +/- 30 % |
| $101101_B$ | $I_{DCHG45}$ | 57 | +/- 30 % |
| $101110_B$ | $I_{DCHG46}$ | 59 | +/- 30 % |
| $101111_B$ | $I_{DCHG47}$ | 61.1 | +/- 30 % |
| $110000_B$ | $I_{DCHG48}$ | 63.2 | +/- 30 % |
| $110001_B$ | $I_{DCHG49}$ | 65.4 | +/- 30 % |
| $110010_B$ | $I_{DCHG50}$ | 67.7 | +/- 30 % |
| $110011_B$ | $I_{DCHG51}$ | 70 | +/- 30 % |
| $110100_B$ | $I_{DCHG52}$ | 72.4 | +/- 30 % |
| $110101_B$ | $I_{DCHG53}$ | 74.8 | +/- 30 % |
| $110110_B$ | $I_{DCHG54}$ | 77.2 | +/- 30 % |
| $110111_B$ | $I_{DCHG55}$ | 79.6 | +/- 30 % |
| $111000_B$ | $I_{DCHG56}$ | 82.1 | +/- 30 % |
| $111001_B$ | $I_{DCHG57}$ | 84.6 | +/- 30 % |
| $111010_B$ | $I_{DCHG58}$ | 87.1 | +/- 30 % |
| $111011_B$ | $I_{DCHG59}$ | 89.6 | +/- 30 % |
| $111100_B$ | $I_{DCHG60}$ | 92.2 | +/- 30 % |
| $111101_B$ | $I_{DCHG61}$ | 94.8 | +/- 30 % |
| $111110_B$ | $I_{DCHG62}$ | 97.4 | +/- 30 % |
| $111111_B$ | $I_{DCHG63}$ | 100 | +/- 30 % |

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### 12.3.7 PWM operation at high and low duty cycles with active freewheeling

This section describes the internal PWM signal of the active and FW MOSFET when the motor operates as load or generator with active freewheeling (AFWx = 1). In particular, at low and high duty cycles, the active freewheeling is disabled.

**Notes**

1. *It is recommended to clear **EN_GEN_CHECK** (**EN_GEN_CHECK** to 0)at very high and very low duty cycles: $t_{ON} < t_{HBxCCP}$ FW or $t_{OFF} < t_{HBxCCP}$ active. Under these conditions, a generator mode cannot be correctly detected. The control scheme of the active MOSFET and of the freewheeling MOSFET can therefore be inverted.*
2. *The device cannot measure the switching times $t_{DON}$, $t_{DOFF}$, $t_{RISE}$ and $t_{FALL}$ at very high and very low duty cycles: $t_{ON} < t_{HBxCCP}$ FW or $t_{OFF} < t_{HBxCCP}$ active.*

**General case, motor operating as load, tON > tHBxCCP FW and tOFF > tHBxCCP FW + tHBxCCP active**

**Figure 70** shows the internal control signals of the PWM MOSFETs and the freewheeling MOSFET while the motor operates as load:

- tON is longer than the FW cross-current protection time (tHBxCCP FW).
- tOFF is longer than the active cross-current protection time (tHBxCCP FW + tHBxCCP Active).

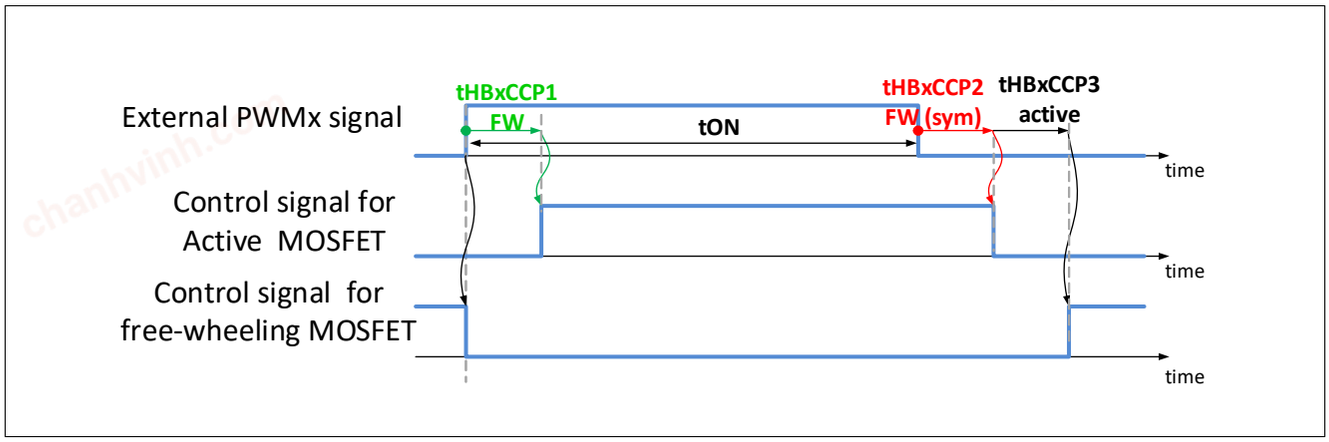



**Figure 70 Internal signals for PWM operation - General case tON > tHBxCCP FW, tOFF > tHBxCCP FW + tHBxCCP active, motor operating as load**

**General case, motor operating as generator, tOFF > tHBxCCP FW and tON > tHBxCCP FW + tHBxCCP active**

**Figure 71** shows the internal control signals of the PWM MOSFETs and the freewheeling MOSFET while the motor operates as generator:

- tOFF is longer than the FW cross-current protection time (tHBxCCP FW).
- tON is longer than the active cross-current protection time (tHBxCCP FW + tHBxCCP Active).

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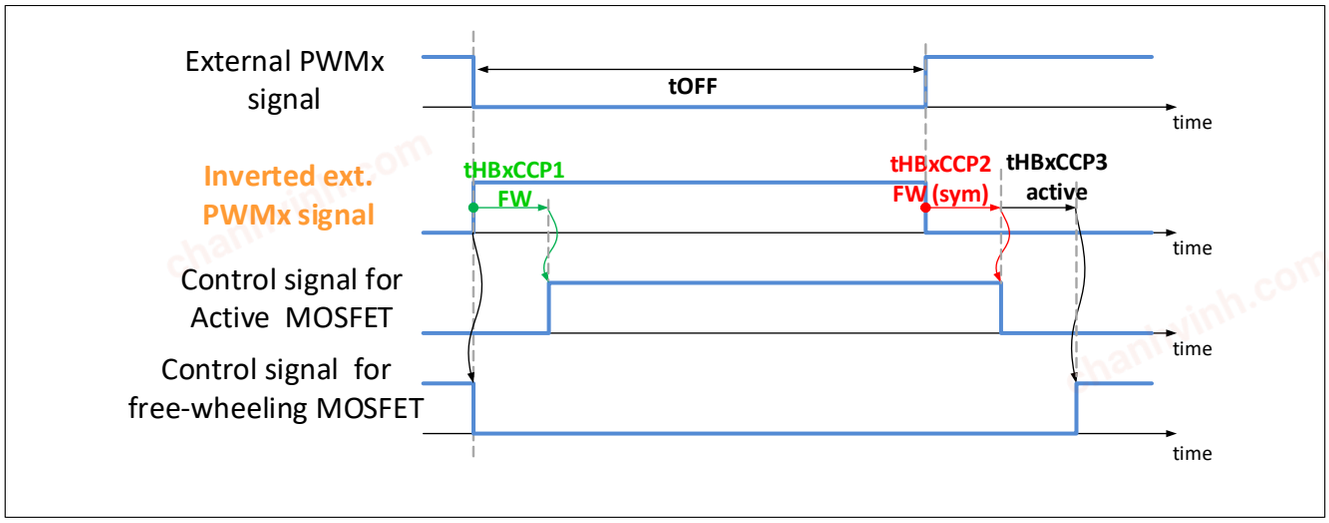



**Figure 71 Internal signals for PWM operation - General case: tOFF > tHBxCCP FW, tON > tHBxCCP FW + tHBxCCP FW, Motor operating as generator**

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### High duty cycle: tOFF < tHBxCCP active

No distinction between active MOSFET and FW MOSFET is possible, when the OFF-time of the external PWM signal is shorter than the configured active cross-current protection time. Therefore the PWM MOSFET (selected by HBxMODE[1:0]) is controlled as the active MOSFET. In other words, it is assumed that the motor operates as load. The control signal of the PWM MOSFET is shifted by one FW cross-current protection time compared to the external PWM signal. The MOSFET opposite to the PWM MOSFET stays OFF (passive FW).

Refer to **Figure 72**.

*Note: No active FW is applied if tOFF < tHBxCCP FW + tHBxCCP active*

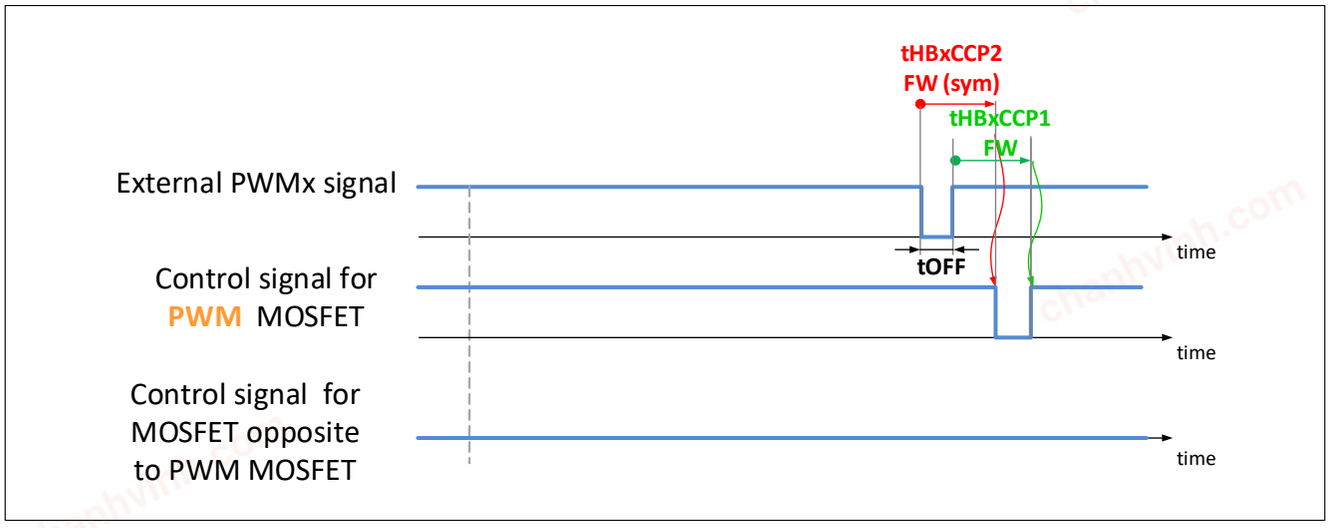



**Figure 72 Internal signals for PWM operation at high duty cycle, tOFF < tHBxCCP Active + tHBxCCP FW**

### Low duty cycle: tON < tHBxCCP FW

No distinction between active MOSFET and FW MOSFET is possible, when the ON-time of the external PWM signal is shorter than the configured FW cross-current protection time. Therefore the PWM MOSFET (selected by HBxMODE[1:0]) is controlled as the active MOSFET. In other words, it is assumed that the motor operates as load. The control signal of the PWM MOSFET is shifted by one cross-current protection time compared to the external PWM signal.

Refer to **Figure 73**.

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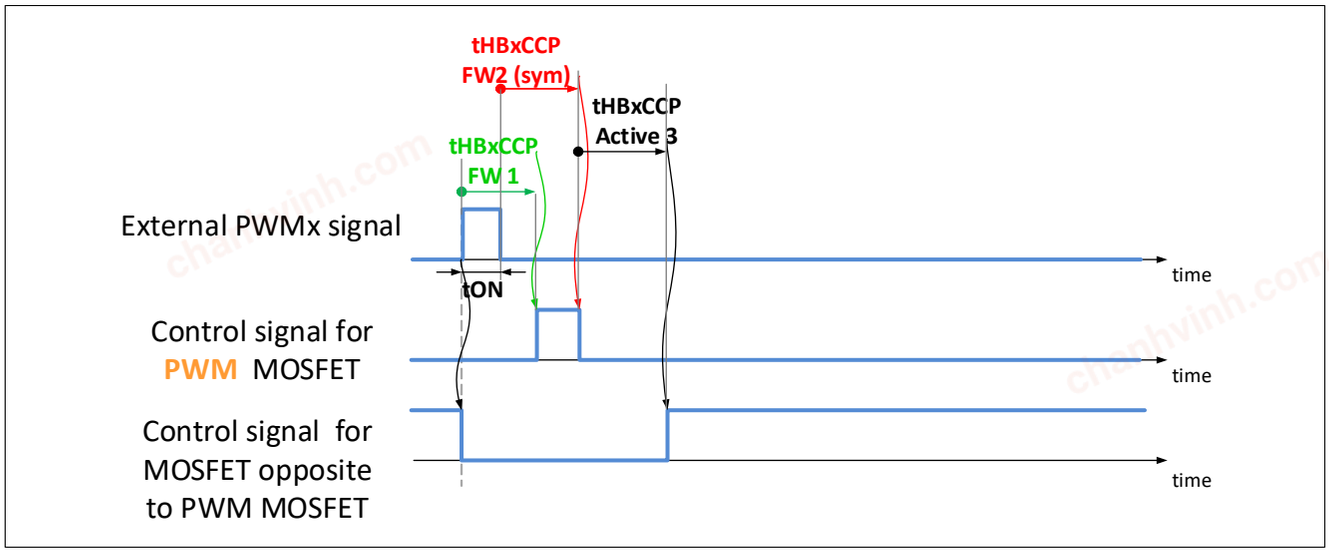



**Figure 73 Internal signals for PWM operation at low duty cycle, tON < tHBxCCP FW**

### 12.3.8 Measurements of the switching times

The effective switching times in PWM operation:

- of the PWM MOSFET if **EN_GEN_CHECK** = 0
- of the active MOSFET if **EN_GEN_CHECK** = 1

are reported in the registers:

**EFF_TDON_OFF1**,**EFF_TDON_OFF2**,**EFF_TDON_OFF3**, **EFF_TDON_OFF4**.

If the end of the rise time for a given MOSFET is not detected before $t_{HBxBLANK}$ Active elapses, then the corresponding status register reports an effective rise time equal to zero.

If the end of the fall time for a given MOSFET is not detected before $t_{HBxCCP}$ Active active elapses, then the corresponding status register reports an effective fall time equal to zero.

The device cannot measure the switching times $t_{DON}$, $t_{DOFF}$, $t_{RISE}$ and $t_{FALL}$ at very high and very low duty cycles: $t_{ON} < t_{HBxCCP}$ FW and $t_{OFF} < t_{HBxCCP}$ active. In this case, the corresponding registers report effective $t_{DON}$, $t_{DOFF}$, $t_{RISE}$ and $t_{FALL}$ equal to zero.

## 12.4 Passive discharge

Resistors ($R_{GGND}$) between the gate of GHx and GND, and between GLx and GND, ensure that the external MOSFETs are turned off in the following conditions:

- $V_{CC1}$ undervoltage
- HBxMODE = $00_B$ in Normal Mode
- **CPEN** = 0 in Normal Mode
- VS overvoltage or VSINT overvoltage
- Charge pump undervoltage and charge pump blank time (**$t_{CPUVBLANK}$**)
- Charge pump overtemperature (**CP_OT**)
- VDS overvoltage after active discharge in Normal Mode

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- In Init Mode, Stop Mode, Fail Safe Mode, Restart Mode and Sleep Mode (exceptions for low-sides in parking braking and VS / VSINT overvoltage braking , refer to **Chapter 12.6** and **Chapter 13.11.3**)

## 12.5 Slam mode

The slam mode is applicable in Normal Mode.

If the SLAM bit is set in **BRAKE** register:

1. If HBxMODE = 01b or 10b , then the corresponding MOSFETs are actively turned off with their static discharge current during their respective tHBxCCP Active.
2. Then charge pump is deactivated independently from **CPEN**
3. Then PWM1/CRC input pin is mapped to LS1, LS2, LS3 and LS4, independently from PMW12MAP, PWM34MAP, HBxMODE and HBx_PWM_EN
   a) If PWM1/CRC is High, then the low-side MOSFETs are turned on within $t_{ON_BRAKE}$.
   b) If PWM1/CRC is Low, then the low-side MOSFETs are turned off within $t_{OFF_BRAKE}$.

There is also the possibility to disable selectively the LSx in SLAM mode.

## 12.6 Parking braking mode

If **PARK_BRK_EN** bit is set, while the device goes in Sleep Mode or in Stop Mode:

1. If HBxMODE = 01b or 10b , then the corresponding MOSFETs are actively turned off with their static discharge current during their respective tHBxCCP Active.
2. Then charge pump is deactivated independently from CPEN bit.
3. Then the passive discharge ($R_{GGND}$) of the low-sides is deactivated, the passive discharge of the high-sides are activated
4. If PWM1/CRC is High, then the low-side MOSFETs are turned on within $t_{ON_BRAKE}$.

Refer to **Chapter 13.11.2** for the protection of the of low-side MOSFETs against short circuits when the parking braking mode is activated.

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## 12.7 Charge pump

A dual-stage charge pump supplies the gate drivers for the high-side and low-side MOSFETs. It requires three external capacitors connected between CPC1N and CPC1P, CPC2N and CPC2P, VS and CP.

The buffer capacitor between VS and CP must have a capacitance equal or higher than 470 nF.

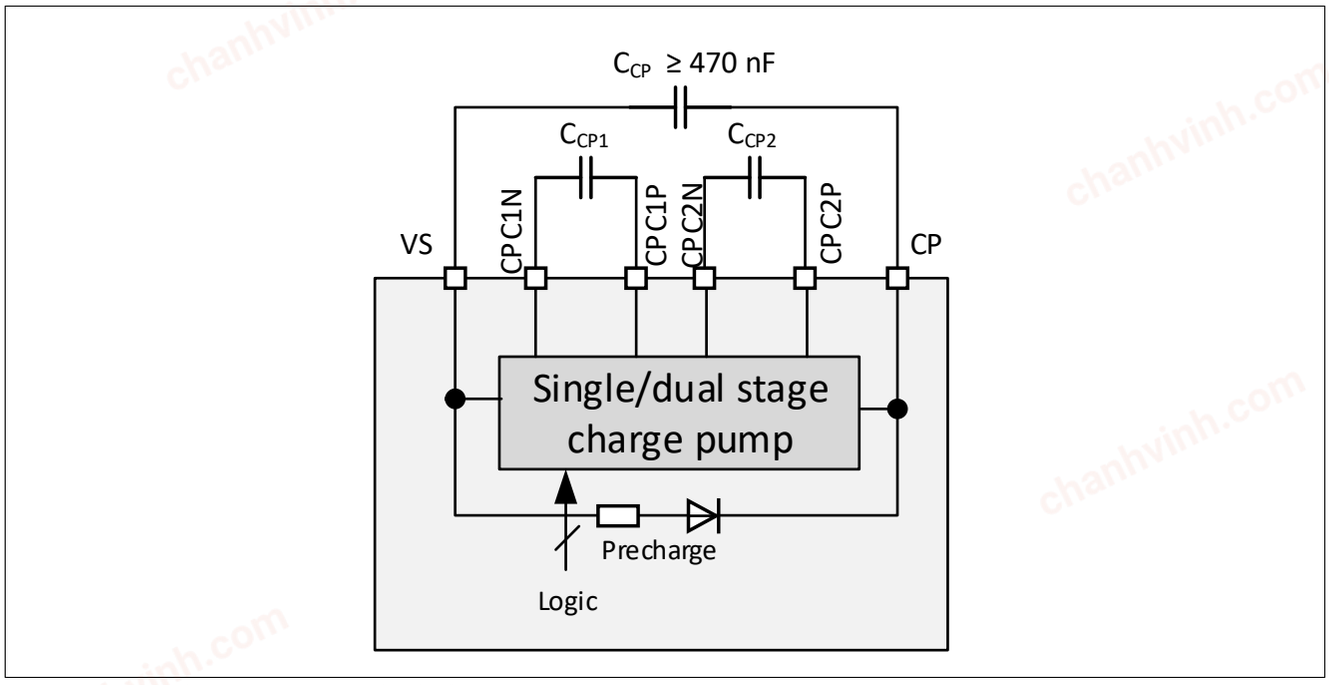



**Figure 74 Charge pump - Block diagram**

### Logic or normal level MOSFETs

The regulation of the charge pump outputs voltage can be configured depending on the type of MOSFET.

**FET_LVL** = 0: Logic level MOSFETs are selected:

- VCP - VS = $V_{CP3}$ (11 V typ. at VS > 8 V).
- The high-side gate-source voltage GHx - SHx is $V_{GH4}$ ($V_S$ > 8 V).
- The low-side gate-source voltage GLx - SL is $V_{GH3}$ ($V_S$ > 8 V).

**FET_LVL** = 1: Normal level MOSFETs are selected:

- VCP - VS = $V_{CP1}$(15 V typ. at VS > 8 V).
- The high-side and low-side gate-source voltage GHx - SHx or GLx - SL is $V_{GH1}$ ($V_S$ > 8 V).

CPSTGA = 0 (default, see **GENCTRL**), the device operates with the dual-stage charge pump.

If CPSTGA = 1, the device switches to single-stage or dual-stage charge pump automatically:

- If $V_S > V_{CPSO\ DS}$: the TLE9562QX switches from a dual-stage to a single-stage charge pump.
- If $V_S < V_{CPSO\ SD}$: the TLE9562QX switches from single-stage to dual-stage charge pump.

The operation with the single-stage charge pump reduces the current consumption from the VS pin.

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## 12.8 Frequency modulation

A modulation of the charge pump frequency can be activated to reduce the peak emission.

The modulation frequency is set by the control bit FMODE in **GENCTRL**:

- FMODE = 0: No modulation.
- FMODE = 1: Modulation frequency = 15.6 kHz (default).

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## 12.9 Electrical characteristics gate driver

The electrical characteristics related to the gate driver are valid for $V_{CP} > V_S + 8.5$ V

**Table 26 Electrical characteristics: gate drivers**

$V_{SINT}$ = 5.5 V to 28 V, $T_j$ = -40°C to +150°C,
$V_{CP} > V_S + 8.5$ V, $V_S$ = 6 to 19V, all voltages with respect to ground, positive current flowing into pin except for $I_{GLx}$ and $I_{GHx}$ (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Comparators** | | | | | | | |
| SHx High Threshold | $V_{SHH}$ | $V_S$ - 2.6 | – | $V_S$ - 1.9 | V | | P_12.11.1 |
| SHx Low Threshold | $V_{SHL}$ | 1.9 | – | 2.6 | V | Referred to GND | P_12.11.2 |
| SHx comparator delay | $t_{SHx}$ | – | 12 | 30 | ns | 1) | P_12.11.3 |
| **MOSFET Driver Output** | | | | | | | |
| High Level Output Voltage GHx vs. SHx and GLx vs. SL | $V_{GH1}$ | 10 | 11.5 | 12.5 | V | 2) $V_S \geq 8$ V, $C_{Load}$ = 10 nF, $I_{CP}$ = -12 mA, FET_LVL = 1 | P_12.11.4 |
| High Level Output Voltage GHx vs. SHx and GLx vs. SL | $V_{GH2}$ | 7 | – | 12.5 | V | $V_S$ = 6 V, $C_{Load}$ = 10 nF, $I_{CP}$ = -6 mA, FET_LVL = 1 | P_12.11.5 |
| High Level Output Voltage GLx vs. SL | $V_{GH3}$ | 10 | – | 12.5 | V | 3) $V_S \geq 6$ V, $C_{Load}$ = 10 nF, FET_LVL = 0 | P_12.11.6 |
| High Level Output Voltage GHx vs. SHx | $V_{GH4}$ | 8.5 | 10 | 12.5 | V | 2) $V_S \geq 8$ V, $C_{Load}$ = 10 nF, $I_{CP}$ = -12 mA, FET_LVL = 0 | P_12.11.7 |
| High Level Output Voltage GHx vs. SHx | $V_{GH5}$ | 7 | – | 12.5 | V | $V_S$ = 6 V, $C_{LOAD}$= 10 nF, $I_{CP}$ = -6 mA, FET_LVL =0 | P_12.11.8 |
| Charge current | $I_{CHG0}$ | -60% | 0.5 | +60% | mA | ICHG = $0_D$ 1) $C_{Load}$ = 2.2 nF $V_S \geq 8$V, $V_{GS} \leq V_{GS(ON)}$ 4) | P_12.11.10 |
| Charge current | $I_{CHG8}$ | -55% | 3.1 | +55% | mA | ICHG = $8_D$ 1) $C_{Load}$ = 2.2 nF $V_S \geq 8$V, $V_{GS} \leq V_{GS(ON)}$ 4) | P_12.11.11 |
| Charge current | $I_{CHG16}$ | -40% | 9.2 | +40% | mA | ICHG = $16_D$ 1) $C_{Load}$ = 2.2 nF $V_S \geq 8$V, $V_{GS} \leq V_{GS(ON)}$ 4) | P_12.11.12 |
| Charge current | $I_{CHG32}$ | -30% | 32.8 | +30% | mA | ICHG = $32_D$ 1) $C_{Load}$ = 10 nF $V_S \geq 8$V, $V_{GS} \leq V_{GS(ON)}$ 4) | P_12.11.13 |

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**Table 26 Electrical characteristics: gate drivers** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V, $T_j$ = -40°C to +150°C,
$V_{CP} > V_S + 8.5$ V, $V_S$ = 6 to 19V, all voltages with respect to ground, positive current flowing into pin except for $I_{GLx}$ and $I_{GHx}$ (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Charge current | $I_{CHG48}$ | -30% | 64.3 | +30% | mA | ICHG = $48_D$ [1]<br>$C_{Load}$ = 10 nF<br>$V_S \geq 8V$, $V_{GS} \leq V_{GS(ON)}$ [4] | P_12.11.14 |
| Charge current | $I_{CHG63}$ | -30% | 100 | +30% | mA | ICHG = $63_D$ [1]<br>$C_{Load}$ = 10 nF<br>$V_S \geq 8V$, $V_{GS} \leq V_{GS(ON)}$ [4] | P_12.11.15 |
| Discharge current | $I_{DCH0}$ | -60 % | -0.5 | +60% | mA | IDCHG = $0_D$ [1]<br>$C_{Load}$ = 2.2 nF<br>$V_S \geq 8V$, $V_{GS} \geq V_{GS(OFF1)}$ | P_12.11.16 |
| Discharge current | $I_{DCH8}$ | -55 % | -3.1 | +55% | mA | IDCHG = $8_D$ [1]<br>$C_{Load}$ = 2.2 nF<br>$V_S \geq 8V$, $V_{GS} \geq V_{GS(OFF1)}$ | P_12.11.17 |
| Discharge current | $I_{DCHG16}$ | -40% | -9.2 | +40% | mA | IDCHG = $16_D$ [1]<br>$C_{Load}$ = 2.2 nF<br>$V_S \geq 8V$, $V_{GS} \geq V_{GS(OFF1)}$ | P_12.11.18 |
| Discharge current | $I_{DCHG32}$ | -30% | -32.2 | +30% | mA | IDCHG = $32_D$ [1]<br>$C_{Load}$ = 10 nF<br>$V_S \geq 8V$, $V_{GS} \geq V_{GS(OFF2)}$ | P_12.11.19 |
| Discharge current | $I_{DCHG48}$ | -30% | -63.2 | +30% | mA | IDCHG = $48_D$ [1]<br>$C_{Load}$ = 10 nF<br>$V_S \geq 8V$, $V_{GS} \geq V_{GS(OFF2)}$ | P_12.11.20 |
| Discharge current | $I_{DCHG63}$ | -30% | -100 | +30% | mA | IDCHG = $63_D$ [1]<br>$C_{Load}$ = 10 nF<br>$V_S \geq 8V$, $V_{GS} \geq V_{GS(OFF2)}$ | P_12.11.21 |
| Charge current temperature drift | $I_{CHG0,TDrift}$ | -37% | -12% | 15% | | ICHG = $0_D$ [1)5)] | P_12.11.107 |
| Charge current temperature drift | $I_{CHG8,TDrift}$ | -17% | 1% | 20% | | ICHG = $8_D$ [1)5)] | P_12.11.108 |
| Charge current temperature drift | $I_{CHG16,TDrift}$ | -12% | 3% | 18% | | ICHG = $16_D$ [1)5)] | P_12.11.109 |
| Charge current temperature drift | $I_{CHG32,TDrift}$ | -11% | -1% | 9% | | ICHG = $32_D$ [1)5)] | P_12.11.110 |
| Charge current temperature drift | $I_{CHG48,TDrift}$ | -7.5% | 0.5% | 8% | | ICHG = $48_D$ [1)5)] | P_12.11.111 |
| Charge current temperature drift | $I_{CHG63,TDrift}$ | -5.5% | 1.5% | 8.5% | | ICHG = $63_D$ [1)5)] | P_12.11.112 |
| Discharge current temperature drift | $I_{DCHG0,TDrift}$ | -29% | -4.5% | 20% | | IDCHG = $0_D$ [1)6)] | P_12.11.113 |

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**Table 26 Electrical characteristics: gate drivers** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V, $T_j$ = -40°C to +150°C,
$V_{CP} > V_S + 8.5$ V, $V_S$ = 6 to 19V, all voltages with respect to ground, positive current flowing into pin except for $I_{GLx}$ and $I_{GHx}$ (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Discharge current temperature drift | $I_{DCHG8,TDrift}$ | -8% | 8.5% | 26% | | IDCHG = $8_D$ 1)6) | P_12.11.114 |
| Discharge current temperature drift | $I_{DCHG16,TDrift}$ | -4% | 9.5% | 23% | | IDCHG = $16_D$ 1)6) | P_12.11.115 |
| Discharge current temperature drift | $I_{DCHG32,TDrift}$ | -4% | 4.5% | 13% | | IDCHG = $32_D$ 1)6) | P_12.11.116 |
| Discharge current temperature drift | $I_{DCHG48,TDrift}$ | -4% | 3.5% | 10% | | IDCHG = $48_D$ 1)6) | P_12.11.117 |
| Discharge current temperature drift | $I_{DCHG63,TDrift}$ | -3.5% | 3.5% | 9.5% | | IDCHG = $63_D$ 1)6) | P_12.11.118 |
| Charge current $V_S$ drift | $I_{CHG0,VsDrift}$ | 3% | 4.5% | 6% | | ICHG = $0_D$ 1)7) | P_12.11.143 |
| Charge current $V_S$ drift | $I_{CHG8,VsDrift}$ | 4.5% | 6% | 7.5% | | ICHG = $8_D$ 1)7) | P_12.11.144 |
| Charge current $V_S$ drift | $I_{CHG16,VsDrift}$ | 4% | 5.8% | 7.5% | | ICHG = $16_D$ 1)7) | P_12.11.145 |
| Charge current $V_S$ drift | $I_{CHG32,VsDrift}$ | 2% | 3.8 | 5.8% | | ICHG = $32_D$ 1)7) | P_12.11.146 |
| Charge current $V_S$ drift | $I_{CHG48,VsDrift}$ | -0.5% | 2% | 4.5% | | ICHG = $48_D$ 1)7) | P_12.11.147 |
| Charge current $V_S$ drift | $I_{CHG63,VsDrift}$ | -2.3% | 0.3 | 2.8% | | ICHG = $63_D$ 1)7) | P_12.11.148 |
| Discharge current $V_S$ drift | $I_{DCHG0,VsDrift}$ | -3% | -1.5% | 0% | | IDCHG = $0_D$ 1)8) | P_12.11.149 |
| Discharge current $V_S$ drift | $I_{DCHG8,VsDrift}$ | -3% | -0.5% | 2% | | IDCHG = $8_D$ 1)8) | P_12.11.150 |
| Discharge current $V_S$ drift | $I_{DCHG16,VsDrift}$ | -3.3% | -0.3% | 2.3% | | IDCHG = $16_D$ 1)8) | P_12.11.151 |
| Discharge current $V_S$ drift | $I_{DCHG32,VsDrift}$ | -2% | 0% | 2% | | IDCHG = $32_D$ 1)8) | P_12.11.152 |
| Discharge current $V_S$ drift | $I_{DCHG48,VsDrift}$ | -1.5% | 0% | 1.5% | | IDCHG = $48_D$ 1)8) | P_12.11.153 |
| Discharge current $V_S$ drift | $I_{DCHG63,VsDrift}$ | -1.5% | 0.2% | 1.5% | | IDCHG = $63_D$ 1)8) | P_12.11.154 |
| Passive discharge resistance between GHx/GLx and GND | $R_{GGND}$ | 10 | 20 | 30 | kΩ | 1) | P_12.11.22 |
| Resistor between SHx and GND | $R_{SHGND}$ | 10 | 20 | 30 | kΩ | 1)9) | P_12.11.23 |
| Low RDSON mode | $R_{ONCCP}$ | – | 22 | 35 | Ω | 1) $V_S$ = 13.5 V<br>$V_{CP} = V_S$ + 14 V<br>$I_{CHG} = I_{DCHG} = 63_D$ | P_12.11.24 |
| **Gate Drivers Dynamic Parameters** | | | | | | | |
| Gate Driver turn-on delay Time | $t_{DGDRV_ON1}$ | – | – | 400 | ns | 10) From PWM11) rising edge to 20% of $I_{CHGx}$ ,<br>x = 0 to 63,<br>$C_{Load}$ = 10 nF,<br>**BDFREQ** = 0 | P_12.11.25 |

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**Table 26 Electrical characteristics: gate drivers** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V, $T_j$ = -40°C to +150°C,
$V_{CP} > V_S + 8.5$ V, $V_S$ = 6 to 19V, all voltages with respect to ground, positive current flowing into pin except for $I_{GLx}$ and $I_{GHx}$ (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Gate Driver turn-on delay Time | $t_{DGDRV_ON2}$ | – | – | 300 | ns | [10] From PWM[11] rising edge to 20% of $I_{CHGx}$, x = 0 to 63, $C_{Load}$ = 10 nF, **BDFREQ** = 1 | P_12.11.93 |
| Gate Driver current turn-on rise time | $t_{GDRV_RISE(ON)}$ | – | 30 | 50 | ns | [10] From 20% of $I_{CHGx}$ to $I_{CHGx}$, x = 0 to 63, $C_{Load}$ = 10 nF | P_12.11.26 |
| Gate Driver turn-off delay Time | $t_{DGDRV_OFF1}$ | – | – | 400 | ns | [10] From PWM[11] rising edge to 20% of $I_{DCHGx}$, x = 0 to 63, $C_{Load}$ = 10 nF, **BDFREQ** = 0 | P_12.11.27 |
| Gate Driver turn-off delay Time | $t_{DGDRV_OFF2}$ | – | – | 300 | ns | [10] From PWM[11] rising edge to 20% of $I_{DCHGx}$, x = 0 to 63, $C_{Load}$ = 10 nF, **BDFREQ** = 1 | P_12.11.94 |
| Gate Driver current turn-off rise time | $t_{GDRV_RISE(OFF)}$ | – | 30 | 50 | ns | [10] From 20% of $I_{DCHGx}$ to $I_{DCHGx}$, x = 0 to 63, $C_{Load}$ = 10 nF | P_12.11.28 |
| External MOSFET gate-to-source voltage - ON | $V_{GS(ON)1}$ | 7 | – | – | V | [1] $V_S \geq 8$ V, **FET_LVL**=1 | P_12.11.29 |
| External MOSFET gate-to-source voltage - ON | $V_{GS(ON)2}$ | 5.5 | – | – | V | [1] $V_S \geq 8$ V, **FET_LVL**=0 | P_12.11.100 |
| External MOSFET gate-to-source voltage - OFF | $V_{GS(OFF)1}$ | – | – | 1.5 | V | [1] IDCHGx ≤ $36_D$ (≤ 40 mA typ.) | P_12.11.30 |
| External MOSFET gate-to-source voltage - OFF | $V_{GS(OFF)2}$ | – | – | 3.8 | V | [1] IDCHGx > $36_D$ (> 40 mA typ.) | P_12.11.101 |
| PWM synchronization delay | $t_{PWM_SYNCH0}$ | 80 | – | 200 | ns | [1] **BDFREQ** = 0 | P_12.11.33 |
| PWM synchronization delay | $t_{PWM_SYNCH1}$ | 40 | – | 100 | ns | [1] **BDFREQ**= 1 | P_12.11.82 |
| Bridge driver frequency | $t_{BDFREQ0}$ | 16.8 | 18.75 | 20.7 | MHz | [1] **BDFREQ**= 0 | P_12.11.83 |
| Bridge driver frequency | $t_{BDFREQ1}$ | 33.7 | 37.5 | 42.3 | MHz | [1] **BDFREQ**= 1 | P_12.11.84 |

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**Table 26 Electrical characteristics: gate drivers** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V, $T_j$ = -40°C to +150°C,
$V_{CP} > V_S + 8.5$ V, $V_S$ = 6 to 19V, all voltages with respect to ground, positive current flowing into pin except for $I_{GLx}$ and $I_{GHx}$ (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Pre-charge time | $t_{PCHG000}$ | 80 | 107 | 140 | ns | 1) TPCHG = 000, **BDFREQ**= 0 or 1 | P_12.11.34 |
| Pre-charge time | $t_{PCHG001}$ | 130 | 160 | 190 | ns | 1) TPCHG = 001, **BDFREQ**= 0 or 1 | P_12.11.35 |
| Pre-charge time | $t_{PCHG010}$ | 170 | 214 | 260 | ns | 1) TPCHG = 010, **BDFREQ**= 0 or 1 | P_12.11.36 |
| Pre-charge time | $t_{PCHG011}$ | 210 | 267 | 330 | ns | 1) TPCHG = 011, **BDFREQ**= 0 or 1 | P_12.11.37 |
| Pre-charge time | $t_{PCHG100}$ | 250 | 320 | 390 | ns | 1) TPCHG = 100, **BDFREQ**= 0 or 1 | P_12.11.85 |
| Pre-charge time | $t_{PCHG101}$ | 420 | 533 | 630 | ns | 1) TPCHG = 101, **BDFREQ**= 0 or 1 | P_12.11.86 |
| Pre-charge time | $t_{PCHG110}$ | 600 | 747 | 900 | ns | 1) TPCHG = 110, **BDFREQ**= 0 or 1 | P_12.11.87 |
| Pre-charge time | $t_{PCHG111}$ | 840 | 1067 | 1260 | ns | 1) TPCHG = 111, **BDFREQ**= 0 or 1 | P_12.11.88 |
| Pre-discharge time | $t_{PDCHG000}$ | 80 | 107 | 140 | ns | 1) TPDCHG = 000, **BDFREQ**= 0 or 1 | P_12.11.38 |
| Pre-discharge time | $t_{PDCHG001}$ | 130 | 160 | 190 | ns | 1) TPDCHG = 001, **BDFREQ**= 0 or 1 | P_12.11.39 |
| Pre-discharge time | $t_{PDCHG010}$ | 170 | 214 | 260 | ns | 1) TPDCHG = 010, **BDFREQ**= 0 or 1 | P_12.11.40 |
| Pre-discharge time | $t_{PDCHG011}$ | 210 | 267 | 330 | ns | 1) TPDCHG = 011, **BDFREQ**= 0 or 1 | P_12.11.41 |
| Pre-discharge time | $t_{PDCHG100}$ | 250 | 320 | 390 | ns | 1) TPDCHG = 100, **BDFREQ**= 0 or 1 | P_12.11.89 |
| Pre-discharge time | $t_{PDCHG101}$ | 420 | 533 | 630 | ns | 1) TPDCHG = 101, **BDFREQ**= 0 or 1 | P_12.11.90 |
| Pre-discharge time | $t_{PDCHG110}$ | 600 | 747 | 900 | ns | 1) TPDCHG = 110, **BDFREQ**= 0 or 1 | P_12.11.91 |
| Pre-discharge time | $t_{PDCHG111}$ | 840 | 1067 | 1260 | ns | 1) TPDCHG = 111, **BDFREQ**= 0 or 1 | P_12.11.92 |
| **Low-side gate driver, CP off - Slam mode, parking braking and VS overvoltage braking** | | | | | | | |
| LS turn-on time, CP off | $t_{ON_BRAKE}$ | – | 4.5 | 9 | µs | $C_{LOAD}$ = 10 nF VGLx-VSL = 5 V, $V_S > 8$ V or $V_{SINT} > 8$ V | P_12.11.42 |

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**Table 26 Electrical characteristics: gate drivers** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V, $T_j$ = -40°C to +150°C,
$V_{CP} > V_S + 8.5$ V, $V_S$ = 6 to 19V, all voltages with respect to ground, positive current flowing into pin except for $I_{GLx}$ and $I_{GHx}$ (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| LS turn-off time, CP off | $t_{OFF_BRAKE}$ | – | 0.7 | 2 | µs | $C_{LOAD}$ = 10 nF VGLx-VSL = 1.5 V, $V_S > 8$ V or $V_{SINT} > 8$ V | P_12.11.43 |
| High output voltage GLx - SL | $V_{GLx_BRAKE}$ | 5 | – | 10 | V | $V_S > 8$ V or $V_{SINT} > 8$ V | P_12.11.48 |
| **Charge pump** | | | | | | | |
| Charge Pump Frequency | $f_{CP}$ | – | 250 | – | kHz | 1) | P_12.11.49 |
| Output Voltage VCP vs. VS | $V_{CPmin1}$ | 8.5 | – | – | V | $V_S$ = 6 V, $I_{CP}$ = - 6 mA, FET_LVL =1 | P_12.11.50 |
| Output Voltage VCP vs. VS | $V_{CPmin2}$ | 7.5 | – | – | V | $V_S$ = 6 V, $I_{CP}$ = - 6 mA, FET_LVL =0 | P_12.11.51 |
| Regulated CP output voltage, VCP vs. VS | $V_{CP1}$ | 12 | 15 | 17 | V | 8 V < $V_S$ < 23 V $I_{CP}$ = - 12 mA13), CPSTGA = 0, FET_LVL =1 | P_12.11.52 |
| Regulated CP output voltage, VCP vs. VS | $V_{CP2}$ | 12 | 15 | 17 | V | 18 V < $V_S$ < 23 V $I_{CP}$ = - 12 mA13), CPSTGA = 1, FET_LVL =1 | P_12.11.53 |
| Regulated CP output voltage, VCP vs. VS | $V_{CP3}$ | 7.5 | 11 | 13 | V | 8 V < $V_S$ < 23 V $I_{CP}$ = - 12 mA13), CPSTGA = 0, FET_LVL =0 | P_12.11.54 |
| Regulated CP output voltage, VCP vs. VS | $V_{CP4}$ | 7.5 | 11 | 13 | V | 13 V < $V_S$ < 23 V $I_{CP}$ = - 12 mA13), CPSTGA = 0, FET_LVL =0 | P_12.11.55 |
| Turn-on time | $t_{ON_VCP1}$ | 5 | – | 60 | µs | 1)12)13)18 V<$V_S$< 23 V (25%), $I_{CP}$ = 0 , CPSTGA = 1, FET_LVL =1 | P_12.11.56 |
| Rise time | $t_{RISE_VCP1}$ | 5 | 30 | 60 | µs | 1)12)13)18 V < $V_S$ < 23 V (25%-75%) $I_{CP}$ = 0 , CPSTGA = 1, FET_LVL =1 | P_12.11.57 |
| Turn-on time | $t_{ON_VCP2}$ | 20 | 60 | 120 | µs | 1)12)13) 13 V < $V_S$ <23 V (25%), $I_{CP}$ = 0, CPSTGA = 1, FET_LVL =0 | P_12.11.58 |

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**Table 26 Electrical characteristics: gate drivers** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V, $T_j$ = -40°C to +150°C,
$V_{CP} > V_S + 8.5$ V, $V_S$ = 6 to 19V, all voltages with respect to ground, positive current flowing into pin except for $I_{GLx}$ and $I_{GHx}$ (unless otherwise specified).

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Rise time | $t_{RISE_VCP2}$ | 5 | 30 | 60 | µs | [1)12)13)] 13 V < $V_S$ < 23 V (25%-75%) $I_{CP}$ = 0 , CPSTGA = 1, FET_LVL =0 | P_12.11.59 |
| Automatic switch over dual to single stage charge pump | $V_{CPSO\ DS}$ | 16 | 17 | 18 | V | CPSTGA = 1, FET_LVL =1, VS rising | P_12.11.60 |
| Automatic switch over dual to single stage charge pump | $V_{CPSO\ DS}$ | 11.5 | 12.25 | 13 | V | CPSTGA = 1, FET_LVL = 0, VS rising | P_12.11.61 |
| Automatic switch over single to dual stage charge pump | $V_{CPSO\ SD}$ | 15.5 | 16.5 | 17.5 | V | CPSTGA = 1, FET_LVL =1, VS falling | P_12.11.62 |
| Automatic switch over single to dual stage charge pump | $V_{CPSO\ SD}$ | 11 | 11.75 | 12.5 | V | CPSTGA = 1, FET_LVL = 0, VS falling | P_12.11.64 |
| Charge pump switch over hysteresis | $V_{CPSO\ HY}$ | – | 0.5 | – | V | [1)] CPSTGA = 1 $V_{CPSO\ DS}$ - $V_{CPSO\ SD}$ | P_12.11.65 |
| Charge pump minimum output current | $I_{CPOC1}$ | – | – | -12 | mA | [13)] 8 V < $V_S$ < 28 V CPSTGA = 0 FET_LVL =1 | P_12.11.68 |
| Charge pump minimum output current | $I_{CPOC2}$ | – | – | -12 | mA | [13)] 8 V < $V_S$ < 28 V CPSTGA = 0 FET_LVL =0 | P_12.11.69 |
| **Digital PWMx Inputs** | | | | | | | |
| High Level Input Voltage Threshold | $V_{PWMH}$ | – | – | 0.7 × $V_{cc1}$ | V | – | P_12.11.95 |
| Low Level Input Voltage Threshold | $V_{PWML}$ | 0.3 × $V_{cc1}$ | – | – | V | – | P_12.11.96 |
| PWMx Input Hysteresis | $V_{PWM,hys}$ | – | 0.12 × $V_{cc1}$ | – | V | [1)] | P_12.11.97 |
| PWMx Pull-down Resistance | $R_{PD_PWM}$ | 20 | 40 | 80 | kΩ | – | P_12.11.98 |
| **CRC Select; Pin PWM1/CRC** | | | | | | | |
| Config Pull-up Resistance | $R_{CFG}$ | | 100 | | kΩ | [14)] | P_12.11.99 |
| Config Select Filter Time | $t_{CFG_F}$ | 5 | 10 | 14 | µs | [1)] | P_12.11.105 |

1) Not subject to production test, specified by design.
2) Independent from **CPSTGA**.
3) ICP = -12 mA for VS ≥ 8 V, ICP = 6 mA for VS = 6 V.

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4) $V_{GS(ON)}$ = **$V_{GS(ON)1}$** if **FET_LVL** = 1, $V_{GS(ON)}$ = **$V_{GS(ON)2}$** if **FET_LVL** = 0.
5) (ICHGx@Tj=150°C - ICHGx@Tj=-40°C) / ICHGx@Tj=25°C
6) (IDCHGx@Tj=150°C - IDCHGx@Tj=-40°C) / IDCHGx@Tj=25°C
7) (ICHGx@VS=19V - ICHGx@VS=8V) / ICHGx@VS=13.5V
8) (IDCHGx@VS=19V - ICHGx@VS=8V) / IDCHGx@VS=13.5V
9) This resistance is the resistance between GHx and GND connected through a diode to SHx. As a consequence, the voltage at SHx can rise up to 0.6 V typ. before it is discharged through the resistor.
10) Not subject to production test, specified by design.
11) External PWM signal.
12) Parameter dependent on the capacitance $C_{CP}$.
13) $C_{CPC1}$ = $C_{CPC2}$ = 220 nF, $C_{CP}$ = 470 nF. Other $C_{CP}$ values higher than 470 nF can be used. Note that this capacitor influences the charge pump rise and turn-on times, and the charge , $V_{CP}$ ripple voltage when charging the gate of a MOSFET.
14) Config Pull-up will be only active during startup-phase for checking external pull-down. After checking, the typ. 40 kΩ Pull-down resistance will be present.

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# 13 Supervision Functions

## 13.1 Reset Function

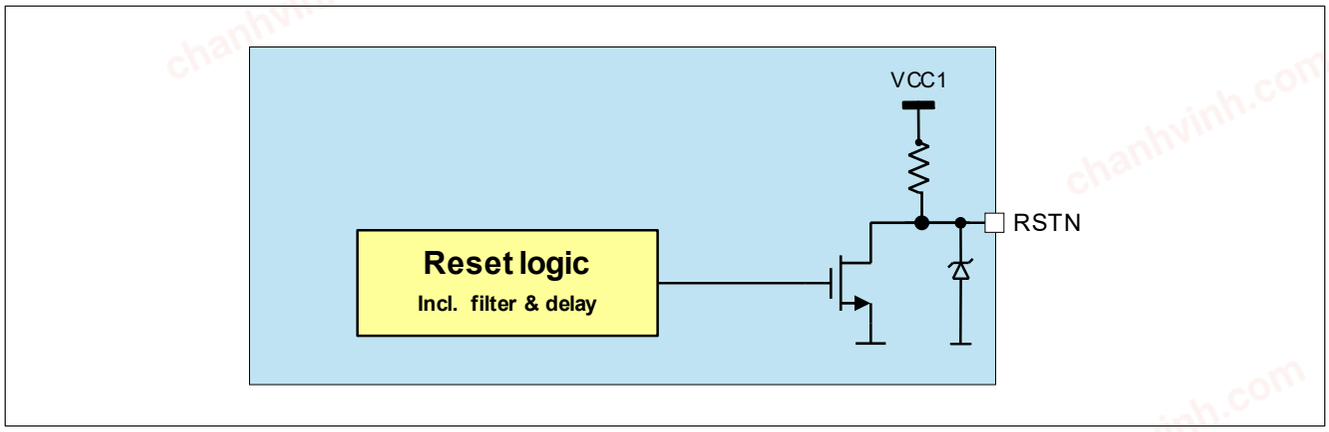



**Figure 75 Reset Block Diagram**

### 13.1.1 Reset Output Description

The reset output pin RSTN provides a reset information to the microcontroller, for example, in the event that the output voltage has fallen below the undervoltage threshold $V_{RTx}$. In case of a reset event, the reset output RSTN is pulled to low after the filter time **$t_{RF}$** and stays low as long as the reset event is present plus a reset delay time **$t_{RD1}$** or **$t_{RD2}$** depending on the value in **RSTN_DEL**. When connecting the device to battery voltage, the reset signal remains low initially. When the output voltage *V*CC1 has reached the reset default threshold $V_{RT1,r}$, the reset output RSTN is released to high after the reset delay time **$t_{RD1}$**. A reset can also occur due to a watchdog trigger failure. The reset threshold can be adjusted via SPI, the default reset threshold is **$V_{RT1,f}$**. The RSTN pin has an integrated pull-up resistor. In case reset is triggered, it will be pulled low for **VCC1** ≥ 1V and for VSINT ≥ **$V_{POR,f}$** (see also **Chapter 13.3**).

The timings for the RSTN triggering regarding VCC1 undervoltage and watchdog trigger is shown in **Figure 76**.

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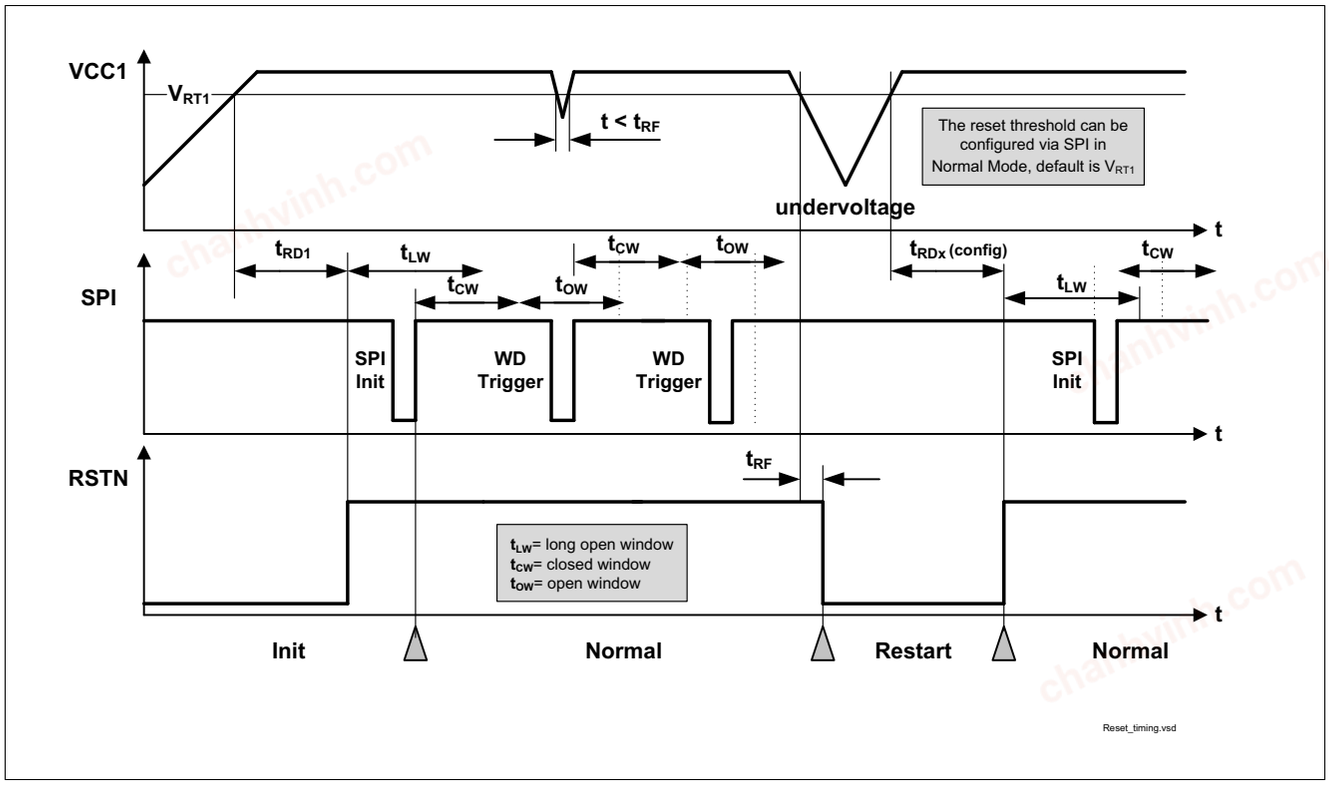



**Figure 76 Reset Timing Diagram**

### 13.1.2 Soft Reset Description

In Normal Mode and Stop Mode, it is also possible to trigger a device internal reset via a SPI command in order to bring the device into a defined state in case of failures. In this case the microcontroller must send a SPI command and set the **MODE** bits to '11' in the **M_S_CTRL** register. As soon as this command becomes valid, the device is set back to Init Mode and all SPI registers are set to their default values (see SPI **Chapter 14.5.1** and **Chapter 14.6.1**).

Two different soft reset configurations are possible via the SPI bit **SOFT_RESET_RO**:

- **SOFT_RESET_RO** = '0': The reset output (RSTN) is triggered when the soft reset is executed (default setting) The configured reset delay time **$t_{RD1}$** or **$t_{RD2}$** is applied depending on the value in **RSTN_DEL**).
- **SOFT_RESET_RO** = '1': The reset output (RSTN) is not triggered when the soft reset is executed.

*Note: The device must be in Normal Mode or Stop Mode when sending this command. Otherwise, the command will be ignored.*

*Note: Allow CRC configuration after software-reset - or better check once again via SPI after software reset.*

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## 13.2 Watchdog Function

The watchdog is used to monitor the software execution of the microcontroller and to trigger a reset or move the device to Fail Safe Mode, if the microcontroller stops serving the watchdog due to a lock up in the software.

Two different types of watchdog functions are implemented and can be selected via the bit **WD_CFG**:

- Time-Out Watchdog (default value)
- Window Watchdog

The respective watchdog functions can be selected and programmed in Normal Mode. The configuration stays unchanged in Stop Mode.

Please refer to **Table 27** to match the device modes with the respective watchdog modes.

**Table 27 Watchdog Functionality by modes**

| Mode | Watchdog Mode | Remarks |
|---|---|---|
| Init Mode | Starts with Long Open Window | Watchdog starts with Long Open Window after RSTN is released. |
| Normal Mode | WD Programmable | Window Watchdog, Time-Out watchdog or switched off for Stop Mode. |
| Stop Mode | Watchdog is fixed or off | |
| Sleep Mode | Off | Device will start with Long Open Window when entering Normal Mode. |
| Restart Mode | Off | Device will start with Long Open Window when entering Normal Mode. |

The watchdog timing is programmed via SPI command in the register **WD_CTRL**. As soon as the watchdog is programmed, the timer starts with the new setting and the watchdog must be served. The watchdog is triggered by sending a valid SPI-write command to the watchdog configuration register. The watchdog trigger command is executed when the SPI command is interpreted.

When coming from Init Mode, Restart Mode or in certain cases from Stop Mode, the watchdog timer is always started with a long open window. The long open window ($t_{LW}$) allows the microcontroller to run its initialization sequences and then to trigger the watchdog via SPI.

The watchdog timer period can be selected via SPI (**WD_TIMER**).The timer setting is valid for both watchdog types.

The following watchdog timer periods are available:

- WD Setting 1: 10 ms
- WD Setting 2: 20 ms
- WD Setting 3: 50 ms
- WD Setting 4: 100 ms
- WD Setting 5: 200 ms
- WD Setting 6: 500 ms
- WD Setting 7: 1 s
- WD Setting 8: 10 s

In case of a reset, Restart Mode or Fail-Safe Mode is entered according to the configuration and the SPI bits **WD_FAIL** are set. Once the RSTN goes high again the watchdog immediately starts with a long open window the device enters automatically Normal Mode.

The Watchdog behaviour in Software Development Mode is described in **Chapter 5.4.7**.

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In case a watchdog-trigger was missed in Software Development Mode, the watchdog will start with the long-open-window once again.

The **WD_FAIL** bits will be set after a watchdog trigger failure.

The **WD_FAIL** bits are cleared automatically when following conditions apply:

- After a successful watchdog trigger.
- When the watchdog is off: in Stop Mode after successfully disabling it, in Sleep Mode, or in Fail-Safe Mode (except for a watchdog failure).

### 13.2.1 Time-Out Watchdog

The time-out watchdog is an easier and less secure watchdog than a window watchdog as the watchdog trigger can be done at any time within the configured watchdog timer period.

A correct watchdog service immediately results in starting a new watchdog timer period. Taking the tolerances of the internal oscillator into account leads to the safe trigger area as defined in **Figure 77**.

If the time-out watchdog period elapses, a watchdog reset is created by setting the reset output RSTN low and the device switches to Restart Mode or Fail-Safe Mode.

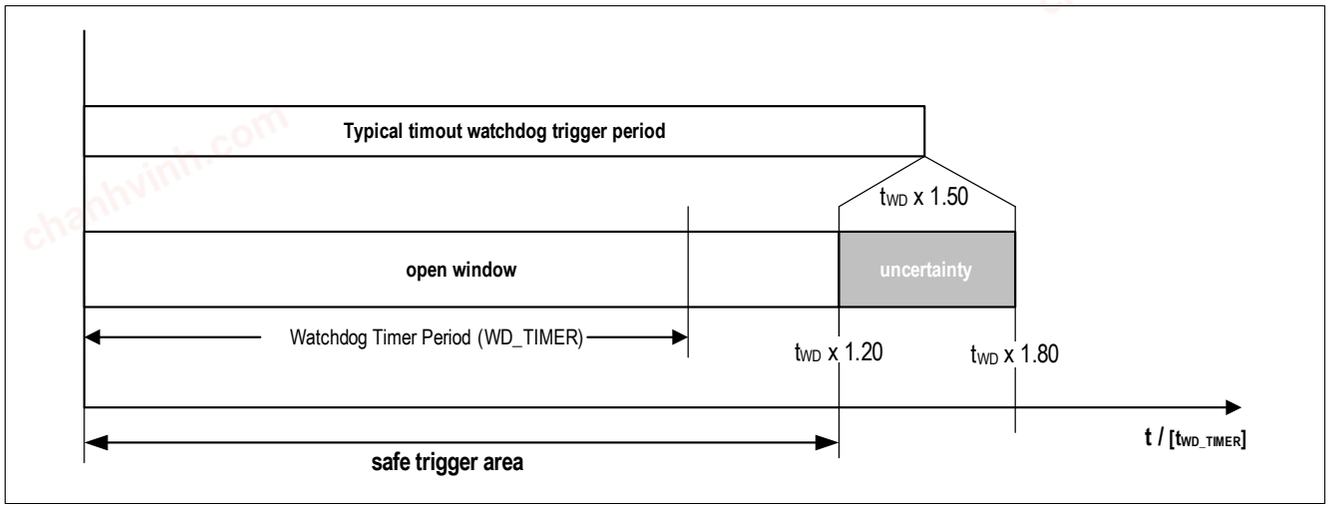



**Figure 77 Time-out Watchdog Definitions**

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### 13.2.2 Window Watchdog

Compared to the time-out watchdog the characteristic of the window watchdog is that the watchdog timer period is divided between a closed and an open window. The watchdog must be triggered within the open window.

A correct watchdog trigger results in starting the window watchdog period by a closed window followed by an open window.

The watchdog timer period is at the same time the typical trigger time and defines the middle of the open window. Taking the oscillator tolerances into account leads to a safe trigger area of:

$t_{WD} \times 0.72 <$ safe trigger area $< t_{WD} \times 1.20$.

The typical closed window is defined to a width of 60% of the selected window watchdog timer period. Taking the tolerances of the internal oscillator into account leads to the timings as defined in **Figure 78**.

A correct watchdog service immediately results in starting the next closed window.

If the trigger signal meet the closed window or if the watchdog timer period elapses, then a watchdog reset is triggered (RSTN low) and the device switches to Restart Mode or Fail-Safe Mode.

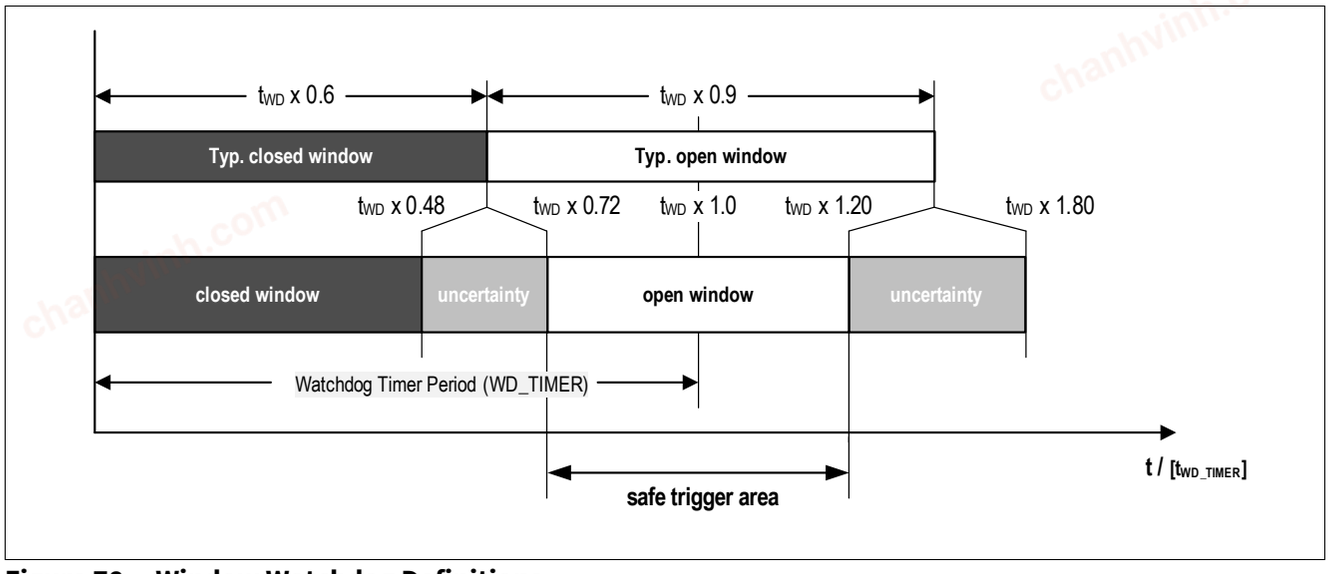



**Figure 78 Window Watchdog Definitions**

### 13.2.3 Watchdog Setting Check Sum

A check sum bit is part of the SPI command to trigger the watchdog and to set the watchdog setting.

The sum of the 16 data bits in the register **WD_CTRL** needs to have even parity (see **Equation (13.1)**). This is realized by either setting the bit **CHECKSUM** to 0 or 1. If the check sum is wrong, then the SPI command is ignored, i.e. the watchdog is not triggered or the settings are not changed and the bit SPI_FAIL is set.

The written value of the reserved bits of the **WD_CTRL** register is considered (even if read as '0' in the SPI output) for checksum calculation, i.e. if a 1 is written on the reserved bit position, then a 1 will be used in the checksum calculation.

(13.1)

$$\mathrm{Bit(CHECKSUM)} = \mathrm{Bit22} \oplus \ldots \oplus \mathrm{Bit8}$$

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### 13.2.4 Watchdog during Stop Mode

The watchdog can be disabled for Stop Mode in Normal Mode. For safety reasons, there is a special sequence to be followed in order to disable the watchdog as described in **Figure 79**. Two different SPI bits (**WD_STM_EN_0**, **WD_STM_EN_1**) in the registers **HW_CTRL** and **WD_CTRL** need to be set.

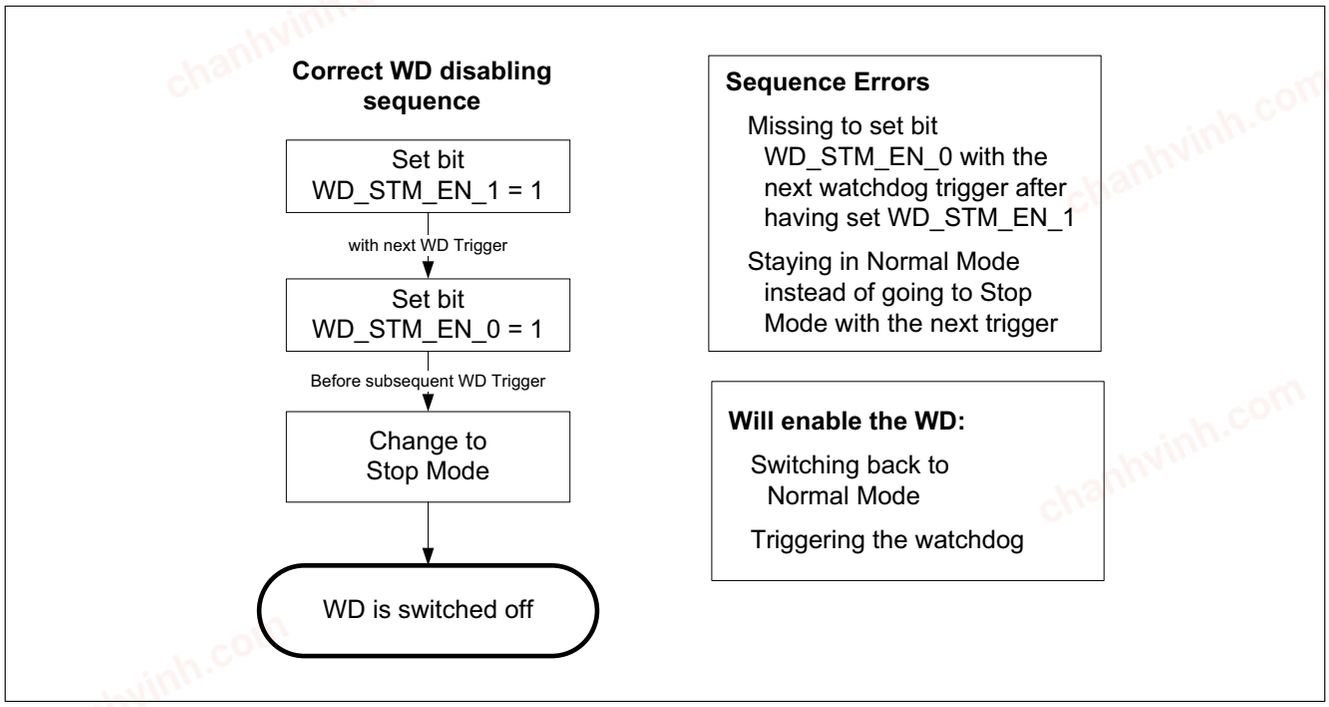



**Figure 79 Watchdog disabling sequence in Stop Mode**

If a sequence error occurs, then the bit **WD_STM_EN_1** will be cleared and the sequence has to be started again.

The watchdog can be enabled by triggering the watchdog in Stop Mode or by switching back to Normal Mode via SPI command. In both cases the watchdog will start with a long open window and the bits **WD_STM_EN_1** and **WD_STM_EN_0** are cleared. After the long open window the watchdog has to be served as configured in the **WD_CTRL** register.

*Note: The bit **WD_STM_EN_0** will be cleared automatically when the sequence is started and it was 1 before. **WD_STM_EN_0** can also not be set if **WD_STM_EN_1** isn't yet set.*

### 13.2.5 Watchdog Start in Stop Mode due to Bus Wake

In Stop Mode the Watchdog can be disabled. In addition a feature is available which will start the watchdog with any BUS wake (CAN, LIN) during Stop Mode. The feature is enabled by setting the bit **WD_EN_ WK_BUS** = 1 (default value after POR). The bit can only be changed in Normal Mode and needs to be programmed before starting the watchdog disable sequence.

A wake on the Bus will generate an interrupt and the RXDCAN, RXDLIN is pulled to low. By these signals the microcontroller is informed that the watchdog is started with a long open window. After the long open window the watchdog has to be served as configured in the **WD_CTRL** register.

To disable the watchdog again, the device needs to be switched to Normal Mode and the sequence needs to be sent again.

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## 13.3 VSINT Power On Reset

At power up of the device, the Power on Reset is detected when VSINT > $V_{POR,r}$ and the SPI bit **POR** is set to indicate that all SPI registers are set to POR default settings. VCC1 is starting up and the reset output will be kept low and will only be released once VCC1 has crossed $V_{RT1,r}$ and after $t_{RD1}$ has elapsed.
In case VSINT < $V_{POR,f}$, an device internal reset will be generated and the device is switched off and will restart in Init Mode at the next VSINT rising. This is shown in **Figure 80**.

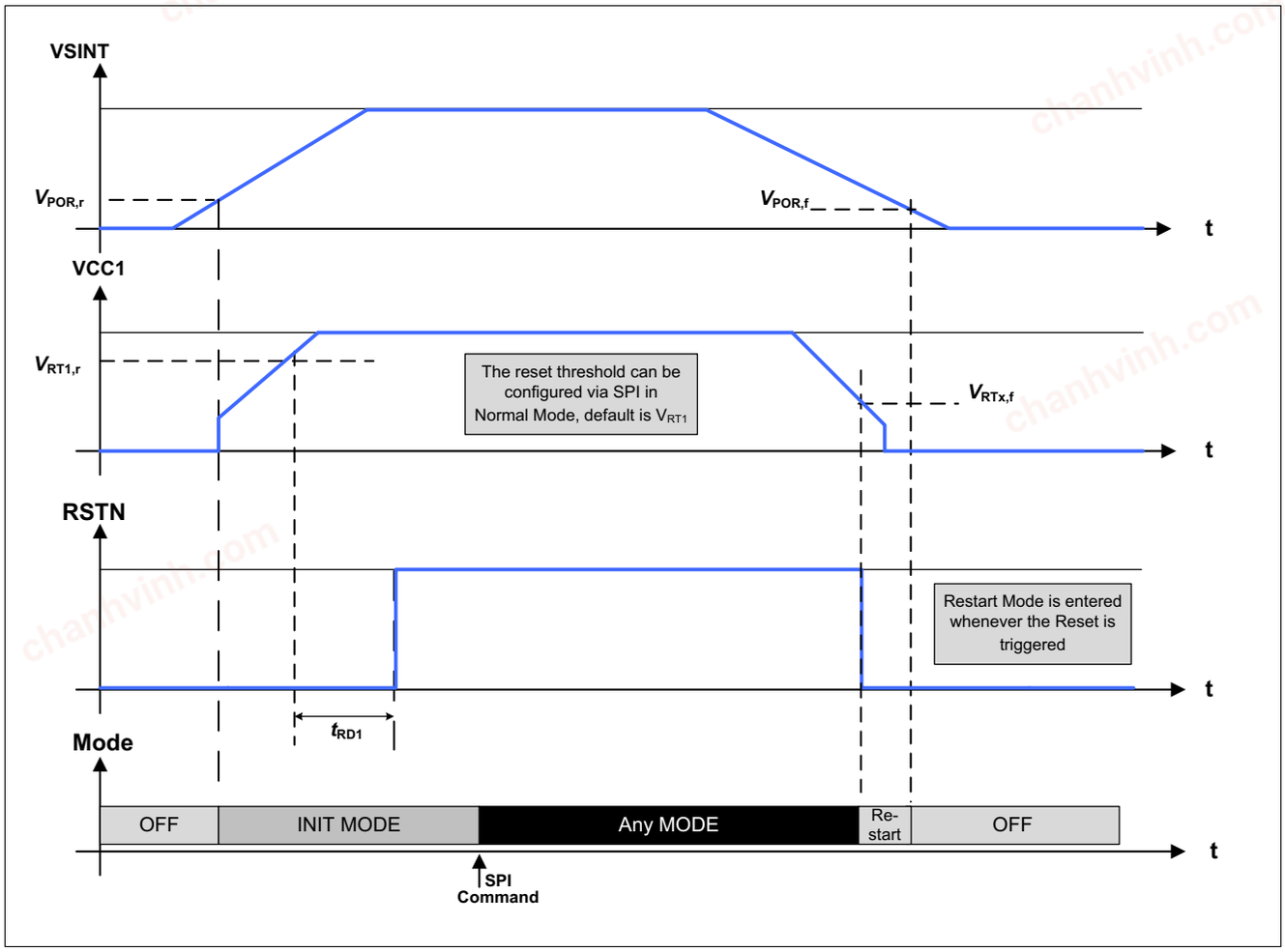



**Figure 80 Ramp up / down example of Supply Voltage**

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## 13.4 VSINT Under- and Overvoltage

### 13.4.1 VSINT Undervoltage

The VSINT under-voltage monitoring is always active in Init Mode, Restart Mode, Normal Mode. If the supply voltage VSINT drops below $V_{SINT,UV}$ for more than $t_{VSUV_FILT}$, then the device does the following measures:

- The VCC1 short circuit diagnosis becomes inactive (see **Chapter 13.8**). However, the thermal protection of the device remains active. If the undervoltage threshold is exceeded (VSINT rising) then the function will be automatically enabled again.
- The status bit **VSINT_UV** is set and latched until a clear command of **SUP_STAT** is received.

*Note: VSINT under-voltage monitoring is not available in Stop Mode due to current consumption saving requirements except if the VCC1 load current is above the active peak threshold (I_PEAK_TH) or if VCC1 is below the VCC1 prewarning threshold.*

### 13.4.2 VSINT Overvoltage

The VSINT over-voltage monitoring is always active in Init Mode, Restart Mode and Normal Mode. If VSINT rises above $V_{S,OVD1}$, $V_{S,OVD2}$ for more than $t_{VSOV_FILT}$ then the device does the following measures:

1. If HBxMODE = 01b or 10b , then the corresponding MOSFETs are actively turned off with their static discharge current during their respective tHBxCCP Active.
2. Then the charge pump is turned off and the passive discharge is activated.
3. The status bits **VSINT_OV** is set and latched until a clear command of **SUP_STAT** is received.

If VS or VSINT fall below $V_{S,OVD1}$ or $V_{S,OVD2}$:

- If **CPEN** = 0 : the charge pumps stays and the bridge driver stay off.
- If **CPEN** = 1 :
  - If **BDOV_REC** = 0 : Then the charge pump is reactivated but the bridge driver stays off until **VS_OV** and **VSINT_OV** are cleared.
  - If **BDOV_REC** = 1 : Then the charge pump is reactivated and the bridge driver is enabled if VCP > $V_{CPUVx}$, even if **VS_OV** or **VSINT_OV** is set. The state of the external MOSFETs is according to the control registers.

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## 13.5 VS Under- and Overvoltage

### 13.5.1 VS Undervoltage

The VS under-voltage monitoring is always active in Init-, Restart Mode and Normal Mode. If VS drops below **$V_{S,UV}$** for more than **$t_{VSUV_FILT}$**, then the device does the following measures:

1. If HBxMODE = 01b or 10b , then the corresponding MOSFETs are actively turned off with their static discharge current during their respective tHBxCCP Active.
2. Then the charge pump is turned off and the passive discharge is activated .
3. The status bits **VS_UV** is set and latched until a clear command of **SUP_STAT** is received.

If VS rises above **$V_{S,UV}$**, then the charge pump is reactivated (provided that **CPEN** is set) but the bridge driver stays off until **VS_UV** is cleared. The bridge driver will be reactivated once the VS_UV bit is cleared.

### 13.5.2 VS Overvoltage

The VS over-voltage monitoring is always active in Init-, Restart Mode and Normal Mode or when the charge pump is enabled. If VS rises above **$V_{S,OVD1}$** or **$V_{S,OVD2}$** for more than **$t_{VSOV_FILT}$**, then the device does the following measures:

1. If HBxMODE = 01b or 10b , then the corresponding MOSFETs are actively turned off with their static discharge current during their respective tHBxCCP Active.
2. Then the charge pump is turned off and the passive discharge is activated.
3. The status bits **VS_OV** is set and latched until a clear command of **SUP_STAT** is received.

If VS and VSINT fall below **$V_{S,OVD1}$** or **$V_{S,OVD2}$**:

- If **CPEN** = 0 : the charge pumps and the bridge driver stay off.
- If **CPEN** = 1 :
  - If **BDOV_REC** = 0 : Then the charge pump is reactivated (provided that **CPEN** = 1 and **CP_UV** = 0) but the bridge driver stays off until **VS_OV** and **VSINT_OV** are cleared.
  - If **BDOV_REC** = 1 : Then the charge pump is reactivated and the bridge driver is enabled if VCP > $V_{CPUVx}$, even if **VS_OV** or **VSINT_OV** is set. The state of the external MOSFETs is according to the control registers.

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## 13.6 VSHS Under- Overvoltage

### 13.6.1 VSHS Undervoltage

If the supply voltage VSHS passes below the undervoltage threshold ($V_{SHS,UVD}$) the device does the following measures:

- HS1...4 are acting accordingly to the SPI setting (refer also to **Chapter 7.2.1**).
- LIN: Transmitter and Receiver are disabled during the VSHS undervoltage condition.
- SPI bit **HS_UV** is set. No other error bits are set. The bit can be cleared once the condition is not present anymore.

### 13.6.2 VSHS Overvoltage

If the supply voltage VSHS reaches the overvoltage threshold ($V_{SHS,OVD}$) the device triggers the following measures:

- HS1...4 are acting accordingly to the SPI setting (refer also to **Chapter 7.2.2**).
- The status bit **HS_OV** is set. No other error bits are set. The bit can be cleared once the condition is not present anymore.

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## 13.7 VCC1 Over-/ Undervoltage and Undervoltage Prewarning

### 13.7.1 VCC1 Undervoltage and Undervoltage Prewarning

This function is always active when the VCC1 voltage regulator is enabled.
A first-level voltage detection threshold is implemented as a prewarning for the microcontroller. The prewarning event is signaled with the bit **VCC1_WARN**. No other actions are taken.

As described in **Chapter 13.1** and **Figure 81**, a reset will be triggered (RSTN pulled low) when the $V_{CC1}$ output voltage falls below the selected undervoltage threshold ($V_{RTx}$). The device will enter Restart Mode and the bit **VCC1_UV** is set when RSTN is released again.

The hysteresis of the VCC1 undervoltage threshold can be increased by setting the bit **RSTN_HYS**. In this case always the highest rising threshold ($V_{RT1,R}$) is used for the release of the undervoltage reset. The falling reset threshold remains as configured.

An additional safety mechanism is implemented to avoid repetitive VCC1 undervoltage resets due to high dynamic loads on VCC1:

- A counter is increased for every consecutive VCC1 undervoltage event (regardless on the selected reset threshold).
- The counter is active in Init Mode, Normal Mode and Stop Mode.
- For VS < **$V_{SINT,UV}$** the counter will be stopped in Normal Mode (i.e. the VS UV comparator is always enabled in Normal Mode).
- A 4th consecutive VCC1 undervoltage event will lead to Fail-Safe Mode entry and to setting the bit **VCC1_UV_FS**.
- This counter is cleared:
  - When Fail-Safe Mode is entered.
  - When the bit VCC1_UV is cleared.
  - When a Soft-Reset is triggered.

*Note: After 4 consecutive VCC1_UV events, the device will enter Fail-Safe Mode and the **VCC1_UV_FS** bit is set.*

*Note: The **VCC1_WARN** or **VCC1_UV** bits are not set in Sleep Mode as $V_{CC1}$ = 0 V in this case.*

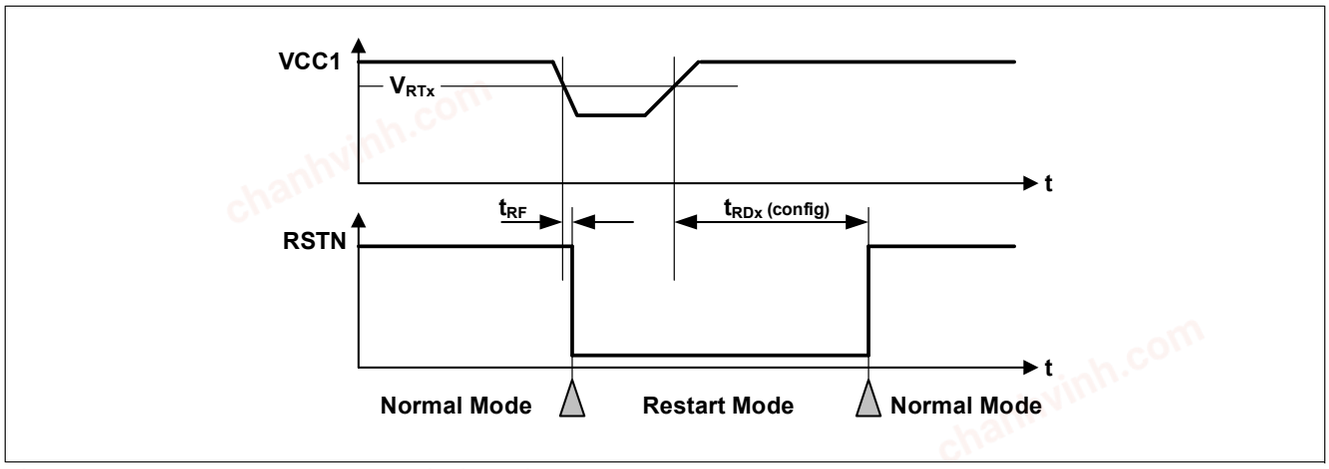



**Figure 81 VCC1 Undervoltage Timing Diagram**

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*Note: It is recommended to clear the **VCC1_WARN** and **VCC1_UV** bit once it is detected by the microcontroller software to verify if the undervoltage still exists or not.*

### 13.7.2 VCC1 Overvoltage

For fail-safe reasons a configurable VCC1 over voltage detection feature is implemented. It is active when the VCC1 voltage regulator is enabled.

In case the **$V_{CC1,OV,r}$** threshold is crossed, the device triggers following measures depending on the configuration:

- The bit **VCC1_OV** is always set.
- Based on the configuration of **VCC1_OV_MOD**, different kind of event are generated from device.
- If the **VCC1_OV_MOD**=$11_B$, in case of the device enters in Fail Safe Mode, the Fail Safe Output is activated (according **WK2_FO** setting).

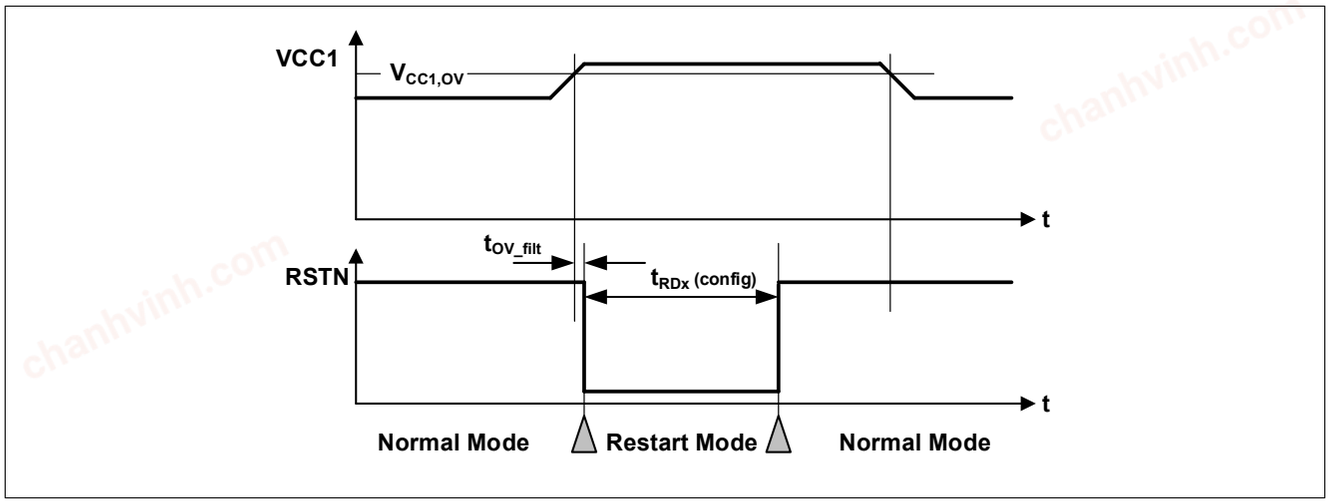



**Figure 82 VCC1 Over Voltage Timing Diagram**

## 13.8 VCC1 Short Circuit Diagnostics

The short circuit protection feature for $V_{CC1}$ is implemented as follows:

- The short circuit detection is only enabled if VS > **$V_{SINT,UV}$**.
- If VCC1 is not above the $V_{RTx}$ within **$t_{VCC1,SC}$** after device power up or after waking from Sleep Mode or Fail-Safe Mode (i.e. after VCC1 is enabled) then the SPI bit **VCC1_SC** bit is set, VCC1 is turned off, the FO pin is enabled, **FAILURE** is set and Fail-Safe Mode is entered. The device can be activated again via a wake-up sources.
- The same behavior applies, if $V_{CC1}$ falls below $V_{RTx}$ for longer than **$t_{VCC1,SC}$**.

## 13.9 VCAN Undervoltage

An undervoltage warning is implemented for VCAN as follows:

- $V_{CAN}$ undervoltage detection: In case *the CAN module is enabled and the voltage on* $V_{CAN}$ will drop below the $V_{CAN_UV,f}$ threshold, then the SPI bit **VCAN_UV** is set and can be only cleared via SPI.

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## 13.10 Thermal Protection

Three independent and different thermal protection features are implemented in the device according to the system impact:

- Individual thermal shutdown of specific blocks
- Temperature prewarning of VCC1 voltage regulator
- Device thermal shutdown due to VCC1 overtemperature

### 13.10.1 Individual Thermal Shutdown

As a first-level protection measure, LIN, CAN, HSx and the charge pump are independently switched off if the respective block reaches the temperature threshold **$T_{jTSD1}$**. Then the **TSD1** bit is set. This bit can only be cleared via SPI once the overtemperature is not present anymore. Independent of the device mode the thermal shutdown protection is only active if the respective block is ON.

The respective modules behave as follows:

- CAN: The transmitter is disabled and stays in CAN Normal Mode acting like CAN Receive Only Mode. The status bits **CAN_FAIL** are set to '01'. Once the overtemperature condition is not present anymore, then the CAN transmitter is automatically switched on.
- LIN: The transmitter is disabled and stays in LIN Normal Mode acting like LIN Receive Only Mode. The status bits **LIN_FAIL** are set to '01'. Once the over temperature condition is not present anymore, then the LIN transmitter is automatically switched on.
- HSx: If one or more HSx switches reach the TSD1 threshold, then the HSx switches are turned OFF (depending on configuration either individually or all at once) and the control bits for HSx are cleared based on **HS_OT_SD_DIS** setting. The status bits HSx_OT are set (see register **HS_OL_OC_OT_STAT**). Once the over temperature condition is not present anymore, then HSx has to be configured again by SPI.
- Charge pump: If the charge pump reaches **$T_{jTSD1}$**, then **CP_OT** is set, **CPEN** is cleared and the activated MOSFETs are actively discharged with their respective static currents during their respective active cross current protection times (tHBxCCP active). When all tHBxCCP active elapsed, then the charge pump and the MOSFETs active discharge are disabled . Once the over temperature condition is not present anymore, then **CPEN** has to be configured again by SPI.

*Note: The diagnosis bits are not cleared automatically and have to be cleared via SPI once the overtemperature condition is not present anymore.*

### 13.10.2 Temperature Prewarning

As a next level of thermal protection a temperature prewarning is implemented if the main supply VCC1 reaches the thermal prewarning temperature threshold $T_{jPW}$. Then the status bit **TPW** is set. This bit can only be cleared via SPI once the overtemperature is not present anymore.

### 13.10.3 Thermal Shutdown

As a highest level of thermal protection a temperature shutdown of the device is implemented if the main supply VCC1 reaches the thermal shutdown temperature threshold $T_{jTSD2}$. Once a TSD2 event is detected Fail-Safe Mode is entered. Only when device temperature falls below the TSD2 threshold then the device remains in Fail-Safe Mode for **$t_{TSD2}$** to allow the device to cool down. After this time has expired, the device will automatically change via Restart Mode to Normal Mode (see also **Chapter 5.4.6**).

When a TSD2 event is detected, then the status bit **TSD2** is set. This bit can only be cleared via SPI in Normal Mode once the overtemperature is not present anymore.

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## Supervision Functions

For increased robustness requirements it is possible to extend the TSD2 waiting time by 64x of $t_{TSD2}$ after 16 consecutive TSD2 events by setting the SPI bit **TSD2_DEL**. The counter is incremented with each TSD2 event even if the bit **TSD2** is not cleared. Once the counter has reached the value 16, then the bit **TSD2_SAFE** is set and the extended TSD2 waiting time is active. The extended waiting time will be kept until **TSD2_SAFE** is cleared. The TSD counter is cleared when **TSD2** or **TSD2_DEL** is cleared.

*Note: In case a TSD2 overtemperature occurs while entering Sleep Mode then Fail-Safe Mode is still entered.*

*Note: In case of a TSD2 event, the **FAILURE** bit is set to '1' and the **DEV_STAT** field is set to '01' inside the **DEV_STAT** register.*

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## 13.11 Bridge driver

This section describes the supervision functions related to the bridge driver.

### 13.11.1 Bridge driver supervision with activated charge pump

This section describes the supervision functions when the charge pump is activated.

#### 13.11.1.1 Drain-source voltage monitoring

Voltage comparators monitor the activated MOSFETs to protect high-side MOSFETs and low-side MOSFETs against a short circuit respectively to ground and to the battery during ON-state.

A drain-source overvoltage is detected on a low-side MOSFET if the voltage difference between VSHx and SL exceeds the threshold voltage configured by **LS_VDS** (see **Table 28**). Consequently, the corresponding half-bridge is latched off with the static discharge current.

A drain-source overvoltage is detected on a high-side MOSFET if the voltage difference between VS and VSHx exceeds the threshold voltage configured by **HS_VDS** (see **Table 29**). Consequently, the corresponding half-bridge is latched off with the static discharge current.

**Table 28 Low-side drain-source overvoltage threshold**

| LSxVDSTH[2:0] | Drain-Source overvoltage threshold for LSx (typical) |
|---|---|
| $000_B$ | 160 mV |
| $001_B$ | 200 mV (default) |
| $010_B$ | 300 mV |
| $011_B$ | 400 mV |
| $100_B$ | 500 mV |
| $101_B$ | 600 mV |
| $110_B$ | 800 mV |
| $111_B$ | 2 V |

**Table 29 High-side drain-source overvoltage threshold**

| HSxVDSTH[2:0] | Drain-Source overvoltage threshold for HSx (typical) |
|---|---|
| $000_B$ | 160 mV |
| $001_B$ | 200 mV (default) |
| $010_B$ | 300 mV |
| $011_B$ | 400 mV |
| $100_B$ | 500 mV |
| $101_B$ | 600 mV |
| $110_B$ | 800 mV |
| $111_B$ | 2 V |

***Attention: 2 V threshold is dedicated for the diagnostic in off-state. It is highly recommended to select another drain-source overvoltage threshold once the routine of the diagnostic in off-state has been performed to avoid additional current consumption from VS and from the charge pump.***

The device reports a Drain-Source overvoltage error if both conditions are met:

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- After expiration of the blank time .
- If the Drain-Source voltage monitoring exceeds the configured threshold for a duration longer than the configured filter time (refer to **Table 30** and **LS_VDS** TFVDS bits).

**Table 30 Drain-Source overvoltage filter time**

| TFVDS[2:0] | Drain-Source overvoltage filter time (typical) |
|---|---|
| $00_B$ | 0.5 µs (default) |
| $01_B$ | 1 µs |
| $10_B$ | 2 µs |
| $11_B$ | 6 µs |

If a short circuit is detected by the Drain-Source voltage monitoring:

- The impacted half-bridge is latched off with the static discharge current for the configured cross-current protection time.
- The corresponding bit in the status register **DSOV** is set.
- The DSOV bit in Global Status Register **GEN_STAT** is set.

If a Drain-Source overvoltage is detected for one of the MOSFETs, then the status register **DSOV** must be cleared in order to re-enable the faulty half-bridge.

### 13.11.1.2 Cross-current protection and drain-source overvoltage blank time

All gate drivers feature a cross-current protection time and a Drain-Source overvoltage blank time.

The cross-current protection avoids the simultaneous activation of the high-side and the low-side MOSFETs of the same half-bridge.

During the blank time, the drain-source overvoltage detection is disabled, to avoid a wrong fault detection during the activation phase of a MOSFET.

*Note: The setting of the cross-current protection and of the blank times may be changed by the microcontroller only if all HBx_PWM_EN bits are reset.*

*Note: Changing the Drain-Source overvoltage of a half-bridge x (HBx) in on-state (HBxMODE[1:0]=(0,1) or (1,0)) may result in a wrong VDS overvoltage detection on HBx. Therefore it is highly recommended to change this threshold when HBxMODE[1:0]=(0,0) or (1,1)*

#### 13.11.1.2.1 Cross-current protection

The active and freewheeling cross-current protection times of each half-bridge is configured individually with the control register **CCP_BLK**.

The typical cross-current protection time applied to the freewheeling MOSFET of the half-bridge x is 587 ns + 266 ns x $TCCP[3:0]_D$, where $TCCP[3:0]_D$ is the decimal value of the control bits TCCP.

#### 13.11.1.2.2 Drain-source overvoltage blank time

A configurable blank time for the Drain-Source monitoring is applied at the turn-on of the MOSFETs. During the blank time, a Drain-Source overvoltage error is masked.

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For Half-Bridges in PWM mode with AFWx = 1:

- the blank time of the PWM MOSFET starts at the expiration of the cross-current protection time of the PWM MOSFET. Refer to **Figure 83**.
- the blank time of the free-wheeling MOSFET starts after expiration of the cross-current protection time at turn-off of the PWM MOSFET. Refer to **Figure 83**.

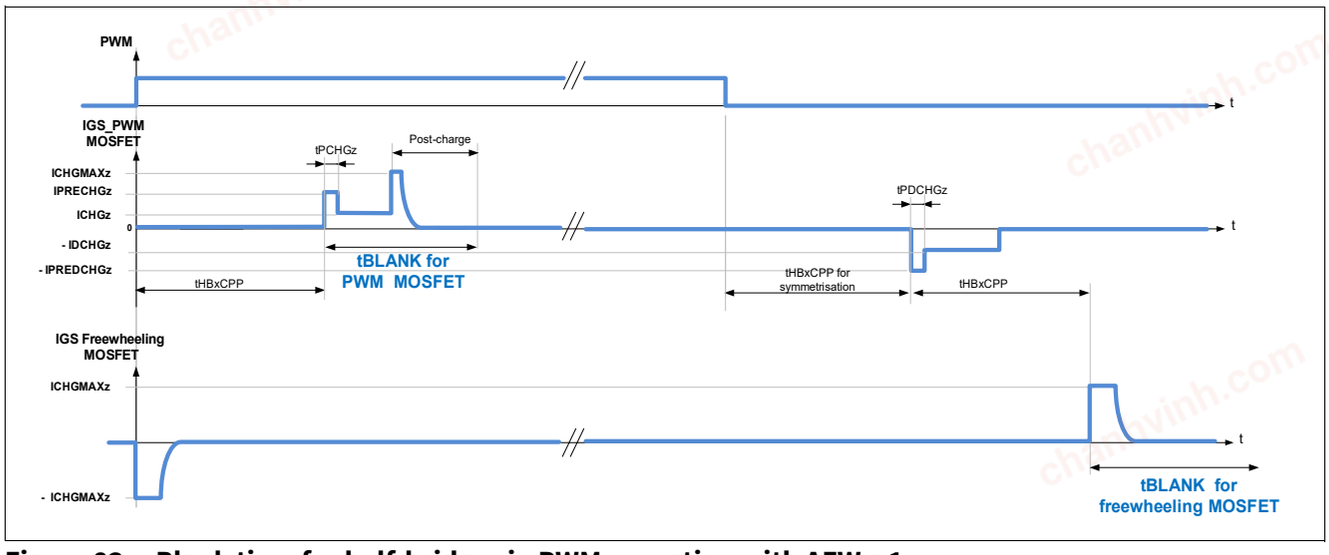



**Figure 83 Blank time for half-bridges in PWM operation with AFW = 1**

For statically activated half-bridges, the blank time starts:

- Case1: at expiration of the cross-current protection (**Figure 43**), if the opposite MOSFET was previously activated.
- Case 2: right after the decoding of the SPI command to turn on a MOSFET, if the half-bridge was in high impedance (**Figure 44**).

The blank times of the active and FW MOSFETs can be configured with the control register **CCP_BLK**.

The typical blank is 587 ns + 266 ns x $TBLK[3:0]_D$).

*Note: The blank time is implemented at every new activation of a MOSFET, including a recovery from VS undervoltage, VS overvoltage, VSINT overvoltage, CP UV, CP OT.*

### 13.11.1.3 OFF-state diagnostic

In order to support the off-state diagnostic (HBxMODE= 11 and **CPEN** = 1), the gate driver of each MOSFET provides pull-up ($I_{PUDiag}$) and a pull-down currents ($I_{PDDiag}$) at the SHx pins. This function requires an activated charge pump.

The pull-up current source of a given half-bridge is on when the half-bridge is active: HBxMODE= 01, 10 or 11 and **CPEN** = 1.

The pull-down current of each low-side gate driver is activated by the control bits HBx (**HB_ICHG_MAX** register).

During the off-state diagnostic routine performed by the microcontroller, the drain-source overvoltage threshold of the relevant half-bridges must be set to 2V nominal. Refer to **Table 28**. Once the routine is finished, it is highly recommended to decrease the drain-source overvoltage threshold to a lower value, avoiding additional current consumption from the VS input.

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The following failures can be detected:

- MOSFET short circuit to GND
- MOSFET short circuit the battery
- Open load (disconnected motor)

The status of the output voltages VOUTx, can be read back with status bit HBxVOUT (register **GEN_STAT**) when the corresponding half-bridge is in off-state (HBxMODE[1:0] = 11).

*Note: HBxVOUT = 0 if the half-bridge x is not actively off (HBxMODE[1:0] = (0,0), (0,1) or (1,0) and **CPEN**=1) or when the charge pump is deactivated (**CPEN**=0).*

### 13.11.1.4 Charge pump undervoltage

The voltage of the charge pump output (VCP) is monitored in order to ensure a correct control of the external MOSFETs.

The charge pump undervoltage threshold is configurable by the control bits **FET_LVL** and **CPUVTH**.

**Table 31 Charge pump undervoltage thresholds**

| | **FET_LVL = 0** | **FET_LVL = 1** |
|---|---|---|
| CPUVTH = 0 | $V_{CPUV1}$ (6 V typ. referred to VS) | $V_{CPUV3}$ (7.5 V typ. referred to VS) |
| CPUVTH = 1 | $V_{CPUV2}$ (6.5 V typ. referred to VS) | $V_{CPUV4}$ (8 V typ. referred to VS) |

If VCP falls below the configured charge pump undervoltage threshold while **CPEN** = 1:

- If one of the MOSFET is on, then all MOSFETs are actively turned off with their configured static discharge current during their respective tHBxCCP active.
- Then the gate drivers are turned off .
- **CP_UV** is set and latched.

The **CP_UV** is reset and the normal operation is resumed once **SUP_STAT** is cleared and VCP > VCPUV.

The charge pump undervoltage detection is blanked ($t_{CPUVBLANK}$) during each new activation of the charge pump[1)].

### 13.11.1.5 Switching parameters of MOSFETs in PWM mode

The effective switching parameters of the active MOSFETs (**EN_GEN_CHECK**=1), respectively PWM MOSFET (**EN_GEN_CHECK**=0)can be read out with dedicated status registers:

- The turn-on and turn off delays, noted tDON and tDOFF are reported by the status register **EFF_TDON_OFF1**, **EFF_TDON_OFF2**, **EFF_TDON_OFF3**, **EFF_TDON_OFF4**.
- The rise and fall times, noted tRISE and tFALL, are reported by the status register **TRISE_FALL1**, **TRISE_FALL2**, **TRISE_FALL3**, **TRISE_FALL4**.

Refer to **Chapter 12.3** for the definition of tDON, tDOFF, tRISE and tFALL for high-side PWM and low-side PWM operations.

1) Including **CPEN** set to 1, recovery from VS under/overvoltage, VSINT overvoltage and CP_ OT

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### 13.11.2 Low-side drain-source voltage monitoring during braking

The low-side MOSFETs are turned-on while the charge pump is deactivated in the following conditions:

- The slam mode is activated and PWM1/CRC is High.
- The parking braking mode is activated and the device is in Sleep Mode or Stop Mode.
- VS overvoltage brake is activated and (VS > VS Overvoltage braking or VSINT > VSINT Overvoltage braking) in all device modes if **OV_BRK_EN** is set.

Under these conditions, the drain-source voltage of the low-sides are monitored and the applied drain-source overvoltage thresholds are according to **VDSTH_BRK**.

The applied blank time, which starts at the beginning of the brake activation, is:

- $t_{BLK_BRAKE1}$ if **TBLK_BRK** = 0
- $t_{BLK_BRAKE2}$ if **TBLK_BRK** = 1

During the blank time, a drain-source overvoltage of the low-sides is masked.

The applied filter time is $t_{FVDS_BRAKE}$.

If a drain-source overvoltage is detected during braking , then all low-side MOSFETs are turned off (latched) within $t_{OFF_BRAKE}$. SLAM_LSx_DIS (**BRAKE**, **SLAM**, **PARK_BRK_EN**, **OV_BRK_EN** are unchanged. The corresponding status bit LSxDSOV_BRK is set in **DSOV**.

The low-sides can be reactivated only if all LSxDSOV_BRK bits (**DSOV**) are cleared (even in slam mode with the respective LSx disabled by the SLAM_LSx_DIS bit).

If any of the status bits LSxDSOV_BRK is set, then the charge pump stays off (**CPEN**=1 command is accepted but the charge pump stays disabled until all LSxDSOV_BRK are cleared).

### 13.11.3 VS or VSINT Overvoltage braking

The VS and VSINT overvoltage braking is activated if the **OV_BRK_EN** bit in **BRAKE** register is set regardless of the device mode.

If VS, respectively VSINT, exceeds $V_{OVBR,cfgx,r}$ (x = 0 to 7), then all low-sides MOSFETs are turned-on within $t_{ON_BRAKE}$. The status bits **VSOVBRAKE_ST**, respectively **VSINTOVBRAKE_ST**, is set and latched (see **DSOV** register).

If VS and VSINT decrease below $V_{OVBR,cfgx,r}$ - $V_{HYS,cfgx}$ (x = 0 to 7), then all low-sides MOSFETs are turned-off within $t_{OFF_BRAKE}$ after the filter time $t_{OV_BR_FILT}$.

If (VSHx - VSL) exceeds the configured threshold, then all low-sides MOSFETs are turned-off within $t_{OFF_BRAKE}$ after the filter time $t_{FVDS_BRAKE}$. The threshold is:

- $V_{VDSMONTH0_BRAKE}$ if **VDSTH_BRK** = 0
- $V_{VDSMONTH1_BRAKE}$ if **VDSTH_BRK** = 1

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## 13.12 Electrical Characteristics

**Table 32 Electrical Characteristics**

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **VCC1 Monitoring; VCC1 = 5.0V Version** | | | | | | | |
| Undervoltage Prewarning Threshold Voltage PW,f | $V_{PW,f}$ | 4.53 | 4.70 | 4.84 | V | VCC1 falling, SPI bit is set | P_13.12.1 |
| Undervoltage Prewarning Threshold Voltage PW,r | $V_{PW,r}$ | 4.60 | 4.75 | 4.90 | V | VCC1 rising | P_13.12.2 |
| Undervoltage Prewarning Threshold Voltage hysteresis | $V_{PW,hys}$ | 30 | 50 | 90 | mV | 4) | P_13.12.3 |
| VCC1 UV Prewarning Detection Filter Time | $t_{VCC1,PW_F}$ | 5 | 10 | 14 | us | 2) rising and falling | P_13.12.4 |
| Reset Threshold Voltage RT1,f | $V_{RT1,f}$ | 4.45 | 4.6 | 4.75 | V | default setting; VCC1 falling | P_13.12.5 |
| Reset Threshold Voltage RT1,r | $V_{RT1,r}$ | 4.58 | 4.74 | 4.90 | V | default setting; VCC1 rising | P_13.12.6 |
| Reset Threshold Voltage RT2,f | $V_{RT2,f}$ | 3.70 | 3.85 | 4.00 | V | VCC1 falling | P_13.12.7 |
| Reset Threshold Voltage RT2,r | $V_{RT2,r}$ | 3.85 | 4.0 | 4.15 | V | VCC1 rising | P_13.12.8 |
| Reset Threshold Voltage RT3,f | $V_{RT3,f}$ | 3.24 | 3.40 | 3.55 | V | VS ≥ 4 V; VCC1 falling | P_13.12.9 |
| Reset Threshold Voltage RT3,r | $V_{RT3,r}$ | 3.39 | 3.54 | 3.70 | V | VS ≥ 4 V; VCC1 rising | P_13.12.10 |
| Reset Threshold Voltage RT4,f | $V_{RT4,f}$ | 2.49 | 2.65 | 2.8 | V | VS ≥ 4 V; VCC1 falling | P_13.12.11 |
| Reset Threshold Voltage RT4,r | $V_{RT4,r}$ | 2.65 | 2.76 | 2.95 | V | VS ≥ 4 V; VCC1 rising | P_13.12.12 |
| Reset Threshold Hysteresis | $V_{RT,hys}$ | 70 | 140 | 220 | mV | 4) | P_13.12.13 |
| VCC1 Over Voltage Detection Threshold Voltage | $V_{CC1,OV,r}$ | 5.5 | 5.65 | 5.8 | V | 1)4) rising VCC1 | P_13.12.26 |
| VCC1 Over Voltage Detection Threshold Voltage | $V_{CC1,OV,f}$ | 5.4 | 5.55 | 5.7 | V | 4) falling VCC1 | P_13.12.27 |
| VCC1 OV Detection Filter Time | $t_{VCC1,OV_F}$ | 51 | 64 | 80 | us | 2) | P_13.12.31 |

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**Table 32 Electrical Characteristics** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| VCC1 Short to GND Filter Time | $t_{VCC1,SC}$ | 3.2 | 4 | 4.8 | ms | 2) blanking time during power-up, short circuit detection for VS ≥ VS,UV | P_13.12.32 |
| **Reset Generator; Pin RSTN** | | | | | | | |
| Reset Low Output Voltage | $V_{RSTN,L}$ | – | 0.2 | 0.4 | V | $I_{RSTN}$ = 1 mA for $V_{CC1}$ ≥ 1 V & $V_S \geq V_{POR,f}$ | P_13.12.33 |
| Reset High Output Voltage | $V_{RSTN,H}$ | 0.8 x $V_{CC1}$ | – | $V_{CC1}$ + 0.3 V | V | $I_{RSTN}$ = -20 µA | P_13.12.34 |
| Reset Pull-up Resistor | $R_{RSTN}$ | 10 | 20 | 40 | kΩ | $V_{RSTN}$ = 0 V | P_13.12.35 |
| Reset Filter Time | $t_{RF}$ | 4 | 10 | 26 | µs | 2) $V_{CC1} < V_{RT1x}$ to RSTN = L see also **Chapter 13.3** | P_13.12.36 |
| Reset Delay Time 1 | $t_{RD1}$ | 8 | 10 | 12 | ms | 2) **RSTN_DEL** = 0 | P_13.12.37 |
| Reset Delay Time 2 | $t_{RD2}$ | 1.6 | 2 | 2.4 | ms | 2) **RSTN_DEL** = 1 | P_13.12.64 |
| **VCAN Monitoring** | | | | | | | |
| CAN Supply undervoltage detection threshold (falling) | $V_{CAN_UV,f}$ | 4.5 | – | 4.75 | V | VCAN falling | P_13.12.38 |
| CAN Supply undervoltage detection threshold (rising) | $V_{CAN_UV,r}$ | 4.6 | – | 4.85 | V | VCAN rising | P_13.12.39 |
| $V_{CAN}$ Undervoltage detection hysteresis | $V_{CAN,UV,\ hys}$ | 50 | 90 | 130 | mV | 4) | P_13.12.40 |
| VCAN UV detection Filter Time | $t_{VCAN,UV_F}$ | 5 | 10 | 14 | µs | 2) VCAN rising and falling | P_13.12.41 |
| **Watchdog Generator / Internal Oscillator** | | | | | | | |
| Long Open Window | $t_{LW}$ | 160 | 200 | 240 | ms | 2) | P_13.12.42 |
| Internal Clock Generator Frequency | $f_{CLKSBC,1}$ | 0.8 | 1.0 | 1.2 | MHz | – | P_13.12.43 |
| **Minimum Waiting time during Fail-Safe Mode** | | | | | | | |
| Min. waiting time Fail-Safe | $t_{FS,min}$ | 80 | 100 | 120 | ms | 2)3) | P_13.12.45 |
| **Power-on Reset, Over / Undervoltage Protection** | | | | | | | |
| VSINT Power on reset rising | $V_{POR,r}$ | – | – | 4.5 | V | VSINT increasing | P_13.12.46 |
| VSINT Power on reset falling | $V_{POR,f}$ | – | – | 3 | V | VSINT decreasing | P_13.12.47 |

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**Table 32 Electrical Characteristics** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| VSINT Undervoltage Detection Threshold | $V_{SINT,UV}$ | 5.3 | – | 6.0 | V | Supply UV threshold for VCC1 SC detection; hysteresis included; includes rising and falling threshold | P_13.12.48 |
| VSHS Overvoltage Detection Threshold | $V_{SHS,OVD}$ | 20 | – | 22 | V | Supply OV supervision for HSx, LIN; hysteresis included | P_13.12.55 |
| VSHS Overvoltage Detection hysteresis | $V_{SHS,OVD,hys}$ | 100 | 500 | – | mV | 4) | P_13.12.56 |
| VSHS Undervoltage Detection Threshold | $V_{SHS,UVD}$ | 4.8 | – | 5.5 | V | Supply UV supervision for HSx, LIN; hysteresis included | P_13.12.57 |
| VSHS Undervoltage Detection hysteresis | $V_{SHS,UVD,hys}$ | 50 | 200 | 350 | mV | 4) | P_13.12.58 |
| VSHS Undervoltage Detection Filter Time | $t_{VSHS,UV}$ | 5 | 10 | 14 | us | 2) rising and falling | P_13.12.300 |
| VSHS Overvoltage Detection Filter Time | $t_{VSHS,OV}$ | 5 | 10 | 14 | us | 2) rising and falling | P_13.12.301 |
| **Charge Pump Undervoltage** | | | | | | | |
| Charge Pump Undervoltage Referred to VS | $V_{CPUV1}$ | 5.4 | 5.9 | 6.4 | V | **FET_LVL** = 0 **CPUVTH** = 0 falling threshold, VS ≥6 V | P_13.12.59 |
| Charge Pump Undervoltage Referred to VS | $V_{CPUV2}$ | 5.85 | 6.35 | 6.85 | V | **FET_LVL** = 0 **CPUVTH** = 1 falling threshold, VS ≥ 6 V | P_13.12.60 |
| Charge Pump Undervoltage Referred to VS | $V_{CPUV3}$ | 6.85 | 7.35 | 7.85 | V | **FET_LVL** = 1 **CPUVTH** = 0 falling threshold, VS ≥ 6 V | P_13.12.61 |

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**Table 32 Electrical Characteristics** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Charge Pump Undervoltage Referred to VS | $V_{CPUV4}$ | 7.5 | 8 | 8.5 | V | **FET_LVL** = 1 **CPUVTH** = 1 falling threshold, VS ≥ 6 V | P_13.12.62 |
| Charge Pump Undervoltage Filter Time | $t_{CPUV}$ | 51 | 64 | 80 | µs | 4) VS ≥ 6 V | P_13.12.63 |
| Charge Pump Undervoltage Blank Time | $t_{CPUVBLANK}$ | 400 | 500 | 600 | µs | 4) VS ≥ 6 V | P_13.12.175 |
| **VS monitoring** | | | | | | | |
| VS undervoltage threshold | $V_{S,UV}$ | 4.7 | – | 5.4 | V | hysteresis included | P_13.12.66 |
| VS overvoltage threshold detection 1 | $V_{S,OVD1}$ | 19 | – | 22.5 | V | hysteresis included, **VS_OV_SEL** = 0 | P_13.12.68 |
| VS overvoltage threshold detection 2 | $V_{S,OVD2}$ | 27.75 | – | 31.25 | V | hysteresis included, **VS_OV_SEL** = 1 | P_13.12.65 |
| VS undervoltage filter time | $t_{VSUV_FILT}$ | 5 | 10 | 14 | µs | 2) rising and falling | P_13.12.71 |
| VS overvoltage filter time | $t_{VSOV_FILT}$ | 5 | 10 | 14 | µs | 2) rising and falling | P_13.12.72 |
| **Off-state open load diagnosis** | | | | | | | |
| Pull-up diagnosis current | $I_{PUDiag}$ | -600 | -400 | -270 | µA | VS ≥ 6 V | P_13.12.73 |
| Pull-down diagnosis current | $I_{PDDiag}$ | 1600 | 2200 | 2800 | µA | VS ≥ 6 V | P_13.12.74 |
| Diagnosis current ratio | $I_{Diag_ratio}$ | 4.25 | 5.25 | 6.25 | | Ratio $I_{PDDiag}$ / $I_{PUDiag}$ | P_13.12.302 |
| **Drain-source monitoring CP activated** | | | | | | | |
| Blank time | $t_{BLANK}$ | typ-20% | 587 +266 xTBLK | typ+20 % | ns | 4) TBLK: decimal value of TBLK[3:0], VS ≥ 6 V | P_13.12.75 |
| Cross-current protection time | $t_{CCP}$ | typ-20% | 587 +266 xTCCP | typ+20 % | ns | 4) TCCP: decimal value of TCCPx[3:0], VS ≥ 6 V | P_13.12.76 |
| HS/LS Drain-source overvoltage 0 | $V_{VDSMONTH0_CPON}$ | 0.115 | 0.16 | 0.195 | V | VDSTH[2:0] = $000_B$, VS≥6 V, TFVDS=$00_B$ | P_13.12.77 |
| HS/LS Drain-source overvoltage 1 | $V_{VDSMONTH1_CPON}$ | 0.16 | 0.2 | 0.25 | V | VDSTH[2:0] = $001_B$, VS≥6 V, TFVDS=$00_B$ | P_13.12.78 |
| HS/LS Drain-source overvoltage 2 | $V_{VDSMONTH2_CPON}$ | 0.24 | 0.3 | 0.36 | V | VDSTH[2:0] = $010_B$, VS≥6 V, TFVDS=$00_B$ | P_13.12.79 |

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**Table 32 Electrical Characteristics** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| HS/LS Drain-source overvoltage 3 | $V_{VDSMONTH3_CPON}$ | 0.32 | 0.4 | 0.48 | V | VDSTH[2:0] = $011_B$, VS≥6 V, TFVDS=$00_B$ | P_13.12.80 |
| HS/LS Drain-source overvoltage 4 | $V_{VDSMONTH4_CPON}$ | 0.4 | 0.5 | 0.6 | V | VDSTH[2:0] = $100_B$, VS≥6 V, TFVDS=$00_B$ | P_13.12.81 |
| HS/LS Drain-source overvoltage 5 | $V_{VDSMONTH5_CPON}$ | 0.48 | 0.6 | 0.72 | V | VDSTH[2:0] = $101_B$, VS≥6 V, TFVDS=$00_B$ | P_13.12.82 |
| HS/LS Drain-source overvoltage 6 | $V_{VDSMONTH6_CPON}$ | 0.64 | 0.8 | 0.96 | V | VDSTH[2:0] = $110_B$, VS≥6 V, TFVDS=$00_B$ | P_13.12.83 |
| HS/LS Drain-source overvoltage 7 | $V_{VDSMONTH7_CPON}$ | 1.75 | 2.0 | 2.25 | V | VDSTH[2:0] = $111_B$, VS≥6 V, TFVDS=$00_B$ | P_13.12.84 |
| **Drain-Source monitoring - Slam mode, parking braking and VS overvoltage braking, VS or VSINT ≥ 8V** | | | | | | | |
| Blank time | $t_{BLK_BRAKE1}$ | 4.5 | 7 | 9.5 | µs | **TBLK_BRK** = 0, VS or VSINT ≥ 8 V | P_13.12.85 |
| Blank time | $t_{BLK_BRAKE2}$ | 9 | 11 | 13 | µs | **TBLK_BRK** = 1, VS or VSINT ≥ 8 V | P_13.12.86 |
| VDS Filter time | $t_{FVDS_BRAKE}$ | 0.5 | 1 | 2.5 | µs | VS or VSINT ≥ 8 V | P_13.12.87 |
| LS Drain-source monitoring thresholds | $V_{VDSMONTH0_BRAKE}$ | 0.56 | 0.8 | 1.05 | V | VS or VSINT ≥ 8 V **VDSTH_BRK** = 0 | P_13.12.89 |
| LS Drain-source monitoring thresholds | $V_{VDSMONTH1_BRAKE}$ | 0.15 | 0.22 | 0.29 | V | VS or VSINT ≥ 8 V **VDSTH_BRK** = 1 | P_13.12.90 |
| **VS Overvoltage Braking Mode** | | | | | | | |
| VS Overvoltage braking config 0 rising | $V_{OVBR,cfg0,r}$ | 25.65 | 27 | 28.35 | V | **OV_BRK_TH**=$000_B$ | P_13.12.97 |
| VS Overvoltage braking config 1 rising | $V_{OVBR,cfg1,r}$ | 26.60 | 28 | 29.40 | V | **OV_BRK_TH**=$001_B$ | P_13.12.98 |
| VS Overvoltage braking config 2 rising | $V_{OVBR,cfg2,r}$ | 27.55 | 29 | 30.45 | V | **OV_BRK_TH**=$010_B$ | P_13.12.99 |
| VS Overvoltage braking config 3 rising | $V_{OVBR,cfg3,r}$ | 28.50 | 30 | 31.50 | V | **OV_BRK_TH**=$011_B$ | P_13.12.100 |
| VS Overvoltage braking config 4 rising | $V_{OVBR,cfg4,r}$ | 29.45 | 31 | 32.55 | V | **OV_BRK_TH**=$100_B$ | P_13.12.101 |
| VS Overvoltage braking config 5 rising | $V_{OVBR,cfg5,r}$ | 30.40 | 32 | 33.60 | V | **OV_BRK_TH**=$101_B$ | P_13.12.102 |
| VS Overvoltage braking config 6 rising | $V_{OVBR,cfg6,r}$ | 31.35 | 33 | 34.65 | V | **OV_BRK_TH**=$110_B$ | P_13.12.103 |
| VS Overvoltage braking config 7 rising | $V_{OVBR,cfg7,r}$ | 32.30 | 34 | 35.70 | V | **OV_BRK_TH**=$111_B$ | P_13.12.104 |
| VS Overvoltage braking config 0 | $V_{HYS,cfg0}$ | 0.64 | 0.75 | 0.85 | V | **OV_BRK_TH**=$000_B$ | P_13.12.105 |

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**Table 32 Electrical Characteristics** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V; $T_j$ = -40°C to +150°C; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| VS Overvoltage braking config 1 | $V_{HYS,cfg1}$ | 0.74 | 0.82 | 0.9 | V | **OV_BRK_TH**=$001_B$ | P_13.12.109 |
| VS Overvoltage braking config 2 | $V_{HYS,cfg2}$ | 0.80 | 0.89 | 0.98 | V | **OV_BRK_TH**=$010_B$ | P_13.12.113 |
| VS Overvoltage braking config 3 | $V_{HYS,cfg3}$ | 0.85 | 0.95 | 1.05 | V | **OV_BRK_TH**=$011_B$ | P_13.12.117 |
| VS Overvoltage braking config 4 | $V_{HYS,cfg4}$ | 0.93 | 1.03 | 1.13 | V | **OV_BRK_TH**=$100_B$ | P_13.12.121 |
| VS Overvoltage braking config 5 | $V_{HYS,cfg5}$ | 0.97 | 1.08 | 1.19 | V | **OV_BRK_TH**=$101_B$ | P_13.12.125 |
| VS Overvoltage braking config 6 | $V_{HYS,cfg6}$ | 1.03 | 1.15 | 1.27 | V | **OV_BRK_TH**=$110_B$ | P_13.12.129 |
| VS Overvoltage braking config 7 | $V_{HYS,cfg7}$ | 1.1 | 1.23 | 1.36 | V | **OV_BRK_TH**=$111_B$ | P_13.12.133 |
| VS and VSINT overvoltage braking filter time | $t_{OV_BR_FILT}$ | 10 | 15 | 20 | µs | 4) | P_13.12.200 |
| **Overtemperature Shutdown**[4] | | | | | | | |
| Thermal Prewarning Temperature | $T_{jPW}$ | 125 | 145 | 165 | °C | $T_j$ rising | P_13.12.169 |
| Thermal Shutdown TSD1 | $T_{jTSD1}$ | 170 | 185 | 200 | °C | $T_j$ rising | P_13.12.170 |
| Thermal Shutdown TSD2 | $T_{jTSD2}$ | 170 | 185 | 200 | °C | $T_j$ rising | P_13.12.171 |
| Thermal Shutdown hysteresis | $T_{jTSD,hys}$ | – | 25 | – | °C | 4) | P_13.12.172 |
| TSD/TPW Filter Time | $t_{TSD_TPW_F}$ | 5 | 10 | 15 | us | rising and falling, applies to all thermal sensors (TPW, TSD1, TSD2) | P_13.12.173 |
| Deactivation time after thermal shutdown TSD2 | $t_{TSD2}$ | 0.8 | 1 | 1.2 | s | 2) | P_13.12.174 |

1) It is ensured that the threshold $V_{CC1,OV,r}$ is always higher than the highest regulated $V_{CC1}$ output voltage $V_{CC1,out4}$.
.
2) Not subject to production test, tolerance defined by internal oscillator tolerance.
3) This time applies for all failure entries except a device thermal shutdown (TSD2 has a typ. 1 s waiting time $t_{TSD2}$).
4) Not subject to production test, specified by design.

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# 14 Serial Peripheral Interface

The Serial Peripheral Interface is the communication link between the device and the microcontroller.
The TLE9562QX is supporting multi-slave operation in full-duplex mode with 32-bit data access.

The SPI behavior for the different device modes is as follows:

- The SPI is enabled in Init Mode, Normal Mode and Stop Mode.
- The SPI is OFF in Sleep Mode, Restart Mode and Fail-Safe Mode.

## 14.1 SPI Block Description

The Control Input Word is read via the data input SDI, which is synchronized with the clock input CLK provided by the microcontroller. The output word appears synchronously at the data output SDO (see **Figure 84** with a 32-bit data access example).
The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), LOW active. After the CSN input returns from LOW to HIGH, the word that has been read is interpreted according to the content. The SDO output switches to tristate status (high impedance) at this point, thereby releasing the SDO bus for other use.The state of SDI is shifted into the input register with every falling edge on CLK. The state of SDO is shifted out of the output register after every rising edge on CLK. The SPI of the device is not daisy chain capable.

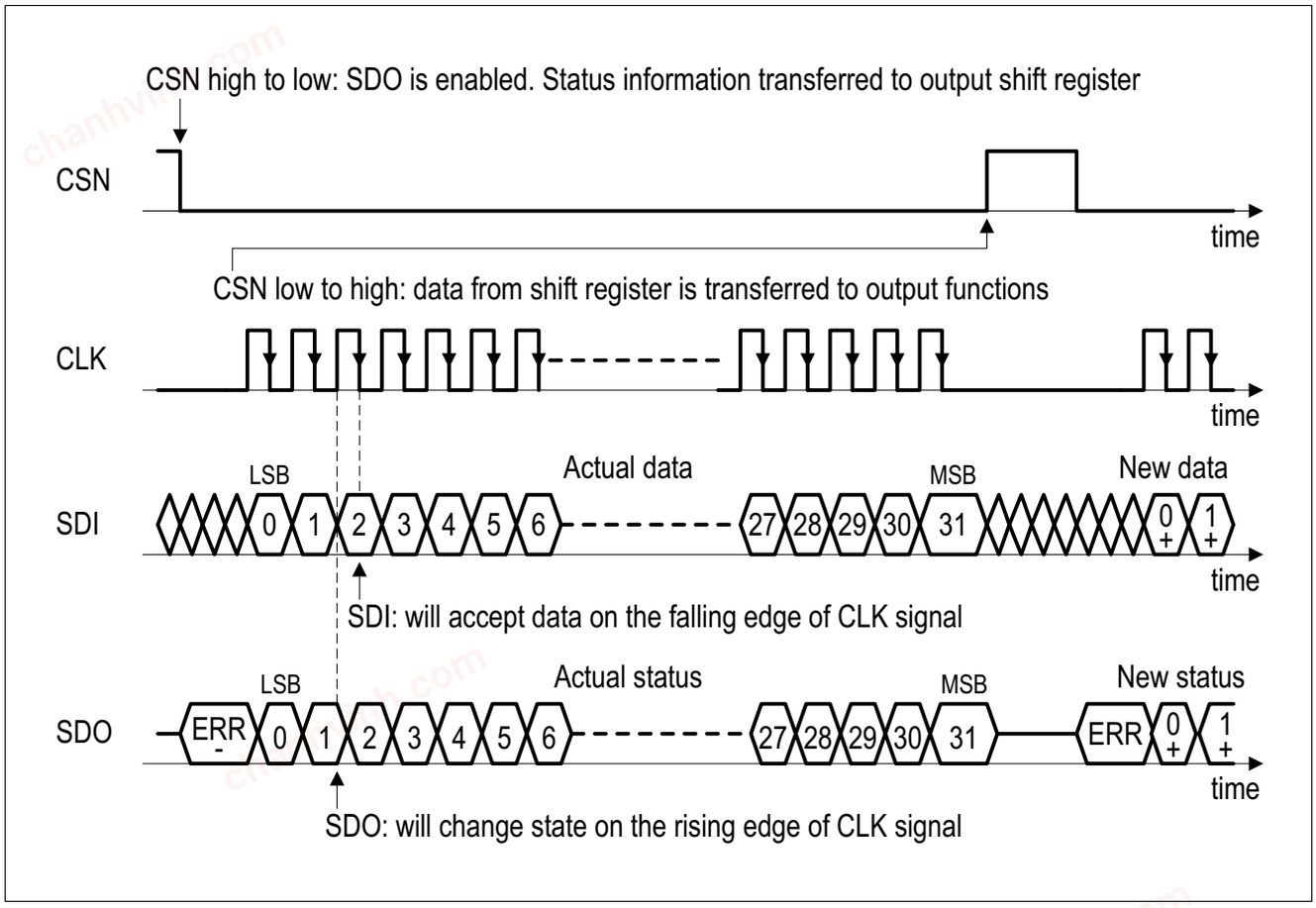



**Figure 84 SPI Data Transfer Timing (note the reversed order of LSB and MSB shown in this figure compared to the register description)**

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## 14.2 Failure Signalization in the SPI Data Output

When the microcontroller sends a wrong SPI command to the device, the device ignores the information. Wrong SPI commands are either invalid device mode commands or commands which are prohibited by the state machine to avoid undesired device or system states (see below). In this case the diagnosis bit **SPI_FAIL** is set and the SPI Write command is ignored (no partial interpretation). This bit can be only reset by actively clearing it via a SPI command.

**Invalid SPI Commands leading to SPI_FAIL are listed below (in this case the SPI command is ignored):**

- Illegal state transitions:
  - Going from Stop Mode to Sleep Mode. In this case the device enters Restart Mode.
  - Trying to go to Stop Mode or Sleep Mode from Init Mode[1)]. In this case Normal Mode is entered.
- Uneven parity in the data bit of the **WD_CTRL** register. In this case the watchdog trigger is ignored and/or the new watchdog settings are ignored respectively.
- In Stop Mode: attempting to change any SPI settings, e.g. changing the watchdog configuration, PWM settings and HSx configuration settings during Stop Mode, etc.;
  the SPI command is ignored in this case;
  only WD trigger, returning to Normal Mode, triggering a device soft reset, and read & clear status registers commands are valid SPI commands in Stop Mode; **Note:** No failure handling is done for the attempt to go to Stop Mode when all bits in the registers **BUS_CTRL** and **WK_CTRL** are cleared because the microcontroller can leave this mode via SPI.
- When entering Stop Mode and **WK_STAT** is not cleared; **SPI_FAIL** will not be set but the INTN pin will be triggered.
- Changing from Stop Mode to Normal Mode and changing the other bits of the **M_S_CTRL** register. The other modifications will be ignored.
- Sleep Mode: attempt to go to Sleep Mode without any wake source set, i.e. when all bits in the **BUS_CTRL** and **WK_CTRL** registers are cleared. In this case the **SPI_FAIL** bit is set and the device enters Restart Mode. Even though the Sleep Mode command is not entered in this case, the rest of the command is executed but restart values apply during Restart Mode; **Note:** At least one wake source must be activated in order to avoid a deadlock situation in Sleep Mode.
  If the only wake source is a timer and the timer is OFF, then the device will wake immediately from Sleep Mode and enter Restart Mode.
- Setting a longer or equal on-time than the timer period of the respective timer.
- SDI stuck at HIGH or LOW, e.g. SDI received all ‘0’ or all ‘1’.
- Any attempt to configure again the **WK2_FO**.
- Configured the HSx controlled by SYNC when the WK4/SYNC is not configured as SYNC-input.

*Note: There is no SPI fail information for unused addresses.*

*Note: In case that the register or banking are accessed but they are not valid as address or banks, the **SPI_FAIL** is not triggered and the cmd is ignored.*

1) If the device is externally configured to use SPI with CRC (by PWM1/CRC pin), the attempt to go to Stop or Sleep from Init , will generate SPI_FAIL even if it is a SPI command with correct CRC. Still, the first SPI command will put the device from Init to Normal Mode even if CRC is not correct (CRC_FAIL status bit will be set).

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**Signalization of the ERR Flag (high active) in the SPI Data Output (see Figure 84):**

The ERR flag presents an additional diagnosis possibility for the SPI communication. The ERR flag is being set for following conditions:

- in case the number of received SPI clocks is not 0 or 32.
- in case RSTN is LOW and SPI frames are being sent at the same time.

*Note: In order to read the SPI ERR flag properly, CLK must be low when CSN is triggered, i.e. the ERR bit is not valid if the CLK is high on a falling edge of CSN.*

**The number of received SPI clocks is not 0 or 32:**

The number of received input clocks is supervised to be 0 or 32 clock cycles and the input word is discarded in case of a mismatch (0 clock cycle to enable ERR signalization). The error logic also recognizes if CLK was high during CSN edges. Both errors ( 0 or 32 bit CLK mismatch or CLK high during CSN edges ) are flagged in the following SPI output by a “HIGH” at the data output (SDO pin, bit ERR) before the first rising edge of the clock is received. The complete SPI command is ignored in this case.

**RSTN is LOW and SPI frames are being sent at the same time:**

The ERR flag will be set when the RSTN pin is triggered (during device restart) and SPI frames are being sent to the device at the same time. The behavior of the ERR flag will be signalized at the next SPI command for below conditions:

- If the command begins when RSTN is HIGH and it ends when RSTN is LOW.
- If a SPI command will be sent while RSTN is LOW.
- If a SPI command begins when RSTN is LOW and it ends when RSTN is HIGH.

And the SDO output will behave as follows:

- Always when RSTN is LOW then SDO will be HIGH.
- When a SPI command begins when RSTN is LOW and ends when RSTN is HIGH, then the SDO should be ignored because wrong data will be sent.

*Note: It is possible to quickly check for the ERR flag without sending any data bits. i.e. only the CSN is pulled low and SDO is observed - no SPI Clocks are sent in this case.*

*Note: The ERR flag could also be set after the device has entered Fail-Safe Mode because the SPI communication is stopped immediately.*

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## 14.3 SPI Programming

For the TLE9562QX, 7 bits are used for the address selection (BIT 6...0). Bit 7 is used to decide between Read Only and Read & Clear for the status bits, and between Write and Read Only for configuration bits. For the actual configuration and status information, 16 data bits (BIT 23...8) are used.

Writing, clearing and reading is done word wise. The SPI status bits are not cleared automatically and must be cleared by the microcontroller. Some of the configuration bits will automatically be cleared by the device (refer to the respective register descriptions for detailed information). In Restart Mode, the device ignores all SPI communication, i.e. it does not interpret it.

There are two types of SPI registers:

- Control registers: These registers are used to configure the device, e.g. mode, watchdog trigger, etc.
- Status registers: These registers indicate the status of the device, e.g. wake events, warnings, failures, etc.

For the status registers, the requested information is given in the same SPI command in the data out (SDO). For the control registers, the status of each byte is shown in the same SPI command as well. However, configuration changes of the same register are only shown in the next SPI command (configuration changes inside the device become valid only after CSN changes from low to high). See **Figure 85**.

Writing of control registers is possible in Init and Normal Mode. During Stop Mode only the change to Normal Mode and triggering the watchdog is allowed as well as reading and clearing the status registers.

No status information can be lost, even if a bit changes right after the first 7 SPI clock cycles before the SPI frame ends. In this case the status information field will be updated with the next SPI command. However, the flag is already set in the relevant status register.The device status information from the SPI status registers is transmitted in a compressed format with each SPI response on SDO in the so-called Status Information Field register (see also **Table 33**). The purpose of this register is to quickly signal changes in dedicated SPI status registers to the microcontroller.

**Table 33 Status Information Field**

| Bit in Status Information Field | Corresponding Address Bit | Status Register Description |
|---|---|---|
| 0 | | SUPPLY_STAT = OR of all bits on SUP_STAT register |
| 1 | | TEMP_STAT = OR of all bits on THERM_STAT register |
| 2 | | BUS_STAT= OR of all bits on BUS_STAT register |
| 3 | | WAKE_UP = OR of all bits on WK_STAT register |
| 4 | | HS_STAT = OR of all bits on HS_OL_OC_OT_STAT register |
| 5 | | DEV_STAT = OR of all bits on DEV_STAT except CRC_STAT and SW_DEV |
| 6 | | BD_STAT = OR of all bits on DSOV register |
| 7 | | SPI_CRC_FAIL = (SPI_FAIL) OR (CRC_FAIL) |

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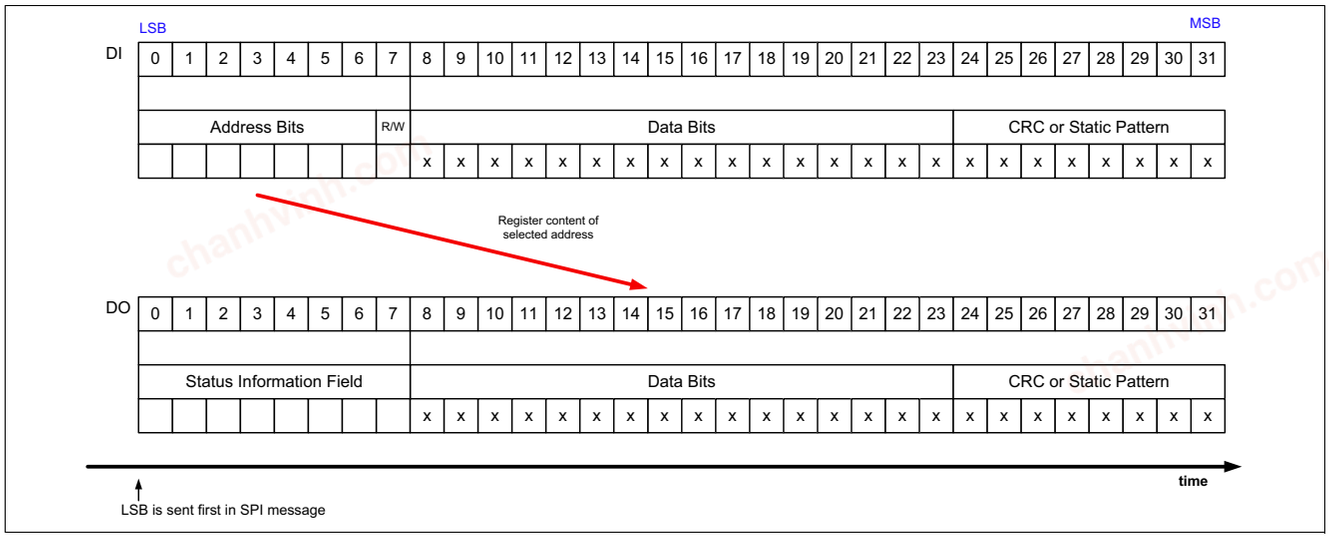



**Figure 85 SPI Operation Mode**

### 14.3.1 CRC

The SPI interface includes also 8 Bits (bits 24 to 31) used for Cyclic Redundancy Check (CRC) to ensure data integrity on sent or received SPI command.

The implemented CRC is based on Autosar specification of CRC Routines revision 4.3.0 and in particular the function CRC8-2FH.

The specification are based on the follow table:

**Table 34 CRC8x2FH definition**

| | |
|---|---|
| CRC result width: | 8 bits |
| Polynomial | $2F_H$ |
| Initial Value | $FF_H$ |
| Input data reflected | No |
| Result data reflected | No |
| XOR value | $FF_H$ |
| Check | $DF_H$ |
| Magic check | $42_H$ |

Some examples of CRC calculation are shown in the follow table:

**Table 35 CRC8x2FH calculation example**

| Data Bytes (hexadecimal) | | | | | | | | | CRC |
|---|---|---|---|---|---|---|---|---|---|
| 00 | 00 | 00 | 00 | | | | | | 12 |
| F2 | 01 | 83 | | | | | | | C2 |
| 0F | AA | 00 | 55 | | | | | | C6 |
| 00 | FF | 55 | 11 | | | | | | 77 |
| 33 | 22 | 55 | AA | BB | CC | DD | EE | FF | 11 |
| 92 | 6B | 55 | | | | | | | 33 |
| FF | FF | FF | FF | | | | | | 6C |

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### Polynominal

The polynomial is:

$$x^8 + x^5 + x^3 + x^2 + x^1 + x^0 \quad (14.1)$$

### Calculation in SDI and SDO

The calculation of the CRC is done considering the first 24 bits (BIT 0..23) either of SDI or SDO.

The content of SDO Payload (BIT 8..23) is referring the previous data written at the addressed register via SDI.

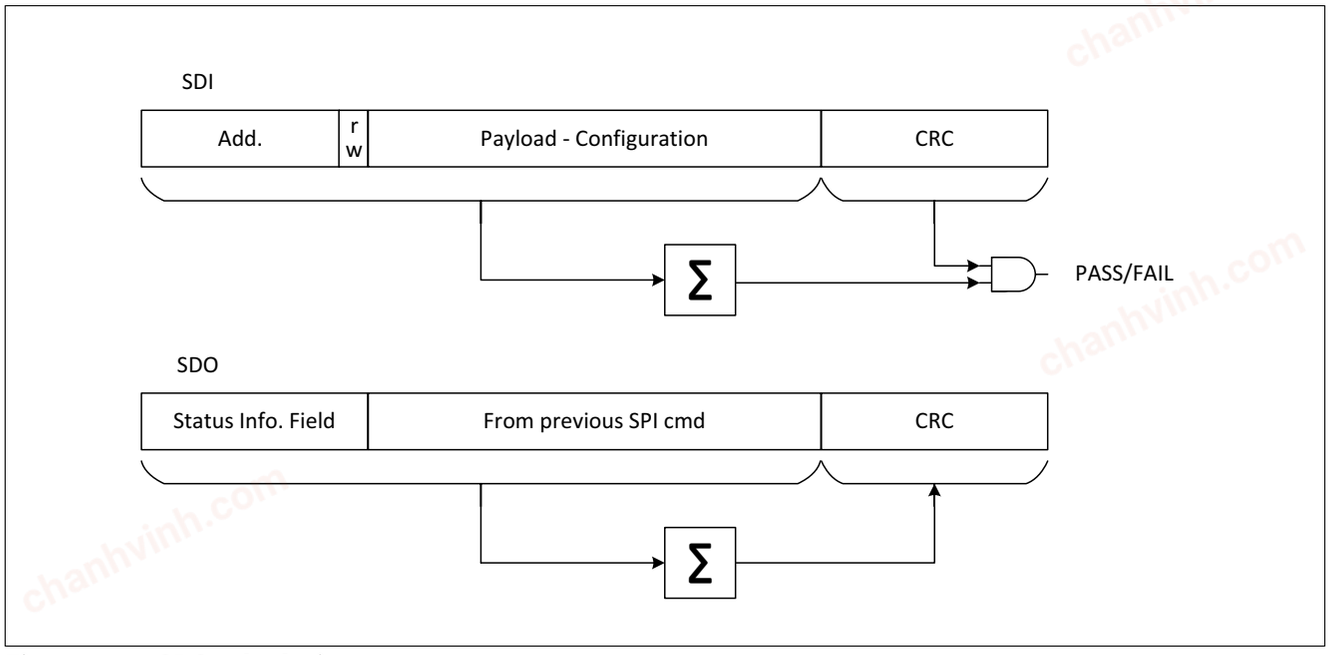



**Figure 86 CRC calculation**

### CRC Activation and status information

For CRC activation, refer to **Chapter 5.2**.

The CRC status (**CRC_STAT**)and failure (**CRC_FAIL**) are readable on **DEV_STAT**.

Read out of the register which contains the **CRC_STAT** and **CRC_FAIL** is done ignoring the CRC field and no failure flag are set.

The **DEV_STAT** register shall be cleared considering the CRC setting (ON or OFF).

The **CRC_STAT** bit is read only.

The **CRC_FAIL** is set in the follow conditions:

- If the CRC is enabled and the µC sends wrong CRC field.
- If the CRC is disabled and the µC sends wrong static pattern (no $A5_H$).

### CRC field in case of CRC disabled

In case that the CRC is not activated, the bits needed for CRC field have to be filled with static pattern.

In case of SDI, the CRC field has to be filled with $A5_H$ (bits 24:31).

In case of SDO, the device will always answer with $5A_H$ (bits 24:31).

The status of the CRC is updated accordingly in **CRC_STAT** bit.

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## 14.4 SPI Bit Mapping

The following figures show the mapping of the registers and the SPI bits of the respective registers.

The Control Registers are Read/Write Register with the following structure:

- Device Control Registers from 000 $0001_B$ to 000 $1011_B$.
- Bridge Driver Control Registers from 001 $0000_B$ to 001 $1101_B$.
- SWK Control Registers from 011 $0000_B$ to 011 $1111_B$.

Depending on bit 7 the bits are only read (setting bit 7 to '0') or also written (setting bit 7 to '1'). The new setting of the bit after a write can be seen with a new read / write command.

The Status Registers are Read/Clear with the following structure:

- Device Status Registers from 100 $0000_B$ to 100 $0110_B$.
- Bridge Driver Status Registers from 101 $0000_B$ to 101 $1011_B$.
- Product Family is 111 $0000_B$.

The registers can be read or can be cleared (if clearing is possible) depending on bit 7. To clear the payload of one of the Status Registers bit 7 must be set to 1.
The registers **WK_LVL_STAT**, and **FAM_PROD_STAT** are an exception as they show the actual voltage level at the respective WKx pin (LOW/HIGH), or a fixed family/ product ID respectively and can thus not be cleared.
It is recommended for proper diagnosis to clear respective status bits for wake events or failure.

When changing to a different device mode, certain configurations bits will be cleared automatically or modified:

- The device mode bits are updated to the actual status, e.g. when returning to Normal Mode.
- When changing to a low-power mode (Stop Mode or Sleep Mode), the diagnosis bits of the integrated module are not cleared.
- When changing to Stop Mode, the CAN, LIN control bits will not be modified.
- When changing to Sleep Mode, the CAN, LIN control bits will be modified if they were not OFF or wake capable before.
- FO will stay activated if it was triggered before. Depending on the respective configuration, CAN, LIN transceivers will be either OFF, woken or still wake capable.

*Note: The detailed behavior of the respective SPI bits and control functions is described in **Chapter 14.5**, **Chapter 14.6**.and in the respective module chapter. The bit type be marked as 'rwh' in case the device will modify respective control bits.*

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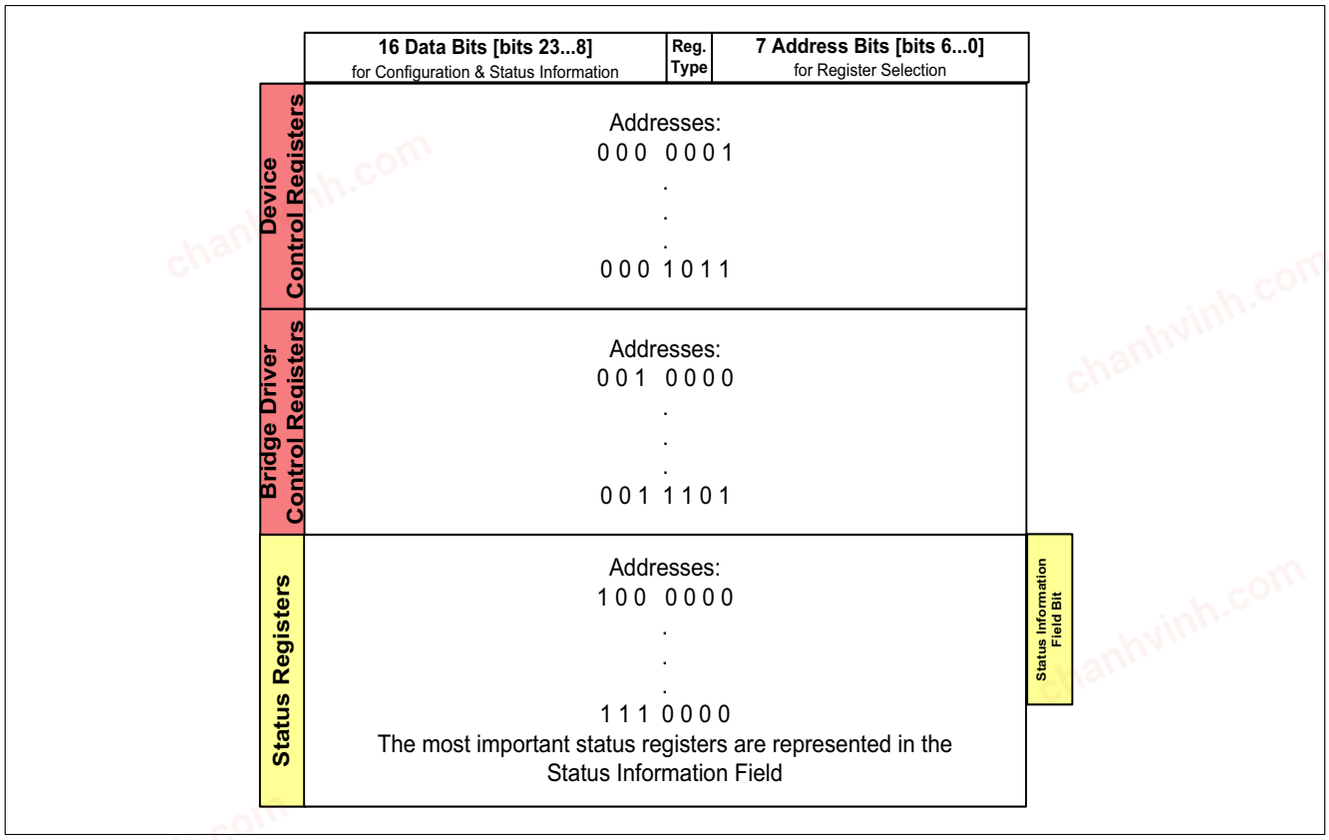



**Figure 87 SPI Register Mapping Structure**

The detailed register mappings for control registers and status registers are shown in **Table 36** and **Table 61** respectively.

### 14.4.1 Register Banking

In order to minimize the number of configuration registers, seven registers follow a bank structure.

The banked registers are:

- **WK_CTRL**
- **PWM_CTRL**
- **CCP_BLK**
- **TPRECHG**
- **HB_ICHG**
- **HB_PCHG_INIT**
- **TDON_HB_CTRL**
- **TDOFF_HB_CTRL**

In these register, the first 3 bits of the payload (bit 8 to 10) select the bank that has to be configured. The rest of the payload is used to configure the selected bank (for more details refer to the specific banked register).

In case that CRC is used, the CRC calculation is done considering the first 24 bits (from bit 0 to 23).

The banked registers can be read like the other configuration registers but in the SDO one ‘0’ is automatically added after the status information field. **Figure 88** shows the structure of SDO in banked register.

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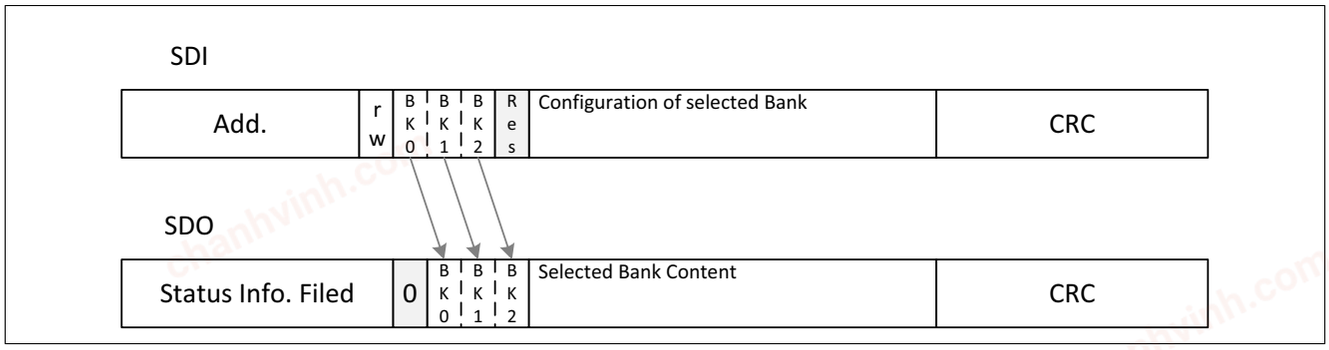



**Figure 88 Register read Out of banked register (3 bit banking)**

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## 14.5 SPI control registers

READ/WRITE Operation (see also **Chapter 14.3**):

- The ‘POR / Soft Reset Value’ defines the register content after POR or device reset.
- The ‘Restart Value’ defines the register content after device restart, where ‘x’ means the bit is unchanged.
- There are different bit types:
  - ‘r’ = READ: read only bits (or reserved bits).
  - ‘rw’ = READ/WRITE: readable and writable bits.
  - ‘rwh’ = READ/WRITE/Hardware: readable/writable bits, which can also be modified by the device hardware.
- Reserved bits are marked as “Reserved” and always read as “0”. The respective bits shall also be programmed as “0”.
- Reading a register is done word wise by setting the SPI bit 7 to “0” (= Read Only).
- SPI control bits are in general not cleared or changed automatically. This must be done by the microcontroller via SPI programming. Exceptions to this behavior are stated at the respective register description and the respective bit type is marked with a ‘h’ meaning that the device is able to change the register content.

The registers are addressed wordwise.

**Table 36 Register Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| **SPI control registers, Device Control Registers** | | | |
| **M_S_CTRL** | Mode and Supply Control | $0000001_B$ | **170** |
| **HW_CTRL** | Hardware Control | $0000010_B$ | **172** |
| **WD_CTRL** | Watchdog Control | $0000011_B$ | **174** |
| **BUS_CTRL** | CAN and LIN Control | $0000100_B$ | **176** |
| **WK_CTRL** | Wake-up Control | $0000101_B$ | **178** |
| **TIMER_CTRL** | Timer 1 and Timer 2 Control and Selection | $0000110_B$ | **180** |
| **SW_SD_CTRL** | High-Side Switch Shutdown Control | $0000111_B$ | **182** |
| **HS_CTRL** | High-Side Switch Control | $0001000_B$ | **185** |
| **INT_MASK** | Interrupt Mask Control | $0001001_B$ | **187** |
| **PWM_CTRL** | PWM Configuration Control | $0001010_B$ | **189** |
| **SYS_STAT_CTRL** | System Status Control | $0001011_B$ | **190** |
| **SPI control registers, Control registers bridge driver** | | | |
| **GENCTRL** | General Bridge Control | $0010000_B$ | **191** |
| **LS_VDS** | Drain-Source monitoring threshold | $0010010_B$ | **193** |
| **HS_VDS** | Drain-Source monitoring threshold | $0010011_B$ | **195** |
| **CCP_BLK** | CCP and  times selection | $0010100_B$ | **197** |
| **HBMODE** | Half-Bridge MODE | $0010101_B$ | **198** |
| **TPRECHG** | PWM pre-charge and pre-discharge time | $0010110_B$ | **200** |
| **ST_ICHG** | Static charge/discharge current | $0010111_B$ | **202** |

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**Table 36 Register Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| HB_ICHG | PWM charge/discharge current | $0011000_B$ | 203 |
| HB_ICHG_MAX | PWM max. pre-charge/pre-discharge current and diagnostic pull-down | $0011001_B$ | 204 |
| HB_PCHG_INIT | PWM pre-charge/pre-discharge initialization | $0011010_B$ | 206 |
| TDON_HB_CTRL | PWM inputs TON configuration | $0011011_B$ | 207 |
| TDOFF_HB_CTRL | PWM inputs TOFF configuration | $0011100_B$ | 208 |
| BRAKE | Brake control | $0011101_B$ | 209 |

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### 14.5.1 Device Control Registers

#### Mode and Supply Control

**M_S_CTRL**
**Mode and Supply Control** **(000 0001$_B$)** **Reset Value: see Table 37**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MODE | | RES | | | VCC1_OV_MOD | | RES | RSTN_HYS | RES | I_PEAK_TH | RES | | | VCC1_RT | |
| rwh | | r | | | rwh | | r | rw | r | rw | r | | | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **MODE** | 15:14 | rwh | **Device Mode Control**<br>$00_B$ **NORMAL**, Normal Mode<br>$01_B$ **SLEEP**, Sleep Mode<br>$10_B$ **STOP**, Stop Mode<br>$11_B$ **RESET**, Device reset: Soft reset is executed (configuration of RSTN triggering in bit **SOFT_RESET_RO**) |
| **RES** | 13:11 | r | **Reserved, always reads as 0** |
| **VCC1_OV_MOD** | 10:9 | rwh | **Reaction in case of VCC1 Over Voltage**<br>$00_B$ **NO**, no reaction<br>$01_B$ **INTN**, INTN event is generated<br>$10_B$ **RSTN**, RSTN event is generated<br>$11_B$ **FAILSAFE**, Fail-Safe Mode is entered |
| **RES** | 8 | r | **Reserved, always reads as 0** |
| **RSTN_HYS** | 7 | rw | **VCC1 Undervoltage Reset Hysteresis Selection (see also Chapter 13.7.1 for more information)**<br>$0_B$ **DEFAULT**, default hysteresis applies as specified in the electrical characteristics table<br>$1_B$ **HIGHEST**, the highest rising threshold (VRT1,R) is always used for the release of the undervoltage reset |
| **RES** | 6 | r | **Reserved, always reads as 0** |
| **I_PEAK_TH** | 5 | rw | **VCC1 Active Peak Threshold Selection**<br>$0_B$ **LOW**, low VCC1 active peak threshold selected<br>$1_B$ **HIGH**, high VCC1 active peak threshold selected |
| **RES** | 4:2 | r | **Reserved, always reads as 0** |
| **VCC1_RT** | 1:0 | rw | **VCC1 Reset Threshold Control**<br>$00_B$ **VRT1**, Vrt1 selected (highest threshold)<br>$01_B$ **VRT2**, Vrt2 selected<br>$10_B$ **VRT3**, Vrt3 selected<br>$11_B$ **VRT4**, Vrt4 selected |

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**Table 37 Reset of M_S_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 $0000_B$ | | | |
| Restart | 0000 0000 x0x0 $00xx_B$ | | | |

**Notes**

1. *It is not possible to change from Stop Mode to Sleep Mode via SPI Command. See also the State Machine Chapter.*
2. *After entering Restart Mode, the MODE bits will be automatically set to Normal Mode.*
3. *The SPI output will always show the previously written state with a Write Command (what has been programmed before) .*

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## Serial Peripheral Interface

### Hardware Control

**HW_CTRL**
**Hardware Control** **(000 0010$_B$)** **Reset Value: see Table 38**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | | TSD2_DEL | VS_OV_SEL | SH_DISABLE | RSTN_DEL | RES | | SOFT_RESET_RO | FO_ON | RES | | WD_STM_EN_1 | RES | |
| r | | | rw | rw | rw | rw | r | | rw | rwh | r | | rwh | r | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:13 | r | **Reserved, always reads as 0** |
| **TSD2_DEL** | 12 | rw | **TSD2 minimum Waiting Time Selection**<br>$0_B$ **1s**, Minimum waiting time until TSD2 is released again is always 1 s<br>$1_B$ **64s**, Minimum waiting time until TSD2 is released again is 1 s, after >16 TSD2 consecutive events, it will extended x 64 |
| **VS_OV_SEL** | 11 | rw | **VS OV comparator threshold change**<br>$0_B$ **20V**, Default threshold setting ($V_{S,OVD1}$)<br>$1_B$ **30V**, increased threshold setting ($V_{S,OVD2}$) |
| **SH_DISABLE** | 10 | rw | **Sample and hold circuitry disable**<br>$0_B$ **ENABLED**, Gate driver S&H circuitry enabled<br>$1_B$ **DISABLED**, Gate driver S&H circuitry disabled |
| **RSTN_DEL** | 9 | rw | **Reset delay time**<br>$0_B$ **10ms**, Reset delay time 10 ms ($t_{RD1}$)<br>$1_B$ **2ms**, Reset delay time to 2 ms ($t_{RD2}$) |
| **RES** | 8:7 | r | **Reserved, always reads as 0** |
| **SOFT_RESET_RO** | 6 | rw | **Soft Reset Configuration**<br>$0_B$ **RSTN**, RSTN will be triggered (pulled low) during a Soft Reset<br>$1_B$ **NO_RSTN**, no RSTN trigger during a Soft Reset |
| **FO_ON** | 5 | rwh | **Failure Output Activation**<br>$0_B$ **DISABLED**, FO not activated by software, FO will be activated by specified failures<br>$1_B$ **ENABLED**, FO activated by software (via SPI), only if WK2/FO pin is configured as Fail Safe Output |
| **RES** | 4:3 | r | **Reserved, always reads as 0** |
| **WD_STM_EN_1** | 2 | rwh | **Watchdog Deactivation during Stop Mode, bit1**<br>$0_B$ **ACTIVE**, Watchdog is active in Stop Mode<br>$1_B$ **INACTIVE**, Watchdog is deactivated in Stop Mode |
| **RES** | 1:0 | r | **Reserved, always reads as 0** |

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**Table 38 Reset of HW_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR | 0000 0000 0000 $0000_B$ | | | |
| Soft reset | 0000 00x0 0000 $0000_B$ | | | |
| Restart | 000x 00x0 0x00 $0000_B$ | | | |

**Notes**

1. *Clearing the FO_ON bit will not disable the FO outputs in case a failure occurred which triggered the FO outputs. In this case the FO outputs have to be disabled by clearing the FAILURE bit.*
   *If the FO_ON bit is set by the software then it will be cleared by the device after Restart Mode was entered and the FO outputs will be disabled (if no failures occurred which triggered the fail outputs) .*
2. *WD_STM_EN_1 will also be cleared when changing from Stop Mode to Normal Mode .*

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## Watchdog Control

### WD_CTRL

**Watchdog Control** **(000 0011$_B$)** **Reset Value: see Table 39**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CHECKSUM | RES | | | | | | | | WD_STM_EN_0 | WD_CFG | WD_EN_WK_BUS | RES | WD_TIMER | | |
| rw | r | | | | | | | | rwh | rw | rwh | r | rwh | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **CHECKSUM** | 15 | rw | **Watchdog Setting Check Sum Bit**<br>$0_B$ **0**, Counts as 0 for checksum calculation<br>$1_B$ **1**, Counts as 1 for checksum calculation |
| **RES** | 14:7 | r | **Reserved, always reads as 0** |
| **WD_STM_EN_0** | 6 | rwh | **Watchdog Deactivation during Stop Mode, bit0**<br>$0_B$ **ACTIVE**, Watchdog is active in Stop Mode<br>$1_B$ **INACTIVE**, Watchdog is deactivated in Stop Mode |
| **WD_CFG** | 5 | rw | **Watchdog Configuration**<br>$0_B$ **TIMEOUT**, Watchdog works as a Time-Out watchdog<br>$1_B$ **WINDOW**, Watchdog works as a Window watchdog |
| **WD_EN_ WK_BUS** | 4 | rwh | **Watchdog Enable after Bus Wake in Stop Mode**<br>$0_B$ **DISABLED**, Watchdog will not start after a CAN or LIN wake-up event<br>$1_B$ **ENABLED**, Watchdog starts with a long open window after CAN or LIN Wake-up event |
| **RES** | 3 | r | **Reserved, always reads as 0** |
| **WD_TIMER** | 2:0 | rwh | **Watchdog Timer Period**<br>$000_B$ **10ms**, 10ms<br>$001_B$ **20ms**, 20ms<br>$010_B$ **50ms**, 50ms<br>$011_B$ **100ms**, 100ms<br>$100_B$ **200ms**, 200ms<br>$101_B$ **500ms**, 500ms<br>$110_B$ **1s**, 1s<br>$111_B$ **10s**, 10s |

**Table 39 Reset of WD_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0001 0100$_B$ | | | |
| Restart | 0000 0000 000x 0100$_B$ | | | |

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**Notes**

1. *See also **Chapter 13.2.4** for more information on disabling the watchdog in Stop Mode.*
2. *See chapter **Chapter 13.2.5** for more information on the effect of the bit WD_EN_WK_BUS.*
3. *See chapter **Chapter 13.2.3** for calculation of checksum.*

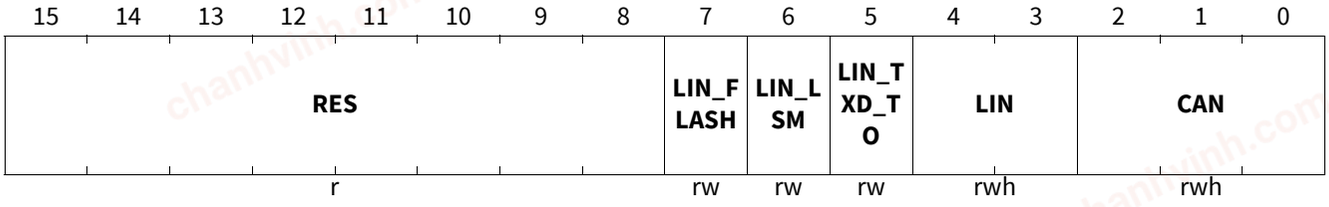
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## CAN and LIN Control

### BUS_CTRL

**CAN and LIN Control** **(000 0100$_B$)** **Reset Value: see Table 40**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:8 | r | **Reserved, always reads as 0** |
| **LIN_FLASH** | 7 | rw | **LIN Flash**<br>$0_B$ **ACTIVE**, Slope control mechanism active<br>$1_B$ **INACTIVE**, Deactivation of slope control for baudrates up to 115 kBaud |
| **LIN_LSM** | 6 | rw | **LIN LSM**<br>$0_B$ **NORMAL**, LIN Normal Mode is activated<br>$1_B$ **LOW_SLOPE**, LIN Low-Slope Mode (10.4 kBaud) activated |
| **LIN_TXD_TO** | 5 | rw | **LIN TXD TO**<br>$0_B$ **DISABLED**, TXD Time-out feature disabled<br>$1_B$ **ENABLED**, TXD Time-out feature enabled |
| **LIN** | 4:3 | rwh | **LIN Module Modes**<br>$00_B$ **OFF**, LIN OFF<br>$01_B$ **WAKE**, LIN wake capable<br>$10_B$ **RECEIVE**, LIN Receive Only Mode<br>$11_B$ **NORMAL**, LIN Normal Mode |
| **CAN** | 2:0 | rwh | **HS-CAN Module Modes**<br>$000_B$ **OFF**, CAN OFF<br>$001_B$ **WAKE**, CAN is wake capable (no SWK)<br>$010_B$ **RECEIVE**, CAN Receive Only Mode (no SWK)<br>$011_B$ **NORMAL**, CAN Normal Mode (no SWK)<br>$100_B$ **OFF**, CAN OFF |

**Table 40 Reset of BUS_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 0000 0000 xx0y 0x00$_B$ | | | |

**Notes**

1. *The reset values for CAN, LIN transceivers are marked with 'y' because they will vary depending on the cause of change.*
2. *See **Figure 25**, **Figure 32** for detailed state changes of CAN, LIN transceivers for different device modes.*

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3. *The bit CAN_2 is not modified by the device but can only be changed by the user. Therefore, the bit type is 'rw' compared to bits CAN_0 and CAN_1.*
4. *In case SYSERR = 0 and the CAN transceiver is configured to 'x11' while going to Sleep Mode, it will be automatically set to wake capable ('x01'). The SPI bits will be changed to wake capable. If configured to 'x10' and Sleep Mode is entered, then the transceiver is set to wake capable, while it will stay in Receive Only Mode when it had been configured to 'x10' when going to Stop Mode. If it had been configured to wake capable or OFF then the mode will remain unchanged.The Receive Only Mode has to be selected by the user before entering Stop Mode.*
5. *Failure Handling Mechanism: When the device enters Fail-Safe Mode due to a failure, then **BUS_CTRL** is modified by the device to 0000 0000 xxx0 $1001_B$ to ensure that the device can be woken again. See also the description in **Chapter 8.1**, **Chapter 9.1** and **Chapter 10.2.1** for **WK_CTRL** for other wake sources when entering Fail-Safe Mode.*
6. *When in Software Development Mode the POR/Soft Reset value are: CAN=$001_B$ , LIN=$11_B$.*

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## Wake-up Control

### WK_CTRL
**Wake-up Control** **(000 0101$_B$)** **Reset Value: see Table 41**

| 15 | 14 | 13 12 11 | 10 9 | 8 7 | 6 5 | 4 3 | 2 1 0 |
|---|---|---|---|---|---|---|---|
| WK2_FO | RES | WK_FILT | WK_PUPD | RES | WK_EN | RES | WK_BNK |
| rw | r | rw | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **WK2_FO** | 15 | rw | **WK2 / FO configuration**<br>$0_B$ **FAIL_SAFE**, WK2/FO pin configured as Fail Safe Output<br>$1_B$ **WAKE_UP**, WK2/FO pin configured as Wake-up Input |
| **RES** | 14 | r | **Reserved, always reads as 0** |
| **WK_FILT** | 13:11 | rw | **Wake-up Filter Time Configuration**<br>$000_B$ **16us**, Filter with 16 µs filter time (static sensing)<br>$001_B$ **64us**, Filter with 64 µs filter time (static sensing)<br>$010_B$ **TIMER1**, Filtering at the end of the on-time; filter time of 16 µs (cyclic sensing) is selected, Timer1<br>$011_B$ **TIMER2**, Filtering at the end of the on-time; filter time of 16 µs (cyclic sensing) is selected, Timer2<br>$100_B$ **SYNC**, Filter at the end of settle time (80 µs), filter time of 16 µs (cyclic sensing) is selected, SYNC[1)2)]<br>$101_B$ , reserved<br>$110_B$ , reserved<br>$111_B$ , reserved |
| **WK_PUPD** | 10:9 | rw | **WKx Pull-Up/Pull-Down Configuration**<br>$00_B$ **NO**, No pull-up/pull-down selected<br>$01_B$ **PULL_DOWN**, Pull-down resistor selected<br>$10_B$ **PULL_UP**, Pull-up resistor selected<br>$11_B$ **AUTO**, Automatic switching to pull-up or pull-down |
| **RES** | 8:7 | r | **Reserved, always reads as 0** |
| **WK_EN** | 6:5 | rw | **WKx Enable**<br>$00_B$ **WK_OFF**, WKx module OFF<br>$01_B$ **WK_ON**, WKx module ON<br>$10_B$ **SYNC**, OFF or (in case of WK4), it is configured as SYNC input<br>$11_B$ **OFF**, OFF |
| **RES** | 4:3 | r | **Reserved, always reads as 0** |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **WK_BNK** | 2:0 | rw | **WKs input Banking**<br>$000_B$ **WK1**, WK1 Module (Bank 1)<br>$001_B$ **WK2**, WK2 Module (Bank 2)<br>$010_B$ **WK3**, WK3 Module (Bank 3)<br>$011_B$ **WK4**, WK4 Module (Bank 4)<br>$101_B$ , reserved<br>$110_B$ , reserved<br>$111_B$ , reserved |

1) This setting is available only in case of WK4 configured as **WK_EN**=$10_B$.
2) The min TON time for cyclic sense with SYNC is 100 µs.

**Table 41 Reset of WK_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0010 $0000_B$ | | | |
| Restart | x0xx xxx0 0xx0 $0000_B$ | | | |

**Notes**

1. ***WK2_FO*** *bit is accessable only if the Bank 2 is selected.*
2. *The SYNC functionality is accessable only if the Bank 4 is selected.*
3. *When selecting a filter time configuration, the user must make sure to also assign the respective timer/SYNC to at least one HS switch during cyclic sense operation.*
4. *At Fail-Safe Mode entry* ***WK_EN*** *will be automatically changed (by the device) in “01”.*
   *Exceptions: WK2 is configured as FO and WK4 if configured as SYNC previously*
5. *During Fail-Safe Mode the* ***WK_FILT*** *bits are ignored and static-sense with 16 µs filter time is used by default.*

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## Timer 1 and Timer2 Control and Selection

### TIMER_CTRL

**Timer 1 and Timer2 Control and Selection (000 0110$_B$) Reset Value: see Table 42**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TIMER2_ON | | | RES | TIMER2_PER | | | CYCWK | | TIMER1_ON | | | RES | TIMER1_PER | | |
| rwh | | | r | rwh | | | rwh | | rwh | | | r | rwh | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **TIMER2_ON** | 15:13 | rwh | **Timer2 On-Time Configuration**<br>$000_B$ **OFF_LOW**, OFF / Low (timer not running, HSx output is low)<br>$001_B$ **100us**, 0.1ms on-time<br>$010_B$ **300us**, 0.3ms on-time<br>$011_B$ **1ms**, 1.0ms on-time<br>$100_B$ **10ms**, 10ms on-time<br>$101_B$ **20ms**, 20ms on-time<br>$110_B$ **OFF_HIGH**, OFF / HIGH (timer not running, HSx output is high)<br>$111_B$ , reserved, same behaviour as $110_B$ |
| **RES** | 12 | r | **Reserved, always reads as 0** |
| **TIMER2_PER** | 11:9 | rwh | **Timer2 Period Configuration**<br>$000_B$ **10ms**, 10ms<br>$001_B$ **20ms**, 20ms<br>$010_B$ **50ms**, 50ms<br>$011_B$ **100ms**, 100ms<br>$100_B$ **200ms**, 200ms<br>$101_B$ **500ms**, 500ms<br>$110_B$ **1s**, 1s<br>$111_B$ **2s**, 2s |
| **CYCWK** | 8:7 | rwh | **Cyclic Wake Configuration**<br>$00_B$ **DISABLED**, Timer1 and Timer2 disabled as wake-up sources<br>$01_B$ **TIMER1**, Timer1 is enabled as wake-up source (Cyclic Wake)<br>$10_B$ **TIMER2**, Timer2 is enabled as wake-up source (Cyclic Wake)<br>$11_B$ , reserved |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **TIMER1_ON** | 6:4 | rwh | **Timer1 On-Time Configuration**<br>$000_B$ **OFF_LOW**, OFF / Low (timer not running, HSx output is low)<br>$001_B$ **100us**, 0.1ms on-time<br>$010_B$ **300us**, 0.3ms on-time<br>$011_B$ **1ms**, 1.0ms on-time<br>$100_B$ **10ms**, 10ms on-time<br>$101_B$ **20ms**, 20ms on-time<br>$110_B$ **OFF_HIGH**, OFF / HIGH (timer not running, HSx output is high)<br>$111_B$ , reserved, same behaviour as $110_B$ |
| **RES** | 3 | r | **Reserved, always reads as 0** |
| **TIMER1_PER** | 2:0 | rwh | **Timer1 Period Configuration**<br>$000_B$ **10ms**, 10ms<br>$001_B$ **20ms**, 20ms<br>$010_B$ **50ms**, 50ms<br>$011_B$ **100ms**, 100ms<br>$100_B$ **200ms**, 200ms<br>$101_B$ **500ms**, 500ms<br>$110_B$ **1s**, 1s<br>$111_B$ **2s**, 2s |

**Table 42 Reset of TIMER_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | $0000\ 0000\ 0000\ 0000_B$ | | | |
| Restart | $0000\ 0000\ 0000\ 0000_B$ | | | |

**Notes**

1. *The timer must be first assigned and is then automatically activated as soon as the on-time is configured.*
2. *If cyclic sense is selected and the HSx switch is cleared during Restart Mode then also the timer settings (period and on-time) are cleared to avoid incorrect switch detection. However, the timer settings are not cleared in case of failure not leading to Restart Mode.*
3. *In case the timer is set as wake sources and cyclic sense is running, then both cyclic sense and cyclic wake will be active at the same time.*
4. *Timer accuracy is linked to the oscillator accuracy (see Parameter P_13.12.43).*

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## High-Side Switch Shutdown Control

### SW_SD_CTRL

**High-Side Switch Shutdown Control** **(000 0111$_B$)** **Reset Value: see Table 43**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HS4_OV_REC | HS3_OV_REC | HS2_OV_REC | HS1_OV_REC | HS_OT_SD_DIS | HS4_OV_SDN_DIS | HS3_OV_SDN_DIS | HS2_OV_SDN_DIS | HS1_OV_SDN_DIS | HS_OV_SDS_DIS | HS_UV_SD_DIS | RES | HS_UV_REC | RES | | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | r | rw | r | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HS4_OV_REC** | 15 | rw | **Switch recovery after removal of VSHS Overvoltage for HS4**<br>$0_B$ **DISABLED**, Switch recovery is disabled<br>$1_B$ **PREVIOUS**, Previous state before VSHS Overvoltage is enabled after Overvoltage considtion is removed |
| **HS3_OV_REC** | 14 | rw | **Switch recovery after removal of VSHS Overvoltage for HS3**<br>$0_B$ **DISABLED**, Switch recovery is disabled<br>$1_B$ **PREVIOUS**, Previous state before VSHS Overvoltage is enabled after Overvoltage considtion is removed |
| **HS2_OV_REC** | 13 | rw | **Switch recovery after removal of VSHS Overvoltage for HS2**<br>$0_B$ **DISABLED**, Switch recovery is disabled<br>$1_B$ **PREVIOUS**, Previous state before VSHS Overvoltage is enabled after Overvoltage considtion is removed |
| **HS1_OV_REC** | 12 | rw | **Switch recovery after removal of VSHS Overvoltage for HS1**<br>$0_B$ **DISABLED**, Switch recovery is disabled<br>$1_B$ **PREVIOUS**, Previous state before VSHS Overvoltage is enabled after Overvoltage considtion is removed |
| **HS_OT_SD_DIS** | 11 | rw | **Shutdown Disabling of all HS in case of Overtemperature event**<br>$0_B$ **ALL**, shudown for all HSx in case of Overtemperature<br>$1_B$ **INDIVIDUAL**, individual shudown in case of Overtemperature |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **HS4_OV_SDN_DIS** | 10 | rw | **Shutdown Disabling of HS4 in case of input supply overvoltage in Normal Mode**<br>$0_B$ **ENABLED**, shudown enabled in case of VSHS Overvoltage<br>$1_B$ **DISABLED**, shudown disabled in case of VSHS Overvoltage |
| **HS3_OV_SDN_DIS** | 9 | rw | **Shutdown Disabling of HS3 in case of input supply overvoltage in Normal Mode**<br>$0_B$ **ENABLED**, shudown enabled in case of VSHS Overvoltage<br>$1_B$ **DISABLED**, shudown disabled in case of VSHS Overvoltage |
| **HS2_OV_SDN_DIS** | 8 | rw | **Shutdown Disabling of HS2 in case of input supply overvoltage in Normal Mode**<br>$0_B$ **ENABLED**, shudown enabled in case of VSHS Overvoltage<br>$1_B$ **DIASBLED**, shudown disabled in case of VSHS Overvoltage |
| **HS1_OV_SDN_DIS** | 7 | rw | **Shutdown Disabling of HS1 in case of input supply overvoltage in Normal Mode**<br>$0_B$ **ENABLED**, shudown enabled in case of VSHS Overvoltage<br>$1_B$ **DISABLED**, shudown disabled in case of VSHS Overvoltage |
| **HS_OV_SDS_DIS** | 6 | rw | **Shutdown Disabling of HSx in case of input supply overvoltage in Stop Mode or Sleep Mode**<br>$0_B$ **ENABLED**, shudown enabled in case of VSHS Overvoltage<br>$1_B$ **DISABLED**, shudown disabled in case of VSHS Overvoltage |
| **HS_UV_SD_DIS** | 5 | rw | **Shutdown Disabling of HSx in case of input supply undervoltage**<br>$0_B$ **ENABLED**, shudown enabled in case of VSHS Undervoltage<br>$1_B$ **DISABLED**, shudown disabled in case of VSHS Undervoltage |
| **RES** | 4 | r | **Reserved, always reads as 0** |
| **HS_UV_REC** | 3 | rw | **Switch recovery after removal of Undervoltage for HSx**<br>$0_B$ **DISABLED**, Switch recovery is disabled<br>$1_B$ **PREVIOUS**, Previous state before VSHS Undervoltage is enabled after Undervoltage considtion is removed |
| **RES** | 2:0 | r | **Reserved, always reads as 0** |

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**Table 43 Reset of SW_SD_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 $0000_B$ | | | |
| Restart | xxxx xxxx xxx0 $x000_B$ | | | |

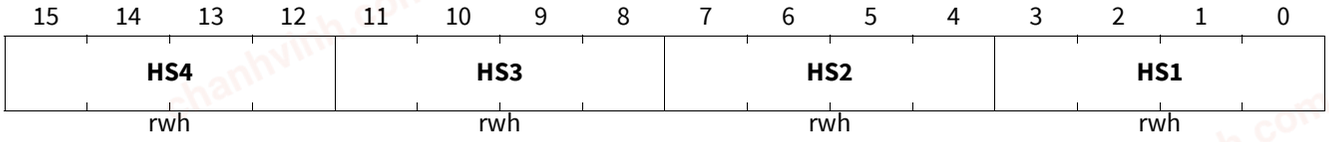
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## High-Side Switch Control

### HS_CTRL

**High-Side Switch Control** **(000 1000$_B$)** **Reset Value: see Table 44**




| Field | Bits | Type | Description |
|---|---|---|---|
| **HS4** | 15:12 | rwh | **HS4 Configuration**<br>$0000_B$**OFF**, OFF<br>$0001_B$**ON**, ON<br>$0010_B$**TIMER1**, Controlled by Timer1<br>$0011_B$**TIMER2**, Controlled by Timer2<br>$0100_B$**PWM1**, Controlled by PWM1<br>$0101_B$**PWM2**, Controlled by PWM2<br>$0110_B$**PWM3**, Controlled by PWM3<br>$0111_B$**PWM4**, Controlled by PWM4<br>$1000_B$**WK4_SYNC**, Synchronized with WK4/SYNC<br>$1001_B$, reserved<br>$1010_B$, reserved<br>$1011_B$, reserved<br>$1100_B$, reserved<br>$1101_B$, reserved<br>$1110_B$, reserved<br>$1111_B$, reserved |
| **HS3** | 11:8 | rwh | **HS3 Configuration**<br>$0000_B$**OFF**, OFF<br>$0001_B$**ON**, ON<br>$0010_B$**TIMER1**, Controlled by Timer1<br>$0011_B$**TIMER2**, Controlled by Timer2<br>$0100_B$**PWM1**, Controlled by PWM1<br>$0101_B$**PWM2**, Controlled by PWM2<br>$0110_B$**PWM3**, Controlled by PWM3<br>$0111_B$**PWM4**, Controlled by PWM4<br>$1000_B$**WK4_SYNC**, Synchronized with WK4/SYNC<br>$1001_B$, reserved<br>$1010_B$, reserved<br>$1011_B$, reserved<br>$1100_B$, reserved<br>$1101_B$, reserved<br>$1110_B$, reserved<br>$1111_B$, reserved |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **HS2** | 7:4 | rwh | **HS2 Configuration**<br>$0000_B$**OFF**, OFF<br>$0001_B$**ON**, ON<br>$0010_B$**TIMER1**, Controlled by Timer1<br>$0011_B$**TIMER2**, Controlled byTimer2<br>$0100_B$**PWM1**, Controlled by PWM1<br>$0101_B$**PWM2**, Controlled by PWM2<br>$0110_B$**PWM3**, Controlled by PWM3<br>$0111_B$**PWM4**, Controlled by PWM4<br>$1000_B$**WK4_SYNC**, Synchronized with WK4/SYNC<br>$1001_B$, reserved<br>$1010_B$, reserved<br>$1011_B$, reserved<br>$1100_B$, reserved<br>$1101_B$, reserved<br>$1110_B$, reserved<br>$1111_B$, reserved |
| **HS1** | 3:0 | rwh | **HS1 Configuration**<br>$0000_B$**OFF**, OFF<br>$0001_B$**ON**, ON<br>$0010_B$**TIMER1**, Controlled by Timer1<br>$0011_B$**TIMER2**, Controlled by Timer2<br>$0100_B$**PWM1**, Controlled by PWM1<br>$0101_B$**PWM2**, Controlled by PWM2<br>$0110_B$**PWM3**, Controlled by PWM3<br>$0111_B$**PWM4**, Controlled by PWM4<br>$1000_B$**WK4_SYNC**, Synchronized with WK4/SYNC<br>$1001_B$, reserved<br>$1010_B$, reserved<br>$1011_B$, reserved<br>$1100_B$, reserved<br>$1101_B$, reserved<br>$1110_B$, reserved<br>$1111_B$, reserved |

**Table 44 Reset of HS_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | $0000\ 0000\ 0000\ 0000_B$ | | | |
| Restart | $0000\ 0000\ 0000\ 0000_B$ | | | |

PWMx in this register designates the internal PWM generators for the integrated high-side switches.

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## Interrupt Mask Control[1)]

**INT_MASK**
**Interrupt Mask Control** **(000 1001$_B$)** **Reset Value: see Table 45**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | | | | | | INTN_CYC_EN | WD_SDM_DISABLE | WD_SDM | SPI_CRC_FAIL | BD_STAT | HS_STAT | BUS_STAT | TEMP_STAT | SUPPLY_STAT |
| r | | | | | | | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:9 | r | **Reserved, always reads as 0** |
| **INTN_CYC_EN** | 8 | rw | **Periodical INTN generation**<br>$0_B$ **DISABLED**, no periodical INTN event generated in case of pending interrupts<br>$1_B$ **ENABLED**, periodical INTN event generated in case of pending interrupts |
| **WD_SDM_DISABLE** | 7 | rw | **Disable Watchdog in Software Development Mode**<br>$0_B$ **ENABLED**, WD is enabled in Software Development Mode<br>$1_B$ **DISABLED**, WD is disabled in Software Development Mode |
| **WD_SDM** | 6 | rw | **Watchdog failure in Software Development Mode**<br>$0_B$ **DISABLED**, no INTN event generated in case of WD trigger failure in Software Development Mode<br>$1_B$ **ENABLED**, one INTN event is generated in case of WD trigger failure in Software Development Mode |
| **SPI_CRC_FAIL** | 5 | rw | **SPI and CRC interrupt generation**<br>$0_B$ **DISABLED**, no INTN event generated in case of SPI_FAIL or CRC_FAIL<br>$1_B$ **ENABLED**, one INTN event is generated n case of SPI_FAIL or CRC_FAIL |
| **BD_STAT** | 4 | rw | **Bridge Driver Interrupt generation**<br>$0_B$ **DISABLED**, no INTN event generated in case BD_STAT (on Status Information Field) is set<br>$1_B$ **ENABLED**, one INTN event generated in case BD_STAT (on Status Information Field) is set |
| **HS_STAT** | 3 | rw | **High Side Interrupt generation**<br>$0_B$ **DISABLED**, no INTN event generated in case HS_STAT (on Status Information Field) is set<br>$1_B$ **ENABLED**, one INTN event generated in case HS_STAT (on Status Information Field) is set |

1) Every event will generate a signal on the INTN pin (when masked accordingly).
Even if the status-bit was already set in the corresponding status-register it can still trigger a signal on the INTN pin.

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| Field | Bits | Type | Description |
|---|---|---|---|
| **BUS_STAT** | 2 | rw | **BUS Interrupt generation**<br>$0_B$ **DISABLED**, no INTN event generated in case BUS_STAT (on Status Information Field) is set<br>$1_B$ **ENABLED**, one INTN event generated in case BUS_STAT (on Status Information Field) is set |
| **TEMP_STAT** | 1 | rw | **Temperature Interrupt generation**<br>$0_B$ **DISABLED**, no INTN event generated in case TEMP_STAT (on Status Information Field) is set<br>$1_B$ **ENABLED**, one INTN event generated in case TEMP_STAT (on Status Information Field) is set |
| **SUPPLY_STAT** | 0 | rw | **SUPPLY Status Interrupt generation**<br>$0_B$ **DISABLED**, no INTN event generated in case SUPPLY_STAT (on Status Information Field) is set<br>$1_B$ **ENABLED**, one INTN event generated in case SUPPLY_STAT (on Status Information Field) is set |

**Table 45 Reset of INT_MASK**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0001 0100 $0000_B$ | | | |
| Restart | 0000 000x xxxx $xxxx_B$ | | | |

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### PWM Configuration Control

**PWM_CTRL**
**PWM Configuration Control** **(000 1010$_B$)** **Reset Value: see Table 46**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | PWM_FREQ | PWM_DC | | | | | | | | | | RES | PWM_BNK | | |
| r | rw | rw | | | | | | | | | | r | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15 | r | **Reserved, always reads as 0** |
| **PWM_FREQ** | 14 | rw | **PWM generator Frequency Setting**<br>$0_B$ **100Hz**, 100Hz is selected<br>$1_B$ **200Hz**, 200Hz is selected |
| **PWM_DC** | 13:4 | rw | **PWM Duty Cycle Setting (bit4 = LSB; bit13 = MSB)**<br>00 0000 0000$_B$, 100% OFF, i.e. HS = OFF<br>xx xxxx xxxx$_B$, ON with duty cycle fraction of 1024<br>11 1111 1111$_B$, 100% ON, i.e. HS = ON |
| **RES** | 3 | r | **Reserved, always reads as 0** |
| **PWM_BNK** | 2:0 | rw | **Internal PWM generator selection**<br>$000_B$ **PWM1**, PWM1 Module<br>$001_B$ **PWM2**, PWM2 Module<br>$010_B$ **PWM3**, PWM3 Module<br>$011_B$ **PWM4**, PWM4 Module<br>$1xx_B$ , Don't care |

**Table 46 Reset of PWM_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 0xxx xxxx xxxx 0000$_B$ | | | |

PWMx in this register designates the internal PWM generators for the integrated high-side switches.

**Notes**

1. *0% and 100% duty cycle settings are used to have the switch turned ON or OFF respectively.*
2. *The desired duty cycle should be set first before the HSx is enabled as PWM.*
3. *The PWM signal is correct only after at least one PWM pulse.*
4. *PWM generator accuracy is linked to the oscillator accuracy (see parameter P_13.12.43).*

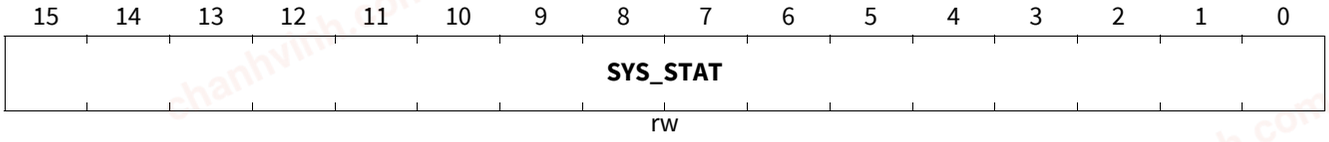
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### System Status Control

#### SYS_STAT_CTRL

**System Status Control** **(000 1011$_B$)** **Reset Value: see Table 47**




| Field | Bits | Type | Description |
|---|---|---|---|
| **SYS_STAT** | 15:0 | rw | **System Status Control (bit0=LSB; bit15=MSB)** Dedicated bytes for system configuration, access only by microcontroller. Cleared after power up and soft reset. |

**Table 47 Reset of SYS_STAT_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR / Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | xxxx xxxx xxxx xxxx$_B$ | | | |

*Note: This register is intended for storing system configuration of the ECU by the microcontroller and is only accessible in Normal Mode. The register is not accessible by the TLE9562QX and is also not cleared after Fail-Safe or Restart Mode. It allows the microcontroller to quickly store system configuration without loosing data.*

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## 14.5.2 Control registers bridge driver

### General Bridge Control

**GENCTRL**
**General Bridge Control** **(001 0000$_B$)** **Reset Value: see Table 48**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BDFREQ | PWM34MAP | PWM12MAP | CPUVTH | FET_LVL | CPSTGA | BDOV_REC | IPCHGADT | AGC | | CPEN | POCHGDIS | AGCFILT | EN_GEN_CHECK | IHOLD | FMODE |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **BDFREQ** | 15 | rw | **Bridge driver synchronization frequency**<br>$0_B$ **18MHz**, typ. 18.75 MHz (default)<br>$1_B$ **37MHz**, typ. 37.5 MHz |
| **PWM34MAP** | 14 | rw | **PWM34MAP**<br>$0_B$ **PWM3_TO_HB3**, PWM3 mapped to HB3 (default)<br>$1_B$ **PWM3_TO_HB4**, PWM3 mapped to HB4 |
| **PWM12MAP** | 13 | rw | **PWM12MAP**<br>$0_B$ **PWM1_TO_HB1**, PWM1/CRC mapped to HB1 (default)<br>$1_B$ **PWM1_TO_HB2**, PWM1/CRC mapped to HB2 |
| **CPUVTH** | 12 | rw | **Charge pump under voltage (referred to VS)**<br>$0_B$ **TH1**, (default) CPUV threshold 1 for FET_LVL = 0, CPUV threshold 1 for FET_LVL = 1<br>$1_B$ **TH2**, CPUV threshold 2 for FET_LVL = 0, CPUV threshold 2 for FET_LVL = 1 |
| **FET_LVL** | 11 | rw | **External MOSFET normal / logic level selection**<br>$0_B$ **LOGIC**, Logic level MOSFET selected<br>$1_B$ **NORMAL**, Normal level MOSFET selected(default) |
| **CPSTGA** | 10 | rw | **Automatic switchover between dual and single charge pump stage**<br>$0_B$ **INACTIVE**, Automatic switch over deactivated (default)<br>$1_B$ **ACTIVE**, Automatic switch over activated |
| **BDOV_REC** | 9 | rw | **Bridge driver recover from VS and VSINT Overvoltage**<br>$0_B$ **INACTIVE**, Recover deactivated (default)<br>$1_B$ **ACTIVE**, Recover activated |
| **IPCHGADT** | 8 | rw | **Adaptation of the pre-charge and pre-discharge current**<br>$0_B$ **1STEP**, 1 current step (default)<br>$1_B$ **2STEPS**, 2 current steps |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **AGC** | 7:6 | rw | **Adaptive gate control**<br>$00_B$ **INACTIVE1**, (default) Adaptive gate control disabled, pre-charge and pre-discharge disabled<br>$01_B$ **INACTIVE2**, Adaptive gate control disabled, precharge is enabled with IPRECHG = IPCHGINIT, predischarge is enabled with IPREDCHG = IPDCHGINIT<br>$10_B$ **ACTIVE**, Adaptive gate control enabled, IPRECHG and IPREDCHG are self adapted<br>$11_B$ , reserved. Adaptive gate control enabled, IPRECHG and IPREDCHG are self adapted |
| **CPEN** | 5 | rw | **CPEN**<br>$0_B$ **DISABLED**, Charge pump disabled (default)<br>$1_B$ **ENABLED**, Charge pump enabled |
| **POCHGDIS** | 4 | rw | **Postcharge disable bit**<br>$0_B$ **ENABLED**, The postcharge phase is enabled during PWM (default)<br>$1_B$ **DISABLED**, The postcharge phase is disabled during PWM |
| **AGCFILT** | 3 | rw | **Filter for adaptive gate control**<br>$0_B$ **NO_FILT**, No filter applied (default)<br>$1_B$ **FILT_APPL**, Filter applied |
| **EN_GEN_CHECK** | 2 | rw | **Detection of active / FW MOSFET**<br>$0_B$ **DISABLED**, Detection disabled (default)<br>$1_B$ **ENABLED**, Detection enabled |
| **IHOLD** | 1 | rw | **Gate driver hold current IHOLD**<br>$0_B$ **TH1**, (default) Charge: $I_{CHG19}$ , discharge $I_{DCHG19}$ .<br>$1_B$ **TH2**, Charge: $I_{CHG25}$, discharge: $I_{CHG25}$ |
| **FMODE** | 0 | rw | **Frequency modulation of the charge pump**<br>$0_B$ **NO**, No modulation<br>$1_B$ **15KHz**, Modulation frequency 15.6 kHz (default) |

**Table 48 Reset of GENCTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 1000 0000 $0001_B$ | | | |
| Restart | xxxx xxxx xxxx $xxxx_B$ | | | |

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### Drain-Source monitoring threshold LS1-4

**LS_VDS**
**VDS monitoring threshold LS1-4** **(001 0010$_B$)** **Reset Value: see Table 49**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | TFVDS | | LS4VDSTH | | | LS3VDSTH | | | LS2VDSTH | | | LS1VDSTH | | |
| r | | rw | | rw | | | rw | | | rw | | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved. Always read as 0** |
| **TFVDS** | 13:12 | rw | **Filter time of drain-source voltage monitoring**<br>$00_B$ **500ns**, 0.5 µs (default)<br>$01_B$ **1us**, 1 µs<br>$10_B$ **2us**, 2 µs<br>$11_B$ **6us**, 6 µs |
| **LS4VDSTH** | 11:9 | rw | **LS4 drain-source overvoltage threshold**<br>$000_B$ **160mV**, 0.16 V<br>$001_B$ **200mV**, 0.20 V (default)<br>$010_B$ **300mV**, 0.30 V<br>$011_B$ **400mV**, 0.40 V<br>$100_B$ **500mV**, 0.50 V<br>$101_B$ **600mV**, 0.60 V<br>$110_B$ **800mV**, 0.80 V<br>$111_B$ **2V**, 2.0 V |
| **LS3VDSTH** | 8:6 | rw | **LS3 drain-source overvoltage threshold**<br>$000_B$ **160mV**, 0.16 V<br>$001_B$ **200mV**, 0.20 V (default)<br>$010_B$ **300mV**, 0.30 V<br>$011_B$ **400mV**, 0.40 V<br>$100_B$ **500mV**, 0.50 V<br>$101_B$ **600mV**, 0.60 V<br>$110_B$ **800mV**, 0.80 V<br>$111_B$ **2V**, 2.0 V |
| **LS2VDSTH** | 5:3 | rw | **LS2 drain-source overvoltage threshold**<br>$000_B$ **160mV**, 0.16V<br>$001_B$ **200mV**, 0.20 V (default)<br>$010_B$ **300mV**, 0.30 V<br>$011_B$ **400mV**, 0.40 V<br>$100_B$ **500mV**, 0.50 V<br>$101_B$ **600mV**, 0.60 V<br>$110_B$ **800mV**, 0.80 V<br>$111_B$ **2V**, 2.0 V |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **LS1VDSTH** | 2:0 | rw | **LS1 drain-source overvoltage threshold**<br>$000_B$ **160mV**, 0.16 V<br>$001_B$ **200mV**, 0.20 V (default)<br>$010_B$ **300mV**, 0.30 V<br>$011_B$ **400mV**, 0.40 V<br>$100_B$ **500mV**, 0.50 V<br>$101_B$ **600mV**, 0.60 V<br>$110_B$ **800mV**, 0.80 V<br>$111_B$ **2V**, 2.0 V |

**Table 49 Reset of LS_VDS**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0010 0100 $1001_B$ | 0000 0000 0000 0000 | | |
| Restart | 0000 xxxx xxxx $xxxx_B$ | | | |

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### Drain-Source monitoring Threshold HS1-4

**HS_VDS**
**VDS monitoring threshold HS1-4** **(001 0011$_B$)** **Reset Value: see Table 50**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | RES | DEEP_ADAP | HS4VDSTH | | | HS3VDSTH | | | HS2VDSTH | | | HS1VDSTH | | |
| r | | rw | rw | rw | | | rw | | | rw | | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved. Always read as 0** |
| **RES** | 13 | rw | **Reserved. This bit must be programmed to ‘0‘** |
| **DEEP_ADAP** | 12 | rw | **Deep adaptation enable**<br>$0_B$ **NO_DEEP_ADAP**, Deep adaptation disabled (default)<br>$1_B$ **DEEP_ADAP**, Deep adaptation enabled |
| **HS4VDSTH** | 11:9 | rw | **HS4 drain-source overvoltage threshold**<br>$000_B$ **160mV**, 0.16 V<br>$001_B$ **200mV**, 0.20 V (default)<br>$010_B$ **300mV**, 0.30 V<br>$011_B$ **400mV**, 0.40 V<br>$100_B$ **500mV**, 0.50 V<br>$101_B$ **600mV**, 0.60 V<br>$110_B$ **800mV**, 0.80 V<br>$111_B$ **2V**, 2.0 V |
| **HS3VDSTH** | 8:6 | rw | **HS3 drain-source overvoltage threshold**<br>$000_B$ **160mV**, 0.16 V<br>$001_B$ **200mV**, 0.20 V (default)<br>$010_B$ **300mV**, 0.30 V<br>$011_B$ **400mV**, 0.40 V<br>$100_B$ **500mV**, 0.50 V<br>$101_B$ **600mV**, 0.60 V<br>$110_B$ **800mV**, 0.80 V<br>$111_B$ **2V**, 2.0 V |
| **HS2VDSTH** | 5:3 | rw | **HS2 drain-source overvoltage threshold**<br>$000_B$ **160mV**, 0.16 V<br>$001_B$ **200mV**, 0.20 V (default)<br>$010_B$ **300mV**, 0.30 V<br>$011_B$ **400mV**, 0.40 V<br>$100_B$ **500mV**, 0.50 V<br>$101_B$ **600mV**, 0.60 V<br>$110_B$ **800mV**, 0.80 V<br>$111_B$ **2V**, 2.0 V |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **HS1VDSTH** | 2:0 | rw | **HS1 drain-source overvoltage threshold**<br>$000_B$ **160mV**, 0.16 V<br>$001_B$ **200mV**, 0.20 V (default)<br>$010_B$ **300mV**, 0.30 V<br>$011_B$ **400mV**, 0.40 V<br>$100_B$ **500mV**, 0.50 V<br>$101_B$ **600mV**, 0.60 V<br>$110_B$ **800mV**, 0.80 V<br>$111_B$ **2V**, 2.0 V |

**Table 50 Reset of HS_VDS**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0010 0100 $1001_B$ | | | |
| Restart | 00xx xxxx xxxx $xxxx_B$ | | | |

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### CCP and times selection

**CCP_BLK**
**CCP and times selection** **(001 0100$_B$)** **Reset Value: see Table 51**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TBLANK | | | | TCCP | | | | RES | | | | | CCP_BNK | | |
| rw | | | | rw | | | | r | | | | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **TBLANK** | 15:12 | rw | **Blank time**<br>nom. tHBxBLANK = 587 ns + 266 x T[3:0]$_D$<br>The CCP_BNK bits select the blank time for the FW or active MOSFET and the half-bridge HBx<br>Reset of active and FW tHBxBLANK: 2450 ns typ. |
| **TCCP** | 11:8 | rw | **Cross-current protection time**<br>nom. tHBxCCP = 587 ns + 266 x TCCP[3:0]$_D$<br>The CCP_BNK bits select the cross-current protection time for the FW or active MOSFET and the half-bridge HBx<br>Reset of all active and FW tHBxCCP: 2450 ns typ. |
| **RES** | 7:3 | r | **Reserved, always reads as 0** |
| **CCP_BNK** | 2:0 | rw | **Cross-current and time banking**<br>$000_B$ **ACT_HB1**, Active blank and cross-current prot. times for HB1 (default)<br>$001_B$ **ACT_HB2**, Active blank and cross-current prot. times for HB2<br>$010_B$ **ACT_HB3**, Active blank and cross-current prot. times for HB3<br>$011_B$ **ACT_HB4**, Active blank and cross-current prot. times for HB4<br>$100_B$ **FW_HB1**, FW blank and cross-current prot. times for HB1<br>$101_B$ **FW_HB2**, FW blank and cross-current prot. times for HB2<br>$110_B$ **FW_HB3**, FW blank and cross-current prot. for times for HB3<br>$111_B$ **FW_HB4**, FW blank and cross-current prot. for times for HB4 |

**Table 51 Reset of CCP_BLK**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0111 0111 0000 0000$_B$ | | | |
| Restart | xxxx xxxx 0000 0000$_B$ | | | |

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## Half-Bridge MODE

### HBMODE

**Half-Bridge MODE** **(001 0101$_B$)** **Reset Value: see Table 52**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HB4MODE | | AFW4 | HB4_PWM_EN | HB3MODE | | AFW3 | HB3_PWM_EN | HB2MODE | | AFW2 | HB2_PWM_EN | HB1MODE | | AFW1 | HB1_PWM_EN |
| rw | | rw | rw | rw | | rw | rw | rw | | rw | rw | rw | | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HB4MODE** | 15:14 | rw | **Half-bridge 4 MODE selection**<br>$00_B$ **PASSIVE_OFF**, LS4 and HS4 are off by passive discharge (default)<br>$01_B$ **LS4_ON**, LS4 is ON<br>$10_B$ **HS4_ON**, HS4 is ON<br>$11_B$ **ACTIVE_OFF**, LS4 and HS4 kept off by the active discharge |
| **AFW4** | 13 | rw | **Active freewheeling for half-bridge 4 during PWM**<br>$0_B$ **DISABLED**, active freewheeling disabled<br>$1_B$ **ENABLED**, active freewheeling enabled (default) |
| **HB4_PWM_EN** | 12 | rw | **PWM mode for half-bridge 4 if PWM34MAP = 1**[1)]<br>$0_B$ **INACTIVE**, PWM deactivated for HB4(default)<br>$1_B$ **ACTIVE**, PWM activated for HB4 |
| **HB3MODE** | 11:10 | rw | **Half-bridge 3 MODE selection**<br>$00_B$ **PASSIVE_OFF**, LS3 and HS3 are off by passive discharge (default)<br>$01_B$ **LS3_ON**, LS3 is ON<br>$10_B$ **HS3_ON**, HS3 is ON<br>$11_B$ **ACTIVE_OFF**, LS3 and HS3 kept off by the active discharge |
| **AFW3** | 9 | rw | **Active freewheeling for half-bridge 3 during PWM**<br>$0_B$ **DISABLED**, active freewheeling disabled<br>$1_B$ **ENABLED**, active freewheeling enabled (default) |
| **HB3_PWM_EN** | 8 | rw | **PWM mode for half-bridge 3 if PWM34MAP=0**[2)]<br>$0_B$ **INACTIVE**, PWM deactivated for HB2(default)<br>$1_B$ **ACTIVE**, PWM activated for HB2 |
| **HB2MODE** | 7:6 | rw | **Half-bridge 2 MODE selection**<br>$00_B$ **PASSIVE_OFF**, LS2 and HS2 are off by passive discharge (default)<br>$01_B$ **LS2_ON**, LS2 is ON<br>$10_B$ **HS2_ON**, HS2 is ON<br>$11_B$ **ACTIVE_OFF**, LS2 and HS2 kept off by the active discharge |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **AFW2** | 5 | rw | **Active freewheeling for half-bridge 2 during PWM**<br>$0_B$ **DISABLED**, active freewheeling disabled<br>$1_B$ **ENABLED**, active freewheeling enabled (default) |
| **HB2_PWM_EN** | 4 | rw | **PWM mode for half-bridge 2 if PWM12MAP = 1**[3]<br>$0_B$ **INACTIVE**, PWM deactivated for HB2(default)<br>$1_B$ **ACTIVE**, PWM activated for HB2 |
| **HB1MODE** | 3:2 | rw | **Half-bridge 1 MODE selection**<br>$00_B$ **PASSIVE_OFF**, LS1 and HS1 are off by passive discharge (default)<br>$01_B$ **LS1_ON**, LS1 is ON<br>$10_B$ **HS1_ON**, HS1 is ON<br>$11_B$ **ACTIVE_OFF**, LS1 and HS1 kept off by the active discharge |
| **AFW1** | 1 | rw | **Active freewheeling for half-bridge 1 during PWM**<br>$0_B$ **DISABLED**, active freewheeling disabled<br>$1_B$ **ENABLED**, active freewheeling enabled (default) |
| **HB1_PWM_EN** | 0 | rw | **PWM mode for half-bridge 1 if PWM12MAP=0**[4]<br>$0_B$ **INACTIVE**, PWM deactivated for HB1 (default)<br>$1_B$ **ACTIVE**, PWM activated for HB1 |

1) If PWM34MAP = 0, HB4 is controlled statically according to HB4MODE independently from HB4_PWM_EN.
2) If PWM34MAP = 1, HB3 is controlled statically according to HB3MODE independently from HB3_PWM_EN.
3) If PWM12MAP = 0, HB2 is controlled statically according to HB2MODE independently from HB2_PWM_EN.
4) If PWM12MAP = 1, HB1 is controlled statically according to HB1MODE independently from HB1_PWM_EN.

**Table 52 Reset of HBMODE**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | $0010\ 0010\ 0010\ 0010_B$ | | | |
| Restart | $0010\ 0010\ 0010\ 0010_B$ | | | |

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### HB pre-charge and pre-discharge time

**TPRECHG**
**HB pre-charge and pre-discharge time** **(001 0110$_B$)** **Reset Value: see Table 53**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPCHG4 | | | TPCHG3 | | | TPCHG2 | | | TPCHG1 | | | RES | TPCHG_BNK | | |
| rw | | | rw | | | rw | | | rw | | | r | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **TPCHG4** | 15:13 | rw | **If TPCHG_BNK=0: precharge time of HB 4, If TPCHG_BNK=1: predischarge time of HB 4**<br>$000_B$ **107ns**, $t_{PCHG000}$ / $t_{PDCHG000}$ (default)<br>$001_B$ **160ns**, $t_{PCHG001}$ / $t_{PDCHG001}$<br>$010_B$ **214ns**, $t_{PCHG010}$ / $t_{PDCHG010}$<br>$011_B$ **267ns**, $t_{PCHG011}$ / $t_{PDCHG011}$<br>$100_B$ **320ns**, $t_{PCHG100}$ / $t_{PDCHG100}$<br>$101_B$ **533ns**, $t_{PCHG101}$ / $t_{PDCHG101}$<br>$110_B$ **747ns**, $t_{PCHG110}$ / $t_{PDCHG110}$<br>$111_B$ **1067ns**, $t_{PCHG111}$ / $t_{PDCHG111}$ |
| **TPCHG3** | 12:10 | rw | **If TPCHG_BNK=0: precharge time of HB 3, If TPCHG_BNK=1: predischarge time of HB 3**<br>$000_B$ **107ns**, $t_{PCHG000}$ / $t_{PDCHG000}$ (default)<br>$001_B$ **160ns**, $t_{PCHG001}$ / $t_{PDCHG001}$<br>$010_B$ **214ns**, $t_{PCHG010}$ / $t_{PDCHG010}$<br>$011_B$ **267ns**, $t_{PCHG011}$ / $t_{PDCHG011}$<br>$100_B$ **320ns**, $t_{PCHG100}$ / $t_{PDCHG100}$<br>$101_B$ **533ns**, $t_{PCHG101}$ / $t_{PDCHG101}$<br>$110_B$ **747ns**, $t_{PCHG110}$ / $t_{PDCHG110}$<br>$111_B$ **1067ns**, $t_{PCHG111}$ / $t_{PDCHG111}$ |
| **TPCHG2** | 9:7 | rw | **If TPCHG_BNK=0: precharge time of HB 2, If TPCHG_BNK=1: predischarge time of HB 2**<br>$000_B$ **107ns**, $t_{PCHG000}$ / $t_{PDCHG000}$ (default)<br>$001_B$ **160ns**, $t_{PCHG001}$ / $t_{PDCHG001}$<br>$010_B$ **214ns**, $t_{PCHG010}$ / $t_{PDCHG010}$<br>$011_B$ **267ns**, $t_{PCHG011}$ / $t_{PDCHG011}$<br>$100_B$ **320ns**, $t_{PCHG100}$ / $t_{PDCHG100}$<br>$101_B$ **533ns**, $t_{PCHG101}$ / $t_{PDCHG101}$<br>$110_B$ **747ns**, $t_{PCHG110}$ / $t_{PDCHG110}$<br>$111_B$ **1067ns**, $t_{PCHG111}$ / $t_{PDCHG111}$ |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **TPCHG1** | 6:4 | rw | **If TPCHG_BNK=0: precharge time of HB 1, If TPCHG_BNK=1: predischarge time of HB 1**<br>$000_B$ **107ns**, $t_{PCHG000}$ / $t_{PDCHG000}$ (default)<br>$001_B$ **160ns**, $t_{PCHG001}$ / $t_{PDCHG001}$<br>$010_B$ **214ns**, $t_{PCHG010}$ / $t_{PDCHG010}$<br>$011_B$ **267ns**, $t_{PCHG011}$ / $t_{PDCHG011}$<br>$100_B$ **320ns**, $t_{PCHG100}$ / $t_{PDCHG100}$<br>$101_B$ **533ns**, $t_{PCHG101}$ / $t_{PDCHG101}$<br>$110_B$ **747ns**, $t_{PCHG110}$ / $t_{PDCHG110}$<br>$111_B$ **1067ns**, $t_{PCHG111}$ / $t_{PDCHG111}$ |
| **RES** | 3 | r | **Reserved, always read as 0** |
| **TPCHG_BNK** | 2:0 | rw | **Precharge/predischarge time selection**<br>$000_B$ **PRECHARGE**, Precharge time selected (default)<br>$001_B$ **PREDISCHARGE**, Predischarge time selected<br>$x1x_B$ , wrong setting of TPCHG_BNK<br>$1xx_B$ , wrong setting of TPCHG_BNK |

**Table 53 Reset of TPRECHG**

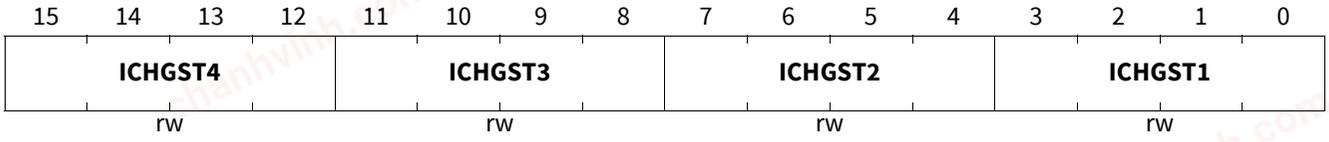
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | $0000\ 0000\ 0000\ 0000_B$ | | | |
| Restart | $xxxx\ xxxx\ xxxx\ 0000_B$ | | | |

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### Static charge/discharge current

**ST_ICHG**
**Static charge/discharge current** **(001 0111$_B$)** **Reset Value: see Table 54**




| Field | Bits | Type | Description |
|---|---|---|---|
| **ICHGST4** | 15:12 | rw | **Static charge and discharge currents of HB4**<br>Refer to **Table 22**<br>Default: 0100$_B$ - charge: $I_{CHG16}$, 9.2 mA typ., discharge $I_{DCHG16}$, 9.2 mA typ. |
| **ICHGST3** | 11:8 | rw | **Static charge and discharge currents of HB3**<br>Refer to **Table 22**<br>Default: 0100$_B$ - charge: $I_{CHG16}$, 9.2 mA typ., discharge: $I_{DCHG16}$, 9.2 mA typ. |
| **ICHGST2** | 7:4 | rw | **Static charge and discharge currents of HB2**<br>Refer to **Table 22**<br>Default: 0100$_B$ - charge: $I_{CHG16}$, 9.2 mA typ., discharge $I_{DCHG16}$, 9.2 mA typ. |
| **ICHGST1** | 3:0 | rw | **Static charge and discharge currents of HB1**<br>Refer to **Table 22**<br>Default: 0100$_B$ - charge: $I_{CHG16}$, 9.2 mA typ., discharge $I_{DCHG16}$, 9.2 mA typ. |

**Table 54 Reset of ST_ICHG**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0100 0100 0100 0100$_B$ | | | |
| Restart | xxxx xxxx xxxx xxxx$_B$ | | | |

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### HB charge/discharge currents for PWM operation

### HB_ICHG
### HB charge/discharge currents for PWM operation

(001 1000$_B$) **Reset Value: see Table 55**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IDCHG | | | | | | ICHG | | | | | | RES | ICHG_BNK | | |
| rw | | | | | | rw | | | | | | r | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **IDCHG** | 15:10 | rw | **If ICHG_BNK =0xx$_B$: Discharge current of HBx active MOSFET**<br>**If ICHG_BNK=1xx$_B$: Reserved. Always read as '0'**<br>Default value for all active MOSFETs discharge currents: 001111$_B$, $I_{DCHG15}$<br>Refer to **Table 25** for the configuration of the discharge current |
| **ICHG** | 9:4 | rw | **If ICHG_BNK=0xx$_B$: Charge current of HBx active MOSFET**<br>**If ICHG_BNK=1xx$_B$: Charge and discharge current of HBx FW MOSFETs**<br>Default value for all active MOSFETs charge currents and all FW MOSFETs charge/discharge currents: 001101$_B$, $I_{CHG13}$<br>Refer to **Table 24** for the configuration of the charge current of the active and FW MOSFET<br>Refer to **Table 25** for the configuration of the discharge current of the FW MOSFET |
| **RES** | 3 | r | **Reserved, always read as 0** |
| **ICHG_BNK** | 2:0 | rw | **Banking bits for charge and discharge currents of active MOSFETs**<br>000$_B$ **ACT_HB1**, Active MOSFET of HB1 is selected (default)<br>001$_B$ **ACT_HB2**, Active MOSFET of HB2 is selected<br>010$_B$ **ACT_HB3**, Active MOSFET of HB3 is selected<br>011$_B$ **ACT_HB4**, Active MOSFET of HB4 is selected<br>100$_B$ **FW_HB1**, FW MOSFET of HB1 is selected<br>101$_B$ **FW_HB2**, FW MOSFET of HB2 is selected<br>110$_B$ **FW_HB3**, FW MOSFET of HB3 is selected<br>111$_B$ **FW_HB4**, FW MOSFET of HB4 is selected |

**Table 55 Reset of HB_ICHG**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0011 1100 1101 0000$_B$ | | | POR value valid for ICHG_BNK = 0 |
| Restart | xxxx xxxx xxxx 0000$_B$ | | | |

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## HB max. pre-charge/pre-discharge in PWM operation current and diagnostic pull-down

### HB_ICHG_MAX

**HB max. pre-charge/pre-discharge in PWM operation current and diagnostic pull-down**

**(001 1001$_B$)** **Reset Value: see Table 56**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HB4IDIAG | HB3IDIAG | HB2IDIAG | HB1IDIAG | RES | | | | ICHGMAX4 | | ICHGMAX3 | | ICHGMAX2 | | ICHGMAX1 | |
| rw | rw | rw | rw | r | | | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HB4IDIAG** | 15 | rw | **Control of HB4 off-state current source and current sink**<br>$0_B$ **INACTIVE**, Pull-down deactivated (default)<br>$1_B$ **ACTIVE**, Pull-down activated |
| **HB3IDIAG** | 14 | rw | **Control of HB3 off-state current source and current sink**<br>$0_B$ **INACTIVE**, Pull-down deactivated (default)<br>$1_B$ **ACTIVE**, Pull-down activated |
| **HB2IDIAG** | 13 | rw | **Control of HB2 pull-down for off-state diagnostic**<br>$0_B$ **INACTIVE**, Pull-down deactivated (default)<br>$1_B$ **ACTIVE**, Pull-down activated |
| **HB1IDIAG** | 12 | rw | **Control of HB1 pull-down for off-state diagnostic**<br>$0_B$ **INACTIVE**, Pull-down deactivated (default)<br>$1_B$ **ACTIVE**, Pull-down activated |
| **RES** | 11:8 | r | **Reserved, always read as 0** |
| **ICHGMAX4** | 7:6 | rw | **Maximum drive current of HB4 during the pre-charge phase and pre-discharge phases**[1)]<br>$00_B$ **19mA**, charge $I_{CHG24}$: typ. 19.2 mA, discharge $I_{DCHG24}$: typ. 18.8 mA (default)<br>$01_B$ **32mA**, charge $I_{CHG32}$: typ. 32.8 mA, discharge $I_{DCHG32}$: typ. 32.2 mA<br>$10_B$ **73mA**, charge $I_{CHG52}$: typ. 73.2 mA, discharge $I_{DCHG52}$: typ. 72.4mA<br>$11_B$ **100mA**, charge $I_{CHG63}$: typ. 100 mA, discharge $I_{DCHG63}$: typ. 100 mA |
| **ICHGMAX3** | 5:4 | rw | **Maximum drive current of HB3 during the pre-charge and pre-discharge phases**[1)]<br>$00_B$ **19mA**, charge $I_{CHG24}$: typ. 19.2 mA, discharge $I_{DCHG24}$: typ. 18.8 mA (default)<br>$01_B$ **32mA**, charge $I_{CHG32}$: typ. 32.8 mA, discharge $I_{DCHG32}$: typ. 32.2 mA<br>$10_B$ **73mA**, charge $I_{CHG52}$: typ. 73.2 mA, discharge $I_{DCHG52}$: typ. 72.4mA<br>$11_B$ **100mA**, charge $I_{CHG63}$: typ. 100 mA, discharge $I_{DCHG63}$: typ. 100 mA |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **ICHGMAX2** | 3:2 | rw | **Maximum drive current of HB2 during the pre-charge phase and pre-discharge phases**[1)]<br>$00_B$ **19mA**, charge $I_{CHG24}$: typ. 19.2 mA, discharge $I_{DCHG24}$: typ. 18.8 mA (default)<br>$01_B$ **32mA**, charge $I_{CHG32}$: typ. 32.8 mA, discharge $I_{DCHG32}$: typ. 32.2 mA<br>$10_B$ **73mA**, charge $I_{CHG52}$: typ. 73.2 mA, discharge $I_{DCHG52}$: typ. 72.4mA<br>$11_B$ **100mA**, charge $I_{CHG63}$: typ. 100 mA, discharge $I_{DCHG63}$: typ. 100 mA |
| **ICHGMAX1** | 1:0 | rw | **Maximum drive current of HB1 during the pre-charge and pre-discharge phases**[1)]<br>$00_B$ **19mA**, charge $I_{CHG24}$: typ. 19.2 mA, discharge $I_{DCHG24}$: typ. 18.8 mA (default)<br>$01_B$ **32mA**, charge $I_{CHG32}$: typ. 32.8 mA, discharge $I_{DCHG32}$: typ. 32.2 mA<br>$10_B$ **73mA**, charge $I_{CHG52}$: typ. 73.2 mA, discharge $I_{DCHG52}$: typ. 72.4mA<br>$11_B$ **100mA**, charge $I_{CHG63}$: typ. 100 mA, discharge $I_{DCHG63}$: typ. 100 mA |

1) ICHGMAX is also the current applied during the post-charge of the PWM MOSFET.

**Table 56 Reset of HB_ICHG_MAX**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | $0000\ 0000\ 0000\ 0000_B$ | | | |
| Restart | $xxxx\ 0000\ xxxx\ xxxx_B$ | | | |

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### HBx pre-charge/pre-dischage initialization configuration in PWM operation

**HB_PCHG_INIT**
**HBx pre-charge/pre-discharge initialization configuration in PWM operation**
**(001 1010$_B$)** **Reset Value: see Table 57**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PDCHGINIT | | | | | | PCHGINIT | | | | | | RES | INIT_BNK | | |
| rw | | | | | | rw | | | | | | r | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **PDCHGINIT** | 15:10 | rw | **Initial predischarge current of HBx, IPDCHGINITx**<br>The INIT_BNK bits select the addressed half-bridge<br>Default: 001111$_B$<br>Refer to **Table 25** |
| **PCHGINIT** | 9:4 | rw | **Initial precharge current of HBx, IPCHGINITx**<br>The INIT_BNK bits select the addressed half-bridge<br>Default: 001101$_B$<br>Refer to **Table 24** |
| **RES** | 3 | r | **Reserved, always reads as 0** |
| **INIT_BNK** | 2:0 | rw | **Banking bits for Precharge an Predischarge Initial Current**<br>000$_B$ **HB1**, precharge/discharge init. for HB1 selected (default)<br>001$_B$ **HB2**, precharge/discharge init. for HB2 selected<br>010$_B$ **HB3**, precharge/discharge init. for HB3 selected<br>011$_B$ **HB4**, precharge/discharge init. for HB4 selected<br>1xx$_B$ , wrong setting of INIT_BANK |

**Table 57 Reset of HB_PCHG_INIT**

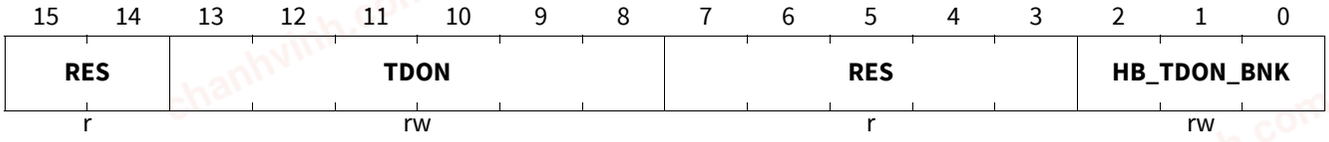
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0011 1100 1101 0000$_B$ | | | |
| Restart | xxxx xxxx xxxx 0000$_B$ | | | |

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### HBx inputs TDON configuration

**TDON_HB_CTRL**
**HBx inputs TDON configuration** **(001 1011$_B$)** **Reset Value: see Table 58**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always read as 0** |
| **TDON** | 13:8 | rw | **Turn-on delay time of active MOSFET of HBx**<br>The **HB_TDON_BNK** bits selects the turn-on delay time of the active MOSFET of the half-bridge HBx<br>Nominal tDON = 53.3 ns x TDON[5:0]$_D$<br>Default: 00 1100$_B$ : 640 ns typ. |
| **RES** | 7:3 | r | **Reserved, always read as 0** |
| **HB_TDON_BNK** | 2:0 | rw | **Banking bits for turn-on delay time**<br>000$_B$ **HB1**, tDON of HB1 selected (default)<br>001$_B$ **HB2**, tDON of HB2 selected<br>010$_B$ **HB3**, tDON of HB3 selected<br>011$_B$ **HB4**, tDON of HB4 selected<br>1xx$_B$ , wrong setting of PWM_TDON_BNK |

**Table 58 Reset of TDON_HB_CTRL**

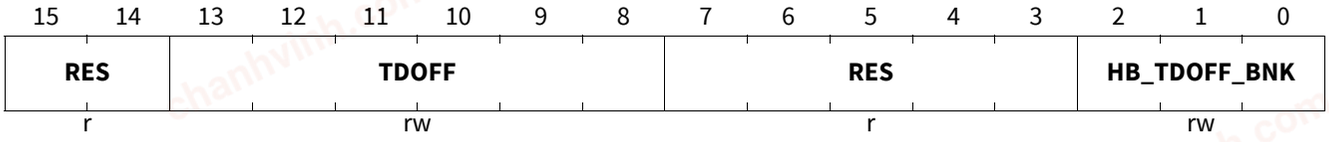
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 1100 0000 0000$_B$ | | | |
| Restart | 00xx xxxx 0000 0000$_B$ | | | |

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### HBx TDOFF configuration

**TDOFF_HB_CTRL**
**HBx TDOFF configuration** **(001 1100$_B$)** **Reset Value: see Table 59**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always read as 0** |
| **TDOFF** | 13:8 | rw | **Turn-off delay time of active MOSFET of HBx**<br>The **HB_TDOFF_BNK** bits selects the turn-off delay time of the active MOSFET of the half-bridge HBx<br>Nominal tDOFF = 53.3 ns x TDOFF[5:0]$_D$<br>Default: 0000 1100$_B$ : 640 ns |
| **RES** | 7:3 | r | **Reserved, always read as 0** |
| **HB_TDOFF_BNK** | 2:0 | rw | **Banking bits for turn-off delay time**<br>000$_B$ **HB1**, tDOFF of HB1 selected (default)<br>001$_B$ **HB2**, tDOFF of HB2 selected<br>010$_B$ **HB3**, tDOFF of HB3 selected<br>011$_B$ **HB4**, tDOFF of HB4 selected<br>1xx$_B$ , wrong setting of PWM_TDOFF_BNK |

**Table 59 Reset of TDOFF_HB_CTRL**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 1100 0000 0000$_B$ | | | |
| Restart | 00xx xxxx 0000 0000$_B$ | | | |

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## Brake control

### BRAKE
**Brake control** **(001 1101$_B$)** **Reset Value: see Table 60**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | SLAM_LS4_DIS | SLAM_LS3_DIS | SLAM_LS2_DIS | SLAM_LS1_DIS | SLAM | VDSTH_BRK | TBLK_BRK | PARK_BRK_EN | OV_BRK_EN | RES | | OV_BRK_TH | | |
| r | | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always read as 0** |
| **SLAM_LS4_DIS** | 13 | rw | **LS4 output disable during SLAM mode**<br>$0_B$ **ACTIVE**, LS4 control active in Slam mode (default)<br>$1_B$ **DISABLED**, LS4 control disabled in Slam mode |
| **SLAM_LS3_DIS** | 12 | rw | **LS3 output disable during SLAM mode**<br>$0_B$ **ACTIVE**, LS3 control active in Slam mode (default)<br>$1_B$ **DISABLED**, LS3 control disabled in Slam mode |
| **SLAM_LS2_DIS** | 11 | rw | **LS2 output disable during SLAM mode**<br>$0_B$ **ACTIVE**, LS2 control active in Slam mode (default)<br>$1_B$ **DISABLED**, LS2 control disabled in Slam mode |
| **SLAM_LS1_DIS** | 10 | rw | **LS1 output disable during SLAM mode**<br>$0_B$ **ACTIVE**, LS1 control active in Slam mode (default)<br>$1_B$ **DISABLED**, LS1 control disabled in Slam mode |
| **SLAM** | 9 | rw | **Slam mode**<br>$0_B$ **INACTIVE**, Slam mode deactivated (default)<br>$1_B$ **AVTIVE**, Slam mode activated |
| **VDSTH_BRK** | 8 | rw | **VDS Overvoltage for LS1-4 during braking**<br>$0_B$ **800mV**, $V_{VDSMONTH0_BRAKE}$, 0.8 V, typ. (default)<br>$1_B$ **220mV**, $V_{VDSMONTH1_BRAKE}$, 0.22 V typ. |
| **TBLK_BRK** | 7 | rw | **Blank time of VDS overvoltage during braking**<br>$0_B$ **7uS**, $t_{BLK_BRAKE1}$,7 µs typ.<br>$1_B$ **11uS**, $t_{BLK_BRAKE2}$, 11 µs typ. (default) |
| **PARK_BRK_EN** | 6 | rw | **Parking brake enable**<br>$0_B$ **DISABLED**, Parking brake disabled (default)<br>$1_B$ **ENABLED**, Parking brake enabled |
| **OV_BRK_EN** | 5 | rw | **Overvoltage brake enable**<br>$0_B$ **DISABLED**, Overvoltage brake disabled<br>$1_B$ **ENABLED**, Overvoltage brake enabled (default) |
| **RES** | 4:3 | rw | **Reserved, to be set to 0** |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **OV_BRK_TH** | 2:0 | rw | **Overvoltage brake threshold**<br>$000_B$ **27V**, typ. 27V (default)<br>$001_B$ **28V**, typ. 28V<br>$010_B$ **29V**, typ. 29V<br>$011_B$ **30V**, typ. 30V<br>$100_B$ **31V**, typ. 31V<br>$101_B$ **32V**, typ. 32V<br>$110_B$ **33V**, typ. 33V<br>$111_B$ **34V**, typ. 34V |

**Table 60 Reset of BRAKE**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | $0000\ 0000\ 1010\ 0000_B$ | | | |
| Restart | $00xx\ xxxx\ xxx0\ 0xxx_B$ | | | |

*Note: For min and max values of **OV_BRK_TH**, refer to **Chapter 13.12**.*

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## 14.6 SPI status information registers

READ/CLEAR Operation (see also **Chapter 14.3**):

- One 32-bit SPI command consist of four bytes:
  - The 7-bit address and one additional bit for the register access mode and
  - following the two data bytes and the CRC.
  The numbering of following bit definitions refers to the data byte and correspond to the bits D0...D7 and to the SPI bits 8...23 (see also figure).
- There are two different bit types:
  - 'r' = READ: read only bits (or reserved bits).
  - 'rc' = READ/CLEAR: readable and clearable bits.
- Reading a register is done word wise by setting the SPI bit 7 to "0" (= Read Only).
- Clearing a register is done word wise by setting the SPI bit 7 to "1". No single bits can be cleared. Therefore the content of a SPI message (bit 8..23) doesn't matter.
- SPI status registers are in general not cleared or changed automatically (an exception are the x bits). This must be done by the microcontroller via SPI command.

The registers are addressed wordwise.

**Table 61 Register Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| **SPI status information registers, Device Status Registers** | | | |
| **SUP_STAT** | Supply Voltage Fail Status | $1000000_B$ | **213** |
| **THERM_STAT** | Thermal Protection Status | $1000001_B$ | **215** |
| **DEV_STAT** | Device Information Status | $1000010_B$ | **216** |
| **BUS_STAT** | Bus Communication Status | $1000011_B$ | **218** |
| **WK_STAT** | Wake-up Source and Information Status | $1000100_B$ | **220** |
| **WK_LVL_STAT** | WK Input Level | $1000101_B$ | **222** |
| **HS_OL_OC_OT_STAT** | High-Side Switch Status | $1000110_B$ | **223** |
| **SPI status information registers, Status registers bridge driver** | | | |
| **GEN_STAT** | GEN Status register | $1010000_B$ | **225** |
| **TDREG** | Turn-on/off delay regulation register | $1010001_B$ | **227** |
| **DSOV** | Drain-source overvoltage HBVOUT | $1010010_B$ | **229** |
| **EFF_TDON_OFF1** | Effective MOSFET turn-on/off delay - PWM half-bridge 1 | $1010011_B$ | **231** |
| **EFF_TDON_OFF2** | Effective MOSFET turn-on/off delay - PWM half-bridge 2 | $1010100_B$ | **232** |
| **EFF_TDON_OFF3** | Effective MOSFET turn-on/off delay - PWM half-bridge 3 | $1010101_B$ | **233** |
| **EFF_TDON_OFF4** | Effective MOSFET turn-on/off delay - PWM half-bridge 4 | $1010110_B$ | **234** |
| **TRISE_FALL1** | MOSFET rise/fall time - PWM half-bridge 1 | $1010111_B$ | **235** |
| **TRISE_FALL2** | MOSFET rise/fall time - PWM half-bridge 2 | $1011000_B$ | **236** |
| **TRISE_FALL3** | MOSFET rise/fall time - PWM half-bridge 3 | $1011001_B$ | **237** |

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**Table 61 Register Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| TRISE_FALL4 | MOSFET rise/fall time - PWM half-bridge 4 | $1011010_B$ | 238 |
| **SPI status information registers, Family and product information register** | | | |
| FAM_PROD_STAT | Family and Product Identification Register | $1110000_B$ | 239 |

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### 14.6.1 Device Status Registers

**Supply Voltage Fail Status**

**SUP_STAT**
**Supply Voltage Fail Status** **(100 0000$_B$)** **Reset Value: see Table 62**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **POR** | **RES** | | **CP_OT** | **VCC1_UV_FS** | **HS_UV** | **HS_OV** | **VSINT_UV** | **VSINT_OV** | **VS_UV** | **VS_OV** | **CP_UV** | **VCC1_SC** | **VCC1_UV** | **VCC1_OV** | **VCC1_WARN** |
| rc | r | | rc | rc | rc | rc | rc | rc | rc | rc | rc | rc | rc | rc | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **POR** | 15 | rc | **Power-On reset detection**<br>$0_B$ **NO_POR**, No POR<br>$1_B$ **POR**, POR occurred |
| **RES** | 14:13 | r | **Reserved, always reads as 0** |
| **CP_OT** | 12 | rc | **Charge pump overtemperature**<br>$0_B$ **NO_CP_OT**, No charge pump OT detected<br>$1_B$ **CP_OT**, Charge pump OT detected |
| **VCC1_UV_FS** | 11 | rc | **4th consecutive VCC1 UV-Detection**<br>$0_B$ **NO_FAILSAFE**, No Fail-Safe Mode entry due to 4th consecutive VCC1_UV<br>$1_B$ **FAILSAFE**, Fail-Safe Mode entry due to 4th consecutive VCC1_UV |
| **HS_UV** | 10 | rc | **HS Supply UV-Detection**<br>$0_B$ **NO_UV**, No Undervoltage<br>$1_B$ **UV_EVENT**, HS Supply Undervoltage detected |
| **HS_OV** | 9 | rc | **HS Supply OV-Detection**<br>$0_B$ **NO_OV**, No Overvoltage<br>$1_B$ **OV_EVENT**, HS Supply Overvoltage detected |
| **VSINT_UV** | 8 | rc | **VSINT UV-Detection**<br>$0_B$ **NO_UV**, No Undervoltage<br>$1_B$ **UV_EVENT**, VSINT Undervoltage detected |
| **VSINT_OV** | 7 | rc | **VSINT OV-Detection**<br>$0_B$ **NO_OV**, No Overvoltage<br>$1_B$ **OV_EVENT**, VSINT Overvoltage detected |
| **VS_UV** | 6 | rc | **VS Undervoltage Detection ($V_{S,UV}$)**<br>$0_B$ **NO_VS**, No VS undervoltage detected<br>$1_B$ **VS_EVENT**, VS undervoltage detected (detection is only active when VCC1 is enabled) |
| **VS_OV** | 5 | rc | **VS Overvoltage Detection ($V_{S,OV}$)**<br>$0_B$ **NO_OV**, No VS overvoltage detected<br>$1_B$ **OV_EVENT**, VS overvoltage detected (detection is only active when VCC1 is enabled) |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **CP_UV** | 4 | rc | **CP_UV**<br>$0_B$ **NO_UV**, No CP undervoltage detected<br>$1_B$ **UV_EVENT**, CP undervoltage detected |
| **VCC1_SC** | 3 | rc | **VCC1 SC**<br>$0_B$ **NO_SC**, No VCC1 short to GND detected<br>$1_B$ **SC_EVENT**, VCC1 short to GND |
| **VCC1_UV** | 2 | rc | **VCC1 UV-Detection (due to Vrtx reset)**<br>$0_B$ **NO_UV**, No VCC1_UV detection<br>$1_B$ **UV_EVENT**, VCC1 undervoltage detected |
| **VCC1_OV** | 1 | rc | **VCC1 Overvoltage Detection**<br>$0_B$ **NO_OV**, No VCC1 overvoltage warning<br>$1_B$ **OV_EVENT**, VCC1 overvoltage detected |
| **VCC1_WARN** | 0 | rc | **VCC1 Undervoltage Prewarning**<br>$0_B$ **NO_UV**, No VCC1 undervoltage prewarning<br>$1_B$ **UV_PREWARN**, VCC1 undervoltage prewarning detected |

**Table 62 Reset of SUP_STAT**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | y000 0000 0000 $0000_B$ | | | |
| Restart | x00x xxxx xxxx $xxxx_B$ | | | |

**Notes**

1. *The VCC1 undervoltage prewarning threshold $V_{PW,f}$ / $V_{PW,r}$ is a fixed threshold and independent of the VCC1 undervoltage reset thresholds.*
2. *VSINT undervoltage monitoring is not available in Stop Mode due to current consumption saving requirements. Exception: VSINT undervoltage detection is also available in Stop Mode if the VCC1 load current is above the active peak threshold (I_PEAK_TH) or if VCC1 is below the VCC1 prewarning threshold (**VCC1_WARN** is set).*
3. *The MSB of the POR/Soft Reset value is marked as 'y': the default value of the POR bit is set after Power-on reset (POR value = 1000 0000). However it will be cleared after a device Soft Reset command (Soft Reset value = 0000 0000).*
4. *During Sleep Mode, the bits VCC1_SC, VCC1_OV and VCC1_UV will not be set when VCC1 is off.*
5. *The VCC1_UV bit is never updated in Restart Mode, in Init Mode it is only updated after RSTN was released, it is always updated in Normal Mode and Stop Mode, and it is always updated in any device modes in a VCC1_SC condition (after VCC1_UV = 1 for > 2 ms).*

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### Thermal Protection Status

**THERM_STAT**
**Thermal Protection Status** **(100 0001$_B$)** **Reset Value: see Table 63**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | | | | | | | | | | | TSD2_SAFE | TSD2 | TSD1 | TPW |
| r | | | | | | | | | | | | rc | rc | rc | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:4 | r | **Reserved, always reads as 0** |
| **TSD2_SAFE** | 3 | rc | **TSD2 Thermal Shut-Down Safe State Detection**<br>$0_B$ **NO_TSD2_SF**, No TSD2 safe state detected<br>$1_B$ **TSD2_SF**, TSD2 safe state detected: >16 consecutive TSD2 events occurred, next TSD2 waiting time will be 64s |
| **TSD2** | 2 | rc | **TSD2 Thermal Shut-Down Detection**<br>$0_B$ **NO_TSD2**, No TSD2 event<br>$1_B$ **TSD2_EVENT**, TSD2 OT detected - leading to Fail-Safe Mode |
| **TSD1** | 1 | rc | **TSD1 Thermal Shut-Down Detection**<br>$0_B$ **NO_TSD1**, No TSD1 fail<br>$1_B$ **TSD1_EVENT**, TSD1 OT detected (affected module is disabled) |
| **TPW** | 0 | rc | **Thermal Pre Warning**<br>$0_B$ **NO_TPW**, No Thermal Pre warning<br>$1_B$ **TPW**, Thermal Pre warning detected |

**Table 63 Reset of THERM_STAT**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 0000 0000 0000 xxxx$_B$ | | | |

*Note: Temperature warning and shutdown bits are not reset automatically, even if the temperature pre warning or the TSD condition is not present anymore.*

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### Device Information Status

**DEV_STAT**
**Device Information Status** **(100 0010$_B$)** **Reset Value: see Table 64**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | | | | | CRC_STAT | CRC_FAIL | DEV_STAT | | RES | SW_DEV | WD_FAIL | | SPI_FAIL | FAILURE |
| r | | | | | | r | rc | rc | | r | rh | rh | | rc | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:10 | r | **Reserved, always read as 0** |
| **CRC_STAT** | 9 | r | **CRC STAT Information**<br>$0_B$ **DISABLED**, CRC disabled<br>$1_B$ **ENABLED**, CRC enabled |
| **CRC_FAIL** | 8 | rc | **CRC Fail Information**[1)]<br>$0_B$ **NO_FAIL**, No CRC Failure<br>$1_B$ **FAIL**, CRC Failure detected |
| **DEV_STAT** | 7:6 | rc | **Device Status before Restart Mode**<br>$00_B$ **CLEARED**, Cleared (Register must be actively cleared)<br>$01_B$ **RESTART**, Restart due to failure (WD fail, TSD2, VCC1_UV, trial to access Sleep Mode without any wake source activated); also after a wake from Fail-Safe Mode<br>$10_B$ **SLEEP**, Sleep Mode<br>$11_B$ , reserved |
| **RES** | 5 | r | **Reserved, always reads 0** |
| **SW_DEV** | 4 | rh | **Status of Operating Mode**<br>$0_B$ **NORMAL**, Normal operation<br>$1_B$ **SW_DEV**, Software Development Mode is enabled |
| **WD_FAIL** | 3:2 | rh | **Number of WD-Failure Events**<br>$00_B$ **NO_FAIL**, No WD Fail<br>$01_B$ **1x**, 1x WD Fail,<br>$10_B$ **2x**, 2x WD Fail<br>$11_B$ **3x**, more than 3xWD Fail |
| **SPI_FAIL** | 1 | rc | **SPI Fail Information**<br>$0_B$ **NO_FAIL**, No SPI fail<br>$1_B$ **INVALID**, Invalid SPI command detected |
| **FAILURE** | 0 | rc | **Failure detection**<br>$0_B$ **NO_FAIL**, No Failure<br>$1_B$ **FAIL**, Failure occured |

1) The CRC_FAIL bit will not be set in case the static CRC enabling / disabling sequence is sent (see **Chapter 5.2**).

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**Table 64 Reset of DEV_STAT**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | $0000\ 0000\ 0000\ 0000_B$ | | | |
| Restart | $0000\ 00xx\ xx0x\ xxxx_B$ | | | |

**Notes**

1. *The bits **DEV_STAT** show the status of the device before exiting Restart Mode. Either the device came from regular Sleep Mode or a failure (Restart Mode or Fail-Safe Mode) occurred. Coming from Sleep Mode will also be shown if there was a trial to enter Sleep Mode without having cleared all wake flags before.*
2. *The **WD_FAIL** bits are implemented as a counter and are the only status bits, which are cleared automatically by the device.*
3. *The SPI_FAIL bit can only be cleared via SPI command.*
4. *The bit **CRC_STAT** and **CRC_FAIL** can be read regardless the CRC setting. The SPI read command on **DEV_STAT** ignores the CRC field.*

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### Bus Communication Status

**BUS_STAT**
**Bus Communication Status** **(100 0011$_B$)** **Reset Value: see Table 65**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | | | | | | | | LIN_FAIL | | CANTO | SYSERR | CAN_FAIL | | VCAN_UV |
| r | | | | | | | | | rc | | rc | rc | rc | | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:7 | r | **Reserved, always reads as 0** |
| **LIN_FAIL** | 6:5 | rc | **LIN failure status**<br>$00_B$ **NO_FAIL**, No failures<br>$01_B$ **LIN_TSD**, LIN Thermal shutdown<br>$10_B$ **LIN_TXD_DOM_TO**, LIN_TXD_DOM: detected a TXDLIN dominant timeout<br>$11_B$ **LIN_BUS_DOM_TO**, LIN_BUS_DOM: detected a LIN dominant timeout |
| **CANTO** | 4 | rc | **CAN Time Out Detection**<br>$0_B$ **NO_FAIL**, Normal operation<br>$1_B$ **TIME_OUT**, CAN Time Out detected |
| **SYSERR** | 3 | rc | **SWK System Error**<br>$0_B$ **NO_FAIL**, Selective Wake Mode is possible<br>$1_B$ **FAIL**, System Error detected, SWK enabling not possible |
| **CAN_FAIL** | 2:1 | rc | **CAN failure status**<br>$00_B$ **NO_ERR**, No error<br>$01_B$ **CAN_TSD**, CAN Thermal shutdown<br>$10_B$ **CAN_TXD_DOM_TO**, CAN_TXD_DOM: TXD dominant time out detected<br>$11_B$ **CAN_BUS_DOM_TO**, CAN_BUS_DOM: BUS dominant time out detected |
| **VCAN_UV** | 0 | rc | **Under Voltage CAN Bus Supply**<br>$0_B$ **NORMAL**, Normal operation<br>$1_B$ **UNDERVOLTAGE**, CAN Supply undervoltage detected. Transmitter disabled |

**Table 65 Reset of BUS_STAT**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 0000 0000 0xxx xxxx$_B$ | | | |

**Notes**

1. *The VCAN_UV comparator is enabled if CAN Normal or CAN Receive Only Mode.*

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2. *CANTO will be set only if CAN2 = 1 (=SWK Mode enabled). It will be set as soon as CANSIL was set and will stay set even in CANSIL it is reset. An interrupt is issued in Stop Mode and Normal Mode as soon as CANTO is set and the interrupt is not masked out, i.e. CANTO_MASK must be set to 1.*
3. *The SYSERR Flag is set in case of a configuration error and in case of an error counter overflow (n > 32) It is only updated if SWK is enabled (CAN_2 = '1'). See also chapter x.*
4. *CANTO is set asynchronously to the INTN pulse. In order to prevent undesired clearing of CANTO and thus possibly missing this interrupt, the bit will be prevented from clearing (i.e. cannot be cleared) until the next falling edge of INTN.*

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### Wake-up Source and Information Status

**WK_STAT**
**Wake-up Source and Information Status** **(100 0100$_B$)** **Reset Value: see Table 66**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | | | | LIN_WU | CAN_WU | TIMER2_WU | TIMER1_WU | RES | | RES | WK4_WU | WK3_WU | WK2_WU | WK1_WU |
| r | | | | | rc | rc | rc | rc | r | | r | rc | rc | rc | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:11 | r | **Reserved, always reads as 0** |
| **LIN_WU** | 10 | rc | **LIN wake up**<br>$0_B$ **NO_WU**, No Wake up<br>$1_B$ **WU**, Wake up detected |
| **CAN_WU** | 9 | rc | **Wake up via CAN Bus**<br>$0_B$ **NO_WU**, No Wake up<br>$1_B$ **WU**, Wake up detected |
| **TIMER2_WU** | 8 | rc | **Wake up via Timer2**<br>$0_B$ **NO_WU**, No Wake up<br>$1_B$ **WU**, Wake up detected |
| **TIMER1_WU** | 7 | rc | **Wake up via Timer1**<br>$0_B$ **NO_WU**, No Wake up<br>$1_B$ **WU**, Wake up detected |
| **RES** | 6:5 | r | **Reserved, always reads as 0** |
| **RES** | 4 | r | **Reserved, always reads as 0** |
| **WK4_WU** | 3 | rc | **Wake up via WK4**<br>$0_B$ **NO_WU**, No Wake up<br>$1_B$ **WU**, Wake up detected |
| **WK3_WU** | 2 | rc | **Wake up via WK3**<br>$0_B$ **NO_WU**, No Wake up<br>$1_B$ **WU**, Wake up detected |
| **WK2_WU** | 1 | rc | **Wake up via WK2**<br>$0_B$ **NO_WU**, No Wake up<br>$1_B$ **WU**, Wake up detected |
| **WK1_WU** | 0 | rc | **Wake up via WK1**<br>$0_B$ **NO_WU**, No Wake up<br>$1_B$ **WU**, Wake up detected |

**Table 66 Reset of WK_STAT**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 0000 0xxx x000 00x0$_B$ | | | |

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*Note: At Fail-Safe Mode entry, the **WK_STAT** register is automatically cleared by the device.*

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### WK Input Level

**WK_LVL_STAT**
**WK Input Level** **(100 0101$_B$)** **Reset Value: see Table 67**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | | | | | | | | | | RES | WK4_LVL | WK3_LVL | WK2_LVL | WK1_LVL |
| r | | | | | | | | | | | r | r | r | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:5 | r | **Reserved, always reads as 0** |
| **RES** | 4 | r | **Reserved, always reads as 0** |
| **WK4_LVL** | 3 | r | **Status of WK4**<br>$0_B$ **LOW**, Low Level (=0)<br>$1_B$ **HIGH**, High Level (=1) |
| **WK3_LVL** | 2 | r | **Status of WK3**<br>$0_B$ **LOW**, Low Level (=0)<br>$1_B$ **HIGH**, High Level (=1) |
| **WK2_LVL** | 1 | r | **Status of WK2**<br>$0_B$ **LOW**, Low Level (=0)<br>$1_B$ **HIGH**, High Level (=1) |
| **WK1_LVL** | 0 | r | **Status of WK1**<br>$0_B$ **LOW**, Low Level (=0)<br>$1_B$ **HIGH**, High Level (=1) |

**Table 67 Reset of WK_LVL_STAT**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 00x0$_B$ | | | |
| Restart | 0000 0000 0000 00x0$_B$ | | | |

*Note: WK_LVL_STAT is updated in Normal Mode and Stop Mode and also in Init and Restart Mode. In cyclic sense or wake mode, the registers contain the sampled level, i.e. the registers are updated after every sampling.*

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## High-Side Switch Status

### HS_OL_OC_OT_STAT

**High-Side Switch Status** **(100 0110$_B$)** **Reset Value: see Table 68**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | HS4_OT | HS3_OT | HS2_OT | HS1_OT | RES | HS4_OL | HS3_OL | HS2_OL | HS1_OL | RES | HS4_OC | HS3_OC | HS2_OC | HS1_OC |
| r | | rc | rc | rc | rc | r | rc | rc | rc | rc | r | rc | rc | rc | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always reads as 0** |
| **HS4_OT** | 13 | rc | **Overtemperature Detection on HS4**<br>$0_B$ **NO_OT**, No OT<br>$1_B$ **OT**, OT detected |
| **HS3_OT** | 12 | rc | **Overtemperature Detection on HS3**<br>$0_B$ **NO_OT**, No OT<br>$1_B$ **OT**, OT detected |
| **HS2_OT** | 11 | rc | **Overtemperature Detection on HS2**<br>$0_B$ **NO_OT**, No OT<br>$1_B$ **OT**, OT detected |
| **HS1_OT** | 10 | rc | **Overtemperature Detection on HS1**<br>$0_B$ **NO_OT**, No OT<br>$1_B$ **OT**, OT detected |
| **RES** | 9 | r | **Reserved, always reads as 0** |
| **HS4_OL** | 8 | rc | **Open-Load Detection on HS4**<br>$0_B$ **NO_OL**, No OL<br>$1_B$ **OL**, OL detected |
| **HS3_OL** | 7 | rc | **Open-Load Detection on HS3**<br>$0_B$ **NO_OL**, No OL<br>$1_B$ **OL**, OL detected |
| **HS2_OL** | 6 | rc | **Open-Load Detection on HS2**<br>$0_B$ **NO_OL**, No OL<br>$1_B$ **OL**, OL detected |
| **HS1_OL** | 5 | rc | **Open-Load Detection on HS1**<br>$0_B$ **NO_OL**, No OL<br>$1_B$ **OL**, OL detected |
| **RES** | 4 | r | **Reserved, always reads as 0** |
| **HS4_OC** | 3 | rc | **Overcurrent Detection on HS4**<br>$0_B$ **NO_OC**, No OC<br>$1_B$ **OC**, OC detected |
| **HS3_OC** | 2 | rc | **Overcurrent Detection on HS3**<br>$0_B$ **NO_OC**, No OC<br>$1_B$ **OC**, OC detected |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **HS2_OC** | 1 | rc | **Overcurrent Detection on HS2**<br>$0_B$ **NO_OC**, No OC<br>$1_B$ **OC**, OC detected |
| **HS1_OC** | 0 | rc | **Overcurrent Detection on HS1**<br>$0_B$ **NO_OC**, No OC<br>$1_B$ **OC**, OC detected |

**Table 68 Reset of HS_OL_OC_OT_STAT**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 $0000_B$ | | | |
| Restart | 00xx xxxx xxxx $xxxx_B$ | | | |

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## 14.6.2 Status registers bridge driver

### General Status register

**GEN_STAT**
**General Status register** **(101 0000$_B$)** **Reset Value: see Table 69**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | | | | | HB4V OUT | HB3V OUT | HB2V OUT | HB1V OUT | RES | RES | RES | PWM3 STAT | RES | PWM1 STAT |
| r | | | | | | r | r | r | r | r | r | r | r | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:10 | r | **Reserved, always reads as 0** |
| **HB4VOUT** | 9 | r | **Voltage level at VSH4 when HB4MODE[1:0] = 11 and CPEN=1**[1)]<br>$0_B$ **LOW**, VSH4 = Low : VS - VSH4 > $V_{HS4VDSTHx}$<br>$1_B$ **HIGH**, VSH4 = High: VS - VSH4 ≤ $V_{HS4VDSTHx}$ |
| **HB3VOUT** | 8 | r | **Voltage level at VSH3 when HB3MODE[1:0] = 11 and CPEN=1**[1)]<br>$0_B$ **LOW**, VSH3 = Low : VS - VSH3 > $V_{HS3VDSTHx}$<br>$1_B$ **HIGH**, VSH3 = High: VS - VSH3 ≤ $V_{HS3VDSTHx}$ |
| **HB2VOUT** | 7 | r | **Voltage level at VSH2 when HB2MODE[1:0] = 11 and CPEN=1**[1)]<br>$0_B$ **LOW**, VSH2 = Low : VS - VSH2 > $V_{HS2VDSTHx}$<br>$1_B$ **HIGH**, VSH2 = High: VS - VSH2 ≤ $V_{HS2VDSTHx}$ |
| **HB1VOUT** | 6 | r | **Voltage level at VSH1 when HB1MODE[1:0] = 11 and CPEN=1**[1)]<br>$0_B$ **LOW**, VSH1 = Low : VS - VSH1 > $V_{HS1VDSTHx}$<br>$1_B$ **HIGH**, VSH1 = High: VS - VSH1 ≤ $V_{HS1VDSTHx}$ |
| **RES** | 5 | r | **Reserved, always reads as 0** |
| **RES** | 4 | r | **Reserved, always reads as 0** |
| **RES** | 3 | r | **Reserved, always reads as 0** |
| **PWM3STAT** | 2 | r | **PWM3 status**<br>$0_B$ **LOW**, PWM3 is Low<br>$1_B$ **HIGH**, PWM3 is High |
| **RES** | 1 | r | **Reserved, always reads as 0** |
| **PWM1STAT** | 0 | r | **PWM1/CRC status**<br>$0_B$ **LOW**, PWM1/CRC is Low<br>$1_B$ **HIGH**, PWM1/CRC is High |

1) HBxVOUT = 0 if (**CPEN**=1 and HBxMODE ≠ 11) or **CPEN**=0.

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**Table 69 Reset of GEN_STAT**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 $0000_B$ | | | |
| Restart | 0000 0000 xx00 $000x_B$ | | | |

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### Turn-on/off delay regulation register

**TDREG**
**Turn-on/off delay regulation register** **(101 0001$_B$)** **Reset Value: see Table 70**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | | | IPDCHG4_ST | IPDCHG3_ST | IPDCHG2_ST | IPDCHG1_ST | IPCHG4_ST | IPCHG3_ST | IPCHG2_ST | IPCHG1_ST | TDREG4 | TDREG3 | TDREG2 | TDREG1 |
| r | | | | r | r | r | r | r | r | r | r | r | r | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:12 | r | **Reserved, always reads as 0** |
| **IPDCHG4_ST** | 11 | r | **HB4 predischarge status**<br>$0_B$ **CLAMP**, the predischarge current is equal to 0.5 mA typ. or ICHGMAX4 if AGC[1:0] = $10_B$ or $11_B$, and HB4_PWM_EN = 1[1)]<br>$1_B$ **NO_CLAMP**, 0.5 mA < predischarge current < ICHGMAX4[1)] |
| **IPDCHG3_ST** | 10 | r | **HB3 predischarge status**<br>$0_B$ **CLAMP**, the predischarge current is equal to 0.5 mA typ. or ICHGMAX3 if AGC[1:0] = $10_B$ or $11_B$, and HB3_PWM_EN = 1[1)]<br>$1_B$ **NO_CLAMP**, 0.5 mA < predischarge current < ICHGMAX3[1)] |
| **IPDCHG2_ST** | 9 | r | **HB2 predischarge status**<br>$0_B$ **CLAMP**, the predischarge current is equal to 0.5 mA typ. or ICHGMAX2 if AGC[1:0] = $10_B$ or $11_B$, and HB2_PWM_EN = 1[1)]<br>$1_B$ **NO_CLAMP**, 0.5 mA < predischarge current < ICHGMAX2[1)] |
| **IPDCHG1_ST** | 8 | r | **HB1 predischarge status**<br>$0_B$ **CLAMP**, the predischarge current is equal to the 0.5 mA typ. or ICHGMAX1 if AGC[1:0] = $10_B$ or $11_B$, and HBx_PWM_EN = 1[1)]<br>$1_B$ **NO_CLAMP**, 0.5 mA < predischarge current < ICHGMAX1[1)] |
| **IPCHG4_ST** | 7 | r | **HB4 discharge status**<br>$0_B$ **CLAMP**, the discharge current is equal to 0.5 mA typ. or ICHGMAX4 if AGC[1:0] = $10_B$ or $11_B$, and HB4_PWM_EN = 1[1)]<br>$1_B$ **NO_CLAMP**, 0.5 mA < discharge current < ICHGMAX4[1)] |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **IPCHG3_ST** | 6 | r | **HB3 precharge status**<br>$0_B$ **CLAMP**, the precharge current is equal to 0.5 mA typ. or ICHGMAX3 if AGC[1:0] = $10_B$ or $11_B$, and HB3_PWM_EN = 1[1)]<br>$1_B$ **NO_CLAMP**, 0.5 mA < precharge current < ICHGMAX3[1)] |
| **IPCHG2_ST** | 5 | r | **HB2 precharge status**<br>$0_B$ **CLAMP**, the precharge current is equal to 0.5 mA typ. or ICHGMAX2 if AGC[1:0] = $10_B$ or $11_B$, and HB2_PWM_EN = 1[1)]<br>$1_B$ **NO_CLAMP**, 0.5 mA < precharge current < ICHGMAX2[1)] |
| **IPCHG1_ST** | 4 | r | **HB1 precharge status**<br>$0_B$ **CLAMP**, the precharge current is equal to the 0.5 mA typ. or ICHGMAX1 if AGC[1:0] = $10_B$ or $11_B$, and HB1_PWM_EN = 1[1)]<br>$1_B$ **NO_CLAMP**, 0.5 mA < precharge current < ICHGMAX1[1)] |
| **TDREG4** | 3 | r | **HB4 Regulation of turn-on/off delay**<br>$0_B$ **NO_REG**, tDON4 and tDOFF4 are not in regulation<br>$1_B$ **REG**, tDON4 and/or tDOFF4 are in regulation |
| **TDREG3** | 2 | r | **HB3 Regulation of turn-on/off delay**<br>$0_B$ **NO_REG**, tDON3 and tDOFF3 are not in regulation<br>$1_B$ **REG**, tDON3 and/or tDOFF3 are in regulation |
| **TDREG2** | 1 | r | **HB2 Regulation of turn-on/off delay**<br>$0_B$ **NO_REG**, tDON2 and tDOFF2 are not in regulation<br>$1_B$ **REG**, tDON2 and/or tDOFF2 are in regulation |
| **TDREG1** | 0 | r | **HB1 Regulation of turn-on/off delay**<br>$0_B$ **NO_REG**, tDON and tDOFF are not in regulation<br>$1_B$ **REG**, tDON and/or tDOFF are in regulation |

1) IPCHGx_ST = 1 otherwise (PWM disabled, HB in high impedance or AGC[1:0] = $00_B$ or $01_B$ ).

**Table 70 Reset of TDREG**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 $0000_B$ | | | |
| Restart | 0000 0000 xx00 $000x_B$ | | | |

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### Drain-source overvoltage status

**DSOV**
**Drain-source overvoltage** **(101 0010$_B$)** **Reset Value: see Table 71**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | RES | VSINTOVBRAKE_ST | VSOVBRAKE_ST | LS4DSOV_BRK | LS3DSOV_BRK | LS2DSOV_BRK | LS1DSOV_BRK | LS4DSOV | HS4DSOV | LS3DSOV | HS3DSOV | LS2DSOV | HS2DSOV | LS1DSOV | HS1DSOV |
| r | r | rc | rc | rc | rc | rc | rc | rc | rc | rc | rc | rc | rc | rc | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15 | r | **Reserved, always reads as 0** |
| **RES** | 14 | r | **Reserved, always reads as 0** |
| **VSINTOVBRAKE_ST** | 13 | rc | **VSINT Brake status**<br>$0_B$ **NOT_DETECT**, VSINT overvoltage brake condition is not detected<br>$1_B$ **DETECT**, VSINT overvoltage brake conditions is detected |
| **VSOVBRAKE_ST** | 12 | rc | **VS Brake status**<br>$0_B$ **NOT_DETECT**, VS overvoltage brake conditions is not detected<br>$1_B$ **DETECT**, VS overvoltage brake conditions is detected |
| **LS4DSOV_BRK** | 11 | rc | **Drain-source overvoltage on low-side 4 during braking**<br>$0_B$ **NO_OV**, No drain-source overvoltage on LS4<br>$1_B$ **OV**, Drain-source overvoltage on LS4 |
| **LS3DSOV_BRK** | 10 | rc | **Drain-source overvoltage on low-side 3 during braking**<br>$0_B$ **NO_OV**, No drain-source overvoltage on LS3<br>$1_B$ **OV**, Drain-source overvoltage on LS3 |
| **LS2DSOV_BRK** | 9 | rc | **Drain-source overvoltage on low-side 2 during braking**<br>$0_B$ **NO_OV**, No drain-source overvoltage on LS2<br>$1_B$ **OV**, Drain-source overvoltage on LS2 |
| **LS1DSOV_BRK** | 8 | rc | **Drain-source overvoltage on low-side 1 during braking**<br>$0_B$ **NO_OV**, No drain-source overvoltage on LS1<br>$1_B$ **OV**, Drain-source overvoltage on LS1 |
| **LS4DSOV** | 7 | rc | **Drain-source overvoltage on low-side 4**<br>$0_B$ **NO_OV**, No drain-source overvoltage on LS4<br>$1_B$ **OV**, Drain-source overvoltage on LS4 |
| **HS4DSOV** | 6 | rc | **Drain-source overvoltage on high-side 4**<br>$0_B$ **NO_OV**, No drain-source overvoltage on HS4<br>$1_B$ **OV**, Drain-source overvoltage on HS4 |

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| Field | Bits | Type | Description |
|---|---|---|---|
| **LS3DSOV** | 5 | rc | **Drain-source overvoltage on low-side 3**<br>$0_B$ **NO_OV**, No drain-source overvoltage on LS3<br>$1_B$ **OV**, Drain-source overvoltage on LS3 |
| **HS3DSOV** | 4 | rc | **Drain-source overvoltage on high-side 3**<br>$0_B$ **NO_OV**, No drain-source overvoltage on HS3<br>$1_B$ **OV**, Drain-source overvoltage on HS3 |
| **LS2DSOV** | 3 | rc | **Drain-source overvoltage on low-side 2**<br>$0_B$ **NO_OV**, No drain-source overvoltage on LS2<br>$1_B$ **OV**, Drain-source overvoltage on LS2 |
| **HS2DSOV** | 2 | rc | **Drain-source overvoltage on high-side 2**<br>$0_B$ **NO_OV**, No drain-source overvoltage on HS2<br>$1_B$ **OV**, Drain-source overvoltage on HS2 |
| **LS1DSOV** | 1 | rc | **Drain-source overvoltage on low-side 1**<br>$0_B$ **NO_OV**, No drain-source overvoltage on LS1<br>$1_B$ **OV**, Drain-source overvoltage on LS1 |
| **HS1DSOV** | 0 | rc | **Drain-source overvoltage on high-side 1**<br>$0_B$ **NO_OV**, No drain-source overvoltage on HS1<br>$1_B$ **OV**, Drain-source overvoltage on HS1 |

**Table 71 Reset of DSOV**

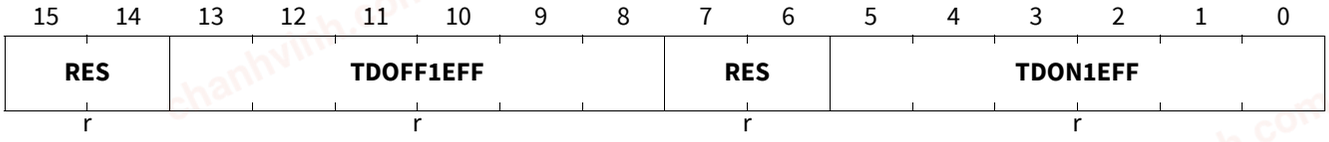
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 $0000_B$ | | | |
| Restart | 00xx xxxx xxxx $xxxx_B$ | | | |

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### Effective MOSFET turn.on/off delay - PWM half-bridge 1

**EFF_TDON_OFF1**
**Effective MOSFET turn.on/off delay - HB1 (101 0011$_B$)** **Reset Value: see Table 72**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always reads as 0** |
| **TDOFF1EFF** | 13:8 | r | **Effective active MOSFET turn-off delay HB1**<br>Nominal effective tDOFF1 = 53.3 ns x TDOFF1EFF[13:8]$_D$ |
| **RES** | 7:6 | r | **Reserved, always reads as 0** |
| **TDON1EFF** | 5:0 | r | **Effective active MOSFET turn-on delay HB1**<br>Nominal effective tDON1 = 53.3 ns x TDON1EFF[5:0]$_D$ |

**Table 72 Reset of EFF_TDON_OFF1**

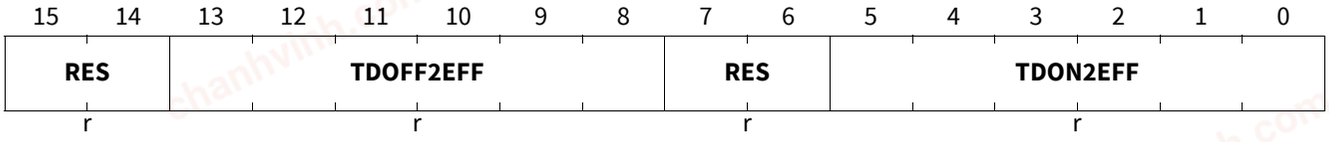
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 00xx xxxx 00xx xxxx$_B$ | | | |

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### Effective MOSFET turn.on/off delay - PWM half-bridge 2

**EFF_TDON_OFF2**
**Effective MOSFET turn.on/off delay - HB 2 (101 0100$_B$)** **Reset Value: see Table 73**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always reads as 0** |
| **TDOFF2EFF** | 13:8 | r | **Effective active MOSFET turn-off delay HB2**<br>Nominal effective tDOFF2 = 53.3 ns x TDOFF2EFF[13:8]$_D$ |
| **RES** | 7:6 | r | **Reserved, always reads as 0** |
| **TDON2EFF** | 5:0 | r | **Effective active MOSFET turn-on delay HB2**<br>Nominal effective tDON2 = 53.3 ns x TDON2EFF[5:0]$_D$ |

**Table 73 Reset of EFF_TDON_OFF2**

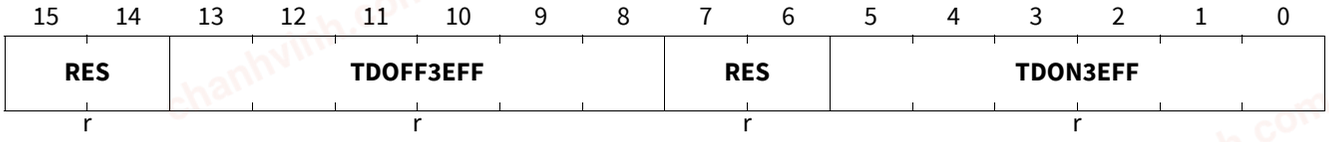
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 00xx xxxx 00xx xxxx$_B$ | | | |

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### Effective MOSFET turn.on/off delay - PWM half-bridge 3

**EFF_TDON_OFF3**
**Effective MOSFET turn.on/off delay - HB3 (101 0101$_B$)** **Reset Value: see Table 74**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always reads as 0** |
| **TDOFF3EFF** | 13:8 | r | **Effective active MOSFET turn-off delay HB3**<br>Nominal effective tDOFF3 = 53.3 ns x TDO3EFF[13:8]$_D$ |
| **RES** | 7:6 | r | **Reserved, always reads as 0** |
| **TDON3EFF** | 5:0 | r | **Effective active MOSFET turn-on delay HB3**<br>Nominal effective tDON3 = 53.3 ns x TDON3EFF[5:0]$_D$ |

**Table 74 Reset of EFF_TDON_OFF3**

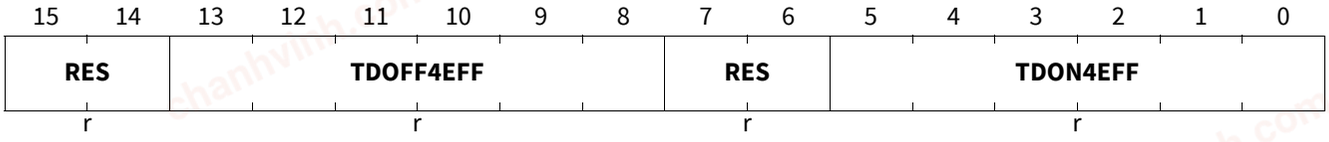
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 00xx xxxx 00xx xxxx$_B$ | | | |

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### Effective MOSFET turn.on/off delay - PWM half-bridge 4

**EFF_TDON_OFF4**
**Effective MOSFET turn.on/off delay - HB4 (101 0110$_B$)** **Reset Value: see Table 75**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always reads as 0** |
| **TDOFF4EFF** | 13:8 | r | **Effective active MOSFET turn-off delay HB4**<br>Nominal effective tDOFF4 = 53.3 ns x TDOFF4EFF[13:8]$_D$ |
| **RES** | 7:6 | r | **Reserved, always reads as 0** |
| **TDON4EFF** | 5:0 | r | **Effective active MOSFET turn-on delay HB4**<br>Nominal effective tDON4 = 53.3 ns x TDON4EFF[5:0]$_D$ |

**Table 75 Reset of EFF_TDON_OFF4**

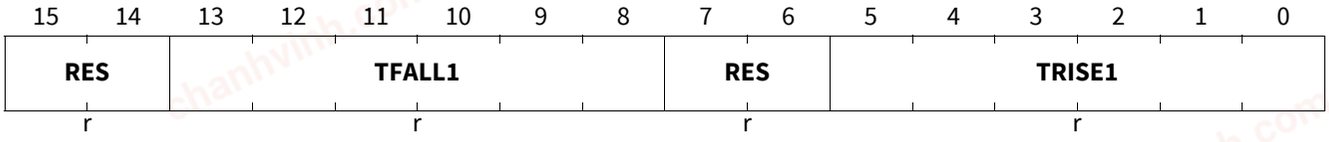
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 00xx xxxx 00xx xxxx$_B$ | | | |

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### MOSFET rise/fall time - PWM half-bridge 1

**TRISE_FALL1**
**MOSFET rise/fall time - HB1** **(101 0111$_B$)** **Reset Value: see Table 76**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always reads as 0** |
| **TFALL1** | 13:8 | r | **Active MOSFET fall time HB1**<br>Nominal tFALL1 = 53.3 ns x TFALL1[5:0]$_D$ |
| **RES** | 7:6 | r | **Reserved, always reads as 0** |
| **TRISE1** | 5:0 | r | **Active MOSFET rise time HB1**<br>Nominal tRISE1 = 53.3 ns x TRISE1[5:0]$_D$ |

**Table 76 Reset of TRISE_FALL1**

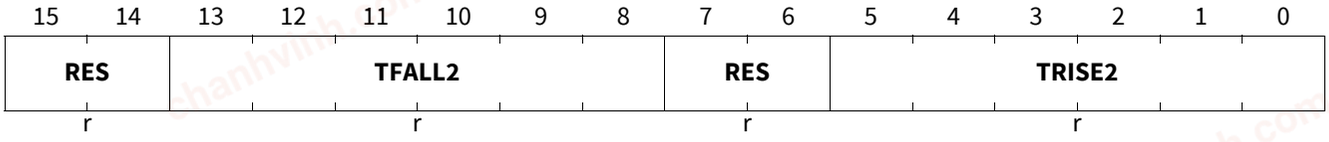
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 00xx xxxx 00xx xxxx$_B$ | | | |

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### MOSFET rise/fall time - PWM half-bridge 2

**TRISE_FALL2**
**MOSFET rise/fall time - HB2** **(101 1000$_B$)** **Reset Value: see Table 77**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always reads as 0** |
| **TFALL2** | 13:8 | r | **Active MOSFET fall time HB2**<br>Nominal tFALL2 = 53.3 ns x TFALL2[5:0]$_D$ |
| **RES** | 7:6 | r | **Reserved, always reads as 0** |
| **TRISE2** | 5:0 | r | **Active MOSFET rise time HB2**<br>Nominal tRISE2 = 53.3 ns x TRISE2[5:0]$_D$ |

**Table 77 Reset of TRISE_FALL2**

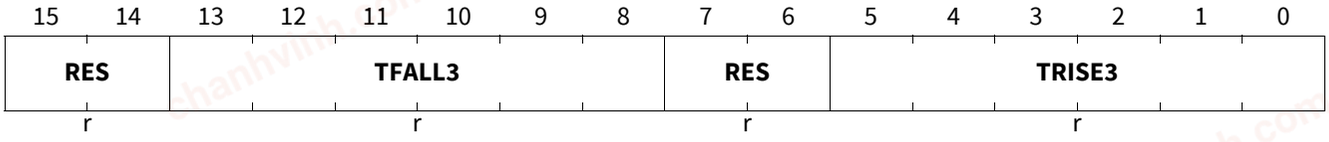
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 00xx xxxx 00xx xxxx$_B$ | | | |

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### MOSFET rise/fall time - PWM half-bridge 3

**TRISE_FALL3**
**MOSFET rise/fall time - HB3** **(101 1001$_B$)** **Reset Value: see Table 78**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always reads as 0** |
| **TFALL3** | 13:8 | r | **Active MOSFET fall time HB3**<br>Nominal tFALL3 = 53.3 ns x TFALL3[5:0]$_D$ |
| **RES** | 7:6 | r | **Reserved, always reads as 0** |
| **TRISE3** | 5:0 | r | **Active MOSFET rise time HB3**<br>Nominal tRISE3 = 53.3 ns x TRISE3[5:0]$_D$ |

**Table 78 Reset of TRISE_FALL3**

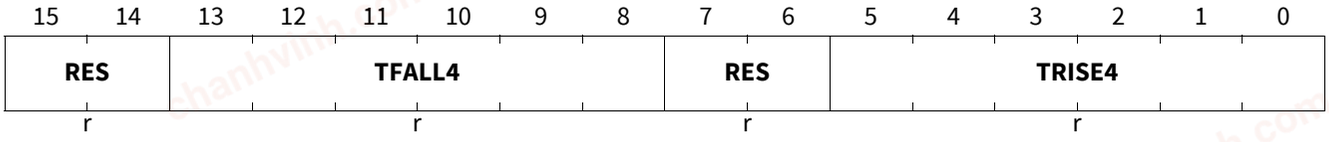
| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 00xx xxxx 00xx xxxx$_B$ | | | |

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### MOSFET rise/fall time - PWM half-bridge 4

**TRISE_FALL4**
**MOSFET rise/fall time - HB4** **(101 1010$_B$)** **Reset Value: see Table 79**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:14 | r | **Reserved, always reads as 0** |
| **TFALL4** | 13:8 | r | **Active MOSFET fall time HB4**<br>Nominal tFALL4 = 53.3 ns x TFALL4[5:0]$_D$ |
| **RES** | 7:6 | r | **Reserved, always reads as 0** |
| **TRISE4** | 5:0 | r | **Active MOSFET rise time HB4**<br>Nominal tRISE4 = 53.3 ns x TRISE4[5:0]$_D$ |

**Table 79 Reset of TRISE_FALL4**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0000 0000 0000$_B$ | | | |
| Restart | 00xx xxxx 00xx xxxx$_B$ | | | |

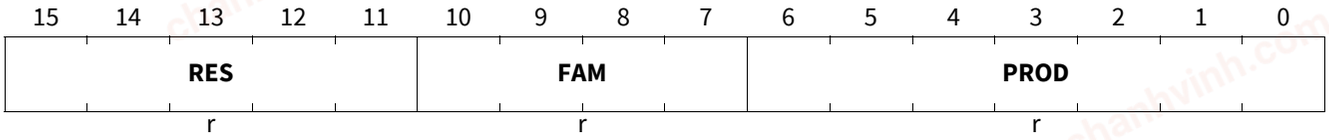
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## 14.6.3 Family and product information register

**Family and Product Identification Register**

**FAM_PROD_STAT**
**Family and Product Identification Register (111 0000$_B$)** **Reset Value: see Table 80**




| Field | Bits | Type | Description |
|---|---|---|---|
| **RES** | 15:11 | r | **Reserved, always reads as 0** |
| **FAM** | 10:7 | r | **Device Family Identifier**<br>1000$_B$, DC Motor System IC |
| **PROD** | 6:0 | r | **Device Product Identifier**<br>000 0000$_B$ **TLE9562-3QX/QX**, TLE9562-3QX/-3QXJ/QX<br>000 0001$_B$ **TLE9561-3QX/QX**, TLE9561-3QX/-3QXJ/QX<br>000 0010$_B$ **TLE9563-3QX**, TLE9563-3QX<br>000 0011$_B$ **TLE9564QX**, TLE9564QX,TLE9185QX<br>001 0000$_B$ **TLE9562-3QX V33**, TLE9562-3QX V33<br>001 0010$_B$ **TLE9563-3QX V33**, TLE9563-3QX V33<br>001 0011$_B$ **TLE9564QX V33**,<br>TLE9564QX V33,TLE9185QX V33<br>001 1000$_B$ **TLE9560QX**, TLE9560-3QX/-3QXJ |

**Table 80 Reset of FAM_PROD_STAT**

| Register Reset Type | Reset Values | Reset Short Name | Reset Mode | Note |
|---|---|---|---|---|
| POR/Soft reset | 0000 0100 0000 0000$_B$ | | | |
| Restart | 0000 0100 0000 0000$_B$ | | | |

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## 14.7 Electrical Characteristics

**Table 81 Electrical Characteristics: Power Stage**

$V_{SINT}$ = 5.5 V to 28 V, $T_j$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **SPI frequency** | | | | | | | |
| Maximum SPI frequency | $f_{SPI,max}$ | – | – | 6.0 | MHz | 1) $V_{CC1}$ > 3 V | P_14.7.1 |
| **SPI Interface; Logic Inputs SDI, CLK and CSN** | | | | | | | |
| H-input Voltage Threshold | $V_{IH}$ | – | – | 0.7 × $V_{CC1}$ | V | – | P_14.7.2 |
| L-input Voltage Threshold | $V_{IL}$ | 0.3 × $V_{CC1}$ | – | – | V | – | P_14.7.3 |
| Hysteresis of input Voltage | $V_{IHY}$ | – | 0.12 × $V_{CC1}$ | – | V | 1) | P_14.7.4 |
| Pull-up Resistance at pin CSN | $R_{ICSN}$ | 20 | 40 | 80 | kΩ | – | P_14.7.5 |
| Pull-down Resistance at pin SDI and CLK | $R_{ICLK/SDI}$ | 20 | 40 | 80 | kΩ | $V_{SDI/CLK}$ = 0.2 × $V_{CC1}$ | P_14.7.6 |
| Input Capacitance at pin CSN, SDI or CLK | $C_I$ | – | 10 | – | pF | 1) $V_{CSN}$, $V_{SDI}$, $V_{CLK}$ = $V_{CC1}$ | P_14.7.7 |
| **Logic Output SDO** | | | | | | | |
| H-output Voltage Level | $V_{SDOH}$ | 0.8 × $V_{CC1}$ | – | – | V | $I_{DOH}$ = -2 mA | P_14.7.8 |
| L-output Voltage Level | $V_{SDOL}$ | – | – | 0.2 × $V_{CC1}$ | V | $I_{DOL}$ = 2 mA | P_14.7.9 |
| 'Tri-state Input Capacitance | $C_{SDO}$ | – | 10 | 15 | pF | 1)$V_{CSN}$, $V_{SDI}$, $V_{CLK}$ = $V_{CC1}$ | P_14.7.11 |
| Tri-state Leakage Current | $I_{SDOLK}$ | –10 | – | 10 | µA | 1)$V_{CSN}$= $V_{CC1}$, 0V < $V_{SDO}$< $V_{CC1}$ | P_14.7.38 |
| **Data Input Timing**[1)] | | | | | | | |
| Clock Period | $t_{pCLK}$ | 160 | – | – | ns | – | P_14.7.12 |
| Clock HIGH Time | $t_{CLKH}$ | 70 | – | – | ns | – | P_14.7.13 |
| Clock LOW Time | $t_{CLKL}$ | 70 | – | – | ns | – | P_14.7.14 |
| Clock LOW before CSN LOW | $t_{bef}$ | 70 | – | – | ns | – | P_14.7.15 |
| CSN Setup Time | $t_{lead}$ | 160 | – | – | ns | – | P_14.7.16 |
| CLK Setup Time | $t_{lag}$ | 160 | – | – | ns | – | P_14.7.17 |
| Clock LOW after CSN HIGH | $t_{beh}$ | 70 | – | – | ns | – | P_14.7.18 |
| SDI Setup Time | $t_{DISU}$ | 60 | – | – | ns | – | P_14.7.19 |
| SDI Hold Time | $t_{DIHO}$ | 40 | – | – | ns | – | P_14.7.20 |

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**Table 81 Electrical Characteristics: Power Stage** (cont'd)

$V_{SINT}$ = 5.5 V to 28 V, $T_j$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Input Signal Rise Time at pin SDI, CLK and CSN | $t_{rIN}$ | – | – | 20 | ns | – | P_14.7.21 |
| Input Signal Fall Time at pin SDI, CLK and CSN | $t_{fIN}$ | – | – | 20 | ns | – | P_14.7.22 |
| Delay Time for Mode Changes[2)] | $t_{Del,Mode}$ | – | – | 5 | µs | [3)] | P_14.7.23 |
| CSN HIGH Time | $t_{CSN(high)}$ | 3 | – | – | µs | – | P_14.7.24 |
| **Data Output Timing[1)]** | | | | | | | |
| SDO Rise Time | $t_{rSDO}$ | – | 30 | 40 | ns | $C_L$ = 50 pF, 0.2 × $V_{CC1}$ to 0.8 × $V_{CC1}$ | P_14.7.25 |
| SDO Fall Time | $t_{fSDO}$ | – | 30 | 40 | ns | $C_L$ = 50 pF, 0.8 × $V_{CC1}$ to 0.2 × $V_{CC1}$ | P_14.7.26 |
| SDO Enable Time | $t_{ENSDO}$ | – | – | 40 | ns | LOW impedance | P_14.7.27 |
| SDO Disable Time | $t_{DISSDO}$ | – | – | 40 | ns | HIGH impedance | P_14.7.28 |
| SDO Valid Time | $t_{VASDO}$ | – | – | 40 | ns | $C_L$ = 50 pF | P_14.7.29 |

1) Not subject to production test; specified by design.
2) Applies to all mode changes triggered via SPI commands.
3) Guaranteed by design.

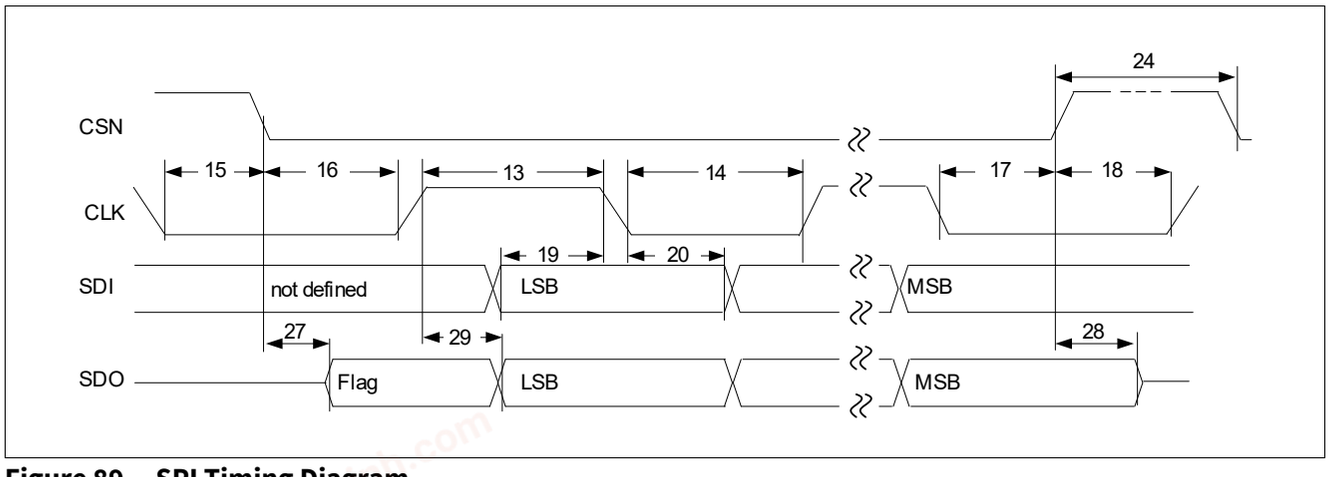



**Figure 89 SPI Timing Diagram**

*Note: Numbers in drawing correlate with the last 2 digits of the Number field in the Electrical Characteristics table.*

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# 15 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

## 15.1 Application Diagrams

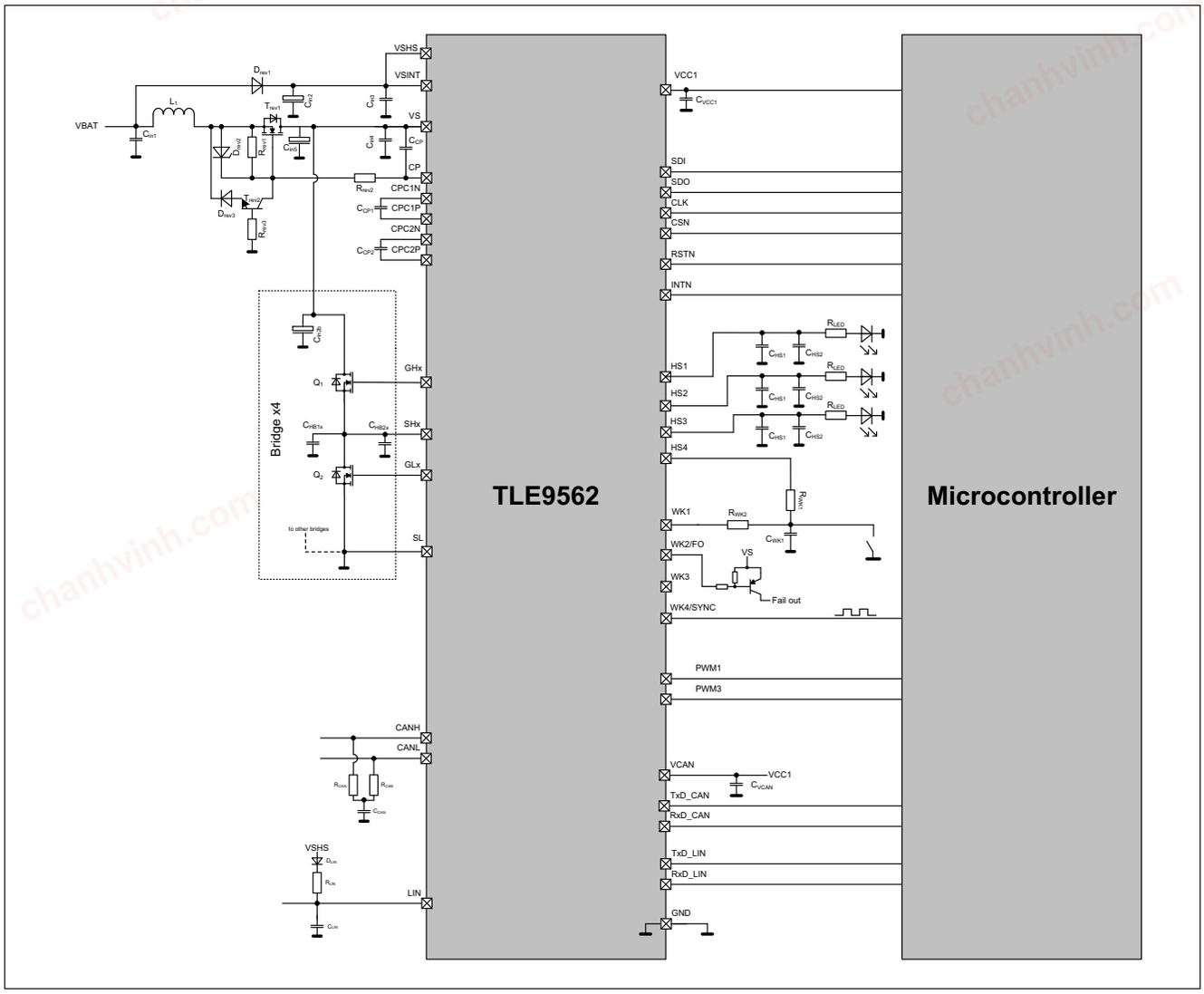



**Figure 90 TLE9562QX Application Diagram**

*Note: This is a very simplified example of an application circuit. The function must be always verified in the real application.*

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**Table 82 Bill of Material**

| Ref. | Typical Value | Purpose / Comment |
|---|---|---|
| **Capacitances** | | |
| $C_{in1}$ | 100 nF ±20% ceramic | Input filter battery capacitor for optimum EMC behavior |
| $C_{in2}$ | 100 µF ±20%, 50 V Electrolytic | Buffering capacitor to cut off battery spikes, depending on the application |
| $C_{in2b}$ | 470 µF ±20%, 50 V Electrolytic | Buffering capacitor for bridges. Cut off battery spikes, depending on the application |
| $C_{in3}$ | 100 nF ±20%, 50 V Ceramic | Input capacitor |
| $C_{in4}$ | 100 nF ±20%, 50 V Ceramic | Input capacitor |
| $C_{in5}$ | 470 µF ±20%, 50 V Electrolytic | Buffering capacitor for bridges. Cut off battery spikes, depending on the application |
| $C_{CP}$ | 470 nF ±20%, 50 V Ceramic | Charge-Pump buffering capacitor |
| $C_{CP1}$/ $C_{CP2}$ | 220 nF ±20%, 50 V Ceramic | Charge-Pump flying capacitor to be placed as closed as possible to the device pins, in order to minimize the length of the PCB tracks |
| $C_{CAN}$ | 4.7 nF / OEM dependent | Split termination stability |
| $C_{LIN}$ | 1 nF / OEM dependent | LIN master termination |
| $C_{VCC1}$ | 2.2 uF ±20%, 16 V | Blocking capacitor. Low ESR. Minimum 1 uF effective capacitance |
| $C_{VCAN}$ | 1 uF ... 4.7 uF | Input filter CAN supply. The capacitor must be placed close to the VCAN pin. For optimum EMC and CAN FD performances, the capacitor has to be ≥ 2.2 µF |
| $C_{HB1x}$ | 10 nF ±20%, 50 V Ceramic | Half-Bridge EME (electromagnetic emission) and ESD suppression filter to be placed close to the connector. Other capacitance values might be needed depending on application |
| $C_{HB2x}$ | 560 pF ±20%, 50 V Ceramic | Optional filter for EMI immunity to be placed close to the SHx pin (PCB footprints highly recommended). Other capacitance values might be needed depending on application |
| $C_{HS1}$ | 47 pF / OEM dependent | Only required om case of off-board connection to optimize EMC behavior, place close to pin |
| $C_{HS2}$ | 33 nF / OEM dependent | As required by application, mandatory protection for off-board connection |
| $C_{WK1}$ / $C_{WK2}$ | 47 nF / OEM dependent | Spike filtering, as required by application, mandatory protection for off-board connections |
| **Inductances** | | |
| $L_1$ | 4 uH ... 6 uH | Input filter for power stage - consider high current rating (application dependent) |

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## Application Information

**Table 82 Bill of Material** (cont'd)

| Ref. | Typical Value | Purpose / Comment |
|---|---|---|
| **Resistances** | | |
| $R_{REV1}$ | 100 kΩ ±5% | Other values needed depending on application |
| $R_{REV2}$ | 10 kΩ ±5% | Device protection against reverse battery |
| $R_{REV3}$ | 10 kΩ ±5% | |
| $R_{CAN}$ | 60 Ω / OEM dependent | CAN bus termination |
| $R_{LIN}$ | 1 k ±5% | LIN master termination |
| $R_{LED}$ | 1 k | Limit LED-current |
| $R_{WK1}$ / $R_{WK2}$ / $R_{WK3\ /\ RWK4}$ | 10 kΩ ±5% | |
| **Active Components** | | |
| $D_{REV1}$ | RR268MM600 | Reverse polarity protection |
| $D_{REV2}$ | BZX84C16 | Gate protection. Limit $V_{GS}$ |
| $D_{REV3}$ | BAS21 | |
| $T_{REV1}$ | IPZ40N04S5L-2R8 | Reverse battery protection, N-MOS |
| $T_{REV2}$ | BC846 | |
| $Q_1$ / $Q_2$ | IPZ40N04S5-5R4 | Main power switches |
| $D_{LIN}$ | BAS70 | Requested by LIN standard; reverse polarity protection of network |

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## 15.2 ESD Tests

### 15.2.1 ESD according to IEC61000-4-2

Tests for ESD robustness according to IEC61000-4-2 “GUN test” (150 pF, 330 Ω) have been performed. The results and test condition are available in a test report. The values for the test are listed below.

**Table 83 ESD “GUN test”[1)2)]**

| Performed Test | Result | Unit | Remarks |
|---|---|---|---|
| ESD at pin CANH, CANL, LIN, HSx, VS,VSINT,VSHS, WKx versus GND | > 6 | kV | positive pulse |
| ESD at pin CANH, CANL, LIN, HSx, VS,VSINT,VSHS, WKx versus GND | < -6 | kV | negative pulse |

1) ESD susceptibility “ESD GUN” according to EMC 1.3 Test specification, Section 4.3 (IEC 61000-4-2). Tested by external test house (IBEE Zwickau, EMC Test report Nr. 20.12.20).
2) ESD Test “Gun Test” is specified with external components for pins VS, VSINT, VSHS, WKx, HSx. See the application diagram in **Chapter 15.1** for more information.

### 15.2.2 ESD according to SAE J2962

Tests for ESD robustness according to SAE J2962 have been performed.

**Table 84 ESD according to SAE J2962**

| Performed Test | Result | Unit | Remarks |
|---|---|---|---|
| ESD at pin CANH, CANL, LIN versus GND | ± 4 | kV | Unpowered, contact discharge |
| ESD at pin CANH, CANL versus GND | ± 8 | kV | Powered, contact discharge |
| ESD at pin LIN versus GND | ± 8 | kV | [1)]Powered, contact discharge |
| ESD at pin CANH, CANL versus GND | ± 15 | kV | Powered, air discharge |
| ESD at pin LIN versus GND | ± 25 | kV | [1)]Powered, air discharge |

1) For ESD pulses ≤ - 6 kV, VCC1 undervoltage may be detected.

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## 15.3 Thermal Behavior of Package

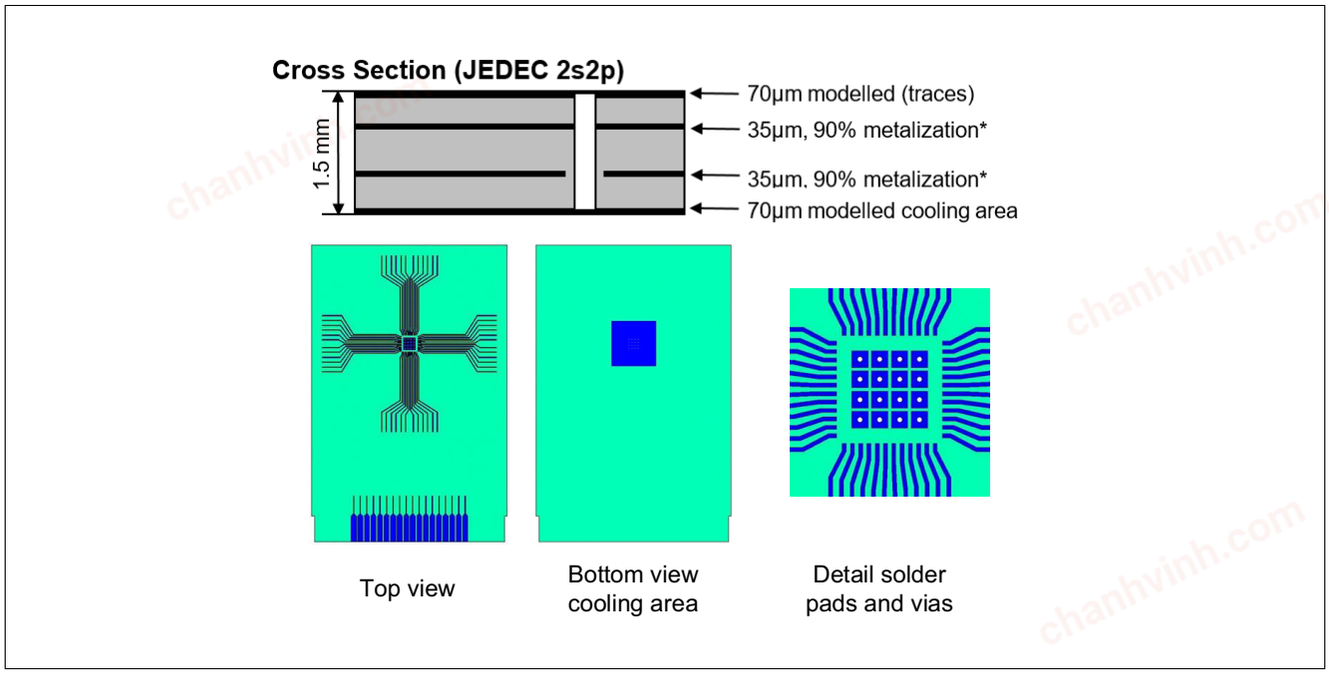



**Figure 91 Board Setup**

Board setup is defined according JESD 51-2, -5, -7.
Board: 76.2 × 114.3 × 1.5 $mm^3$ with 2 inner copper layers (35 µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300 $mm^2$ cooling area on the bottom layer (70 µm).

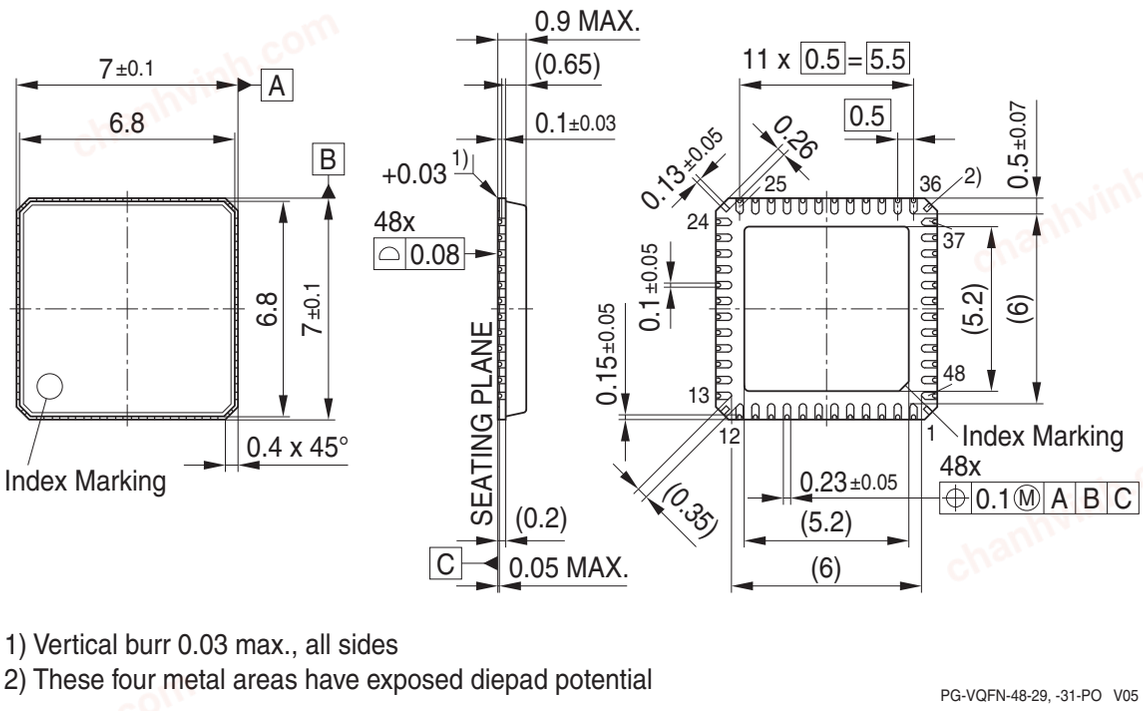
## 15.4 Further Application Information

- The VS pin supplies the bridge driver and the charge pump, and is the sense pin for the high-side MOSFETs drain voltage. It is therefore highly recommended to connect a 100 nF / 50V ceramic by-pass capacitor as close as possible to the VS pin with a short PCB trace to GND.
- Please contact us for information regarding the FMEA pin
- For further information you may contact **http://www.infineon.com/**

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# 16 Package Outlines




1) Vertical burr 0.03 max., all sides
2) These four metal areas have exposed diepad potential

PG-VQFN-48-29, -31-PO V05

**Figure 92 PG-VQFN-48[1)]**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

**https://www.infineon.com/packages**

1) Dimensions in mm

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# 17 Revision History

| Revision | Date | Changes |
|---|---|---|
| 1.0 | 2021-01-21 | First release |

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