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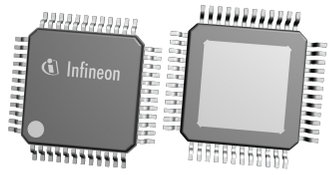
TLE9015DQU

iso UART transceiver IC

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AEC Qualified · RoHS

Features



- Compatibility for ring mode topology
- Two UART ports for serial communication to host microcontroller
- Two iso UART interfaces for communication to other BMS ICs
- 2 Mbit/s data rate for fast communication
- Fully transparent communication scheme from UART to iso UART
- Integrated internal logic for minimizing pin count on the UART side
- Differential current edge triggered iso UART communication interface
- High robustness against external noise
- Two external fault inputs (EMM and ERRQ_ext)
- Latching error output pin for triggering external microcontroller
- Internal supply monitoring
- Green Product (RoHS compliant)

Potential applications

Multi-cell battery monitoring and balancing system IC designed for Li-ion battery packs used in hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), battery electric vehicles (BEV) as well as in 12 V Li-ion batteries.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE9015DQU is a iso UART transceiver IC.

The TLE9015DQU is a general purpose transceiver IC to be used in battery systems for enabling the communication between the main host microcontroller and the cell supervision ICs which are usually connected to the battery module potential. The IC is designed for Li-Ion battery packs used in hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), battery electric vehicles (BEV) as well as stationary Li-Ion batteries.

Additionally to the physical layer translation, the TLE9015DQU offers the possibility to communicate potential detected errors in a cell inside the battery pack to the main microcontroller.

Type	Package	Marking
TLE9015DQU	PG-TQFP-48	TLE9015DQU

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1 Block diagram

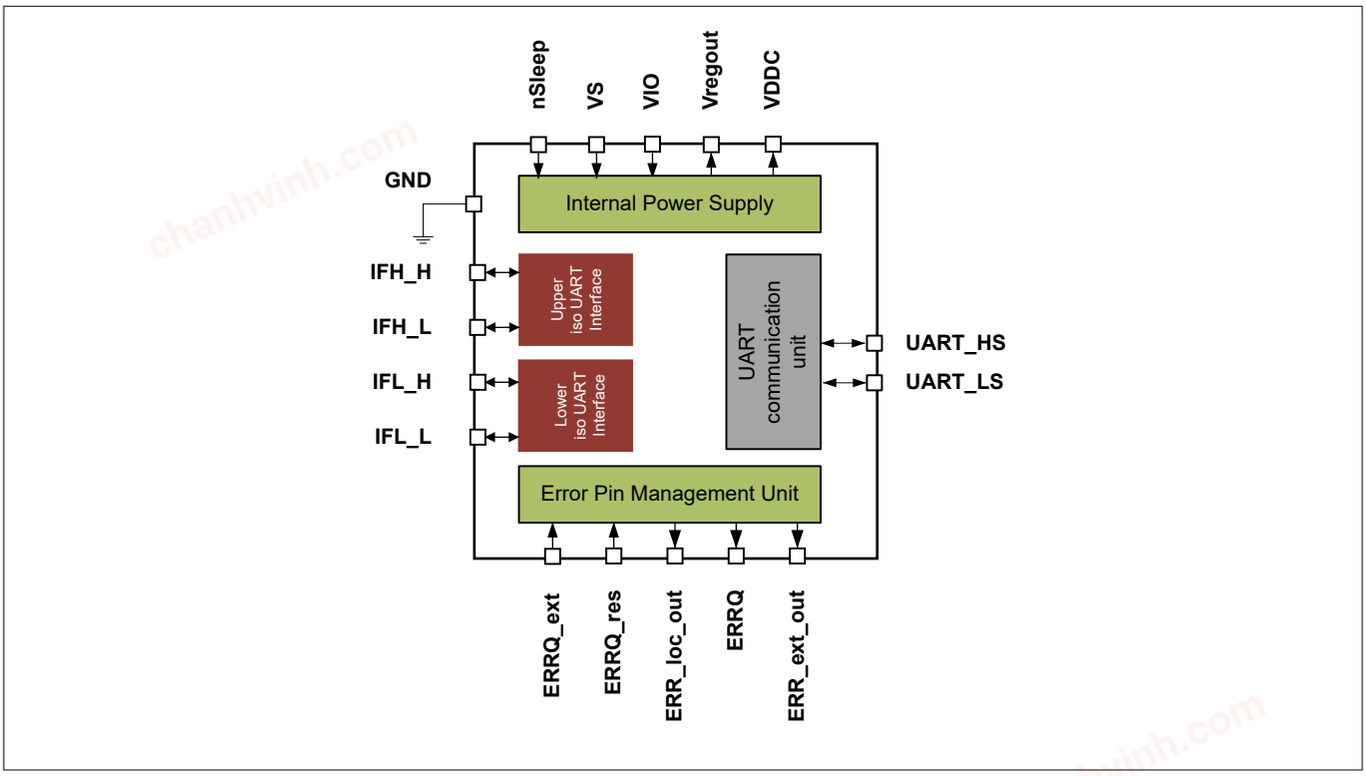


Figure 1 Block diagram

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2 Pin configuration

2.1 Pin assignment

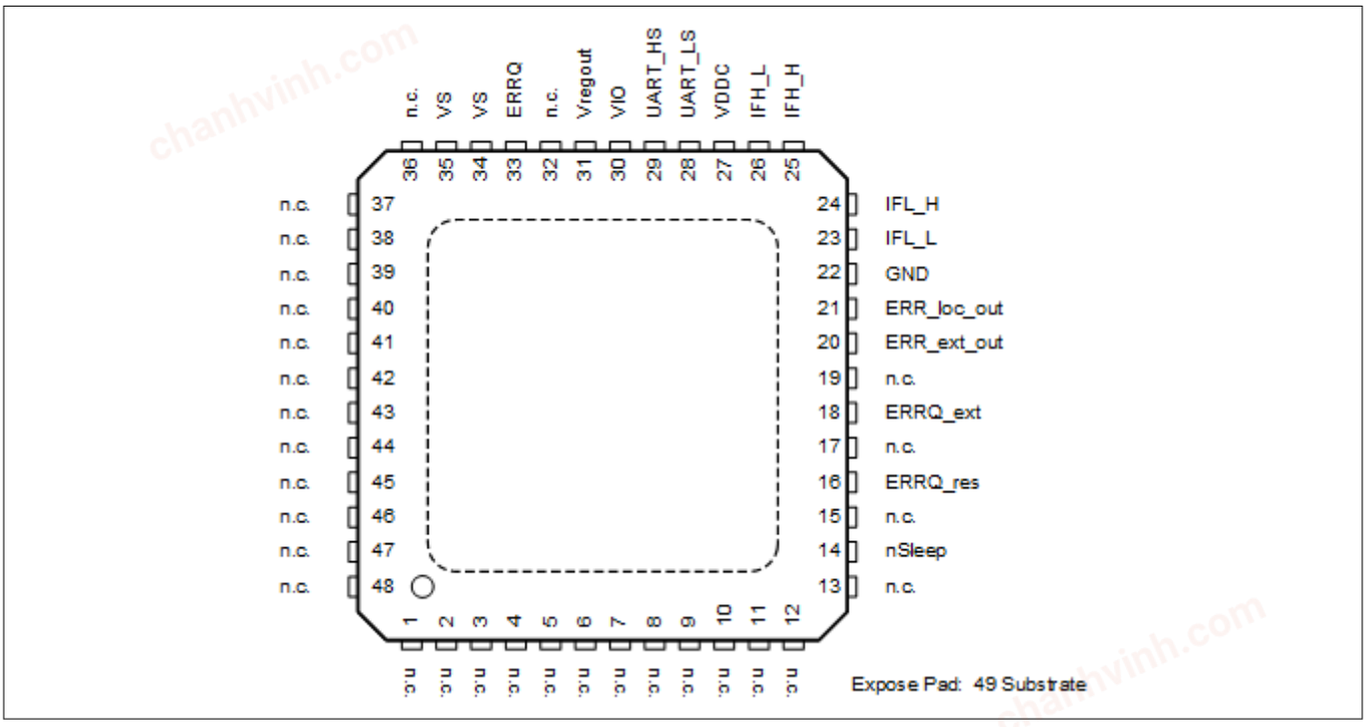


Figure 2 Pin configuration (top view)

2.2 Pin definitions and functions

Pin	Symbol	Pin type	Function
1	n. c.		Not connected. Connect to GND in application.
2	n. c.		Not connected. Connect to GND in application.
3	n. c.		Not connected. Connect to GND in application.
4	n. c.		Not connected. Connect to GND in application.
5	n. c.		Not connected. Connect to GND in application.
6	n. c.		Not connected. Connect to GND in application.
7	n. c.		Not connected. Connect to GND in application.
8	n. c.		Not connected. Connect to GND in application.
9	n. c.		Not connected. Connect to GND in application.
10	n. c.		Not connected. Connect to GND in application.
11	n. c.		Not connected. Connect to GND in application.
12	n. c.		Not connected. Connect to GND in application.
13	n. c.		Not connected. Connect to GND in application.
14	nSleep	I	Input pin to force the device to go to sleep; active low.

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2 Pin configuration

Pin	Symbol	Pin type	Function
15	n. c.		Not connected. Connect to GND in application.
16	ERRQ_res	I	Reset the ERRQ pin; active low.
17	n. c.		Not connected. Connect to GND in application.
18	ERRQ_ext	I	Input for external ERRQ. If not used, connect to VREGOUT.
19	n. c.		Not connected. Connect to GND in application.
20	ERR_ext_out	O	Output for external ERRQ; active high.
21	ERR_loc_out	O	Output pin to indicate local ERRQ; active high.
22	GND	GND	Local GND of the device.
23	IFL_L	D_I / O	Lower isolated UART (iso UART) L pin.
24	IFL_H	D_I / O	Lower isolated UART (iso UART) H pin.
25	IFH_H	D_I / O	Upper isolated UART (iso UART) H pin.
26	IFH_L	D_I / O	Upper isolated UART (iso UART) L pin.
27	VDDC	Supply	Buffer capacitor pin for internal iso UART supply.
28	UART_LS	D_I / O	UART LS channel.
29	UART_HS	D_I / O	UART HS channel.
30	VIO	S	Supply for UART interface.
31	VREGOUT	S	Output pin for the internal regulator.
32	n.c.	n.c.	Not connected. Connect to GND in application.
33	ERRQ	HV_D_O	Error pin; open drain NMOS. This pin is latching.
34	VS	S	Supply pin.
35	VS	S	Supply pin.
36	n. c.		Not connected. Connect to GND in application.
37	n. c.		Not connected. Connect to GND in application.
38	n. c.		Not connected. Connect to GND in application.
39	n. c.		Not connected. Connect to GND in application.
40	n. c.		Not connected. Connect to GND in application.
41	n. c.		Not connected. Connect to GND in application.
42	n. c.		Not connected. Connect to GND in application.
43	n. c.		Not connected. Connect to GND in application.
44	n. c.		Not connected. Connect to GND in application.
45	n. c.		Not connected. Connect to GND in application.
46	n. c.		Not connected. Connect to GND in application.
47	n. c.		Not connected. Connect to GND in application.
48	n. c.		Not connected. Connect to GND in application.

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2 Pin configuration

Pin	Symbol	Pin type	Function
49	Exposed Pad	GNDA	Cooling tab. Connect to GND in the application.

Pin types: A = analog, D = digital, HV = high-voltage, I = input, O = output, I/O = bidirectional, P = power, S = supply

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3 General product characteristics

Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage VS	V_{VS_max}	-0.3	–	45	V	–	PRQ-1368
Supply voltage VS relative	$V_{VS_rel_max}$	$V_{VREGOUT}$ - 0.3	–	–	V	–	PRQ-489
Supply voltage VIO	V_{VIO_max}	-0.3	–	5.5	V	–	PRQ-488
Regulator output VREGOUT	$V_{VREGOUT_max}$	-0.3	–	3.6	V	–	PRQ-490
Regulator output VDDC	V_{VDDC_max}	-0.3	–	3.6	V	Assuming $I_{VDDC} \leq 1$ mA continuous current	PRQ-491
iso UART interface IFL_x	$V_{IFL_L_max}$ $V_{IFL_H_max}$	-4.1	–	6.6	V	1) BCI test maximum 300 mA injected via twisted pair cable onto iso UART interface (maximum pin current 150 mA)	PRQ-493
iso UART interface IFH_x	$V_{IFH_L_max}$ $V_{IFH_H_max}$	-4.1	–	6.6	V	1) BCI test maximum 300 mA injected via twisted pair cable onto iso UART interface (maximum pin current 150 mA)	PRQ-492
Ground pin GND	V_{GND}	0	–	0	V	Absolute GND	PRQ-511
High voltage input pin nSleep	V_{nSleep_max}	-0.3	–	45	V	2)	PRQ-524

(table continues...)

1 Positive and negative transients with a maximum duration of 100 ns allowed between ± 8 V; This should simulate ESD events; however, during normal and steady-state condition voltage on these pins must stay inside the maximum ratings specified.

2 Not subject to production test, specified by design.

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Table 1 (continued) Absolute maximum ratings

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High voltage input pin ERRQ_res	$V_{ERRQ_res_max}$	-0.3	–	45	V	2)	PRQ-526
High voltage input pin ERRQ_ext	$V_{ERRQ_ext_max}$	-0.3	–	45	V	2)	PRQ-528
Digital output pin absolute ERR_ext_out	$V_{ERR_ext_out_max}$	-0.3	–	5.5	V	2)	PRQ-531
Digital output pin relative ERR_ext_out	$V_{ERR_ext_out_rel_max}$	-0.3	–	V_{VIO} + 0.3	V	2)	PRQ-530
Digital output pin absolute ERR_loc_out	$V_{ERR_loc_out_max}$	-0.3	–	5.5	V	2)	PRQ-533
Digital output pin relative ERR_loc_out	$V_{ERR_loc_out_rel_max}$	-0.3	–	V_{VIO} + 0.3	V	2)	PRQ-532
UART interface pins absolute	$V_{UART_x_max}$	-0.3	–	5.5	V	2) x → LS or HS	PRQ-535
UART interface pins relative	$V_{UART_x_rel_max}$	-0.3	–	V_{VIO} + 0.3	V	2) x → LS or HS	PRQ-534
ESD robustness							
ESD robustness 2 kV	$V_{ESD_2kV_max}$	-2	–	2	kV	3) HBM; all pins	PRQ-514
ESD robustness 4 kV	$V_{ESD_4kV_max}$	-4	–	4	kV	3) HBM; robustness versus GND for pins: VS, IFH_x, IFL_x	PRQ-1831

(table continues...)

2 Not subject to production test, specified by design.
3 ESD robustness, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).

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Table 1 (continued) Absolute maximum ratings

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ESD robustness CDM 500 V	$V_{ESD_cdm_all_max}$	-500	–	500	V	[4] CDM; all pins	PRQ-516
ESD robustness CDM 750 V	$V_{ESD_Corner_max}$	-750	–	750	V	[4] CDM; corner pins	PRQ-517
Temperatures							
Junction temperature	T_{j_max}	-40	–	150	°C	–	PRQ-512
Storage temperature	T_{stg_max}	-55	–	150	°C	–	PRQ-513

Notes:

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Functional range

Table 2 Functional range

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage VS	$V_{VS_functional}$	4.75	–	45	V	–	PRQ-1367
Supply voltage VIO	$V_{VIO_functional}$	3	–	5.5	V	–	PRQ-520

[4] ESD robustness, Charged Device Model JESD22-C101.

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3.3 Thermal resistance

Table 3 Thermal resistance

$V_{VS} = V_{VS_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	20	–	K/W		PRQ-1846
Junction to ambient	R_{thJA}	–	48	–	K/W	5)	PRQ-1847

5 Specified *R*thJA value is according to JEDEC JESD51-5,-7 at natural convection on FR4 2s2p board; The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). The thermal via array under the exposed pad consists of 16 vias with a diameter of 0.3 mm and a plating thickness of 25 µm.

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4 Power Management Unit (PMU)

4.1 Functional description

The transceiver IC can be powered from an external LDO via VS pin or any other source which can supply the voltage V_{VS}.

To supply the communication interface, the device provides a regulated output voltage V_{VDDC} on pin VDDC.

The device provides a regulated output voltage $V_{VREGOUT}$ with an output current $I_{VREGOUT}$ on pin VREGOUT which can supply the GPIOs of the device or other loads.

The voltage at the VIO pin sets the logic levels and supplies the GPIOs. The pin can be connected directly to the VREGOUT pin or to another desired voltage level using an external regulator.

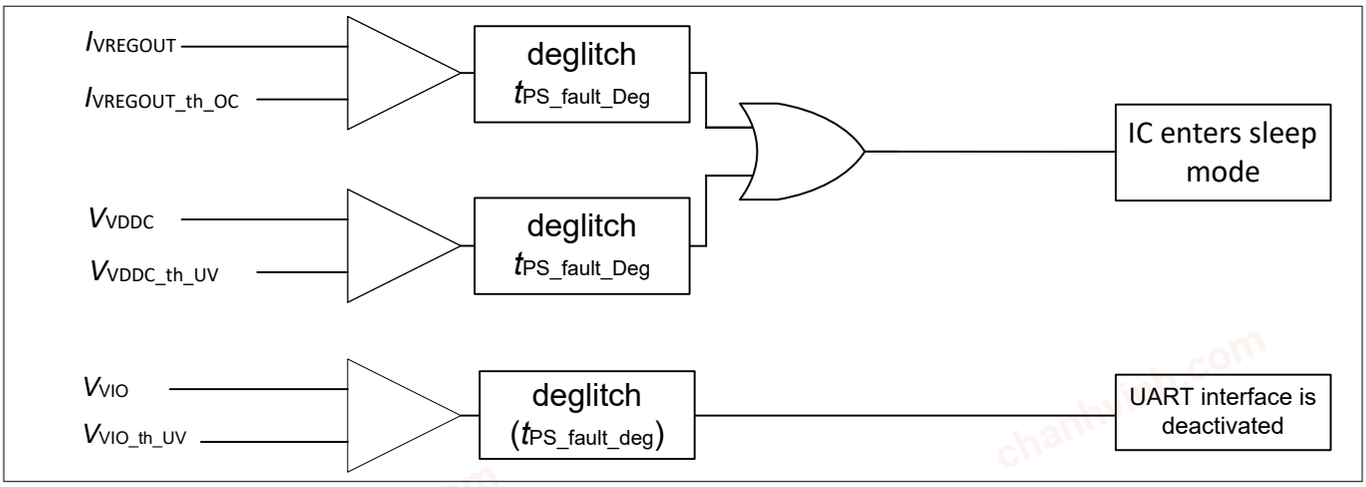


Figure 3 Power supply monitoring

The IC is forced to go to sleep mode via the nSleep pin. The pin is edge triggered from "high" to "low" and has an internal pull-up resistor R_{nSleep_PU}.

4.2 Electrical characteristics power management unit (PMU)

Table 4 Electrical characteristics

$V_{VS} = V_{VS_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Internal regulators							
VREGOUT internal regulator output voltage	$V_{VREGOUT}$	3.3	3.45	3.6	V	–	PRQ-544
VDDC output voltage	V_{VDDC}	2.42	2.5	2.63	V	–	PRQ-549

(table continues...)

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Table 4 (continued) Electrical characteristics

$V_{VS} = V_{VS_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply currents							
VS sleep mode current	I_{VS_sleep}	–	3	23	µA	**1.** typical value T_j = 25°C **2.** -40°C < T_j < 50°C	PRQ-1341
VS idle current	I_{VS_idle}	–	4.9	6.5	mA	IC in idle mode	PRQ-557
VREGOUT current consumption multi purpose supply	$I_{VREGOUT}$	–	–	5	mA	No load on VIO	PRQ-1373
VIO current consumption during UART communication	I_{VIO_comm}	–	–	5	mA	No load on VREGOUT	PRQ-695
VS current consumption during communication	I_{VS_comm}	–	$I_{VS_idle_typ}$ + 0.9	$I_{VS_idle_max}$ + 1.2	mA	• UART communication. • Current to charge external interface components not included.	PRQ-694
VS current consumption during iso UART communication including external interface components	$I_{VS_comm_isoU}$	–	–	I_{VS_comm} + 7.6	mA	6) **1.** C_{ser} = 1 nF **2.** BR_{iso_U} = 2 Mbit/s **3.** R_{ser} = 39 Ω **4.** $C_{isoUART_F}$ = 220 pF **5.** Valid for one iso UART interface in TX mode	PRQ-562
Protection and Detection							
VREGOUT overcurrent threshold	$I_{VREGOUT_th_OC}$	31	40	60	mA	Tested during idle mode	PRQ-545
VIO undervoltage threshold falling	$V_{VIO_th_UV_fall}$	2.2	–	2.76	V	–	PRQ-546

(table continues...)

6 Not subject to production test; verified by design or characterization.

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Table 4 (continued) Electrical characteristics

$V_{VS} = V_{VS_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VIO undervoltage threshold rising	$V_{VIO_th_UV_rise}$	2.24	–	2.9	V	–	PRQ-547
VIO undervoltage threshold hysteresis	$V_{VIO_th_UV_hys}$	40	100	160	mV	–	PRQ-548
VDDC undervoltage threshold	$V_{VDDC_th_UV}$	2.15	–	2.42	V	–	PRQ-550
VDDC undervoltage threshold hysteresis	$V_{VDDC_th_UV_hys}$	80	100	140	mV	–	PRQ-551
Power supply error detection deglitch time	$t_{PS_ERR_deg}$	8	15	24	µs	6)	PRQ-552
nSleep pin							
nSleep input range voltage "low"	V_{nSleep_LOW}	0	–	0.99	V	–	PRQ-690
nSleep input range voltage "high"	V_{nSleep_HIGH}	2.52	–	V_{VS}	V	–	PRQ-691
nSleep internal pull up resistor	R_{nSleep_PU}	200	300	400	kΩ	connected to an internal 3.3 V supply	PRQ-692
nSleep input deglitch	$t_{nSleep_deglitch}$	19.85	21.82	24	us	6)	PRQ-693

6 Not subject to production test; verified by design or characterization.

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5 Watchdog and wake-up function (WD)

5.1 Functional description

The IC generates the wake-up pattern on:

- IFL, if the IC received a valid wake-up pattern on interface UART_HS.
  - (1) indicates the source of wake-up, (2) indicates the propagation on IFL_x
  - Ring mode: (5) indicates propagated wake-up signal received on IFH_x and (6) forwarded to UART_LS.
- IFH, if the IC received a valid wake-up pattern on interface UART_LS.
  - (3) indicates the source of wake-up, (4) indicates the propagation on IFH_x

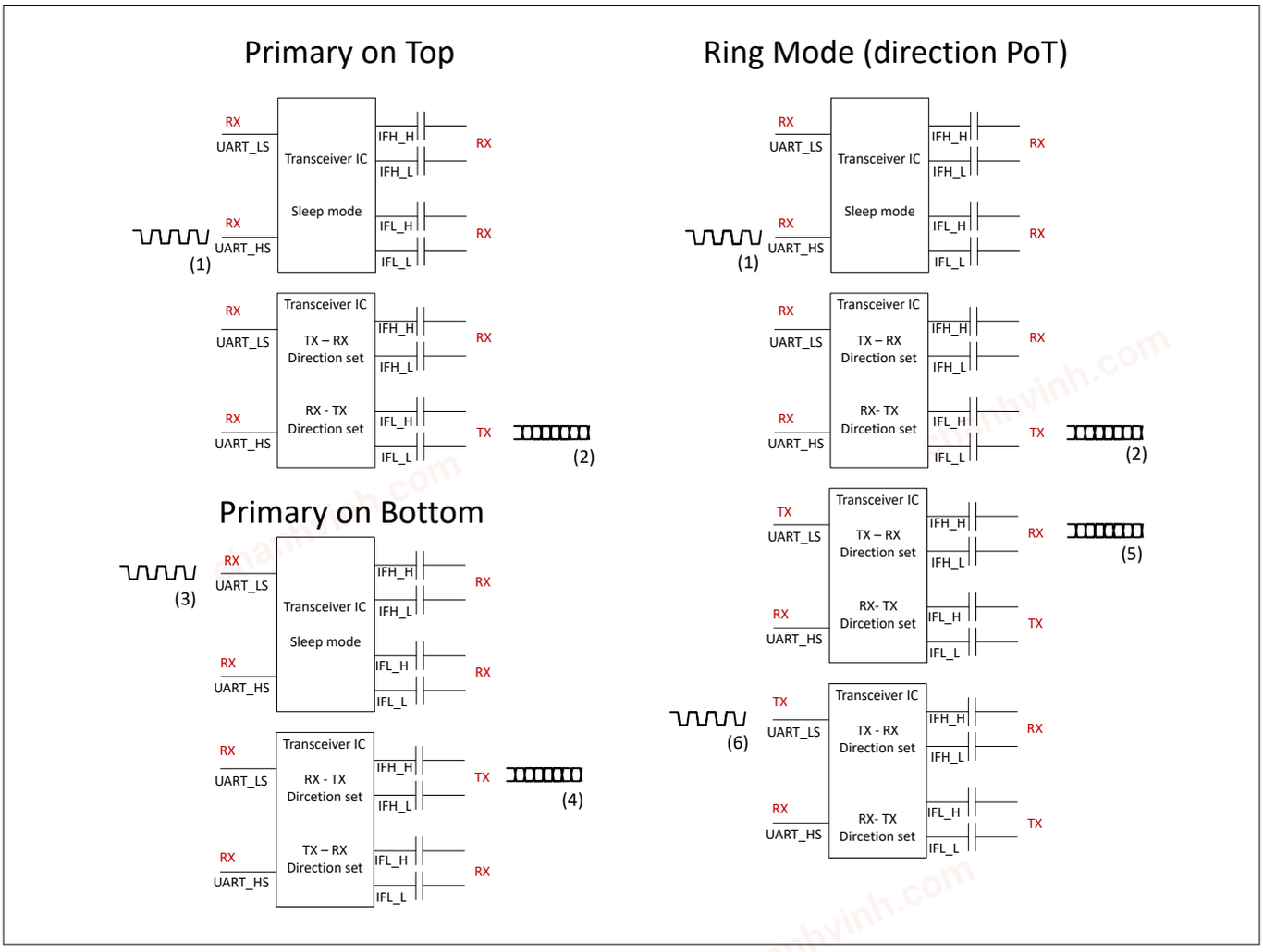


Figure 4 Wake-up signal propagation

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5.2 Electrical characteristics watchdog and wake-up function (WD)

Table 5 Electrical characteristics

$V_{VS} = V_{VS_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Wake-up function							
WD wake-up signal frequency	f_{WAKEUP}	48	50	1040	kHz	–	PRQ-572
WD device wake-up time	t_{WAKE}	200	370	500	µs	48 kHz wake-up frequency. From the first falling edge of the input pattern to the first edge of the propagated wake-up sequence.	PRQ-573
WD wake-up - number of detected periods	n_{WAKE_det}	4	–	8	periods	–	PRQ-574
WD wake-up propagation - length in periods	n_{WAKE}	8	–	8	periods	–	PRQ-575

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6 Communication

6.1 Functional description

The device supports the following communication interfaces.

1. UART
2. iso UART

iso UART communications allows to stack multiple devices.

The IC acts as link between UART and iso UART interfaces supporting all communication modes:

- Ring mode
- Primary on bottom (PoB)
- Primary on top (PoT)
- Simultaneous PoB and PoT in case of broken wire between sensing ICs iso UART interfaces

The device forwards a received message to the next device in the system. The time between receiving and forwarding the message is defined depending upon the receiving interface:

- Receiving on UART and forwarding on iso UART: $t_{UART_isoU_del}$
- Receiving on iso UART and forwarding on UART: $t_{UART_isoU_del}$

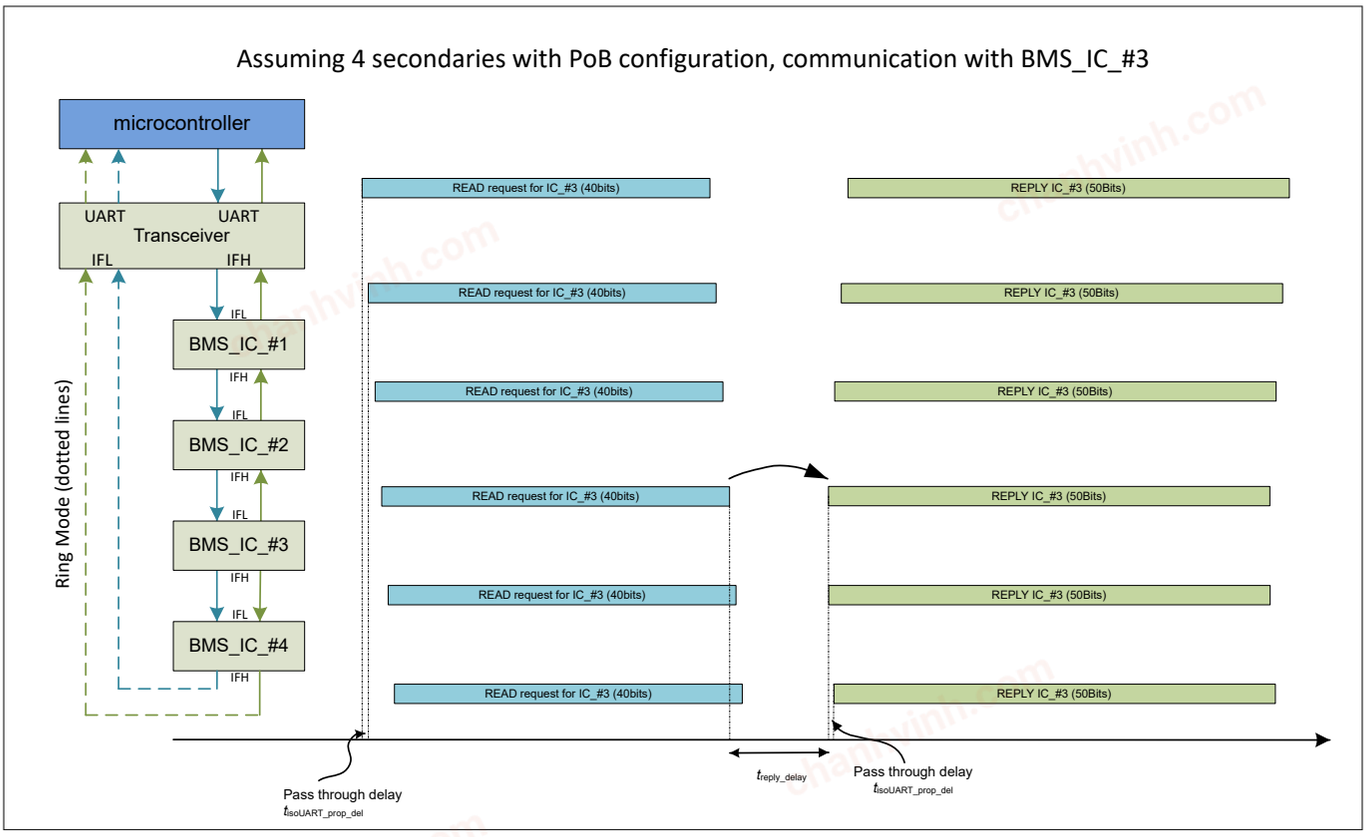


Figure 5 Communication propagation delays

iso UART waveform specification

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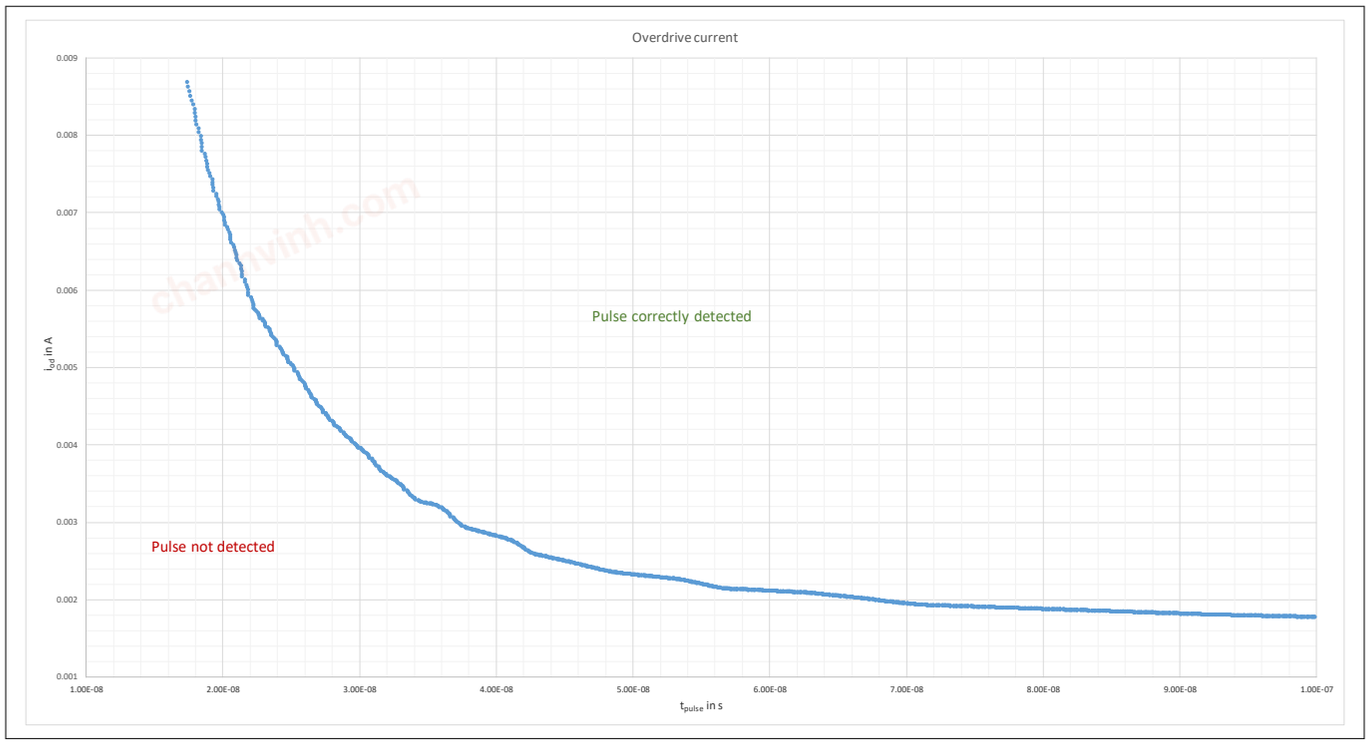


Figure 6 iso UART waveform specification

6.2 Electrical characteristics communication

Table 6 Electrical characteristics

$V_{VS} = V_{VS_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
UART physical layer							
UART input "low" level	V_{UART_low}	0	–	V_{VIO} × 0.3	V	–	PRQ-719
UART input "high" level	V_{UART_high}	V_{VIO} × 0.7	–	V_{VIO}	V	–	PRQ-720
UART output "low" level	V_{UART_low}	0	–	0.45	V	$I_{UART} \leq 5$ mA	PRQ-721
UART output high level	V_{UART_HIGH}	V_{VIO} - 0.45	–	V_{VIO}	V	$I_{UART} \geq -5$ mA	PRQ-722
UART output current	I_{UART}	-5	–	5	mA	Current capability of UART output; x → LS or HS	PRQ-723
UART bit rate	BR_{UART}	0.97	2.0	2.1	Mbit/s	Determined by microcontroller. Device's responses are synchronized to microcontroller UART bit rate.	PRQ-724

(table continues...)

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Table 6 (continued) Electrical characteristics

$V_{VS} = V_{VS_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External capacitance on UART pin	C_{UART_ext}	–	–	30	pF	–	PRQ-725
UART to iso UART propagation delay	$t_{UART_isoU_del}$	–	25	70	ns	Propagation delay from UART to iso UART	PRQ-828
iso UART current threshold "high"	$I_{isoU_th_high}$	2.25	4.5	6.5	mA	$(I_{IFx_H} - I_{IFx_L}) / 2$ I_{IFx_H}: Current in the iso UART high pin I_{IFx_L}: Current in the iso UART low pin	PRQ-832
iso UART current threshold "low"	$I_{isoU_th_low}$	-6.5	-4.5	-2.25	mA	$(I_{IFx_H} - I_{IFx_L}) / 2$ I_{IFx_H}: Current in the iso UART high pin I_{IFx_L}: Current in the iso UART low pin	PRQ-833
iso UART propagation delay	$t_{isoU_prop_del}$	–	25	70	ns	7) Propagation delay from IFH to IFL and IFL to IFH	PRQ-834
iso UART overdrive current	I_{od}	3	–	–	mA	8) with t_{pulse} = 38 ns	PRQ-1370
Reply delay time	t_{reply_delay}	0	1.7	3	µs	8) internal reply delay time of one IC	PRQ-837
iso UART bit rate	BR_{isoU}	0.97	2	2.1	Mbit/s	–	PRQ-838
Series resistor value	R_{ser}	37.05	39	40.95	Ω	8) 9)	PRQ-836
Series capacitor value	C_{ser}	0.95	1	1.05	nF	8) 9)	PRQ-835
Transceiver Ron @100mA	R_{ON}	19	22	27	Ω	–	PRQ-1845

7 Tested with standard external circuit (C_{ser}, R_{ser}).
8 Not subject to production test; verified by design or characterization.
9 External RC network needs to be adjusted depending on the application constraints, for example cable length.

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7 Emergency mode (EMM) and ERR pin (ERR)

7.1 Functional description

The following events trigger the ERRQ pin:

- Incoming emergency mode signal (EMM) via iso UART interface
- Fault input pin ERRQ_ext

The emergency signal is an alternating signal with the frequency f_{EMM}. In case of an incoming EMM signal, the IC enters EMM and starts the fault handling.

The EMM signal has a duration of n_{EMM} periods. The number of periods the IC needs to detect an EMM signal is depending on the operation mode:

1. Idle mode: n_{EMM_dect}
2. Straight after wake-up caused by EMM: $n_{EMM_dect_wake\text{-}up}$

The output of the ERRQ pin is open drain. The "low" state is latching and can be reset by the ERRQ_res pin.

The ERR_loc_out pin indicates, whether an incoming EMM signal triggered the error handling procedure. On detection of an EMM signal, the device sets the ERR_loc_out pin "high" for the duration of $t_{ERR_loc_out}$. The logic levels of the pin are VIO and GND.

The ERR_ext_out pin is an output pin. It indicates that the fault was triggered by the ERRQ_ext pin and represents the deglitched and inverted ERRQ_ext signal. The pin is active high and the logic levels are VIO and GND.

The ERRQ_ext pin is an input pin to trigger the ERRQ pin externally. The pin is level triggered active low with a deglitch time of $t_{ERRQ_ext_deglitch}$. The pin has an internal pull-up resistor $R_{ERRQ_ext_PU}$ to the internal 3.3 V supply implemented.

The ERRQ_res pin is the input pin to reset the ERRQ pin function. The pin is level triggered active low. The pin has an internal pull-up resistor $R_{ERRQ_res_PU}$ to the internal 3.3 V supply implemented and includes a deglitch filter with deglitch time defined by $t_{ERRQ_res_deglitch}$.

7.2 Electrical characteristics emergency mode (EMM) and ERR pin (ERR)

Table 7 Electrical characteristics

$V_{VS} = V_{VS_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
EMM number of periods to detect EMM signal - straight after wake-up	$n_{EMM_dect_wake\text{-}up}$	4	–	4	periods	[10] IC just entered IDLE state straight after wake-up procedure.	PRQ-739
EMM number of periods to detect EMM signal - idle mode	n_{EMM_dect}	16	–	16	periods	[10] IC is in idle mode	PRQ-741

(table continues...)

10 Not subject to production test; verified by design or characterization.

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Table 7 (continued) Electrical characteristics

$V_{VS} = V_{VS_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ERRQ pins							
ERRQ functional voltage range	V_{ERRQ}	4.75	–	V_{VS}	V	$V_{VS} \leq 20$ V	PRQ-718
ERRQ activated output voltage	V_{ERRQ_low}	0	–	0.3	V	$I_{ERRQ} \leq 1.5$ mA	PRQ-717
ERRQ sink current	I_{ERRQ}	–	–	1.5	mA	10)	PRQ-1340
ERRQ_res input voltage range "low"	$V_{ERRQ_res_low}$	0	–	0.99	V	–	PRQ-704
ERRQ_res input voltage range "high"	$V_{ERRQ_res_high}$	2.52	–	V_{VS}	V	–	PRQ-705
ERRQ_ext input voltage range "low"	$V_{ERRQ_ext_low}$	0	–	0.99	V	–	PRQ-706
ERRQ_ext input voltage range "high"	$V_{ERRQ_ext_high}$	2.52	–	V_{VS}	V	–	PRQ-707
ERR_loc_out output voltage	$V_{ERR_loc_out_low}$	0	–	0.45	V	$I_{ERR_loc_out} \leq 5$ mA	PRQ-708
ERR_loc_out output voltage "high"	$V_{ERR_loc_out_high}$	V_{VIO} - 0.45	–	V_{VIO}	V	$I_{ERR_loc_out} \geq -5$ mA	PRQ-709
ERR_ext_out output voltage "low"	$V_{ERR_ext_out_low}$	0	–	0.45	V	$I_{ERR_ext_out} \leq 5$ mA	PRQ-710
ERR_ext_out output voltage high	$V_{ERR_ext_out_high}$	V_{VIO} - 0.45	–	V_{VIO}	V	$I_{ERR_ext_out} \geq -5$ mA	PRQ-711

(table continues...)

10 Not subject to production test; verified by design or characterization.

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Table 7 (continued) Electrical characteristics

$V_{VS} = V_{VS_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ERRQ_ext internal pull-up resistor	$R_{ERRQ_ext_pu}$	200	300	400	kΩ	Connected to an internal 3.3 V supply	PRQ-712
ERRQ_res internal pull-up resistor	$R_{ERRQ_res_pu}$	200	300	400	kΩ	Connected to an internal 3.3 V supply	PRQ-713
ERRQ_ext input deglitch	$t_{ERRQ_ext_deglitch}$	47.26	49.74	52.42	ms	10)	PRQ-714
ERRQ_res input deglitch	$t_{ERRQ_res_deglitch}$	844	951	1067	µs	10)	PRQ-715
ERR_loc_out active time	$t_{ERR_loc_out}$	281.32	293.74	307.2	ms	10)	PRQ-716

10 Not subject to production test; verified by design or characterization.

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8 Application information

8.1 External circuitry and components

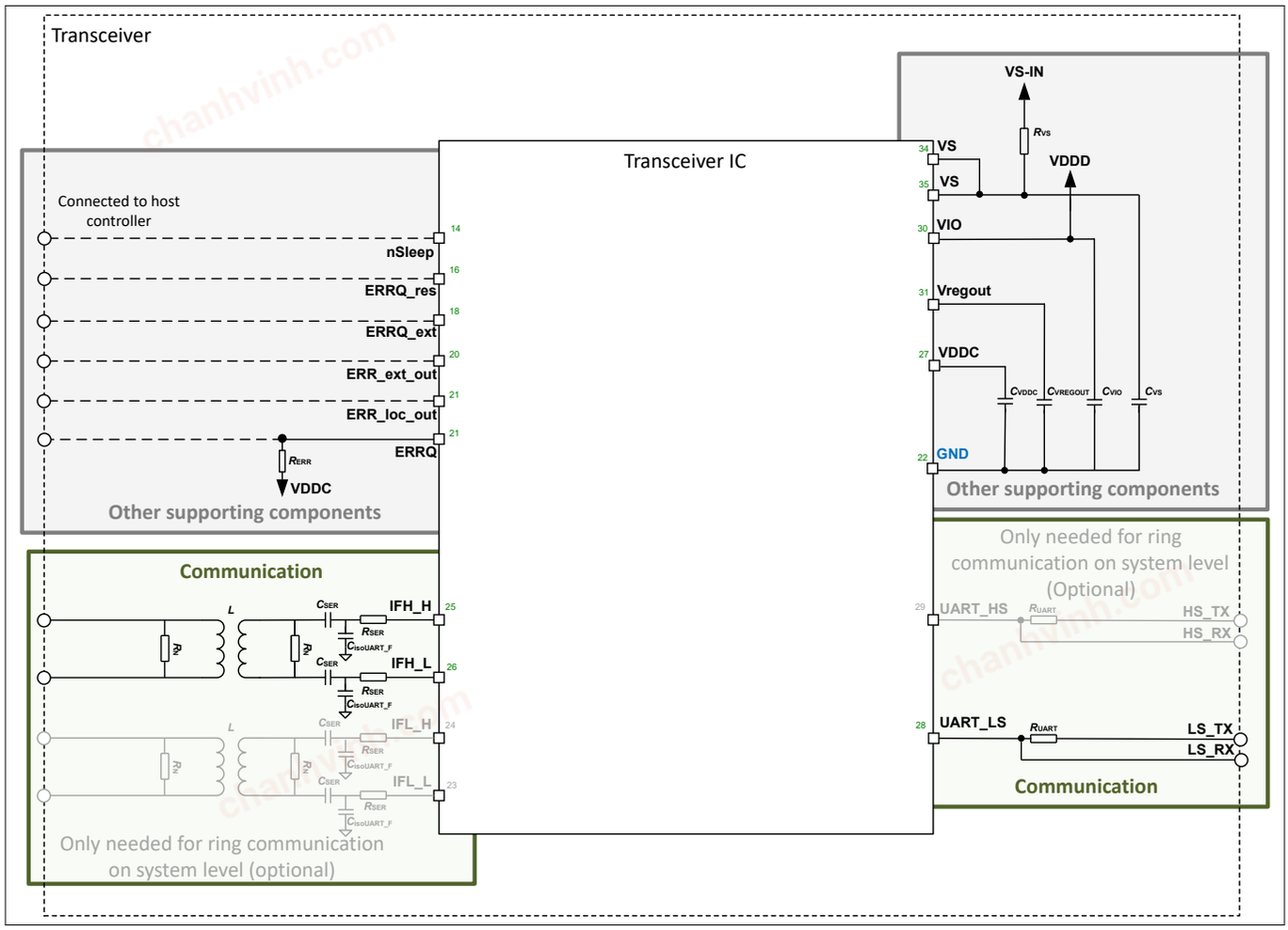


Figure 7 External circuitry transceiver IC

Table 8 External components

Buffer capacitor VS	C_{VS}	100	nF	
Filtering resistor VS	R_{VS}	5.1	Ω	
Buffer capacitor on VREGOUT	$C_{VREGOUT}$	100	nF	
Buffer capacitor on VIO	C_{VIO}	100	nF	If VIO is connected to VREGOUT, then C_{VIO} is omitted.
Buffer capacitor on VDDC	C_{VDDC}	330	nF	
Bypass capacitor on iso UART	$C_{isoUART_F}$	220	pF	

(table continues...)

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Table 8 (continued) External components

Damping resistor	R_N	1	kΩ	With Pulse HM2116ANL transformer
UART network	R_{UART}	1	kΩ	$\tau \leq 50$ ns
Transformer	L	–	–	Transformer L from Pulse HM2116ANL.

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9 Package information

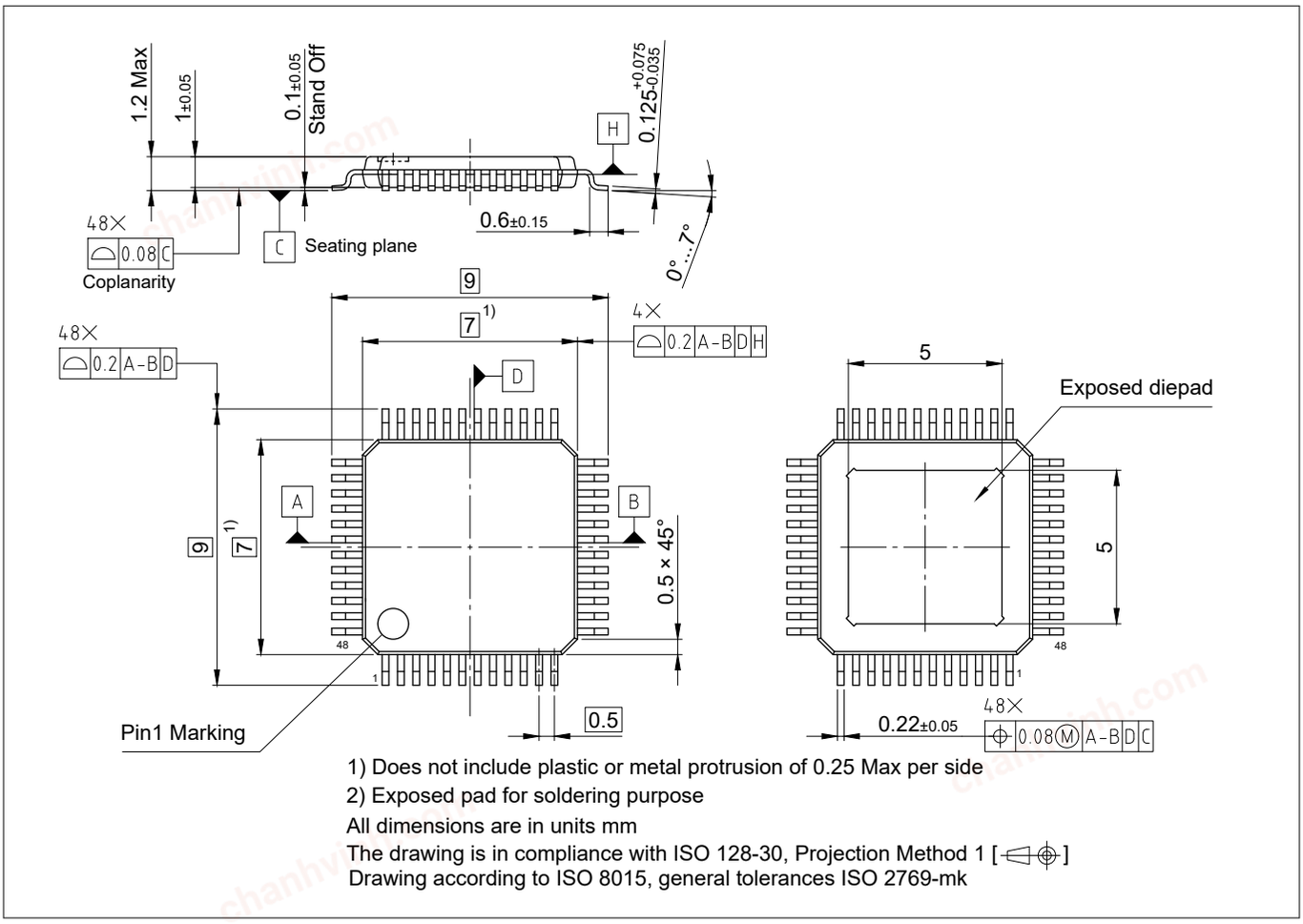


Figure 8 PG-TQFP-48

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on alternative packages

Please visit www.infineon.com/packages.

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Revision history

Revision	Date	Changes
1.0	2022-01-24	Initial release of datasheet

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