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Never stop thinking

TLE8366

1.8A DC/DC Step-Down Voltage Regulator

TLE8366EV50
TLE8366EV
TLE8366EV33

Data sheet

Rev. 1.0, 2009-05-18

Automotive Power

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1.8A DC/DC Step-Down Voltage Regulator TLE8366

AEC Qualified RoHS

1 Overview

- 1.8A step down voltage regulator
- Output voltage versions: 5.0 V, 3.3 V and adjustable
- ± 2% output voltage tolerance (+-4% for full load current range)
- Integrated power transistor
- PWM regulation with feedforward
- Input voltage range from 4.75V to 45V
- 370 kHz switching frequency
- Synchronization input
- Very low shutdown current consumption (<2uA)
- Soft-start function
- Input undervoltage lockout
- Suited for automotive applications: T_j = -40 °C to +150 °C
- Green Product (RoHS compliant)
- AEC Qualified



PG-DSO-8

Description

The TLE8366 is a PWM step-down DC/DC converter with an integrated 1.8 A power switch, packaged in a small PG-DSO-8 with exposed pad. There are three versions available, two fixed voltage with 5.0 V (TLE8366EV50) or 3.3 V (TLE8366EV33) and a variable voltage variant named TLE8366EV with a reference feedback voltage of only 600 mV. The wide input voltage range from 4.75 to 45 V makes the TLE8366 suitable for a wide variety of applications. The device is designed to be used under harsh automotive environment.

The switching frequency of nominal 370 kHz allows the use of small and cost-effective inductors and capacitors, resulting in a low, predictable output ripple and in minimized consumption of board space. (If desired the device could be synchronized to an external frequency source between 200 and 530 kHz.)

The TLE8366 includes safety features such as a cycle-by-cycle current limitation, over-temperature shutdown and input under voltage lockout. The enable function, in shutdown mode with less than 2 µA current consumption, enables easy power management in battery-powered systems.

The voltage regulation loop provides an excellent line and load regulation. The stability of the loop could be adjusted by using an external compensation network. This compensation network combined with voltage mode regulation and a feed-forward control path guarantees a highly effective line transient rejection. During start-up the integrated soft-start limits the inrush current peak and prevents from a voltage overshoot.

Type	Package	Marking
TLE8366EV50	PG-DSO-8	8366EV50
TLE8366EV33	PG-DSO-8	8366EV33
TLE8366EV	PG-DSO-8	8366EV

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2 Block Diagram

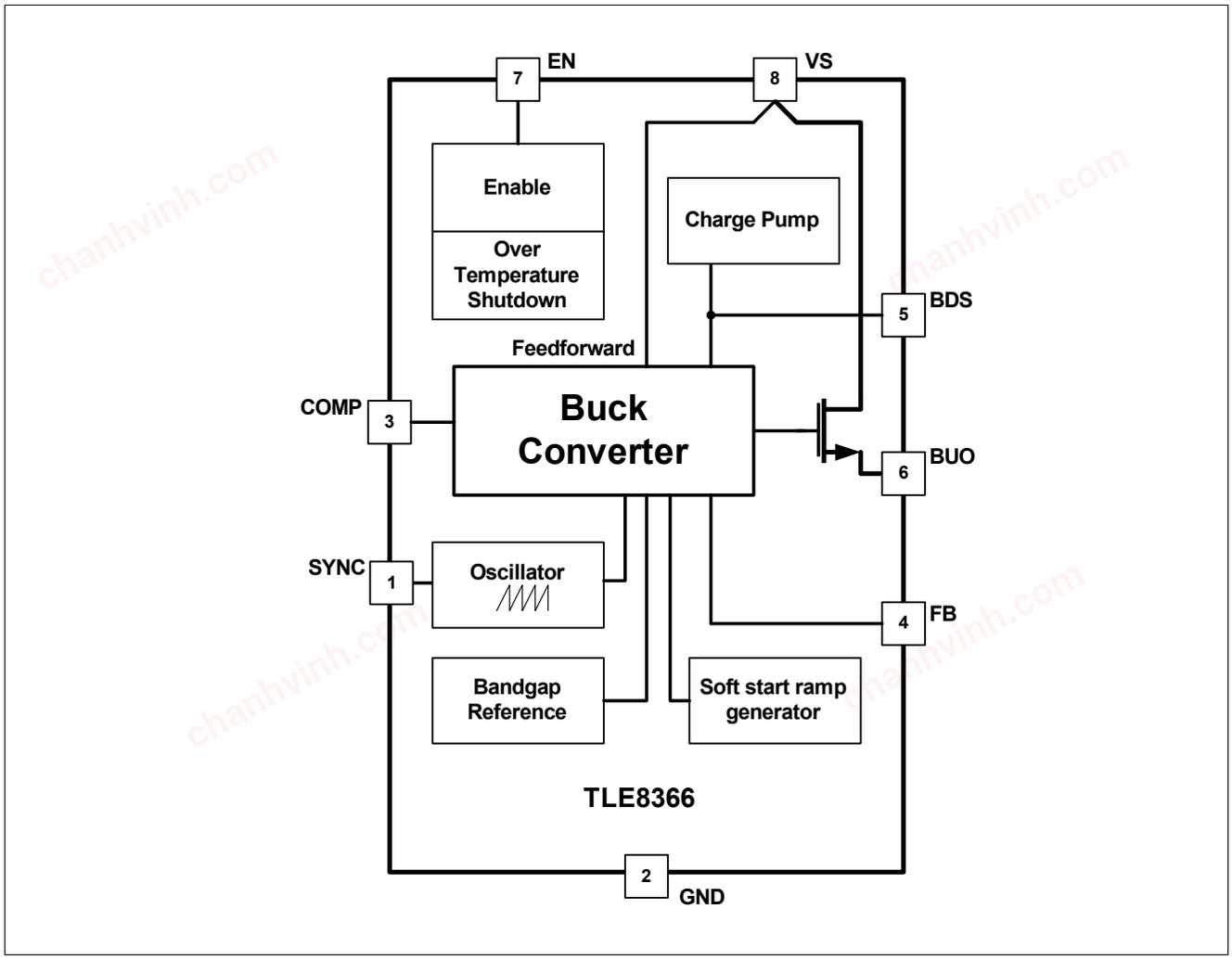


Figure 1 Block Diagram

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3 Pin Configuration

3.1 Pin Assignment

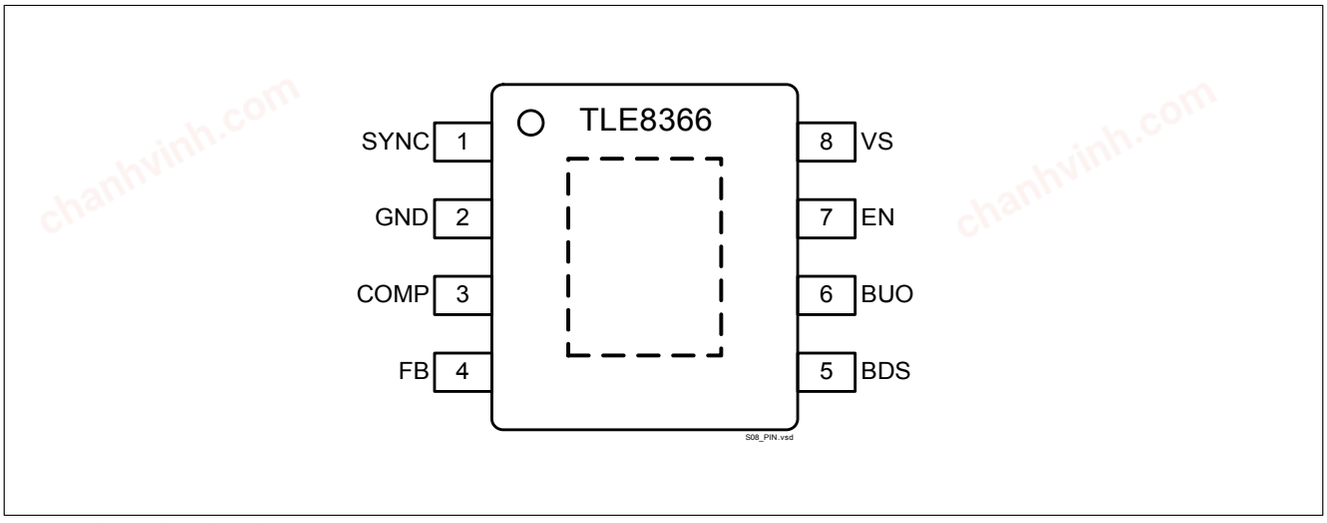


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	SYNC	**Synchronization Input.** Connect to an external clock signal in order to synchronize/adjust the switching frequency. If not used connect to GND.
2	GND	**Ground.**
3	COMP	**Compensation Input.** Frequency compensation for regulation loop stability. Connect to compensation RC-network.
4	FB	**Feedback Input.** For the adjustable output voltage versions (TLE8366EV) connect via voltage divider to output capacitor. For the fixed voltage version (TLE8366EV50, TLE8366EV33) connect this pin directly to the output capacitor.
5	BDS	**Buck Driver Supply Input.** Connect the bootstrap capacitor between this pin and pin BUO.
6	BUO	**Buck Switch Output.** Source of the integrated power-DMOS transistor. Connect directly to the cathode of the catch diode and the buck circuit inductance.
7	EN	**Enable Input.** Active-high enable input with integrated pull down resistor.
8	VS	**Supply Voltage Input.** Connect to supply voltage source.
Exposed Pad		Connect to heatsink area and GND by low inductance wiring.

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4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Synchronization Input	V_{SYNC}	-0.3	5.5	V	–
				6.2	V	t < 10s[2)]
4.1.2	Compensation Input	V_{COMP}	-0.3	5.5	V	–
4.1.3				6.2	V	t < 10s[2)]
4.1.4	Feedback Input	V_{FB}	-0.3	10	V	TLE8366EV50; TLE8366EV33
4.1.5			-0.3	5.5	V	TLE8366EV
4.1.6	Buck Driver Supply Input	V_{BDS}	V_{BUO} - 0.3	V_{BUO} + 5.5	V	
4.1.7	Buck Switch Output	V_{BUO}	-2.0	V_{VS} + 0.3	V	
4.1.8	Enable Input	V_{EN}	-40	45	V	
4.1.9	Supply Voltage Input	V_{VS}	-0.3	45	V	
Temperatures						
4.1.10	Junction Temperature	T_j	-40	150	°C	–
4.1.11	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.12	ESD Resistivity	V_{ESD}	-2	2	kV	HBM [3)]
4.1.13	ESD Resistivity to GND	V_{ESD}	-500	500	V	CDM [4)]
4.1.14	ESD Resistivity corner pins to GND	V_{ESD}	-750	750	V	CDM [4)]

1) Not subject to production test, specified by design

2) Exposure to those absolute maximum ratings for extended periods of time (t > 10s) may affect device reliability

3) ESD susceptibility HBM according to EIA/JESD 22-A 114B (1.5kΩ,100pF).

4) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

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4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage	V_S	4.75	45	V	–
4.2.2	Output Voltage adjust range	V_{CC}	0.60	16	V	TLE8366EV
4.2.3	Buck inductor	L_{BU}	18	56	µH	–
4.2.4	Buck capacitor	C_{BU1}	33	120	µF	–
4.2.5	Buck capacitor ESR	ESR_{BU1}	–	0.3	Ω	– 1)
4.2.6	Junction Temperature	T_j	-40	150	°C	–

1) See section "**"Application Information" on Page 14**" for loop compensation requirements.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1)]	R_{thJC}	–	10	12	K/W	–
4.3.2	Junction to ambient[1)]	R_{thJA}	–	52	–	K/W	2)

1) Not subject to production test, specified by design.

2) According to Jedec JESD52-1,-5,-7 at natural convection on 2s2p FR4 PCB for 1W power dissipation. PCB 76.2x114.3x1.5mm^3 with 2 inner copper layers of 70µm thickness. Thermal via array conected to the first inner copper layer under the exposed pad.

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5 Buck Regulator

5.1 Description

5.1.1 Arrangement

The step-down (or buck) regulator consists of several functional blocks, which shall be explained in the following: The oscillator, the regulator, the safety functions, the gate driver and the internal MOSFET.

5.1.1.1 Regulator Block

The oscillator creates a saw-tooth signal, which is supplied to the PWM comparator and the Schmitt-Trigger 1. The frequency of the oscillator might be synchronized to an external frequency connected to pin sync.

The Error Amplifier compares the feedback signal to the reference voltage. At the variable voltage version the feedback pin shall be connected to an external resistor divider, the fixed voltage versions contain an internal resistor divider. The soft start function is included by the ramp generator between the reference voltage source and the error amplifier. It generates a defined ramp after the initialization of the device. (The device is initialized after signal EN turns to high (with supply voltage at VS present) or with rising Supply voltage (with EN = H connected to VS) or at restarting after a thermal shutdown. The ramp starts, if the Buck Driver Supply (BDS) external capacitor is charged.

Only for the variable voltage version: If the feedback signal at pin FB gets lost, an internal pull-up current source will pull the pin too high thus preventing the output voltage from overshooting.

A compensation network needs to be connected to the output of the error amplifier using pin COMP.

The PWM comparator creates the Pulse-Width Modulated (PWM) signal by comparing the error amplifier output with the saw-tooth signal from the oscillator.

5.1.1.2 Safety Functions Block

The safety functions block consists of the Error-Flip Flop, the Nor1 Gate and the PWM-Flip-Flop.

The Error Flip-Flop collects the failure events such as the over-current shutdown of the internal MOSFET, the output overvoltage shutdown and the temperature shutdown.

The over-current shutdown signal is created by the OC comparator. It detects the voltage across an internal shunt resistor. If the current exceeds the reference level, the pulse is shut down and the MOSFET switched off.

The bootstrap under-voltage shutdown is created by the BDS UV comparator, which compares the bootstrap capacitor voltage to a reference level. If the bootstrap capacitor voltage is too low, the pulse will be shut down and the MOSFET switched off.

If the output voltage exceeds a reference value, the pulse will also be shut down and the MOSFET switched off.

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An internal temperature sensor detects the temperature of the device, it will be switched off if the junction temperature exceeds 175 °C.

The error Flip flop is set by the Schmitt Trigger 1 and will be reset by one of these signals. This will close the NOR1 gate and shutdown the pulse. The bootstrap capacitor monitoring is connected directly to the NOR1 gate.

The bootstrap under-voltage shutdown is created by the BDS UV comparator, which compares the bootstrap capacitor voltage to a reference level. If the bootstrap capacitor voltage is too low, the pulse will be shut down.

PWM pulses are passing through the NOR 1 gate. In case if one of the mentioned failures will occur this gate will be closed and the pulse switched immediately off.

The PWM Flip-Flop is set by NAND2, which combines the clock from the Schmitt Trigger 1 with the output from NOR1. The PWM Flip-Flop is reset by the output of the NOR1.

5.1.1.3 Internal Power Stage

The gate driver consists of the Gate driver itself, an inverter for the PWM signal and the gate driver supply. The gate Driver Supply is connected over pin BDS to the BDS capacitor. A charge pump is integrated to support the gate drive in cases of low input voltage, small differential voltage between input supply and output voltage and during start up. To minimize emissions the charge pump is switched off if the input voltage is high enough to charge the bootstrap capacitor.

5.1.2 Operation Mode

The PWM pulses are voltage controlled. The error amplifier and the PWM comparator are creating the PWM pulses using the oscillator saw-tooth signal and the feedback voltage. The pulse-width modulation is done so that the feedback voltage (at pin FB for the adjustable version) is similar to the reference voltage (0.6 V).

Between input voltages from 8.0 to 36 V the integrated feed forward path provides a fast line transient rejection. (feed-forward means sensing the input voltage and react on fluctuations before they influence the output)

To achieve a stable output voltage even under low duty cycle conditions (light load down to zero output load and/or high input voltage) a pulse skipping mode is implemented. Pulse skipping is also used for operation with low supply voltages leading to duty cycles > 92%.

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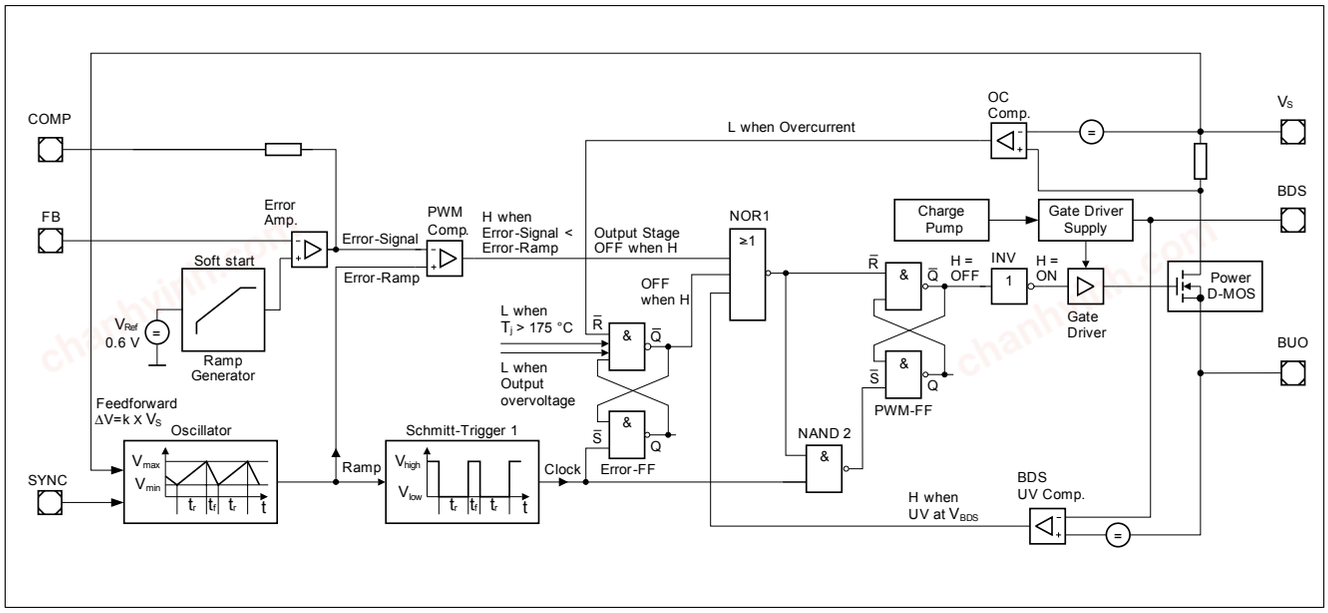


Figure 3 Block Diagram Buck Regulator

5.2 Electrical Characteristics

Electrical Characteristics: Buck Regulator

V_S = 6.0 V to 40 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Output voltage	V_{FB}	4.90	5.00	5.10	V	TLE8366EV50; $V_{VEN} = V_S$ 0.1A < I_{CC} < 1.0A
5.2.2		V_{FB}	4.80	5.00	5.20	V	TLE8366EV50; $V_{VEN} = V_S$; 1mA < I_{CC} < 1.8A
5.2.3	Output voltage	V_{FB}	3.23	3.30	3.37	V	TLE8366EV33; $V_{VEN} = V_S$; 0.1A < I_{CC} < 1.0A
5.2.4		V_{FB}	3.17	3.30	3.43	V	TLE8366EV33; $V_{VEN} = V_S$; 1mA < I_{CC} < 1.8A
5.2.5	Output voltage	V_{FB}	0.588	0.60	0.612	V	TLE8366EV; $V_{VEN} = V_S$; FB connected to V_{CC}; V_S = 12V 0.1A < I_{CC} < 1.0A
5.2.6		V_{FB}	0.576	0.60	0.624	V	TLE8366EV; $V_{VEN} = V_S$; FB connected to V_{CC}; V_S = 12V 1mA < I_{CC} < 1.8A

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Electrical Characteristics: Buck Regulator

V_S = 6.0 V to 40 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.7	Minimum output load requirement	$I_{CC,MIN}$	0	–	–	mA	TLE8366EV50[1]
5.2.8			1	–	–	mA	TLE8366EV33[1]
5.2.9			1.5			mA	TLE8366EV V_{CC} > 3V[1]
5.2.10			5			mA	TLE8366EV V_{CC} > 1.5V[1]
5.2.11			10	–	–	mA	TLE8366EV V_{CC} ≥ 0.6V[1]
5.2.12	FB input current	I_{FB}	-1	-0.1	0	µA	TLE8366EV V_{FB} = 0.6V
5.2.13	FB input current	I_{FB}	–	–	900	µA	TLE8366EV50, TLE8366EV33
5.2.14	Power stage on-resistance	R_{on}	–	–	500	mΩ	tested at 300 mA
5.2.15	Current transition rise/fall time	t_r	–	50	–	ns	I_{CC}=1 A [2]
5.2.16	Buck peak over current limit	I_{BUOC}	2.2	–	3.6	A	–
5.2.17	Bootstrap under voltage lockout, turn-off threshold	$V_{BDS,off}$	V_{BUO} +3.3	–	–	V	Bootstrap voltage decreasing
5.2.18	Charge pump current	I_{CP}	2	–	–	mA	V_S = 12V; V_{BUO} = V_{BDS} = GND
5.2.19	Charge pump switch-off threshold	V_{BDS} - V_{BUO}	–	–	5	V	(V_{BDS} - V_{BUO}) increasing
5.2.20	Maximum duty cycle	D_{max}	–	–	100	%	[3]
5.2.21	Soft start ramp	t_{start}	350	500	750	µs	V_{FB} rising from 5% to 95% of $V_{FB,nom}$
5.2.22	Input under voltage shutdown threshold	$V_{S,off}$	3.75	–	–	V	V_S decreasing
5.2.23	Input voltage startup threshold	$V_{S,on}$	–	–	4.75	V	V_S increasing
5.2.24	Input under voltage shutdown hysteresis	$V_{S,hyst}$	150	–	–	mV	–

1) Not subject to production test, application related parameter
2) Not subject to production test; specified by design.
3) Consider “**Chapter 4.2, Functional Range**”

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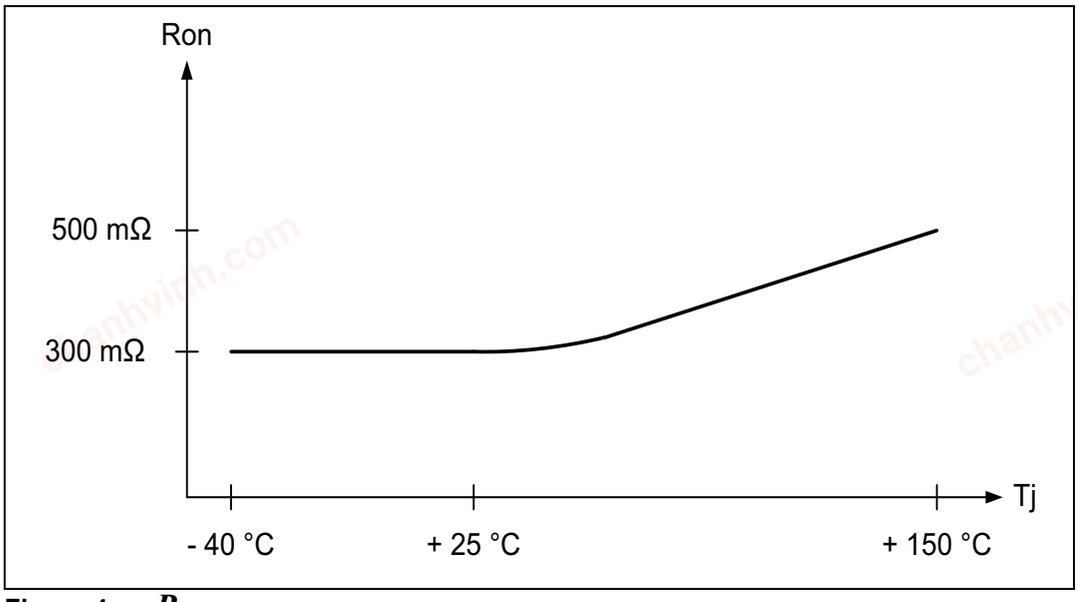


Figure 4 R_{on}

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6 Module Enable and Thermal Shutdown

6.1 Description

With the enable pin the device can be set in off-state reducing the current consumption to less than 2µA.

The enable function features an integrated pull down resistor which ensures that the IC is shut down and the power switch is off in case the pin EN is left open.

The integrated thermal shutdown function turns the power switch off in case of overtemperature. The typ. junction shutdown temperature is 175°C, with a min. of 160°C. After cooling down the IC will automatically restart operation. The thermal shutdown is an integrated protection function designed to prevent IC destruction when operating under fault conditions. It should not be used for normal operation.

6.2 Electrical Characteristics Module Enable, Bias and Thermal Shutdown

Electrical Characteristics: Enable, Bias and Thermal Shutdown

V_S = 6.0 V to 40 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.2.1	Current Consumption, shut down mode	$I_{q,OFF}$	–	0.1	2	µA	V_{EN} = 0.8V; T_j < 105°C; V_S = 16V
6.2.2	Current Consumption, active mode	$I_{q,ON}$	–	–	7	mA	V_{EN} = 5.0V; I_{CC} = 0mA; V_S = 16V FB connected to V_{OUT}
6.2.3	Current Consumption, active mode	$I_{q,ON}$	–	–	10	mA	V_{EN} = 5.0V; I_{CC} = 1.8A; V_S = 16V FB connected to V_{OUT} 1)
6.2.4	Enable high signal valid	$V_{EN,lo}$	3.0	–	–	V	–
6.2.5	Enable low signal valid	$V_{EN,hi}$	–	–	0.8	V	–
6.2.6	Enable hysteresis	$V_{EN,HY}$	50	200	400	mV	1)
6.2.7	Enable high input current	$I_{EN,hi}$	–	–	30	µA	V_{EN} = 16V
6.2.8	Enable low input current	$I_{EN,lo}$	–	0.1	1	µA	V_{EN} = 0.5V
6.2.9	Over temperature shutdown	$T_{j,sd}$	160	175	190	°C	1)
6.2.10	Over temperature shutdown hysteresis	T_{j,sd_hyst}	–	15	–	K	1)

1) Specified by design. Not subject to production test.

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7 Module Oscillator

7.1 Description

The oscillator supplies the device with a constant frequency. The power switch will be switched on and off with a constant frequency. The duty-cycle is derived from this frequency and some safety functions are synchronized to this frequency.

The internal sawtooth signal used for the PWM generation has an amplitude proportional to the input supply voltage (feedforward).

The turn-on frequency can optionally be set externally via the 'SYNC' pin. In this case the synchronization of the PWM-on signal refers to the falling edge of the 'SYNC'-pin input signal. In case the synchronization to an external clock signal is not needed the 'SYNC' pin should be connected to GND.

Leaving pin SYNC open or short-circuiting it to GND leads to normal operation with the internal switching frequency.

7.2 Electrical Characteristics Module Oscillator

Electrical Characteristics: Buck Regulator

V_S = 6.0 V to 40 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.2.1	Oscillator frequency	f_{osc}	330	370	420	kHz	V_{SYNC} = 0V
7.2.2	Synchronization capture range	f_{sync}	200		530	kHz	
7.2.3	SYNC signal high level valid	$V_{SYNC,hi}$	2.9			V	1)
7.2.4	SYNC signal low level valid	$V_{SYNC,lo}$			0.8	V	1)
7.2.5	SYNC input internal pull-down	R_{SYNC}	0.60	1.0	1.4	MΩ	V_{SYNC} = 5V

1) Synchronization of PWM-on signal to falling edge.

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8 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

8.1 Frequency Compensation

The stability of the output voltage can be achieved with a simple RC connected between pin COMP and GND. The standard configuration using the swiching frequency of the internal oscillator is a ceramic capacitor C_{COMP} = 22nF and R_{COMP} = 22kΩ. By slight modifications to the compensation network the stability can be optimized for different application needs, such as varying switching frequency (using the sychronizing function), different types of buck capacitor (ceramic or tantalum) etc.

The compensation network is essential for control loop stability. Leaving pin COMP open might lead to instable operation.

8.2 Compensating a tantalum buck capacitor C_{BU1}

The control loop is optimized for use of ceramic buck capacitors C_{BU}. In order to maintain stability also for tantalum capacitors with ESR up to 300mΩ, an additional compensation capacitance C_{COMP2} at pin COMP to GND is required. It's value calculates:

$$C_{COMP2} = C_{BU} * ESR(C_{BU}) / R_{COMP} ,$$

whereas C_{COMP2} needs to stay below 5nF.

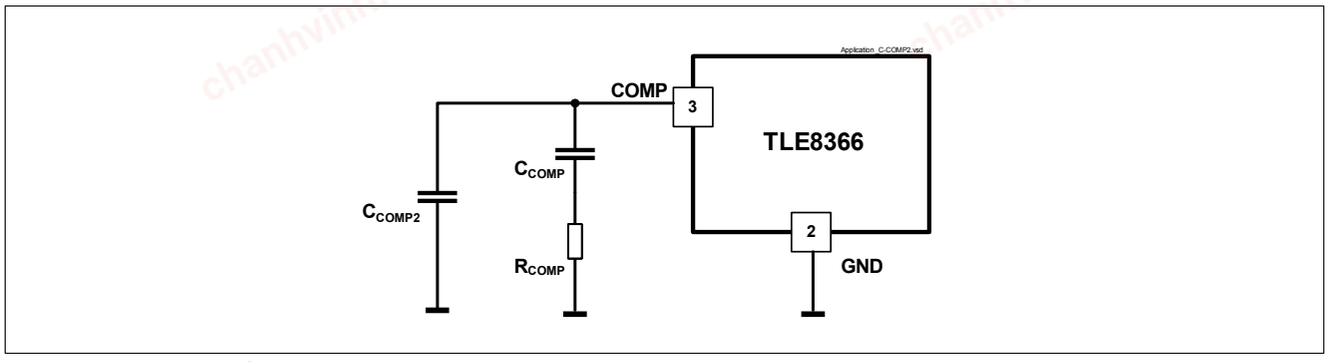


Figure 5 High-ESR buck capacitor compensation

8.3 Catch Diode

In order to minimize losses and for fast recovery, a schottky catch diode is required. Disconnecting the catch diode during operation might lead to destruction of the IC.

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8.4 TLE8366EV50, TLE8366EV33 with fixed Output Voltage

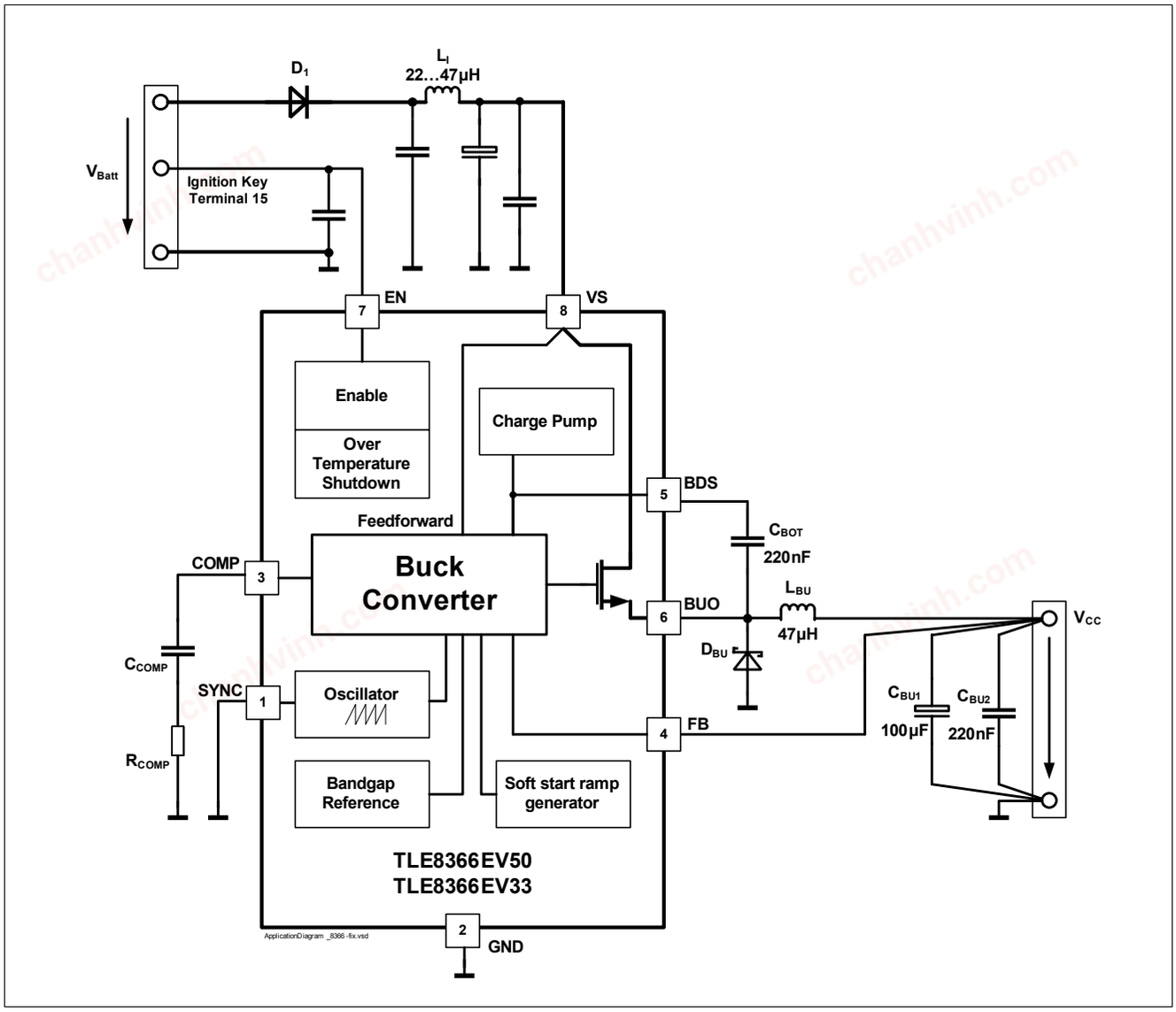


Figure 6 Application Diagram TLE8366EV50 or TLE8366EV33

Note: This is a very simplified example of an application circuit. The function must be verified in the real application

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8.5 Adjustable Output Voltage Device

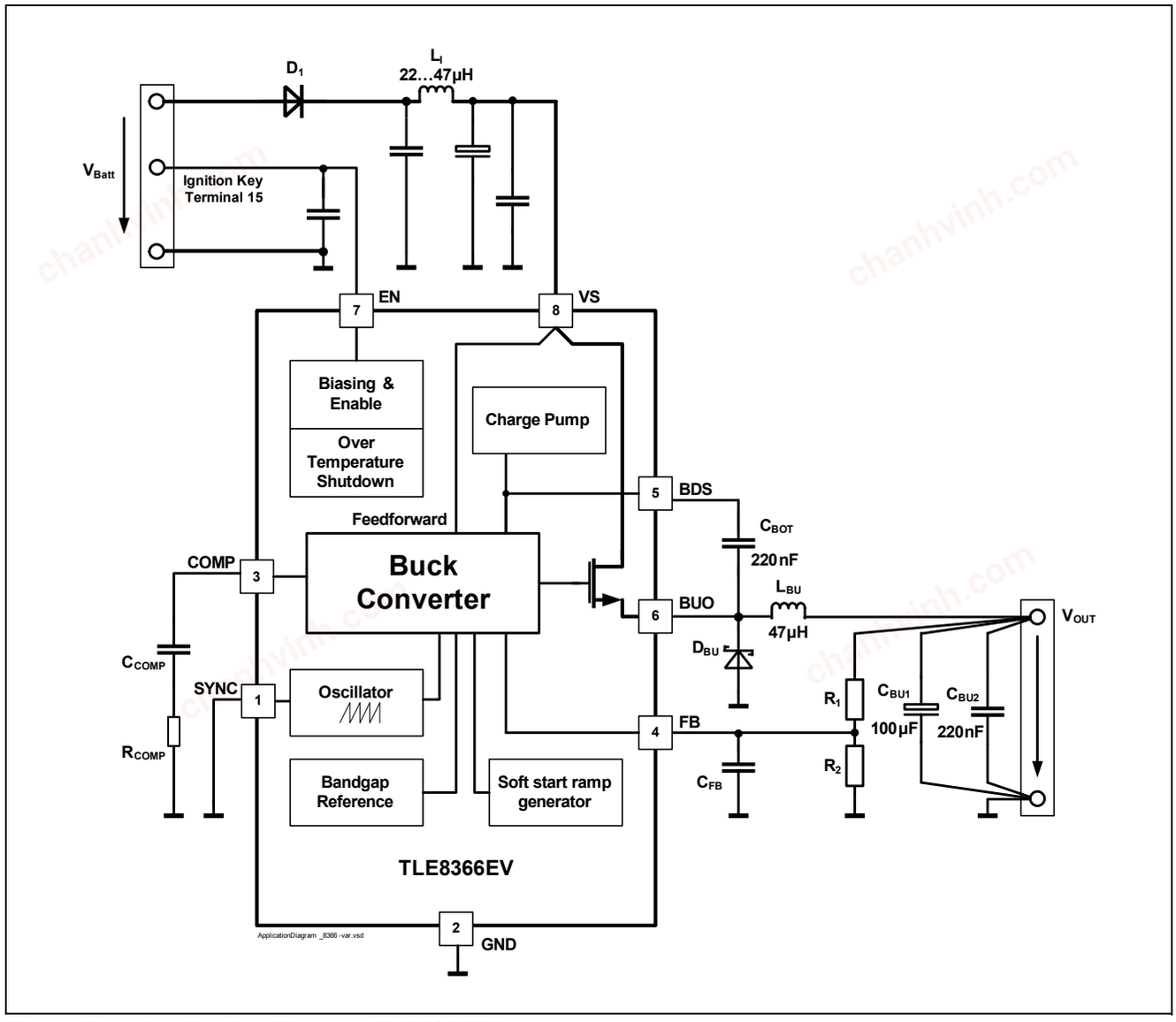


Figure 7 Application Diagram TLE8366EV

Note: This is a very simplified example of an application circuit. The function must be verified in the real application

The output voltage of the TLE8366EV can be programmed by a voltage divider connected to the feedback pin FB. The divider cross current should be 300 µA at minimum, therefore the maximum R_2 calculates:

$$R_2 \leq V_{FB} / I_{R2} \quad \text{-->} \quad R_2 \leq 0.6\text{V} / 300\ \mu\text{A} = 2\ \text{k}\Omega$$

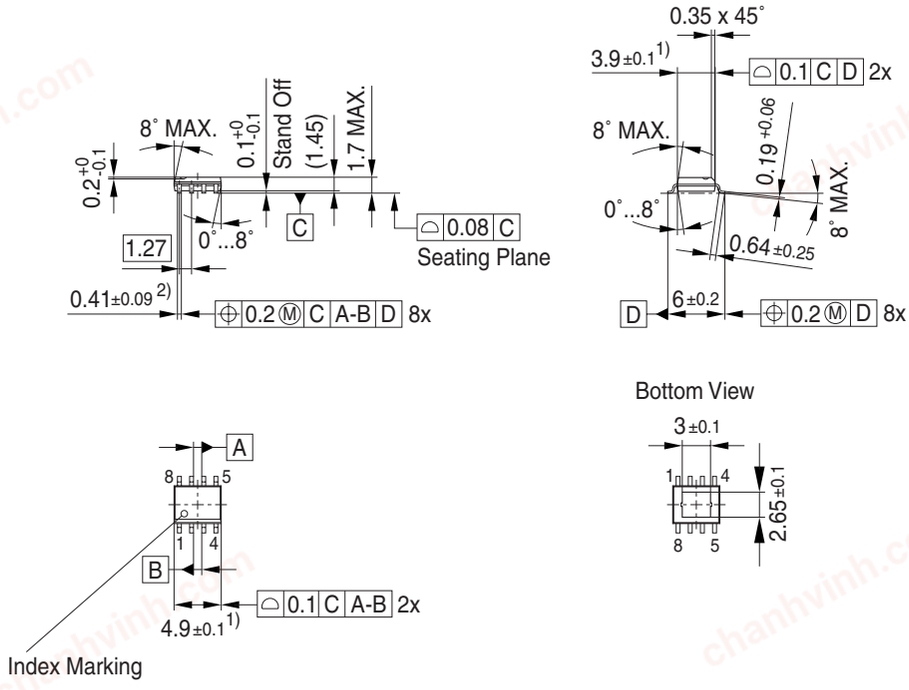
For the desired output voltage level V_{CC}, R_1 calculates then (neglecting the small FB input current):

$$R_1 = R_2\left(\frac{V_{CC}}{V_{FB}} - 1\right).$$

Add a 0.5 nF capacitor close to FB pin.

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9 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area
3) JEDEC reference MS-012 variation BA

GPS01206

Figure 9 Outline PG-DSO-8

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further package information, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

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10 Revision History

Rev

Version	Date	Changes
Rev.1.0	2009-05-18	Final data sheet

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