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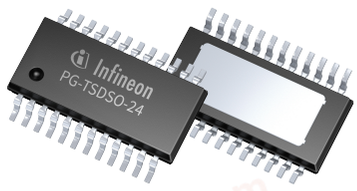
TLE8082ES

Small engine management IC

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Features



- Power supplies
  - Voltage pre-regulator with external FET
  - 5 V sensor supply (tracking 5 V supply input)
  - 5 V communication supply (tracking 5 V supply input)
- Permanent supply feature
  - dedicated KEY input
  - After-run functionality
- 4 low side drivers for inductive loads with overtemperature and overcurrent protection and open load/short to GND in off diagnosis
  - 3 low-side power stages
  - 1 low-side power stage with current measurement feature (O_2-heater)
- Window watchdog module
- Serial Peripheral Interface (SPI)
- Green Product (RoHS compliant)

Potential applications

All automotive applications, in particular

- Motorcycles, 2- and 3-wheelers and scooters
- Watercraft, marines and jet-skis
- Snow mobiles

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE8082ES is a companion IC to TLE8080-xEM or TLE8088EM that includes enhanced functions and features to support OBDII-compliant EURO5/ BHARATVI 2-/3-wheeler combustion engine systems with the focus on enhanced Electronic Fuel Injection (EFI) technologies.

It is protected against overtemperature and overcurrent and provides diagnostic features for each integrated power stage. The TLE8082ES integrates a pre-regulator for external FETs, a sensor supply, a communication supply for on-board transceivers, an SPI interface and four power stages to drive different load types used in engine management systems.

The IC is a compact and cost optimized solution to meet modern emission standards and regulations of engine management systems.

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Description

Product type	Package	Marking
TLE8082ES	PG-TSDSO-24	TLE8082ES

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1 Block diagram

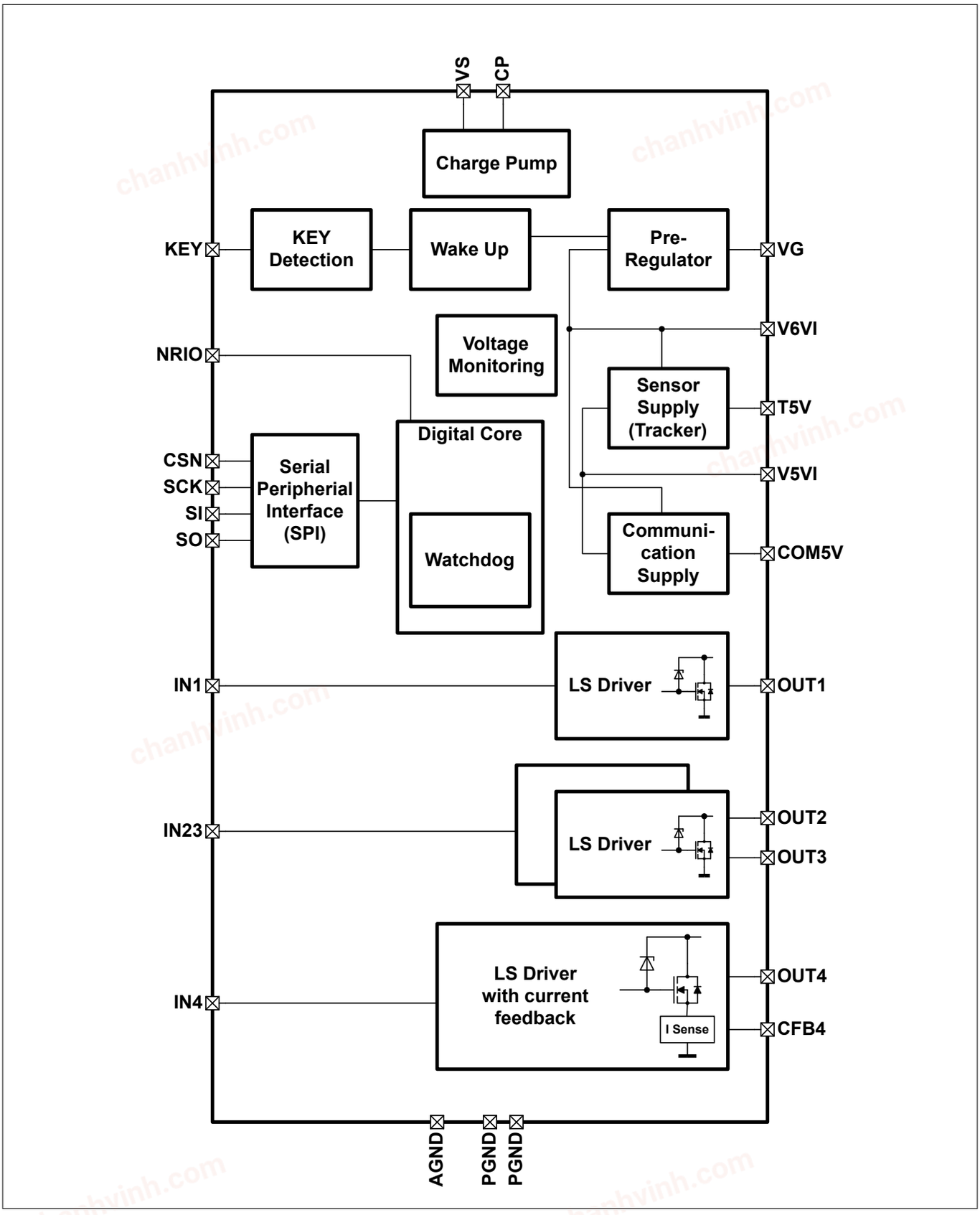


Figure 1 Block diagram

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2 Pin configuration

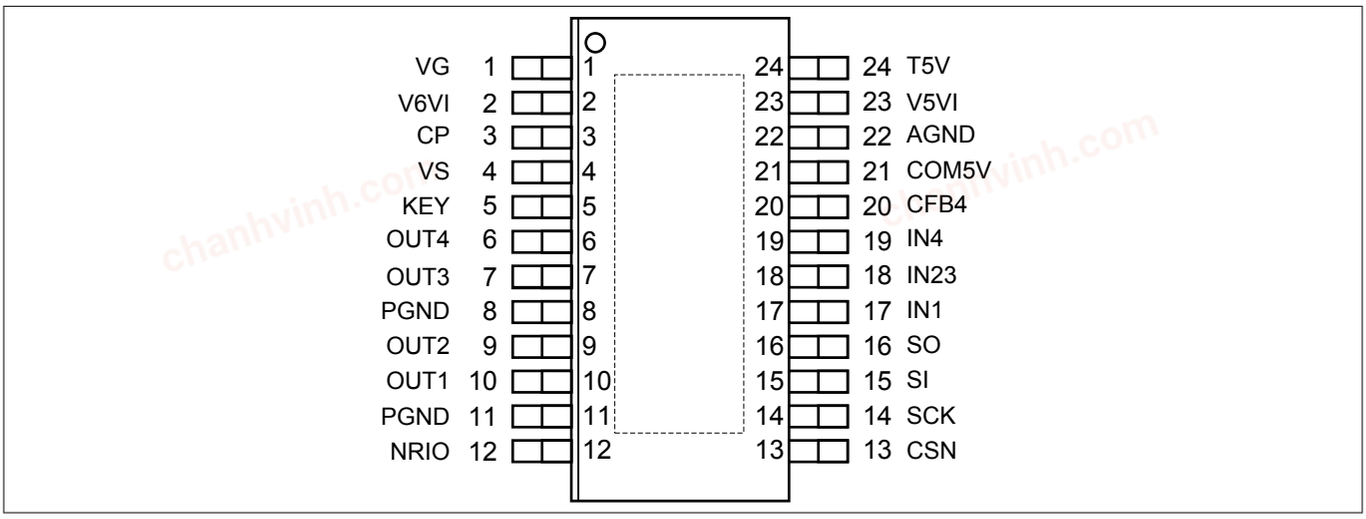


Figure 2 Pin configuration

Table 1 Pin definition and functions

Pin #	Pin name	Function	Description
1	VG	OUT	**Control Output of Pre-Regulator:** connect gate of external MOSFET, add external capacitor
2	V6VI	IN	**Pre-Regulator Control Input:** connect source of external MOSFET, supply input for sensor and communication supplies, add external capacitor
3	CP	OUT	**Charge-Pump Output:** add external capacitor
4	VS	IN	**Battery Supply Input**
5	KEY	IN	**KEY Input**
6	OUT4	OUT	**Low-Side Power Stage 4**
7	OUT3	OUT	**Low-Side Power Stage 3**
8	PGND	GND	**Power Ground:** connect to cooling tab, must be connected externally
9	OUT2	OUT	**Low-Side Power Stage 2**
10	OUT1	OUT	**Low-Side Power Stage 1**
11	PGND	GND	**Power Ground:** connect to cooling tab, must be connected externally
12	NRIO	IN/OUT	**Reset Input/Output**: open drain low active, add pull up resistor
13	CSN	IN	**SPI Slave Chip Select Input**
14	SCK	IN	**SPI Slave Clock Input**
15	SI	IN	**SPI Slave Data Input**
16	SO	OUT	**SPI Slave Data Output**
17	IN1	IN	**Control Input of Power Stage 1**
18	IN23	IN	**Control Input of Power Stage 2 and 3**
19	IN4	IN	**Control Input of Power Stage 4**

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Pin configuration

Table 1 Pin definition and functions (continued)

Pin #	Pin name	Function	Description
20	CFB4	OUT	**Current Feedback Output of Power Stage 4**
21	COM5V	OUT	**5 V Communication Supply Output:** add external capacitor
22	AGND	GND	**Signal Ground**
23	V5VI	IN	**5 V Main Supply Input:** reference voltage for sensor and communication supplies
24	T5V	OUT	**5 V Sensor Supply Output:** add external capacitor

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3 General product characteristics

3.1 Maximum ratings

Table 2 Maximum ratings

T_J = -40°C to 150°C; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Battery supply pin VS	$V_{VS,mr}$	-0.3	–	40	V		DS-34
Charge pump pin CP	$V_{CP,mr}$	-0.3	–	40	V	In addition, the maximum ratings parameter **Charge pump pin CP to pin VS** must be observed.	DS-35
Charge pump pin CP to pin VS	$V_{CP_VS,mr}$	-0.3	–	6	V	$V_{CP_VS,mr} = V_{CP} - V_{VS}$ In addition, the maximum ratings parameter **Charge pump pin CP** must be observed.	DS-36
Key detection input pin KEY	$V_{KEY,mr}$	-0.3	–	40	V		DS-37
Preregulator gate output pin VG	$V_{VG,mr}$	-0.3	–	40	V	In addition, the maximum ratings parameter **Preregulator gate output pin VG to pin CP** must be observed.	DS-38
Preregulator gate output pin VG to pin CP	$V_{VG_CP,mr}$	-40	–	0.3	V	$V_{VG_CP,mr} = V_{VG} - V_{CP}$ In addition, the maximum ratings parameter **Preregulator gate output pin VG** must be observed.	DS-40
6V input pin V6VI	$V_{V6VI,mr}$	-0.3	–	40	V		DS-41
Sensor supply output pin T5V	$V_{T5V,mr}$	-1	–	40	V		DS-42
5V supply input V5VI	$V_{V5VI,mr}$	-0.3	–	5.5	V		DS-43
Analog ground pin AGND	$V_{AGND,mr}$	-0.3	–	0.3	V	related to PGND	DS-44
Communication supply output COM5V	$V_{COM5V,mr}$	-0.3	–	5.5	V		DS-45

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Table 2 Maximum ratings (continued)

T_J = -40°C to 150°C; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current feedback ouput pin CFB4	$V_{CFB4,mr}$	-0.3	–	5.5	V		DS-46
Direct input pin IN1	$V_{IN1,mr}$	-0.3	–	5.5	V		DS-47
Direct drive input pin IN23	$V_{IN23,mr}$	-0.3	–	5.5	V		DS-264
Direct drive input pin IN4	$V_{IN4,mr}$	-0.3	–	5.5	V		DS-48
SPI output pin SO	$V_{SO,mr}$	-0.3	–	5.5	V	In addition, the maximum ratings parameter **SPI output pin SO to pin V5VI** must be observed.	DS-49
SPI output pin SO to pin V5VI	$V_{SO,V5VI,mr}$	-5.5	–	0.3	V	$V_{SO,V5VI,mr} = V_{SO} - V_{V5VI}$ In addition, the maximum ratings parameter **SPI output pin SO** must be observed.	DS-266
SPI input pin SI	$V_{SI,mr}$	-0.3	–	5.5	V		DS-50
SPI clock input pin SCK	$V_{SCK,mr}$	-0.3	–	5.5	V		DS-51
SPI chip select input pin CSN	$V_{CSN,mr}$	-0.3	–	5.5	V		DS-52
Reset input output pin NRIO	$V_{NRIO,mr}$	-0.3	–	5.5	V		DS-53
Power stage output OUT1	$V_{OUT1,mr}$	-0.3	–	50	V	repetitive clamping allowed	DS-54
Power stage output OUT2	$V_{OUT2,mr}$	-0.3	–	50	V	repetitive clamping allowed	DS-55
Power stage output OUT3	$V_{OUT3,mr}$	-0.3	–	35	V	repetitive clamping allowed	DS-56
Power stage output OUT4	$V_{OUT4,mr}$	-0.3	–	35	V	repetitive clamping allowed	DS-57

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Electrostatic Discharge Robustness

Table 3 Electrostatic Discharge Robustness

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
HBM ESD robustness for global pins	$V_{HBM,glo}$	-4	–	4	kV	acc. ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF) for pins VS, V6VI, T5V, KEY, OUT1-4 to PGND	DS-58
HBM ESD robustness for local pins	$V_{HBM,loc}$	-2	–	2	kV	acc. ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF) remaining pins	DS-59
CDM ESD robustness corner pins	$V_{CDM,cor}$	-750	–	750	V	acc. JESD22-C101 corner pins 1, 12, 13, 24	DS-60
CDM ESD robustness remaining pins	V_{CDM}	-500	–	500	V	acc. JESD22-C101 remaining pins	DS-61

Note: A "local" pin carries a signal or power which does not leave the application board. It remains on the application PCB as a signal between two components.
A "global" pin carries a signal or power which enters or leaves the application board without any active component in between.

3.3 Thermal resistance

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal resistance junction to case	$R_{th,j-c}$	–	1.3	1.5	K/W		DS-288

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3.4 Functional range

Table 5 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage in normal operation range	$V_{VS,nop}$	6	–	40	V		DS-62
Supply voltage in low battery condition	$V_{VS,low}$	3.5	–	6	V		DS-63
Operating temperature range	T_J	-40	–	150	°C		DS-64
Storage temperature range	T_{stg}	-55	–	150	°C		DS-65

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4 Operation behavior

4.1 Operation states

The TLE8082ES implements 11 operations states:

- Sleep state
- Wake-up state
- Power on reset (POR) state
- Normal operation watchdog (WD) inactive state
- Normal operation watchdog (WD) safe state
- Normal operation watchdog (WD) ready state
- Afterrun watchdog safe state
- Afterrun watchdog ready state
- External reset state
- Error state and
- Reset timer state

4.1.1 State diagram

The state diagram is valid for VS voltage levels above the **VS reset threshold** (see DS-278 and DS-279). The device starts in sleep mode after power up.

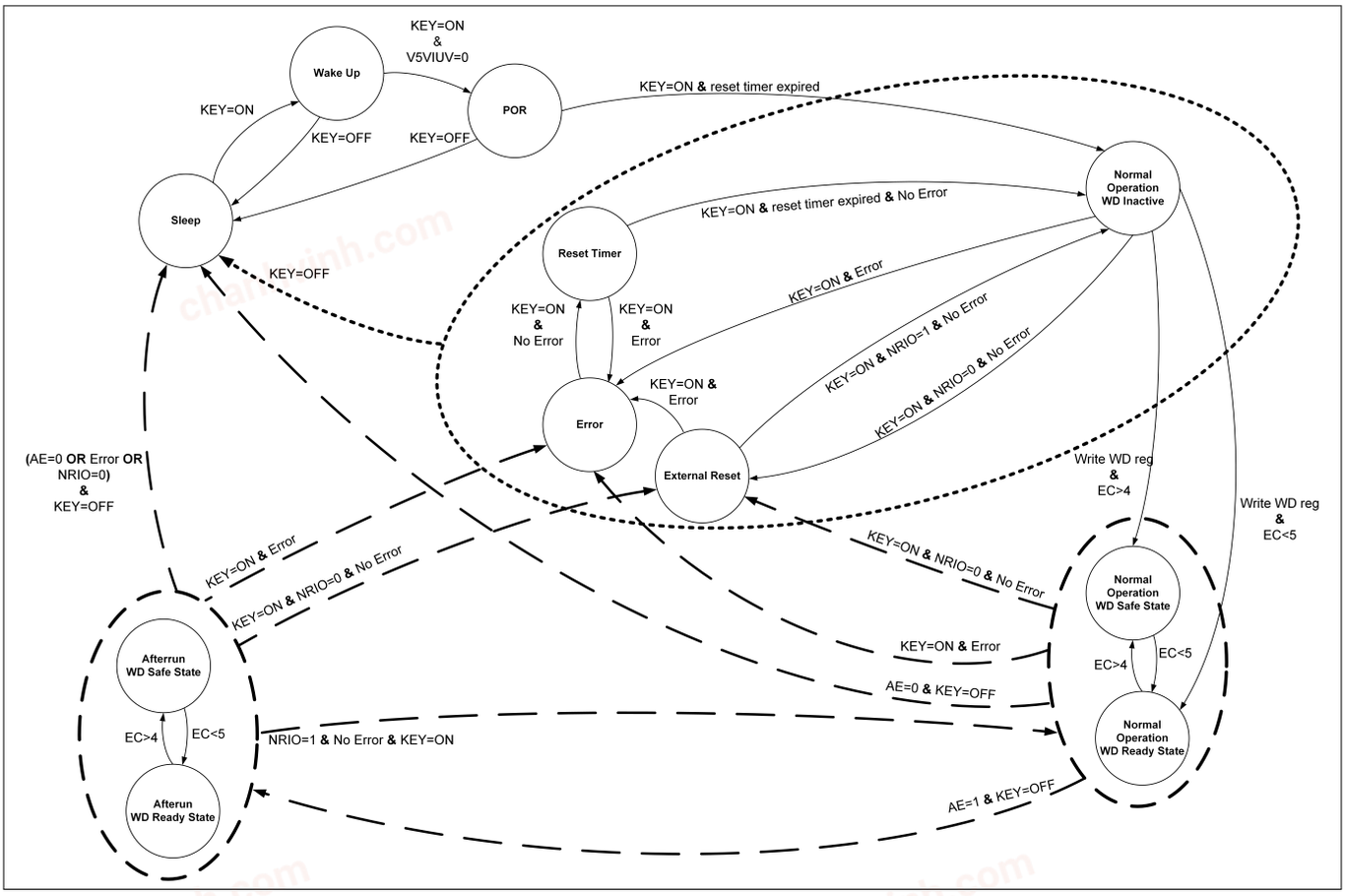


Figure 3 Operation state diagram

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Table 6 State diagram terms and descriptions

Term	Description
KEY	Key on detection, see ***Chapter 4.3*** ON: high voltage level at pin KEY OFF: low voltage level at pin KEY
V5VIUV	5 V undervoltage detection at pin V5VI Diag0.V5VIUV = 0: voltage in operational range Diag0.V5VIUV = 1: undervoltage at pin V5VI
AE	Afterrun setting Config.AE = 0: afterrun disabled Config.AE = 1: afterrun enabled
NRIO	logic status of NRIO pin NRIO = 0: logic low level NRIO = 1: logic high level
Write WD register	SPI write access to watchdog register
Watchdog reset	see ***Chapter 4.2.4***
Error	watchdog reset OR Diag0.V5VIUV = 1 (boolean OR)
No error	no watchdog reset AND Diag0.V5VIUV = 0 (boolean AND)

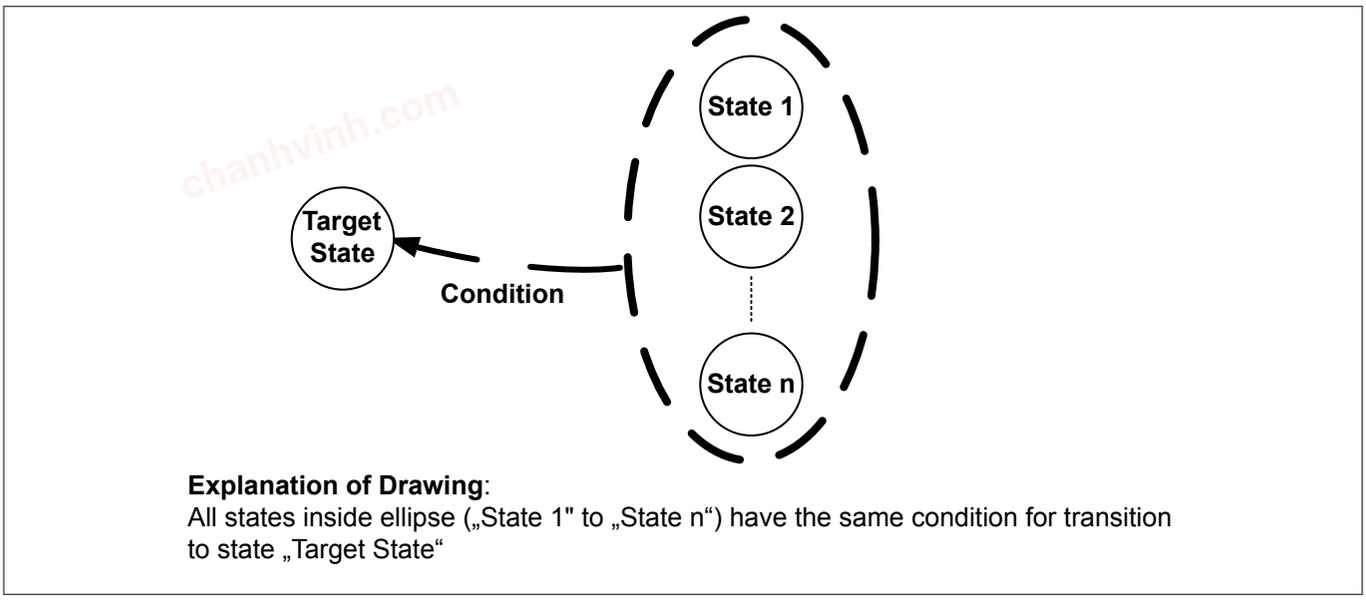


Figure 4 Detailed states movement

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4.1.2 Sleep state

In the Sleep state, the TLE8082ES is inactive. The current consumption in Sleep state at pin VS is **VS sleep current**.

Table 7 Sleep state

Function	Status	Note
Pre-regulator; 5 V Sensor supply, 5 V Communication supply	disabled	no internal supply available
Power stages	disabled	
SPI	no communication	
Register	reset	
Watchdog	reset	
Key input pin KEY	low	driven from outside
Reset output pin NRIO	not defined	no internal supply available

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4.1.3 Wake-up state

In the Wake-up state, all function of the TLE8082ES are ramping up.

Table 8 Wake-up state

Function	Status	Note
Pre-regulator, 5 V Sensor supply, 5 V Communication supply	ramp up	Sensor and communication supply referring to voltage at pin V5VI
Power stages	disabled	
SPI	no communication	
Register	reset	
Key input pin KEY	high	driven from outside
Reset output pin NRIO	active low	after V5VI supply ramp up; pull down transistor driven by V5VI supply

4.1.4 Power on reset (POR) state

In the POR state, the pin NRIO is kept low for the **Power On reset time**.

Table 9 POR state

Function	Status	Note
Pre-regulator, 5 V Sensor supply, 5 V Communication supply	ramped up	output voltage according to Electrical characteristics external supplies (see ***Table 19***)
Power stages	disabled	
SPI	no communication	
Register	reset	
Watchdog	reset	
Key input pin KEY	high	driven from outside
Reset output pin NRIO	active low	pull down transistor driven by V5VI supply

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4.1.5 Normal operation watchdog (WD) inactive state

In the Normal operation WD inactive state, all functions are working according to their definitions.

Table 10 Normal Operation WD inactive state

Function	Status	Note
Pre-regulator, 5 V Sensor supply, 5 V Communication supply	output voltage according to Electrical characteristics external supplies (see ***Table 19***)	
Power stages	disabled	
SPI	communication enabled	
Register	normal access	
Watchdog	waiting for watchdog command	
Key input pin KEY	high	driven from outside
Reset output pin NRIO	high	

4.1.6 Normal operation watchdog (WD) safe state

In the Normal operation WD safe state, all functions are working according to their definitions.

Table 11 Normal operation WD safe state

Function	Status	Note
Pre-regulator, 5 V Sensor supply, 5 V Communication supply	output voltage according to Electrical characteristics external supplies (see ***Table 19***)	
Power stages	disabled	
SPI	communication enabled	
Register	normal access	
Watchdog	watchdog period running, EC>4	
Key input pin KEY	high	driven from outside
Reset output pin NRIO	high	

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4.1.7 Normal operation watchdog (WD) ready state

In the Normal operation WD ready state, all functions are working according to their definitions.

Table 12 Normal operation WD ready state

Function	Status	Note
Pre-regulator, 5 V Sensor supply, 5 V Communication supply	output voltage according to Electrical characteristics external supplies (see ***Table 19***)	
Power stages	controlled by microcontroller	
SPI	communication enabled	
Register	normal access	
Watchdog	watchdog period running, EC<5	
Key input pin KEY	high	driven from outside
Reset output pin NRIO	high	

4.1.8 Afterrun watchdog (WD) ready state

In the Afterrun WD ready state state, all functions are working according to their definitions. The only difference to the Normal operation states is that ramp down is controlled by the microcontroller via SPI communication. The bit AE is set to "1".

Table 13 Afterrun WD ready state

Function	Status	Note
Pre-regulator, 5 V Sensor supply, 5 V Communication supply	output voltage according to Electrical characteristics external supplies (see ***Table 19***)	
Power stages	controlled by microcontroller	
SPI	communication enabled	
Register	normal access	
Watchdog	watchdog period running, EC<5	
Key input pin KEY	low	driven from outside
Reset output pin NRIO	high	

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4.1.9 Afterrun watchdog (WD) safe state

In the Afterrun WD safe state, all functions are working according to their definitions. The only difference to the Normal operation states is that ramp down is controlled by the microcontroller via SPI communication. The bit AE is set to "1".

Table 14 Afterrun WD safe state

Function	Status	Note
Pre-regulator, 5 V Sensor supply, 5 V Communication supply	output voltage according to Electrical characteristics external supplies (see ***Table 19***)	
Power stages	disabled	
SPI	communication enabled	
Register	normal access	
Watchdog	watchdog period running, EC>4	
Key input pin KEY	low	driven from outside
Reset output pin NRIO	high	

4.1.10 External reset state

If an external device requests a reset at the pin NRIO, the external reset state is entered.

Table 15 External reset state

Function	Status	Note
Pre-regulator, 5 V Sensor supply, 5 V Communication supply	output voltage according to Electrical characteristics external supplies (see ***Table 19***)	
Power stages	disabled	
SPI	communication disabled	
Register	Diag 0 register bits V5VIUV, V5VIOV, WDRES, NRIORES according to the status of the device, remaining reset	
Watchdog	WD inactive state	
Key input pin KEY	high	driven from outside
Reset output pin NRIO	low	pull down transistor driven by V5VI supply

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4.1.11 Error state

If an error of the system is detected, the error state is entered.

Table 16 Error state

Function	Status	Note
Pre-regulator, 5 V Sensor supply, 5 V Communication supply	output voltage according to Electrical characteristics external supplies (see ***Table 19***)	
Power stages	disabled	
SPI	communication disabled	
Register	Diag 0 register bits V5VIUV, V5VIOV, WDRES, NRIORES acc. status of the device, remaining reset	
Watchdog	WD inactive state	
Key input pin KEY	high	driven from outside
Reset output pin NRIO	active low	pull down transistor driven by V5VI supply

4.1.12 Reset timer state

After all errors have been disappeared, the reset timer state is entered.

Table 17 Reset timer state

Function	Status	Note
Pre-regulator, 5 V Sensor supply, 5 V Communication supply	output voltage according to Electrical characteristics external supplies (see ***Table 19***)	
Power stages	disabled	
SPI	communication disabled	
Register	Diag 0 register bits V5VIUV, V5VIOV, WDRES, NRIORES acc. status of the device, remaining reset	
Watchdog	WD inactive state	
Key input pin KEY	high	driven from outside
Reset output pin NRIO	active low	pull down transistor driven by V5VI supply

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4.2 Reset

The TLE8082ES implements following resets:

- Power on reset
- Operation reset:
  - external reset (NRIO)
  - V5VI undervoltage reset
  - watchdog reset

4.2.1 Power On reset

After an internal and external V5VI supply ramp up, a power on reset (POR) is performed. The pin NRIO is kept low for **Power On reset time**.

The status of the device after a POR is described in ***Chapter 4.1.4***.

4.2.2 External reset (NRIO)

The pin NRIO is an input/output pin. The output consists of an open drain pull down transistor. The pull down transistor is supplied by the pin V5VI.

An external reset (NRIO externally pulled to low) can only be detected if the pin is internally not pulled low e.g. in error state (see Operation states).

An input filter for the low level detection at the pin NRIO is implemented to suppress disturbances. The filter time is **NRIO input filter time.** If an external reset is detected, the bit NRIORES in register DIAG0 is set. The bit is cleared after an SPI readout.

4.2.3 V5VI undervoltage reset

If an undervoltage according to V5VI Undervoltage monitoring (see ***Chapter 5.2***) is detected, the pin NRIO is switched to low. After recovery, the pin NRIO is kept low for **Operation reset time**.

The device status is changed according to the definition in Operation states (see ***Chapter 4.1***).

4.2.4 Watchdog reset function

The watchdog reset is generated by the watchdog (see ***Chapter 6***) and bit WDRES in register DIAG0 is set. After readout of DIAG0 the bit WDRES is reset. The pin NRIO is kept low for **Operation reset time**.

The status of the device is changed according to the Operation states (see ***Chapter 4.1***).

4.3 Key detection

The TLE8082ES implements a voltage detection function at the pin KEY.

An "ON" is detected with a voltage at pin KEY higher than **Key On detection threshold** for a time longer than **Key detection filter time**. The TLE8082ES starts working according to the description in Operation states (see ***Chapter 4.1***).

An "OFF" is detected with a voltage at pin KEY lower than **Key On detection threshold** for a time longer than **Key detection filter time**. The TLE8082ES reacts according to the Operation states (see ***Chapter 4.1***).

For noise suppression, a **Key On detection hysteresis** is implemented. The key on detection status is indicated by the bit KEY in register DIAG0.

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4.4 Electrical characteristics operation behavior

Table 18 Electrical characteristics operation behavior

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Key On detection threshold - rising	$V_{KEY,th,rise}$	3.5	–	4.5	V		DS-276
Key On detection threshold - falling	$V_{KEY,th,fall}$	2.5	–	4.5	V		DS-277
Key On detection hysteresis	$V_{KEY,hys}$	0.35	–	1.5	V		DS-110
Key input current	I_{KEY}	–	–	200	µA	V_{KEY} = 4.5 V	DS-111
Key detection filter time	$t_{KEY,f}$	100	–	500	µs		DS-112
VS sleep current	$I_{VS,sleep}$	–	–	0.5	µA	V_{VS} = 14 V, T_j = 25°C, sleep state	DS-113
VS operation current	$I_{VS,op}$	–	–	16	mA	V_{VS} = 14 V	DS-292
Power On reset time	$t_{res,POR}$	10	–	15	ms		DS-114
Operation reset time	$t_{res,op}$	1	–	2	ms		DS-115
NRIO input filter time	$t_{fil,NRIO}$	8	–	16	µs		DS-116
VS reset threshold - rising	$V_{VS,res,rise}$	2	–	4	V		DS-278
VS reset threshold - falling	$V_{VS,res,fall}$	2	-	3.5	V		DS-279

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5 Power supply and voltage monitoring function

5.1 Supply functions

The TLE8082ES implements:

- one internal charge pump
- one pre-regulator controlling an external n-channel MOSFET
- one 5 V sensor supply with reverse supply protection
- one 5 V communication supply

5.1.1 V5VI supply input

The V5VI supply input is used as reference voltage for the 5 V sensor and 5 V communication supply. Additionally, it supplies the SPI output buffer and power stage gate drivers.

The 5 V main supply of the electronic control unit (ECU) has to be connected to the pin V5VI.

5.1.2 Charge pump

An internal charge pump is implemented for low drop operation. An external capacitor at CP pin must be connected to AGND.

5.1.3 6.5V Pre-regulator with external MOSFET

The pre-regulator regulates the voltage at pin V6VI to **Pre-regulator output voltage** via the gate voltage of an external n-channel MOSFET. In normal operation, the maximum output level of pin VG is defined by **Pre-regulator voltage drop VS to VG - normal operation** and **Pre-regulator delta voltage VG to VS - low battery**.

The drain of the external MOSFET and the pin VS are connected to the same supply node, normally battery supply.

The function of the pre-regulator is verified with Infineon MOSFET IPD30N06S2L-23.

For stable operation and ripple reduction capacitors are recommended at pin V6VI, pin VG, and pin CP.

5.1.4 5 V Sensor supply

The output T5V of the 5 V sensor supply follows the voltage level at pin V5VI. The sensor supply is supplied out of pin V6VI.

The output is protected against overload (e.g short to GND) and overtemperature. In case of an overcurrent, the output current is limited and the diagnosis bit is set. The diagnosis bit is cleared with a readout of register DIAG0 if no overcurrent is present anymore.

The output is protected against reverse supply to pin V6VI.

The 5 V sensor supply is designed for low battery operation (see **Sensor supply low drop resistance**).

The 5 V sensor supply can be deactivated through SPI configuration of bit COM5VEN in the CONFIG register.

A capacitor at the pin T5V is recommended for stable operation and ripple reduction.

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5.1.5 5 V Communication supply

The output COM5V of the 5 V communication supply follows the voltage level at pin V5VI. The communication supply is supplied out of pin V6VI.

The output is protected against overload (e.g short to GND) and overtemperature. In case of an overcurrent, the output current is limited and the diagnosis bit is set. The diagnosis bit is cleared with a readout of register DIAG0 if no overcurrent is present anymore.

The 5 V communication supply is designed for low battery operation (see **Communication supply low drop resistance**).

The 5 V communication supply can be deactivated through SPI configuration of bit T5VEN in the CONFIG register.

A capacitor, at the pin COM5V is recommended for stable operation and ripple reduction.

5.2 Voltage monitoring

The TLE8082ES implements an undervoltage detection and overvoltage detection at pins V5VI, T5V and COM5V. All undervoltage and overvoltage diagnosis bits are located in the register DIAG0.

The V5VI undervoltage detection monitors the pin V5VI. Two thresholds are implemented, one for rising voltages and one for falling voltages. For falling voltages the diagnosis bit is set if the voltage level is below the **V5VI Undervoltage detection threshold 2**. If the voltage level is above **V5VI Undervoltage detection threshold 1**, the diagnosis bit is reset after an SPI read out. An **Undervoltage detection filter time** is implemented. In case of an undervoltage, the V5VI undervoltage reset is triggered (see ***Chapter 4.2***).

The V5VI overvoltage detection monitors the pin V5VI. For voltage levels above **V5VI Overvoltage detection threshold**, the diagnosis bit is set. If the voltage level is below the threshold, the diagnosis bit is reset after an SPI read out. An **Overvoltage detection hysteresis** and an **Overvoltage detection filter time** are implemented.

The T5V undervoltage detection monitors the pin T5V. For voltage levels below the **T5V Undervoltage detection threshold**, the diagnosis bit is set. If the voltage level is above the threshold, the diagnosis bit is reset after an SPI read out. An **Undervoltage detection hysteresis** and an **Undervoltage detection filter time** are implemented.

The T5V overvoltage detection monitors the pin T5V. For voltage levels above the **T5V Overvoltage detection threshold**, the diagnosis bit is set. If the voltage level is below the threshold, the diagnosis bit is reset after an SPI read out. An **Overvoltage detection hysteresis** and an **Overvoltage detection filter time** are implemented.

The COM5V undervoltage detection monitors the pin COM5V. For voltage levels below the **COM5V Undervoltage detection threshold** the diagnosis bit is set. If the voltage level is above the threshold, the diagnosis bit is reset after an SPI read out. An **Undervoltage detection hysteresis** and an **Undervoltage detection filter time** are implemented.

The COM5V overvoltage detection monitors the pin COM5V. For voltage levels above the **COM5V Overvoltage detection threshold** the diagnosis bit is set. If the voltage level is below the threshold, the diagnosis bit is reset after an SPI read out. An **Overvoltage detection hysteresis** and an **Overvoltage detection filter time** are implemented.

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5.3 Overtemperature protection

5.3.1 T5V Overtemperature monitoring

The T5V overtemperature monitoring protects the sensor supply T5V against high temperatures. For temperatures above the **T5V Overtemperature detection threshold**, the diagnosis bit T5VOT in register DIAG0 is set. If the temperature level is below the threshold, the diagnosis bit is reset after an SPI read out.

An **Overtemperature detection hysteresis** and an **Overtemperature filter time** are implemented.

5.3.2 COM5V Overtemperature monitoring

The COM5V overtemperature monitoring protects the communication supply COM5V against high temperatures. For temperatures above the **COM5V Overtemperature detection threshold**, the diagnosis bit COM5VOT in register DIAG0 is set. If the temperature level is below the threshold, the diagnosis bit is reset after an SPI read out.

An **Overtemperature detection hysteresis** and an **Overtemperature filter time** are implemented.

5.4 Electrical characteristics power supplies

Table 19 Electrical characteristics power supplies

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Pre-regulator output voltage	V_{V6VI}	6	6.5	7	V		DS-155
Pre-regulator voltage drop VS to VG - normal operation	V_{VS-VG}	–	–	2	V	$V_{VS} \geq 12$ V; $V_{V6VI} < 6$ V $V_{VS-VG} = V_{VS} - V_{VG}$ capacitive load at pin VG	DS-281
Pre-regulator delta voltage VG to VS - low battery	ΔV_{VG-VS}	3.5	–	–	V	4.5 V ≤ V_{VS} ≤ 12 V; $V_{V6VI} < 6$ V $\Delta V_{VG-VS} = V_{VG} - V_{VS}$ capacitive load at pin VG	DS-280
Capacitor at pin VG	C_{VG}	–	4.7	–	nF	connect to AGND	DS-158
Capacitor at pin V6VI	C_{V6VI}	–	20	–	µF	$I_{COM5V} \geq 35$ mA; connect to AGND	DS-159
Capacitor at pin CP	C_{CP}	–	4.7	–	nF	connect to AGND; no static load	DS-160
V5VI current consumption	I_{V5VI}	–	–	1.5	mA	no SPI communication, power stages disabled	DS-293

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Table 19 Electrical characteristics power supplies (continued)

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Sensor supply tracking accuracy	$\Delta V_{T5V,acc}$	-10	–	10	mV	$\Delta V_{T5V} = V_{T5V} - V_{V5VI}$ 2.9 V ≤ V_{V5VI} ≤ 5.1 V	DS-161
Sensor supply operation current	$I_{T5V,op}$	–	–	150	mA		DS-162
Sensor supply current limitation	$I_{T5V,lim}$	150	–	–	mA		DS-163
Sensor supply sleep current	$I_{T5V,sleep}$	–	–	0.5	µA	V_{T5V} = 0 V	DS-291
Sensor supply low drop resistance	$R_{T5V,low}$	–	–	3.3	Ω	$V_{V6VI} = V_{VS} = V_{V5VI}$ = 4.5 V	DS-164
Capacitor at pin T5V	C_{T5V}	–	10	–	nF	connect to AGND	DS-165
Communication supply tracking accuracy	$\Delta V_{COM5V,acc}$	-35	–	35	mV	$\Delta V_{COM5V} = V_{COM5V} - V_{V5VI}$ 2.9 V ≤ V_{V5VI} ≤ 5.1 V	DS-166
Communication supply operation current	$I_{COM5V,op}$	–	–	200	mA		DS-167
Communication supply current limitation	$I_{COM5V,lim}$	200	–	–	mA		DS-168
Communication supply sleep current	$I_{COM5V,sleep}$	–	–	0.5	µA	V_{COM5V} = 0 V	DS-294
Communication supply low drop resistance	$R_{COM5V,low}$	–	–	2	Ω	$V_{V6VI} = V_{VS} = V_{V5VI}$ = 4.5 V	DS-169

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Table 19 Electrical characteristics power supplies (continued)

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Capacitor at pin COM5V	C_{COM5V}	–	10	–	µF	I_{COM5V} ≥ 7 mA; connect to AGND	DS-170
V5VI Undervoltage detection threshold 1	$V_{V5VI,UV,th1}$	4.1	–	4.8	V		DS-171
V5VI Undervoltage detection threshold 2	$V_{V5VI,UV,th2}$	2.8	–	3.2	V		DS-172
T5V Undervoltage detection threshold	$V_{T5V,UV,th}$	4.25	–	4.85	V		DS-173
COM5V Undervoltage detection threshold	$V_{COM5V,UV,th}$	4.25	–	4.85	V		DS-174
V5VI Overvoltage detection threshold	$V_{V5VI,OV,th}$	5.1	–	5.85	V		DS-175
T5V Overvoltage detection threshold	$V_{T5V,OV,th}$	5.1	–	5.8	V		DS-176
COM5V Overvoltage detection threshold	$V_{COM5V,OV,th}$	5.1	–	5.8	V		DS-177
Undervoltage detection hysteresis	$V_{UV,hys}$	10	–	100	mV		DS-178
Overvoltage detection hysteresis	$V_{OV,hys}$	10	–	130	mV		DS-179
Undervoltage detection filter time	$t_{UV,fil}$	5	–	15	µs		DS-180

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Table 19 Electrical characteristics power supplies (continued)

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overvoltage detection filter time	$t_{OV,fil}$	5	–	15	µs		DS-181
T5V Overtemperature detection threshold	$T_{T5V,ot}$	150	–	200	°C		DS-182
COM5V Overtemperature detection threshold	$T_{COM5V,ot}$	150	–	200	°C		DS-183
Overtemperature detection hysteresis	T_{hys}	–	20	–	°C		DS-184
Overtemperature filter time	t_{ot}	10	–	20	µs		DS-185

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6 Watchdog

The device implementes a window watchdog with a closed and an open time window serviced by a watchdog command via SPI.

The watchdog consists of:

- a watchdog state machine and
- an error counter

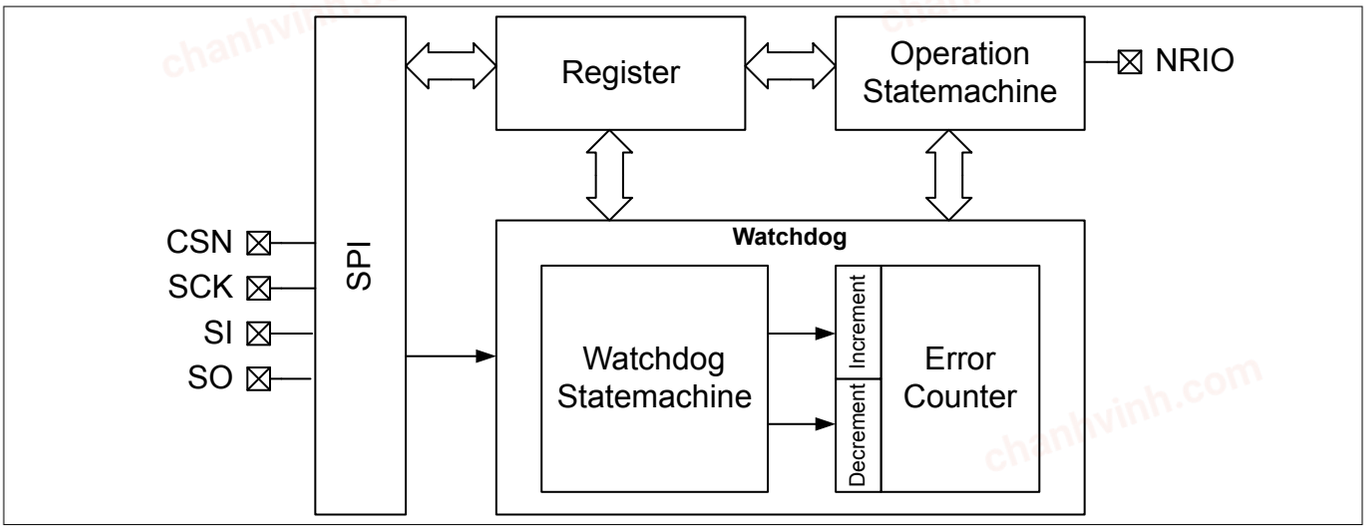


Figure 5 Watchdog function diagram

6.1 Watchdog period

The watchdog period $t_{WD,per}$ consists of a closed window t_{cw} and an open window t_{ow}.

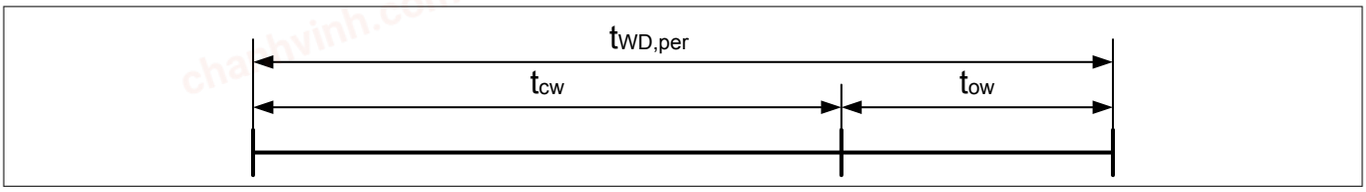


Figure 6 Watchdog period

The watchdog period time $t_{WD,per}$ can be configured to 4 different values by setting the bit WDP in the WD register. The open window can be configured to a short and a long value for each watchdog period value with the bit WDOW in the WD register. The configuration of the watchdog period can be changed together with the watchdog command.

Table 20 Watchdog period configuration (all values are typical values)

Watchdog period $t_{WD,per}$	Open window setting	Open window time t_{ow}	Closed window time t_{cw}
$t_{WD,per1}$ = 32 ms	short	$t_{ow1,s}$ = 4 ms	28 ms
$t_{WD,per1}$ = 32 ms	long	$t_{ow1,l}$ = 8 ms	24 ms
$t_{WD,per2}$ = 48 ms	short	$t_{ow2,s}$ = 8 ms	40 ms
$t_{WD,per2}$ = 48 ms	long	$t_{ow2,l}$ = 12 ms	36 ms

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Table 20 Watchdog period configuration (all values are typical values) (continued)

Watchdog period $t_{WD,per}$	Open window setting	Open window time t_{ow}	Closed window time t_{cw}
$t_{WD,per3}$ = 64 ms	short	$t_{ow3,s}$ = 8 ms	56 ms
$t_{WD,per3}$ = 64 ms	long	$t_{ow3,l}$ = 16 ms	48 ms
$t_{WD,per4}$ = 128 ms	short	$t_{ow4,s}$ = 16 ms	112 ms
$t_{WD,per4}$ = 128 ms	long	$t_{ow4,l}$ = 30 ms	98 ms

6.2 Trigger of the watchdog - watchdog (WD) command

The watchdog trigger event is a rising edge at the pin CSN of an SPI communication frame with write access to register WD. The trigger event is called watchdog command.

Note: All other SPI communications are not triggering the watchdog.

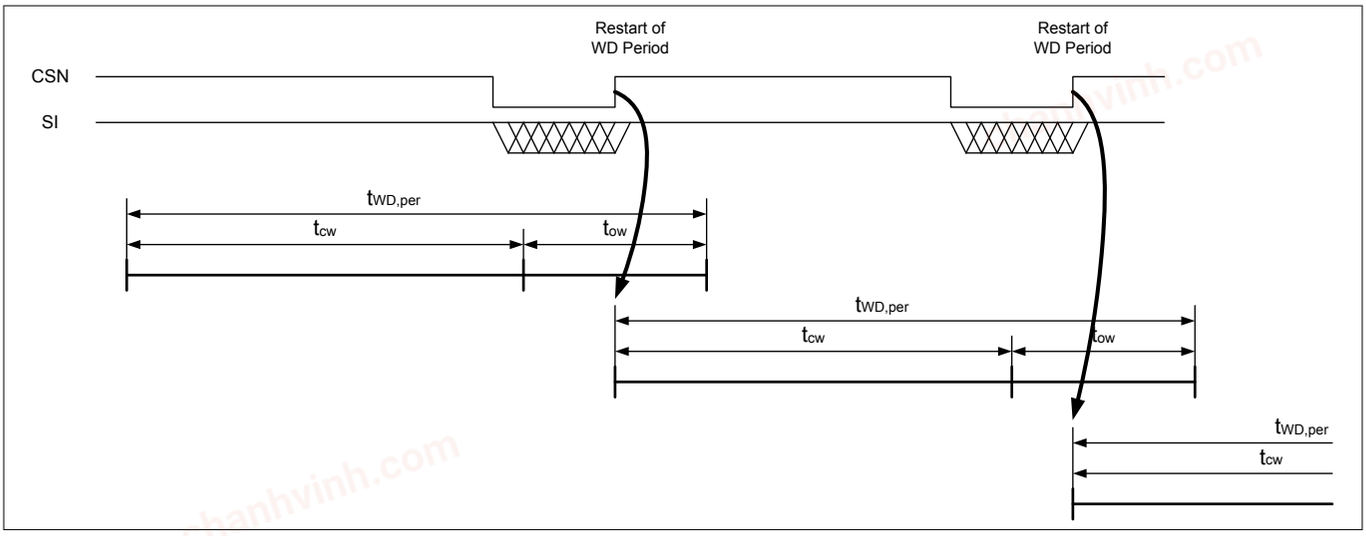


Figure 7 Watchdog trigger

6.3 Watchdog operation and error definition

The watchdog provides two functions to check the microcontroller:

1. timing check and
2. controlling of the functional check inside the microcontroller

A correct trigger of the watchdog is confirmed if the timing check and the control of the functional check inside the microcontroller are passed. This leads to a decrement of the error counter. All other situations are considered as watchdog errors and lead to an increment of the error counter. The watchdog status is indicated by the bits EC, WDTO, WDCE and WDERR in the register WD.

Timing check:

The watchdog expects a watchdog command via SPI inside the open window. If the timing of the microcontroller is too fast, the watchdog detects a watchdog command inside the closed window. In this case, the watchdog command too early bit WDCE in register WD is set to 1. If the microcontroller timing is too slow, the watchdog period is expired and the watchdog time out bit WDTO in register WD is set to 1.

Controlling of the internal functional check of the microcontroller:

The microcontroller transmits the status of the internal functional check by setting the watchdog check command bit WDC in register WD. If the internal functional check of the microcontroller is not ok, the watchdog error bit WDERR in register WD is set to 1.

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6.4 Watchdog state machine

After a reset condition the watchdog state machine is set to the state "WD inactive". The watchdog states are described in ***Table 21***. The transitions of the state machine are described in ***Table 22***.

Definitions:

- WDC: Watchdog check command bits; WDC=10_B check ok
- Timer expired: watchdog period time is expired

The following figure shows the watchdog state machine.

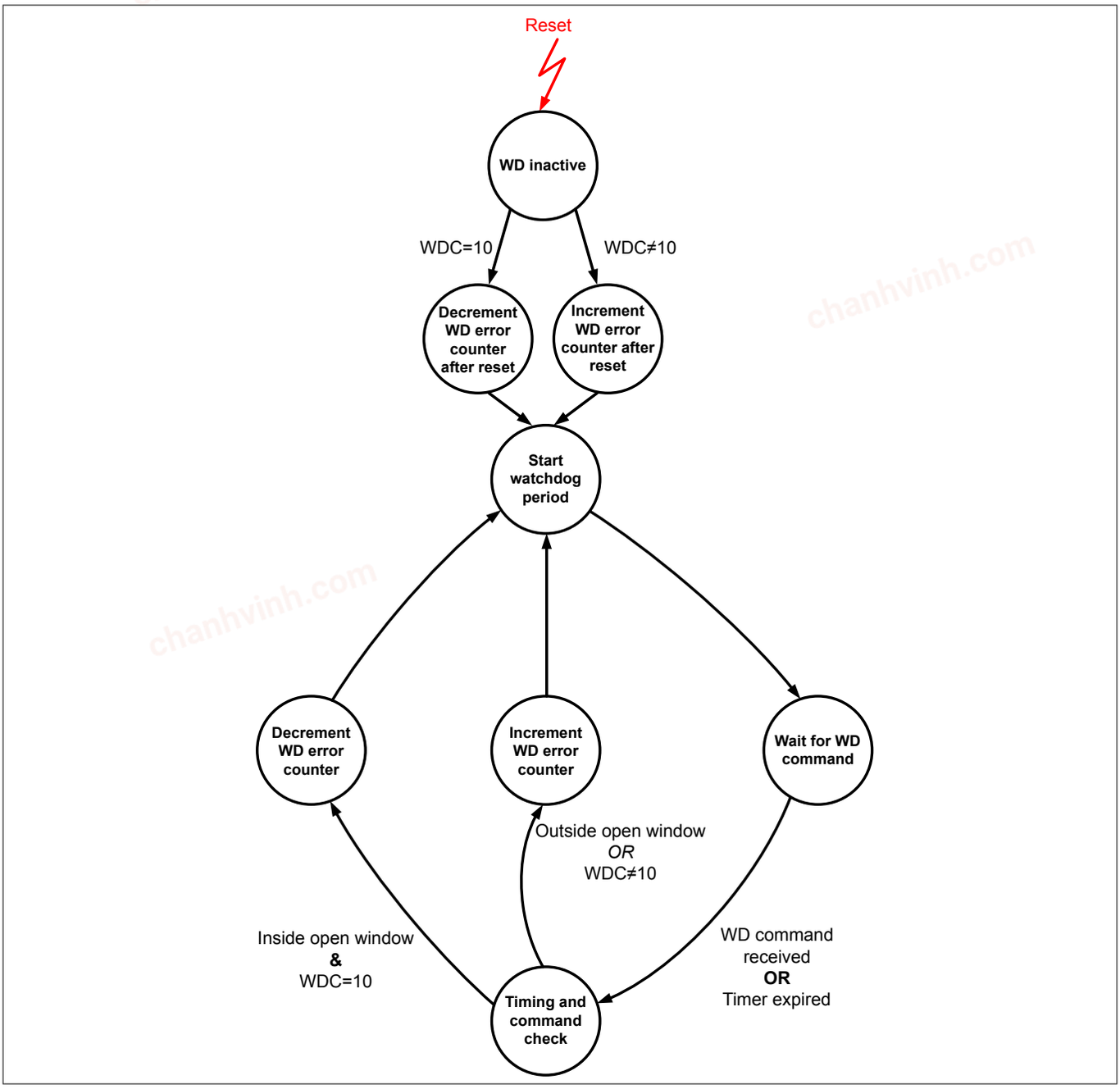


Figure 8 Watchdog state machine

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Watchdog

Table 21 Watchdog state machine

Watchdog state	Description
WD inactive	In the "WD inactive" state the watchdog is waiting for the first WD command after a reset. The configuration of the watchdog was set by the prior occurred reset to the default state after a reset according to the definition in ***Chapter 4.1***.
Decrement WD error counter after reset	In this state the error counter is decremented by 1. This state is active only once after a reset.
Increment WD error counter after reset	In this state the error counter is incremented by 1. This state is active only once after a reset.
Start watchdog period	In this state the watchdog period is started with the closed window and the setup according to the watchdog configuration.
Wait for WD command	In this state, the watchdog period is active until a watchdog command is received (via SPI) or the watchdog period is expired.
Timing and command check	In this state, the timing and the command are checked. The watchdog diagnosis error bits WDTO, WDCE and WDERR are set according to the status of the watchdog period and the watchdog check command bit WDC.
Increment WD error counter	In this state the WD error counter is incremented by 1.
Decrement WD error counter	In this state the WD error counter is decremented by 1.

Table 22 Watchdog state machine transitions

State	Event or condition for transition to target state	Target state	Notes
	Reset acc. Operation states	WD inactive	see ***Chapter 4.1***
WD inactive	WD command: WDC=10	Decrement WD error counter after reset	
WD inactive	WD command: WDC≠10	Increment WD error counter after reset	
Decrement WD error counter after reset	not event triggered	Start watchdog period	no condition or event needed for transition, only decrement must be performed for automatic transition
Increment WD error counter after reset	not event triggered	Start watchdog period	no condition or event needed for transition, only increment must be performed for automatic transition
Start watchdog period	not event triggered	Wait for WD check command	no condition or event needed for transition, only watchdog period started for automatic transition

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Table 22 Watchdog state machine transitions (continued)

State	Event or condition for transition to target state	Target state	Notes
Wait for WD command	WD command received OR watchdog period timer expired	Timing and command check	
Timing and command check	WDC=10_B AND WD command inside open window	Decrement WD error counter	
Timing and command check	WDC≠10_B OR WD command outside open window	Increment WD error counter	
Decrement WD error counter	not event triggered	Start watchdog period	no condition or event needed for transition, only decrement must be performed for automatic transition
Increment WD error counter	not event triggered	Start watchdog period	no condition or event needed for transition, only increment must be performed for automatic transition

6.5 Watchdog error counter

The device implements a 3 bits error counter EC located in the register WD. This corresponds to a counting range from 0_D (000_B) to 7_D (111_B).

The actual counter value can be read via SPI.

The status of the error counter EC defines the state of the device.

- Ready state: EC < 5_D
- Safe state: EC > 4_D

A watchdog reset is generated by an overflow of the error counter EC. For more information about the Reset state of the watchdog, see ***Chapter 4.1.5***.

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6.6 Electrical characteristics watchdog

Table 23 Electrical characteristics watchdog

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Accuracy of watchdog period and window times	a_{wd}	-5	–	+5	%		DS-19
Window watchdog period time 1	$t_{WD,per1}$	–	32	–	ms		DS-20
Window watchdog period time 2	$t_{WD,per2}$	–	48	–	ms		DS-21
Window watchdog period time 3	$t_{WD,per3}$	–	64	–	ms		DS-22
Window watchdog period time 4	$t_{WD,per4}$	–	128	–	ms		DS-23
Window watchdog open window time 1 short	$t_{ow1,s}$	–	4	–	ms		DS-24
Window watchdog open window time 1 long	$t_{ow1,l}$	–	8	–	ms		DS-25
Window watchdog open window time 2 short	$t_{ow2,s}$	–	8	–	ms		DS-26
Window watchdog open window time 2 long	$t_{ow2,l}$	–	12	–	ms		DS-27
Window watchdog open window time 3 short	$t_{ow3,s}$	–	8	–	ms		DS-28

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Table 23 Electrical characteristics watchdog (continued)

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Window watchdog open window time 3 long	$t_{ow3,l}$	–	16	–	ms		DS-29
Window watchdog open window time 4 short	$t_{ow4,s}$	–	16	–	ms		DS-30
Window watchdog open window time 4 long	$t_{ow4,l}$	–	30	–	ms		DS-31

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7 Power stages

7.1 Outputs 1 to 3 - inductive load drivers

The TLE8082ES implements 3 low-side switches. Output 1 to 3 are intended to drive inductive loads like injectors, valves or relays. The outputs contain a clamping circuit for freewheeling of inductive loads.

The control of OUT1 can be configured to direct drive with input pin IN1 or SPI control. OUT2 and OUT3 can be configured to direct drive with input pin IN23 or SPI control. The output configuration can be determined in the configuration register.

If the pin control is selected, a high level at input pins IN1 and IN23 switches on the respective output (see ***Figure 11***).

7.2 Output 4 - O2 heater driver

The low-side switch output 4 is intended to drive resistive loads like O2 heaters. The output contains a clamping circuit for freewheeling of inductive loads, too.

The TLE8082ES provides a current feedback output. The provided sink current at pin CFB4 is proportional to the current of OUT4. If OUT4 is switched off, CFB4 is in high ohmic state. The output current at pin CFB4 can be calculated as follows.

$$I_{CFB4} = g_{CFB4} \cdot I_{OUT4}$$

Equation 1

The control of OUT4 can be configured to direct drive with input pin IN4 or SPI control.

If pin control is selected, a high level at input pin IN4 switches on OUT4 (see ***Figure 11***).

7.3 Protection and diagnosis of low-side output stages

All low-side output stages are protected against overcurrent.

If the current through a power stage is above the **Overcurrent detection threshold** for a time longer than **Overcurrent switch off filter time**, an overcurrent is detected and the affected powerstage is switched off. Additionally, the according overcurrent bit in register Diag1 is set.

The following conditions must be fulfilled to switch on the powerstages after an overcurrent event has occurred:

- no overcurrent condition
- readout of register Diag1 to reset the diagnosis bit
- power stage switch on command (SPI switch-on command or positive edge at pin INx)

All low-side output stages are protected against overtemperature.

If the power stage temperature is above the **OUTx overtemperature detection threshold** for a time longer than **OUTx overtemperature filter time**, an overtemperature is detected and the affected powerstage is switched off. Additionally, the overtemperature bit in register Diag1 is set. An **Overtemperature hysteresis** avoids a premature switch on.

The following conditions must be fulfilled to switch-on the powerstages after an overtemperature event has occurred:

- no overtemperature condition
- readout of register Diag1 to reset the diagnosis bit
- switch-on command (SPI switch on command or positive edge at pin INx)

The OUT3 output switching status (ON/OFF) is detected by **Diagnosis in off threshold high**. The status bit O3Stat in register Diag0 is "1" with an output voltage below the threshold.

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7.3.1 Diagnosis in OFF-state

All low-side output stages provide open load diagnosis in OFF-state.

All low-side output power stages provide a short to GND diagnosis in OFF-state.

A pull-up current source, a pull-down current source and two detection thresholds are implemented for each output OFF-state diagnosis.

A short to GND in OFF-state is detected if the output voltage level is below the **Diagnosis in off threshold low** for a time longer than the specified filter time (**Diagnosis in off filter time OUT1 and OUT2**, **Diagnosis in off filter time OUT3 and OUT4**).

An open load in OFF-state is detected if the output voltage level is between the **Diagnosis in off threshold low** and the **Diagnosis in off threshold high** for a time longer than specified filter time (**Diagnosis in off filter time OUT1 and OUT2**, **Diagnosis in off filter time OUT3 and OUT4**).

In case of an OFF-state diagnosis detection condition, the respective diagnosis bit in register Diag1 is set. The diagnosis bits are reset after a readout of register Diag1 if no fault condition is present.

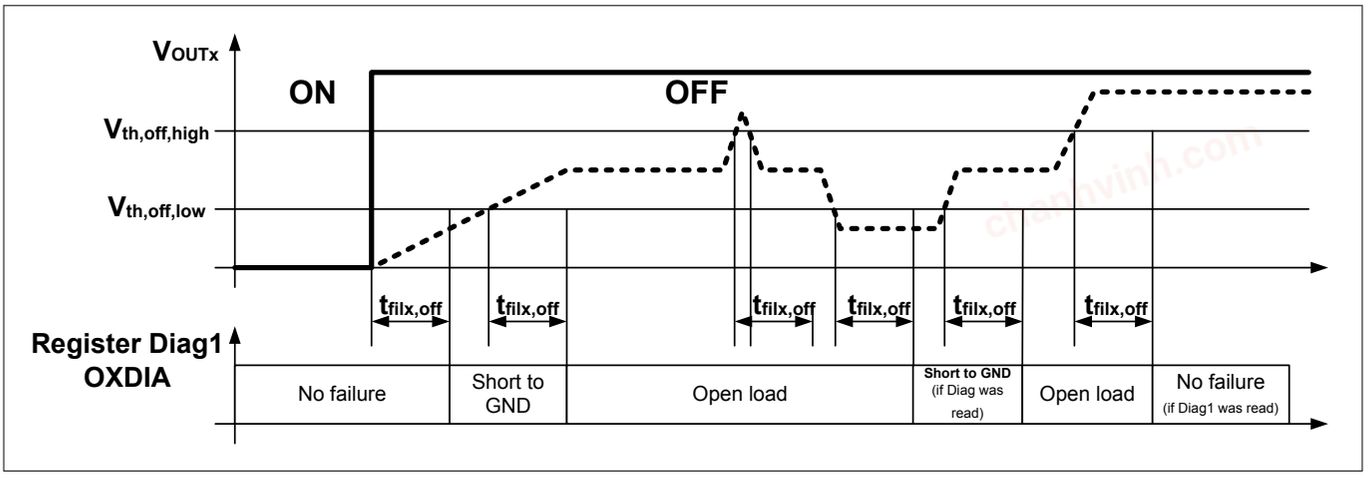


Figure 9 Short circuit to GND and open load diagnostic function timings (overview only)

The pull current sources are implemented to define the output voltage level in case of an open load in between the two thresholds.

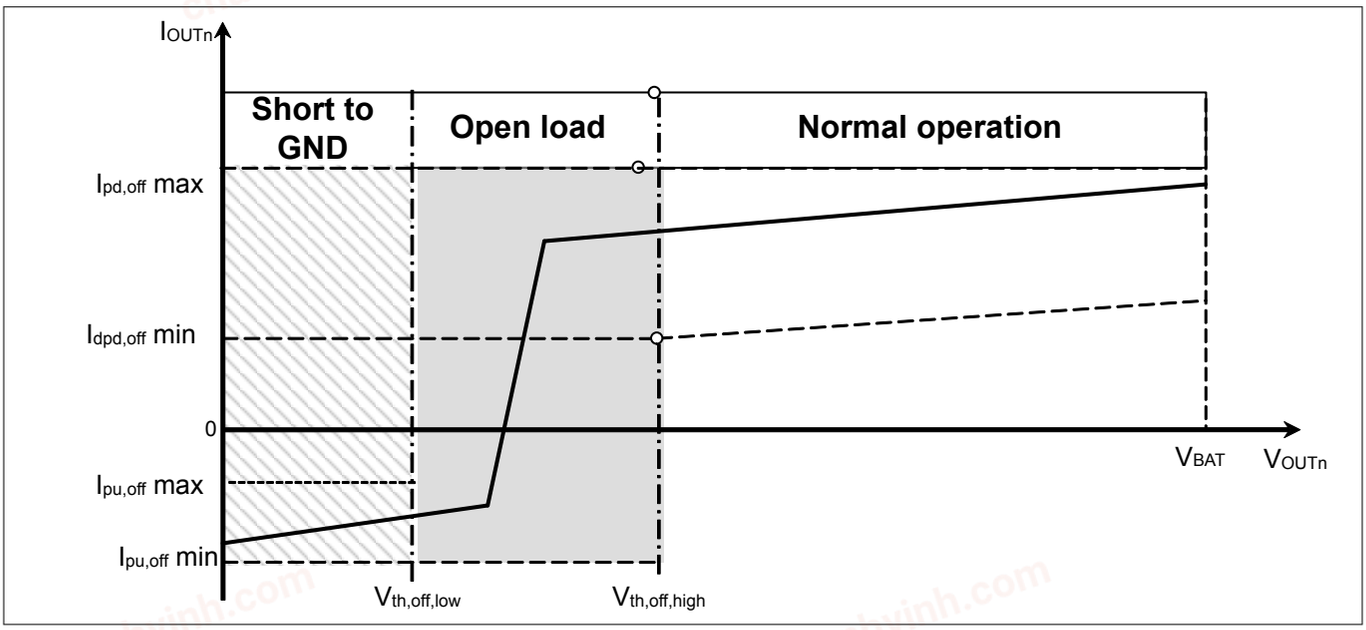


Figure 10 Diagnosis current behavior over output voltage

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7.3.2 Priority of diagnosis bit setting

The diagnosis bits OxDIA in register DIAG1 are set according to the diagnosis information .

In OFF-state, open load and short to GND diagnosis information are available. In ON-State, overcurrent protection and short to battery diagnosis information are available.

To avoid conflicts, the setting of the diagnosis bits is performed according to the priorites below:

1. short to battery (highest priority)
2. open load
3. short to GND (lowest priority)

In case of a parallel diagnostic condition, the bit with higher priority is set. The information on the occurrence of a diagnosis condition with lower priority is lost.

The diagnosis bits are set to the actual diagnosis status of the device by a read command via SPI.

7.4 Electrical characteristics power stages

Table 24 Electrical characteristics power stages

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Operation current OUT1 and OUT2	$I_{OUT1,2,op}$	–	–	2.6	A		DS-202
Operation current OUT3	$I_{OUT3,op}$	–	–	3.3	A		DS-289
Operation current OUT4	$I_{OUT4,op}$	–	–	4.5	A		DS-203
On resistance OUT1 and OUT2	$R_{OUT1,2,on}$	–	–	0.7	Ω		DS-204
On resistance OUT3	$R_{OUT3,on}$	–	–	410	mΩ		DS-283
On resistance OUT4	$R_{OUT4,on}$	–	–	350	mΩ		DS-205
Output clamping voltage OUT1 and 2	V_{cl1}	50	–	60	V	I_{OUTx} = 20 mA	DS-206
Output clamping voltage OUT3 and 4	V_{cl2}	35	–	45	V	I_{OUTx} = 20 mA	DS-207
Current measurement range OUT4	$I_{OUT4,meas}$	0.02	–	4.5	A		DS-208

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Table 24 Electrical characteristics power stages (continued)

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current measurement accuracy OUT4 - low range	$a_{CFP4,low}$	-20	–	20	%	20 mA ≤ I_{OUT4} ≤ 100 mA $a_{CFB4} = (I_{CFB4}/g_{CFB4,typ} - I_{OUT4}) / I_{OUT4}$	DS-290
Current measurement accuracy OUT4 - high range	$a_{CFB4,h}$	-7	–	7	%	100 mA < I_{OUT4} ≤ 4.5 A $a_{CFB4} = (I_{CFB4}/g_{CFB4,typ} - I_{OUT4}) / I_{OUT4}$	DS-209
Current measurement gain OUT4	g_{CFB4}	–	0.95	–	mA/A	see **Current measurement accuracy**	DS-210
Current feedback pin delta voltage CFB	ΔV_{CFB}	–	–	100	mV	$V_{CFB} = I_{OUT4} \cdot R_{OUT4} + \Delta V_{CFB}$	DS-295
Switch on time OUT1 and OUT2	t_{on12}	–	–	2.3	µs	I_{OUTx} = 2.6 A resistive load, V_{OUTx} = 14 V, see Switching time definition ***Figure 11***	DS-211
Switch off time OUT1 and OUT2	t_{off12}	–	–	2.5	µs	I_{OUTx} = 2.6 A resistive load, V_{OUTx}=14 V, see Switching time definition ***Figure 11***	DS-212
Switch on time OUT3	t_{on3}	–	–	5.7	µs	I_{OUTx} = 3.3 A resistive load, V_{OUTx} = 14 V, see Switching time definition ***Figure 11***	DS-213
Switch off time OUT3	t_{off3}	–	–	5.7	µs	I_{OUTx} = 3.3 A resistive load, V_{OUTx} = 14 V, see Switching time definition ***Figure 11***	DS-214
Swtich on time OUT4	t_{on4}	–	–	6	µs	I_{OUTx} = 4.5 A resistive load, V_{OUTx} = 14 V, see Switching time definition ***Figure 11***	DS-215
Switch off time OUT4	t_{off4}	–	–	6.2	µs	I_{OUTx} = 4.5 A resistive load, V_{OUTx} = 14 V, see Switching time definition ***Figure 11***	DS-216
Time delay switch on OUT1 to 2	$t_{d,on,12}$	–	–	2.1	µs	I_{OUTx} = 2.6 A resistive load, V_{OUTx} = 14 V, see Switching time definition ***Figure 11***	DS-285
Time delay switch off OUT 1 to 2	$t_{d,off,12}$	–	–	4.8	µs	I_{OUTx} = 2.6 A resistive load, V_{OUTx} = 14 V, see Switching time definition ***Figure 11***	DS-284

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Table 24 Electrical characteristics power stages (continued)

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Time delay switch on OUT 3 to 4	$t_{d,on,34}$	–	–	4.7	µs	I_{OUT3} = 3.3 A resistive load, I_{OUT4} = 4.5 A resistive load, V_{OUTx} = 14 V, see Switching time definition ***Figure 11***	DS-287
Time delay switch off OUT 3 to 4	$t_{d,off,34}$	–	–	12.5	µs	I_{OUT3} = 3.3 A resistive load, I_{OUT4} = 4.5 A resistive load, V_{OUTx} = 14 V, see Switching time definition ***Figure 11***	DS-286
Overcurrent switch off threshold OUT1 to 2	$I_{OUT1,2,oc}$	2.6	–	–	A		DS-217
Overcurrent switch off threshold OUT3	$I_{OUT3,oc}$	3.3	–	–	A		DS-282
Overcurrent switch off threshold OUT4	$I_{OUT4,oc}$	4.5	–	–	A		DS-218
Overcurrent switch off filter time	t_{oc}	0.5	–	3	µs		DS-219
Diagnosis in off threshold high	$V_{th,off,high}$	2.5	–	3.1	V		DS-220
Diagnosis in off threshold low	$V_{th,off,low}$	1.7	–	2.15	V		DS-221
Diagnosis in off pull-down current	$I_{pd,off}$	100	–	250	µA		DS-222
Diagnosis in off pull-up current	$I_{pu,off}$	-750	–	-250	µA		DS-223
Diagnosis in off filter time OUT1 and OUT2	$t_{fil12,off}$	15	–	20	µs		DS-224

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Table 24 Electrical characteristics power stages (continued)

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Diagnosis in off filter time OUT3 and OUT4	$t_{fil34,off}$	20	–	25	µs		DS-225
OUTx overtemperature detection threshold	$T_{OUTx,ot}$	150	–	200	°C		DS-226
OUTx overtemperature detection hysteresis	$T_{OUTx,hys}$	–	20	–	°C		DS-227
OUTx overtemperature filter time	$t_{OUTx,ot}$	10	–	20	µs		DS-228

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7.5 Switching time definition

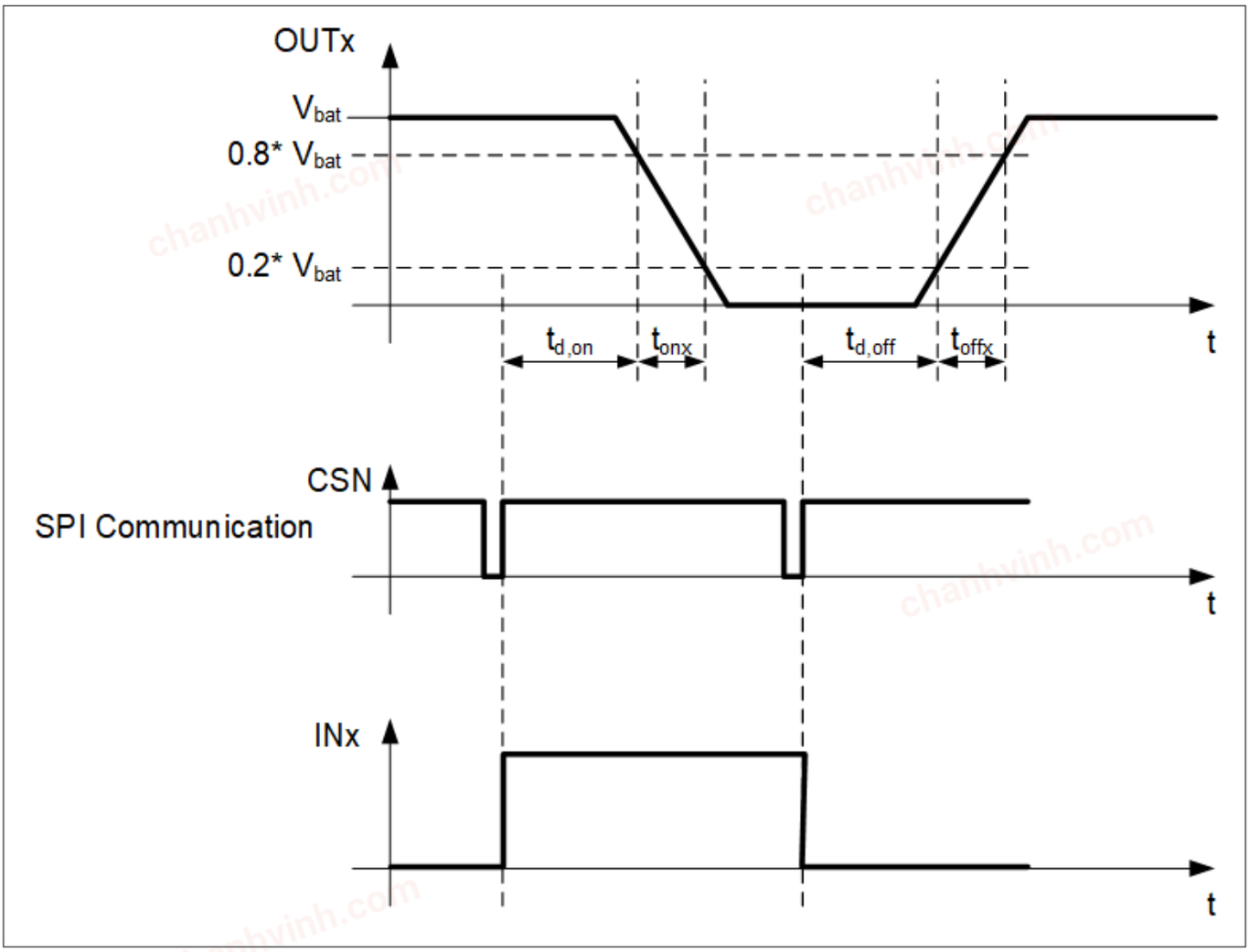


Figure 11 Power stage switching time definition

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8 Inputs and outputs

8.1 Electrical characteristics inputs and outputs

Table 25 Electrical characteristics inputs and outputs

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low level input voltage pins IN1, IN23, IN4, CSN, SI, SCK, NRIO	$V_{in,l}$	–	–	1	V		DS-233
High level input voltage pins IN1, IN23, IN4, CSN SI, SCK, NRIO	$V_{in,h}$	2	–	–	V		DS-234
Input voltage hysteresis pins IN1, IN23, IN4, CSN, SI, SCK, NRIO	$V_{in,hys}$	50	–	500	mV		DS-235
Pull down current pins IN1, IN23, IN4, SI, SCK	I_{pd}	25	–	130	µA	$V_{INx} \geq 1$ V	DS-236
Pull up current pin CSN	I_{pu}	-100	–	-25	µA		DS-237
Low level output voltage pin SO	$V_{out,l}$	–	–	100	mV	I_{out} = 2 mA	DS-238
High level output voltage pin SO	$V_{out,h}$	4.8	–	–	V	I_{out} = -2 mA	DS-239
Low level output current 1 pin NRIO	I_{NRIO1}	1	–	–	mA	V_{NRIO} = 1 V; V_{V5VI} = 2 V	DS-240

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Table 25 Electrical characteristics inputs and outputs (continued)

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low level output current 2 pin NRIO	I_{NRIO2}	5	–	–	mA	V_{NRIO} < 0.5 V, V_{V5VI} ≥ 4.5 V	DS-296

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9 Serial Peripheral Interface (SPI)

The device has a 16 bit Serial Peripheral Interface (SPI). The SPI is a full duplex synchronous serial interface with 3 inputs and 1 output.

CSN: Chip Select Not (low active) input
SCK: SPI Clock input
SI: Slave Input
SO: Slave Output

The data information at SI and SO is synchronous to the SPI clock. The output levels of the SPI pins are related to pin V5VI.

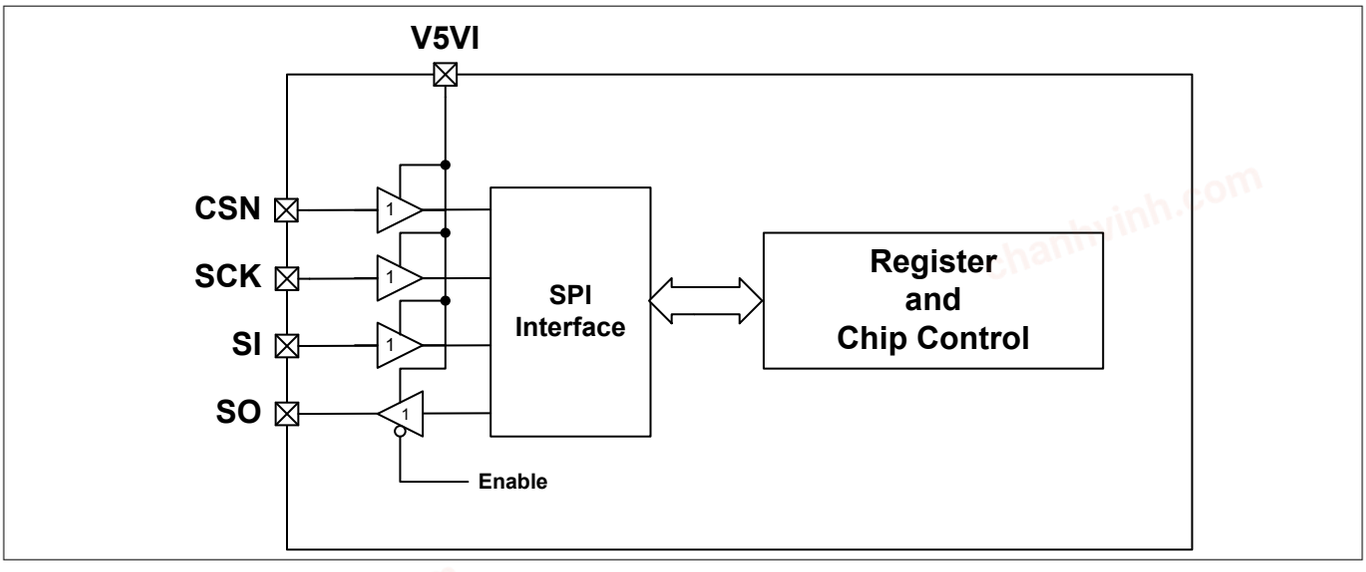


Figure 12 SPI Function diagram

9.1 Parallel SPI operation together with TLE8080ES

The implementation of the SPI and the definition of the registers (two addresses for CTRL register) enable a parallel operation of the SPI communication together with the device TLE8080EM.

9.2 SPI mode definition

A communication frame starts with the falling edge at CSN. At the beginning the clock must be "0" according to timing definition (***Figure 16***). The data at pin SI is sampled with the falling edge of SCK. The data at pin SO is shifted with the rising edge of SCK. The communication frame ends with the rising edge at CSN. At that time the data received via pin SI is executed and stored internally and the result of the request is prepared for the next communication as output data. A correct communication frame consists of 16 bits and starts with the MSB first.

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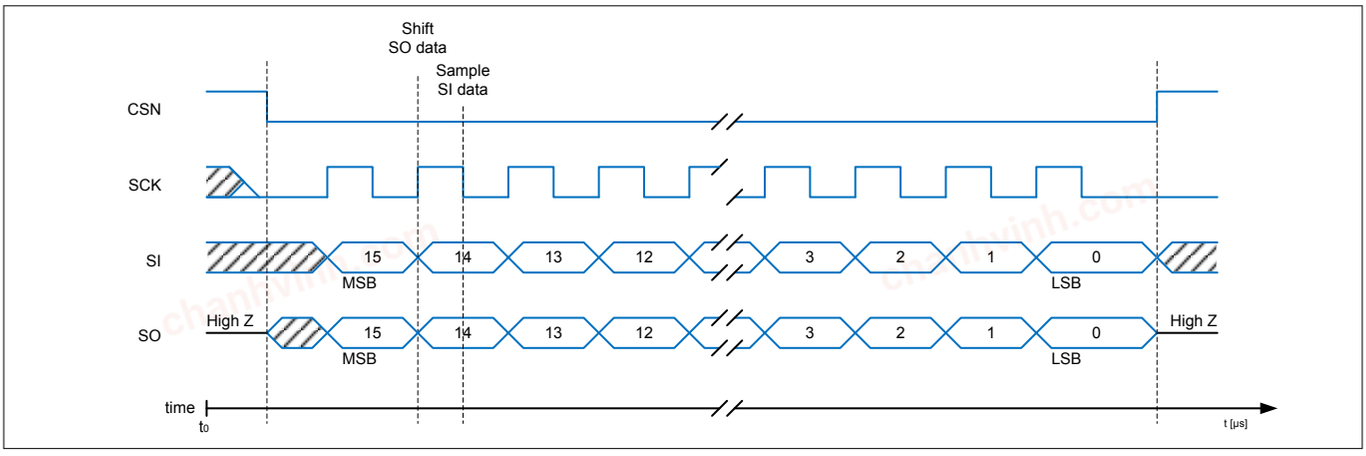


Figure 13 Communication frame

Note: This definition corresponds to AURIX™ microcontrollers to the mode definition clock polarity CPOL="0$_b$" and clock phase CPHA="1$_b$".

9.3 SPI data frame

The data frame consist of 1 read/write bit (RN/W), 3 address bits (A2 to A0) and 12 data bits (D11 to D0) according to the register definition.

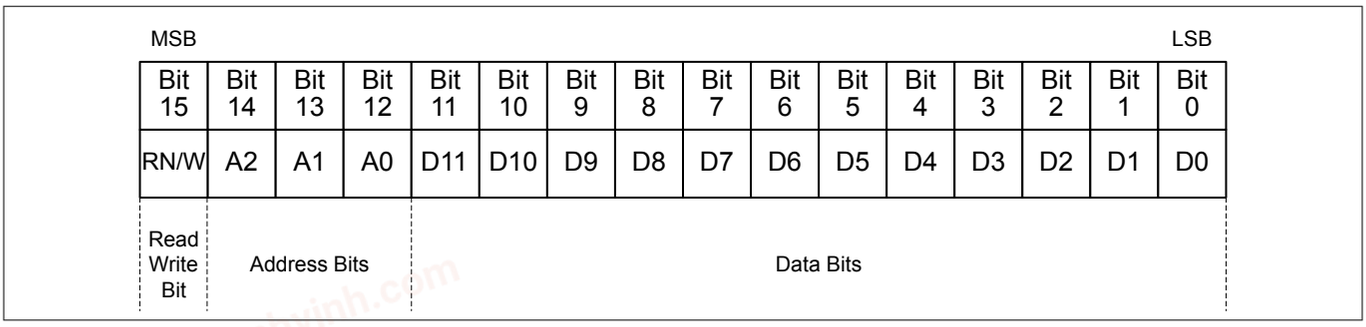


Figure 14 Data frame

A correct communication consists of 16 bits in one communication frame and the value of the address bits must refer to an existing register.

All other communication frames are invalid.

9.4 SPI send and response scheme

The logical frame dependency is defined as out-of-frame communication where the logical response of the slave is within the next frame of the master.

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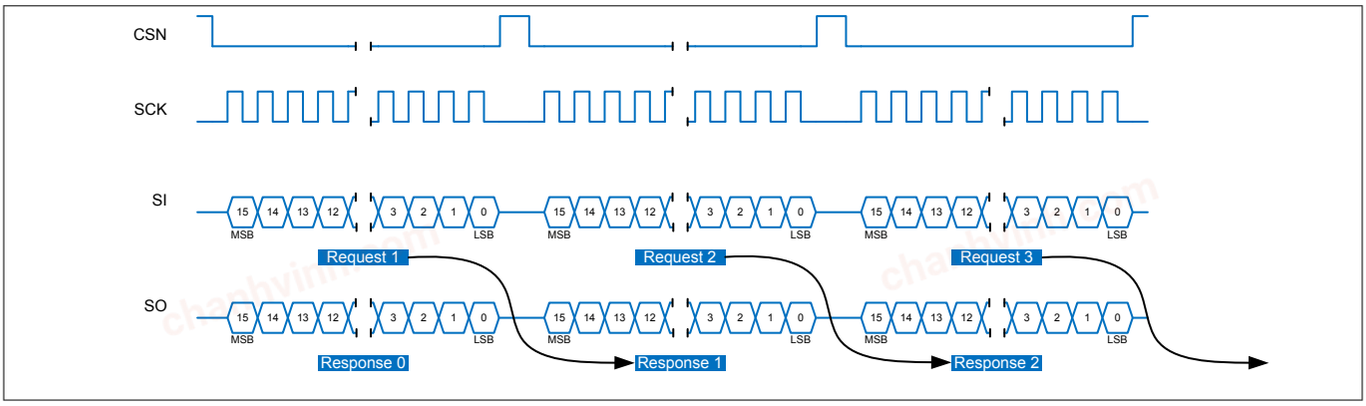


Figure 15 Send and response scheme

Definition of the response:

- during power on reset: no SPI communication enabled - no response
- 1st response after power on reset: content of register Config (*NOTE*: consider power on reset time)
- during operation reset: no SPI communication enabled - no response
- 1st response after operation reset: content of register Diag0 (*NOTE*: consider operation reset time)
- 1st response after NRIO reset: content of register Diag0 (*NOTE*: consider NRIO input filter time, DIAG0.NRIORES set)
- 1st response after watchdog reset: content of register Diag0 (*NOTE*: DIAG0.WDRES is set)
- response after correct communication: content of addressed register
- response after invalid communication: content of register Diag0 (*NOTE*: DIAG0 content is not reliable)

RN/W bit of the response corresponds to the RN/W bit of the request for correct communication. For all other responses the RN/W bit is "0" (read).

9.5 SPI timing diagram

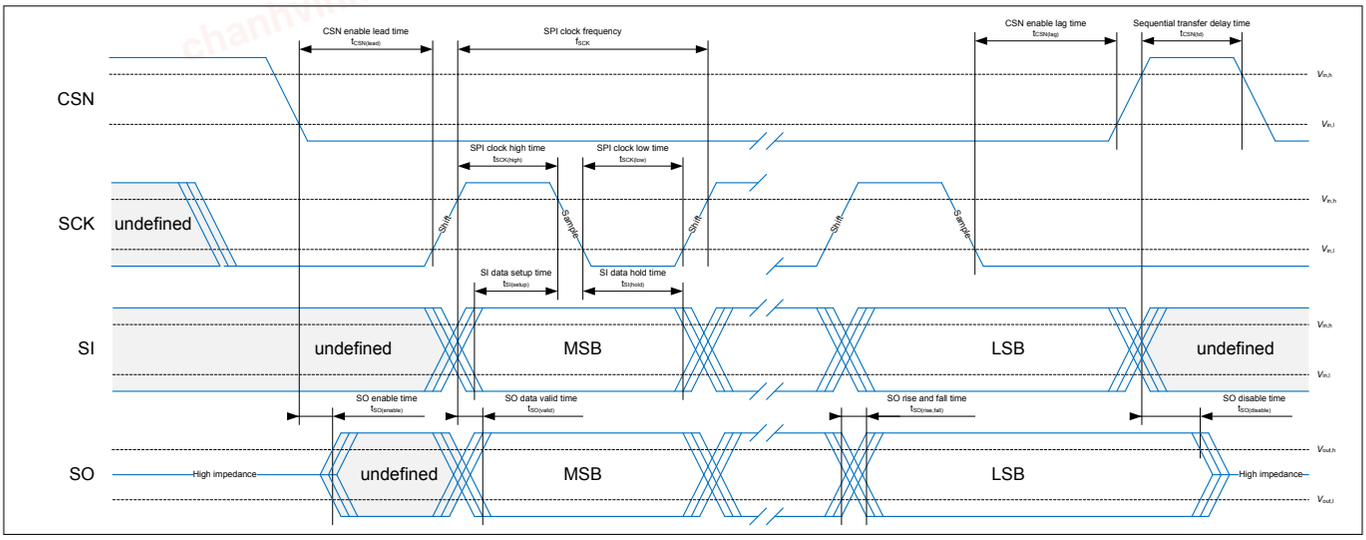


Figure 16 Timing diagram

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9.6 Electrical characteristics SPI

Table 26 Electrical characteristics SPI

T_J = -40°C to 150°C; V_{VS} = 10 - 18 V; V_{V5VI} = 5 V; all voltages with respect to AGND = PGND, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI SCK frequency	f_{SCK}	–	–	10	MHz		DS-250
SPI SCK high time	$t_{SCK(high)}$	37	–	–	ns		DS-251
SPI SCK low time	$t_{SCK(low)}$	37	–	–	ns		DS-252
SPI CSN enable lead time	$t_{CSN(lead)}$	35	–	–	ns		DS-253
SPI CSN enable lag time	$t_{CSN(lag)}$	25	–	–	ns		DS-254
SPI sequential transfer delay time	$t_{CSN(td)}$	500	–	–	ns		DS-255
SPI SI data setup time	$t_{SI(setup)}$	20	–	–	ns		DS-256
SPI SI data hold time	$t_{SI(hold)}$	20	–	–	ns		DS-257
SPI SO enable time	$t_{SO(enable)}$	0	–	50	ns	From CSN falling edge to SO high or low. Output load capacitance on SO pin is ≤ 60 pF.	DS-258
SPI SO disable time	$t_{SO(disable)}$	–	–	100	ns	From CSN rising edge to SO hi-Z. Output load capacitance on SO pin is ≤ 60 pF.	DS-259
SPI SO data valid time	$t_{SO(valid)}$	0	–	30	ns	Output load capacitance on SO pin is ≤ 60 pF.	DS-260
SPI SO rise and fall time	$t_{SO(rise;fall)}$	–	–	20	ns	Output load capacitance on SO pin is ≤ 30 pF.	DS-261
SPI SO tristate current	$I_{SO(tristate)}$	-10	–	10	µA		DS-262

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10 Registers

Bit type short name	Bit type description
r	read
w	write
rw	read/write
"X", "-"	do not care

10.1 Register Overview - TLE8082 (ascending Offset Address)

Table 27 Register Overview - TLE8082 (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
CTRL	Control Register Test	00_H	*50*
Diag0	General Diagnosis Register	02_H	*51*
Diag1	Output Stage Diagnosis Register	03_H	*53*
WD	Watchdog Register	06_H	*55*
Config	Configuration Register	07_H	*57*

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10.1.1 Control Register Test

For operation states Afterrun WD safe state, Normal operation WD inactive state and Normal operation WD safe state, the bits can be set without switching the power stage.

The register CTRL can be accessed by two addresses "000" and "001".

CTRL Offset address: 00_H

Control Register Test Reset values see: ***Table 28***

11	10	9	8	7	6	5	4	3	2	1	0
Res				**CTR4**	**CTR3**	**CTR2**	**CTR1**	**Res**			
r				rw	rw	rw	rw	r			

Field	Bits	Type	Description
CTR1	4	rw	**Output stage 1 control bit** 0_B OUT1 is switched off 1_B OUT1 is switched on
CTR2	5	rw	**Output stage 2 control bit** 0_B OUT2 is switched off 1_B OUT2 is switched on
CTR3	6	rw	**Output stage 3 control bit** 0_B OUT3 is switched off 1_B OUT3 is switched on
CTR4	7	rw	**Output stage 4 control bit** 0_B OUT4 is switched off 1_B OUT4 is switched on

Table 28 Reset Values of *CTRL*

Reset Type	Reset Value	Note
PowerOn	$X0X_H$	
Operation	$X0X_H$	

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10.1.2 General Diagnosis Register

Diag0 Offset address: 02_H

General Diagnosis Register Reset values see: ***Table 29***

11	10	9	8	7	6	5	4	3	2	1	0
KEY	**O3STAT**	**NRIORES**	**WDRES**	**V5VIOV**	**V5VIUV**	**COM5VOT**	**COM5VOV**	**COM5VUV**	**T5VOT**	**T5VOV**	**T5VUV**
r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
T5VUV	0	r	**T5V undervoltage bit** 0_B no undervoltage 1_B undervoltage
T5VOV	1	r	**T5V overvoltage bit** 0_B no overvoltage 1_B overvoltage
T5VOT	2	r	**T5V overtemperature bit** 0_B no overtemperature 1_B overtemperature
COM5VUV	3	r	**COM5V undervoltage bit** 0_B no undervoltage 1_B undervoltage
COM5VOV	4	r	**COM5V overvoltage bit** 0_B no overvoltage 1_B overvoltage
COM5VOT	5	r	**COM5V overtemperature bit** 0_B no overtemperature 1_B overtemperature
V5VIUV	6	r	**V5VI undervoltage bit** 0_B no undervoltage 1_B undervoltage
V5VIOV	7	r	**V5VI overvoltage bit** 0_B no overvoltage 1_B overvoltage
WDRES	8	r	**Watchdog reset bit** 0_B no watchdog reset occurred 1_B watchdog reset occurred
NRIORES	9	r	**NRIO reset bit** 0_B no NRIO reset occurred

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Registers

(continued)

Field	Bits	Type	Description
			1_B NRIO reset occurred
O3STAT	10	r	**Output stage 3 switching status bit** 0_B OUT3 switched off 1_B OUT3 switched on
KEY	11	r	**KEY input voltage status bit** 0_B KEY off - low voltage 1_B KEY on - high voltage

Table 29 Reset Values of *Diag0*

Reset Type	Reset Value	Note
PowerOn	000_H	
Operation	00XX XX00 0000_B	

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10.1.3 Output Stage Diagnosis Register

Diag1 Offset address: 03_H

Output Stage Diagnosis Register Reset values see: ***Table 30***

11	10	9	8	7	6	5	4	3	2	1	0
O4OT	**O4DIA**		**O3OT**	**O3DIA**		**O2OT**	**O2DIA**		**O1OT**	**O1DIA**	
r	r		r	r		r	r		r	r	

Field	Bits	Type	Description
O1DIA	1:0	r	**Output 1 diagnosis bits** 00_B no fault 01_B short circuit to battery 10_B open load in off 11_B short to ground in off
O1OT	2	r	**Output 1 overtemperature bit** 0_B no overtemperature 1_B overtemperature
O2DIA	4:3	r	**Output 2 diagnosis bits** 00_B no fault 01_B short circuit to battery 10_B open load in off 11_B short to ground in off
O2OT	5	r	**Output 2 overtemperature bit** 0_B no overtemperature 1_B overtemperature
O3DIA	7:6	r	**Output 3 diagnosis bits** 00_B no fault 01_B short circuit to battery 10_B open load in off 11_B short to ground in off
O3OT	8	r	**Output 3 overtemperature bit** 0_B no overtemperature 1_B overtemperature
O4DIA	10:9	r	**Output 4 diagnosis bits** 00_B no fault 01_B short circuit to battery 10_B open load in off 11_B short to ground in off
O4OT	11	r	**Output 4 overtemperature bit**

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Registers

(continued)

Field	Bits	Type	Description
			0_B no overtemperature 1_B overtemperature

Table 30 Reset Values of *Diag1*

Reset Type	Reset Value	Note
PowerOn	000_H	
Operation	000_H	

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10.1.4 Watchdog Register

WD

Watchdog Register

Offset address: 06_H

Reset values see: ***Table 31***

11	10	9	8	7	6	5	4	3	2	1	0
EC			**WDTO**	**WDCE**	**WDERR**	**WDOW**	**Res**	**WDP**		**WDC**	
r			r	r	r	rw	r	rw		w	

Field	Bits	Type	Description
WDC	1:0	w	**Watchdog check command bits** 01_B microcontroller check not ok 10_B microcontroller check ok not allowed
WDP	3:2	rw	**Watchdog period configuration bits** 00_B 32ms 01_B 48ms 10_B 64ms 11_B 128ms
WDOW	5	rw	**Watchdog open window configuration bit** 0_B short open window 1_B long open window
WDERR	6	r	**Watchdog error bit** 0_B no watchdog error occurred 1_B watchdog error occurred
WDCE	7	r	**Watchdog command too early status bit** 0_B watchdog command not too early 1_B watchdog command too early
WDTO	8	r	**Watchdog time out status bit** 0_B no watchdog timeout occurred 1_B watchdog timeout occurred
EC	11:9	r	**Error counter status bits** 000_B **ECready0**: Ready state … 100_B **ECready4**: Ready state 101_B **EC_safe5**: Safe state … 111_B **EC_safe7**: Safe state

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Registers

Table 31 Reset Values of *WD*

Reset Type	Reset Value	Note
PowerOn	1010 001X 1100_B	
Operation	1010 001X 1100_B	

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10.1.5 Configuration Register

Config Offset address: 07_H

Configuration Register Reset values see: ***Table 32***

11	10	9	8	7	6	5	4	3	2	1	0
Res					COM5VEN	T5VEN	AE	DRV4	SEL23	DRV23	DRV1
r					rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DRV1	0	rw	**Output stage 1 drive configuration** 0_B OUT1 driven by pin IN1 1_B OUT1 driven by SPI
DRV23	1	rw	**Output stage defined by SEL23 drive configuration** 0_B OUTx driven by pin IN23 1_B OUTx driven by SPI
SEL23	2	rw	**Output stage 2/3 drive selection** 0_B OUT2 is controlled by DRV23 configuration; OUT3 is controlled by SPI 1_B OUT3 is controlled by DRV23 configuration; OUT2 is controlled by SPI
DRV4	3	rw	**Output stage 4 drive configuration** 0_B OUT4 driven by pin IN4 1_B OUT4 driven by SPI
AE	4	rw	**Afterrun enable bit** 0_B no afterrun enabled 1_B afterrun enabled
T5VEN	5	rw	**T5V supply enable bit** 0_B T5V not enabled 1_B T5V enabled
COM5VEN	6	rw	**COM5V supply enable bit** 0_B COM5V not enabled 1_B COM5V enabled

Table 32 Reset Values of *Config*

Reset Type	Reset Value	Note
PowerOn	XXXX X110 0000_B	
Operation	XXXX X110 0000_B	

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11 Application information

Note: This is a simplified application circuit. The function must be verified in the real application.

Note: Analog GND (AGND) and power GND (PGND) can share the same potential. Low ohmic GND connection is required to avoid GND shifts.

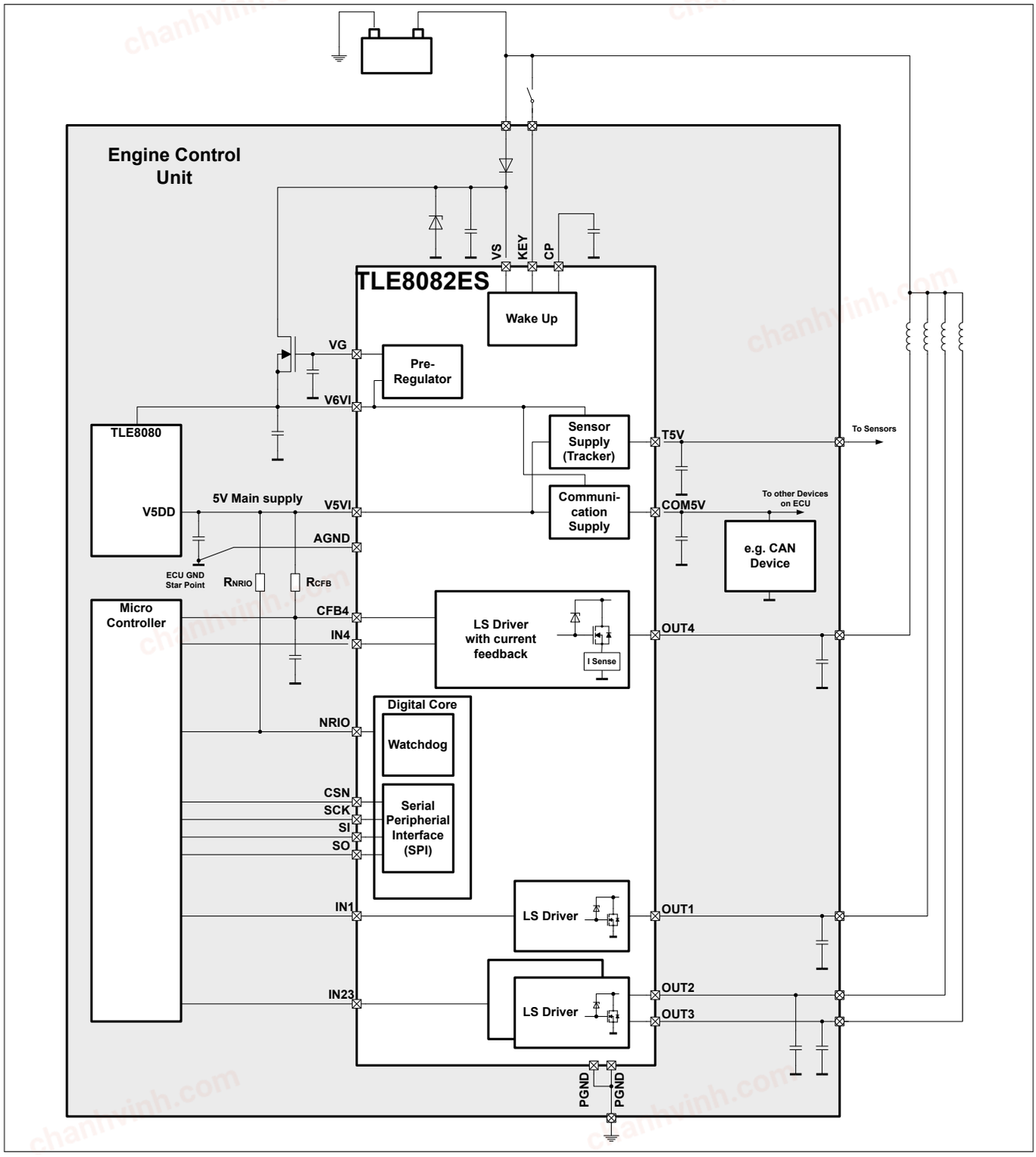
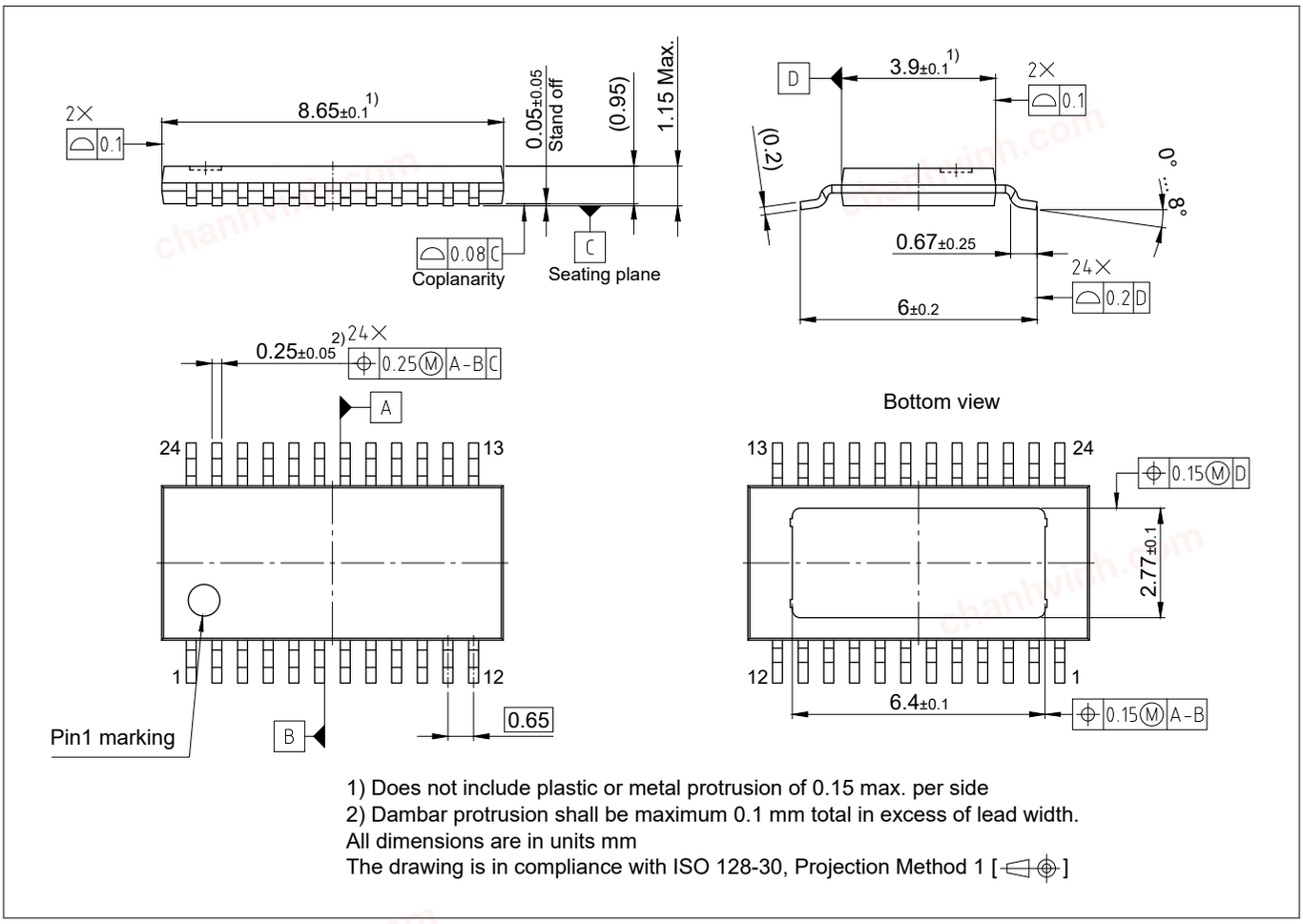


Figure 17 Application diagram

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12 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 18 PG-TSDSO-24

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on alternative packages

Please visit ***www.infineon.com/packages***.

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Revision history

Date	Revision	Changes
2021-03-23	1.0	Initial datasheet creation

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Trademarks

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