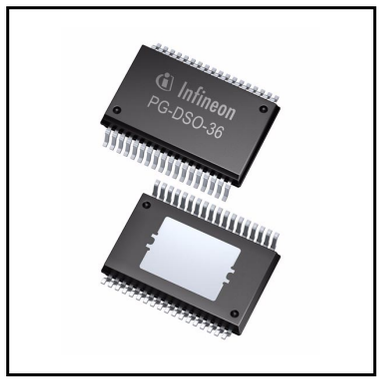
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TLE7368

Next Generation Microcontroller Supply

AEC Qualified RoHS



1 Overview

Features

- High efficient next generation microcontroller power supply system
- Wide battery input voltage range < 4.5 V up to 45 V
- Operating temperature range T_j = -40°C to +150°C
- Pre-regulator for low all over power loss:
  Integrated current mode Buck converter 5.5 V/2.5 A
- Post-regulators, e.g. for system and controller I/O supply:
  - LDO1: 5 V ±2%, 800 mA current limit
  - LDO2: 3.3 V ±2% or 2.6V ±2% (selectable output), 700 mA current limit
- Integrated linear regulator control circuit to supply controller cores:
  - LDO3 control for an external NPN power stage:
  - 1.5 V ±2% at TLE7368E
  - 1.2 V ±2% at TLE7368-2E
  - 1.3 V ±2% at TLE7368-3E
- Post-regulators for off board supply:
  - 2 Tracking regulators following the main 5 V, 105 mA and 50 mA
- Stand-by regulator with lowest current consumption:
  - Linear voltage regulator as stand-by supply for e.g.memory circuits
  - Hardware selectable output voltages as 1.0 V or 2.6 V, 30 mA
  - Independent battery input, separated from Buck regulator input
- Hardware controlled on/off logic
- Undervoltage detection:
  - Undervoltage reset circuits with adjustable reset delay time at power up
  - Undervoltage monitoring circuit on stand-by supply
- Window watchdog circuit
- Overcurrent protection on all regulators
- Power sequencing on controller supplies
- Overtemperature shutdown
- Package: Small exposed pad PG-DSO-36
- Green Product (RoHS compliant)

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TLE7368

Next Generation Microcontroller Supply

Overview

Potential application

Microcontroller supply

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The **TLE7368** device is a multifunctional power supply circuit especially designed for Automotive powertrain systems using a standard 12 V battery. The device is intended to supply and monitor next generation 32-bit microcontroller families (13 µm lithography) where voltage levels such as 5 V, 3.3 V or 1.5/1.2/1.3 V are required.

The regulator follows the concept of its predecessor TLE6368/SONIC, where the output of a pre-regulator feeds the inputs of the micro's linear supplies. In detail, the **TLE7368** cascades a Buck converter with linear regulators and voltage followers to achieve lowest power dissipation. This configuration allows to power the application even at high ambient temperatures.

The step-down converter delivers a pre-regulated voltage of 5.5 V with a minimum peak current capability of 2.5 A.

Supplied by this step down converter two low drop linear post-regulators offer 5 V and 3.3 V (2.6 V) with high accuracy. The current capability of the regulators is 800 mA and 700 mA. The 3.3 V (2.6 V) linear regulator does have its own input allowing to insert a dropper from the Buck output to reduce the on chip power dissipation if necessary. For the same reason, reduction of on chip power dissipation, the core supply (1.5 V, 1.2 V or 1.3 V) follows the concept of integrated control circuit with external power stage.

Implementing the on board and microcontroller supplies in this way described, allows operation even at high ambient temperatures.

The regulator system contains the so called power sequencing function which provides a controlled power up sequence of the three output voltages.

In addition to the main regulators the inputs of two voltage trackers are connected to the 5.5 V Buck converter output voltage. Their protected outputs follow the main 5 V linear regulator with high accuracy and are able to drive loads of 50 mA and 105 mA.

To monitor the output voltage levels of each of the linear regulators two independent undervoltage detection circuits are available. They can be used to implement the reset or an interrupt function.

For energy saving reasons, e.g. while the motor is turned off, the **TLE7368** offers a stand-by mode. The standby mode can be enabled and disabled either by battery or the microcontroller. In this stand-by mode just the stand-by regulator remains active and the current drawn from battery is reduced to a minimum for extended battery lifetime. A selection pin allows to configure the output voltages of the stand-by regulator to the application's needs. The input of the stand-by regulator is separated from the high power input of the pre-/post-regulator system.

The **TLE7368** is based on Infineon's Power technology SPT™ which allows bipolar, CMOS and power DMOS circuitry to be integrated on the same monolithic chip/circuitry.

Type	Package	Marking
TLE7368E	PG-DSO-36	TLE7368 E
TLE7368-2E	PG-DSO-36	TLE7368-2 E
TLE7368-3E	PG-DSO-36	TLE7368-3 E

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2 Block Diagram

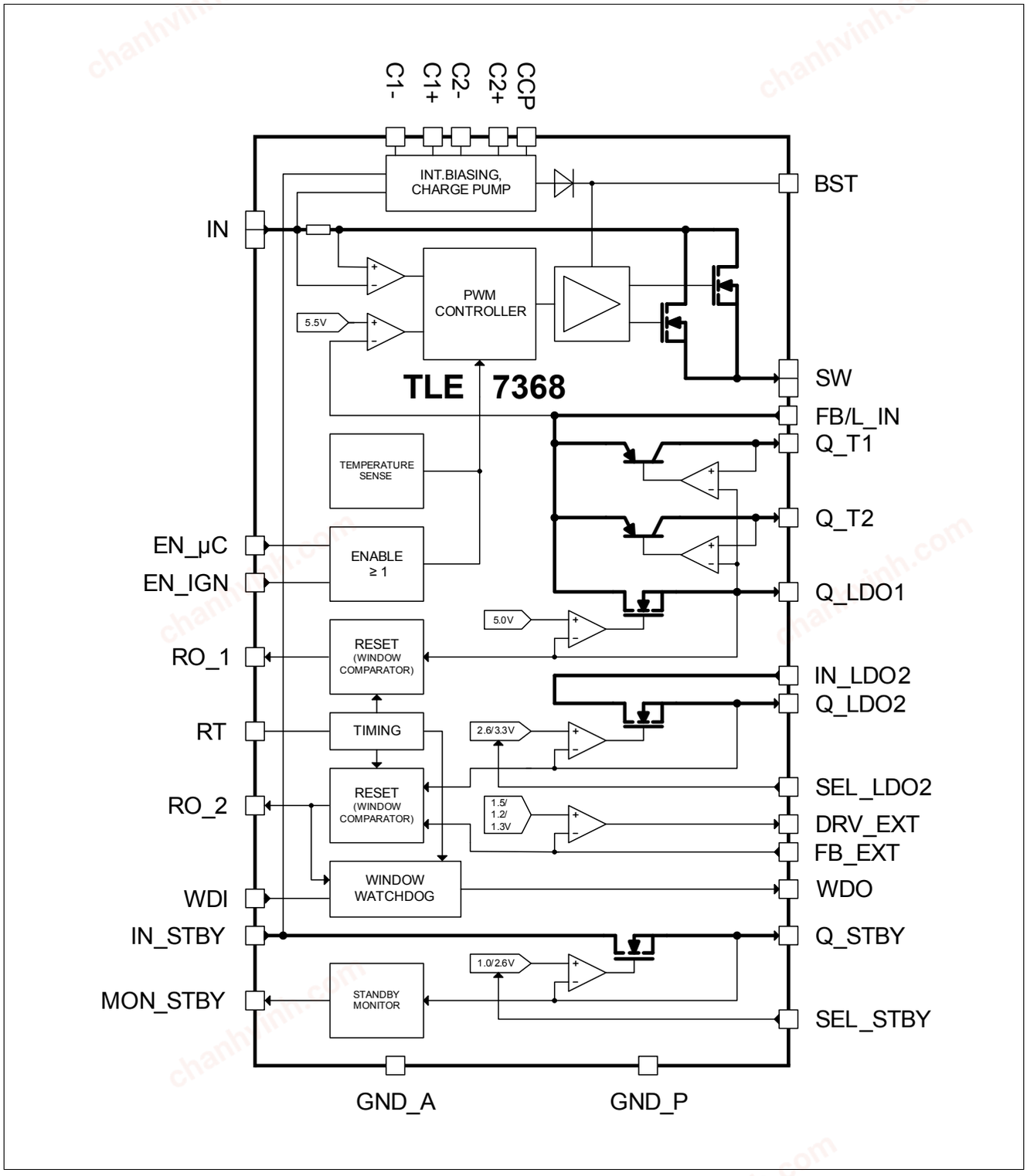


Figure 1 Block Diagram

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3 Pin Configuration

3.1 Pin Assignment

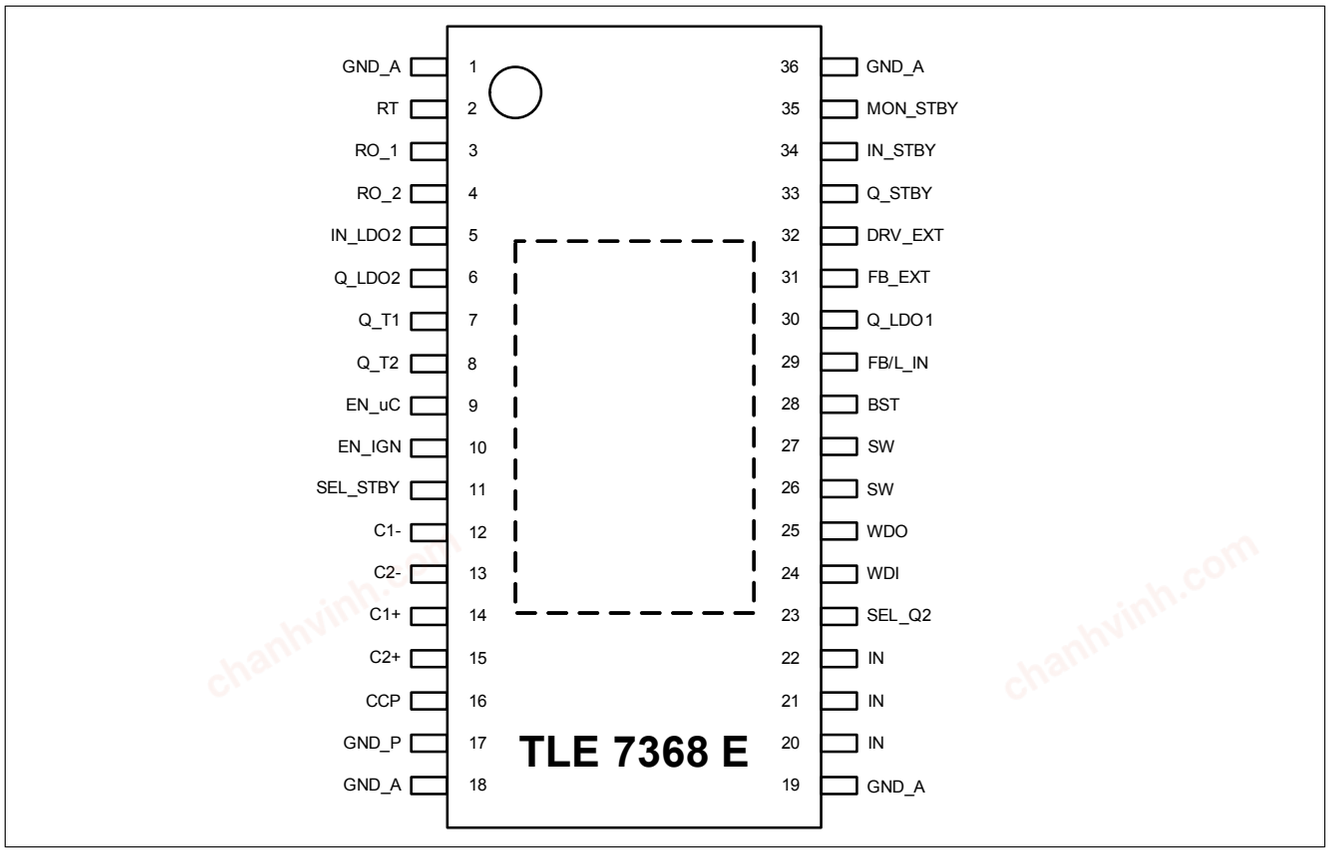


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions TLE7368E

Pin	Symbol	Function
1	GND_A	**Analog ground connection;** Connect to heatslug resp. exposed pad.
2	RT	**Reset and watchdog timing pin;** Connect a ceramic capacitor to GND to determine the time base for the reset delay circuits and the watchdog cycle time
3	RO_1	**Reset output Q_LDO1;** Open drain output, active low. Connect an external 10 kΩ pull-up resistor to microcontroller I/O voltage.
4	RO_2	**Reset output Q_LDO2 and FB_EXT;** Open drain output, active low. Connect an external 10 kΩ pull-up resistor to microcontroller I/O voltage
5	IN_LDO2	**LDO2 input;** Connect this pin straight to the Buck converter output or add a dropper in between to reduce power dissipation on the chip.

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Pin Configuration

Pin	Symbol	Function
6	Q_LDO2	**Voltage regulator 2 output;** 3.3 V or 2.6 V, depending on the state of SEL_LDO2. Block to GND with capacitor close to the IC pins for stable regulator operation; selection of capacitor C_{Q_LDO2} according to **Chapter 4.4** and **Chapter 6**.
7	Q_T1	**Tracking regulator 1 output;** Block to GND with capacitor close to the IC pins for stable regulator operation; selection of capacitor C_{Q_T1} according to **Chapter 4.4** and **Chapter 6**.
8	Q_T2	**Tracking regulator 2 output;** Block to GND with capacitor close to the IC pins for stable regulator operation; selection of capacitor C_{Q_T2} according to **Chapter 4.4** and **Chapter 6**.
9	EN_uC	**Enable input microcontroller;** High level enables / low level disables the IC except the stand-by regulators; Integrated pull-down resistor
10	EN_IGN	**Enable input ignition line;** High level enables / low level disables the IC except the stand-by regulators; Integrated pull-down resistor
11	SEL_STBY	**Selection input for stand-by regulator;** Connect to GND to select 2.6 V output voltage for Q_STBY; Connect straight to Q_STBY to select 1.0 V output voltage for Q_STBY
12	C1-	**Charge pump negative #1;** Connect a ceramic capacitor 100 nF, to C1+
13	C2-	**Charge pump negative #2;** Connect a ceramic capacitor 100 nF, toC2+
14	C1+	**Charge pump positive #1;** Connect a ceramic capacitor 100 nF, to C1-
15	C2+	**Charge pump positive #2;** Connect a ceramic capacitor 100 nF, to C2-
16	CCP	**Charge pump output;** Connect a ceramic capacitor, 220 nF, to GND; Used for internal IC supply, do not use for other circuitry.
17	GND_P	**Power ground;** Exclusive GND connection of charge pump; Connect this pin to the power ground star point on the PCB.
18, 19	GND_A	**Analog ground connection;** Connect to exposed pad.
20, 21, 22	IN	**Buck regulator input;** Connect to a pi-filter (or if not used to battery) with short lines; connect filter capacitors in any case with short lines; connect a small ceramic directly at the pin; For details refer to **Chapter 6**. Interconnect the pins.
23	SEL_LDO2	**Selection input LDO2;** Connect to GND to select 2.6 V output voltage for LDO2; Connect straight to Q_LDO2 to select 3.3 V output voltage for LDO2.

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Pin Configuration

Pin	Symbol	Function
24	WDI	**Window Watchdog input;** Apply a watchdog trigger signal to this pin
25	WDO	**Window Watchdog output;** Open drain output, active low, connect external 10 kΩ pull-up resistor to microcontroller I/O voltage
26, 27	SW	**Buck power stage's output;** Connect both pins directly, on short lines, to the Buck converter circuit, i.e. the catch diode and the Buck inductance
28	BST	**Bootstrap driver supply input;** Connect the buck power stage's driver supply capacitor to the SW pins; For capacitor selection please refer to **Chapter 6**.
29	FB/L_IN	**Buck converter feedback input plus input for LDO1 and trackers;** Connect the output of the buck converter circuit with short lines to these pins; For Buck output capacitor selection please refer to **Chapter 6**.
30	Q_LDO1	**Voltage regulator 1 output;** 5 V output; Block to GND with capacitor close to the IC pins for stable regulator operation; Selection of capacitor C_{Q_LDO1} according to **Chapter 4.4** and **Chapter 6**.
31	FB_EXT	**External regulator feedback input;** Feedback input of control loop for the external power stage regulator. Connect to the emitter of the regulating transistor; Block to GND with capacitor close to the IC pins for stable regulator operation; Selection of capacitor $C_{Q_FB_EXT}$ according to **Chapter 4.4** and **Chapter 6**.
32	DRV_EXT	**Bipolar power stage driver output;** Connect the base of an external NPN transistor directly to this pin; Regarding choice of the external power stage refer to **Chapter 6**.
33	Q_STBY	**Stand-by regulator output;** Output voltage depending on the state of SEL_STBY; Block to GND with capacitor close to the IC pins for stable regulator operation; Selection of capacitor C_{Q_STBY} according to **Chapter 4.4** and **Chapter 6**.
34	IN_STBY	**Input to stand-by regulator;** Always connect the reverse polarity protected battery line to this pin; Input to all IC internal biasing circuits; Block to GND directly at the IC with ceramic capacitor; For proper choice of input capacitors please refer to **Chapter 6**.
35	MON_STBY	**Monitoring output for stand-by regulator;** power fail active low output with special timing, open drain, connect external pull-up resistor.
36	GND_A	**Analog ground connection;** Connect to exposed pad.

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4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1], T_j = -40°C to +150°C; all voltages with respect to ground.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Stand-by Regulator Input IN_STBY							
Voltage	V_{IN_STBY}	-0.3	–	45	V	–	P_4.1.1
Current	I_{IN_STBY}	–	–	–	A	Limited internally	P_4.1.2
Selection Input SEL_STBY							
Voltage	V_{SEL_STBY}	-0.3	–	5.5	V	–	P_4.1.3
Voltage	V_{SEL_STBY}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.4
Current	I_{SEL_STBY}	–	–	–	A	Limited internally	P_4.1.5
Buck Regulator Inputs IN							
Voltage	V_{IN}	V_{SW} - 0.3	–	45	V	–	P_4.1.6
Voltage	V_{IN}	-0.3	–	45	V	–	P_4.1.7
Current	I_{IN}	–	–	–	A	Limited internally	P_4.1.8
Watchdog Input WDI							
Voltage	V_{WDI}	-0.3	–	5.5	V	–	P_4.1.9
Voltage	V_{WDI}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.10
Current	I_{WDI}	–	–	–	A	Limited internally	P_4.1.11
Watchdog Output WDO							
Voltage	V_{WDO}	-0.3	–	5.5	V	–	P_4.1.12
Voltage	V_{WDO}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.13
Current	I_{WDO}	–	–	–	A	Limited internally	P_4.1.14
Charge Pump Positive C<1+, 2+>							
Voltage	$V_{C<1+,\ 2+>}$	-0.3	–	18	V	–	P_4.1.15
Current	$I_{C<1+,\ 2+>}$	–	–	–	mA	–	P_4.1.16
Charge Pump Negative C<1-, 2->							
Voltage	$V_{C<1-,\ 2->}$	-0.3	–	5.5	V	–	P_4.1.17
Current	$I_{C<1-,\ 2->}$	–	–	–	mA	–	P_4.1.18
Charge Pump Output CCP							
Voltage	V_{CCP}	-0.3	–	18	V	–	P_4.1.19
Current	I_{CCP}	–	–	–	mA	–	P_4.1.20
Reset Output RO_1							
Voltage	V_{RO_1}	-0.3	–	5.5	V	–	P_4.1.21
Voltage	V_{RO_1}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.22

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Table 1 Absolute Maximum Ratings[1], T_j = -40°C to +150°C; all voltages with respect to ground.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current	I_{RO_1}	–	–	–	A	Limited internally	P_4.1.23
Reset Output RO_2							
Voltage	V_{RO_2}	-0.3	–	5.5	V	–	P_4.1.24
Voltage	V_{RO_2}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.25
Current	I_{RO_2}	–	–	–	A	Limited internally	P_4.1.26
Reset Timing RT							
Voltage	V_{RT}	-0.3	–	5.5	V	–	P_4.1.27
Voltage	V_{RT}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.28
Current	I_{RT}	–	–	–	A	Limited internally	P_4.1.29
Tracking Regulator Outputs Q_T<1..2>							
Voltage	$V_{Q_T<1..2>}$	-5	–	40	V	V_{FB/L_IN} = 5.5V	P_4.1.30
Voltage	$V_{Q_T<1..2>}$	-5	–	35	V	off mode; V_{FB/L_IN} = 0V	P_4.1.31
Current	$I_{Q_T<1..2>}$	–	–	–	A	Limited internally	P_4.1.32
Enable Ignition EN_IGN							
Voltage	V_{EN_IGN}	-0.3	–	45	V	–	P_4.1.33
Current	I_{EN_IGN}	–	–	–	mA	–	P_4.1.34
Enable Micro EN_uC							
Voltage	V_{EN_uC}	-0.3	–	5.5	V	–	P_4.1.35
Voltage	V_{EN_uC}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.36
Current	I_{EN_uC}	-5	–	5	mA	–	P_4.1.37
Voltage Regulator Outputs Q_LDO<1..2>							
Voltage	V_{Q_LDO1}	-0.3	–	V_{FB/L_IN} + 0.3	V	–	P_4.1.38
Voltage	V_{Q_LDO2}	-0.3	–	V_{IN_LDO2} + 0.3	V	–	P_4.1.39
Voltage	$V_{Q_LDO<1..2>}$	-0.3	–	5.5	V	–	P_4.1.40
Voltage	$V_{Q_LDO<1..2>}$	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.41
Current	$I_{Q_LDO<1..2>}$	–	–	–	A	Limited internally	P_4.1.42
Selection Input SEL_LDO2							
Voltage	V_{SEL_LDO2}	-0.3	–	5.5	V	–	P_4.1.43
Voltage	V_{SEL_LDO2}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.44
Current	I_{SEL_LDO2}	–	–	–	A	Limited internally	P_4.1.45
External Driver Output DRV_EXT							
Voltage	V_{DRV_EXT}	-0.3	–	5.5	V	–	P_4.1.46
Voltage	V_{DRV_EXT}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.47
Current	I_{DRV_EXT}	–	–	–	A	Limited internally	P_4.1.48

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Table 1 Absolute Maximum Ratings[1], T_j = -40°C to +150°C; all voltages with respect to ground.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
External Regulator Feedback Input FB_EXT							
Voltage	V_{FB_EXT}	-0.3	–	5.5	V	–	P_4.1.49
Voltage	V_{FB_EXT}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.50
Current	I_{FB_EXT}	–	–	–	A	Limited internally	P_4.1.51
Feedback and Post-Regulators Input FB/L_IN							
Voltage	V_{FB/L_IN}	V_{Q_LDO1} - 0.3	–	18	V	–	P_4.1.52
Voltage	V_{FB/L_IN}	-0.3	–	18	V	–	P_4.1.53
Current	I_{FB/L_IN}	–	–	–	A	Limited internally	P_4.1.54
Linear Regulator 2 Input IN_LDO2							
Voltage	V_{IN_LDO2}	V_{Q_LDO2} - 0.3	–	18	V	–	P_4.1.55
Voltage	V_{IN_LDO2}	-0.3	–	18	V	–	P_4.1.56
Current	I_{IN_LDO2}	–	–	–	A	Limited internally	P_4.1.57
Bootstrap Supply BST							
Voltage	V_{BST}	V_{SW} - 0.3	–	V_{SW} + 5.5	V	–	P_4.1.58
Voltage	V_{BST}	-0.3	–	51	V	–	P_4.1.59
Current	I_{BST}	–	–	–	A	Limited internally	P_4.1.60
Buck Power Stage SW							
Voltage	V_{SW}	-2	–	V_{IN} + 0.3	V	–	P_4.1.61
Voltage	V_{SW}	-2	–	45	V	–	P_4.1.62
Current	I_{SW}	–	–	–	A	Limited internally	P_4.1.63
Stand-by Regulator Output Q_STBY							
Voltage	V_{Q_STBY}	-0.3	–	5.5	V	–	P_4.1.64
Voltage	V_{Q_STBY}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.65
Current	I_{Q_STBY}	–	–	–	A	Limited internally	P_4.1.66
Monitoring Output MON_STBY							
Voltage	V_{MON_STBY}	-0.3	–	5.5	V	–	P_4.1.67
Voltage	V_{MON_STBY}	-0.3	–	6.2	V	t < 10 s[2]	P_4.1.68
Current	I_{MON_STBY}	–	–	–	A	Limited internally	P_4.1.69
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.70
Storage Temperature	T_{stg}	-50	–	150	°C	–	P_4.1.71
ESD-Protection (Human Body Model)							
Electrostatic discharge voltage	V_{ESD}	-2	–	2	kV	Human Body Model (HBM)[3]	P_4.1.72

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Table 1 Absolute Maximum Ratings[1], T_j = -40°C to +150°C; all voltages with respect to ground.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD-Protection (Charged Device Model)							
Electrostatic discharge voltage to GND	V_{ESD}	-500	–	500	V	Charged Device Model (CDM)[4]	P_4.1.73
Electrostatic discharge voltage, corner pins to GND	V_{ESD}	-750	–	750	V	Charged Device Model (CDM)[4]	P_4.1.74

1) Not subject to production test, specified by design.
2) Exposure to those absolute maximum ratings for extended periods of time (t > 10 s) may affect device reliability.
3) According to JEDEC standard EIA/JESD22-A114-B (1.5 kΩ, 100 pF)
4) According to EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Stand-by input voltage	V_{IN_STBY}	3.0	–	45	V	1)	P_4.2.1
Buck input voltage	V_{IN}	4.5	–	45	V	1)	P_4.2.2
Peak to peak ripple voltage at FB/L_IN	V_{FB/L_IN}	0	–	150	mVpp	–	P_4.2.3
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) At minimum battery voltage regulators with higher nominal output voltage will not be able to provide the full output voltage. Their outputs follow the battery with certain drop.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

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4.3 Thermal Resistance

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PG-DSO-36							
Junction to ambient	R_{thJA}	–	54	–	K/W	Footprint only[1)]	P_4.3.5
Junction to ambient	R_{thJA}	–	42	–	K/W	Heat sink area 300mm^2 [1)]	P_4.3.6
Junction to ambient	R_{thJA}	–	35	–	K/W	Heat sink area 600mm^2 [1)]	P_4.3.7
Junction to case	R_{thJC}	–	5.6	–	K/W	–	P_4.3.8

1) Worst case regarding peak temperature; zero airflow; mounted on FR4; 80 × 80 × 1.5 mm^3; 35 µm Cu; 5 µm Sn

4.4 Electrical Characteristics

Table 4 Electrical Characteristics, $V_{IN} = V_{IN_STBY}$ = 13.5 V, T_j = -40°C to +150°C, V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Buck Regulator							
Switching frequency	f	280	370	425	kHz	–	P_4.4.1
Current transition rise/fall time	$t_{r,I}$	–	50	–	ns	[1)]; slope magnitude 1 A; fixed internally	P_4.4.2
Power stage on resistance	$R_{ON,Buck}$	–	–	280	mΩ	–	P_4.4.3
Power stage peak current limit	$I_{peak,SW}$	2.5	–	4.6	A	V_{IN} = 5.0 V; V_{SW} ramped down from 5.0 V to 3.7 V; V_{FB/L_IN} = 5.0 V	P_4.4.4
Buck converter output voltage	V_{FB/L_IN}	5.4	–	6.0	V	I_{Buck} = 2.0 A[2)]	P_4.4.5
Buck converter output voltage	V_{FB/L_IN}	5.4	–	6.4	V	I_{Buck} = 100 mA[2)]	P_4.4.6
Buck converter, turn on threshold	$V_{IN,on}$	–	–	4.5	V	V_{IN} increasing	P_4.4.7
Buck converter, turn off threshold	$V_{IN,off}$	3.5	–	–	V	V_{IN} decreasing	P_4.4.8
Buck converter On/off hysteresis	$V_{IN,hyst}$	450	500	550	mV	$V_{IN,hyst} = V_{IN,on} - V_{IN,off}$	P_4.4.9

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Table 4 Electrical Characteristics, V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40°C to +150°C, V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground. (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bootstrap undervoltage lockout, turn on threshold	$V_{BST_UV, on}$	–	–	V_{SW} + 5.0	V	Bootstrap voltage increasing	P_4.4.10
Bootstrap undervoltage lockout, turn off threshold	$V_{BST_UV, off}$	V_{SW} + 3.2	–	–	V	Bootstrap voltage decreasing	P_4.4.11
Bootstrap undervoltage lockout, hysteresis	$V_{BST_UV, hyst}$	0.2	–	1	V	$V_{BST_UV, hyst}$ = $V_{BST_UV, on}$ - $V_{BST_UV, off}$	P_4.4.12
Charge Pump							
Charge pump voltage	V_{CCP}	9	–	15	V	C_{C1} = 100 nF; C_{C2} = 100 nF; C_{CCP} = 220 nF	P_4.4.13
Charge pump voltage	V_{CCP}	9	–	13.5	V	V_{IN} = 4.5 V; C_{C1} = 100 nF; C_{C2} = 100 nF; C_{CCP} = 220 nF	P_4.4.14
Charge pump switching frequency	f_{CCP}	1.0	–	2.5	MHz	–	P_4.4.15
Voltage Regulator Q_LDO1							
Output voltage	V_{Q_LDO1}	4.9	–	5.1	V	1 mA < I_{Q_LDO1} < 700 mA[3]	P_4.4.16
Output current limitation	$I_{Q_LDO1, lim}$	800	–	1600	mA	V_{Q_LDO1} = 4.0 V	P_4.4.17
Drop voltage	V_{dr, Q_LDO1}	–	–	400	mV	I_{Q_LDO1} = 500 mA; V_{FB/L_IN} = 5.0 V;[3] [4]	P_4.4.18
Drop voltage	V_{dr, Q_LDO1}	–	–	400	mV	I_{Q_LDO1} = 250 mA; V_{IN} = 4.5 V;[3] [4]	P_4.4.19
Load regulation	ΔV_{Q_LDO1}	–	60	120	mV/A	–	P_4.4.20
Power supply ripple rejection	$PSRR_{Q_LDO1}$	26	–	–	dB	V_{FB/L_IN} = 5.6 V; $V_{FB/L_IN, ripple\ pp}$ = 150 mV; $f_{FB/L_IN, ripple}$ = 370 kHz; I_{Q_LDO1} = 250 mA; C_{Q_LDO1} = 4.7 µF, X7R[1]	P_4.4.21
Output capacitor	C_{Q_LDO1}	1	–	470	µF	[1] [5]	P_4.4.22
Output capacitor	ESR C_{Q_LDO1}	–	–	2	Ω	at 10 kHz[1]	P_4.4.23
Voltage Regulator Q_LDO2							
Output voltage	V_{Q_LDO2}	3.23	–	3.37	V	SEL_LDO2 = Q_LDO2; IN_LDO2 = FB/L_IN; 1 mA < I_{Q_LDO2} < 500 mA	P_4.4.24

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Table 4 Electrical Characteristics, V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40°C to +150°C, V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground. (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output current limitation	$I_{Q_LDO2, lim}$	700	–	1400	mA	SEL_LDO2 = Q_LDO2; IN_LDO2 = FB/L_IN; V_{Q_LDO2} = 2.8 V	P_4.4.25
Drop voltage	V_{dr, Q_LDO2}	–	–	400	mV	SEL_LDO2 = Q_LDO2; V_{CCP} = 9 V; I_{Q_LDO2} = 500 mA;[4) 6)]	P_4.4.26
Drop voltage	V_{dr, Q_LDO2}	–	–	400	mV	SEL_LDO2 = Q_LDO2; V_{CCP} = 9 V; I_{Q_LDO2} = 250 mA; V_{IN} = 4.5 V; [4)6)]	P_4.4.27
Load regulation	ΔV_{Q_LDO2}	–	–	80	mV/A	3.3 V mode 1 mA < I_{Q_LDO2} < 650 mA	P_4.4.28
Output voltage	V_{Q_LDO2}	2.56	–	2.67	V	SEL_LDO2 = GND; IN_LDO2 = FB/L_IN; 1 mA < I_{Q_LDO2} < 500 mA	P_4.4.29
Output current limitation	$I_{Q_LDO2, lim}$	700	–	1400	mA	SEL_LDO2 = GND; IN_LDO2 = FB/L_IN; V_{Q_LDO2} = 2.0 V	P_4.4.30
Drop voltage	V_{dr, Q_LDO2}	–	–	400	mV	SEL_LDO2 = GND; V_{CCP} = 9 V; I_{Q_LDO2} = 500 mA;[4)6)]	P_4.4.31
Drop voltage	V_{dr, Q_LDO2}	–	–	400	mV	SEL_LDO2 = GND; V_{CCP} = 9 V; I_{Q_LDO2} = 250 mA; V_{IN} = 4.5 V;[4)6)]	P_4.4.32
Load regulation	ΔV_{Q_LDO2}	–	–	65	mV/A	2.6 V mode 1 mA < I_{Q_LDO2} < 650 mA	P_4.4.33
Power supply ripple rejection	$PSRR_{Q_LDO2}$	26	–	–	dB	V_{IN_LDO2} = 5.6 V; $V_{IN_LDO2, ripple\ pp}$ = 150 mV; $f_{IN_LDO2, ripple}$ = 370 kHz; I_{Q_LDO2} = 250mA; C_{Q_LDO2} = 4.7 µF ceramic X7R[1)]	P_4.4.34
Selector Pull-down resistor	R_{SEL_LDO2}	0.7	1.2	1.9	MΩ	–	P_4.4.35
Output capacitor	C_{Q_LDO2}	1	–	470	µF	[1)5)]	P_4.4.36
Output capacitor	ESR C_{Q_LDO2}	–	–	2	Ω	at 10 kHz;[1)]	P_4.4.37
External Voltage Regulator Control							
Driver current limit	$I_{DRV_EXT, lim}$	75	–	150	mA	TLE7368E V_{FB_EXT} = 1.2 V	P_4.4.38
Driver current limit	$I_{DRV_EXT, lim}$	75	–	150	mA	TLE7368-2E V_{FB_EXT} = 0.9V	P_4.4.39

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Table 4 Electrical Characteristics, V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40°C to +150°C, V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground. (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Driver current limit	$I_{DRV_EXT, lim}$	75	–	150	mA	TLE7368-3E V_{FB_EXT} = 1.0V	P_4.4.40
Feedback voltage	V_{FB_EXT}	1.505	–	1.55	V	TLE7368E	P_4.4.41
Feedback voltage	V_{FB_EXT}	1.19	–	1.23	V	TLE7368-2E	P_4.4.42
Feedback voltage	V_{FB_EXT}	1.30	–	1.34	V	TLE7368-3E	P_4.4.43
Feedback input current	I_{FB_EXT}	-250	–	–	µA	–	P_4.4.44
Load regulation	ΔV_{FB_EXT}	–	–	20	mV/A	V_{FB/L_IN} = 5.4 V; V_{CCP} = 9.0 V; I_{Q_LDO3} = 100 µA to 1 A;[7)]	P_4.4.45
Output capacitor	C_{FB_EXT}	4.7	–	–	µF	[2)5)7)] I_{Q_LDO3} = 1 A	P_4.4.46
Output capacitor	ESR C_{FB_EXT}	0.006	–	0.1	Ω	at 1 MHz;[2)]	P_4.4.47
Voltage Tracker Q_T1							
Output voltage tracking accuracy to Q_LDO1	ΔV_{Q_T1}	-10	–	10	mV	0 mA < I_{Q_T1} < 105 mA	P_4.4.48
Output current limitation	I_{Q_T1}	120	–	240	mA	V_{Q_T1} = 4.0 V	P_4.4.49
Drop voltage	V_{dr, Q_T1}	–	–	400	mV	I_{Q_T1} = 105 mA; V_{FB/L_IN} = 5.3 V; V_{Q_LDO1} = 5.0 V[4)]	P_4.4.50
Power supply ripple rejection	$PSRR_{Q_T1}$	26	–	–	dB	V_{FB/L_IN} = 5.6 V; $V_{FB/L_IN, ripple\ pp}$ = 150 mV; $f_{FB/L_IN, ripple}$ = 370 kHz; V_{Q_LDO1} = 5.0 V; I_{Q_T1} = 100 mA; C_{Q_T1} = 4.7 µF ceramic X7R;[1)]	P_4.4.51
Output capacitor	C_{Q_T1}	4.7	–	–	µF	[1)5)]	P_4.4.52
Output capacitor	ESR C_{Q_T1}	–	–	3	Ω	at 10 kHz;[1)]	P_4.4.53
Voltage Tracker Q_T2							
Output voltage tracking accuracy to Q_LDO1	ΔV_{Q_T2}	-10	–	10	mV	0 mA < I_{Q_T2} < 50 mA;	P_4.4.54
Output current limitation	I_{Q_T2}	60	–	110	mA	V_{Q_T2} = 4.0 V	P_4.4.55
Drop voltage	V_{dr, Q_T2}	–	–	400	mV	I_{Q_T2} = 50 mA; V_{FB/L_IN} = 5.3 V; V_{Q_LDO1} = 5.0 V[4)]	P_4.4.56

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Table 4 Electrical Characteristics, V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40°C to +150°C, V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground. (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power supply ripple rejection	$PSRR_{Q_T2}$	26	–	–	dB	V_{FB/L_IN} = 5.6 V; $V_{FB/L_IN,\ ripple\ pp}$ = 150 mV; $f_{FB/L_IN,\ ripple}$ = 370 kHz; V_{Q_LDO1} = 5.0 V; I_{Q_T2} = 40 mA; C_{Q_T2} = 4.7 µF ceramic X7R;[1)]	P_4.4.57
Output capacitor	C_{Q_T2}	4.7	–	–	µF	[1)5)]	P_4.4.58
Output capacitor	ESR C_{Q_T2}	–	–	3	Ω	at 10 kHz;[1)]	P_4.4.59
Stand-by Regulator							
Output voltage	V_{Q_STBY}	0.93	1.02	1.08	V	V_{IN_STBY} > 3 V; 100 µA < I_{Q_STBY} < 10 mA; SEL_STBY = Q_STBY	P_4.4.60
Output voltage	V_{Q_STBY}	0.93	1.02	1.08	V	V_{IN_STBY} > 4.5 V; I_{Q_STBY} = 30 mA; SEL_STBY = Q_STBY	P_4.4.61
Output voltage	V_{Q_STBY}	2.51	2.62	2.73	V	V_{IN_STBY} > 3.0 V; 100 µA < I_{Q_STBY} < 10 mA; SEL_STBY = GND	P_4.4.62
Selector pull-up current	I_{SEL_STBY}	-2	-5	-10	µA	SEL_STBY = GND	P_4.4.63
Output current limitation	$I_{Q_STBY,\ lim}$	31	–	90	mA	V_{Q_STBY} = 0.5 V	P_4.4.64
Load regulation	ΔV_{Q_STBY}	–	–	5	V/A	I_{Q_STBY} = 100µA to 10 mA; V_{IN_STBY} > 4.5 V; SEL_STBY = Q_STBY; V_{Q_STBY} = 1.0V	P_4.4.65
		–	–	10	V/A	I_{Q_STBY} = 100µA to 10 mA; V_{IN_STBY} > 4.5 V; SEL_STBY = GND; V_{Q_STBY} = 2.6V	
Line regulation	ΔV_{Q_STBY}	–	–	5	mV/V	–	P_4.4.66
Power supply ripple rejection	$PSRR_{Q_STBY}$	60	–	–	dB	$V_{IN_STBY,\ ripple\ pp}$ = 500 mV; $f_{IN_STBY,\ ripple}$ = 100 Hz; I_{Q_STBY} = 5 mA; C_{Q_STBY} = 1 µF ceramic X7R;[1)]	P_4.4.67
Output capacitor	C_{Q_STBY}	0.47	–	2	µF	[1) 5)]	P_4.4.68
Output capacitor	ESR C_{Q_STBY}	–	–	0.5	Ω	at 10 kHz;[1)]	P_4.4.69
Device Enable Blocks and Quiescent Current							
Ignition turn on threshold	$V_{EN_IGN,\ on}$	–	–	4.0	V	Device operating	P_4.4.70

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Table 4 Electrical Characteristics, $V_{IN} = V_{IN_STBY}$ = 13.5 V, T_j = -40°C to +150°C, V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground. (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Ignition turn off threshold	$V_{EN_IGN, off}$	2.0	–	–	V	Only stand-by regulators are active if $V_{EN_IGN} < V_{EN_IGN, off}$ and $V_{EN_uC} < V_{EN_uC, off}$	P_4.4.71
Ignition pull-down resistor current	I_{EN_IGN}	-100	–	–	µA	V_{EN_IGN} = 13.5 V	P_4.4.72
Turn on threshold	$V_{EN_uC, on}$	–	–	2.0	V	Device operating	P_4.4.73
Turn off threshold	$V_{EN_uC, off}$	0.8	–	–	V	Only stand-by regulators are active if $V_{EN_IGN} < V_{EN_IGN, off}$ and $V_{EN_uC} < V_{EN_uC, off}$	P_4.4.74
Pull-down resistor current	I_{EN_uC}	-30	–	–	µA	V_{EN_uC} = 5 V	P_4.4.75
Quiescent current	$I_q = I_{IN_STBY} - I_{Q_STBY}$	-120	–	–	µA	$V_{EN_uC} = V_{EN_IGN}$ = 0 V; SEL_STBY = Q_STBY; MON_STBY = H; I_{Q_STBY} = 100 µA; T_j < 125 °C	P_4.4.76
Quiescent current	$I_q = I_{IN_STBY} - I_{Q_STBY}$	-130	–	–	µA	$V_{EN_uC} = V_{EN_IGN}$ = 0 V; SEL_STBY = GND; MON_STBY = H; I_{Q_STBY} = 100 µA; T_j < 125 °C	P_4.4.77
Quiescent current	$I_{q, IN}$	-10	–	–	µA	$V_{EN_uC} = V_{EN_IGN}$ = 0 V; V_{IN_STBY} = 0 V; T_j < 125 °C	P_4.4.78
Reset Generator RO_1 Monitoring Q_LDO1							
Undervoltage Reset threshold on Q_LDO1	$V_{URT\ Q_LDO1, de}$	4.50	–	4.75	V	V_{Q_LDO1} decreasing; V_{FB/L_IN} = open;	P_4.4.79
Undervoltage Reset threshold on Q_LDO1	$V_{URT\ Q_LDO1, in}$	4.55	–	4.90	V	V_{Q_LDO1} increasing	P_4.4.80
Undervoltage Reset hysteresis	$V_{URO_1, hyst}$	100	–	220	mV	–	P_4.4.81
Overvoltage Reset threshold on Q_LDO1	$V_{ORT\ Q_LDO1, in}$	5.40	–	5.65	V	V_{Q_LDO1} increasing	P_4.4.82
Overvoltage Reset threshold on Q_LDO1	$V_{ORT\ Q_LDO1, de}$	5.25	–	5.60	V	V_{Q_LDO1} decreasing	P_4.4.83
Overvoltage Reset hysteresis	$V_{ORO_1, hyst}$	80	–	180	mV	–	P_4.4.84
RO_1, Reset output low voltage	$V_{RO_1, low}$	–	–	0.4	V	I_{RO_1} = -10 mA; V_{Q_LDO1} > 2.5 V	P_4.4.85
RO_1, Reset output low voltage	$V_{RO_1, low}$	–	–	0.25	V	V_{IN_STBY} = 3.0 V; V_{Q_LDO1} = 2.5V; I_{RO_1} = -500 µA;	P_4.4.86

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Table 4 Electrical Characteristics, V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40°C to +150°C, V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground. (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
RO_1, Reset output leakage	$I_{RO_1, high}$	-1	–	1	µA	V_{RO_1} = 5.0 V	P_4.4.87
Reset delay time base	T_{cycle}	41.6	50	62.5	µs	C_{RT} = 1 nF	P_4.4.88
Reset timing capacitor range	C_{RT}	0.33	1.0	4.7	nF	–	P_4.4.89
Reset delay time RO_1	t_{RD, RO_1}	–	160	–	T_{cycle}	–	P_4.4.90
Undervoltage Reset reaction time	t_{UVRR, RO_1}	2	–	10	µs	Voltage step at Q_LDO1 from 5.00 V to 4.48 V	P_4.4.91
Overvoltage Reset reaction time	t_{OVRR, RO_1}	20	–	80	µs	Buck converter operating; Voltage step at Q_LDO1 from 5.00 V to 5.67 V	P_4.4.92
Reset Generator RO_2 Monitoring Q_LDO2 and FB_EXT							
Undervoltage Reset threshold on Q_LDO2	$V_{URT\ Q_LDO2, de}$	3.135	–	3.230	V	SEL_LDO2 = Q_LDO2; V_{Q_LDO2} decreasing; V_{IN_LDO2} = open	P_4.4.93
Undervoltage Reset headroom on Q_LDO2	$V_{URT\ Q_LDO2, head}$	55	117.5	–	mV	SEL_LDO2 = Q_LDO2; $V_{URT\ Q_LDO2, head}$ = V_{Q_LDO2} - $V_{URT\ Q_LDO2, de}$; V_{Q_LDO2} @ I_{Q_LDO2} = 500 mA	P_4.4.94
Undervoltage Reset hysteresis Q_LDO2	$V_{URO_2, hyst}$	15	–	55	mV	SEL_LDO2 = Q_LDO2; $V_{URO_2, hyst}$ = $V_{URT\ Q_LDO2, in}$ - $V_{URT\ Q_LDO2, de}$	P_4.4.95
Overvoltage Reset threshold on Q_LDO2	$V_{ORT\ Q_LDO2, in}$	3.70	–	3.85	V	SEL_LDO2 = Q_LDO2; V_{Q_LDO2} increasing	P_4.4.96
Overvoltage Reset threshold on Q_LDO2	$V_{ORT\ Q_LDO2, de}$	3.55	–	3.80	V	SEL_LDO2 = Q_LDO2; V_{Q_LDO2} decreasing	P_4.4.97
Overvoltage Reset hysteresis	$V_{ORO_2, hyst}$	50	–	200	mV	SEL_LDO2 = Q_LDO2;	P_4.4.98
Undervoltage Reset threshold on Q_LDO2	$V_{URT\ Q_LDO2, de}$	2.470	–	2.560	V	SEL_LDO2 = GND; V_{Q_LDO2} decreasing; V_{IN_LDO2} = open	P_4.4.99
Undervoltage Reset headroom on Q_LDO2	$V_{URT\ Q_LDO2, head}$	47	–	–	mV	SEL_LDO2 = GND; $V_{URT\ Q_LDO2, head}$ = V_{Q_LDO2} - $V_{URT\ Q_LDO2, de}$; V_{Q_LDO2} @ I_{Q_LDO2} = 500 mA	P_4.4.100
Undervoltage Reset hysteresis Q_LDO2	$V_{URO_2, hyst}$	15	–	60	mV	SEL_LDO2 = GND; $V_{URO_2, hyst}$ = $V_{URT\ Q_LDO2, in}$ - $V_{URT\ Q_LDO2, de}$	P_4.4.101
Overvoltage Reset threshold on Q_LDO2	$V_{ORT\ Q_LDO2, in}$	2.85	–	3.0	V	SEL_LDO2 = GND; V_{Q_LDO2} increasing	P_4.4.102

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Table 4 Electrical Characteristics, V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40°C to +150°C, V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground. (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overvoltage Reset threshold on Q_LDO2	$V_{ORT\ Q_LDO2,\ de}$	2.73	–	2.95	V	SEL_LDO2 = GND; V_{Q_LDO2} decreasing	P_4.4.103
Overvoltage Reset hysteresis Q_LDO2	$V_{ORO_2,\ hyst}$	50	–	120	mV	SEL_LDO2 = GND;	P_4.4.104
Undervoltage Reset threshold on FB_EXT	$V_{URT\ FB_EXT,\ de}$	1.425	–	1.480	V	TLE7368E V_{FB_EXT} decreasing; V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V	P_4.4.105
Undervoltage Reset headroom on FB_EXT	V_{FB_EXT} - $V_{URT\ FB_EXT,\ de}$	40	60	–	mV	TLE7368E V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V; V_{FB_EXT} @ I_{Q_LDO3} = 1 A	P_4.4.106
Undervoltage Reset hysteresis FB_EXT	$V_{URO_2,\ hyst}$	15	–	45	mV	TLE7368E	P_4.4.107
Overvoltage Reset threshold on FB_EXT	$V_{ORT\ FB_EXT,\ in}$	1.65	–	1.72	V	TLE7368E V_{FB_EXT} increasing	P_4.4.108
Overvoltage Reset threshold on FB_EXT	$V_{ORT\ FB_EXT,\ de}$	1.55	–	1.67	V	TLE7368E V_{FB_EXT} decreasing	P_4.4.109
Overvoltage Reset hysteresis FB_EXT	$V_{ORO_2,\ hyst}$	50	–	120	mV	TLE7368E	P_4.4.110
Undervoltage Reset threshold on FB_EXT	$V_{URT\ FB_EXT,\ de}$	1.08	–	1.15	V	TLE7368-2E V_{FB_EXT} decreasing; V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V;	P_4.4.111
Undervoltage Reset headroom on FB_EXT	V_{FB_EXT} - $V_{URT\ FB_EXT,\ de}$	40	60	–	mV	TLE7368-2E V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V;	P_4.4.112
Undervoltage Reset hysteresis	$V_{URO_2,\ hyst}$	15	–	45	mV	TLE7368-2E	P_4.4.113
Overvoltage Reset threshold on FB_EXT	$V_{ORT\ FB_EXT,\ in}$	1.30	–	1.39	V	TLE7368-2E V_{FB_EXT} increasing;	P_4.4.114
Overvoltage Reset threshold on FB_EXT	$V_{ORT\ FB_EXT,\ de}$	1.23	–	1.38	V	TLE7368-2E V_{FB_EXT} decreasing;	P_4.4.115
Overvoltage Reset hysteresis	$V_{ORO_2,\ hyst}$	10	–	70	mV	TLE7368-2E	P_4.4.116
Undervoltage Reset threshold on FB_EXT	$V_{URT\ FB_EXT,\ de}$	1.17	–	1.25	V	TLE7368-3E V_{FB_EXT} decreasing; V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V;	P_4.4.117

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Table 4 Electrical Characteristics, V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40°C to +150°C, V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground. (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Undervoltage Reset headroom on FB_EXT	V_{FB_EXT} - $V_{URT\ FB_EXT, de}$	40	60	–	mV	TLE7368-3E V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V;	P_4.4.118
Undervoltage Reset hysteresis	$V_{URO_2, hyst}$	15	–	45	mV	TLE7368-3E	P_4.4.119
Overvoltage Reset threshold on FB_EXT	$V_{ORT\ FB_EXT, in}$	1.35	–	1.43	V	TLE7368-3E V_{FB_EXT} increasing;	P_4.4.120
RO_2, Reset output low voltage	$V_{RO_2, low}$	–	–	0.4	V	I_{RO_2} = -10 mA; V_{Q_LDO2} > 2.0 V	P_4.4.121
RO_2, Reset output low voltage	$V_{RO_2, low}$	–	–	0.25	V	I_{RO_2} = -500 µA; V_{Q_LDO2} = 1V	P_4.4.122
RO_2, Reset output leakage	$I_{RO_2, high}$	-1	–	1	µA	V_{RO_2} = 5.0 V	P_4.4.123
Reset delay time RO_2	t_{RD, RO_2}	–	160	–	T_{cycle}	–	P_4.4.124
Undervoltage Reset reaction time	t_{UVRR, RO_2}	2	–	10	µs	Voltage step on Q_LDO2 from $V_{Q_LDO2, nom}$ to $V_{URT\ Q_LDO2, de, min}$ - 20 mV	P_4.4.125
Undervoltage Reset reaction time	t_{UVRR, RO_2}	2	–	10	µs	Voltage step on FB_EXT from $V_{FB_EXT, nom}$ to $V_{URT\ FB_EXT, de, min}$ - 20 mV	P_4.4.126
Overvoltage Reset reaction time	t_{OVRR, RO_2}	20	–	80	µs	Buck converter operating; Voltage step on Q_LDO2 from $V_{Q_LDO2, nom}$ to $V_{ORT\ Q_LDO2, in, max}$ + 20 mV	P_4.4.127
Overvoltage Reset reaction time	t_{OVRR, RO_2}	20	–	80	µs	Buck converter operating; Voltage step on FB_EXT from $V_{FB_EXT, nom}$ to $V_{ORT\ FB_EXT, in, max}$ + 20 mV	P_4.4.128

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Table 4 Electrical Characteristics, $V_{IN} = V_{IN_STBY} = 13.5$ V, T_j = -40°C to +150°C, $V_{CCP} = 9.0$ V; SEL_STBY = Q_STBY; all voltages with respect to ground. (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Monitoring Block							
MON_STBY, Threshold on Q_STBY	$V_{MON, Q_STBY, de}$	0.90	–	–	V	V_{IN_STBY} = 3.0 V; SEL_STBY = Q_STBY; V_{Q_STBY} decreasing;	P_4.4.129
MON_STBY headroom	$V_{MON, Q_STBY, head}$	10	–	–	mV	V_{IN_STBY} = 3.0 V; SEL_STBY = Q_STBY; V_{Q_STBY} decreasing;	P_4.4.129a
MON_STBY hysteresis	$V_{MON_STBY, hyst}$	10	–	30	mV	SEL_STBY = Q_STBY	P_4.4.130
MON_STBY, Threshold on Q_STBY	$V_{MON, Q_STBY, de}$	2.36	–	2.50	V	V_{IN_STBY} = 3.0 V; SEL_STBY = GND; V_{Q_STBY} decreasing;	P_4.4.131
MON_STBY hysteresis	$V_{MON_STBY, hyst}$	20	–	50	mV	SEL_STBY = GND	P_4.4.132
MON_STBY, Monitoring output low voltage	$V_{MON_STBY, low}$	–	–	0.4	V	I_{MON_STBY1} < 10 mA; V_{IN_STBY} > 3.0 V	P_4.4.133
MON_STBY time delay	t_{MON_STBY}	–	8	–	t_{RD, RO_1}	see diagram in section **"Monitoring Circuit" on Page 30**	P_4.4.134
Monitor reaction time	t_{RR, MON_STBY}	3	–	6	µs	–	P_4.4.135

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Table 4 Electrical Characteristics, V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40°C to +150°C, V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground. (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Window Watchdog							
H-input voltage threshold	$V_{WDI, high}$	–	–	2.0	V	–	P_4.4.136
L-input voltage threshold	$V_{WDI, low}$	0.8	–	–	V	–	P_4.4.137
WDI pull-up resistor	R_{WDI}	60	100	140	kΩ	connected to Q_LDO2	P_4.4.138
Watchdog cycle time	T_{WD}	–	2	–	T_{cycle}	–	P_4.4.139
Window duration (OW, CW, FW)	$t_{WD, W}$	–	512	–	T_{WD}	–	P_4.4.140
Window duration (IW)	$t_{WD, IW}$	–	32	–	T_{WD}	–	P_4.4.141
Window watchdog initialization time	$t_{WD, start}$	–	32	–	T_{WD}	Watchdog will start/initialized if WDI is kept low for this period and RO_2 is released	P_4.4.142
Watchdog output low voltage	$V_{WDO,low}$	–	–	0.4	V	I_{WDO} = 2 mA	P_4.4.143
Watchdog output leakage current	$I_{WDO,leak}$	–	–	1	µA	WDO state = High	P_4.4.144
Thermal Shutdown							
Overtemperature shutdown	$T_{j, shtdwn}$	160	175	190	°C	1) 8)	P_4.4.145
Overtemperature shutdown hysteresis	ΔT	15	–	30	K	1)	P_4.4.146

1) Specified by design, not subject to production test.
2) Tested according to measurement figure 10, application diagram
3) V_{CCP} supplied externally with a voltage according to the actual value of V_{CCP} measurement.
4) $V_{dr, Q_LDO1} = V_{FB/L_IN} - V_{Q_LDO1}$; $V_{dr, Q_LDO2} = V_{IN_LDO2} - V_{Q_LDO2}$; $V_{dr, T<1, 2>} = V_{FB/L_IN} - V_{Q_T<1, 2>}$
5) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.
6) Measured when V_{Q_LDO2} has dropped 100 mV from its nominal value obtained at V_{IN_LDO2} = 5.4 V.
7) External power transistor type: Fairchild KSH200.
8) Permanent operation of the device above 150 °C degrades lifetime; please refer to quality information.

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5 Detailed Internal Circuits Description

In the following the main circuit blocks of the TLE7368, namely the Buck converter, the linear regulators, the trackers, the charge pump, the enable and reset circuits and the watchdog are described in more detail.

5.1 Buck Regulator

The TLE7368's DC to DC converter features all the functions necessary to implement a high efficient, low emission Buck regulator with minimum external components. The step down regulator in the TLE7368 follows a concept similar to the one of its predecessor, TLE6368, which allows operation over a battery voltage range from as low as 4.5 V up to a maximum of 45 V at peak currents of 2.5 A at minimum. **Figure 3** shows the block diagram of the converter with its major components, i.e. the internal DMOS power stages, the high side driver including its supply scheme, the power stage slope control circuit for reduced EME, the current mode control scheme and various protection circuits for safe converter operation.

5.1.1 Buck Regulator Control Scheme

The step down converter's control method is based upon the current mode control scheme. Current mode control provides an inherent line feed forward, cycle by cycle current limiting and ease of loop compensation. No external compensation components are needed to stabilize the loop, i.e. the operation of the Buck converter. The slope compensation circuit in addition to the current sense amplifier and the error amplifier prevents instabilities/sub harmonic oscillations at duty cycles higher than 0.5. The cycle by cycle current limiting feature supports also a soft start feature during power up. Additional implemented current blanking prevents faulty DMOS turn off signals during switching operation.

5.1.2 High Side Driver Supply and 100% Duty Cycle Operation

The supply concept of the Buck converter's power stage driver follows the Bootstrapping principle. A small external capacitor, placed between pins SW and BST, is used to provide the necessary charge at the gate of the power stage. The capacitor is refreshed at each switching cycle while the power stage is turned off resulting in the ability to power the gate at the next turn on of the power stage.

In cases where the input/battery voltage approaches the nominal Buck converter output voltage, the duty cycle of the converter increases. At the point where the power stage is statically turned on (100% duty cycle) a refresh of the Bootstrap capacitor as described above is not possible. In this case the charge pump helps to accomplish the gate over drive in order to keep the power stage turned on with low R_{dson}. With decreasing input voltage, shortly before switching to 100% duty cycle, the device operates in pulse skipping mode. In this mode the device appears to be operating at much lower frequencies with very small duty cycles. In real, the device is doing a few 100% duty cycle periods followed by a period with a duty cycle smaller than 1.

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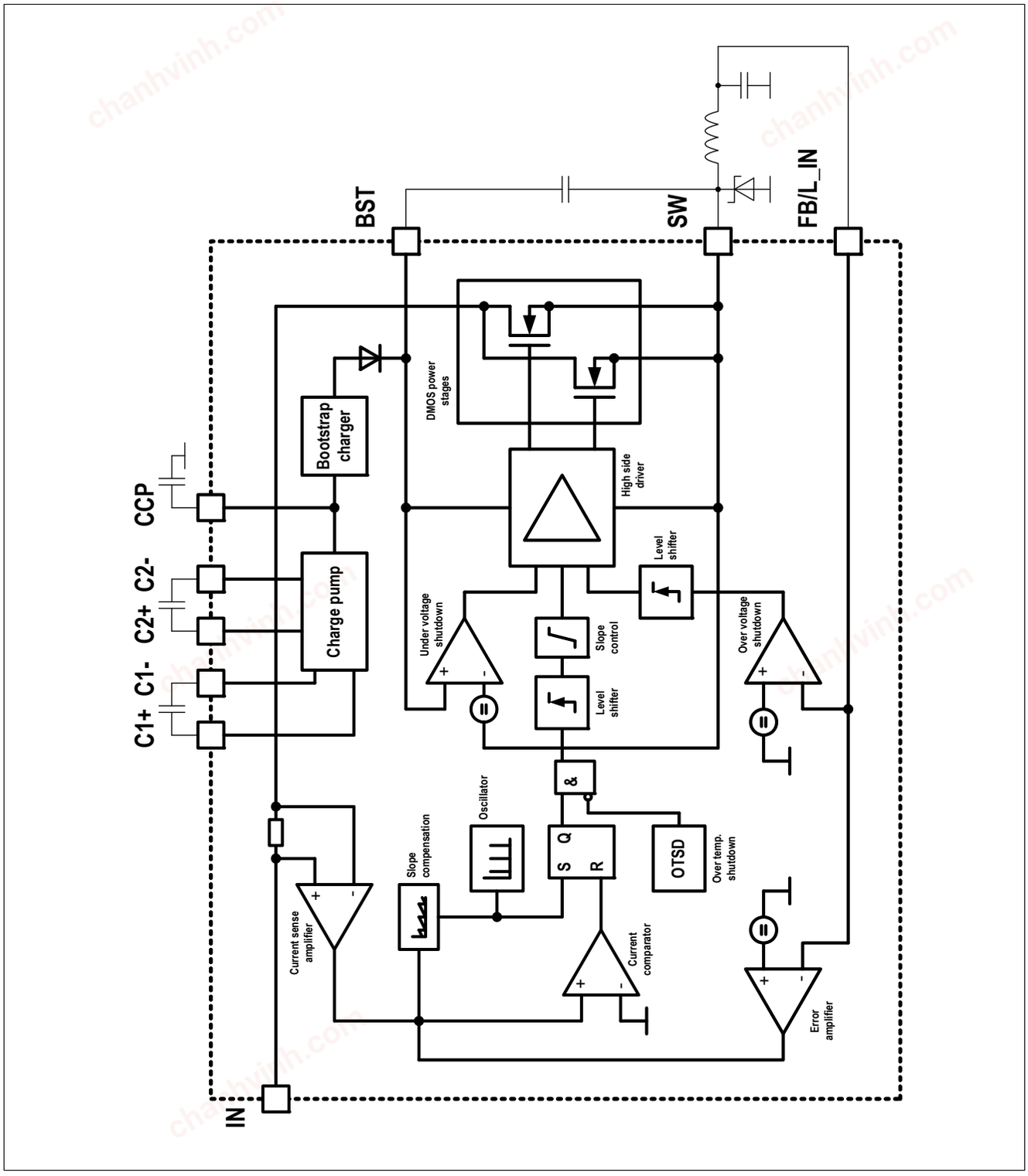


Figure 3 Buck Converter Block Diagram

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5.1.3 Electromagnetic Emission Reduction

The Buck DMOS power stage is implemented as multiple cells. This allows to control the slope of the power stage's current at turn on/off by sequentially turning on/off the cells, achieving a smooth turn on/off and therefore avoiding high frequency components in the electromagnetic emissions to the battery line. The current slope control is adjusted internally, the typical current slew rate is 50 ns/A.

5.1.4 Charge Pump

The charge pump serves as support circuit for the Buck converter's high side driver supply, the linear regulators drive circuits for low drop operation and the internal device biasing blocks. In order to guarantee full device operation at battery voltages as allow as even 4.5 V, the concept of a voltage tripler is chosen for the charge pump. It operates at a switching frequency of typical 2 MHz utilizing three small external capacitors, two pumping caps and one storage capacitor. The CCP circuit is equipped with a current limit function which avoids destruction in case of a short of one of the external CCP capacitors. The charge pump's output, CCP, is designed to supply the circuitry described above, it should not be used as e.g. driver rail for external on board/PCB circuits.

5.1.5 Buck Converter Protection Circuits

Besides the circuits mandatory for the Buck converter operation additional protection circuits are foreseen which help preventing false operation of the device. Undervoltage lockouts are foreseen at the battery input line[1)] and the high side driver supply rail to ensure the device operates only with proper voltages present. The overvoltage shutdown at the Buck converter output provides a safe high side shutdown for the case where the Buck control loop becomes messed up due to non predictable circumstances. At overtemperatures the thermal shutdown circuit disables the Buck converter until the device cools down to be enabled again.

5.2 Linear Regulators

The TLE7368 features three linear voltage regulator circuits, two fully integrated DMOS low drop voltage regulators and one integrated linear control circuit to operate with an external NPN power stage.

Integrated linear regulator one (LDO1) offers a 5 V output and the second integrated linear regulator (LDO2) can be configured with pin SEL_LDO2 either for 2.6 V or for 3.3 V. With SEL_LDO2 tied to GND 2.6 V will adjust at the output of LDO2, SEL_LDO2 being connected to Q_LDO2 gives the 3.3 V option. The external regulator will adjust its output to 1.5 V or 1.2 V or 1.3 V (depending on variant of TLE7368) with the emitter of the NPN power stage directly connected to pin FB_EXT, by using a voltage divider, higher output voltages can be achieved.

The regulators are designed for low drop operation and offer high output voltage accuracies to meet the needs of current and next generation 32-bit microcontroller families. Additionally all regulators feature a short circuit protection, i.e. the integrated regulators contain a output current limit function whereas the control circuit for the external NPN power stage limits the maximum base current.

For low on chip power dissipation the input of LDO1 is internally directly connected to the Buck converter output (FB/L_IN). LDO2's input is on purpose externally accessible at IN_LDO2. This allows the insertion of a drop element between the Buck converter output and IN_LDO2 to split the power dissipation and avoid high losses on the TLE7368. Similar for the external NPN power stage regulator, the collector of the NPN can be either connected directly to the Buck converter output or a drop element can be inserted in between to split power dissipation.

1) Not shown in the schematic, **Figure 3**.

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5.3 Voltage Tracking Regulators

For off board/off PCB supplies, i.e. sensors, two voltage tracking regulators are incorporated in the TLE7368. Their outputs follow the output of the main 5 V regulator, Q_LDO1, within a tight tolerance of ±10 mV. The tracking regulators are implemented with bipolar PNP power stages for improved ripple rejection to reduce emission when lead off board. Both tracker outputs can withstand short circuits to GND and battery in a range of -5 V to +40 V. When shorted to lower levels than the nominal output voltage level the current limit function prevents excessive current draw.

5.4 Power Up and Power Down Sequencing

In a supply system with multiple outputs the sequence of enabling the individual regulators is important. Especially 32-bit microcontrollers require a defined power up and power down sequencing. **Figure 4** shows the details for the power up and power down sequence of the TLE7368.

At power up, the first circuit block to be enabled is the charge pump as it is mandatory for the other circuits to operate. With the charge pump reaching its nominal value, the Buck converter starts to power up its output. Also the output voltage the linear regulators are enabled. The three linear regulators power up simultaneously. The 5 V regulator acts as the master, the 3.3 V/2.6 V regulator and the 1.5 V regulator follow. As the 5 V regulator powers up also the tracking regulators follow. The ramp if the increasing output voltage of each line is determined by the connected output capacitance, the load current and the current limit of the regulator under consideration. In addition an integrated supervision circuit ensures the following two conditions during power-up:

$$-0.3\ V < (V_{Q_LDO1} - V_{Q_LDO2}) < 3.1\ V \text{ and} \quad (5.1)$$

$$-0.3\ V < (V_{Q_LDO2} - V_{FB_EXT}) \quad (5.2)$$

The power down sequence is practically vice versa to the start up procedure. With the battery decreasing to zero the charge pump and Buck regulator will stop to operate at the minimum battery threshold, the Buck output voltage will fall down and so will the outputs of the linear regulators.

In the event where the device is disabled, EN_IGN = low and EN_uC = low, the charge pump, the Buck converter and the linear regulators are disabled immediately.

The linear regulators' outputs are not discharged actively in any case of power down. Diode circuitry (i.e. Schottky diodes) might be necessary to avoid violation of certain microcontrollers' sequencing requirements.

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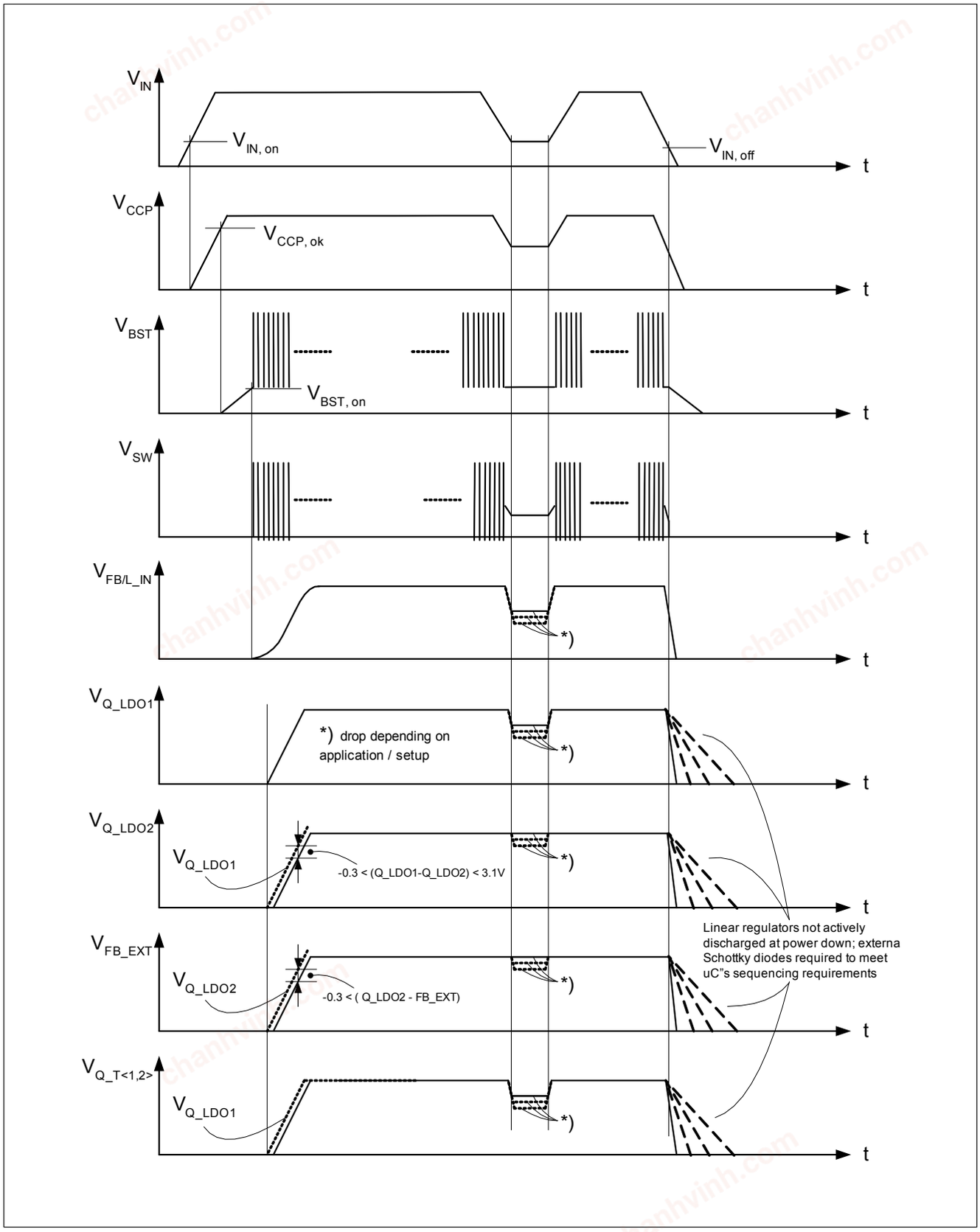


Figure 4 Power Sequencing of the TLE7368

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5.5 Stand-by Regulator

The intention of the stand-by or keep alive regulator is to supply e.g. external memory even with the main microcontroller supply being disabled. Therefore the state of the stand-by regulator is not controlled by the enable block, but it is active all the time. The stand-by regulator starts to operate as soon as the battery voltage increases above its operating threshold. The current consumption during single operation of the stand-by regulator is reduced to a minimum. It can be configured for output voltages as either 1.0 V or 2.6 V through the SEL_STBY pin.

5.6 Overtemperature Protection

At junction temperatures between 160 °C and 190 °C, which can be caused by e.g. excessive power dissipation or increased ambient temperatures, the overtemperature protection kicks in and disables the Buck converter. With the Buck converter disabled the linear regulators will most likely not be able to keep up their output voltage and a system reset can be expected. Due to the drop in power dissipation the junction temperature will decrease. The built in hysteresis circuit ensures that the junction temperature cools down by a certain temperature delta before the Buck converter is enabled again.

5.7 Device Enable Function

The device enable block controls the operation of the Buck converter as well as of the linear regulators and tracker blocks. Two external signal inputs determine the state of those blocks, a high voltage input EN_IGN and a low voltage input EN_uC. Internally the two signals are logic OR-ed which means that with either signal the Buck and linear regulators can be turned on or held active, provided that the battery voltage is above its minimum operating range. In order to turn off the regulator blocks, the signals on both inputs, EN_IGN and EN_uC must be lower than their deactivating threshold. The stand-by regulator's operation is not affected by the device enable block.

5.8 Reset Function

The Reset concept of the TLE7368 is chosen to support multiple microcontroller platforms. Two open drain outputs, i.e. the Reset outputs, RO_1 and RO_2, indicate the states of the different regulators. **Figure 5** gives the details on the Reset timing. RO_1 is tied to LDO1 and will indicate whenever its output, Q_LDO1, is crossing the under- or overvoltage threshold. The second Reset output, RO_2, turns low whenever one of the two outputs, Q_LDO2 or FB_EXT, are crossing their under- and overvoltage thresholds. At power up in order to avoid a faulty microcontroller start, a so called Reset delay function, i.e. the Reset release delay, is implemented. This delay until the reset is released, counted from the time where the regulator outputs cross the threshold, is determined by a small external delay capacitor at pin RT.

The power up reset delay time t_{RD} is directly proportional to the capacitance C_{RT} within the capacitance range of 0.33 nF … 4.7 nF:

$$t_{RD} = 160 \times 50\ \mu s \times C_{RT}/nF \quad (5.3)$$

For the tolerance calculation please refer to the parameters **P_4.4.81**, **P_4.4.82** and **P_4.4.83**. In order to find the worst case limits of t_{RD} the capacitance tolerance should be taken into account.

The Reset generators within the TLE7368 are supplied from multiple sources, VIN_STBY, VCCP, VFB_L/IN, VQ_LDO1 and VQ_LDO2, to fulfill next generation microcontroller requirements during power up and power down.

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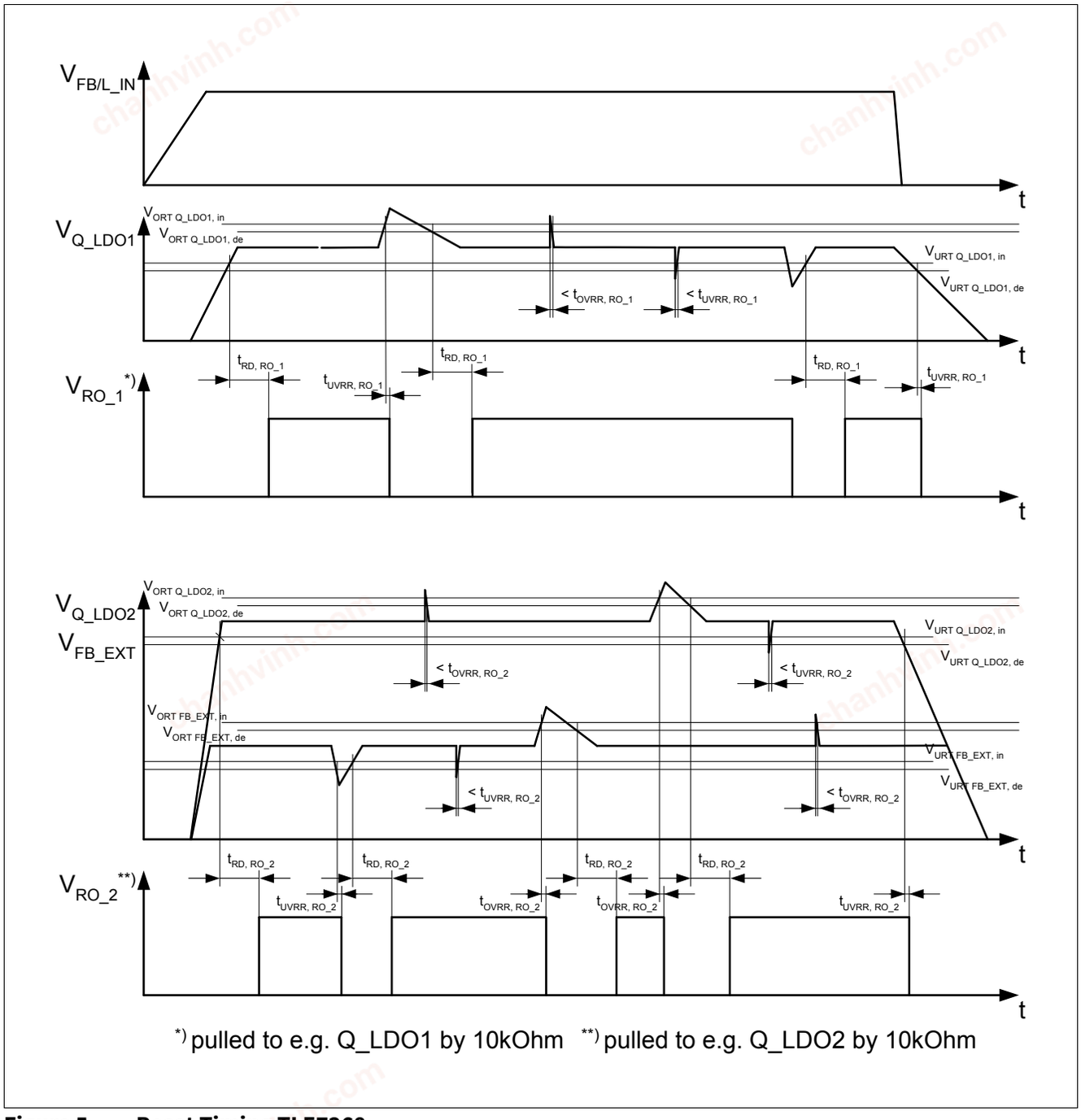


Figure 5 Reset Timing TLE7368

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5.9 Monitoring Circuit

The monitoring block within the TLE7368 detects an undervoltage at the stand-by regulator output and is able to distinguish between two different undervoltage situations. When the stand-by output gets back into regulation after an undervoltage event, the timing on the MON_STBY output signal indicates the kind of undervoltage scenario which has happened before. The behavior of the monitoring block is also described in **Figure 6** and **Figure 7** below.

In case of an undervoltage at the stand-by regulator with the 5 V regulator LDO1 in regulation (which means that RO_1 = HIGH) the monitoring circuit has basically a power fail functionality which means that the MON_STBY output will be LOW just as long as the undervoltage at the stand-by output occurs. As soon as Q_STBY is coming back into regulation MON_STBY turns high again.

When the 5 V regulator is out of regulation (RO_1 = LOW), e.g. in case of EN_uC = EN_IGN = LOW, the MON_STBY will turn LOW again if an undervoltage event happens at Q_STBY. The difference to the scenario described above is now that when Q_STBY gets back into regulation the toggling of the MON_STBY output to HIGH is coupled with the 5 V Reset line, RO_1, turning HIGH. In detail, the MON_STBY line turns high delayed by t_{MON_STBY} after the Reset line RO_1 had gone high.

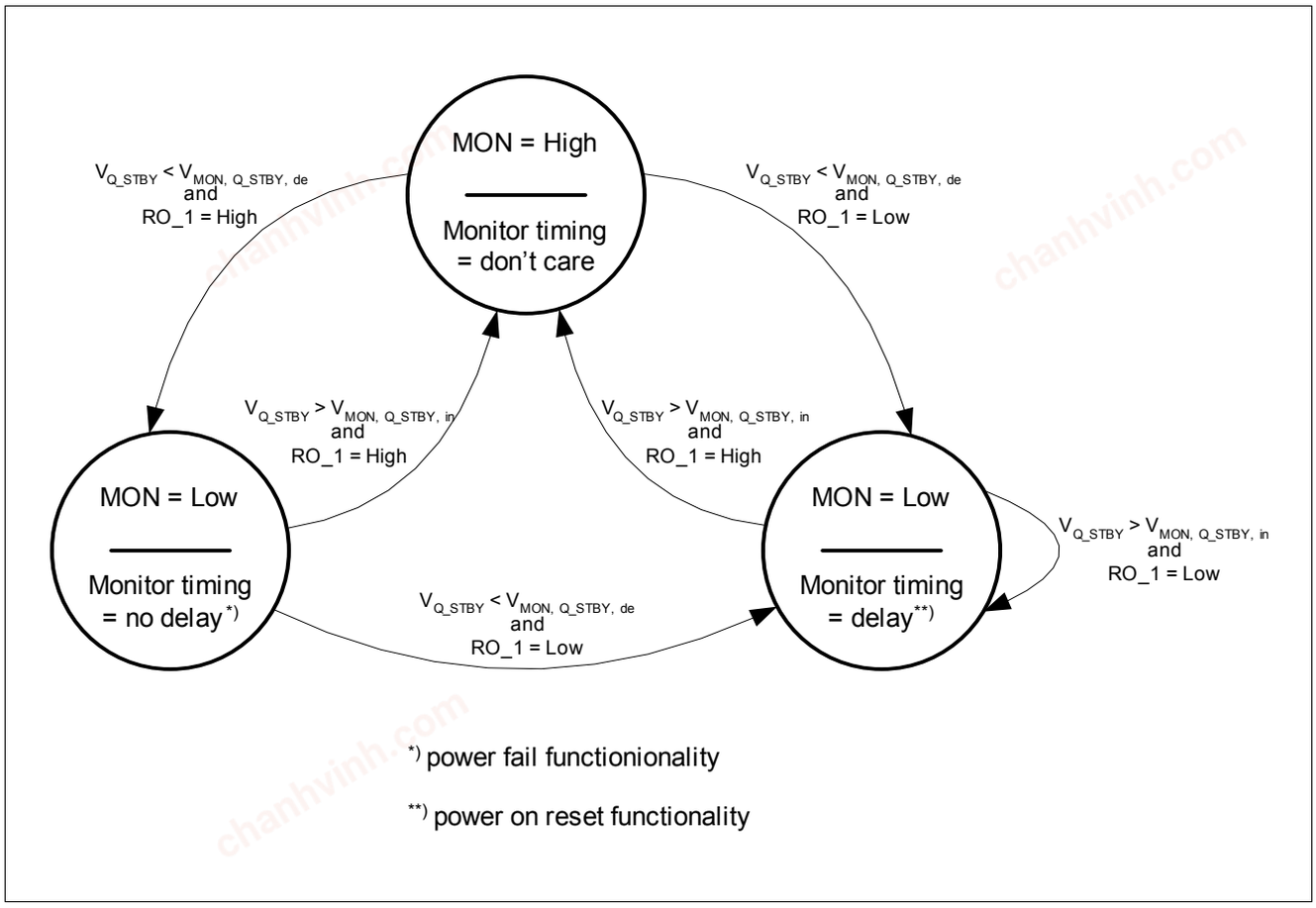


Figure 6 Stand by Monitor State Diagram

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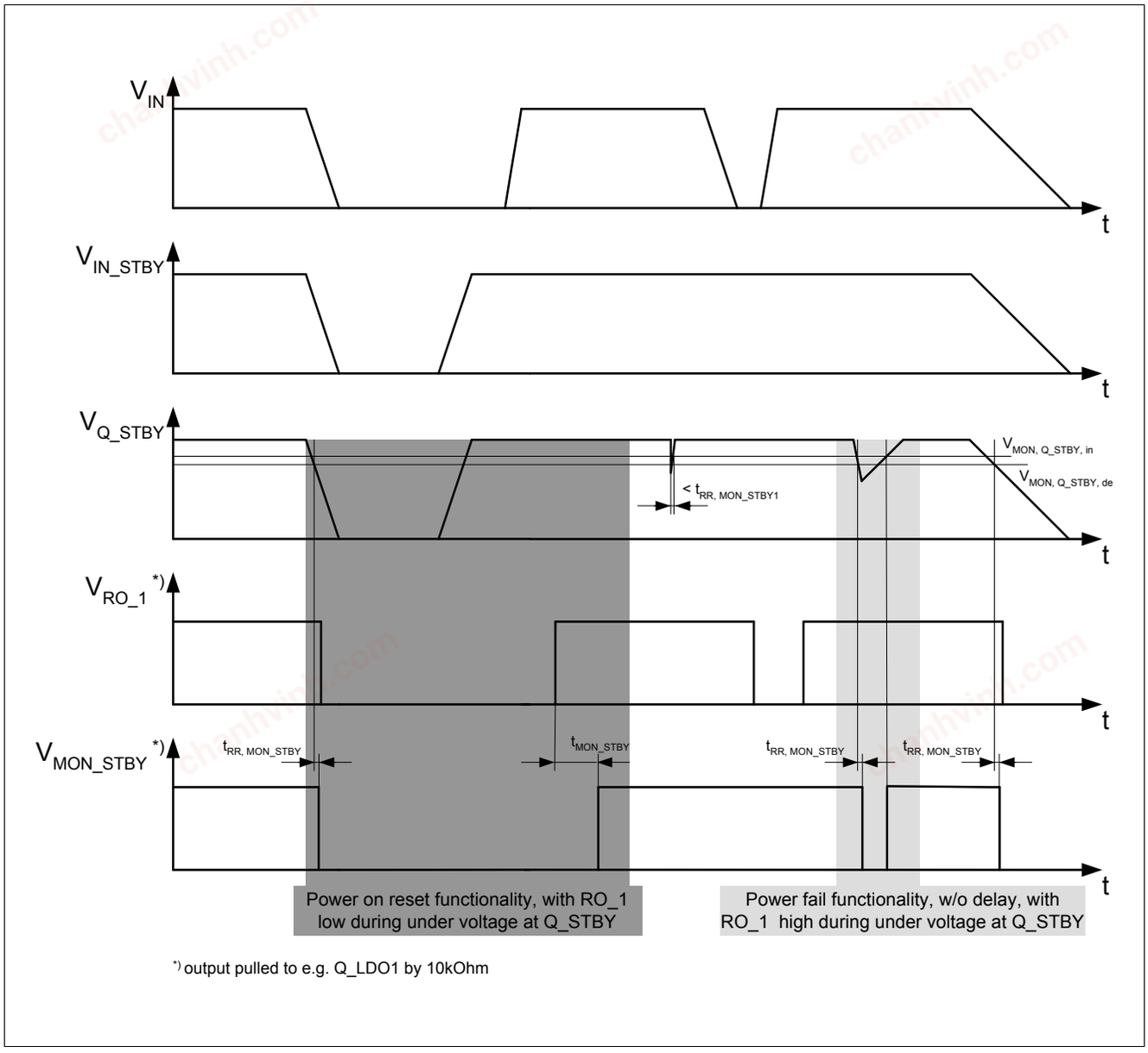


Figure 7 Stand by Monitor Timing Diagram

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5.10 Watchdog Circuit

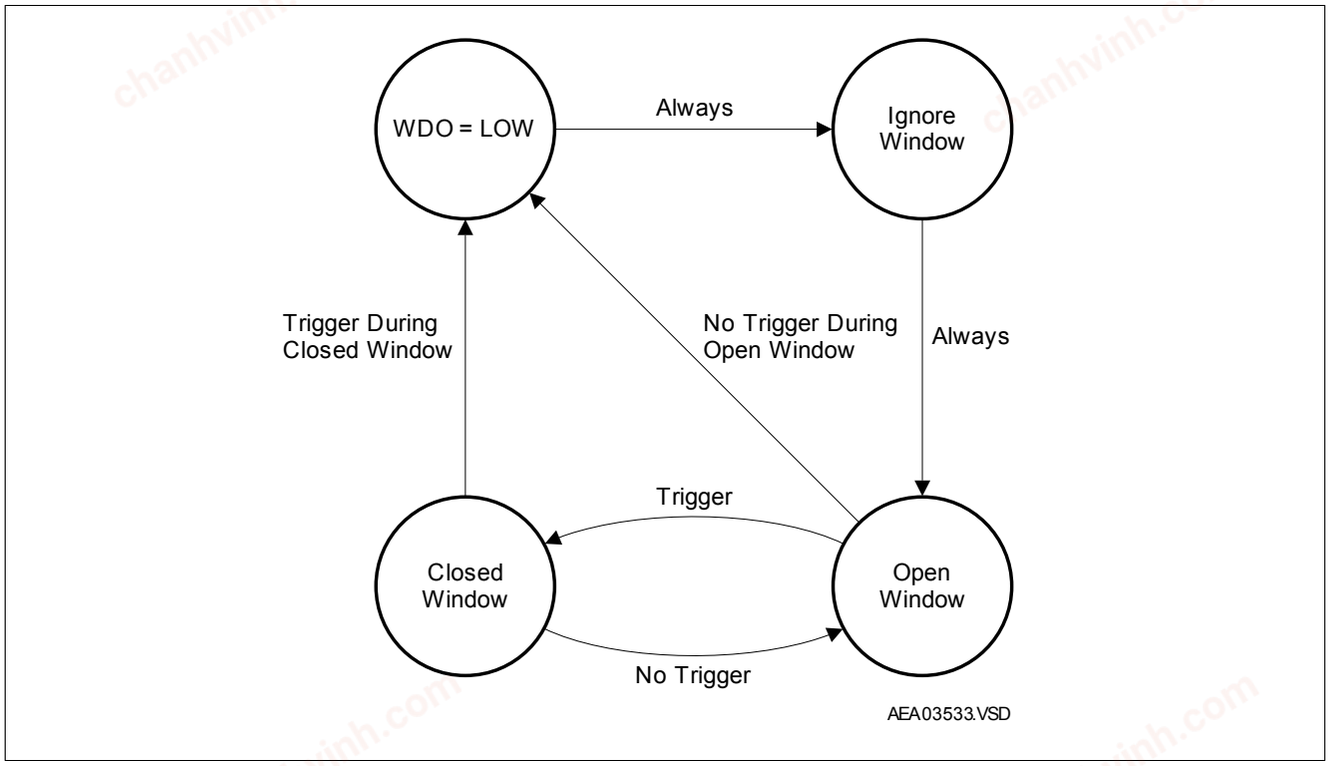


Figure 8 Window Watchdog State Diagram

Principle of Operation:

A Window Watchdog is integrated in the TLE7368 to monitor a microcontroller. The Window Watchdog duty cycle consists of an "Open window" and a "Closed window". The microcontroller that is being monitored has to send a periodic falling edge trigger signal to the watchdog input pin WDI within the "Open Window". If a trigger signal is not sent or if it is sent during the "Closed Window", then Watchdog Output (WDO) switches from high to low signaling a potential microcontroller fault has occurred. The watchdog cycle time T_{WD} is derived from the time base T_{Cycle}. An external capacitor connected between pins RT and GND determines T_{Cycle}.

Initialization:

The Watchdog is switched off per default and activated by pulling WDI to low at least for the time $t_{WD,start}$ after RO_2 has turned to high. Watchdog input pin WDI has an integrated pull-up resistor R_{WDI} connected to Q_LDO2. If WDI transitions to high before $t_{WD,start}$ has elapsed, then the watchdog will not start operation. To initialize the Watchdog the watchdog input WDI should transition to high within the "Ignore Window". The WDI signal may also transition to high during the following "Open Window", but sufficient time must be left for a falling edge transition before the end of the "Open Window". The watchdog function is turned off following a RO_2 reset, and must be reinitialized to be turned back on.

Normal Operation:

Please refer to **Figure 8**.

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Detailed Internal Circuits Description

The Watchdog starts operating in the "Ignore Window" state for a duration of $t_{WD,IW}$. Within the "Ignore Window" the microcontroller is given time to initialize. Any signal to watchdog input WDI within the "Ignore Window" is ignored. After time $t_{WD,IW}$, the watchdog transitions from the "Ignore Window" state to the "Open Window" state for a maximum duration of $t_{WD,W}$. Within the "Open Window" a valid trigger signal must be applied to the watchdog input WDI. A valid trigger signal is a falling edge from $V_{WDI,high}$ to $V_{WDI,low}$. After receiving a valid trigger signal within the "Open Window" the watchdog immediately terminates the "Open Window" and enters the "Closed Window" state. The "Closed Window" has a fixed duration $t_{WD,W}$. During normal operation a trigger signal should not be applied during the "Closed Window. After the "Closed Window" time $t_{WD,W}$ an the watchdog returns back to the "Open Window" state. Within the "Open Window", a valid trigger signal must be applied to the watchdog input WDI. In normal operation, the watchdog continues to cycle between the "Open Window" and "Closed Window" state. If reset signal RO_2 is asserted and transitions to a low state, then the watchdog needs to be reinitialized as described in the Initialization section. The watchdog output WDO stays high as long as the watchdog input WDI is triggered correctly.

Valid Trigger Signal:

Please refer to **Figure 9**.

Watchdog input WDI is periodically sampled with a period of T_{WD}. A valid trigger signal is a falling edge from $V_{WDI,high}$ to $V_{WDI,low}$. To improve immunity against noise or glitches on the WDI input, at least two high samples followed two low samples are required for a valid trigger signal. For example, if the first three samples (two HGH one LOW) of the trigger pulse at pin WDI are inside the closed window and only the fourth sample (the second LOW sample) is taken in the open window then the watchdog output WDO will remain High.

Invalid Triggering:

Please refer to **Figure 8** and **Figure 9**.

No trigger signal detected during the "Open Window" or a trigger signal detected during the "Closed Window", is considered invalid triggering. Watchdog output WDO switches to low for a duration of $t_{WD,W}$ immediately after no valid trigger during the "Open Window" or immediately if a trigger signal is detected during the "Closed Window".

Fault Operation:

If a capacitor failure on the watchdog timing pin RT causes a short circuit to GND during normal operation, there is no dedicated fault operation. The WDO, RO_1 and RO_2 pins keep their current status. At the following start up procedure, the RO_1 and RO_2 signals remain low without being released. An open circuit at pin RT causes WDO to switch from high to low.

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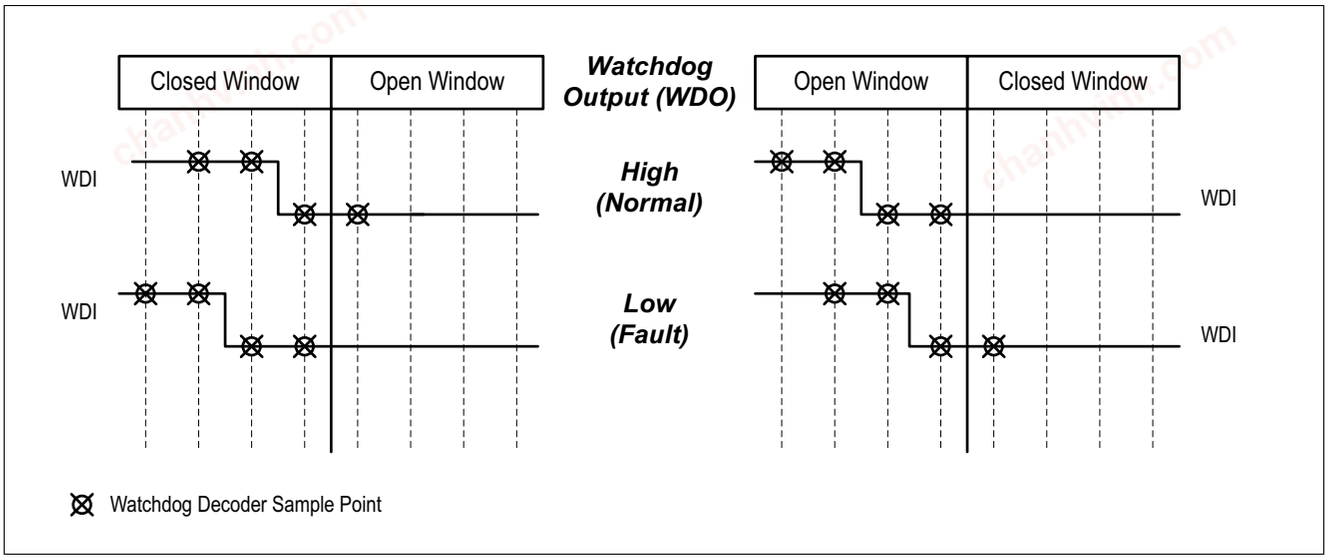


Figure 9 Window Watchdog Input Signal Validation

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6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

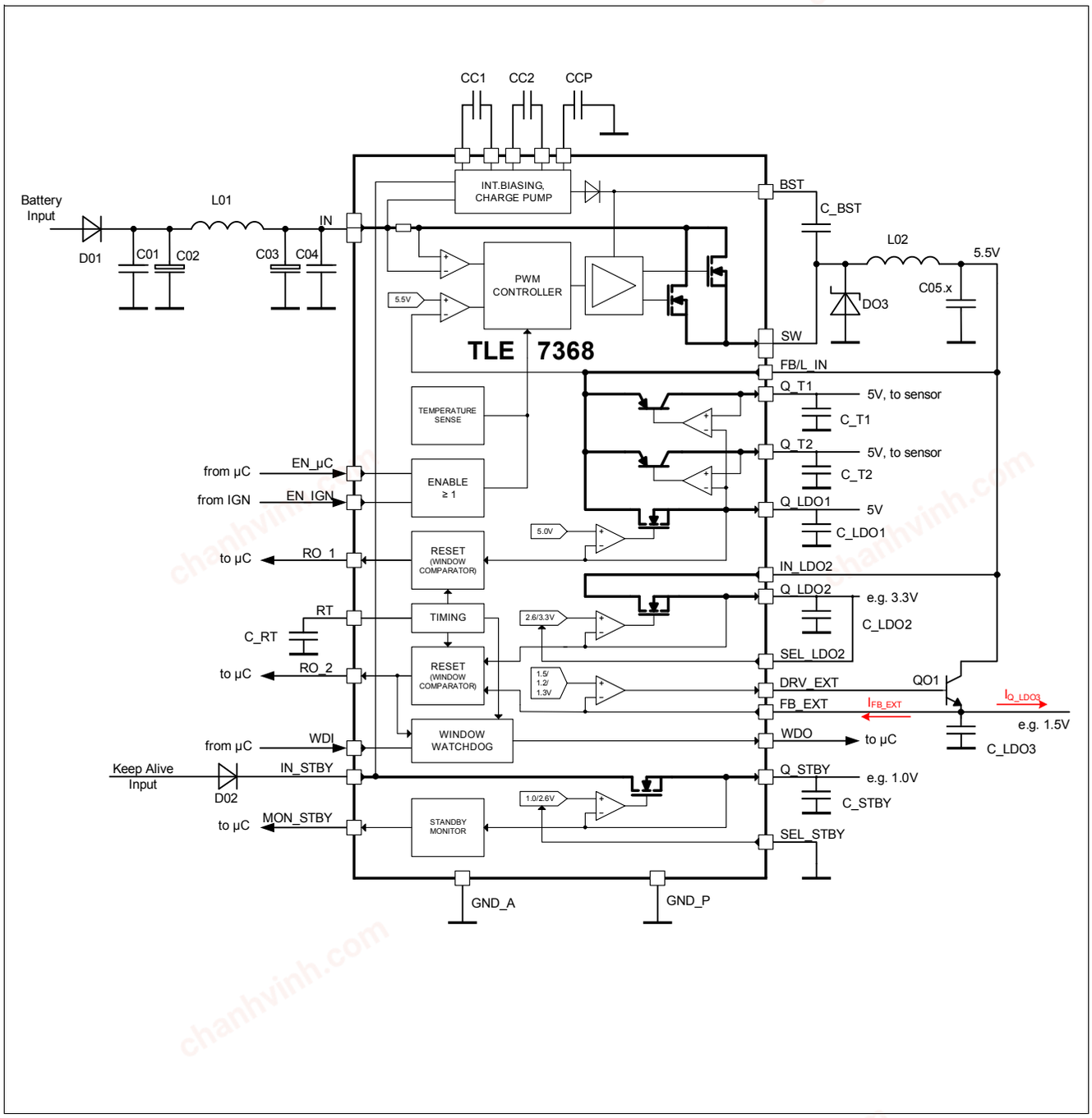


Figure 10 Application Diagram, Example

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

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	Value	Type	Remarks
C01	0.1 µF/50V	Ceramic capacitor	
C02	10 µF/50V	Electrolitic capacitor	
C03	47 µF/50V	Electrolitic capacitor	
C04	0.1 µF/50V	Ceramic capacitor	
C05.x	5 x 4.7 µF/16V (in parallell)	Ceramic capacitor	C3216X7R1E475K160AC - TDK
CC1	0.1 µF/16V	Ceramic capacitor	
CC2	0.1 µF/16V	Ceramic capacitor	
CCP	0.22 µF/25V	Ceramic capacitor	
C_RT	1 nF/10V	Ceramic capacitor	
C_BST	0.1 µF/10V	Ceramic capacitor	
C_LDO1	1 µF/10V	Ceramic capacitor	C2012X7R1E105K125AB - TDK
C_LDO2	1 µF/10V	Ceramic capacitor	C2012X7R1E105K125AB - TDK
C_LDO3	22 µF/10V	Tantalum capacitor	Ceramic capacitor also possible
C_STBY	1 µF/10V	Ceramic capacitor	C2012X7R1E105K125AB - TDK
D01	100V 12A, 3-Pin PowerDI 5	Schottky diode	SMT
D02	MMBD914LT1G	Diode	Onsemi
D03	100V 12A, 3-Pin PowerDI 5	Schottky diode	SMT
L01	10 µH/2.1 A	Inductor	Coilcraft
L02	33 µH/2.1 A	Inductor	Coilcraft
Q01	KSH200TF	NPN Bipolar transistor	Fairchild

Figure 11 Application Diagram, Bill of Material

This section intends to give hints for correct set up of the IC, i.e. to avoid misbehavior caused by the influence of other PCB board circuits and shows also how to calculate external components, power loss, etc.

6.1 Choosing Components for the Buck Regulator

Stable operation of the Buck converter is ensured when choosing the external passive components according to the characteristics given below:

- Buck inductance: 18 µH < L_{Buck} < 220 µH
- Buck output capacitor: C_{Buck} > 20 µF
- ESR of Buck output capacitor: ESR_C_{Buck} < 150 mΩ

6.2 Setting up LDO1, LDO2

The linear regulators LDO1 and LDO2 need to be connected to appropriate output capacitors in order to keep the regulation loop stable and avoid oscillations. The essential parameters of the output capacitor are the minimum capacitance and the equivalent series resistance (ESR). The required ranges for each output are specified in **Chapter 4.4** (**Electrical Characteristics**). Tantalum capacitors as well as multi layer ceramic capacitors are suitable for LDO1 and LDO2.

Table 5 LDO2 Output Voltage Configuration

No.	SEL_LDO2	Q_LDO2
1	GND	2.6 V
2	Q_LDO2	3.3 V

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6.3 Setting up of LDO3

LDO3 consists of an integrated regulator which needs to be equipped with an external power transistor (NPN-Type). The most important parameters to be checked when choosing the external transistor are the ‘current gain bandwidth product’ (f_T), the ‘DC current gain’ (h_{FE}) and the thermal resistance of the package. Darlington type transistors should not be used. For stability of the regulation loop a multi layer ceramic capacitor of min. 4.7 µF must be connected to the LDO3 output voltage (Emitter of the external power transistor). In order to improve suppression load current steps an additional capacitor of tantalum type can be connected in parallel.

In case LDO3 voltage is not needed the external NPN transistor can be spared. For this configuration the pins ‘DRV_EXT’ and ‘FB_EXT’ should be directly connected to each other in order to ensure correct operation of Reset 2. Also in this case a small ceramic capacitor of 220 nF connected from pin ‘FB_EXT’ to GND is recommended in order to avoid oscillations of the regulation loop LDO3.

6.4 Setting up the Stand-by Regulator

The stand by regulator provides an output current up to 30 mA sourced via linear regulation directly from Battery even when the main regulator is disabled. This low quiescent current regulator is commonly used as supply for stand by memory. The output voltage can be selected as 1.0 V or 2.6 V. For stability of the regulation loop the output Q_STBY should be connected via a ceramic capacitor (470 nF to 2 µF) to GND.

6.4.1 Stand-by Regulator’s Output Voltage Configuration

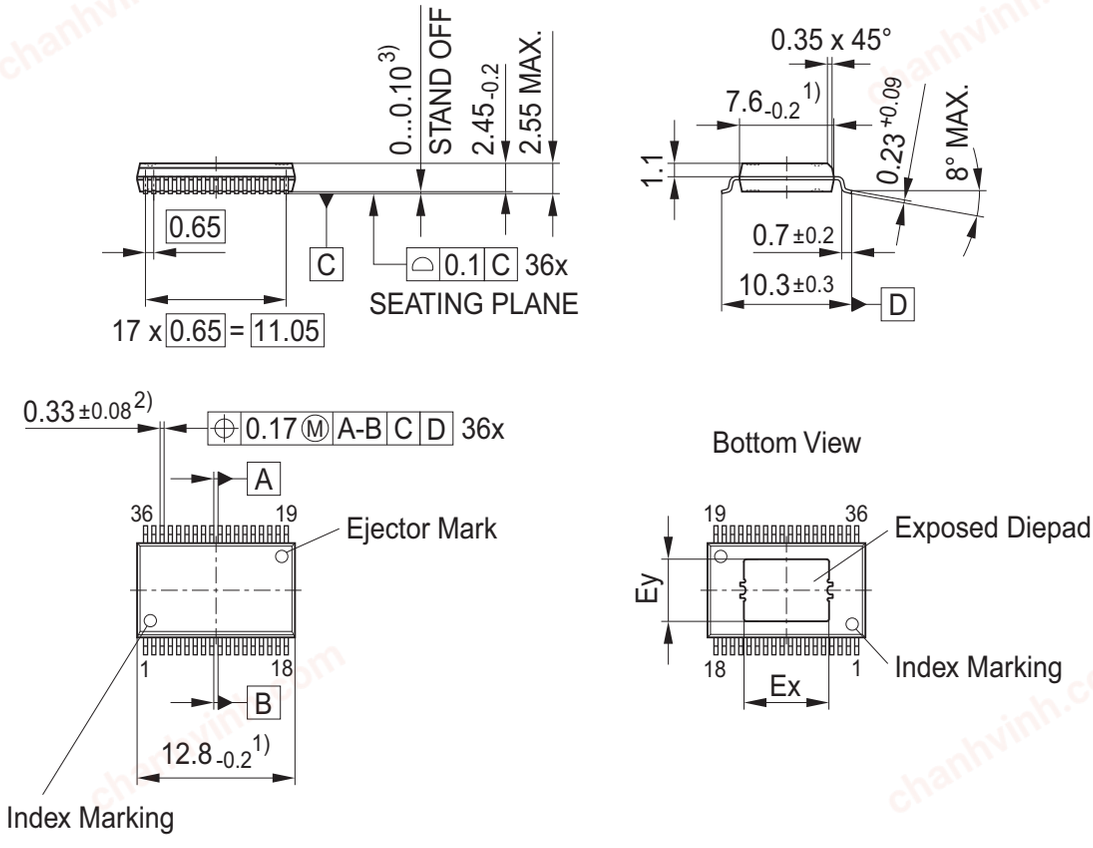
The stand by regulator provides an output voltage of nominal 1.0 V or 2.6 V which is associated with an appropriate stand-by monitoring threshold. The output voltage level is selected by the SEL_STBY configuration. Connecting SEL_STBY to GND results in a voltage level of 2.6 V at Q_STBY, while connecting SEL_STBY with Q_STBY leads to 1.0 V configuration. An integrated pull-up current ensures that the system will turn in the lower stand-by voltage mode in case of open mode at the SEL_STBY pin. However the SEL_STBY pin should be connected either to Q_STBY or to GND in order to select the appropriate Q_STBY voltage level. Intermediate voltage levels at SEL_STBY should be avoided.

Table 6 Stand-by Regulator’s Output Voltage Configuration

No.	SEL_STBY	Q_STBY
1	GND	2.6 V
2	Q_STBY	1.0 V

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7 Package Outlines



Exposed Diepad Dimensions 4)			
Package	Leadframe	Ex	Ey
PG-DSO-36	A6901-C003	7	5.1

1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side
3) Distance from leads bottom (= seating plane) to exposed diepad
4) Excluding the mold flash allowance of 0.3 max per side

Figure 12 **PG-DSO-36** (Plastic Green - Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

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8 Revision History

Rev	Date	Changes
2.6	2019-12-09	• style template updated • editorial changes • figure 12: Package outline drawing updated • chapter 6.3: sentence “Suitable NPN power transistors types are e.g. KSH 200 from Fairchild semiconductor or NJD 2873T4 from ON semiconductor.” removed • P_4.4.47, test specification for capacitor changed from 10 kHz to 1 MHz. • P_4.4.45, P_4.4.46, and P_4.4.106: Output current of Q_LDO3 is corrected to I_{Q_LDO3} • chapter 4.4, table 4: footnote 2, Reference to figure 10 inserted • chapter 6.3: typo corrected • figure 10 application diagram updated • figure 11, bill of material included. • Feedback voltage V_{FB_EXT} 4.4.41: updated minimum value from 1.51V to 1.505V. • Undervoltage Reset threshold on Q_LDO2 $V_{URT\ Q_LDO2,de}$ 4.4.99: updated minimum value from 2.485V to 2.470V. • G-version deleted, as TLE7368G is discontinued. • ESR C_{Q_LDO1} 4.4.23: updated minimum value . • ESR C_{Q_LDO2} 4.4.37: updated minimum value . • ESR C_{FB_EXT} 4.4.47: updated minimum value . • ESR C_{Q_T1} 4.4.53: updated minimum value . • ESR C_{Q_T2} 4.4.59: updated minimum value . • ESR C_{Q_STBY} 4.4.69: updated minimum value . • Pin Configuration table update for Q_LDO1, Q_LDO2, FB_EXT, Q_T1, Q_T2 and Q_STBY: Block to GND with capacitor close to the IC pins for stable regulator operation. • chapter 5.10 Watchdog circuit: Fault Operation: short circuit on pin RT, description reviewed and changed
2.1	2010-11-22	• Final datasheet for TLE7368G, TLE368E, TLE7368-2E and TLE7368-3E • No modification of component or change of electrical parameters
2.0	2009-12-16	• Final datasheet for TLE7368G and TLE7368E • Target Datasheet for TLE7368-2E and TLE7368-3E • Overview updated • Figure 1 and Figure 10 updated • Electrical characteristics: LDO_3 for variants TLE7368-2E and TLE7368-3E included
1.2	2009-04-27	• page 1 updated coverpage • page 37: updated package outline PG-DSO-36-24

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Revision History

Rev	Date	Changes
1.1	2007-11-08	• Final datasheet for both versions, TLE7368G and TLE7368E. • Page 3, Overview: Updated package pictures. • Page 3, Overview: Updated table: Status Final/Target removed. • Page 12, Thermal resistance table: Inserted values for version TLE7368E. • Page 12, Thermal resistance table: Updated values for version TLE7368G. • 4.4.72/4.4.73: Condition described more precise: Inserted “MON_STBY = H”. • **Figure 9**: Modified graph for better description of the window watchdog function. • **Chapter 5.10** Watchdog: Revised phrasing for better understanding
1.0	2007-08-13	• Final Datasheet Version TLE7368G; Target Datasheet Version TLE7368E • “Features section”: AEC certified statement added • “Features section”: RoHS compliance statement and Green product feature added (TLE7368-2E) • **Page 38**: Package changed to RoHS compliant version (TLE7368-2E) • Generally: Improved wording for better understanding • Application and Block Diagrams: Updated to show more details. • Pin Description: Added exposed pad version pinout. • 4.1.30/31: Specified conditions. • Thermal Resistance Table: Modified. Added exposed pad package. • 4.4.51: Voltage Tracker T2: Modified output current limitation to min. 60mA, max 110mA (was min. 50mA, max 100mA) • Selector Pull-down resistor RSEL_LDO2: Max. value changed to 1.9 MOhm. Typ. value changed • 4.4.56/57: Standby Regulator Output Voltage VQ_STBY: Minimum limit changed to 0.93V. Added max. value. • 4.4.60: Standby Regulator Output Current Limitation IQ_STBY, lim: Added test condition • 4.4.61: Standby Regulator Load Regulation DVQ_ STBY: Modified max. limits and defined condition: a) max 5 V/A (was 10 V/A) @ IQ_STBY = 100µA to 10 mA; SEL_STBY = Q_STBY b) max 10 V/A @ IQ_STBY = 100µA to 10 mA; SEL_STBY = GND • 4.4.82, 4.4.108: Updated test conditions. • 4.4.84: Reset delay time base Tcycle: Removed comment “equivalent +/-20%” since it makes no sense here. • 4.4.115: MON_STBY, Threshold on Q_STBY VMON, Q_STBY, de: Removed max. limit because headroom specification was added. • 4.4.115a: New spec line for MON_STBY headroom VMON,Q_STBY,head @ SEL_STBY = Q_STBY. Min. limit 10mV. • 4.4.116: MON_STBY hysteresis VMON,Q_STBY,hy: inserted max. limit of 30mV
0.61	2006-12-18	• Target Datasheet

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