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TLE7259-3

LIN Transceiver

TLE7259-3GE
TLE7259-3LE

Data Sheet

Rev. 1.0, 2013-08-13

Automotive Power

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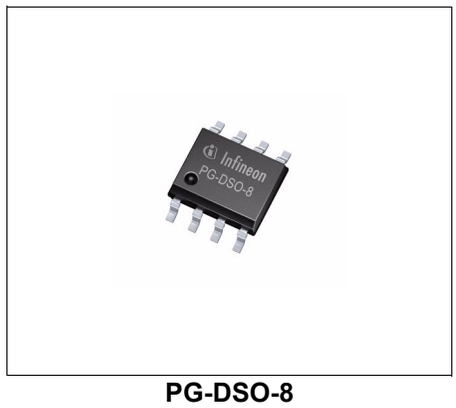
TLE7259-3GE
TLE7259-3LE

AEC Qualified RoHS

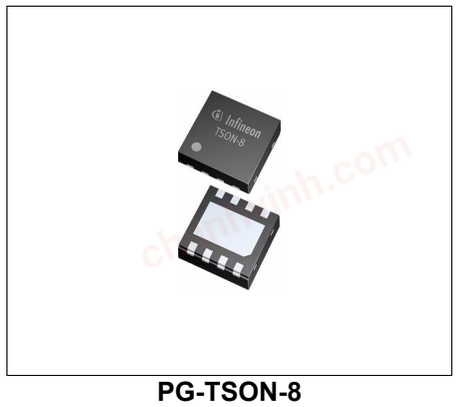
1 Overview

Features

- Single-wire LIN transceiver for transmission rates up to 20 kbps
- Compliant to ISO 17987-4 and LIN Specification 2.2A
- Very low current consumption in sleep mode with wake-up functions
- Very low leakage current on the BUS pin
- Digital I/O levels compatible with 3.3 V and 5 V microcontrollers
- TxD protected with dominant time-out function
- Improved receiver performance:
  Reduced progration delay and increased delay symmetry
- BUS short to V_{BAT} protection and BUS short to GND handling
- Over temperature protection and supply undervoltage detection
- Flash mode supporting accelerated microcontroller programming
- Very high ESD robustness, ± 15 kV according to IEC61000-4-2
- Optimized for high electromagnetic compatibility (EMC);
  Very low emission and high immunity to interference
- Availible in standard PG-DSO-8 and leadless PG-TSON-8 packages
- PG-TSON-8 package supports Automated Optical Inspection (AOI)
- Suitable for 12 V and 24 V board net
- Green Product (RoHS compliant)
- AEC Qualified



PG-DSO-8



PG-TSON-8

Description

The TLE7259-3 is a transceiver for the Local Interconnect Network (LIN) with integrated wake-up and protection features. It is designed for in-vehicle networks using data transmission rates from 2.4 kbps to 20 kbps. The TLE7259-3 operate as a bus driver between the protocol controller and the physical bus of the LIN network. Compliant to all LIN standards and with a wide operational supply range the TLE7259-3 can be used in all automotive applications.

The usage of different operation modes and the INH output allow the TLE7259-3 to control external components, like e.g. voltage regulators. In Sleep-mode the TLE7259-3 draws typically less than 8 µA of quiescent current while still being able to wake up when detecting LIN bus traffic and a local wake up signalst. The very low leakage current on the BUS pin makes the TLE7259-3 especially suitable for partially supplied networks.

Based on the Infineon Smart Power Technology SPT®, the TLE7259-3 provides excellent ESD Robustness and a very high electromagnetic compliance (EMC). The TLE7259-3 reaches very low levels of electromagnetic emission within a broad frequency range, independent from the battery voltage. The TLE7259-3 and the Infineon SPT® technology are AEC qualified and tailored to withstand the harsh condition of the automotive environment.

Type	Package	Marking
TLE7259-3GE	PG-DSO-8	7259-3GE
TLE7259-3LE	PG-TSON-8	7259-3

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2 Block Diagram

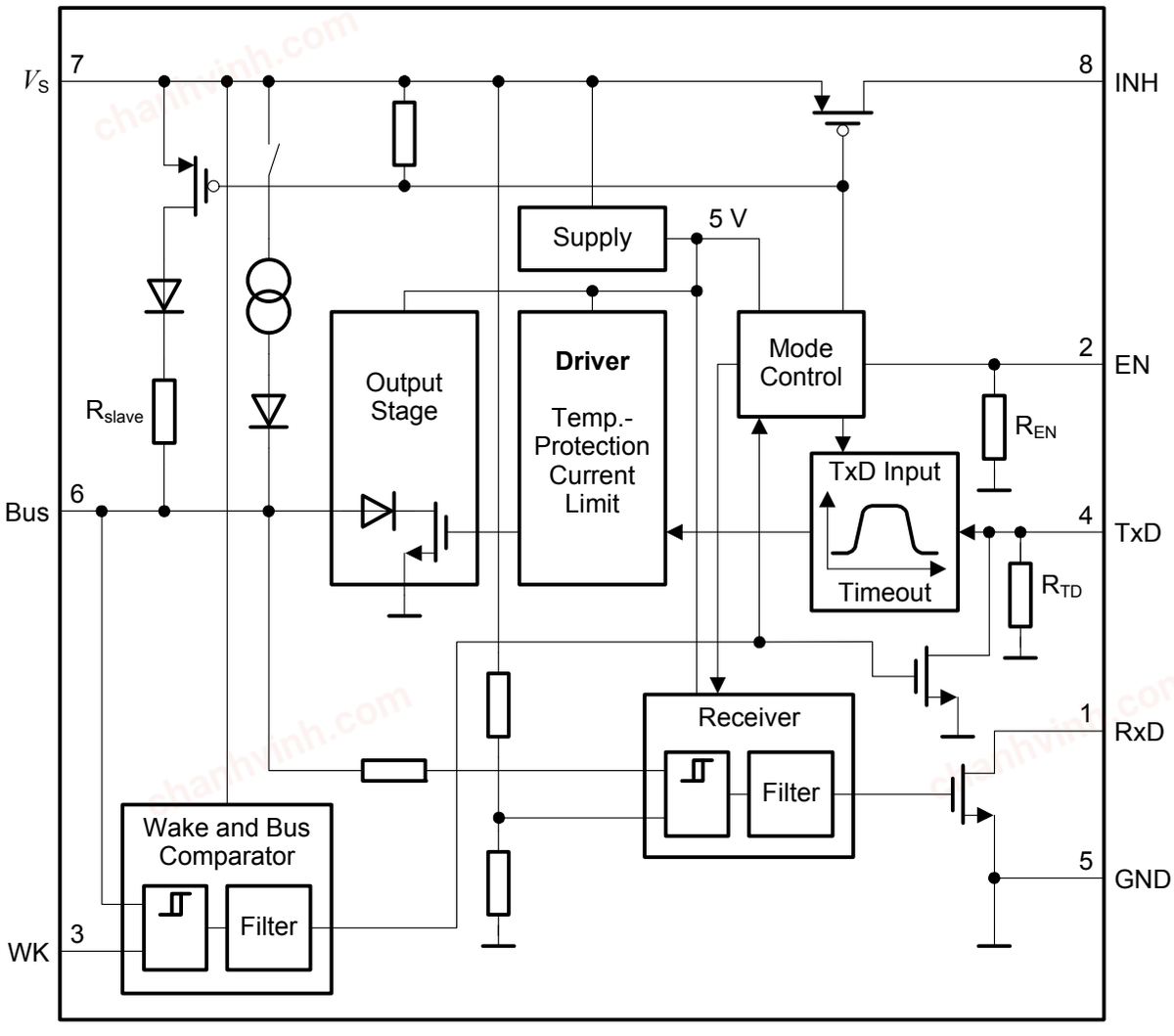


Figure 1 Block Diagram

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3 Pin Configuration

3.1 Pin Assignment

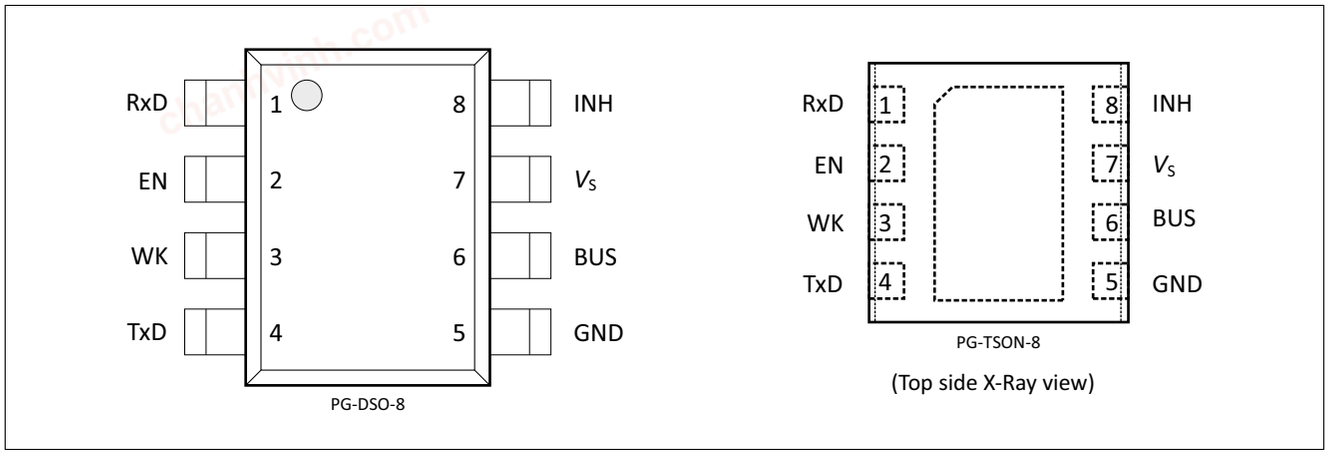


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	RxD	**Receive data output;** External Pull Up necessary LOW in dominant state, active LOW after a Wake-Up event at BUS or WK pin
2	EN	**Enable input;** integrated pull-down, device set to normal operation mode when HIGH
3	WK	**Wake input;** active LOW, negative edge triggered, internal pull-up
4	TxD	**Transmit data input;** integrated pull-down, LOW in dominant state; active LOW after Wake-Up via WK pin
5	GND	**Ground**
6	BUS	**Bus input / output;** LIN bus line input / output LOW in dominant state Internal termination and pull-up current source
7	V_S	**Battery supply input**
8	INH	**Inhibit output;** battery supply related output HIGH (V_S) in Normal and Stand-By operation mode can be used to control an external voltage regulator can be used to control external bus termination resistor when the device will be used as Master node

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4 Functional Description

The LIN Bus is a single wire, bi-directional bus, used for in-vehicle networks. The LIN Transceiver TLE7259-3 is the interface between the microcontroller and the physical LIN Bus (see **Figure 16** and **Figure 17**). The logical values of the microcontroller are driven to the LIN bus via the TxD input of the TLE7259-3. The transmit data stream on the TxD input is converted to a LIN bus signal with optimized slew rate to minimize the EME level of the LIN network. The RxD output reads back the information from the LIN bus to the microcontroller. The receiver has an integrated filter network to suppress noise on the LIN Bus and to increase the EMI (Electro Magnetic Immunity) level of the transceiver.

Two logical states are possible on the LIN bus according to the LIN Specification 2.2A (see **Figure 3**):

In dominant state, the voltage on the LIN bus is set to the GND level. In recessive state, the voltage on the LIN bus is set to the supply voltage V_S. By setting the TxD input of the TLE7259-3 to “Low” the transceiver generates a dominant level on the BUS interface pin. The RxD output reads back the signal on the LIN bus and indicates a dominant LIN bus signal with a logical “Low” to the microcontroller. Setting the TxD pin to “High” the transceiver TLE7259-3 sets the LIN interface pin BUS to the recessive level, at the same time the recessive level on the LIN bus is indicated by a logical “High” on the RxD output.

Every LIN network consists of a master node and one or more slave nodes. To configure the TLE7259-3 for master node applications, a resistor in the range of 1 kΩ and a reverse diode must be connected between the LIN bus and the power supply V_S or the INH pin of the TLE7259-3 (see **Figure 16** and **Figure 17**).

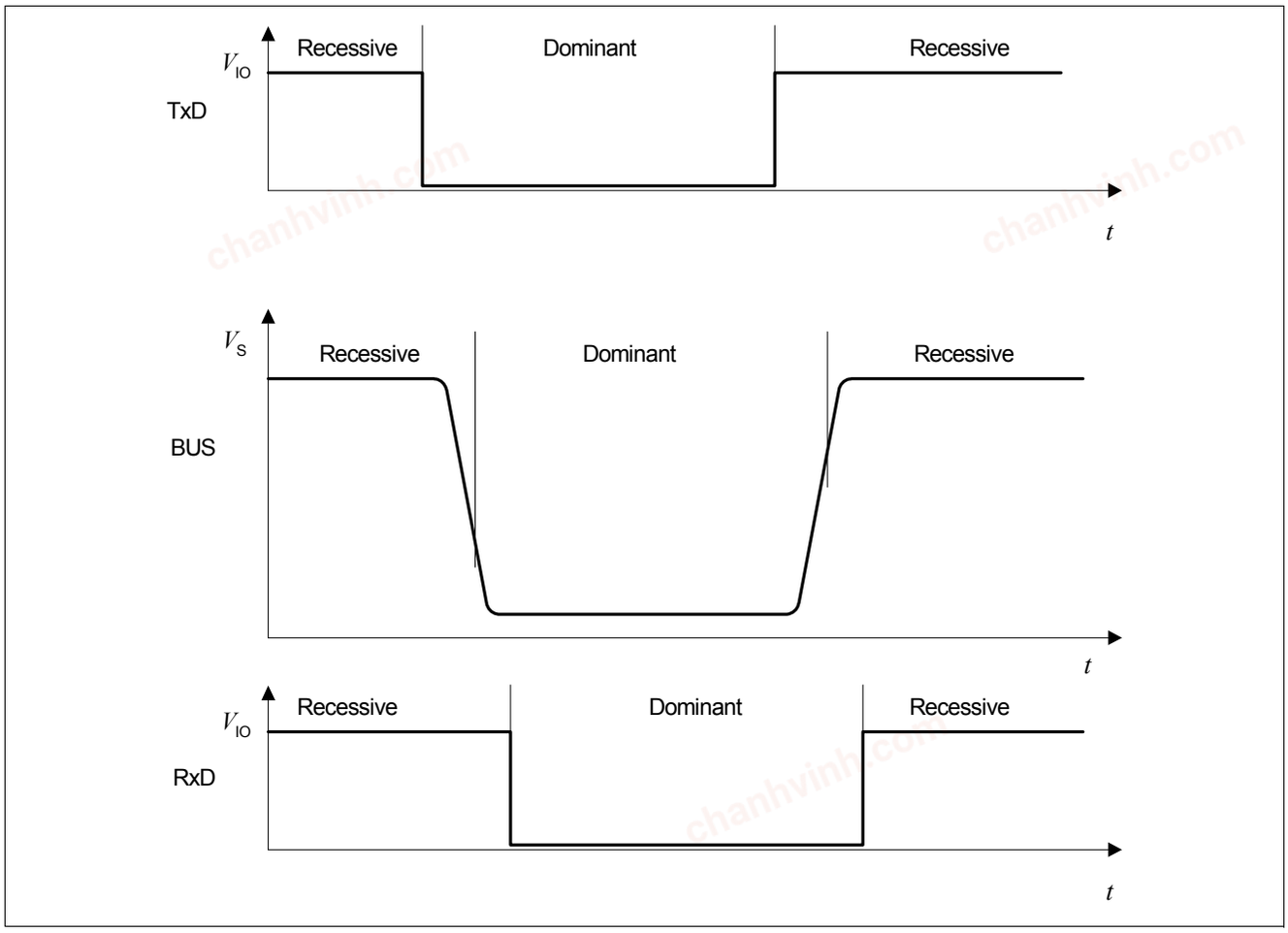


Figure 3 LIN bus signals

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4.1 Operating Modes

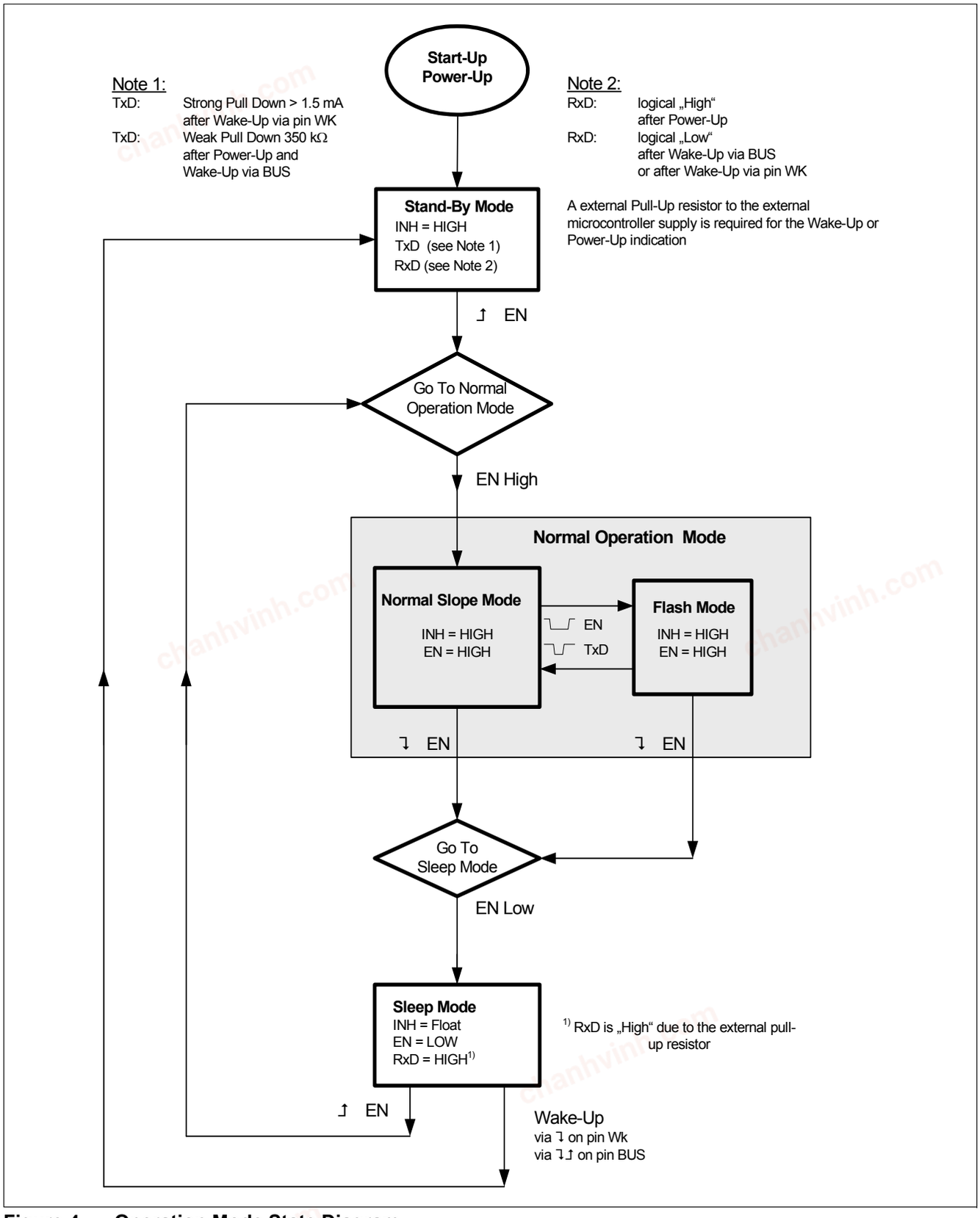


Figure 4 Operation Mode State Diagram

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The TLE7259-3 has 3 major operation modes:

- Stand-By mode
- Normal Operation mode
- Sleep mode

The Normal Operation mode contains 2 sub-operation modes, which differentiate by the slew rate control of the LIN Bus signal (see **Figure 4**).

Sub-operation modes with different slew rates on the BUS pin:

- Normal Slope mode, for data transmission rates up to 20 kBaud
- Flash mode, for programming of the external microcontroller

The operation mode of the TLE7259-3 is selected by the EN pin. (see **Figure 4**).

Table 1 Operating modes

Mode	EN	INH	TxD	RxD	LIN Bus Termination	Comments
Sleep	Low	Floating	Low	High[1)]	High Impedance	No wake-up request detected
Stand-By	Low	High	Low High[2)]	Low High [1)]	30 kΩ (typical)	RxD “Low” after local Wake-Up (pin WK) or bus wake-up (pin BUS) RxD “High“ after power-up TxD strong pull down after local wake-up (WK pin)[2)] TxD weak pull down after bus wake-up (pin BUS) or Power-Up[2)]
Normal Operation	High	High	Low High	Low High	30 kΩ (typical)	RxD reflects the signal on the BUS TxD driven by the microcontroller

1) A pull-up resistor to the external microcontroller supply is required.

2) The TxD input needs an external termination to indicate a “High” or a “Low” signal. The external termination could be a pull-up resistor or an active microcontroller output.

4.2 Normal Operation Mode

The TLE7259-3 enters the Normal Operation mode after the microcontroller sets EN to “High” (see **Figure 4**). In Normal Operation mode the LIN bus receiver and the LIN bus transmitter are active. Data from the microcontroller is transmitted to the LIN bus via the TxD pin, the receiver detects the data stream on the LIN bus and forwards it to the RxD output pin. In Normal Operation mode, the INH pin is “High” (set to V_S) and the bus termination is set to 30 kΩ.

Normal Slope mode and the Flash mode are Normal Operation modes and in these sub-modes the behavior of the INH pin and the bus termination is the same. Per default the TLE7259-3 always enters into Normal Slope mode, either from Sleep mode or from Stand-By mode. The Flash mode can only be entered from Normal Slope mode.

In order to avoid any bus disturbance during a mode change, the output stage of the TLE7259-3 is disabled and set to recessive state during the mode change procedure. To release the TLE7259-3 for data communication on the LIN bus, the TxD pin needs to be set to “High” for the time $t_{to,rec}$.

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4.2.1 Normal Slope Mode

In Normal Slope mode data transmission rates up to 20 kBauds are possible. Setting the EN pin to “High” starts the transition to Normal Slope mode. (see **Figure 5**).

The mode change to Normal Slope mode is defined by the time t_{MODE}. The time t_{MODE} specifies the delay time between the threshold, where the EN pin detects a “High” input signal, and the actual mode change of TLE7259-3 into Normal Slope mode. Entering in Normal Operation mode, the TLE7259-3 always enters per default into Normal Slope mode. The signal on the TxD pin is not relevant for entering into Normal Slope mode.

Finally to release the data communication it is required to set the TxD pin to “High” for the time $t_{to,rec.}$

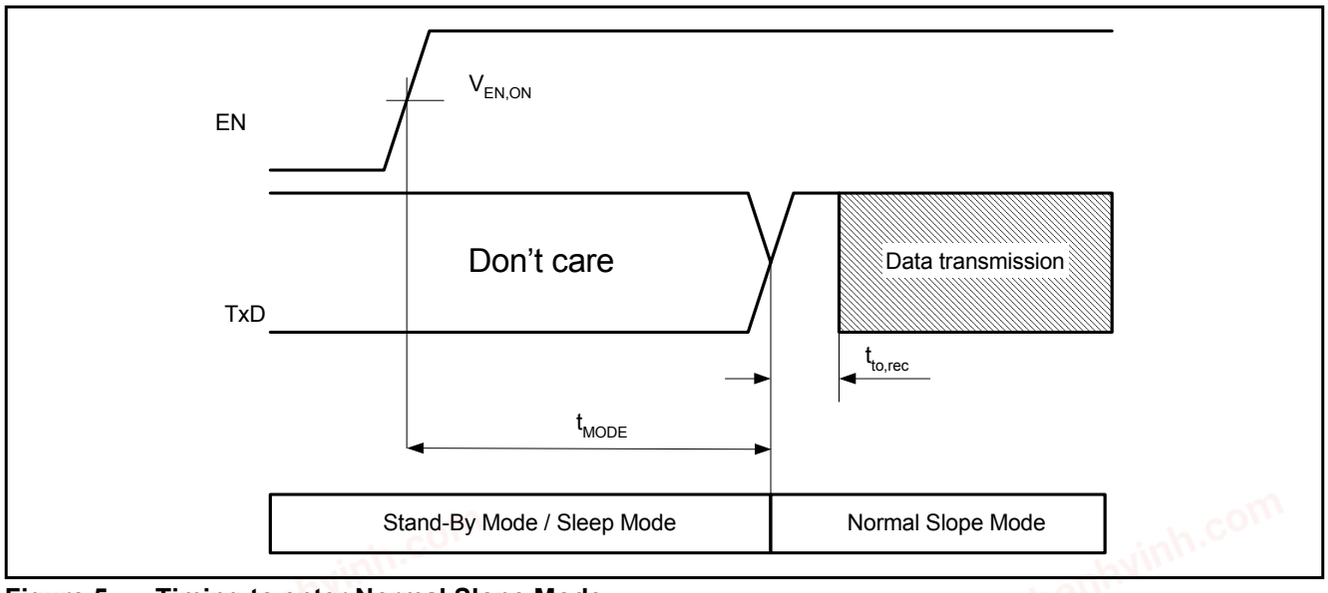


Figure 5 Timing to enter Normal Slope Mode

4.2.2 Flash Mode

In Flash mode it is possible to transmit and receive LIN messages on the LIN bus. The slew rate control mechanism of the LIN bus signal is disabled. This allows higher data transmission rates, disregarding the EMC limitations of the LIN network. The Flash mode is intended to be used during the ECU production for programming the microcontroller via the LIN bus interface.

The TLE7259-3 can be set to Flash mode only from Normal Slope mode (see **Figure 4**). Flash mode is entered by setting the EN pin to “Low” for the time t_{fl1} and generating a falling and a rising edge at the TxD pin with the timing t_{fl2}, t_{fl3} and t_{fl4} (see **Figure 6**). Leaving the Flash mode by the same sequence, sets the TLE7259-3 back to Normal Slope mode. Finally to release the data transmission it is required to set the TxD pin to “High” for the time $t_{to,rec}$.

Additionally the TLE7259-3 can leave the Flash mode as well by switching only the EN pin to “Low”. By applying this “Low” signal to the EN pin the TLE7259-3 is put into Sleep mode.

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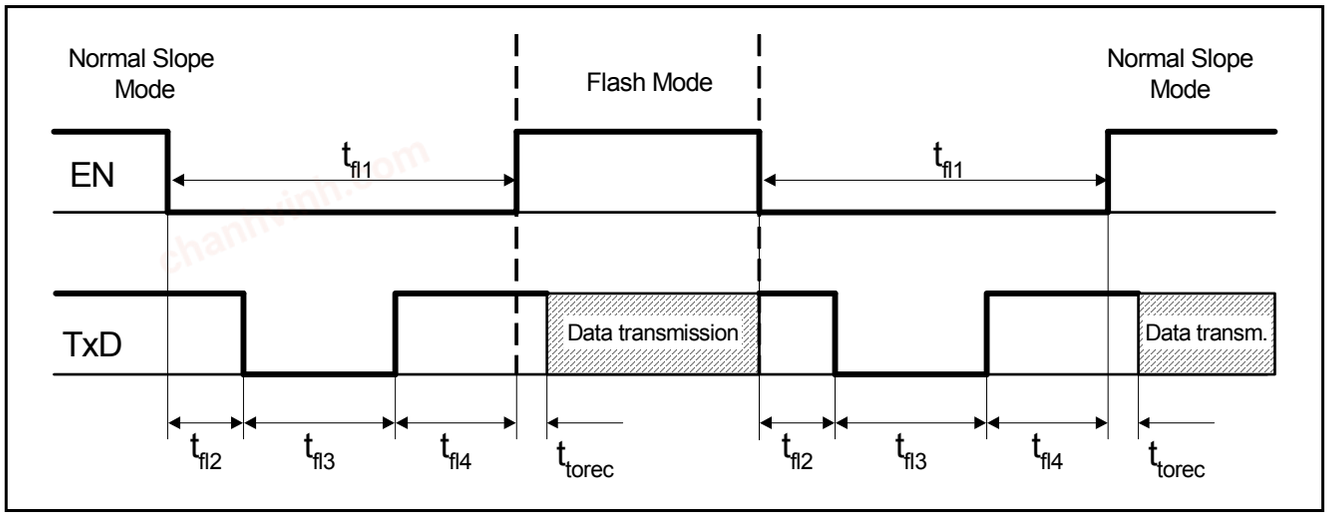


Figure 6 Timing to enter and leave Flash Mode

4.3 Stand-By Mode

The Stand-By mode is entered automatically after:

- A power-up event at the supply V_S.
- A bus wake-up event at the pin BUS.
- A local wake-up event at the pin WK.
- A power on reset caused by power supply V_S.
- In Stand-By mode the Wake-Up sources are monitored by the TxD and RxD pins.

In Stand-By mode no communication on the LIN Bus is possible. The output stage is disabled and the LIN Bus termination remains activated. The RxD and the TxD pin are used to indicate the wake-up source or a power-up event. The RxD pin remains “Low“ after a local wake-up event on the pin WK and a bus wake-up event on the LIN bus. A power-up event is indicated by a logical “High“ on the RxD pin. The signal on the TxD pin indicates the wake-up source, a weak pull-down signals a bus wake-up event on the LIN bus and a strong pull-down signals a local wake-up event caused by the WK pin (see **Table 1** and **Table 2**). In order to detect a wake-up event via the TxD pin, the external microcontroller output needs to provide a logical “High” signal. The wake-up flags indicating the wake-up source on the pins TxD and RxD are reset by changing the operation mode to Normal Operation mode.

The signal on the EN pin remains “Low“ due to an internal pull-down resistor. Setting the EN pin to “High“, by the microcontroller returns the TLE7259-3 to Normal Operation mode. In Stand-By mode the INH output is switching to V_S. The INH output can be used to control external devices like a voltage regulator.

Table 2 Logic table for wake up monitoring

Power up	WK	BUS	RxD[1)]	TxD[2)]	Remarks
Yes	1	1	1	1	No wake-up, power-up event
No	Wake-up[3)]	1	0	0	Wake via wake pin
No	1	Wake-up[4)]	0	1	Wake via BUS

1) To indicate the wake-up sources via the RxD pin, a pull-up resistor to the external microcontroller supply is required.
2) The TxD input needs an external termination to indicate a “High” or a “Low” signal. The external termination could be a pull-up resistor or an active microcontroller output.
3) A local wake-up event is considered after a low signal on the pin WK (see **Chapter 4.7**).
4) A bus wake-up event is considered after a low to high transition on the LIN bus (see **Chapter 4.6**)

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4.4 Sleep Mode

In order to reduce the current consumption the TLE7259-3 offers a Sleep mode. In Sleep mode the quiescent current on V_S and the leakage current on the pin BUS are cut back to a minimum.

To switch the TLE7259-3 from Normal Operation mode to Sleep mode, the EN pin has to be set to “Low”. Conversely a logical “High” on the EN pin sets the device directly back to Normal Operation mode (see **Figure 4**).

While the TLE7259-3 is in Sleep mode the following functions are available:

- The output stage is disabled and the internal bus terminations are switched off (High Impedance on the pin BUS). The internal current source on the bus pin ensures that the level on the pin BUS remains recessive and protects the LIN network against accidental bus wake-up events.
- The receiver stage is turned off.
- RxD output pin is “High” if a pull-up resistor is connected to the external microcontroller supply. The TxD pin is disabled. The logical state on the TxD pin is “Low”, due to the internal pull-down resistor.
- The INH output is switched off and floating.
- The bus wake-up comparator is active and will cause a transition to Stand-By mode in case of a bus wake-up event.
- The WK pin is active and turns the TLE7259-3 to Stand-By mode in case of a local wake-up.
- The EN pin remains active, switching the EN pin to “High“ changes the operation mode to Normal Slope mode.

4.5 Wake-Up Events

A wake-up event changes the operation mode of the TLE7259-3 from Sleep mode to Stand-By mode. There are 3 different ways to wake-up the TLE7259-3 from Sleep mode.

- Bus wake-up via a minimum dominant signal ($t_{WK,bus}$) on the pin BUS.
- Local wake-up via a minimum dominant time (t_{WK}) on the WK pin.
- Mode change from Sleep mode to Normal Operation mode, by setting the EN pin to logical “High”.

4.6 Bus Wake-Up via LIN bus

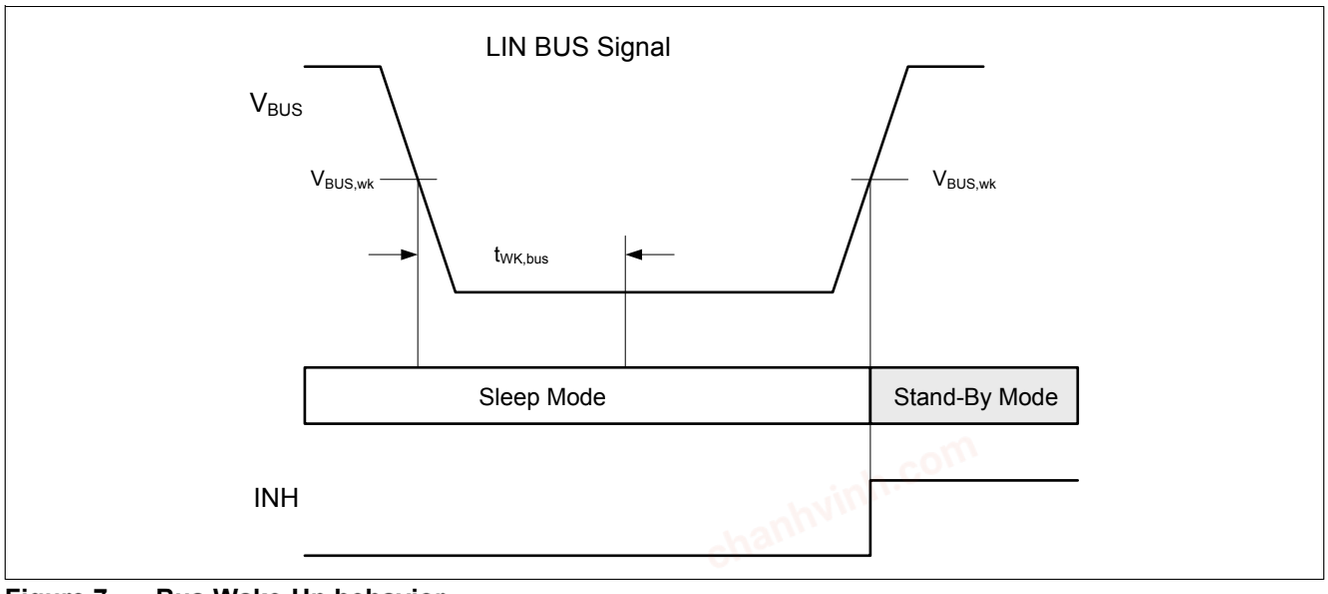


Figure 7 Bus Wake-Up behavior

The bus wake-up event, often called remote Wake-Up, changes the operation mode from Sleep mode to Stand-By mode. A falling edge on the LIN bus, followed by a dominant bus signal t > $t_{WK,bus}$ results in a bus wake-up event. The mode change to Stand-By mode becomes active with the following rising edge on the LIN bus. The

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TLE7259-3 remains in Sleep mode until it detects a change from dominant to recessive on the LIN bus (see **Figure 7**).

In Stand-By mode the TxD pin indicates the source of the wake-up event. A weak pull-down on the pin TxD indicates a bus wake-up event (see **Figure 4**). The RxD pin signals if a wake-up event occurred or the power-up event. A “Low” signal on the RxD pin reports a local or bus wake-up event, a logical “High“ signal on RxD indicates a power-up event.

4.7 Local Wake-Up

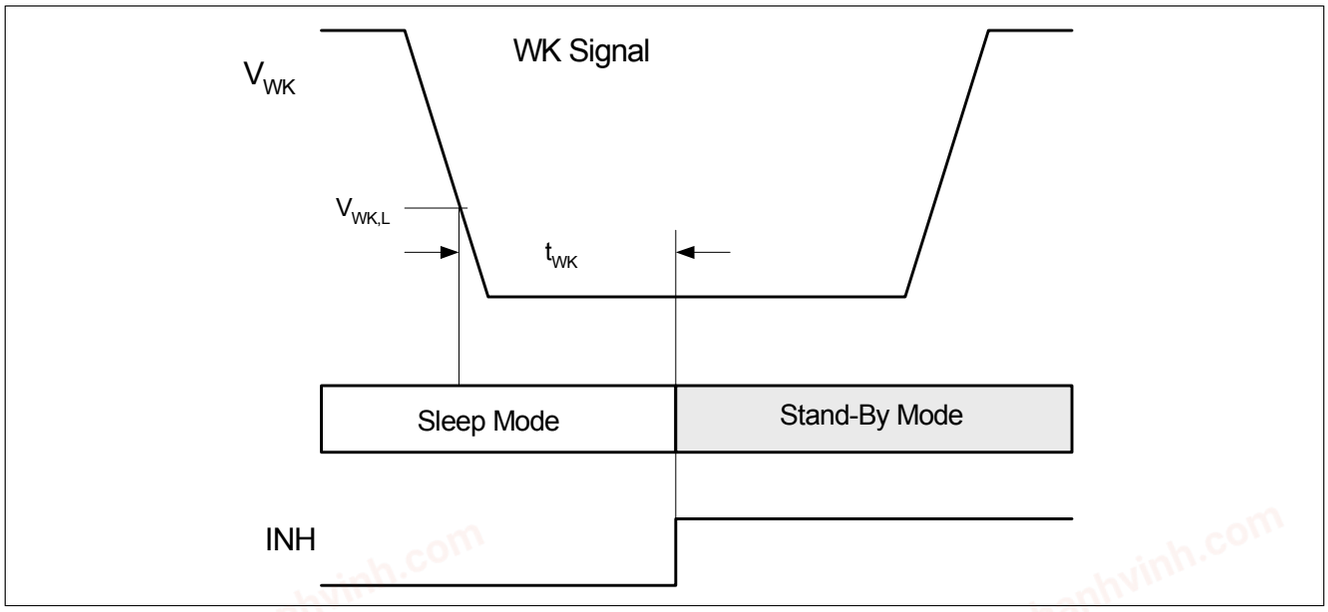


Figure 8 Local wake-up behavior

Beside the remote wake-up, a wake-up of the TLE7259-3 via the WK pin is possible. This type of wake-up event is called “Local Wake Up”. A falling edge on the WK pin followed by a “Low“ signal for t > t_{WK} results in a local wake-up (see **Figure 8**) and changes the operation mode to Stand-By mode.

In Stand-By mode the TxD pin indicates the source of the Wake-Up event. A strong pull-down on the pin TxD indicates a local wake-up event (see **Figure 4**). The RxD pin signals if a wake-up event or the power-up event occurred. A “Low” signal on the RxD pin reports a local or bus wake-up event, a logical “High“ signal on RxD indicates a power-up event.

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4.8 Mode Transition via EN pin

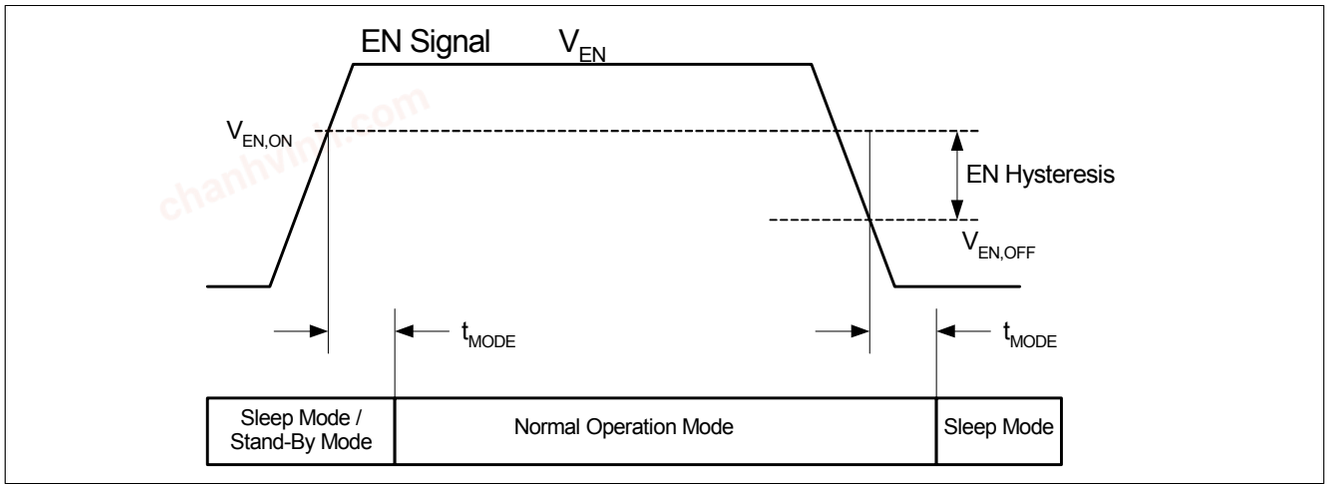


Figure 9 Mode Transition via EN pin

It is also possible to change from Sleep mode to Normal Operation mode by setting the EN pin to logical “High“. This feature is useful if the external microcontroller is continuously powered, the microcontroller power-supply is not controlled by the INH pin. The EN pin has an integrated pull-down resistor to ensure the device remains in Sleep or Stand-By mode even if the voltage on the EN pin is floating. The EN pin has an integrated hysteresis (see **Figure 9**).

A transition from logical “High“ to logical “Low“ on the EN pin changes the operation mode from Normal Operation mode to Sleep mode. If the TLE7259-3 is already in Sleep mode, changing the EN from “Low“ to “High” results into a mode change from Sleep mode to Normal Operation mode. If the device is in Stand-By mode a change from “Low“ to “High” on the EN pin changes the mode to Normal Operation mode, as well (see **Figure 4**).

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4.9 TxD Time Out function

If the TxD signal is dominant for a time $t > t_{timeout}$ the TxD time-out function deactivates the transmission of the LIN signal to the bus and disables the output stage. This is realized to prevent the bus from being blocked by a permanent “Low” signal on the TxD pin, caused by an error on the external microcontroller (see **Figure 10**).

The transmission is released again, after a rising edge at the pin TxD has been detected.

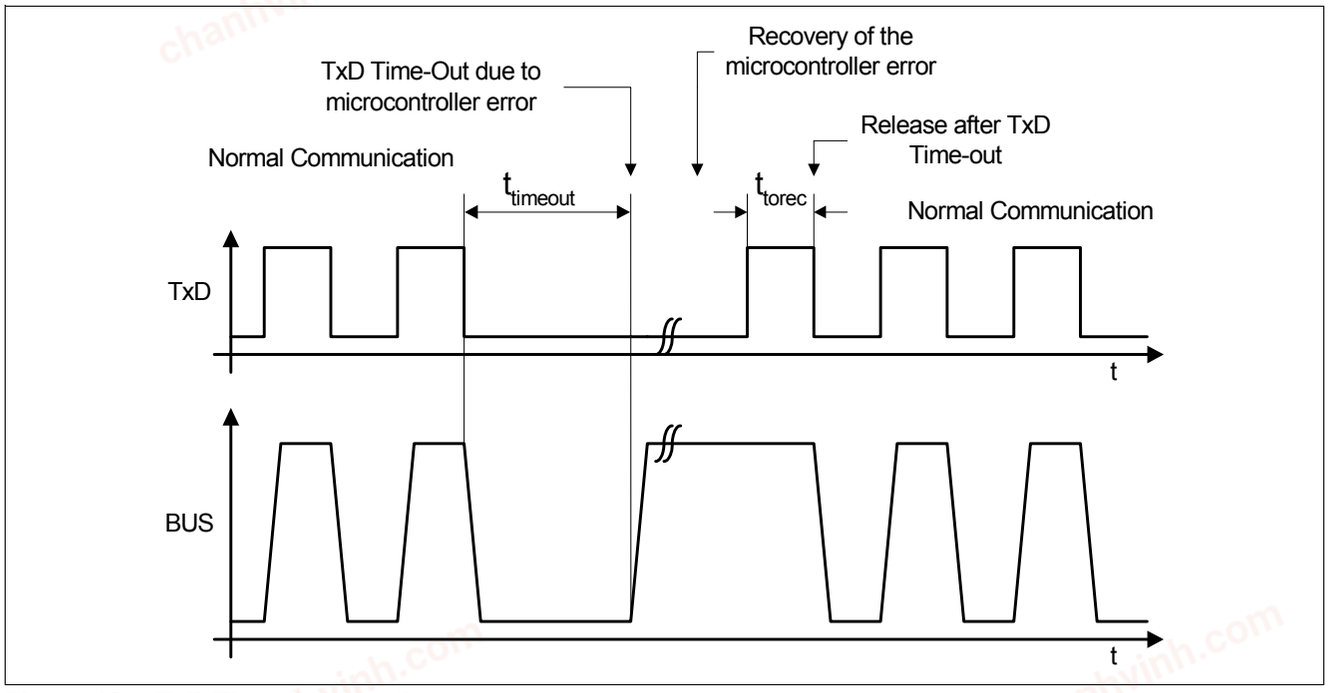


Figure 10 TxD Time-Out function

4.10 Over Temperature protection

The TLE7259-3 has an integrated over temperature sensor to protect the device against thermal overstress on the output stage. In case of an over temperature event, the temperature sensor will disable the output stage (see **Figure 1**). An over temperature event will not cause any mode change and will not be indicated by the RxD pin or the TxD pin. When the junction temperature falls below the thermal shut down level $T_J < T_{jSD}$, the output stage is re-enabled and data communication can start again on the LIN bus. A 10°C hysteresis avoids toggling during the temperature shut down.

4.11 3.3 V and 5 V Logic Capability

The TLE7259-3 can be used for 3.3 V and 5 V microcontrollers. The inputs and the outputs are capable to operate with both voltage levels. The RxD output must have an external pull-up resistor to the microcontroller supply to define the output voltage level.

BUS Short to GND Feature

The TLE7259-3 has a feature implemented to protect the battery from running out of charge in case the LIN bus is shorted to GND.

In this failure case a normal master termination, a 1 kΩ resistor and diode between the LIN bus and the power supply V_S, would cause a constantly drawn current even in Sleep mode. The resulting resistance of this short to GND is lower than 1 kΩ. To avoid this current during a generator off state, like in a parked car, the TLE7259-3 has a bus short to GND feature implemented, which is activated in Sleep mode.

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This feature is only applicable, if the master termination of the LIN bus is connected to the INH pin, instead of being connected to the power supply V_S (see **Figure 16** and **Figure 17**). Internally, the 30 kΩ path is also switched off from the power supply V_S (see **Figure 1**).

A separate Master Termination Switch is implemented at the pin BUS, to avoid a voltage drop on the recessive level of LIN bus, in case of a dominant level or a short to ground on at the LIN bus.

4.12 LIN Specifications 1.2, 1.3, 2.0, 2.1, 2.2 and 2.2A

The device fulfills the Physical Layer Specification of LIN 1.2, 1.3, 2.0, 2.1, 2.2 and 2.2A.

The differences between LIN specification 1.2 and 1.3 is mainly the physical layer specification. The reason was to improve the compatibility between the nodes.

The LIN specification 2.0 is a super set of the 1.3 version. The 2.0 version offers new features. However, it is possible to use the LIN 1.3 slave node in a 2.0 node cluster, as long as the new features are not used. Vice versa it is possible to use a LIN 2.0 node in the 1.3 cluster without using the new features.

In terms of the physical layer the LIN 2.1, LIN 2.2 and LIN 2.2A Specification doesn’t include any changes and is fully compliant to the LIN Specification 2.0.

LIN 2.2A is the latest version of the LIN specification, released in December 2010.

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5 General Product Characteristics

5.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings Voltages, Currents and Temperatures[1)]

All voltages with respect to ground; positive current flowing into pin;

(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
Voltages						
5.1.1	Battery supply voltage	V_S	-0.3	40	V	LIN Spec 2.2A (Par. 11)
5.1.2	Bus and WK input voltage versus GND versus V_S	 $V_{BUS,G}$ $V_{BUS,Vs}$	 -40 -40	 40 40	 V V	–
5.1.3	Logic voltages at EN, TxD, RxD	V_{logic}	-0.3	5.5	V	–
5.1.4	INH Voltage versus GND versus V_S	 $V_{INH,G}$ $V_{INH, Vs}$	 -0.3 -40	 40 0.3	 V V	–
Currents						
5.1.5	Output current at INH	I_{INH}	-150	80	mA	2)
Temperatures						
5.1.6	Junction temperature	T_j	-40	150	°C	–
5.1.7	Storage temperature	T_s	-55	150	°C	–
ESD Resistivity						
5.1.8	Electrostatic discharge voltage at V_S, Bus, WK versus GND	V_{ESD}	-6	6	kV	Human Body Model (100 pF via 1.5 kΩ)[3)]
5.1.9	Electrostatic discharge voltage all pins	V_{ESD}	-2	2	kV	Human Body Model (100 pF via 1.5 kΩ)[3)]

1) Not subject to production test, specified by design

2) Output current is internally limited to -150 mA

3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

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5.2 Functional Range

Table 4 Operating Range

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Supply voltages							
5.2.1	Extended Supply Voltage Range for Operation	$V_{S(ext)}$	5	–	40	V	Parameter deviations possible
5.2.1	Supply Voltage range for Normal Operation	$V_{S(nor)}$	5.5	–	27	V	LIN Spec 2.2A (Par. 10)
Thermal parameters							
5.2.2	Junction temperature	T_j	-40	–	150	°C	1)

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.3 Thermal Characteristics

Table 5 Thermal Resistance[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Thermal Resistance, PG-DSO-8 Package Version							
5.3.1	Junction to Soldering Point	R_{thJSP}	–	–	25	K/W	measured on pin 5
5.3.2	Junction ambient	R_{thJA}	–	130	–	K/W	2)
Thermal Resistance, PG-TSON-8 Package Version							
5.3.1	Junction ambient	R_{thJA}	–	60	–	K/W	2)
5.3.2			–	190	–	K/W	Footprint only 3)
5.3.3			–	70	–	K/W	300 mm^2 heatsink on PCB 3)
Thermal Shutdown Junction Temperature							
5.3.4	Thermal shutdown temp.	T_{jSD}	150	175	190	°C	–
5.3.5	Thermal shutdown hyst.	ΔT	–	10	–	K	–

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted to the first inner copper layer.

3) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1 inner copper layer (1 x 70 µm Cu).

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6 Electrical Characteristics

6.1 Functional Device Characteristics

Table 6 Electrical Characteristics

5.5 V < V_S < 27 V; R_L = 500 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Current Consumption							
6.1.1	Current consumption at V_S	$I_{S,rec}$	0.5	1.1	3.0	mA	Recessive state, without R_L; V_S = 13.5 V; V_{TxD} = “High”
6.1.2	Current consumption at V_S Dominate State	$I_{S,dom}$	–	1.5	5.0	mA	Dominant state, without R_L; V_S = 13.5 V; V_{TxD} = 0 V
6.1.3	Current consumption at V_S in sleep mode	$I_{S,sleep}$	–	5	12	µA	Sleep mode; V_S = 18 V; V_{WK} = V_S = V_{BUS}
6.1.4	Current consumption at V_S in sleep mode	$I_{S,sleep,typ}$	–	–	10	µA	Sleep mode; T_j < 85°C; V_S = 13.5 V; V_{WK} = V_S = V_{BUS}
6.1.5	Current consumption in sleep mode bus shorted to GND	I_{S,lkg,SC_GND}	–	45	100	µA	Sleep mode; V_S = 13.5 V; V_{BUS} = 0 V
Receiver Output: RxD							
6.1.6	HIGH level leakage current	$I_{RD,H,leak}$	-5	–	5	µA	V_{RxD} = 5 V; V_{BUS} = V_S
6.1.7	LOW level output current	$I_{RD,L}$	1.7	–	10	mA	V_{RxD} = 0.9 V; V_{BUS} = 0 V
Transmission Input: TxD							
6.1.8	HIGH level input voltage range	$V_{TD,H}$	2	–	5.5	V	Recessive state
6.1.9	Input hysteresis	$V_{TD,hys}$	150	300	450	mV	1)
6.1.10	LOW level input voltage range	$V_{TD,L}$	-0.3	–	0.8	V	Dominant state
6.1.11	Pull-down resistance	R_{TD}	100	350	800	kΩ	V_{TxD} = “High”
6.1.12	Dominant current standby mode after Wake-Up	$I_{TD,L}$	1.5	3	10	mA	V_{TxD} = 0.9 V; V_{WK} = 0 V; V_S = 13.5 V
6.1.13	Input capacitance	C_i	–	5	–	pF	1)

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Table 6 Electrical Characteristics (cont'd)

5.5 V < V_S < 27 V; R_L = 500 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Enable Input: EN							
6.1.14	HIGH level input voltage range	$V_{EN,ON}$	2	–	5.5	V	Normal Operation mode
6.1.15	LOW level input voltage range	$V_{EN,OFF}$	-0.3	–	0.8	V	Sleep mode or Stand-By mode
6.1.16	Input hysteresis	$V_{EN,hys}$	150	300	450	mV	1)
6.1.17	Pull-down resistance	R_{EN}	15	30	60	kΩ	–
6.1.18	Input capacitance	Ci_{EN}	–	5	–	pF	1)
Inhibit, Master Termination Output: INH							
6.1.19	Inhibit R_{on} resistance	$R_{INH,on}$	22	36	50	Ω	I_{INH} = -15 mA
6.1.20	Maximum INH output current	I_{INH}	-150	-110	-40	mA	V_{INH} = 0 V
6.1.21	Leakage current	$I_{INH,lk}$	-5.0	–	5.0	µA	Sleep mode; V_{INH} = 0 V
Wake Input: WK							
6.1.22	High level input voltage	$V_{WK,H}$	V_S - 1 V	–	V_S + 3 V	V	tested V_S = 13.5 V;
6.1.23	Low level input voltage	$V_{WK,L}$	-0.3	–	V_S - 4 V	V	tested V_S = 13.5 V;
6.1.24	Pull-up current	$I_{WK,PU}$	-60	-20	-3	µA	–
6.1.25	High level leakage current	$I_{WK,H,leak}$	-5	–	5	µA	V_S = 0 V; V_{WK} = 40 V
6.1.26	Dominant time for Wake-Up	t_{WK}	30	–	150	µs	–
6.1.27	Input Capacitance	Ci_{WK}	–	15	–	pF	1)
Bus Receiver: BUS							
6.1.28	Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	–	V	–
6.1.29	Receiver dominant state	V_{BUSdom}	V_S - 40 V	–	0.4 × V_S	V	LIN Spec 2.2A (Par. 17) 2)
6.1.30	Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	–	0.55 × V_S	0.6 × V_S	V	–
6.1.31	Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 x V_s	V	LIN Spec 2.2A (Par. 18) 3)
6.1.32	Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	7.0V < V_S < 27V; LIN Spec 2.2A (Par. 19) 4)
6.1.33	Receiver hysteresis	V_{HYS}	0.07 × V_S	0.12 × V_S	0.175 × V_S	V	LIN Spec 2.2A (Par. 20) 5)
6.1.34	Wake-Up threshold voltage	$V_{BUS,wk}$	0.40 × V_S	0.5 × V_S	0.6 × V_S	V	–
6.1.35	Dominant time for bus Wake-Up	$t_{WK,bus}$	30	–	150	µs	–

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Table 6 Electrical Characteristics (cont'd)

5.5 V < V_S < 27 V; R_L = 500 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Bus Transmitter BUS							
6.1.36	Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = "High"
6.1.37	Bus dominant output voltage maximum load	$V_{BUS,do}$					V_{TxD} = 0 V; R_L = 500 Ω
			–	–	1.2	V	5.5 ≤ V_S ≤ 7.3 V;
			–	–	0.2 x V_S	V	7.3 < V_S ≤ 10 V;
			–	–	2.0	V	10 < V_S ≤ 18 V;
							(see **Figure 12**)
6.1.38	Bus short circuit current	I_{BUS_LIM}	70	100	150	mA	V_{BUS} = 13.5 V; LIN Spec 2.2A (Par. 12)
6.1.39	Leakage current	$I_{BUS_NO_GND}$	-1	-0.5	–	mA	V_S = 0 V; V_{BUS} = -12 V; LIN Spec 2.2A (Par. 15)
6.1.40	Leakage current	$I_{BUS_NO_BAT}$	–	1	8	µA	V_S = 0 V; V_{BUS} = 18 V; LIN Spec 2.2A (Par. 16)
6.1.41	Leakage current	$I_{BUS_PAS_dom}$	-1	-0.5	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN Spec 2.2A (Par. 13)
6.1.42	Leakage current	$I_{BUS_PAS_rec}$	–	1	8	µA	V_S = 8 V; V_{BUS} = 18 V; LIN Spec 2.2A (Par. 14)
6.1.43	Bus pull-up resistance	R_{slave}	20	30	47	kΩ	Normal mode; LIN Spec 2.2A (Par. 26)
6.1.44	LIN output current	I_{BUS}	-60	-30	-5	µA	Sleep mode; V_S = 13.5 V; V_{EN} = 0 V
6.1.45	Input Capacitance	Ci_{BUS}		15	–	pF	[1]
Dynamic Transceiver Characteristics: BUS							
6.1.46	Propagation delay LIN bus to RxD						LIN Spec 2.2A (Par. 31) R_{RxD} = 2.4 kΩ; C_{RxD} = 20 pF
	Dominant to RxD Low	t_{rx_pdf}	–	1	5	µs	
	Recessive to RxD High	t_{rx_pdr}	–	1	5	µs	
6.1.47	Receiver delay symmetry	t_{rx_sym}	-1.3	–	1.3	µs	LIN Spec 2.2A (Par. 32) t_{rx_sym} = t_{rx_pdf} - t_{rx_pdr}; R_{RxD} = 2.4 kΩ; C_{RxD} = 20 pF
6.1.48	Delay time for mode change	t_{MODE}	–	–	150	µs	[1] See **Figure 5**
6.1.49	TxD dominant time out	$t_{timeout}$	8	13	20	ms	V_{TxD} = 0 V
6.1.50	TxD dominant time out recovery time	t_{torec}	–	–	15	µs	[1]
6.1.51	EN toggling to enter the flash mode	t_{fl1}	25	35	50	µs	[1] See **Figure 6**
6.1.52	TxD time for flash activation	t_{fl2}	5	–	–	µs	[1] See **Figure 6**
		t_{fl3}	10	–	–		
		t_{fl4}	10	–	–		

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Table 6 Electrical Characteristics (cont'd)

5.5 V < V_S < 27 V; R_L = 500 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
6.1.53	Duty cycle D1 (for worst case at 20 kBit/s)	D1	0.396	–	–		duty cycle 1[6] TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) =0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus_rec(min)}$/2 t_{bit}; LIN Spec 2.2A (Par. 27)
6.1.54	Duty cycle D1 for V_s supply 5.5 V to 7.0 V (for worst case at 20 kBit/s)	D1	0.396	–	–		duty cycle 1[6] TH_{Rec}(min)= 0.760 × V_S; TH_{Dom}(min)= 0.593 × V_S; 5.5 V < V_S < 7.0 V; t_{bit} = 50 µs; D1 = $t_{bus_rec(min)}$/2 t_{bit};
6.1.55	Duty cycle D2 (for worst case at 20 kBit/s)	D2	–	–	0.581		duty cycle 2[6] TH_{Rec}(min)= 0.422 × V_S; TH_{Dom}(min)= 0.284 × V_S; V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus_rec(max)}$/2 t_{bit}; LIN Spec 2.2A (Par. 28)
6.1.56	Duty cycle D2 for V_s supply 6.1 V to 7.6 V (for worst case at 20 kBit/s)	D2	–	–	0.581		duty cycle 2[6] TH_{Rec}(min)= 0.410 × V_S; TH_{Dom}(min)= 0.275 × V_S; 6.1 V < V_S < 7.6 V; t_{bit} = 50 µs; D2 = $t_{bus_rec(max)}$/2 t_{bit};

1) Not subject to production test, specified by design
2) Minimum limit specified by design
3) Maximum limit specified by design
4) $V_{BUS_CNT} = (V_{th_dom} + V_{th\ rec})/2$
5) $V_{HYS} = V_{th_rec} - V_{th_dom}$
6) Bus load concerning LIN Spec 2.2A:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}

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6.2 Diagrams

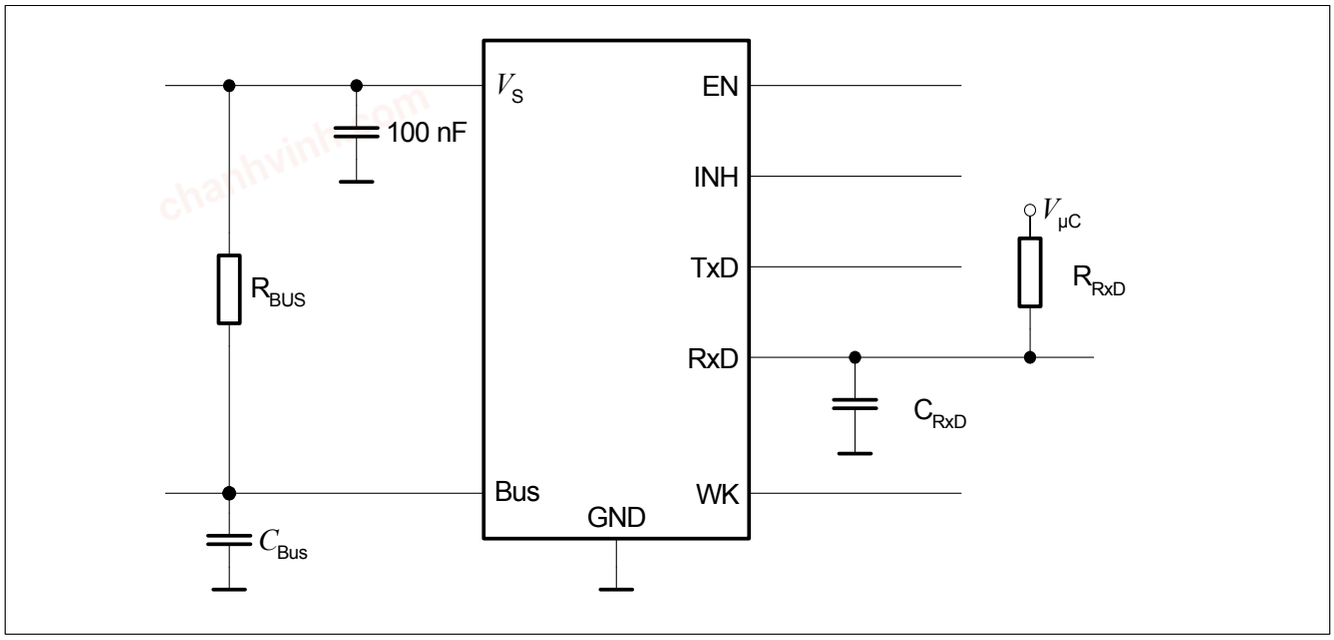


Figure 11 Simplified test circuit for dynamic characteristics

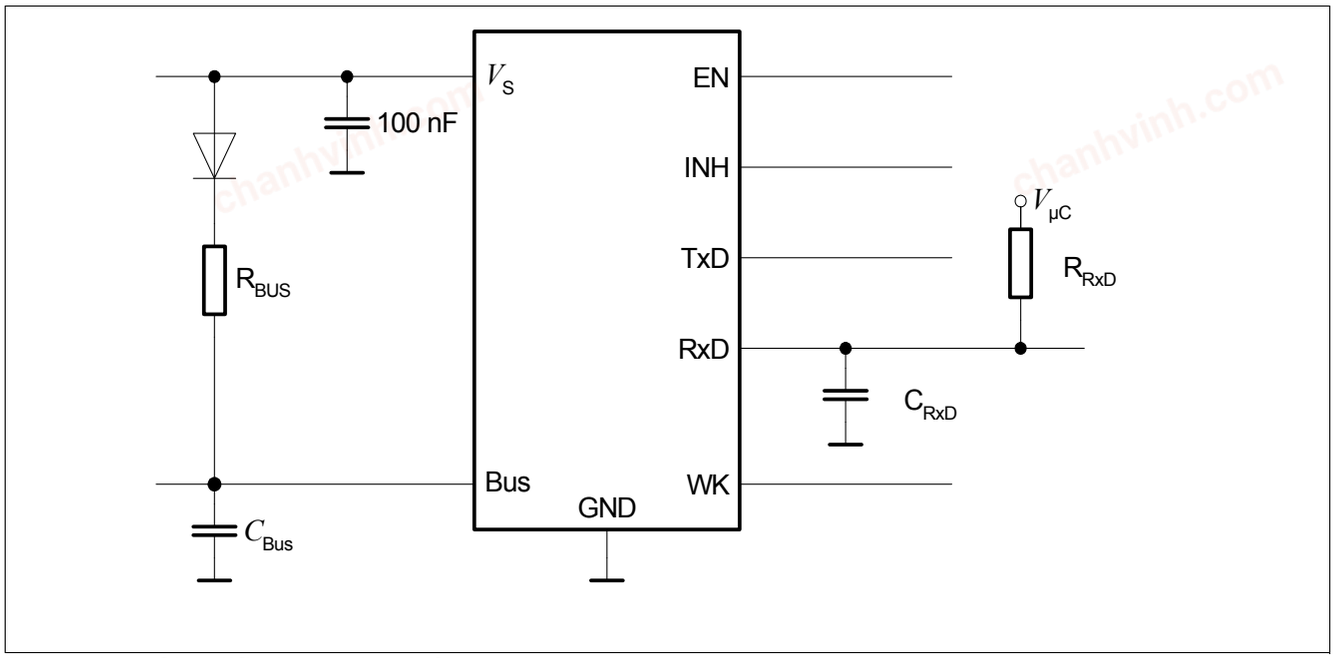


Figure 12 Simplified test circuit for static characteristics

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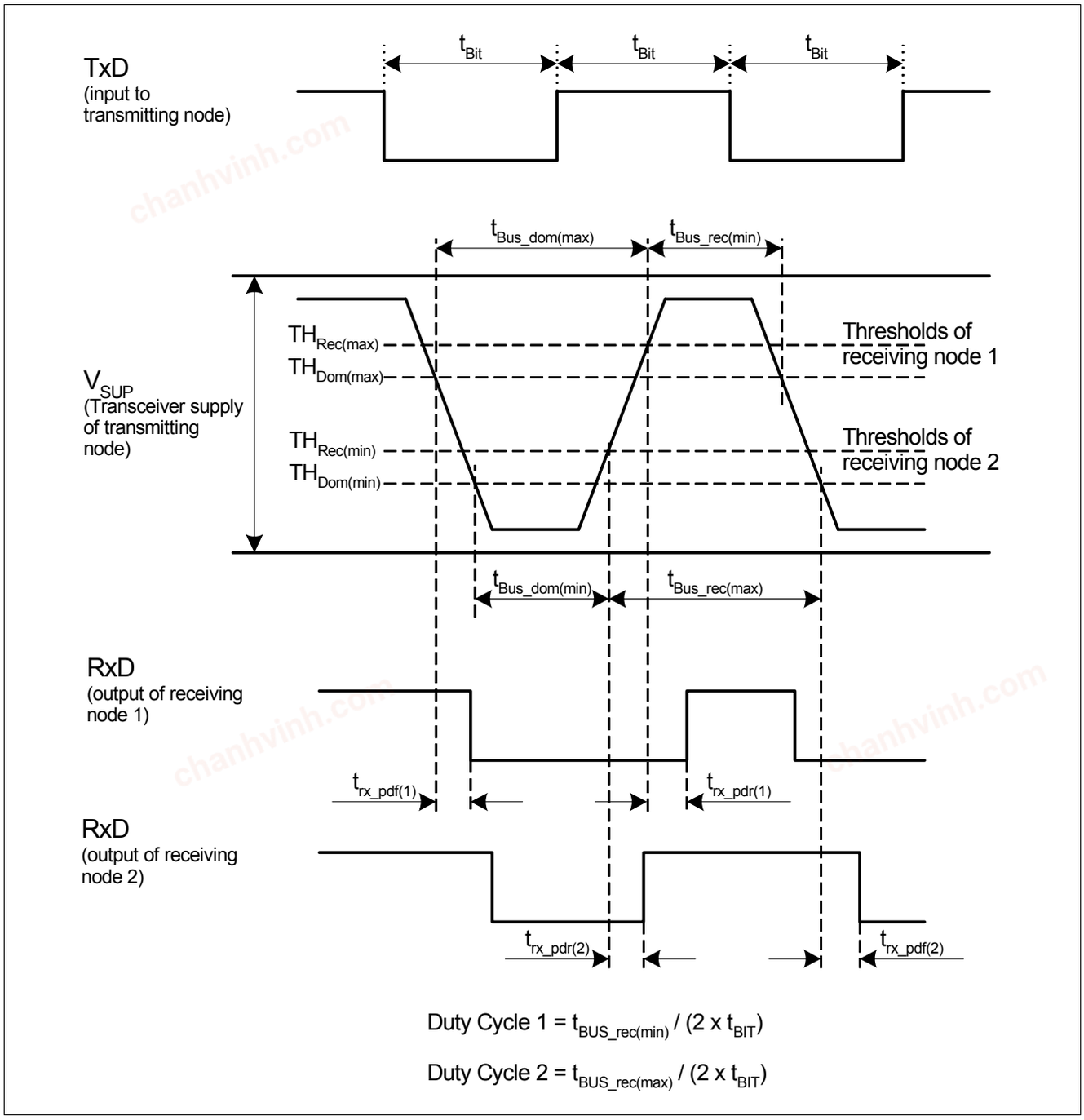


Figure 13 Timing diagram for dynamic characteristics

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7 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

7.1 Compatibility with other Infineon LIN Transceivers

The TLE7259-3 is pin-to-pin compatible with other Infineon LIN transceivers in PG-DSO-8 package (TLE7257SJ and TLE7258SJ) and in PG-TSON-8 package (TLE7257LE, TLE7258D and TLE7258LE). The only differences are the pins named N.C (= Not Connected) which can be left open on the PCB in applications where these functionalities are not needed. The N.C. pins are internally not bonded, so the devices will not be affected if these pins are connected to signals on the application PCB.

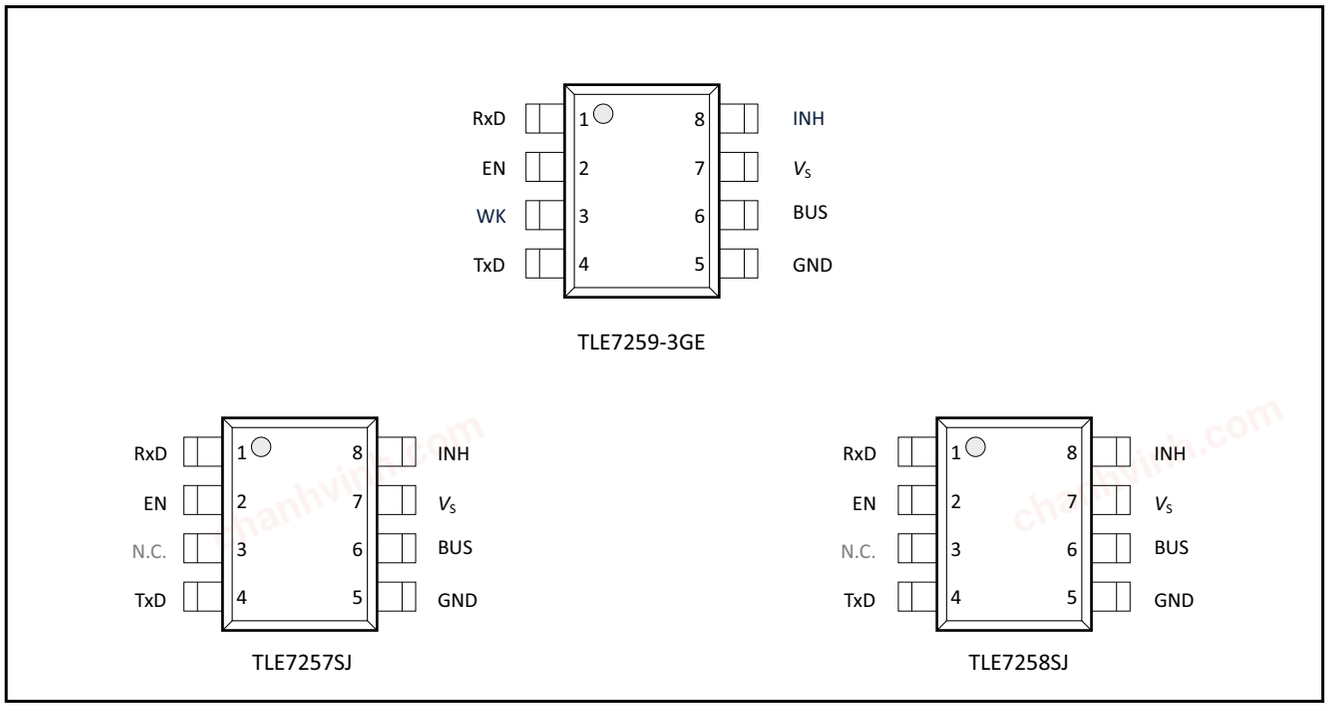


Figure 14 Pin compatibility between TLE7259-3GE, TLE7257SJ and TLE7258SJ

Table 7 Functionality of LIN transceiver family, PG-DSO-8 package

Device	TLE7259-3GE	TLE7257SJ	TLE7258SJ
Applications	High End LIN	Standard LIN Master node	Standard LIN Slave node
Features			
Fast Programming mode	✓	–	–
Local Wake input	✓	–	–
Inhibit output usage	VREG control Master Termination	VREG control	VREG control
TxD Timeout	✓	✓	✓
Power-Up mode	Standby mode	Sleep mode	Standby mode

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The functional difference between the devices in the Infineon LIN transceiver family is summarized in **Table 7** and in **Table 8**. For mode details on the functional and parametric differences, plese refer to the respctive part's datasheet.

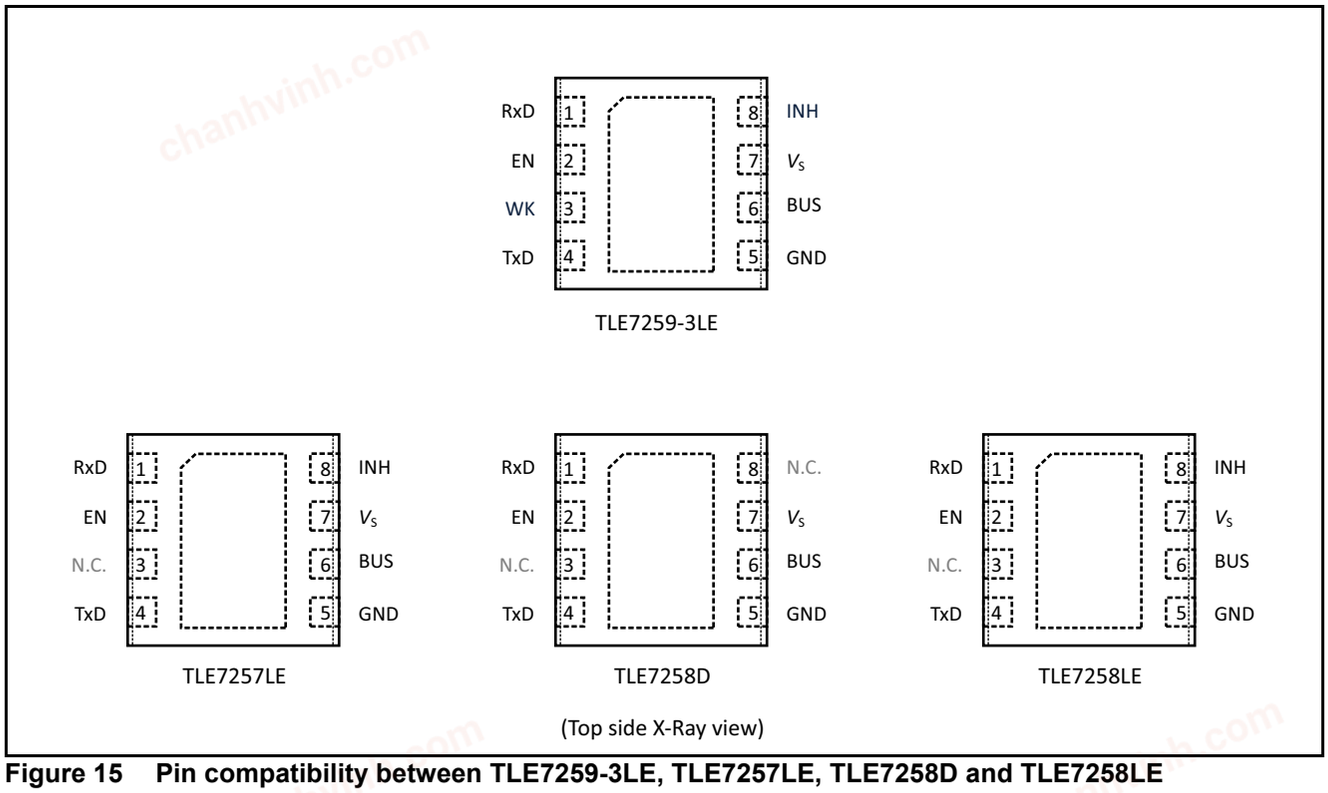


Figure 15 Pin compatibility between TLE7259-3LE, TLE7257LE, TLE7258D and TLE7258LE

Table 8 Functionality of LIN transceiver family, PG-TSON-8 package

Device	TLE7259-3LE	TLE7257LE	TLE7258LE	TLE7258D
Applications	High End LIN	Standard LIN Master node	Standard LIN Slave node	K-Line MOST ECL
Features				
Fast Programming mode	✓	–	–	–
Local Wake input	✓	–	–	–
Inhibit output usage	VREG control Master Termination	VREG control	VREG control	–
TxD Timeout	✓	✓	✓	–
Power-Up mode	Standby mode	Sleep mode	Standby mode	Standby mode

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7.2 ESD Robustness according to IEC61000-4-2

Test for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 9 ESD Robustness according to IEC61000-4-2

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin V_S, BUS versus GND	≥ +15	kV	1)Positive pulse
Electrostatic discharge voltage at pin V_S, BUS versus GND	≤ -15	kV	1)Negative pulse
Electrostatic discharge voltage at pin WK versus GND	≥ +9	kV	1)Positive pulse
Electrostatic discharge voltage at pin WK versus GND	≤ -9	kV	1)Negative pulse

1) ESD susceptibility “ESD GUN” according LIN EMC 1.3 Test Specification, Section 4.3. (IEC 61000-4-2) -Tested by external test house.

7.3 Master Termination

To achieve the required timings for the dominant to recessive transition of the bus signal an additional external termination resistor of 1 kΩ is mandatory. It is recommended to place this resistor at the master node. To avoid reverse currents from the bus line into the battery supply line it is recommended to place a diode in series with the external pull-up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1 nF at the master node (see **Figure 16** and **Figure 17**).The values for the Master Termination resistor and the bus capacitances influence the performance of the LIN network. They depend on the number of nodes inside the LIN network and on the parasitic cable capacitance of the LIN bus wiring.

7.4 External Capacitors

A capacitor of 10 µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting a power down conditions in case of negative transients on the supply line (see **Figure 16** and **Figure 17**).

The 100 nF capacitor close to the V_S pin of the TLE7259-3 is required to get the best EMC performance.

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7.5 Application Example

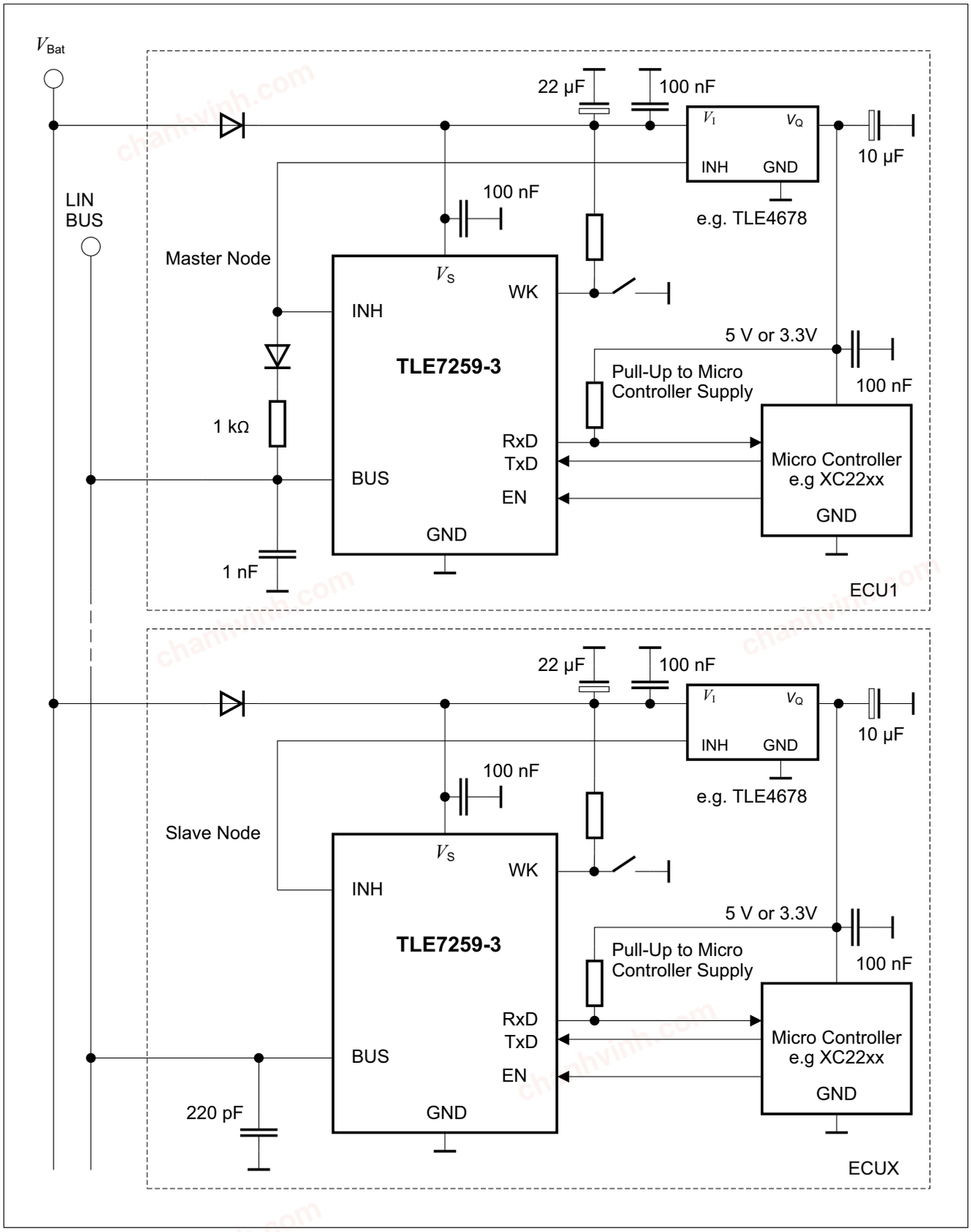


Figure 16 Simplified Application Circuit with Bus Short to GND Feature applied

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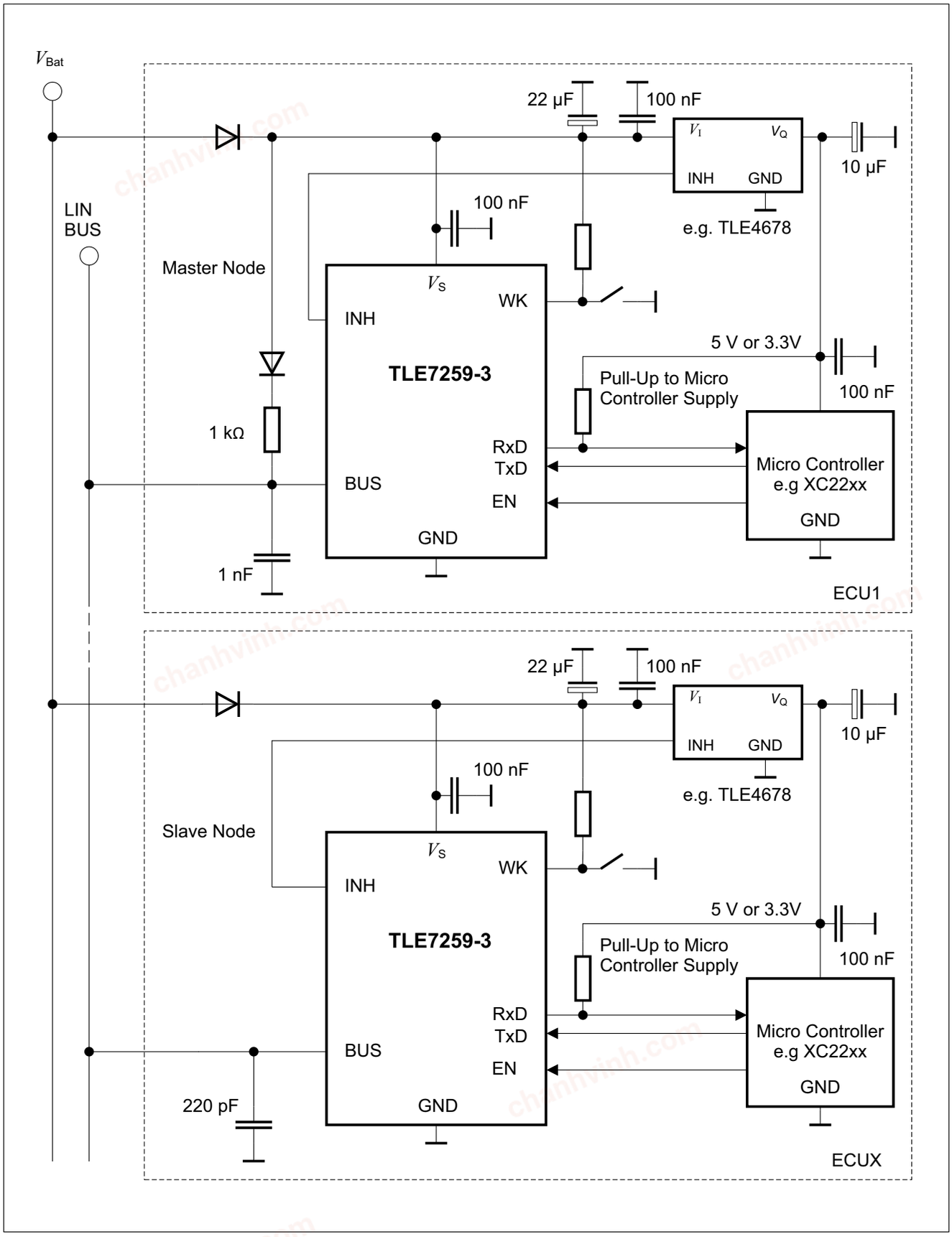
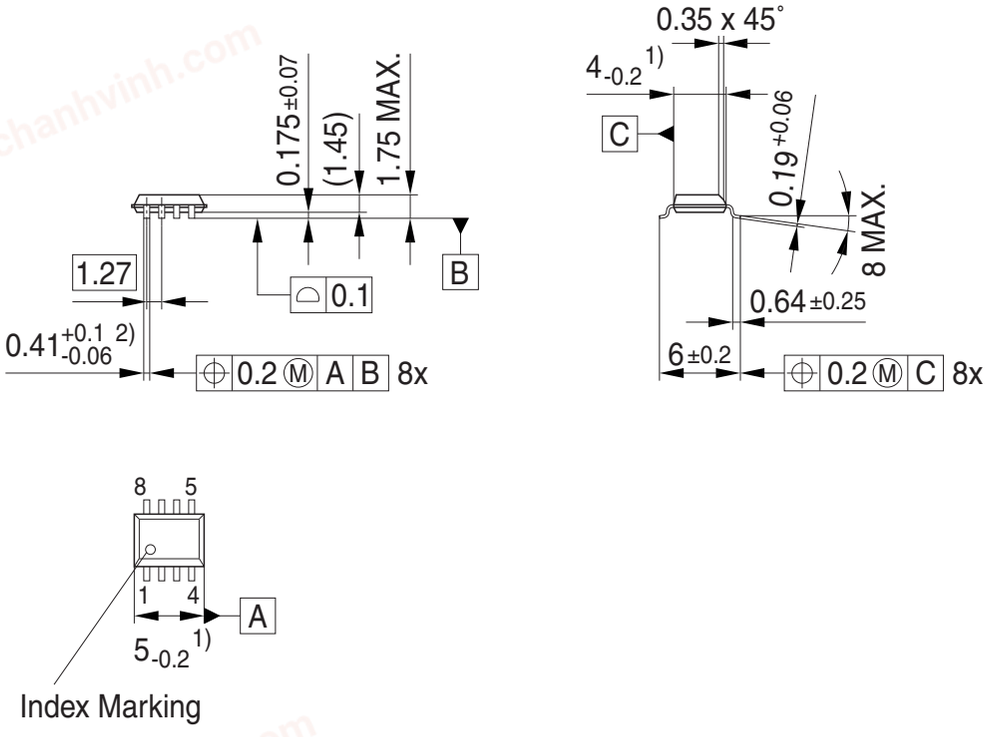


Figure 17 Simplified application Circuit without Bus Short to GND Feature

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8 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

GPS01181

Figure 18 **PG-DSO-8** (Plastic Dual Small Outline PG-DSO-8-16)

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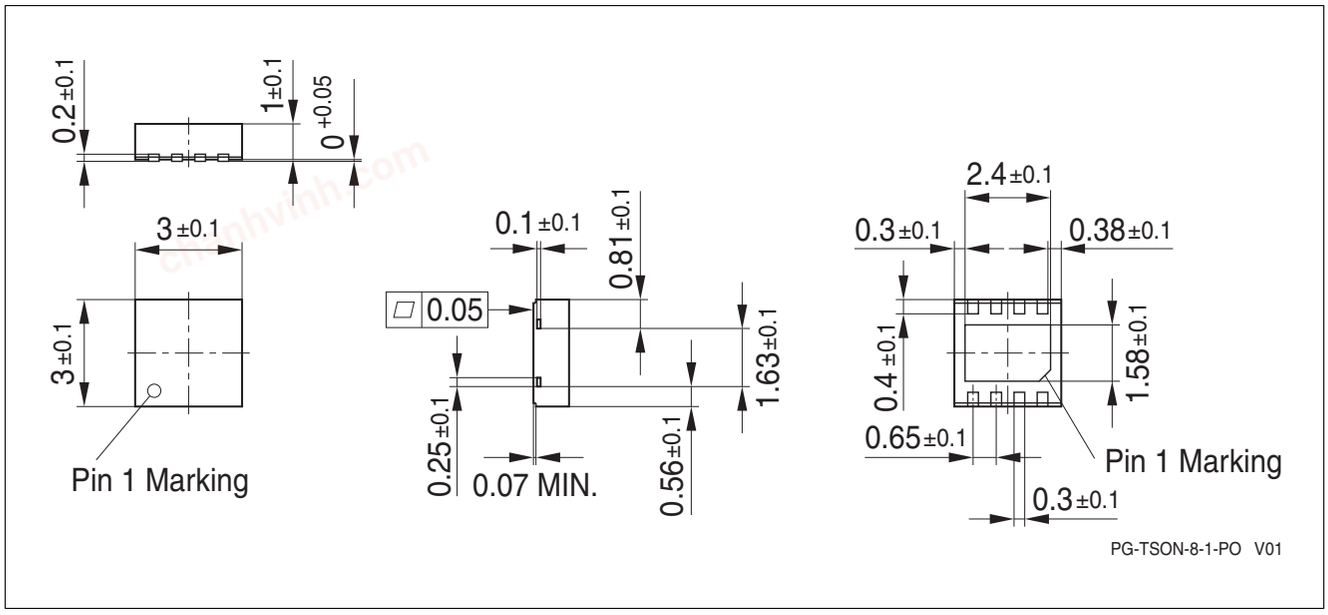


Figure 19 PG-TSON-8 (Plastic Thin Small Outline Nonleaded PG-TSON-8-1)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

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9 Revision History

Revision	Date	Changes
1.0	2013-08-13	Data Sheet created

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