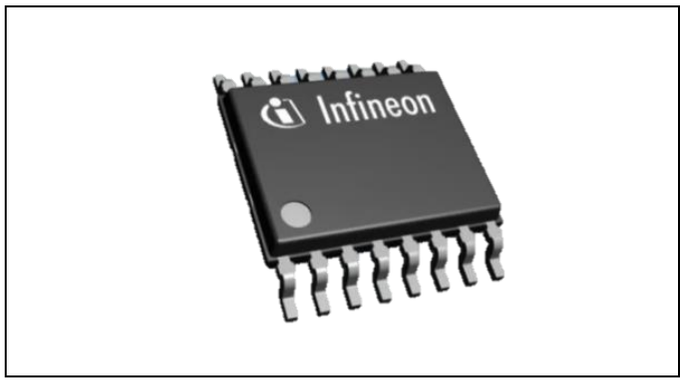
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TLE4972 high precision coreless current sensor for automotive applications

Features & Benefits

- High accurate, scalable, DC & AC current sensing.
- Very low sensitivity error over temperature and lifetime.
- Excellent stability of offset over temperature and lifetime.
- High bandwidth provides fast response time and low phase delay.
- Differential sensor principle ensures superior magnetic stray field suppression.
- Two independent fast Over-Current Detection (OCD) pins with configurable thresholds enable fast protection mechanisms for power circuitry (typical 0.7µs).
- Full scale up to 31 mT for high current applications.
- Small form factor enables low insertion resistance and less power loss.
- Configurable analog output operational modes (fully-differential, semi-differential or single-ended, uni- and bidirectional with or without ratiometricity)
- Supply voltage 3.1 to 3.5V.
- Developed in accordance with ISO 26262 for safety requirements rated up to ASIL B.
- Different package solutions for optimal system integration in different wiring schemes.



TLE4972-AE35D5

Description

TLE4972 is a high precision miniature coreless magnetic current sensor for AC and DC measurements with analog interface and two fast over-current detection outputs.

Infineon's well-established and robust monolithic Hall technology enables accurate and highly linear measurement of the magnetic field caused by currents. With a full scale up to ±31mT it is possible to measure currents up to 2,000 ampere. All negative effects (e.g. saturation, hysteresis) commonly known from open loop sensors using flux concentration techniques are avoided. The sensor is developed in accordance to functional safety standard ISO 26262 and is equipped with internal self-diagnostics.

Typical applications are electrical drives, on board chargers, battery main switches, power supplies, over-load and over-current detection in high voltage applications.

The digitally assisted analog concept of TLE4972 offers superior stability over temperature and lifetime thanks to the Infineon proprietary digital stress and temperature compensation. The differential measurement principle allows great stray field suppression for operation in harsh environments.

The sensor is available in two packages to support a wide range of different system integration scenarios.

Two separate over current detection pins (OCD) provide a fast output signal in case the measurement current exceeds the configured thresholds in typical 0.7µs.

The sensor is shipped as a pre-calibrated product, which provides an accurate performance over temperature and stress. The TLE4972 has in-situ calibration capability to achieve maximum accuracy at the system level.

The high configurability enables customization for a wide variety of applications.

Order Information

Product Name	Product Type	Package	Ordering Number
TLE4972-AE35D5	Current sensor for automotive applications	PG-TDSO-16	SP004914362

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Pin Configuration

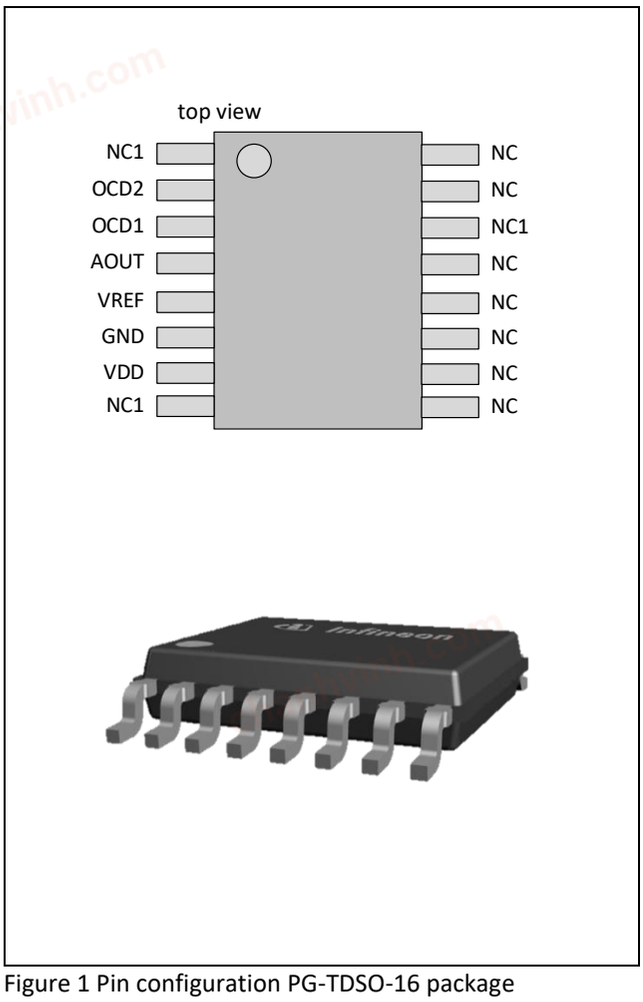


Figure 1 Pin configuration PG-TDSO-16 package

Table 1 Pin configuration PG-TDSO-16 package

Pin No.	Symbol	Function
1[1)]	NC1	Pin shorted with lead frame.
2	OCD2	Over-current detection output 2 (open drain output).
3	OCD1	Over-current detection output 1 (open drain output).
4	AOUT	Analog signal output.
5	VREF	Reference voltage I/O or analog signal output in fully-differential mode.
6	GND	Ground.
7	VDD	Supply voltage.
8[1)]	NC1	Pin shorted with lead frame.
9-13	NC	Not connected with lead frame or sensor.
14[1)]	NC1	Pin shorted with lead frame.
15-16	NC	Not connected with lead frame or sensor.

1) Lead frame shall be connected to GND. Only one pin to be connected to GND to avoid GND loops through the lead frame.

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Standard Product Configuration

Table 2 Standard Product Configuration

Parameter	Symbol	Value / Note
Sensitivity range[1)]	Sx	62mV / mT ±19.35mT FS[2)] S3
Output mode[1)]	OP_{mode}	Semi-differential
Quiescent output voltage[1)]	V_{OQbid_1}	$V_{DD}/2$
Ratiometricity[3)]	Ratio	OFF
OCD1 threshold level[1)4)]	$B_{THR1.x}$	$B_{THR1.2}$ 1.39 x FS
OCD1 deglitch filter setting[1)]	$OCD1_{gl_mul}$	0, filter disabled
OCD2 threshold level[1)4)]	$B_{THR2.x}$	$B_{THR2.4}$ 0.82 x FS
OCD2 deglitch filter setting[1)]	$OCD2_{gl_mul}$	0, filter disabled

1) Can be changed in the EEPROM.
2) FS = Full Scale.
3) Specified accuracy parameters are valid for standard configuration.
Please contact your local Infineon sales office for ratiometricity ON configuration.
Please refer to application note AN_TLE4972_non_default_config for further details.
4) Symmetric threshold level for positive and negative currents.

Target Applications

The TLE4972 is suitable for AC as well as DC current measurement applications:

- Automotive electrical drives
- Auxiliary drives
- Current monitoring
- Overload and over-current detection
- Automotive power train
- Battery main switch
- Electronic power steering
- On board chargers, etc.

With its differential magnetic measurement principle, it is extremely robust when exposed to an external magnetic fields. The device is suitable for fast over-current detection with configurable threshold levels. This allows the control unit to switch off and protect the affected system from damage.

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Block Diagram

The current flowing through an external current rail on the primary side induces a magnetic field that is measured by two Hall probes differentially. The differential measurement principle provides superior magnetic stray field suppression. A high performance amplifier combines the signal resulting from the differential field and the compensation information provided by the temperature and stress compensation unit. Finally, the amplifier output signal is fed into a differential output amplifier which is able to drive the analog output of the sensor.

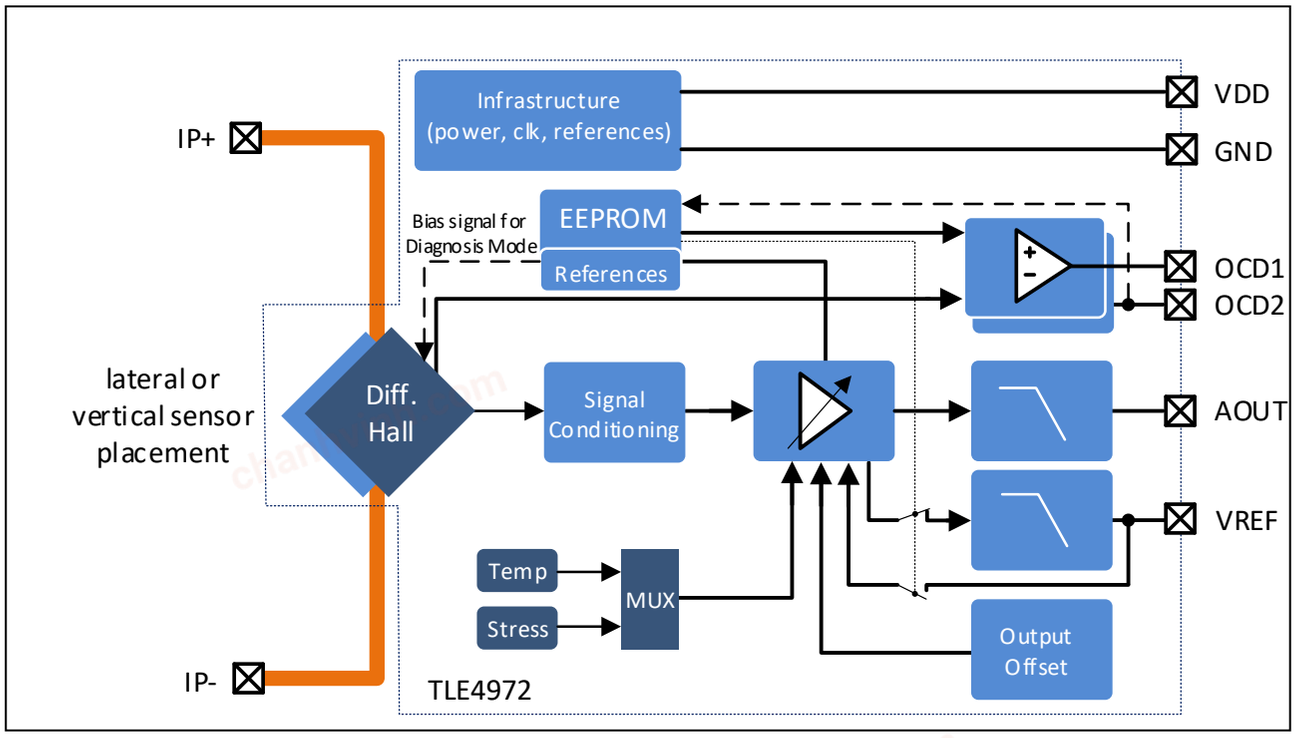


Figure 2 Block diagram

Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Note / Test Condition
Supply voltage	V_{DD}	-0.3	3.3	3.6	V	
Voltage on interface pins VREF, OCD1, AOUT	V_{IO}	-0.3	-	V_{DD} + 0.3	V	
Voltage on Interface Pin OCD2	V_{IO_OCD2}	-0.3	-	21	V	
ESD Voltage	V_{ESD_HBM}	-	-	±2	kV	Human Body Model (HBM), according to standard AEC-Q 100-002
ESD Voltage	V_{ESD_CDM}	-	-	±1	kV	Charged Device Model (CDM), according to AEC – Q100-011
Maximum junction temperature	T_{j_max}	-	-	175	°C	
Storage temperature	T_{A_STORE}	-40	-	150	°C	
Life time	LT	15	-	-	Years	

Stresses above the limit values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

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Product Characteristics

Table 4 Operating Ranges
General conditions (unless otherwise specified): V_{DD} = 3.3V; T_a = -40°C … +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note / Test Condition
Supply voltage	V_{DD}	3.1	3.3	3.5	V	
Ambient temperature	T_a	-40	-	+125	°C	
Operating junction temperature	T_{J_OP}	-40	-	+160	°C	
Capacitance on analog output pins	C_O	4.7	6.8	8	nF	Without series resistor, including parasitic cap on the board.
Reference input voltage	V_{REF_NOM}	-	1.65	-	V	Single-ended mode reference voltage. Other values can be configured in EEPROM: 1.5V, 1.8V. For other values please refer to application note: AN_TLE4972_non_default_config
Reference input voltage variation	V_{REF_var}	-10	-	+10	%	In single-ended mode.
EEPROM programming voltage	V_{IO_PRG}	20.5	20.6	20.7	V	To be applied on OCD2 pin.
Sensitivity calibration range	S_{cal_rng}	-15	-	+15	%	Calibration range available for eol calibration.

Table 5 Operating Parameters
General conditions (unless otherwise specified): V_{DD} = 3.3V; T_a = -40°C … +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note / Test Condition
Current consumption	I_{DD}	-	18	25	mA	I(AOUT) = 0mA
Current consumption during programming[1)]	I_{DD_Prog}	-	-	10	mA	Type tested. Through OCD2 pin
Power-on delay time	t_{POR}	-	-	1.5	ms	From V_{DD} rising above V_{DD}(min) to full operation. Output with lower accuracy is available within 0.5 ms.
Voltage on interface pin OCD1	V_{IO_OCD1}	-0.3	-	3.5	V	
Voltage on interface pin OCD2	V_{IO_OCD2}	-0.3	-	3.5	V	In functional mode
Voltage on analog output AOUT	V_{AOUT}	-0.3	-	V_{DD} + 0.3	V	
Supply undervoltage lockout threshold	U_{VLOH_R}	-	-	2.93	V	V_{DD} at rising edge
Supply undervoltage lockout threshold	U_{VLOH_F}	2.5	-	-	V	V_{DD} at falling edge
Supply overvoltage lockout threshold	O_{VLOH}	3.55	-	-	V	V_{DD} at rising edge
OCD undervoltage detection limit	V_{DD_OCD}	1.8	-	U_{VLOH_R}	V	For V_{DD}<V_{DD_OCD} undervoltage may not be performed.
Undervoltage/overvoltage lockout delay	t_{UVLOe}	1	-	3	µs	Enabled to disabled

1) Not subject to production test – specified by design and characterization.

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Functional Output Description

The analog output signal depends on the following output mode:

- Single-Ended
- Fully-Differential
- Semi-Differential

Single-Ended Output Mode

In single-ended mode, the VREF pin is used as an input pin to provide the analog reference voltage, V_{REF}. The voltage on AOUT, V_{AOUT}, is proportional to the measured current I_{PN} trough the current rail.

Being S the sensitivity and V_{OQ} the quiescent voltage of the sensor, the output voltage can be expressed as:

$$V_{O(IPN)} = V_{OQ} + S \cdot B_{diff}$$

Where B_{diff} is defined as the average differential magnetic field at the Hall probes location:

$$B_{diff} = \frac{(B_{H1} - B_{H2})}{2}$$

The quiescent voltage V_{OQ} is the value of V_{AOUT} when I_{PN}=0. V_{OQ} tracks the voltage on VREF. The quiescent voltage V_{OQ} is ratiometric with respect to the voltage applied on the VREF pin, if the single-ended mode is selected.

$$V_{OQ}(V_{REF}) = V_{REF}$$

The output sensitivity is ratiometric with respect to the reference voltage applied on the VREF pin if the gain ratiometricity is enabled

$$S(V_{REF}) = S(V_{REF_nom}) \cdot \left[1 + \frac{(V_{REF} - V_{REF_nom}) \cdot K_S}{V_{REF_nom}}\right]$$

As K_S = 1 the formula becomes

$$S(V_{REF}) = S(V_{REF_nom}) \cdot \left[\frac{V_{REF}}{V_{REF_nom}}\right]$$

The possible values of nominal V_{REF_nom} are indicated in Table 4.

Fully-Differential Output Mode

In fully-differential mode, both VREF and AOUT are analog outputs with a phase shift of 180° to achieve the double voltage swing.

At zero input current, both AOUT and VREF nominally provide a voltage level of $V_{DD}/2$.

In this case the chip internal reference voltage is derived from the supply pins VDD and GND.

The AOUT and VREF are expressed as follows:

$$V_{AOUT}(I_{PN}) = V_{QAOUT} + S \cdot B_{diff}$$

$$V_{REF}(I_{PN}) = V_{QVREF} - S \cdot B_{diff}$$

In this mode, the nominal quiescent voltage of AOUT (V_{QAOUT}) and VREF (V_{QVREF}) is programmable for 2 different values (see V_{OQBid}). If the nominal quiescent voltage is 1.65V and the offset ratiometricity is enabled the quiescent voltage can be expressed as follows:

$$V_{QAOUT}(V_{DD}) = V_{QVREF}(V_{DD}) =$$

$$= V_{QAOUT}(3.3V)\left[1 + \frac{(V_{DD} - 3.3V) \cdot K_{OQ}}{3.3V}\right]$$

As the nominal value of the ratiometric factor K_{OQ} is 1 the formula becomes:

$$V_{QAOUT}(V_{DD}) = V_{QVREF} = \frac{V_{DD}}{2}$$

The sensitivity as a function of VDD in the fully-differential mode can be generally expressed as follows:

$$S(V_{DD}), diff = S(3.3V), diff \cdot \left[1 + \frac{(V_{DD} - 3.3V) \cdot K_S}{3.3V}\right]$$

As the ratiometric factor K_S = 1, the above formula becomes as follows:

$$S(V_{DD}), diff = S(3.3V), diff \cdot \frac{V_{DD}}{3.3V}$$

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Semi-Differential Output Mode

In semi-differential mode, the sensor is using a chip-internal reference voltage to generate the quiescent voltage that is available on pin VREF (used as output).

The analog measurement result is available as single-ended output signal on AOUT.

The quiescent voltage is programmable at 3 different values, V_{OQbid_1} and V_{OQbid_2} for bidirectional current and V_{OQuni} for unidirectional current (see Table 6). The quiescent voltage on AOUT is nominally equal to the internal reference voltage that is provided as an output on the VREF pin.

The Quiescent Voltage is either set to half of the supply or 1.5V (V_{OQbid}) to measure bidirectional current, whereas the quiescent voltage is set to a lower value (V_{OQuni}) in order to better exploit the full voltage range during the uni-directional current measurement.

The output sensitivity is programmable and ratiometric with respect to V_{DD}, according to the same formula specified for the fully-differential mode, if semi-differential mode is selected and the sensitivity ratiometricity is enabled.

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Analog Output Characteristics

Table 6 Analog Output Characteristics
General conditions (unless otherwise specified): V_{DD} = 3.3V; T_a = -40°C … +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Note / Test conditions
Quiescent output voltage (bidirectional option 1)[1)2)3)]	V_{OQbid_1}	-	$V_{DD}/2$	-	V	Bdiff = 0 T; programmable options in fully-differential or semi-differential[3)] (bidirectional) modes
Quiescent output voltage (bidirectional option 2)[1)]	V_{OQbid_2}	-	1.5	-	V	Bdiff = 0 T; programmable options in fully-differential or semi-differential (bidirectional) modes
Quiescent output voltage (unidirectional mode)[1)]	V_{OQuni}	-	$V_{DD}/5.5$	-	V	Bdiff = 0 T; programmable option in semi-differential mode, unidirectional case.
Analog output saturation voltage	V_{SAT}	-	150	300	mV	$V_{DD} - V_{AOUT}$ Output current = 2 mA
Analog output drive capability	I_O	-2	-	2	mA	DC current
Sensitivity range 1[1)3)]	S1	-	38.75	-	mV/mT	±30.97 mT FS (Full Scale)
Sensitivity range 2[1)3)]	S2	-	46.5	-	mV/mT	±25.81 mT FS
Sensitivity range 3[1)2)3)]	S3	-	62	-	mV/mT	±19.35 mT FS
Sensitivity range 4[1)3)]	S4	-	93	-	mV/mT	±12.9 mT FS
Sensitivity range 5[1)3)]	S5	-	124	-	mV/mT	±9.68 mT FS
Sensitivity range 6[1)3)]	S6	-	186	-	mV/mT	±6.45 mT FS
Sensitivity ratiometry factor	K_S	-	1	-	-	
Quiescent ratiometry factor	K_{OQ}	-	1	-	-	
Transfer function cutoff frequency	BW	120	210	-	kHz	-3dB criterion, C_O= 6.8 nF
Output phase delay[4)]	φ_{delay}	-	43.2	60.5	°	Type tested, f_{signal} = 120 kHz
Output group delay[4)]	ϕ_{gdelay}	-	1	1.4	µs	Type tested
Output group delay variation[4)]	ϕ_{gdelay_v}	-20	-	20	%	Type tested, Over temperature and lifetime
Output noise density[5)6)]	I_{NOISE}	-	90	175	nT/√Hz	Referenced to input differential magnetic field. Typical value is at 25°C, max value is for T_a < 125°C. Higher noise is present at higher temperatures.

1) Can be programmed by user.
2) Pre-configured setting.
3) Values refer to the input differential field Bdiff defined as the average differential magnetic field at the Hall probes nominal location: Bdiff = (BH1 - BH2) / 2. Values are valid for semi-differential mode or single-ended mode, with VREF = 1.65 V. In fully-differential mode the sensitivity value is doubled.
4) Not subject to production test – specified by design, characterization and qualification.
5) Typical value in fully-differential mode, sensitivity range 6.
6) $Noise\ Density = \frac{Output\ Noise\ [V_{RMS}]}{\sqrt{\frac{\pi}{2} * BW[Hz]}} * \frac{1}{Sensitivity\left[\frac{mV}{mT}\right]}$

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Table 6 Analog Output Characteristics (cont'd)

Parameter	Symbol	Min	Typ	Max	Unit	Note / Test conditions
External homogeneous magnetic field suppression[4)]	BSR	34	40	-	dB	Type tested. Frequency up to 4kHz. Up to 20mT homogeneous field applied.
Initial sensitivity error[4)]	E_{SENS}	-5	-	5	%	@ T_a = 25 °C. Initial error can be compensated in application by EOL-calibration at RT.
Sensitivity drift over temperature [4)7)]	E_{SENST}	-1.5	±1	1.5	%	Typical refers to 3σ
Sensitivity drift over temperature and lifetime [4)7)8)]	E_{SENSL}	-1.9	±1.1	1.9	%	Temperature range: 25°C – 125°C
Initial offset error	E_{OFF_init}	-200	-	200	µT	@ T_a = 25 °C. Type tested with standard product configuration. Initial error can be compensated in application by EOL-calibration at RT.
Output offset variation over temperature and lifetime [4)8)]	E_{OFF_L}	-100	±30	100	µT	
Total drift over temperature [4)7)]	E_{TOTT}	-1.6	-	1.6	%	Percentage of FS, range S1. Includes gain, offset, and linearity error. Includes also ratiometricity error if ratiometricity is enabled.
Total drift over temperature and lifetime [4)7)8)]	E_{TOTL}	-2	±1.4	2	%	Percentage of FS, range S1. Includes gain, offset, and linearity error. Temperature range: 25°C – 125°C.

4) Not subject to production test – specified by design, characterization and qualification.
7) Valid for ratiometricity set to OFF (default configuration). Please contact your local Infineon sales office for ratiometricity ON configuration. Please refer to application note AN_TLE4972_non_default_config for further details.
8) Min/Max values derived from AEC-Q100 qualification.
Typical values are ±3 sigma values measured during AEC-Q100 qualification.

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Temperature drift

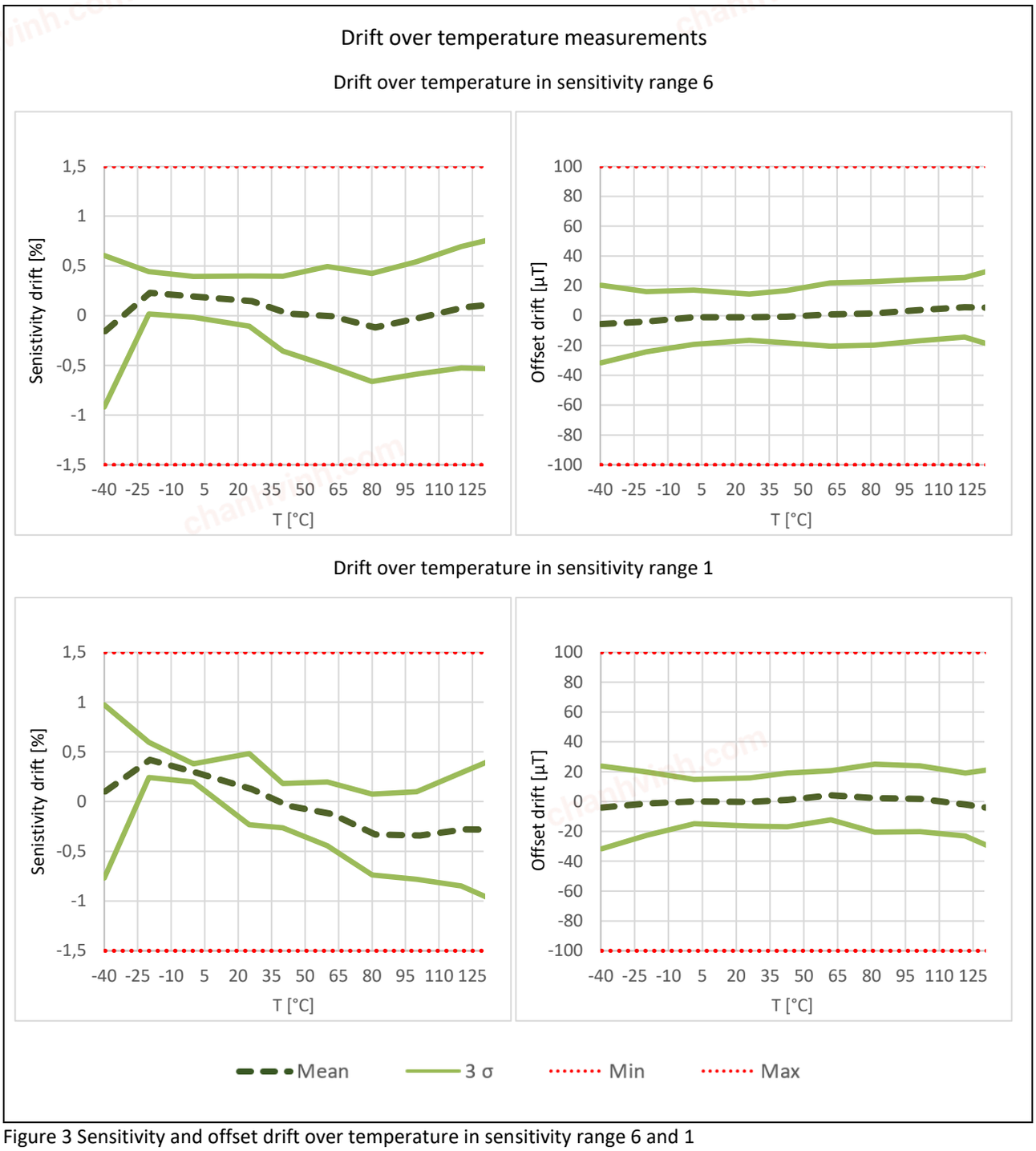


Figure 3 Sensitivity and offset drift over temperature in sensitivity range 6 and 1

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Fast Over Current Detection (OCD)

The Over-Current Detection (OCD) function allows fast detection of over-current events. The raw analog output of the Hall probes is fed directly into comparators with programmable switching thresholds. A user programmable deglitch filter is implemented to avoid false triggering due to fast switching transients. The open-drain OCD pins are active low and can be directly combined into a wired-AND configuration on board level to have a general over-current detection signal. TLE4972 supports two independent programmable OCD outputs, which are suited for different application needs.

The OCD pins are providing a very fast response. The OCD pins can be used as a trap functionality to quickly shut down the current source as well as for precise detection of soft overload conditions.

OCD pins external connection

The OCD pins can be connected to a logic input pin of the microcontroller and/or the pre-driver to quickly react to over-current events. They are designed as open-drain outputs to easily setup a wired-AND configuration and allow monitoring of several current sensors outputs via only one microcontroller pin.

OCD thresholds

The symmetric threshold level of the OCD outputs is adjustable and triggers an over-current event in case of a positive or negative over-current. The possible threshold levels are listed in Table 8 and Table 9.
The instructions for programming the settings will be documented in a separate document called TLE4972 programming guide.

OCD outputs timing behavior

Both output pins feature a deglitch filter to avoid false triggering by noise spikes on the current rail.
Deglitch filter settings can be programmed according to application needs. Available options are listed in Table 8 and Table 9.
The specified deglitching timing is valid when the input current step overtakes the threshold of at least 10%. Figure 4 shows the typical behavior of the OCD output pin during different over-current events.

Over-current Pulse 1: Duration exceeds the over-current response time which is tD_OCDx + response time jitter ΔtD_OCDx + deglitch filter time $t_{deglitch}$. The OCD output voltage is set to low until the current value drops below the OCD threshold.

Over-current Pulse 2: duration does not exceed the over-current response time tD_OCDx and therefore no OCD event is generated.

Over-current Pulse 3: duration exceeds the response time tD_OCDx + response time jitter ΔtD_OCDx, but does not exceed the glitch filter time $t_{deglitch}$ and no OCD event is generated.

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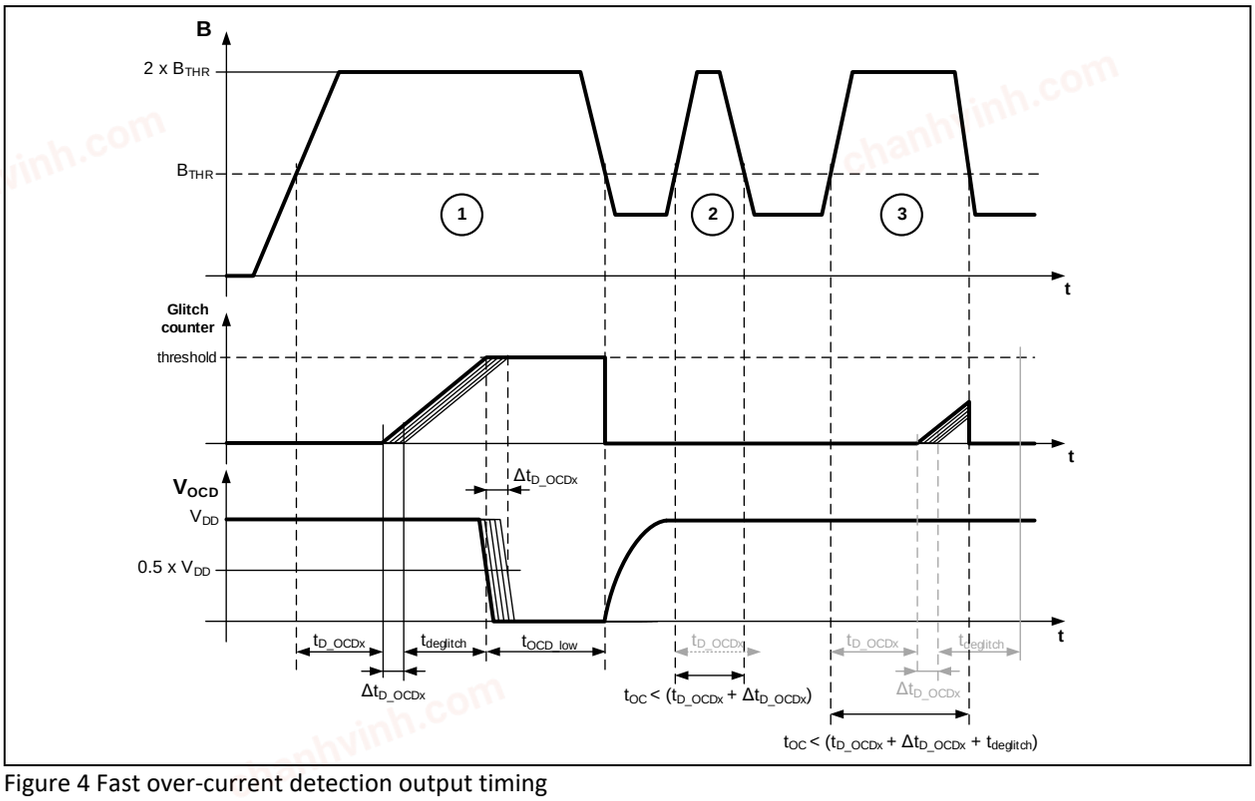


Figure 4 Fast over-current detection output timing

Fast Over-Current Detection (OCD) Output Parameters

Table 7 Common OCD Parameters

General conditions (unless otherwise specified): V_{DD} = 3.3V; T_a = -40°C … +125°C,
All OCD timing related requirements refer to the maximum load capacitance specified.

Parameter	Symbol	Min	Typ	Max	Unit	Note / Test Conditions
Threshold level tolerance[1)]	I_{THT}	-10	-	10	%	Type tested
Response time jitter[1)]	Δt_{D_OCDx}	-	-	0.11	µs	1σ, type tested B = 2 x BTHR, input rise time 0.5us
Deglitch filter basic time	t_{OCDgl}	400	500	600	ns	Basic time for deglitching filter setting $OCDx_{gl_mul}$
Load capacitance	C_L	-	-	1	nF	
Open-drain current	I_{OD_ON}	-	-	1	mA	DC current
Pull-up resistor	R_{PU}	-	4.7	10	kΩ	To V_{DD}

1) Not subject to production test – specified by design, characterization and qualification.

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Table 8 OCD1 Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Note / Test Conditions
Threshold level 1[1)2)]	$B_{THR1.1}$	-	1.25	-	-	Factor with respect to FS (Full Scale)
Threshold level 2[1)2)3)]	$B_{THR1.2}$	-	1.39	-	-	Factor with respect to FS
Threshold level 3[1)2)]	$B_{THR1.3}$	-	1.54	-	-	Factor with respect to FS
Threshold level 4[1)2)]	$B_{THR1.4}$	-	1.68	-	-	Factor with respect to FS
Threshold level 5[1)2)]	$B_{THR1.5}$	-	1.82	-	-	Factor with respect to FS
Threshold level 6[1)2)]	$B_{THR1.6}$	-	1.96	-	-	Factor with respect to FS
Threshold level 7[1)2)]	$B_{THR1.7}$	-	2.11	-	-	Factor with respect to FS
Threshold level 8[1)2)]	$B_{THR1.8}$	-	2.25	-	-	Factor with respect to FS
Response time[4)]	t_{D_OCD1}	-	0.7	1	µs	$B_{diff_Hall} = 2 \times B_{THR}$
Fall time[5)]	t_{f_OCD1}	-	100	150	ns	Type tested
Deglitch filter setting[2)6)]	$OCD1_{gl_mul}$	0	-	7	-	$t_{deglitch} = OCD1_{gl_mul} * t_{OCDgl}$ pre-configured setting = 0
Threshold level setting[2)]	$OCD1_{THRLVL}$	0	-	63	-	

1) Symmetric threshold level for positive and negative currents.
2) Can be programmed by user. Intermediate threshold levels can be set according the formulas below. Further detail to be found at Application note AN_TLE4972_Calibration.
3) Pre-configured threshold.
4) Falling edge level of OCD1-pin < 0.5 x V_{DD}.
5) Not subject to production test – specified by design and characterization.
6) The specified deglitching timing is valid when input current step overtakes the threshold of at least 10%.

$$Threshold\ level\ OCD1\ [A]_{S1\ to\ S3} = \frac{\left((OCD1_{THRLVL}[LSB6] \cdot 1.6493) + 10.356\right) \cdot 1000}{Current\ rail\ transfer\ factor\ [\frac{\mu T}{A}]} + offset\ [A]$$

$$Threshold\ level\ OCD1\ [A]_{S4\ to\ S6} = \frac{\left((OCD1_{THRLVL}[LSB6] \cdot 0.6313) + 3.6305\right) \cdot 1000}{Current\ rail\ transfer\ factor\ [\frac{\mu T}{A}]} + offset\ [A]$$

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Table 9 OCD2 Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Note / Test Conditions
Threshold level 1[1)2)]	$B_{THR2.1}$	-	0.5	-	-	Factor with respect to FS
Threshold level 2[1)2)]	$B_{THR2.2}$	-	0.61	-	-	Factor with respect to FS
Threshold level 3[1)2)]	$B_{THR2.3}$	-	0.71	-	-	Factor with respect to FS
Threshold level 4[1)2)3)]	$B_{THR2.4}$	-	0.82	-	-	Factor with respect to FS
Threshold level 5[1)2)]	$B_{THR2.5}$	-	0.93	-	-	Factor with respect to FS
Threshold level 6[1)2)]	$B_{THR2.6}$	-	1.04	-	-	Factor with respect to FS
Threshold level 7[1)2)]	$B_{THR2.7}$	-	1.14	-	-	Factor with respect to FS
Threshold level 8[1)2)]	$B_{THR2.8}$	-	1.25	-	-	Factor with respect to FS
Response time[4)]	t_{D_OCD2}	-	0.7	1.2	µs	B_{diff_Hall} = 2 x B_{THR}
Fall time[5)]	t_{f_OCD2}	-	200	300	ns	Type tested
Deglitch filter setting[2)6)]	$OCD2_{gl_mul}$	0	-	15	-	$t_{deglitch}$ = $OCD2_{gl_mul}$*t_{OCDgl} pre-configured setting = 0
Threshold level setting[2)]	$OCD2_{THRLVL}$	0	-	63	-	

1) Symmetric threshold level for positive and negative currents.
2) Can be programmed by user. Intermediate threshold levels can be set according the formulas below. Further detail to be found at Application note AN_TLE4972_Calibration.
3) Pre-configured threshold.
4) Falling edge level of OCD2-pin < 0.5 x V_{DD}.
5) Not subject to production test – specified by design and characterization.
6) The specified deglitching timing is valid when input current step overtakes the threshold of at least 10%.

$$Threshold\ level\ OCD2\ [A]_{S1\ to\ S3} = \frac{\left((OCD2_{THRLVL}[LSB6] \cdot 0.7989) + 4.6475\right) \cdot 1000}{Current\ rail\ transfer\ factor\ \left[\frac{\mu T}{A}\right]} + offset\ [A]$$

$$Threshold\ level\ OCD2\ [A]_{S4\ to\ S6} = \frac{\left((OCD2_{THRLVL}[LSB6] \cdot 0.3156) + 1.6584\right) \cdot 1000}{Current\ rail\ transfer\ factor\ [\frac{\mu T}{A}]} + offset\ [A]$$

Undervoltage / Overvoltage detection

TLE4972 is able to detect undervoltage and overvoltage condition of its own power supply (V_{DD}). When an undervoltage (V_{DD}<U_{VLOH}) or overvoltage (V_{DD}>O_{VLOH}) condition is detected both OCD pins are pulled down in order to provide a fault condition.
The undervoltage detection on OCD pins is performed only if V_{DD} > V_{DD_OCD}.

Both OCD pins are pulled down at start up. When V_{DD} exceeds the undervoltage threshold U_{VLOH_R} and the power on delay time t_{POR} has been reached, the sensor indicates the correct functionality and high accuracy by releasing the OCD pins.

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System integration

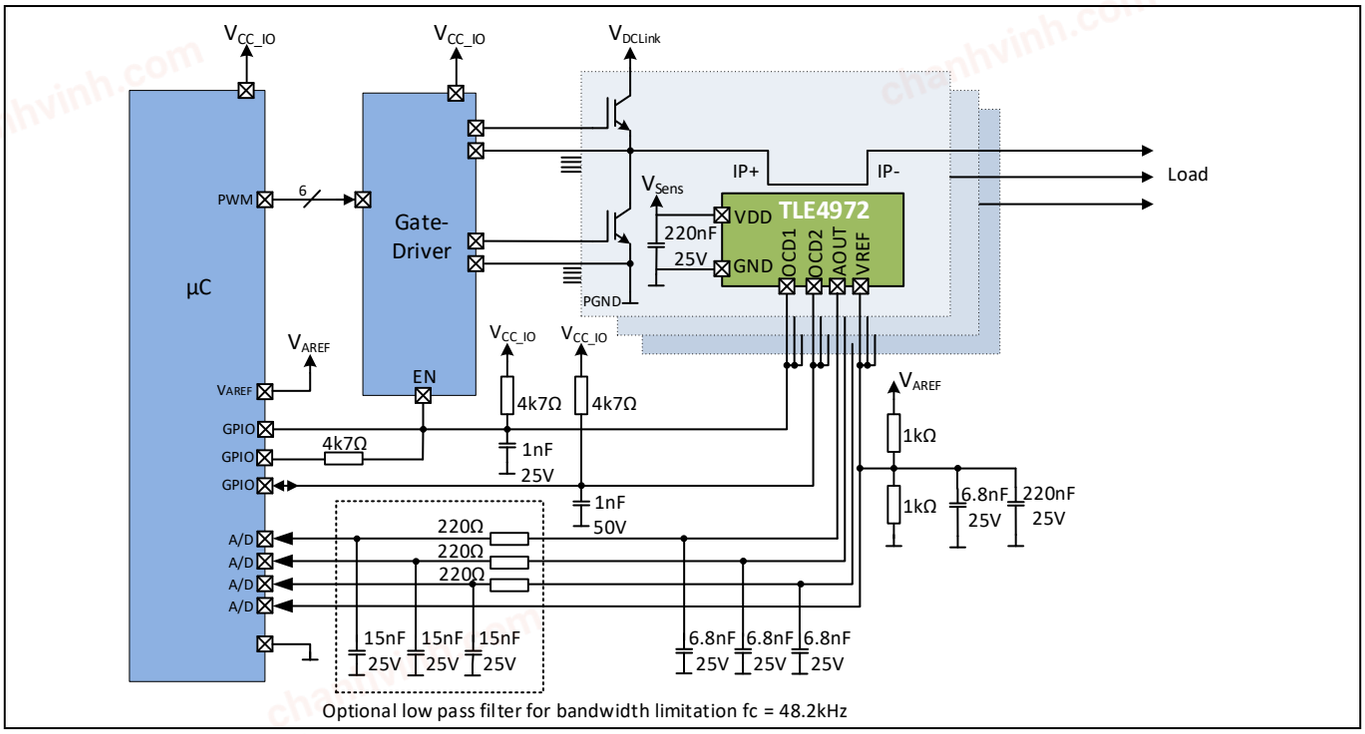


Figure 5 Application circuit for three phase system in single-ended mode.

Note:
In order to protect the OCD1 pin against over voltage while programming the EEPROM, the OCD1 and OCD2 pin shall not be shorted together.

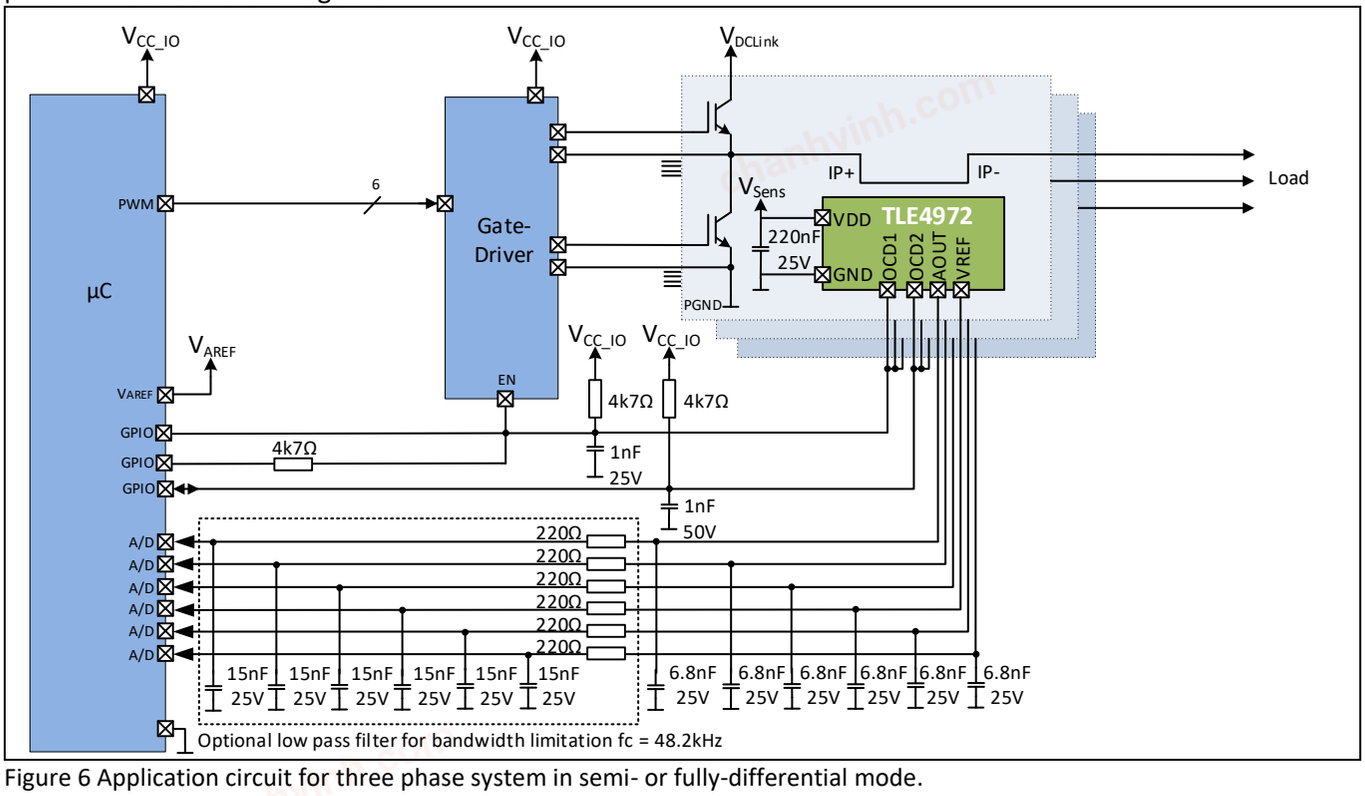


Figure 6 Application circuit for three phase system in semi- or fully-differential mode.

Note:
In order to protect the OCD1 pin against over voltage while programming the EEPROM, the OCD1 and OCD2 pin shall not be shorted together.

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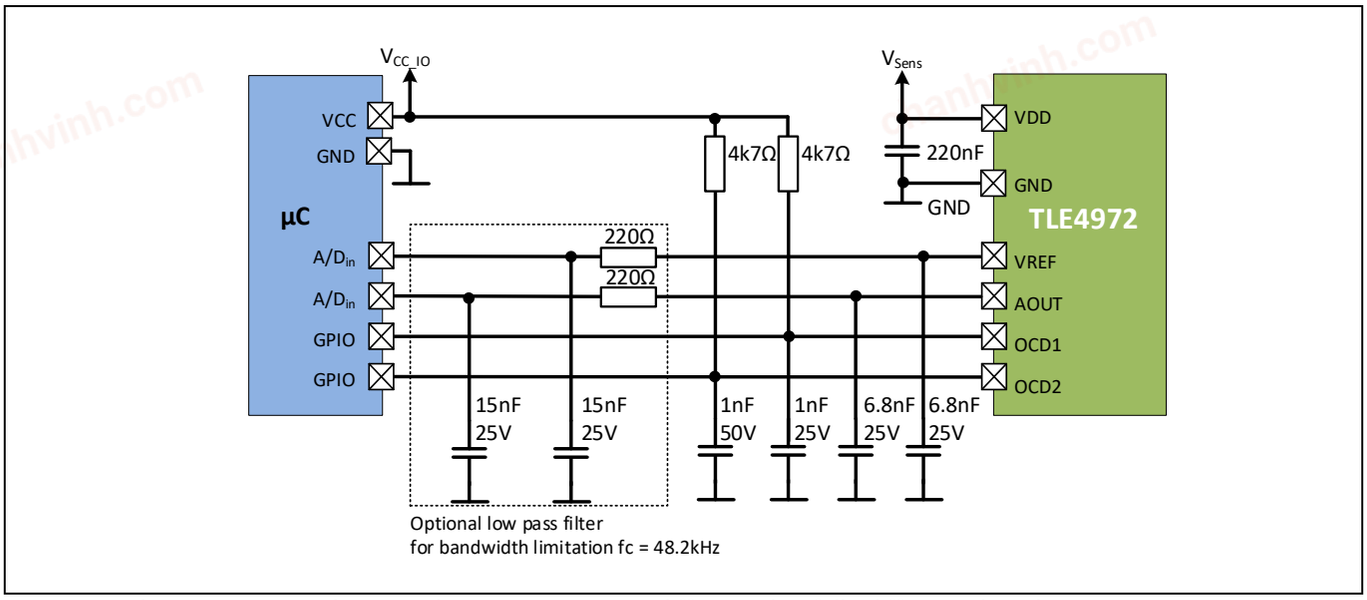


Figure 7 Application circuit with external components. Semi-differential or fully-differential mode.

Package Outline

The TLE4972 is available in two RoHS compliant, halogen-free packages.

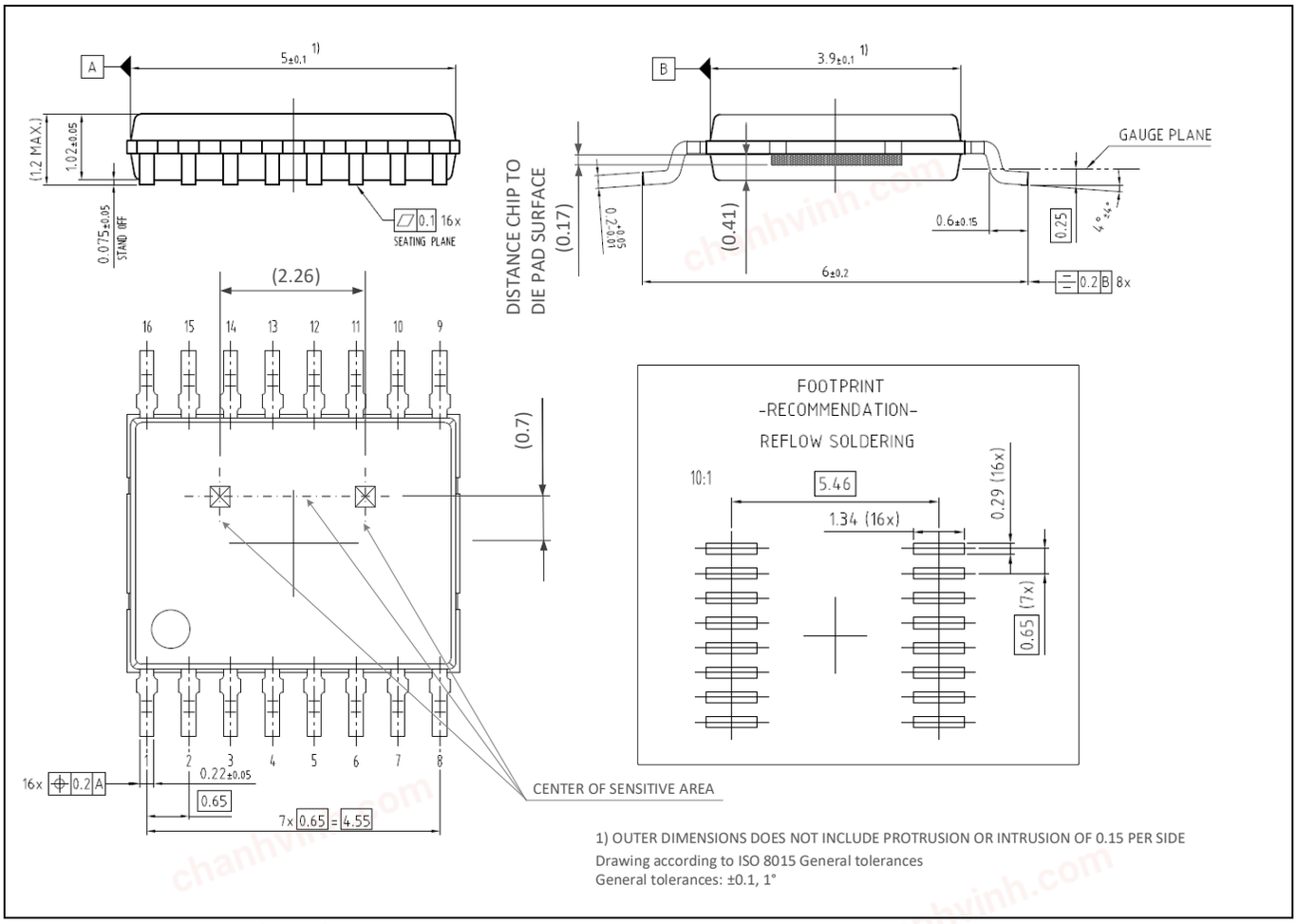


Figure 8 PG-TDSO-16 package dimensions.

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Sensing principle, polarity description

The TLE4972 coreless magnetic current sensor measures the differential magnetic field caused by a current flowing in an external conductor. The below figure shows that the magnetic field $+B_{IPN}$ and $-B_{IPN}$ at the sensor's Hall cell position is depending on the current I_{PN}. Being S the sensitivity and V_{OQ} the quiescent voltage of the sensor, the output voltage as function of the magnetic field is expressed as follows:

$$V_{O(IPN)} = V_{OQ} + S \cdot B_{diff}$$

Where B_{diff} is defined as the average differential magnetic field at the Hall probes location.

$$B_{diff} = \frac{((+B_{IPN}) - (-B_{IPN}))}{2}$$

The below figure shows the package orientation relative to the current direction. If the current I_{PN} is flowing according to the direction shown in the below figure then the sensor provides an output voltage $V_{O(IPN)}$ in respect to the polarity of the input current I_{PN}, otherwise the sensor provides an inverted output voltage $V_{O(IPN)}$ in respect to the polarity of the input current I_{PN}.

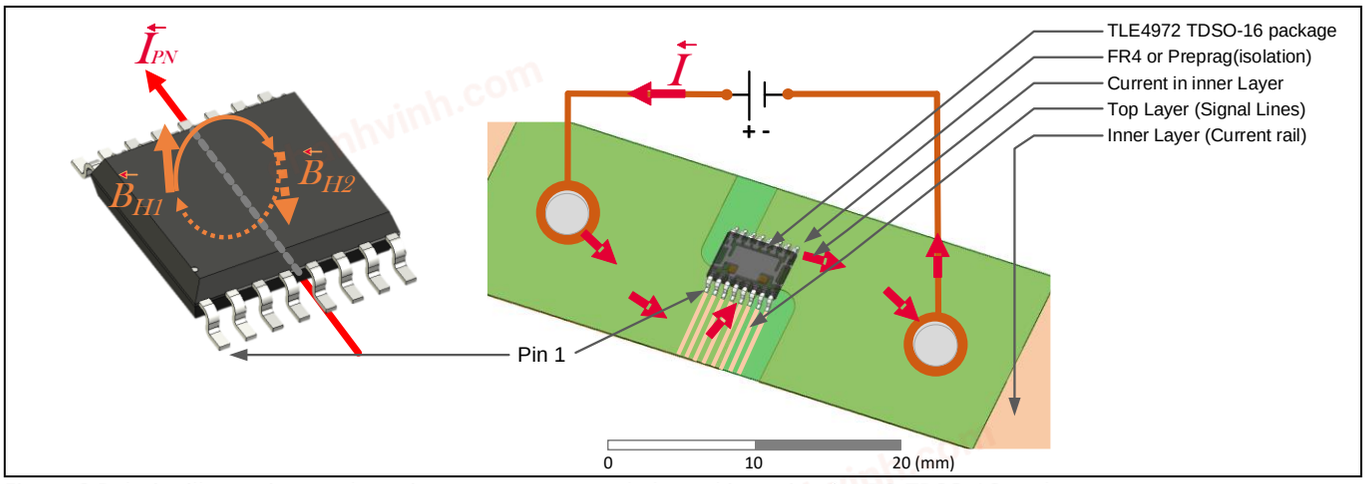


Figure 9 Polarity illustration, and sensing structure example lateral insertion for PG-TDSO-16 package.

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Revision History

Major changes since the last revision

Revision number	Date of release	Description of change
1.00	24-08-2021	Initial release
1.01	29-09-2021	• Typical value of I_{DD} updated (page 6) • Table of contents added (page 4) • Trademark section in the final page updated • Typos and formatting issues corrected

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