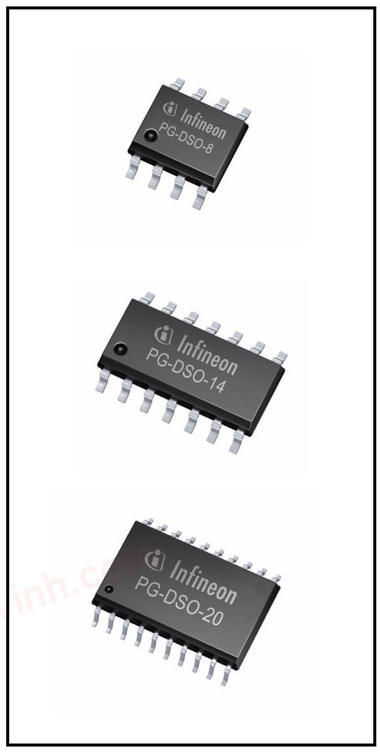
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OPTIREG™ Linear TLE4269

5 V low drop fixed voltage regulator

AEC Qualified RoHS



Features

- Output voltage tolerance ≤ ±2%
- 150 mA current capability
- Very low current consumption
- Early warning
- Reset output low down to V_Q = 1 V
- Overtemperature protection
- Reverse polarity proof
- Adjustable reset threshold
- Very low drop voltage
- Wide temperature range
- Integrated pull-up resistor at logic outputs
- Green Product (RoHS compliant)

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The OPTIREG™ Linear TLE4269 is an automotive voltage regulator with a 5 V fixed output. The maximum operating voltage is 45 V. The output is able to drive 150 mA load. The device features short-circuit protection. The thermal shutdown feature switches the output off when the junction temperature exceeds 150°C to ensure the device is not damaged by overheating. A reset signal is generated when the output voltage drops below V_Q < 4.65 V. The reset threshold voltage can be decreased by an external connection of a voltage divider. The reset delay time can be set by an external capacitor. Reset and sense output have integrated pull-up resistors. If the integrated resistors are not required, the TLE4279 can be used instead. It is also possible to supervise the input voltage by using an integrated comparator to give a low voltage warning.

Type	Package	Marking
TLE4269G	PG-DSO-8	TLE 4269
TLE4269GM	PG-DSO-14	TLE 4269
TLE4269GL	PG-DSO-20	TLE 4269

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Table of contents

Features **1**
Potential applications **1**
Product validation **1**
Description **1**
Table of contents **2**
1 Block diagram **3**
2 Pin configuration **4**
3 General product characteristics **7**
3.1 Absolute maximum ratings 7
3.2 Electrical characteristics 9
4 Functional description **10**
5 Application information **11**
5.1 Application diagram 11
5.2 Typical performance characteristics 13
6 Package information **16**
7 Revision history **18**

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1 Block diagram

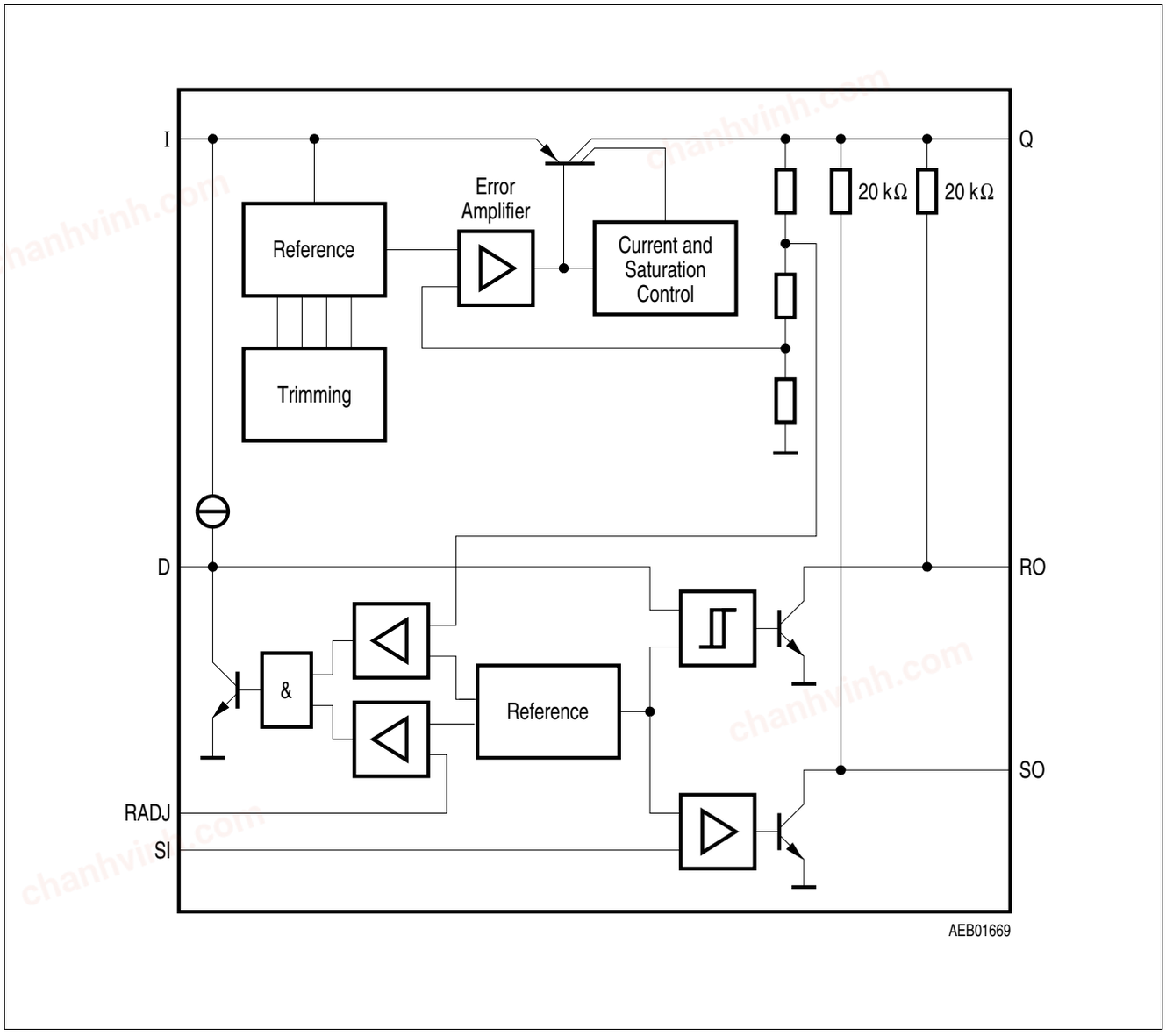


Figure 1 Block diagram

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2 Pin configuration

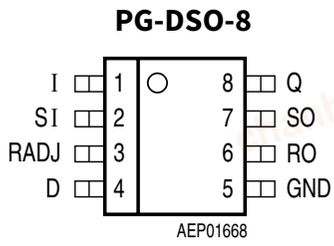


Figure 2 **Pin configuration** PG-DSO-8 (top view)

Table 1 **Pin definitions and functions (TLE4269G)**

Pin No.	Symbol	Function
1	I	**Input** connected with a ceramic capacitor to GND directly at the IC.
2	SI	**Sense input** if not needed connect to Q.
3	RADJ	**Reset threshold adjust** if not needed connect to GND.
4	D	**Reset delay** to select delay time, connect to GND via capacitor.
5	GND	**Ground**
6	RO	**Reset output** the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the reset function is not needed
7	SO	**Sense output** the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the sense comparator is not needed.
8	Q	**5 V output** connect to GND with a 10 µF capacitor, ESR < 10 Ω

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Pin configuration

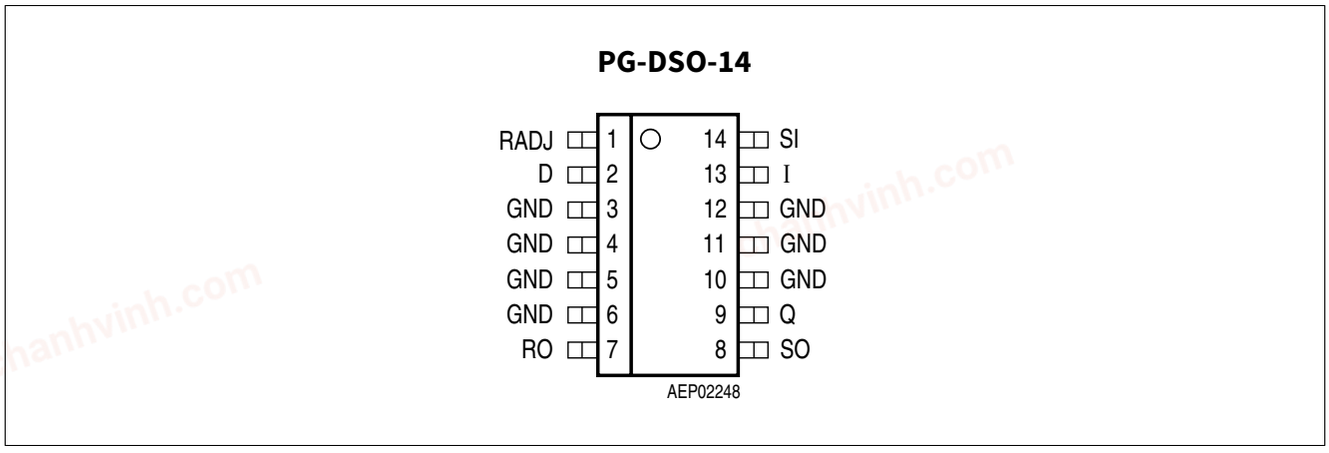


Figure 3 **Pin configuration** PG-DSO-14 (top view)

Table 2 **Pin definitions and functions (TLE4269GM)**

Pin No.	Symbol	Function
1	RADJ	**Reset threshold adjust** if not needed connect to GND.
2	D	**Reset delay** to select delay time; connect to GND via capacitor.
3, 4, 5, 6	GND	**Ground**
7	RO	**Reset output** the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the reset function is not needed
8	SO	**Sense output** the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the sense comparator is not needed.
9	Q	**5 V Output** connect to GND with a 10 µF capacitor, ESR < 10 Ω.
10, 11, 12	GND	**Ground**
13	I	**Input** connected with a ceramic capacitor to GND directly at the IC.
14	SI	**Sense input** if not needed connect to Q.

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Pin configuration

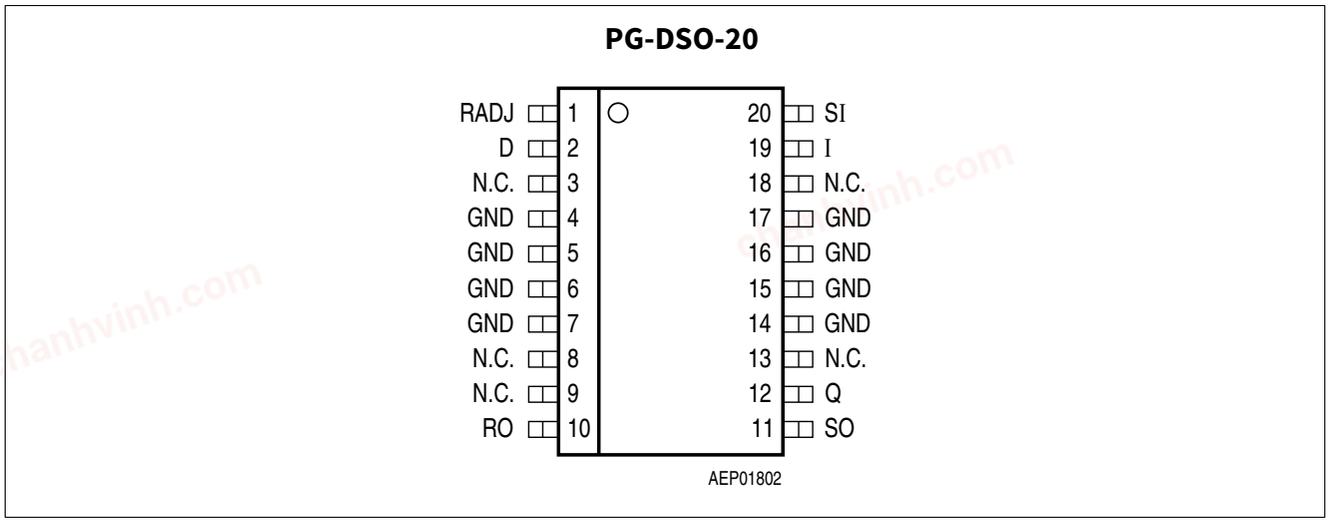


Figure 4 **Pin configuration** PG-DSO-20 (top view)

Table 3 **Pin definitions and functions (TLE4269GL)**

Pin No.	Symbol	Function
1	RADJ	**Reset threshold adjust** if not needed connect to ground.
2	D	**Reset delay** to select delay time, connect to GND via external capacitor.
4 - 7, 14 - 17	GND	**Ground**
10	RO	**Reset output** the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the reset function is not needed
11	SO	**Sense output** the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the sense comparator is not needed.
12	Q	**Output** connect to GND with a 10 µF capacitor, ESR < 10 Ω.
19	I	**Input** connected with a ceramic capacitor to GND directly at the IC.
20	SI	**Sense input** if not needed connect to Q.

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3 General product characteristics

3.1 Absolute maximum ratings

Table 4 Absolute maximum ratings

T_j = -40°C to 150°C

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input						
Input voltage	V_I	-40	–	45	V	–
Input current	I_I	–	–	–	–	Internal limited
Sense input						
Input voltage	V_{SI}	-40	–	45	V	–
Input current	I_{SI}	1	–	1	mA	–
Reset threshold						
Voltage	V_{RADJ}	-0.3	–	7	V	–
Current	I_{RADJ}	-10	–	10	mA	–
Reset delay						
Voltage	V_D	-0.3	–	7	V	–
Current	I_D	–	–	–	–	Internal limited
Ground						
Current	I_{GND}	50	–	–	mA	–
Reset output						
Voltage	V_R	-0.3	–	7	V	–
Current	I_R	–	–	–	–	Internal limited
Sense output						
Voltage	V_{SO}	-0.3	–	7	V	–
Current	I_{SO}	–	–	–	–	Internal limited
5 V output						
Output voltage	V_Q	-0.5	–	7	V	–
Output current	I_Q	-10	–	–	mA	–
Temperature						
Junction temperature	T_j	–	–	150	°C	–
Storage temperature	T_{Stg}	-50	–	150	°C	–
Operating range						
Input voltage	V_I	–	–	45	V	–
Junction temperature	T_j	-40	–	150	°C	–

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Table 4 Absolute maximum ratings (cont'd)

T_j = -40°C to 150°C

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal data						
Junction-ambient	R_{thja}	–	–	200	K/W	PG-DSO-8
		–		70	K/W	PG-DSO-14
		–		70	K/W	PG-DSO-20
Junction-pin	R_{thjp}	–	–	30	K/W	PG-DSO-8[1)]
		–		30	K/W	PG-DSO-14[2)]
				30	K/W	PG-DSO-20[2)]

1) Measured to pin 5.

2) Measured to pin 4.

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3.2 Electrical characteristics

Table 5 Electrical characteristics

V_I = 13.5 V; -40°C ≤ T_j ≤ 125°C

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output voltage	V_Q	4.90	5.00	5.10	V	1 mA ≤ I_Q ≤ 100 mA, 6 V ≤ V_I ≤ 16 V
Current limit	I_Q	150	200	500	mA	–
Current consumption; $I_q = I_I - I_Q$	I_q	–	240	300	µA	I_Q ≤ 1 mA, T_j < 85°C
Current consumption; $I_q = I_I - I_Q$	I_q	–	250	700	µA	I_Q = 10 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	2	8	mA	I_Q = 50 mA
Drop voltage	V_{dr}	–	0.25	0.5	V	I_Q = 100 mA[1]
Load regulation	ΔV_Q	–	10	30	mV	I_Q = 5 mA to 100 mA
Line regulation	ΔV_Q	–	10	40	mV	V_I = 6 V to 26 V, I_Q = 1 mA
Reset generator						
Switching threshold	V_{RT}	4.50	4.65	4.80	V	–
Reset adjust switching threshold	$V_{RADJ, TH}$	1.26	1.35	1.44	V	V_Q > 3.5 V
Reset pull-up	–	10	20	40	kΩ	–
Saturation voltage	$V_{RO, SAT}$	–	0.1	0.4	V	R_{intern}
Upper delay switching threshold	V_{UD}	1.4	1.8	2.2	V	–
Lower delay switching threshold	V_{LD}	0.3	0.45	0.60	V	–
Saturation voltage delay capacitor	$V_{D, SAT}$	–	–	0.1	V	V_Q < V_{RT}
Charge current	I_D	3.0	6.5	9.5	µA	V_D = 1 V
Delay time L → H	t_d	17	28	–	ms	C_D = 100 nF
Delay time H → L	t_t	–	1	–	µs	C_D = 100 nF
Input voltage sense						
Sense threshold high	$V_{SI, high}$	1.24	1.31	1.38	V	–
Sense threshold low	$V_{SI, low}$	1.16	1.20	1.28	V	–
Sense output low voltage	$V_{SO, low}$	–	0.1	0.4	V	V_{SI} < 1.20 V; V_Q > 3 V, R_{intern}
Sense pull-up	–	10	20	40	kΩ	–
Sense input current	I_{SI}	-1	0.1	1	µA	–

1) Drop voltage = V_I - V_Q measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input.

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4 Functional description

The control amplifier compares a reference voltage, made highly accurate by resistance balancing, with a voltage proportional to the output voltage and drives the base of the series PNP transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

The reset output RO is in high-state if the voltage on the delay capacitor C_D is greater or equal V_{UD}. The delay capacitor C_D is charged with the current I_D for output voltages greater than the reset threshold V_{RT}. If the output voltage gets lower than V_{RT} ('reset condition') a fast discharge of the delay capacitor C_D sets in and as soon as V_D gets lower than V_{LD} the reset output RO is set to low-level.

The time gap for the delay capacitor discharge is the reset reaction time t_{RR}.

The reset threshold V_{RT} can be decreased via an external voltage divider connected to the pin RADJ. In this case the reset condition is reached if $V_Q < V_{RT}$ and $V_{RADJ} < V_{RAQDJ, TH}$. Dimensioning the voltage divider (**Figure 5**) according to:

(4.1)

$$V_{THRES} = \frac{V_{RAD(J, TH)} \times (R_{ADJ1} + R_{ADJ2})}{R_{ADJ2}}$$

the reset threshold can be decreased down to 3.5 V. If the reset-adjust-option is not needed the RADJ-pin should be connected to GND causing the reset threshold to go to its default value (typ. 4.65 V).

A built in comparator compares the signal of the pin SI, normally fed by a voltage divider from the input voltage, with the reference and gives an early warning on the pin SO. It is also possible to superwise another voltage e.g. of a second regulator, or to build a watchdog circuit with few external components.

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5 Application information

The input capacitor C_I is necessary for compensating line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values ≥ 10 µF and an ESR ≤ 10 Ω within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

5.1 Application diagram

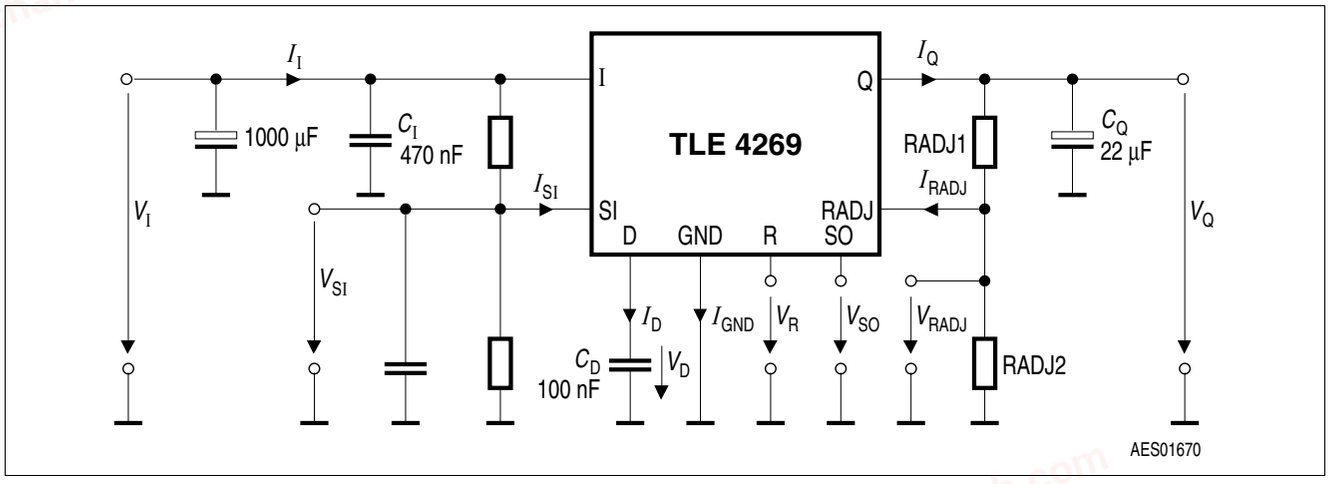


Figure 5 Measuring circuit

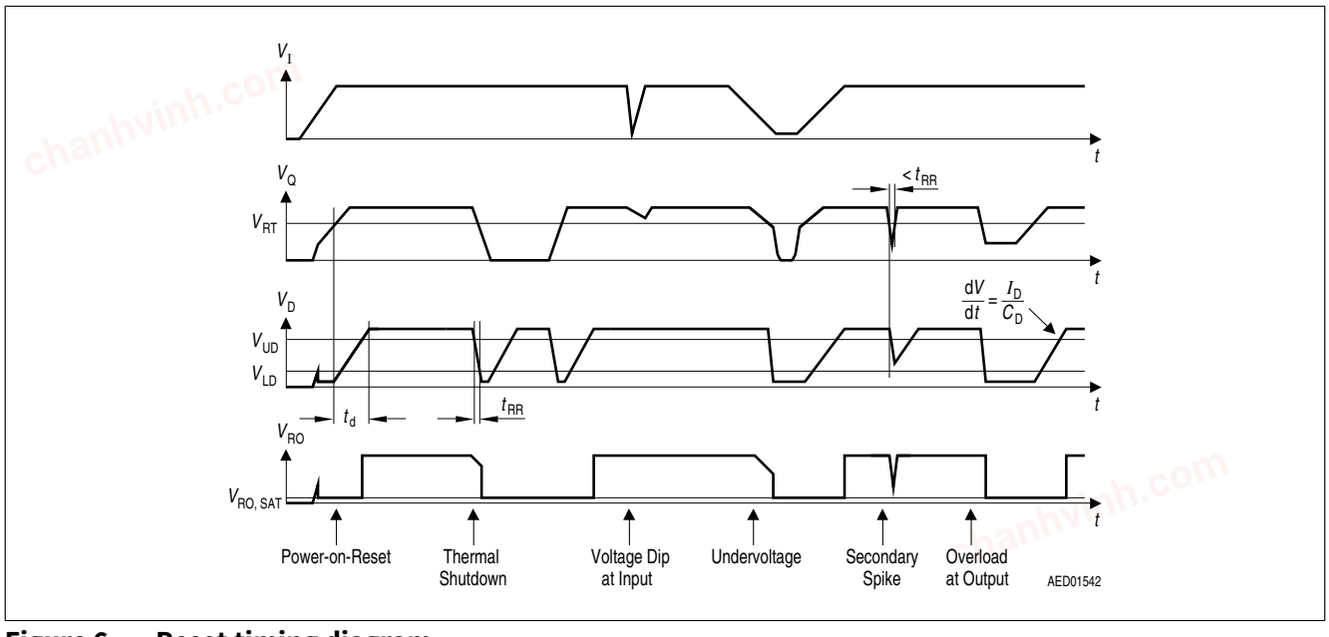


Figure 6 Reset timing diagram

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Application information

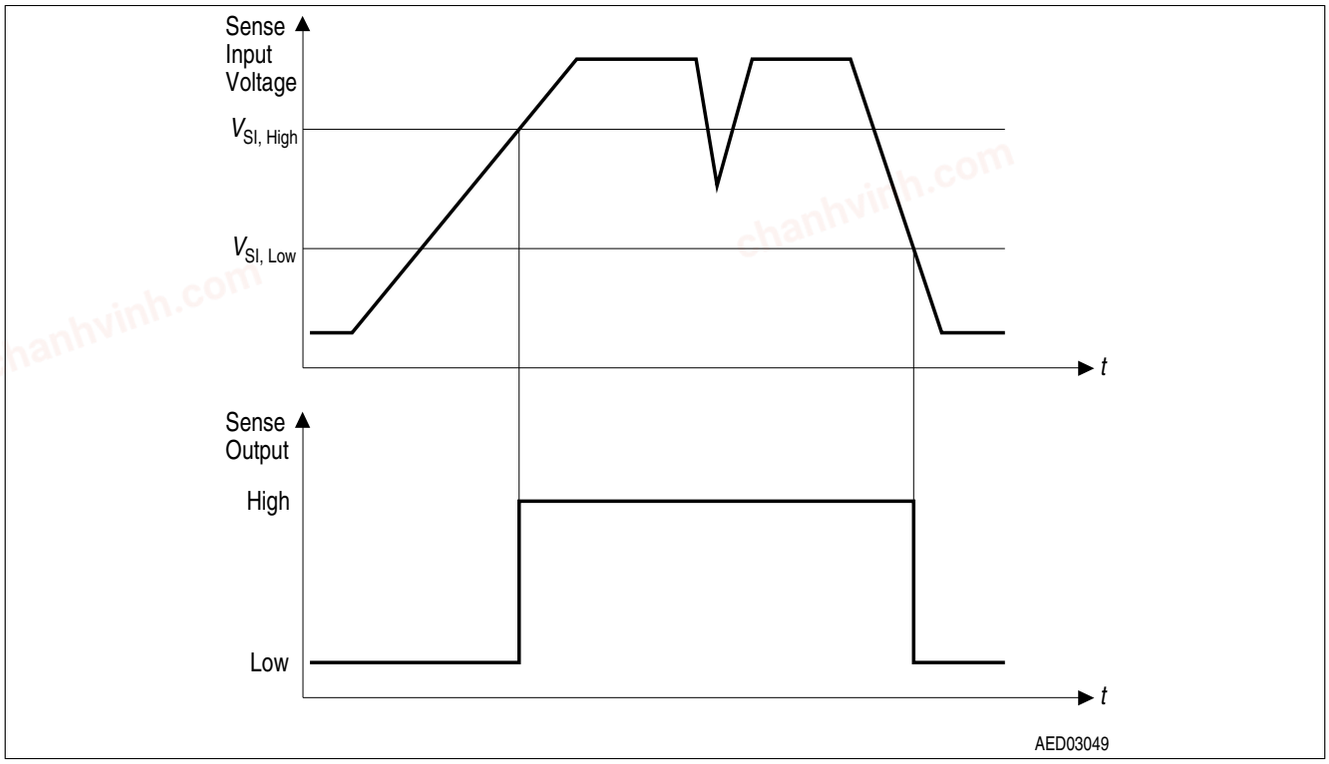
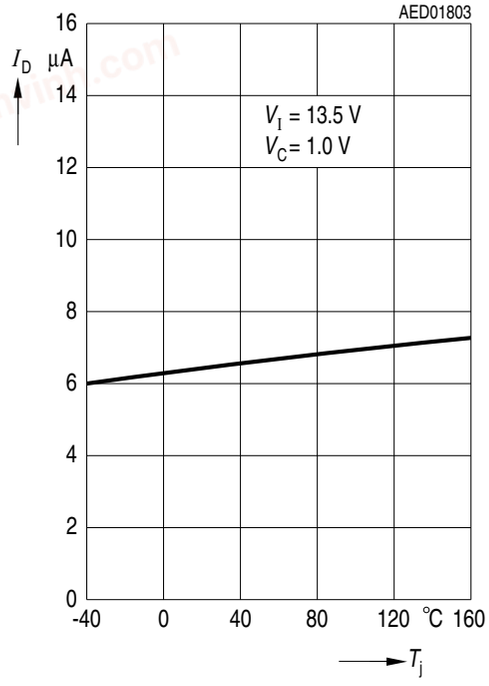


Figure 7 Sense timing diagram

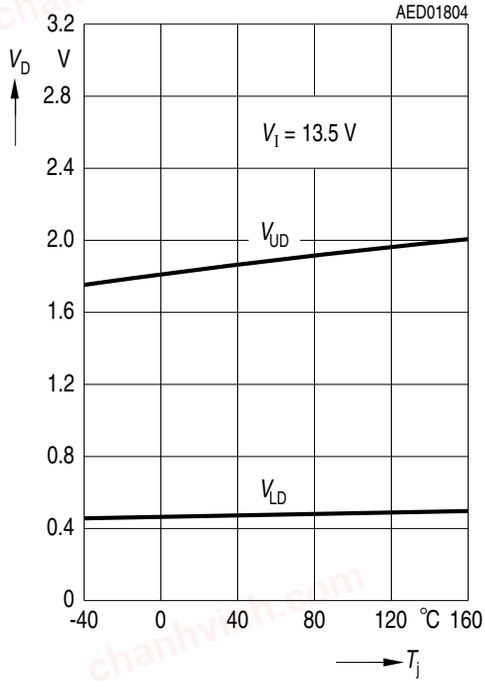
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5.2 Typical performance characteristics

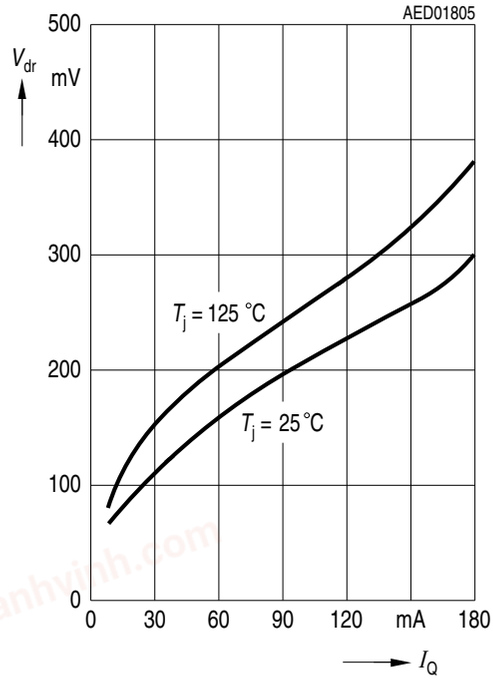
Charge current I_D versus junction temperature T_j



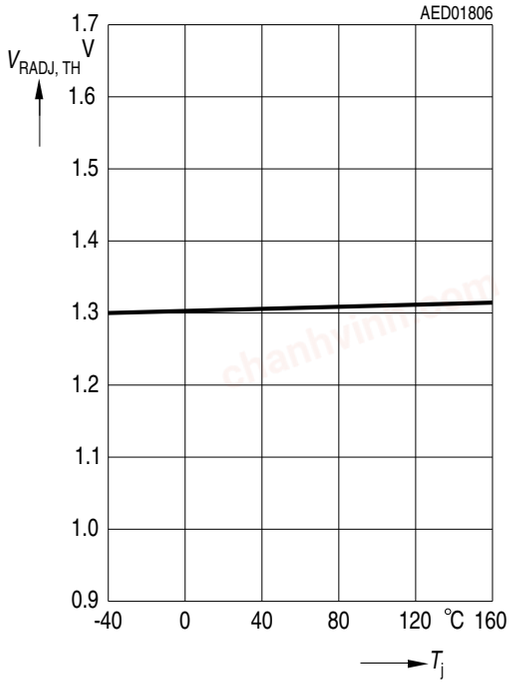
Switching voltage V_{UD} and V_{LD} versus junction temperature T_j



Drop voltage V_{dr} versus output current I_Q



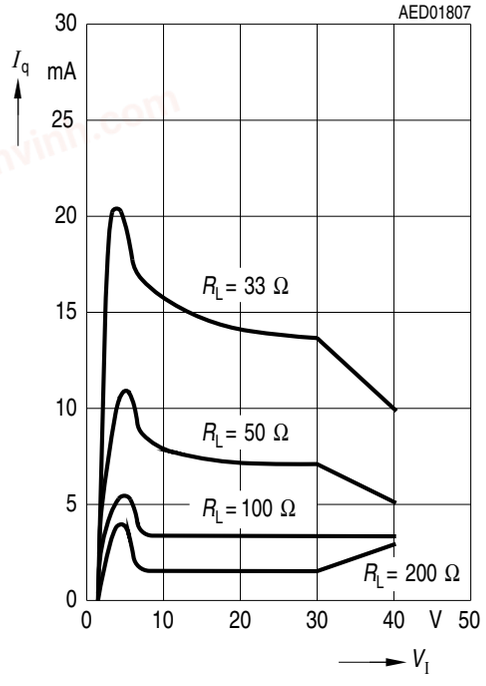
Reset adjust switching threshold $V_{RADJ,TH}$ versus junction temperature T_j



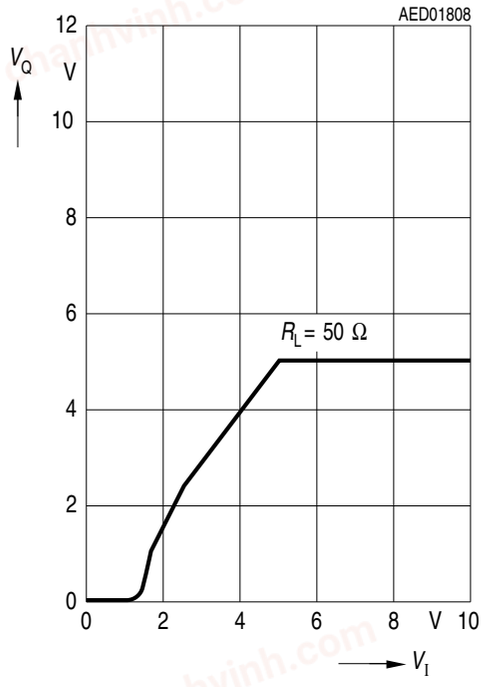
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Application information

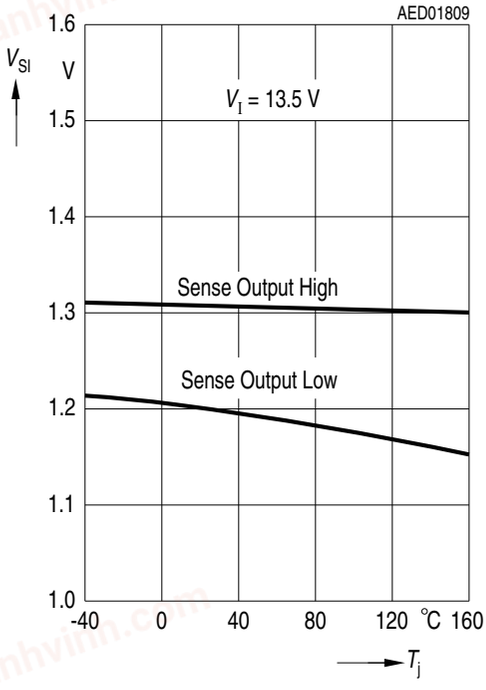
Current consumption I_Q versus input voltage V_I



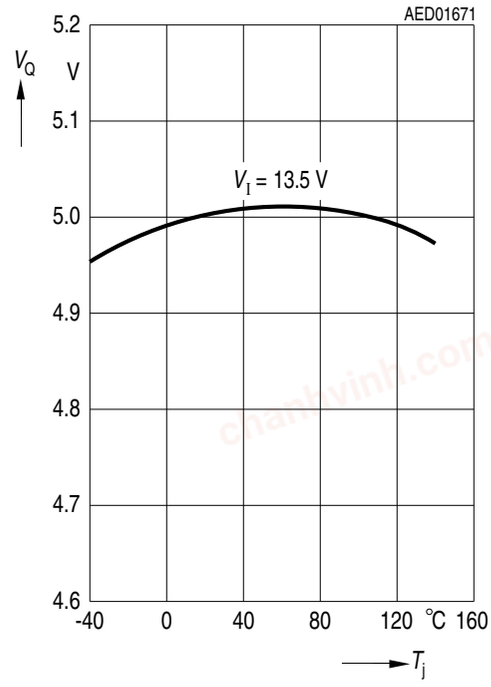
Output voltage V_Q versus input voltage V_I



Sense threshold V_{SI} versus junction temperature T_j



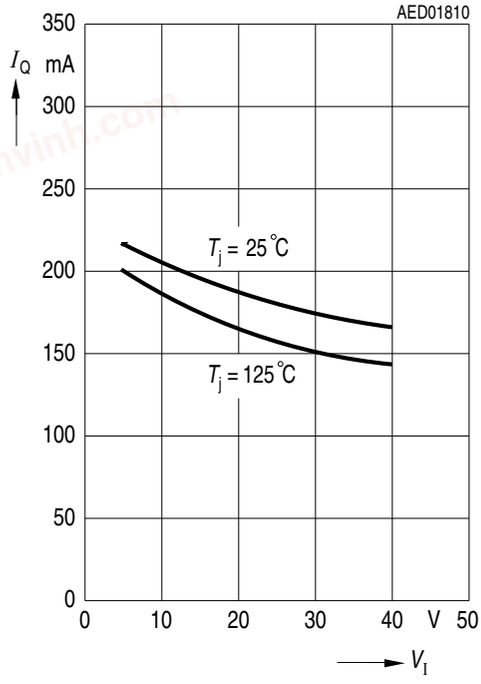
Output voltage V_Q versus junction temperature T_j



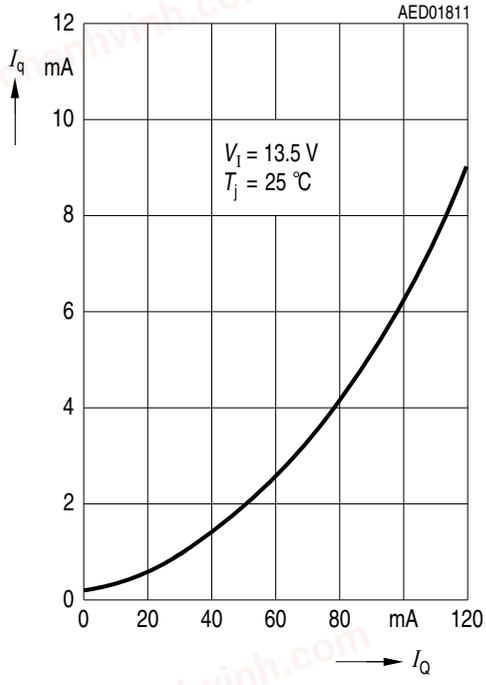
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Application information

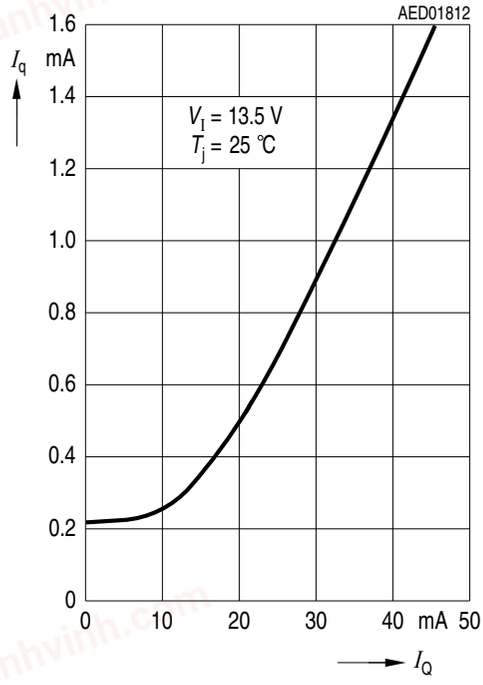
Output current I_Q versus input voltage V_I



Current consumption I_Q versus output current I_Q

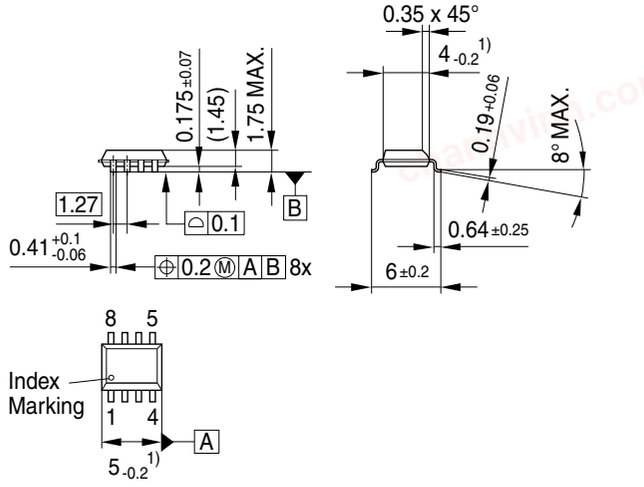


Current consumption I_q versus output current I_Q



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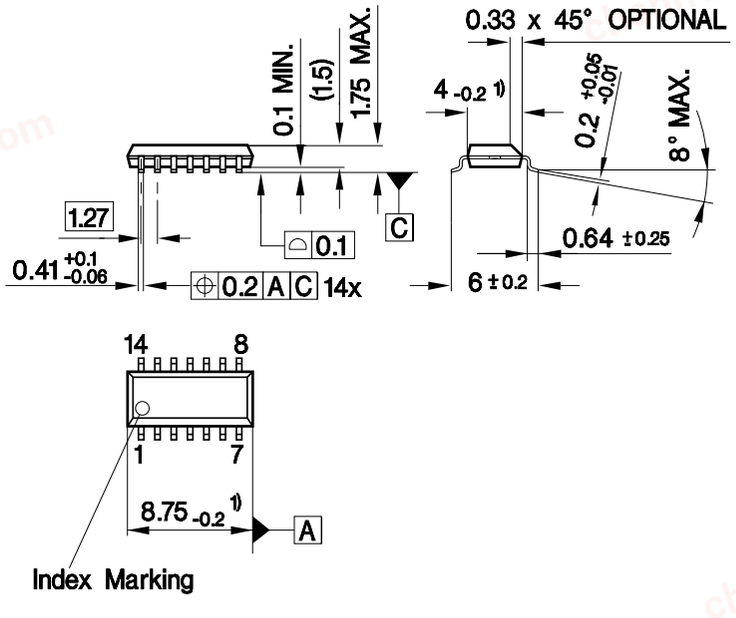
6 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

GPS01229

Figure 8 PG-DSO-8 1)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 9 PG-DSO-14 1)

1) Dimensions in mm

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Package information

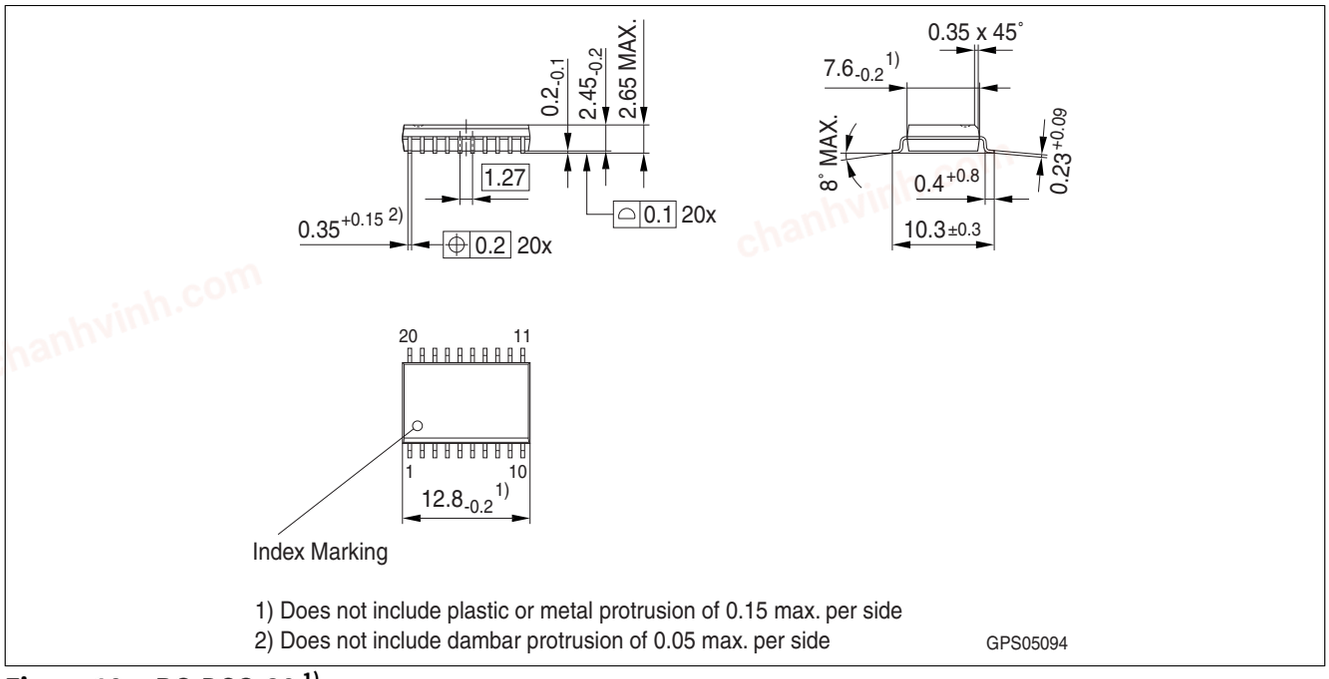


Figure 10 PG-DSO-20 [1)]

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

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7 Revision history

Revision	Date	Changes
2.6	2018-11-20	Update layout and structure Updated packaged drawing “PG-DSO-14” Editorial changes
2.5	2013-11-25	Package version changed: - PG-DSO-20-35 to PG-DSO-20 Package naming harmonized according to Infineon standards: - PG-DSO-8-16 to PG-DSO-8 - PG-DSO-14-30 to PG-DSO-14
2.4	2007-03-20	Initial version of RoHS-compliant derivate of TLE4269 **Page 1**: AEC certified statement added **Page 1** and **Page 16** : RoHS compliance statement and Green product feature added **Page 1** and **Page 16** : Package changed to RoHS compliant version Legal Disclaimer updated
2.3	2004-01-01	

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Edition 2018-11-20
Published by
Infineon Technologies AG
81726 Munich, Germany

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Z8F52238104

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