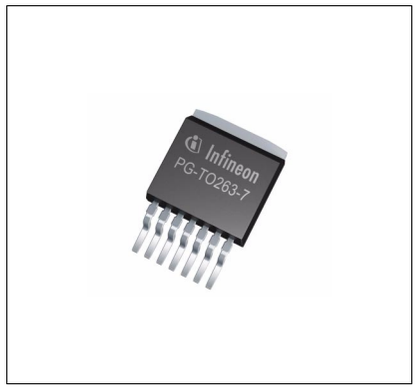
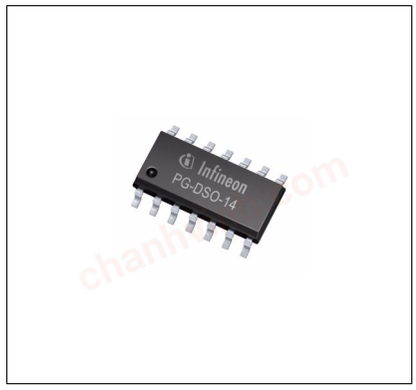
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# TLE4267

## 5 V Low Drop Voltage Regulator

AEC Qualified RoHS




## Features

- Output voltage tolerance ≤ ±2%
- 400 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Input voltage up to 40 V
- Overvoltage protection up to 60 V (≤ 400 ms)
- Reset function down to 1 V output voltage
- ESD protection up to 2000 V
- Adjustable reset time
- On/off logic
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Wide temperature range
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)

## Potential applications

- Automotive applications directly connected to the battery
- Applications with a protected power supply for off-board load

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

## Description

TLE4267 is a 5 V low drop voltage regulator for automotive applications in the PG-TO263-7 or PG-DSO-14 package. It supplies an output current of greater than 400 mA. The IC is short-circuit-proof and has an overtemperature protection circuit.

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| Type | Package | Marking |
|---|---|---|
| TLE4267G | PG-TO263-7 | TLE4267 |
| TLE4267GM | PG-DSO-14 | TLE4267 |

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# 1 Block diagram

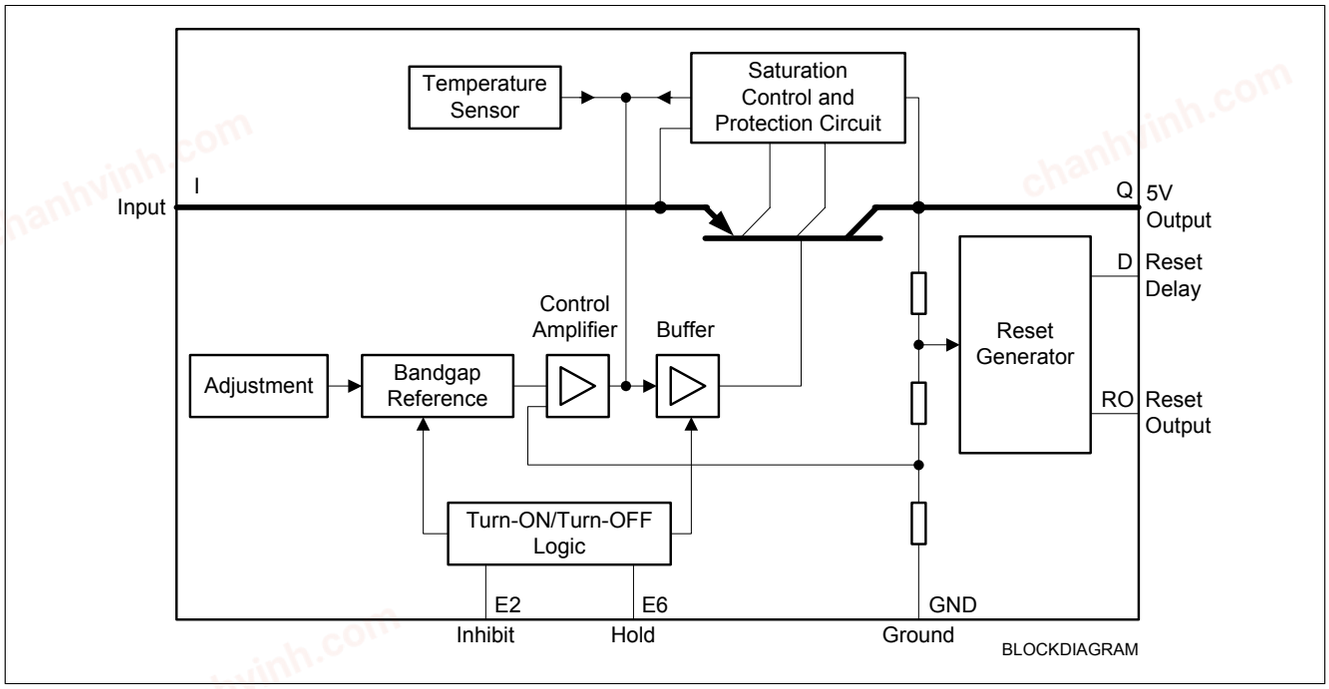



**Figure 1 Block diagram TLE4267**

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# 2 Pin configuration

## 2.1 Pin assignment PG-TO263-7

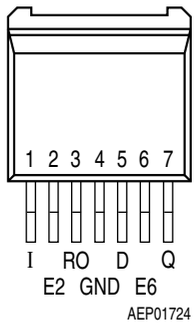



**Figure 2 Pin configuration** (top view)

**Table 1 Pin definitions and functions**

| Pin | Symbol | Function |
|---|---|---|
| 1 | I | **Input;** block to ground directly at the IC by a ceramic capacitor |
| 2 | E2 | **Inhibit;** device is turned on by High signal on this pin; internal pull-down resistor of 100 kΩ |
| 3 | RO | **Reset Output;** open-collector output internally connected to the output via a resistor of 30 kΩ |
| 4 | GND | **Ground;** connected to rear of chip |
| 5 | D | **Reset Delay;** connect via capacitor to GND |
| 6 | E6 | **Hold;** see **Table 6** for function; this input is connected to output voltage via a pull-up resistor of 50 kΩ |
| 7 | Q | **5 V Output;** block to GND with 22 µF capacitor, ESR < 3 Ω |

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## 2.2 Pin assignment PG-DSO-14

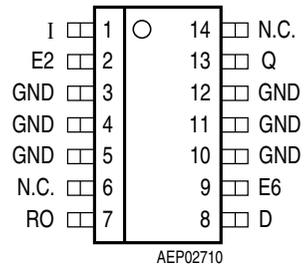



**Figure 3** **Pin configuration** (top view)

**Table 2** **Pin definitions and functions**

| Pin | Symbol | Function |
|---|---|---|
| 1 | I | **Input;** block to ground directly at the IC by a ceramic capacitor |
| 2 | E2 | **Inhibit;** device is turned on by High signal on this pin; internal pull-down resistor of 100 kΩ |
| 7 | RO | **Reset Output;** open-collector output internally connected to the output via a resistor of 30 kΩ |
| 3, 4, 5, 10, 11, 12 | GND | **Ground;** connected to rear of chip |
| 8 | D | **Reset Delay;** connect with capacitor to GND for setting delay |
| 9 | E6 | **Hold;** see **Table 6** for function; this input is connected to output voltage via a pull-up resistor of 50 kΩ |
| 13 | Q | **5 V Output;** block to GND with 22 µF capacitor, ESR ≤ 3 Ω |
| 6, 14 | N.C. | Not Connected |

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# 3 General product characteristics

## 3.1 Absolute maximum ratings

**Table 3 Absolute maximum ratings[1)]**

$T_J$ = -40 to 150°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Input** | | | | | | | |
| Voltage | $V_I$ | -42 | – | 42 | V | – | P_3.1.1 |
| Voltage | $V_I$ | – | – | 60 | V | $t \leq 400$ ms | P_3.1.2 |
| Current | $I_I$ | – | – | – | – | Internally limited | P_3.1.3 |
| **Reset output** | | | | | | | |
| Voltage | $V_{RO}$ | -0.3 | – | 7 | V | – | P_3.1.4 |
| Current | $I_{RO}$ | – | – | – | – | Internally limited | P_3.1.5 |
| **Reset delay** | | | | | | | |
| Voltage | $V_D$ | -0.3 | – | 42 | V | – | P_3.1.6 |
| Current | $I_D$ | – | – | – | – | – | P_3.1.7 |
| **Output** | | | | | | | |
| Voltage | $V_Q$ | -0.3 | – | 7 | V | – | P_3.1.8 |
| Current | $I_Q$ | – | – | – | – | Internally limited | P_3.1.9 |
| **Inhibit** | | | | | | | |
| Voltage | $V_{E2}$ | -42 | – | 42 | V | – | P_3.1.10 |
| Current | $I_{E2}$ | -5 | – | 5 | mA | $t \leq 400$ ms | P_3.1.11 |
| **Hold** | | | | | | | |
| Voltage | $V_{E6}$ | -0.3 | – | 7 | V | – | P_3.1.12 |
| Current | $I_{E6}$ | – | – | – | mA | Internally limited | P_3.1.13 |
| **GND** | | | | | | | |
| Current | $I_{GND}$ | -0.5 | – | – | A | – | P_3.1.14 |
| **Temperatures** | | | | | | | |
| Junction temperature | $T_J$ | – | – | 150 | °C | – | P_3.1.15 |
| Storage temperature | $T_{stg}$ | -50 | – | 150 | °C | – | P_3.1.16 |

1) Not subject to production test, specified by design.

**Notes**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.*

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## 3.2 Functional range

**Table 4 Functional range**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Input voltage | $V_I$ | 5.5 | – | 40 | V | – | P_3.2.1 |
| Junction temperature | $T_J$ | -40 | – | 150 | °C | – | P_3.2.2 |

*Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*

## 3.3 Thermal resistance

**Table 5 Thermal resistance**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **PG-TO263-7 package** | | | | | | | |
| Junction ambient | $R_{thja}$ | – | – | 70 | K/W | – | P_3.3.4 |
| Junction-case | $R_{thjc}$ | – | – | 6 | K/W | – | P_3.3.5 |
| Junction-case | $Z_{thjc}$ | – | – | 2 | K/W | $t < 1$ ms | P_3.3.6 |
| **PG-DSO-14 package** | | | | | | | |
| Junction ambient | $R_{thja}$ | – | – | 70 | K/W | – | P_3.3.10 |
| Junction-pin | $R_{thjp}$ | – | – | 30 | K/W | – | P_3.3.11 |

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.*

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# 4 Functional description

### Application

The IC regulates an input voltage $V_I$ in the range of 5.5 V < $V_I$ < 40 V to a nominal output voltage of $V_Q$ = 5.0 V. A reset signal is generated for an output voltage of $V_Q$ < $V_{RT}$ (typ. 4.5 V). The reset delay can be set with an external capacitor. The device has two logic inputs. A voltage of $V_{E2}$ > 4.0 V applied to the E2-pin (e.g. by ignition) turns the device on. Depending on the voltage on pin E6 the IC may be kept in Hold active-state even if $V_{E2}$ goes to low level (see **Table 6**). This makes it simple to implement a self-holding circuit without external components. When the device is turned off, the output voltage drops to 0 V and current consumption tends towards 0 µA.

### Design notes for external components

The input capacitor $C_I$ is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approximately 1 Ω in series with $C_I$. The output capacitor is necessary for the stability of the regulating circuit. Stability is specified at values of $C_Q$ ≥ 22 µF and an ESR of ≤ 3 Ω within the operating temperature range.

### Circuit description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturating of the power element.

The reset output RO is in high-state if the voltage on the delay capacitor $C_D$ is greater or equal $V_{UD}$. The delay capacitance $C_D$ is charged with the current $I_D$ for output voltages greater than the reset threshold $V_{RT}$. If the output voltage drops below $V_{RT}$ a fast discharge of the delay capacitor $C_D$ sets in and as soon as $V_{CD}$ drops below $V_{LD}$ the reset output RO is set to low-level (see **Figure 6**). The reset delay can be set within a wide range by dimensioning the capacitance of the external capacitor.

**Table 6 Truth table for turn-ON/turn-OFF logic**

| E2, Inhibit[1)] | E6, Hold[2)] | $V_Q$ | Remarks |
|---|---|---|---|
| L | X | OFF | Initial state |
| H | X | ON | Regulator switched on via Inhibit, by ignition for example |
| H | L | ON | Hold clamped active to ground by controller while Inhibit is still high |
| X | L | ON | Previous state remains, even if ignition is shutting off: self-holding state |
| L | L | ON | Ignition shut off while regulator is in self-holding state |
| L | H | OFF | Regulator shut down by releasing of Hold while Inhibit remains Low, final state. No active clamping required by external self-holding circuit (µC) to keep regulator in off-state |

1) Inhibit: E2 Enable function, active high.
2) Hold: E6 Hold and release function, active low.

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## 4.1 Electrical characteristics

**Table 7 Electrical characteristics**

$V_I$ = 13.5 V; -40°C < $T_J$ < 125°C; $V_{E2}$ > 4 V (unless specified otherwise)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Output voltage | $V_Q$ | 4.9 | 5 | 5.1 | V | 5 mA ≤ $I_Q$ ≤ 400 mA<br>6 V ≤ $V_I$ ≤ 26 V | P_4.1.1 |
| Output voltage | $V_Q$ | 4.9 | 5 | 5.1 | V | 5 mA ≤ $I_Q$ ≤ 150 mA<br>6 V ≤ $V_I$ ≤ 40 V | P_4.1.2 |
| Output current limiting | $I_Q$ | 500 | – | – | mA | $T_J$ = 25°C | P_4.1.3 |
| Current consumption<br>$I_q = I_I - I_Q$ | $I_q$ | – | – | 50 | µA | IC turned off | P_4.1.4 |
| Current consumption<br>$I_q = I_I - I_Q$ | $I_q$ | – | 1.0 | 10 | µA | $T_J$ = 25°C<br>IC turned off | P_4.1.5 |
| Current consumption<br>$I_q = I_I - I_Q$ | $I_q$ | – | 1.3 | 4 | mA | $I_Q$ = 5 mA<br>IC turned on | P_4.1.6 |
| Current consumption<br>$I_q = I_I - I_Q$ | $I_q$ | – | – | 60 | mA | $I_Q$ = 400 mA | P_4.1.7 |
| Current consumption<br>$I_q = I_I - I_Q$ | $I_q$ | – | – | 80 | mA | $I_Q$ = 400 mA<br>$V_I$ = 5 V | P_4.1.8 |
| Drop voltage | $V_{Dr}$ | – | 0.3 | 0.6 | V | $I_Q$ = 400 mA[1)] | P_4.1.9 |
| Load regulation | $\Delta V_Q$ | – | – | 50 | mV | 5 mA ≤ $I_Q$ ≤ 400 mA | P_4.1.10 |
| Supply-voltage regulation | $\Delta V_Q$ | – | 15 | 25 | mV | $V_I$ = 6 to 36 V;<br>$I_Q$ = 5 mA | P_4.1.11 |
| Supply-voltage rejection | $SVR$ | – | 54 | – | dB | $f_r$ = 100 Hz;<br>$V_r$ = 0.5 Vpp | P_4.1.12 |
| Longterm stability | $\Delta V_Q$ | – | 0 | – | mV | 1000 h | P_4.1.13 |
| **Reset generator** | | | | | | | |
| Switching threshold | $V_{RT}$ | 4.2 | 4.5 | 4.8 | V | – | P_4.1.14 |
| Reset High level | – | 4.5 | – | – | V | $R_{ext}$ = ∞ | P_4.1.15 |
| Saturation voltage | $V_{RO,SAT}$ | – | 0.1 | 0.4 | V | $R_R$ = 4.7 kΩ[2)] | P_4.1.16 |
| Internal Pull-up resistor | $R_{RO}$ | – | 30 | – | kΩ | – | P_4.1.17 |
| Saturation voltage | $V_{D,SAT}$ | – | 50 | 100 | mV | $V_Q$ < $V_{RT}$ | P_4.1.18 |
| Charge current | $I_D$ | 8 | 15 | 25 | µA | $V_D$ = 1.5 V | P_4.1.19 |
| Upper delay switching threshold | $V_{UD}$ | 2.6 | 3 | 3.3 | V | – | P_4.1.20 |
| Delay time | $t_D$ | – | 20 | – | ms | $C_D$= 100 nF | P_4.1.21 |
| Lower delay switching threshold | $V_{LD}$ | – | 0.43 | – | V | – | P_4.1.22 |
| Reset reaction time | $t_{RR}$ | – | 2 | – | µs | $C_D$ = 100 nF | P_4.1.23 |
| **Inhibit** | | | | | | | |
| Turn on voltage | $V_{U,INH}$ | – | 3 | 4 | V | IC turned on | P_4.1.24 |
| Turn off voltage | $V_{L,INH}$ | 2 | – | – | V | IC turned off | P_4.1.25 |

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**Table 7 Electrical characteristics** (cont'd)

$V_I$ = 13.5 V; -40°C < $T_J$ < 125°C; $V_{E2}$ > 4 V (unless specified otherwise)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Pull-down resistor | $R_{INH}$ | 50 | 100 | 200 | kΩ | – | P_4.1.26 |
| Hysteresis | $\Delta V_{INH}$ | 0.2 | 0.5 | 0.8 | V | – | P_4.1.27 |
| Input current | $I_{INH}$ | – | 35 | 100 | µA | $V_{INH}$ = 4 V | P_4.1.28 |
| Hold voltage | $V_{U,HOLD}$ | 30 | 35 | 40 | % | Referred to $V_Q$ | P_4.1.29 |
| Turn off voltage | $V_{L,HOLD}$ | 60 | 70 | 80 | % | Referred to $V_Q$ | P_4.1.30 |
| Pull-up resistor | $R_{HOLD}$ | 20 | 50 | 100 | kΩ | – | P_4.1.31 |
| **Overvoltage Protection** | | | | | | | |
| Turn off voltage | $V_{I,OV}$ | 42 | 44 | 46 | V | $V_I$ increasing | P_4.1.32 |
| Turn on voltage | $V_{I,turn\ on}$ | 36 | – | – | V | $V_I$ decreasing after turn off | P_4.1.33 |

1) Drop voltage = $V_I$ - $V_Q$ (measured when the output voltage $V_Q$ has dropped 100 mV from the nominal value obtained at $V_I$ = 13.5 V).

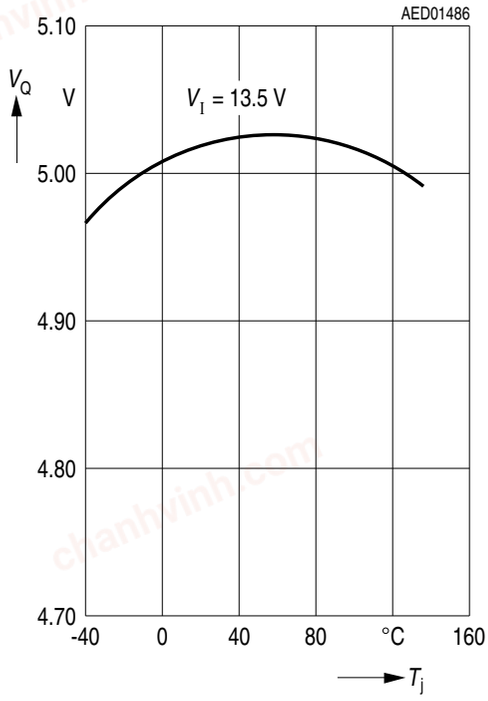
2) The reset output is low for 1 V < $V_Q$ < $V_{RT}$.

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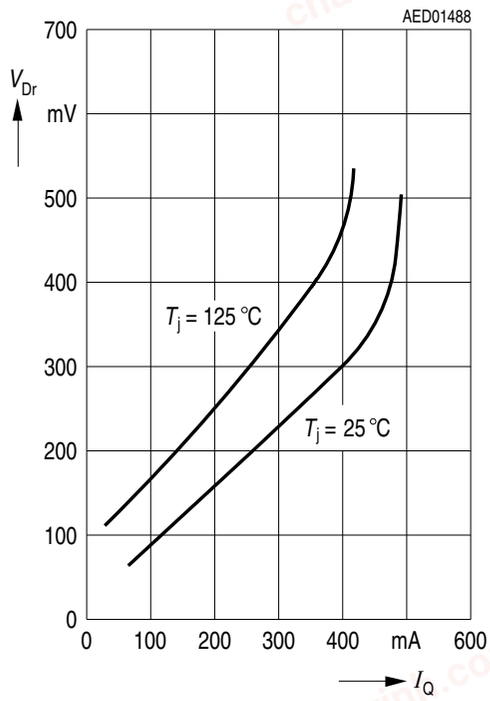


## 4.2 Typical performance characteristics

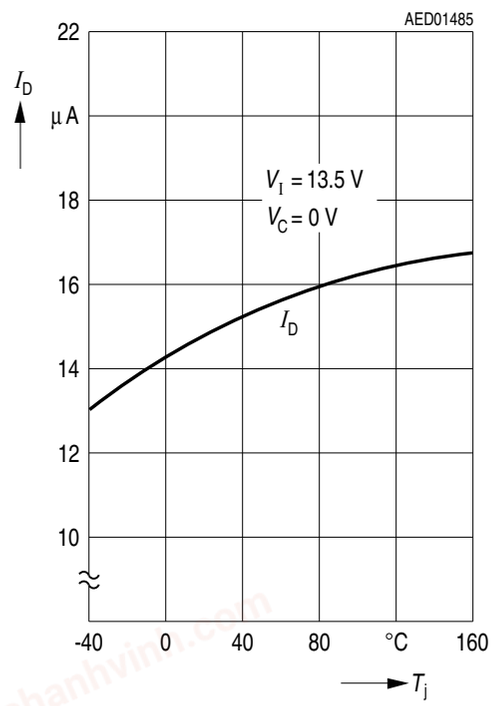
**Output voltage $V_Q$ versus junction temperature $T_j$**



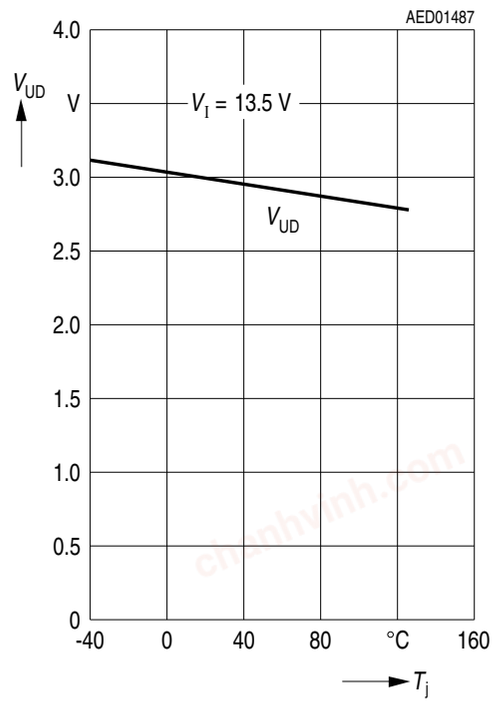

**Drop voltage $V_{Dr}$ versus output current $I_Q$**




**Charge current $I_D$ versus junction temperature $T_j$**




**Delay switching threshold $V_{UD}$ versus junction temperature $T_j$**

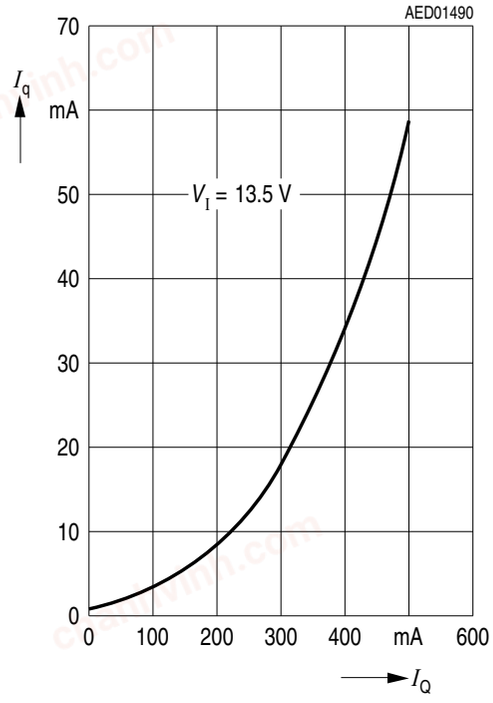


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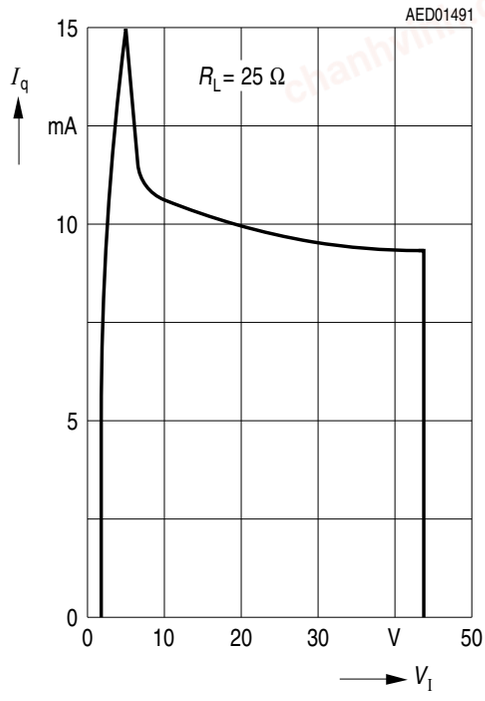


## Functional description

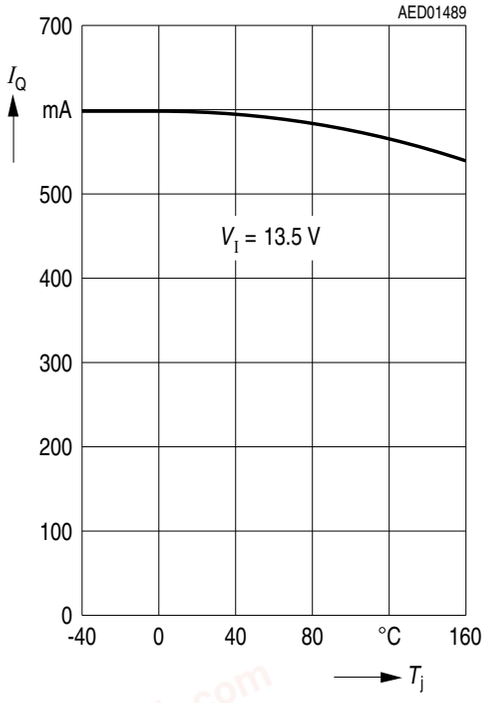
### Current consumption $I_q$ versus output current $I_Q$



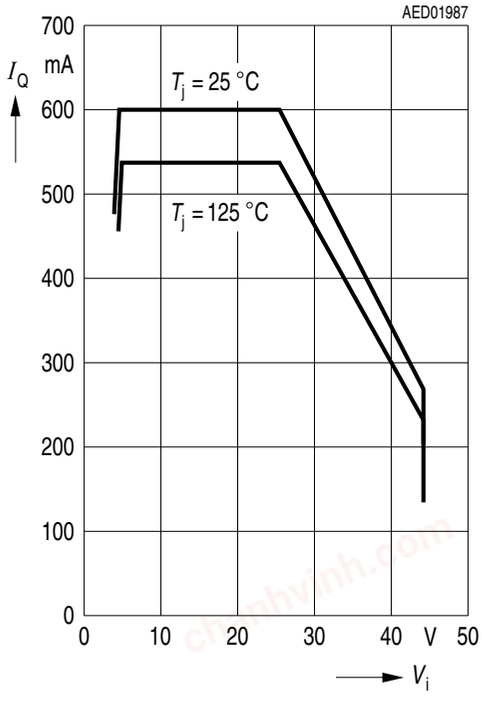

### Current consumption $I_q$ versus input voltage $V_I$




### Output current limiting $I_Q$ versus junction temperature $T_j$




### Output current limiting $I_Q$ versus input voltage $V_I$

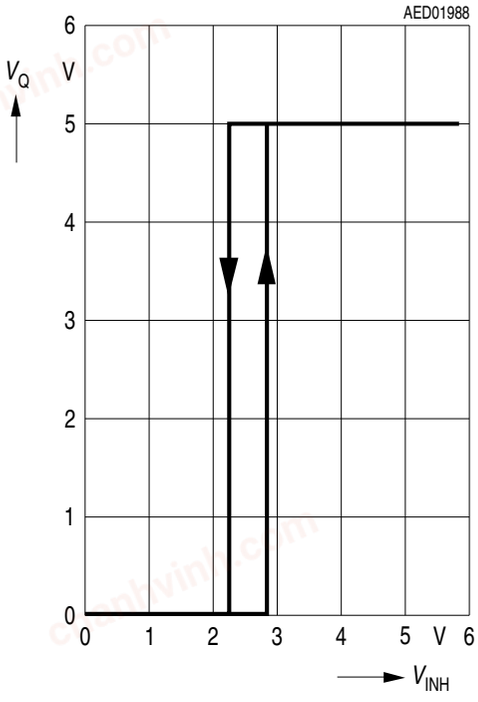


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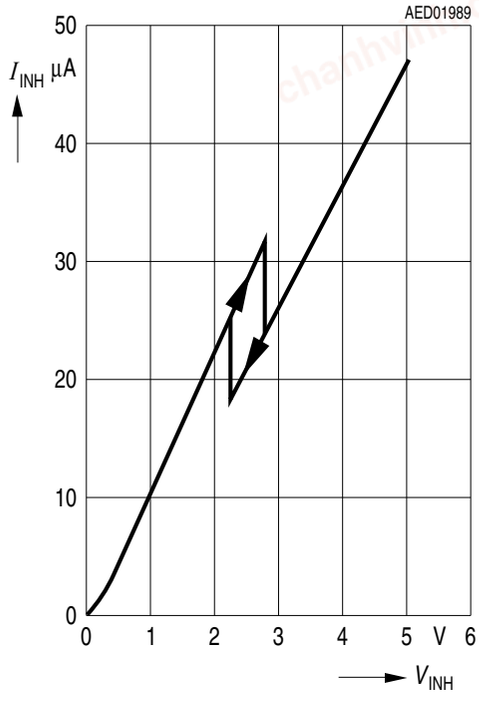


## Functional description

### Output voltage $V_Q$ versus inhibit voltage $V_{INH}$




### Inhibit current $I_{INH}$ versus inhibit voltage $V_{INH}$



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# 5 Test and application circuit

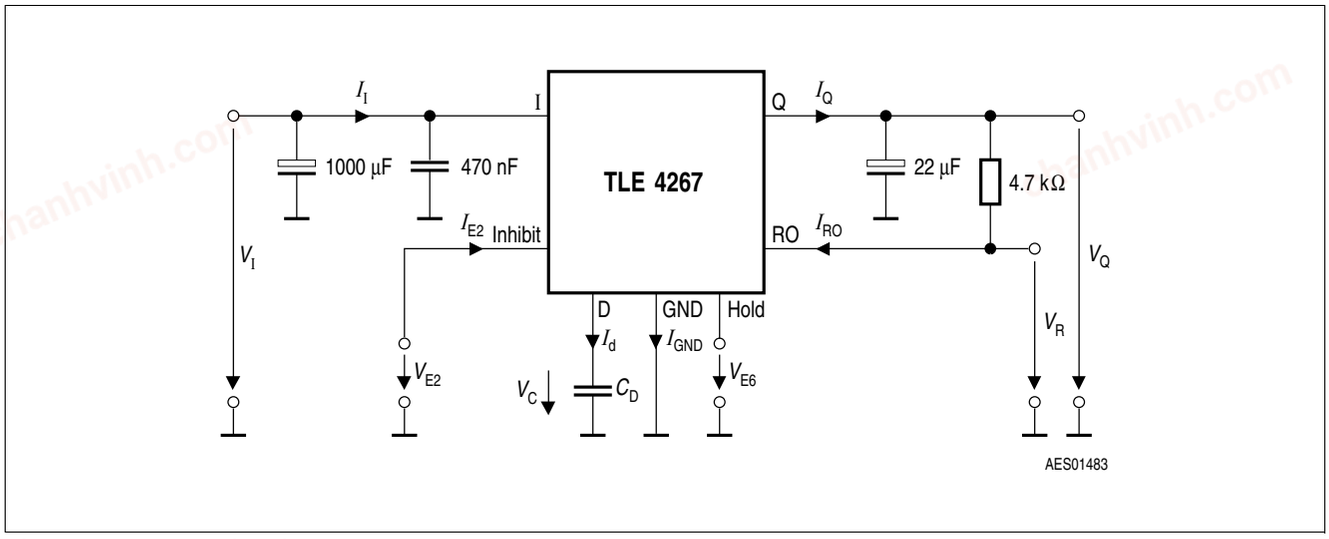



**Figure 4 Test circuit TLE4267**

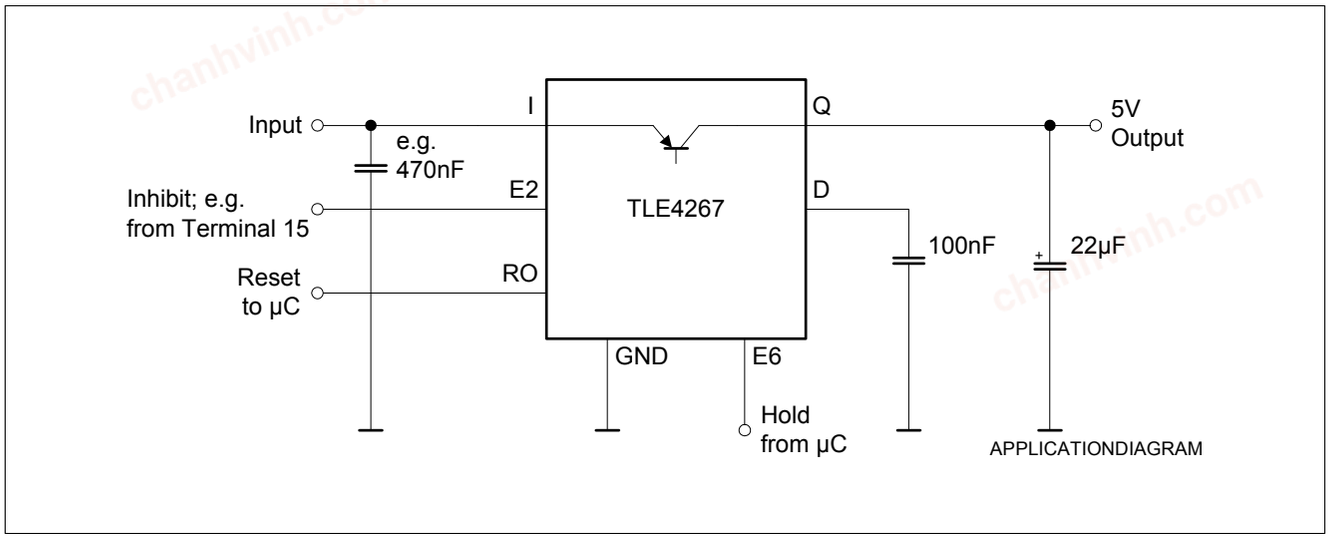



**Figure 5 Application circuit TLE4267**

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## Test and application circuit

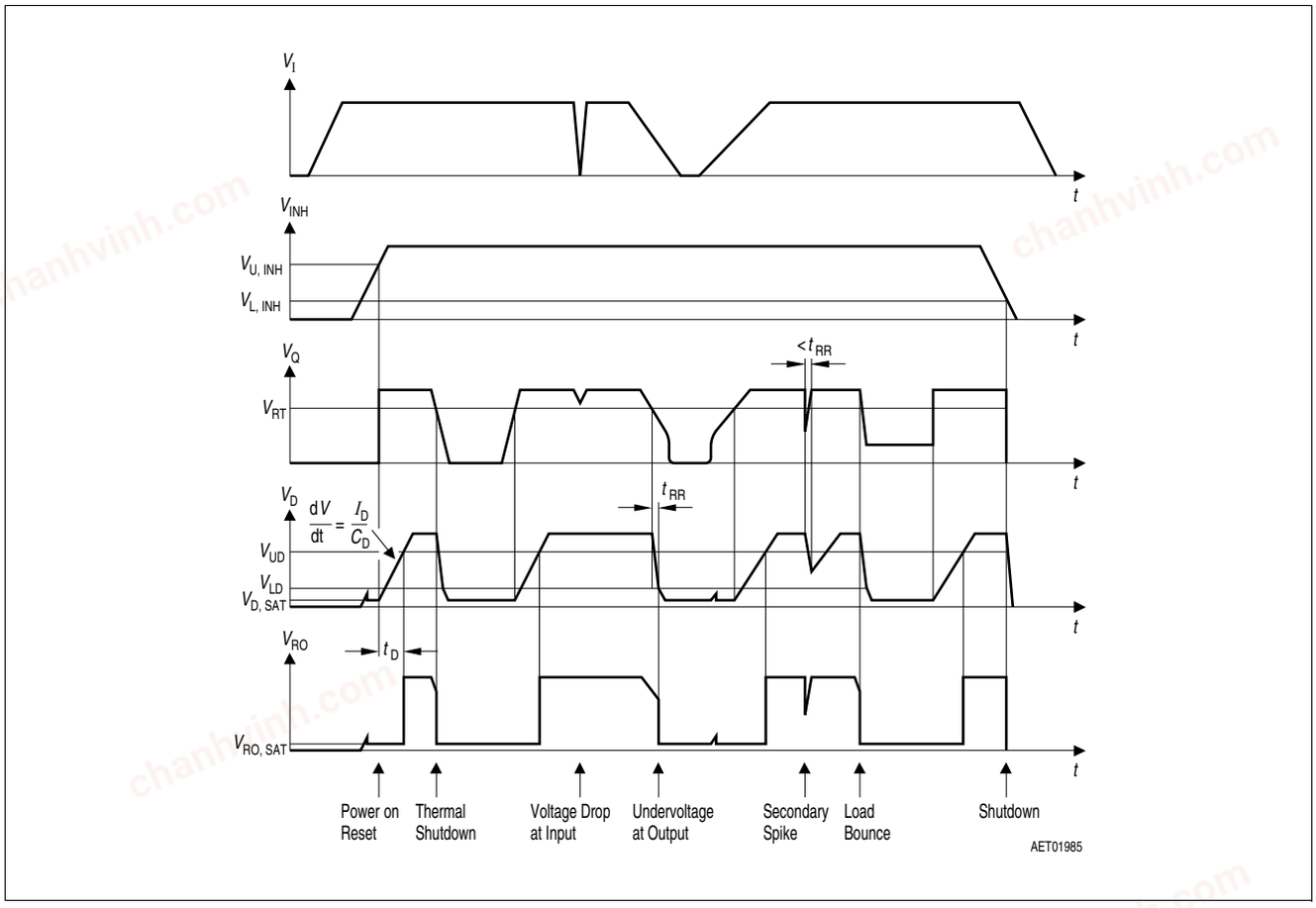
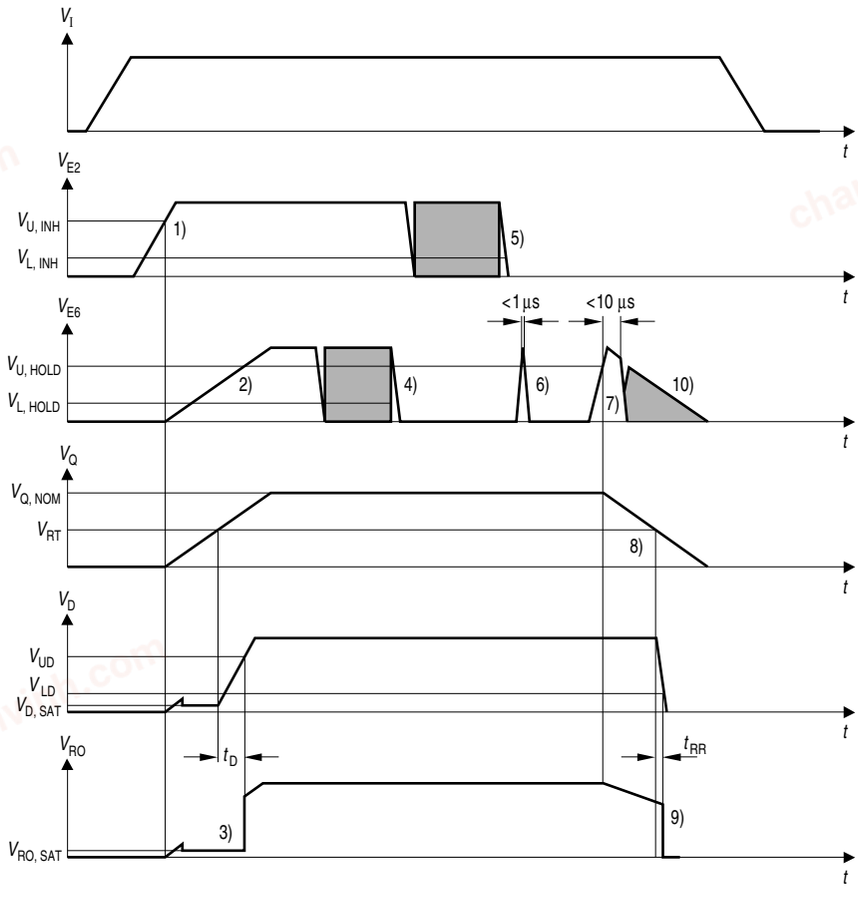



**Figure 6 Time response**

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## Test and application circuit




1) Enable active
2) Hold inactive, pulled up by $V_Q$
3) Power-ON reset
4) Hold active, clamped to GND by external µC
5) Enable inactive, clamped by int. pull-down resistor
6) Pulse width smaller than 1 µs
7) Hold inactive, released by µC
8) Voltage controller shutdown
9) Output-low reset
10) No switch on via $V_{E6}$ possible after E6 was released to $V_{E6} > V_{E6, rel}$ for more than 4 µs

AET01986

**Figure 7 Enable and Hold behavior**

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# 6 Package outlines

**Green Product** (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

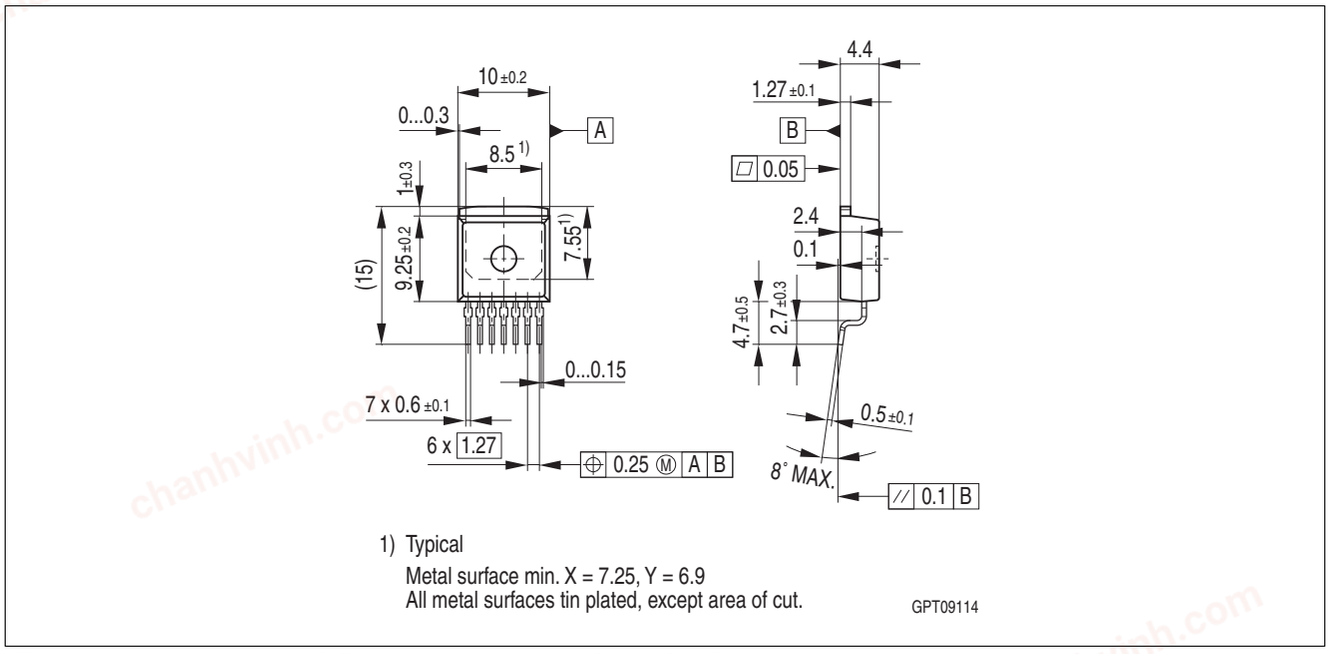



**Figure 8** **PG-TO263-7** (Plastic Transistor Single Outline)

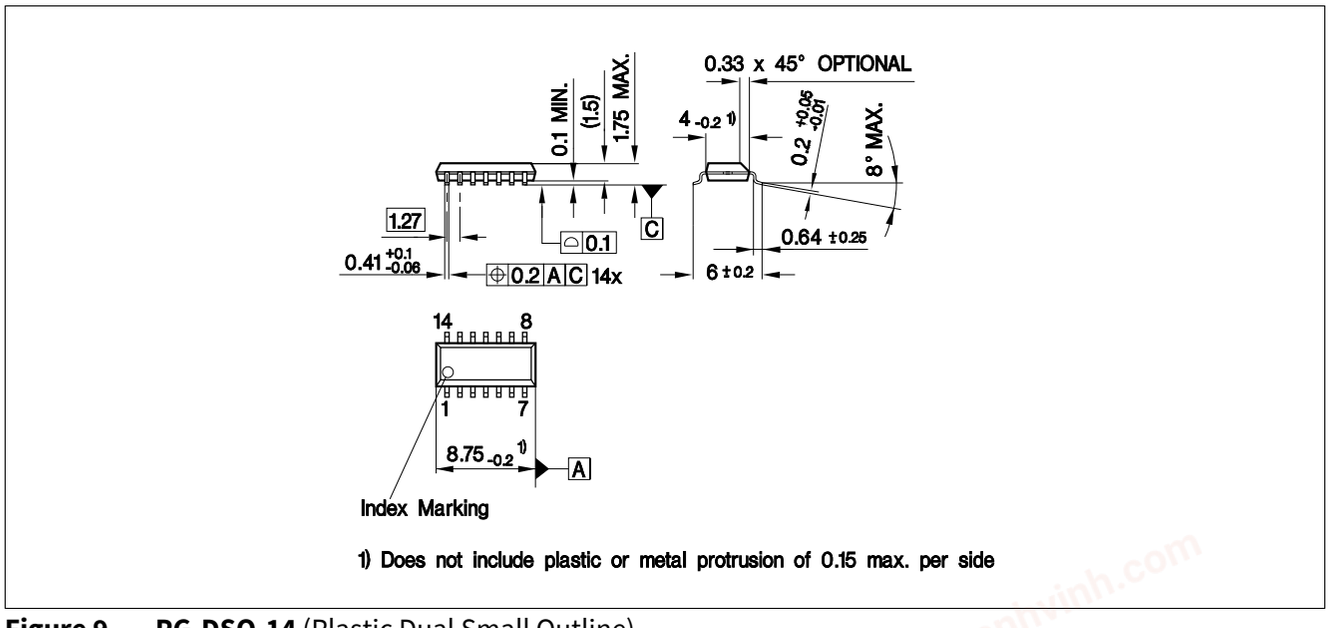



**Figure 9** **PG-DSO-14** (Plastic Dual Small Outline)

For further information on alternative packages, please visit our website:
**http://www.infineon.com/packages**.

Dimensions in mm

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# 7 Revision history

| Revision | Date | Changes |
|---|---|---|
| 2.6 | 2018-07-03 | Discontinued product variants TLE4267 and TLE4267S removed from data sheet.<br>Editorial changes.<br>Package updated by optional chamfer for PG-DSO-14. |
| 2.51 | 2012-02-20 | **Page 1**: Cover page added.<br>**Page 4**: **Figure 1** “**Block diagram TLE4267**” updated with clear label for reset output pin.<br>**Page 15**: **Figure 5** “**Application circuit TLE4267**” updated with clear labels for inhibit, hold, reset and reset delay pin. |
| 2.5 | 2007-03-20 | Initial version of RoHS-compliant derivative of TLE4267:<br>**Page 1**: AEC certified statement added.<br>**Page 1** and **Page 18** ff: RoHS compliance statement and Green product feature added.<br>**Page 1** and **Page 18** ff: Package changed to RoHS compliant version<br>Legal Disclaimer updated. |

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