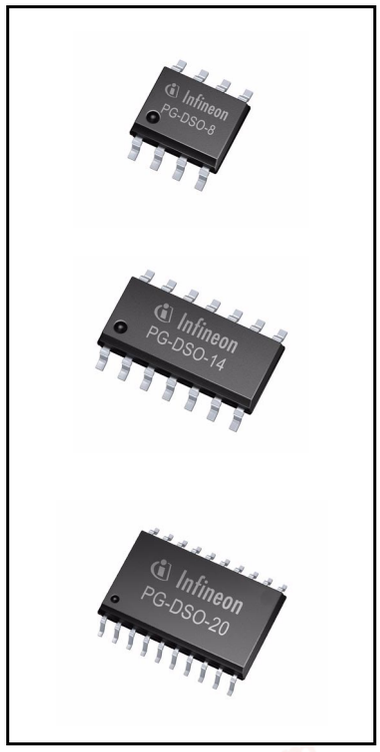
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OPTIREG™ Linear TLE4263

5 V low drop fixed voltage regulator

AEC Qualified RoHS



Features

- Output voltage tolerance ≤ ±2%
- 200 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Adjustable reset threshold
- Watchdog
- Wide temperature range
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The OPTIREG™ Linear TLE4263 is a 5 V low drop voltage regulator in a SMD package PG-DSO-14, PG-DSO-20, or PG-DSO-8. The maximum input voltage is 45 V. The maximum output current is 200 mA. The IC is short-circuit proof and incorporates temperature protection which turns off the IC at overtemperature.

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The IC regulates an input voltage V_I in the range between 6 V and 45 V to an output voltage to $V_{Q,nom}$ = 5.0 V. A reset signal is generated for an output voltage of $V_{Q,rt}$ < 4.5 V. This voltage threshold can be decreased to 3.5 V by external connection of a voltage divider. The reset delay can be set externally by a capacitor. The integrated watchdog logic supervises the connected microcontroller. The IC can be switched off via the inhibit input, which causes the current consumption to drop from 900 µA to typical 0 µA.

Type	Package	Marking
TLE4263GS	PG-DSO-8	TLE4263
TLE4263GM	PG-DSO-14	TLE4263
TLE4263G	PG-DSO-20	TLE4263

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1 Block diagram

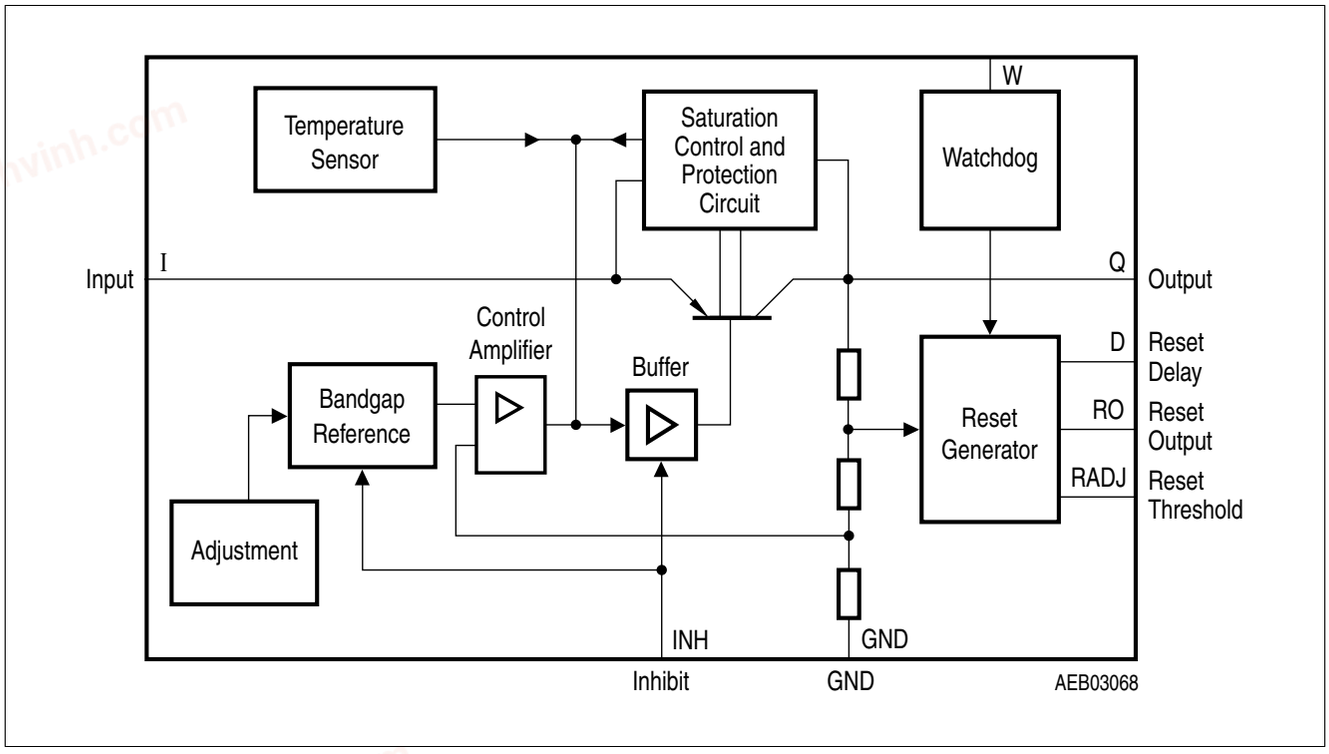


Figure 1 Block diagram

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2 Pin configuration

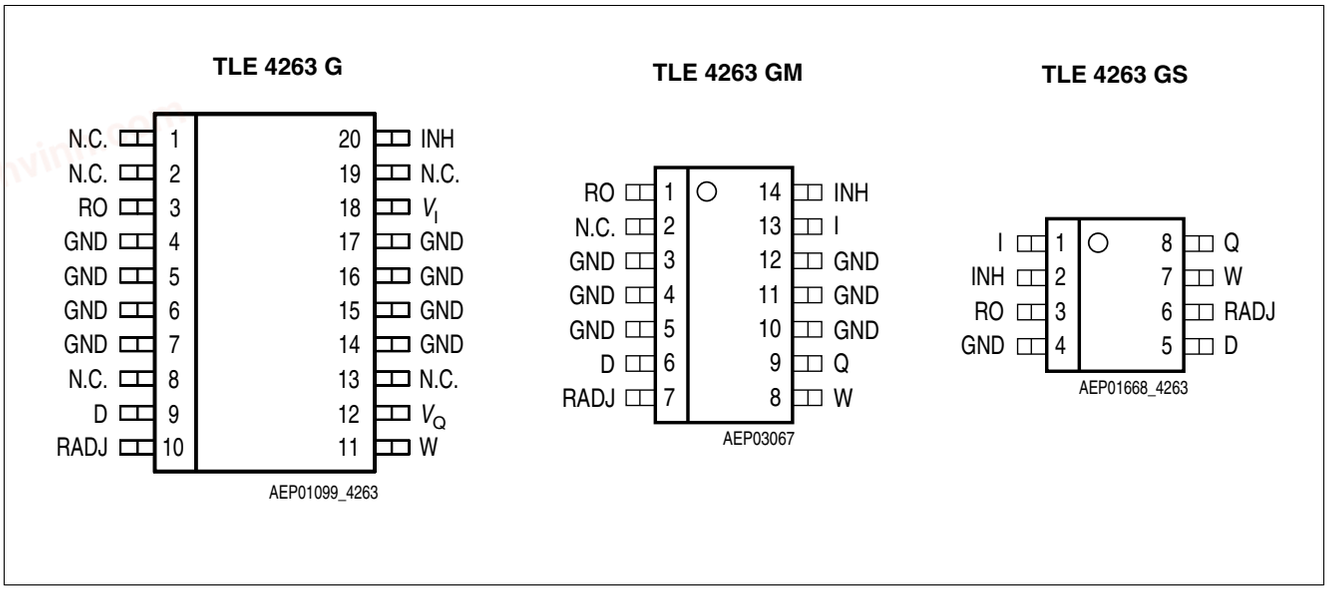


Figure 2 Pin configuration (top view)

Table 1 Pin definitions and functions

Pin PG-DSO-14	Pin PG-DSO-20	Pin PG-DSO-8	Symbol	Function
1	3	3	RO	**Reset output;** open-collector output connected to the output via a resistor of 30 kΩ.
2	1, 2, 19, 13	–	N.C.	**Not connected.**
3 - 5, 10 - 12	4-7, 14-17	4	GND	**Ground.**
6	9	5	D	**Reset delay;** connected to ground with a capacitor.
7	10	6	RADJ	**Reset threshold;** to adjust the switching threshold connect a voltage divider (output to GND) to the pin. If this input is connected to GND, reset is triggered at an output voltage of 4.5 V.
8	11	7	W	**Watchdog;** rising edge triggered input for monitoring a microcontroller.
9	12	8	Q	**5 V output voltage;** block to ground with a capacitor, C ≥ 22 µF, ESR ≤ 3 Ω at 10 kHz.
13	18	1	I	**Input voltage;** block to ground directly at the IC with a ceramic capacitor.
14	20	2	INH	**Inhibit;** TTL-compatible, low-active input.

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3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input I						
Input voltage	V_I	-42	–	45	V	–
Input current	I_I	–	–	–	–	Internally limited
Reset output RO						
Voltage	V_R	-0.3	–	42	V	–
Current	I_R	–	–	–	–	Internally limited
Reset threshold RADJ						
Voltage	V_{RADJ}	-0.3	–	6	V	–
Reset delay D						
Voltage	V_D	-0.3	–	42	V	–
Current	I_D	–	–	–	–	Internally limited
Output Q						
Voltage	V_Q	-0.3	–	7	V	–
Current	I_Q	–	–	–	–	Internally limited
Inhibit INH						
Voltage	V_{INH}	-42	–	45	V	–
Watchdog W						
Voltage	V_W	-0.3	–	6	V	–
Ground GND						
Current	I_{GND}	-0.5	–	–	A	–
Temperature						
Junction temperature	T_j	–	–	150	°C	–
Storage temperature	T_{stg}	-50	–	150	°C	–
Operating range						
Input voltage	V_I	–	–	45	V	–
Junction temperature	T_j	-40	–	150	°C	–

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Table 2 Absolute maximum ratings (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal resistance						
Junction-ambient	R_{thj-a}	–	–	112	K/W	PG-DSO-14[1]; Footprint only
		–	–	92	K/W	PG-DSO-14[1]; 300 mm² Heat sink
		–	–	185	K/W	PG-DSO-8[1]; Footprint only
		–	–	164	K/W	PG-DSO-8[1]; 300 mm² Heat sink
		–	–	84	K/W	PG-DSO-20[1]; Footprint only
		–	–	66	K/W	PG-DSO-20[1]; 300 mm² Heat sink
Junction-pin	R_{thj-p}	–	–	32	K/W	PG-DSO-14[2]

1) Worst case; package mounted on PCB 80 × 80 × 1.5 mm³; 35 µm Cu; 5 µm Sn; zero airflow.
2) Measured to pin 4.

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4 Functional description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. When the voltage of the capacitor reaches the lower threshold V_{DRL}, a reset signal occurs at the reset output and is held until the upper threshold V_{DU} is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of typ. 4.65 V. A connected microcontroller will be monitored through the watchdog logic. In case of missing pulses at pin W, the reset output is set to “low”. The pulse sequence time can be set in a wide range with the reset delay capacitor. The IC can be switched at the TTL-compatible, low-active inhibit input. The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

4.1 Choosing external components

The input capacitor C_I is necessary for compensation of line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is ensured at values $C_Q \geq 22$ µF and an ESR of ≤ 3 Ω within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

4.2 Electrical characteristics

Table 3 Electrical characteristics

V_I = 13.5 V; -40°C < T_j < 125°C; V_{INH} > 3.5 V; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Normal Operation						
Output voltage	V_Q	4.90	5.00	5.10	V	5 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 28 V
Output voltage	V_Q	4.90	5.00	5.10	V	6 V ≤ V_I ≤ 32 V; I_Q = 100 mA; T_j = 100°C
Output current limitation	$I_{Q,max}$	201	250	400	mA	V_Q = 4.8V
Current consumption; $I_q = I_I - I_Q$	I_q	–	0	50	µA	V_{INH} = 0
	I_q	–	900	1300	µA	I_Q = 0 mA
	I_q	–	10	18	mA	I_Q = 150 mA
	I_q	–	15	23	mA	I_Q = 150 mA; V_I = 4.5 V
Drop voltage	V_{dr}	–	0.35	0.50	V	I_Q = 150 mA[1)]
Load regulation	$\Delta V_{Q,lo}$	–	–	25	mV	I_Q = 5 mA to 150 mA
Line regulation	$\Delta V_{Q.li}$	–	3	25	mV	V_I = 6 V to 28 V; I_Q = 150 mA

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Table 3 Electrical characteristics (cont'd)

V_I = 13.5 V; -40°C < T_j < 125°C; V_{INH} > 3.5 V; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Power supply ripple rejection	*PSRR*	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Reset Generator						
Switching threshold	$V_{Q,rt}$	4.5	4.65	4.8	V	V_{RADJ} = 0 V
Reset adjust threshold	$V_{RADJ,th}$	1.26	1.35	1.44	V	V_Q > 3.5 V
Reset low voltage	$V_{RO,l}$	–	0.10	0.40	V	I_{RO} = 1 mA
Saturation voltage	$V_{D,sat}$	–	50	100	mV	V_Q < $V_{R,th}$
Upper timing threshold	V_{DU}	1.45	1.70	2.05	V	–
Lower reset timing threshold	V_{DRL}	0.20	0.35	0.55	V	–
Charge current	$I_{D,ch}$	40	60	85	µA	–
Reset delay time	t_{rd}	1.3	2.8	4.1	ms	C_D = 100 nF
Reset reaction time	t_{rr}	0.5	1.2	4	µs	C_D = 100 nF
Watchdog						
Discharge current	$I_{D,wd}$	4.40	6.25	9.10	µA	V_D = 1.0 V
Upper timing threshold	V_{DU}	1.45	1.70	2.05	V	–
Lower timing threshold	V_{DWL}	0.20	0.35	0.55	V	–
Watchdog trigger time	$T_{WI,tr}$	16	22.5	27	ms	C_D = 100 nF
Inhibit						
Switching voltage	$V_{INH,ON}$	3.6	–	–	V	IC turned on
Turn-OFF voltage	$V_{INH,OFF}$	–	–	0.8	V	IC turned off
Input current	I_{INH}	5	10	25	µA	V_{INH} = 5 V

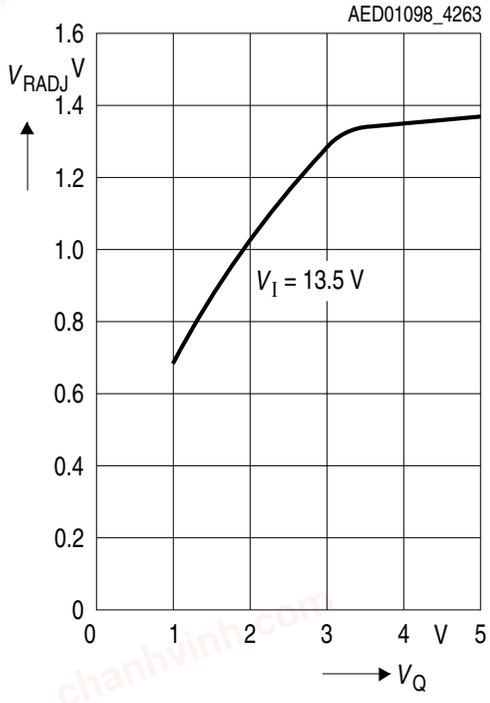
1) Drop voltage = V_i - V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 6 V input).

Note: The reset output is "low" within the range V_Q = 1 V to $V_{Q,rt}$.

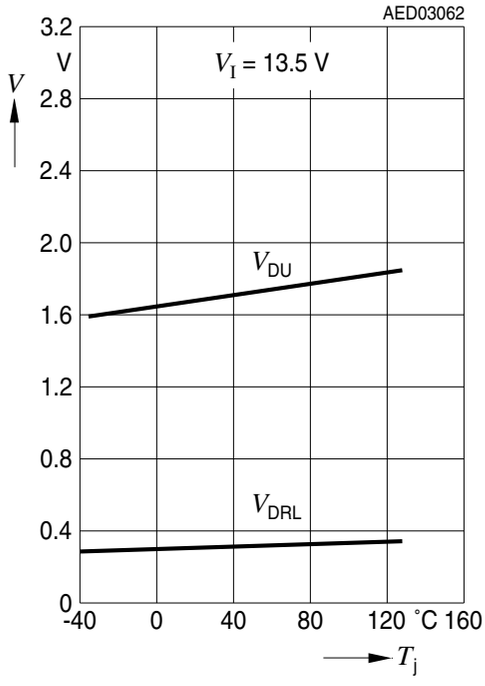
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4.3 Typical performance characteristics

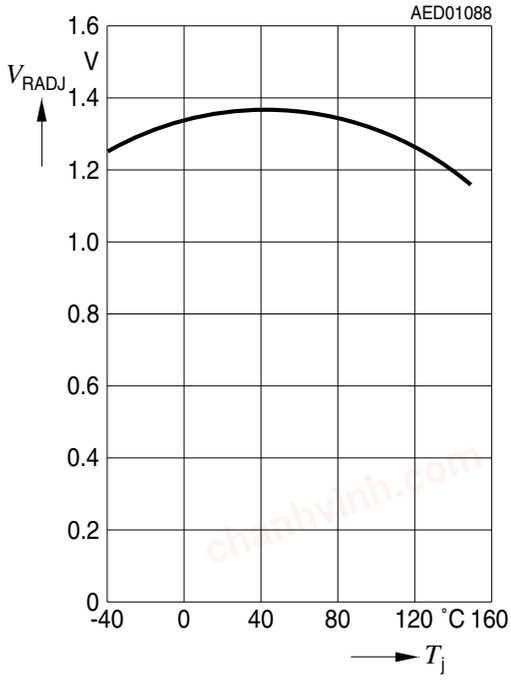
Reset switching threshold versus output voltage



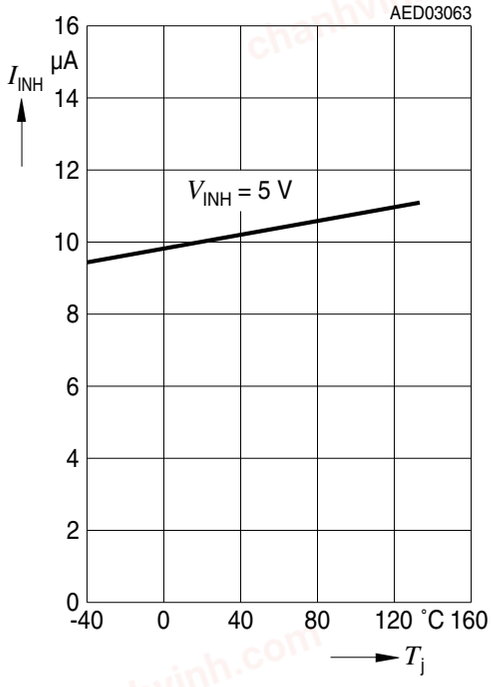
Timing threshold voltage V_{DU} and V_{DRL} versus junction temperature



Reset switching threshold versus junction temperature



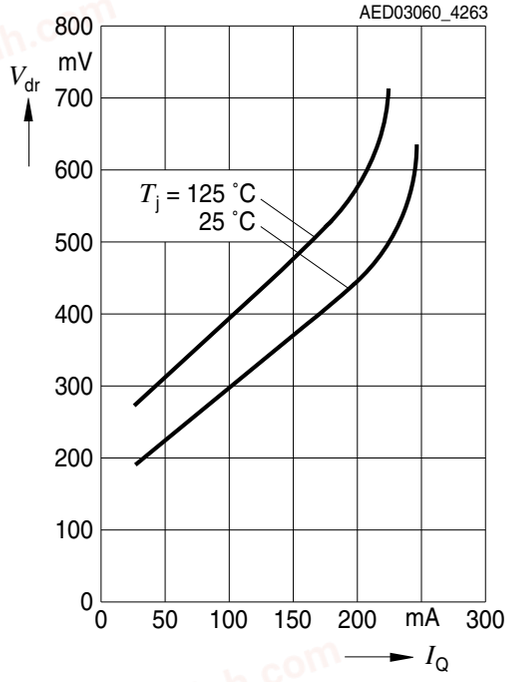
Current consumption of inhibit versus junction temperature



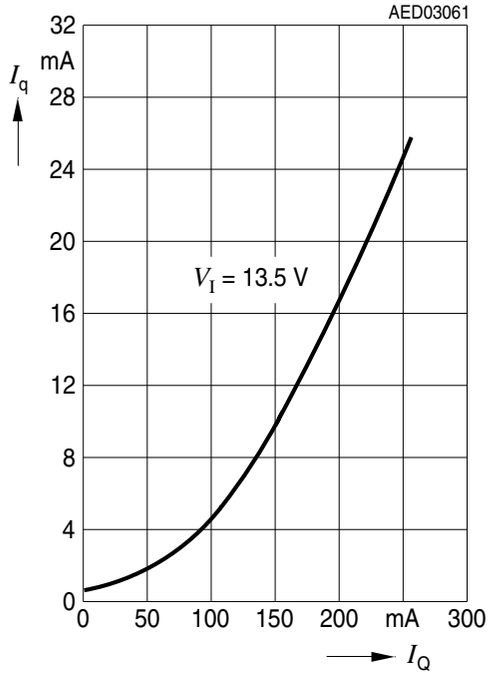
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Functional description

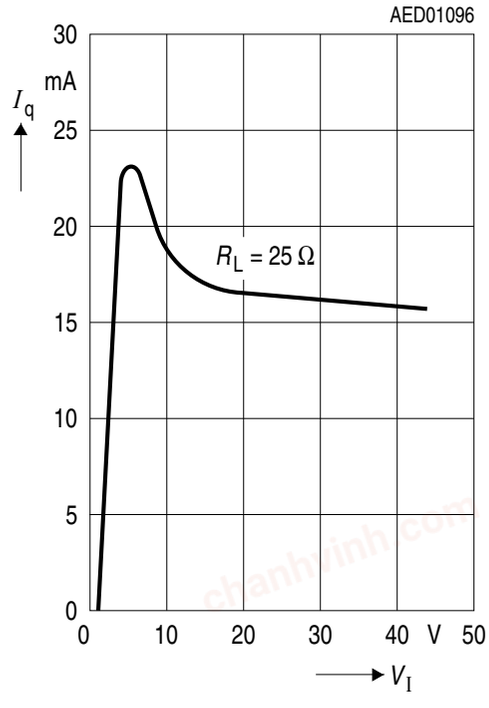
Drop voltage versus output current



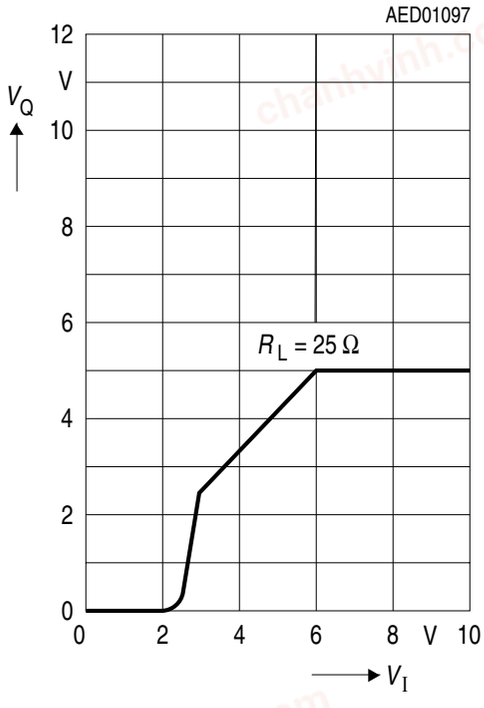
Current consumption versus output current



Current consumption versus input voltage



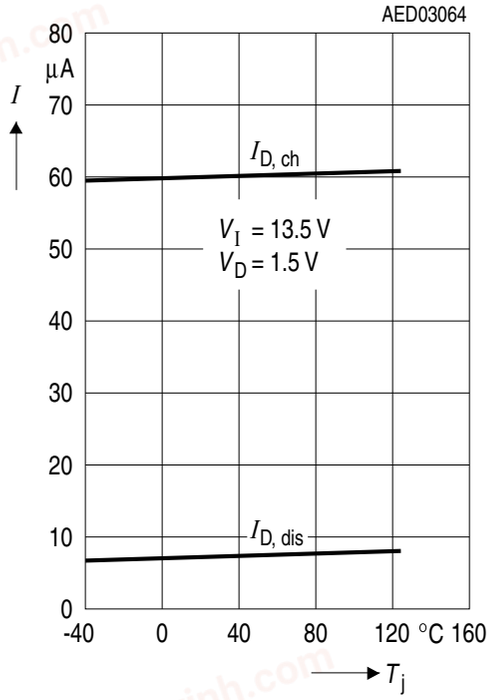
Output voltage versus input voltage



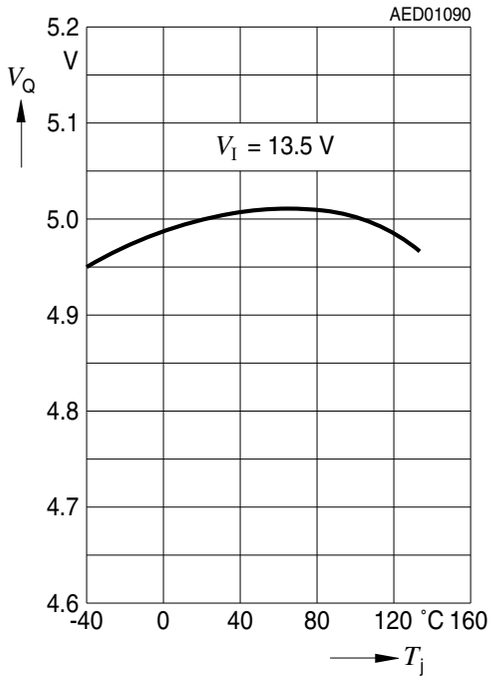
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Functional description

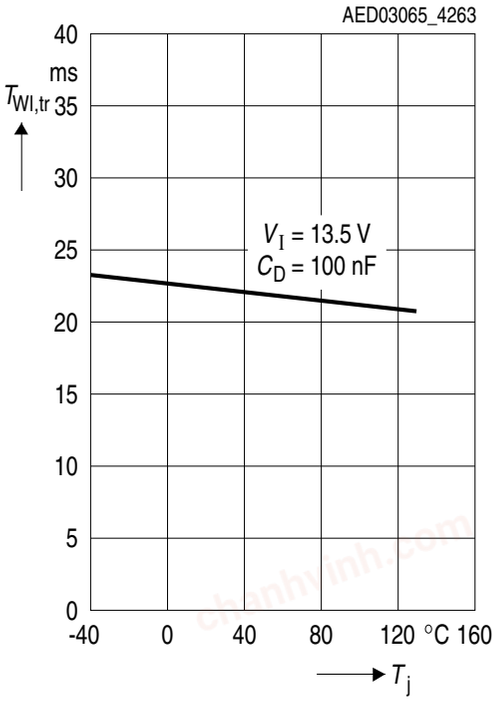
Charge current and discharge current versus junction temperature



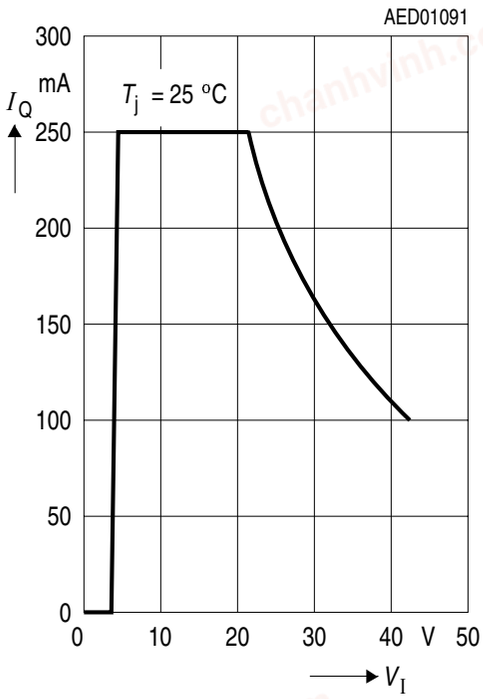
Output voltage versus junction temperature



Pulse time versus junction temperature



Output current versus input voltage



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5 Application information

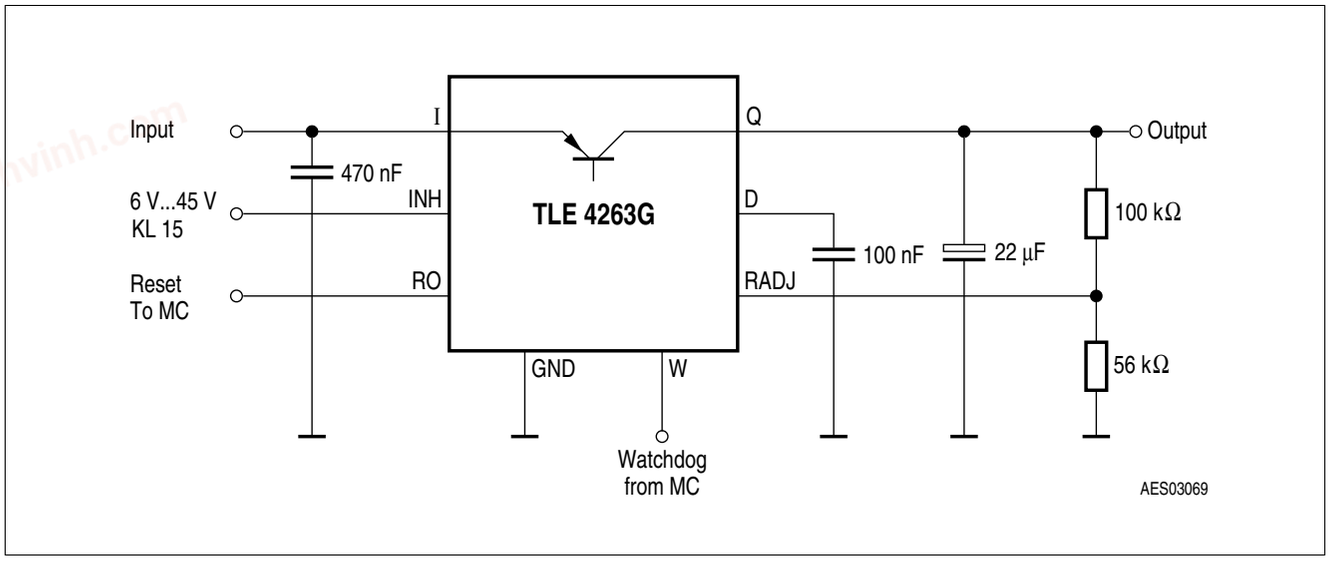


Figure 3 Application circuit

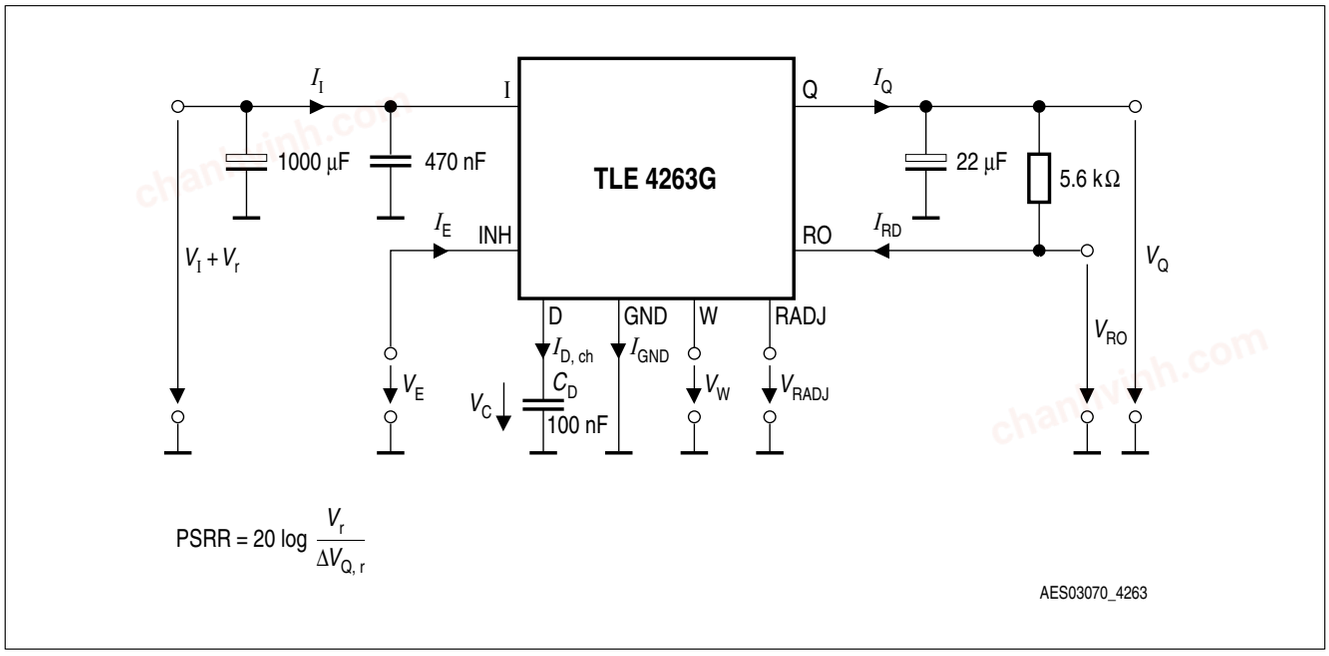


Figure 4 Test circuit

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5.1 Reset timing

The power-on reset delay time is defined by the charging time of an external capacitor C_D which can be calculated as follows:

$$C_D = (t_{rd} \times I_{D,ch})/\Delta V \quad (5.1)$$

Definitions:

- C_D = delay capacitor
- t_{rd} = reset delay time
- $I_{D,ch}$ = charge current, typical 60 µA
- $\Delta V = V_{DU}$, typical 1.70 V
- V_{DU} = upper delay switching threshold at C_D for reset delay time

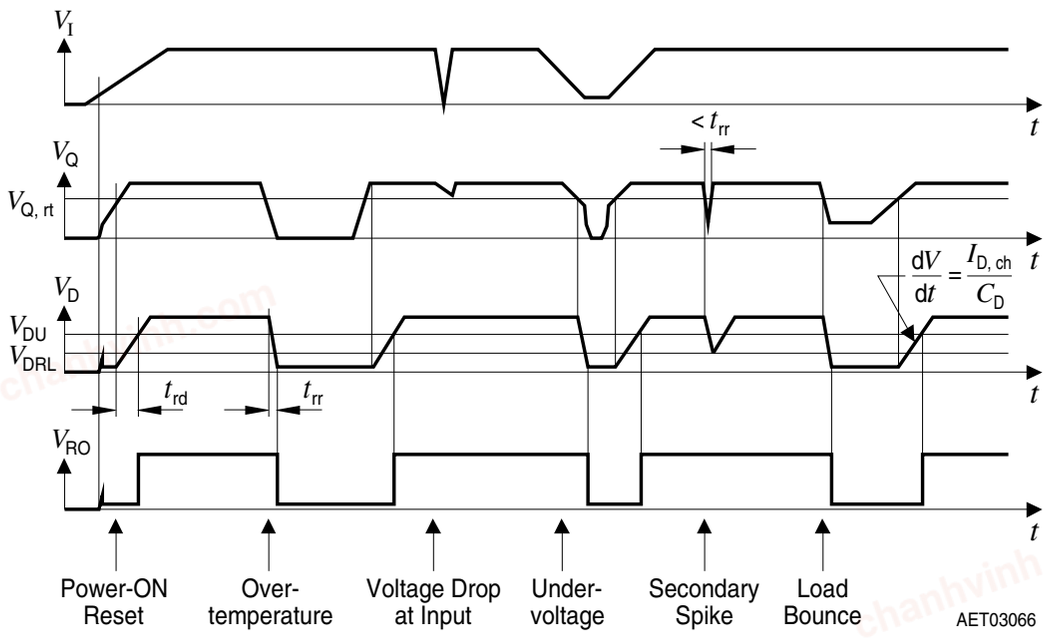


Figure 5 Time response, watchdog with high-frequency clock

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5.2 Reset switching threshold

The present default value is typ. 4.65 V. When using the TLE4263 the reset threshold can be set to 3.5 V < $V_{Q,rt}$ < 4.6 V by connecting an external voltage divider to pin RADJ. The calculation can be easily done since the reset adjust input current can be neglected. If this feature is not needed, the pin must be connected to GND.

$$V_{Q,rt} = (1 + R_1/R_2) \times V_{RADJ,th} \quad (5.2)$$

Definitions:

- $V_{Q,rt}$ = reset threshold
- $V_{RADJ,th}$ = comparator reference voltage, typical 1.35 V

5.3 Watchdog timing

The frequency of the watchdog pulses must be higher than the minimum pulse sequence which is set by the external reset delay capacitor C_D. Calculation can be done according to the formula given in **Figure 6**.

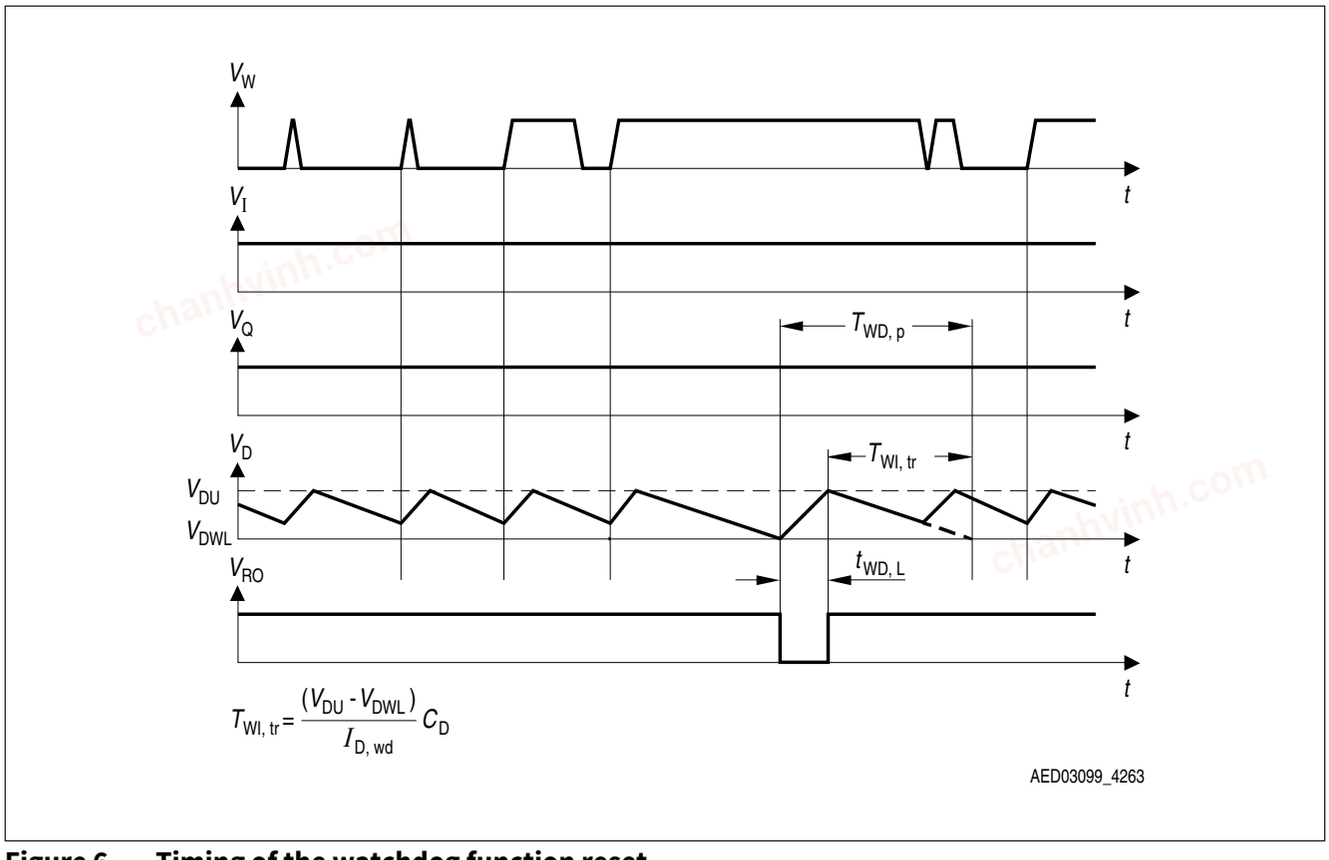
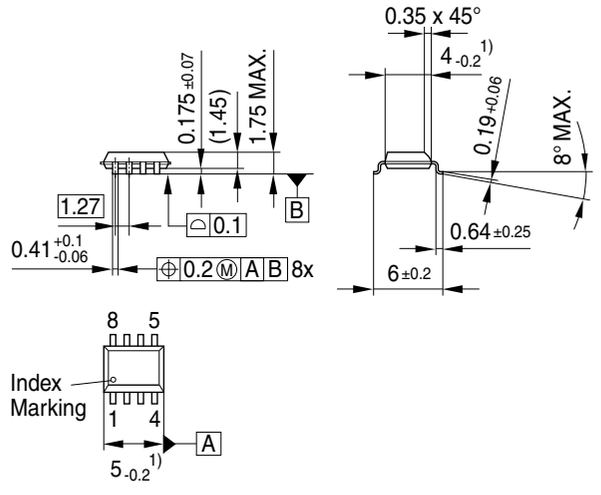


Figure 6 Timing of the watchdog function reset

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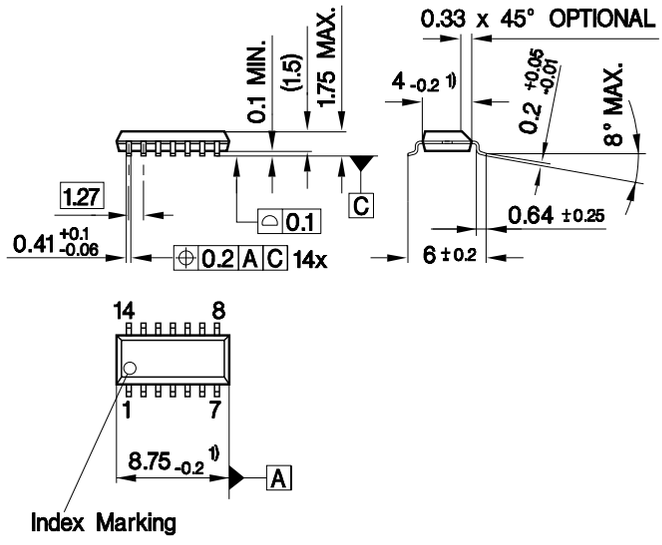
6 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

GPS01229

Figure 7 PG-DSO-8 (Plastic Dual Small Outline)[1)]



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 8 PG-DSO-14 (Plastic Dual Small Outline)[1)]

1) Dimension in mm

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Package information

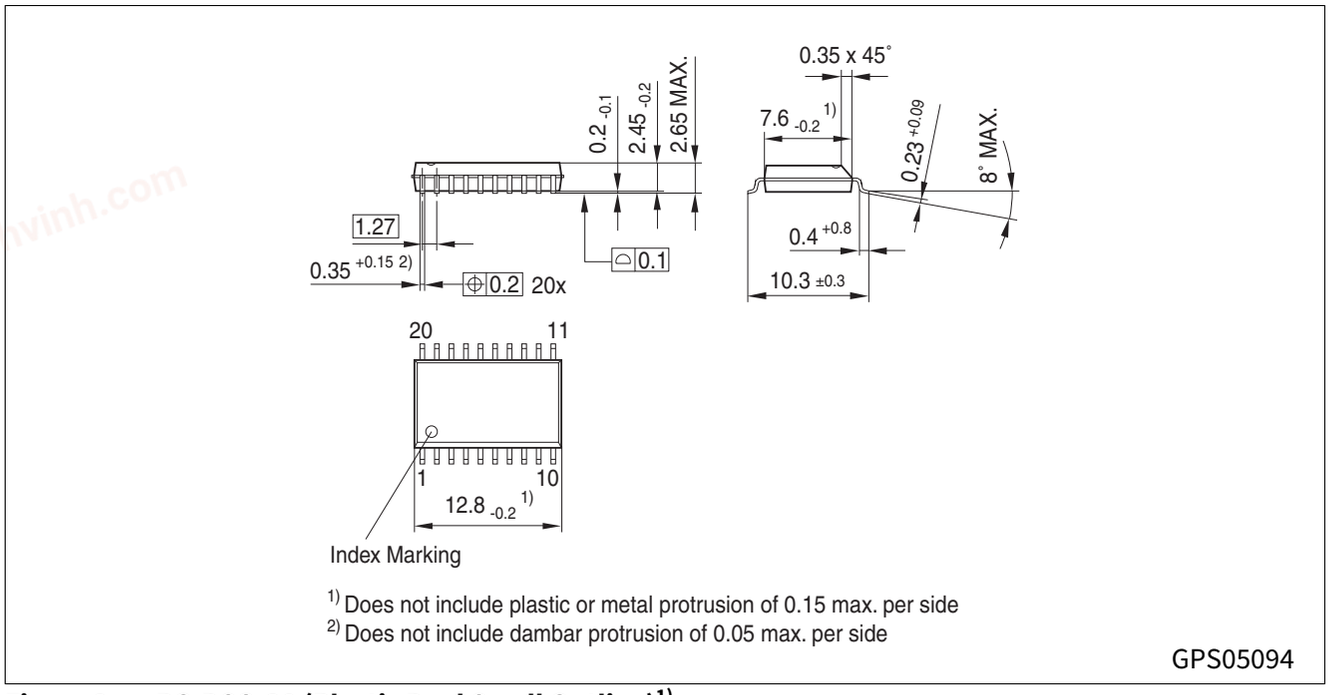


Figure 9 PG-DSO-20 (Plastic Dual Small Outline)[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

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7 Revision history

Revision	Date	Changes
3.0	2018-10-04	Updated layout and structure Page 8: output current changed to output current limitation, add note V_Q = 4.8V Drop voltage: added footnote Updated package drawing “PG-DSO-14” Editorial changes
2.9	2013-11-25	Package version changed: - PG-DSO-20-35 to PG-DSO-20 Package naming harmonized according to Infineon standards: - PG-DSO-8-16 to PG-DSO-8 - PG-DSO-14-30 to PG-DSO-14
2.8	2007-03-20	Initial version of RoHS-compliant derivate of TLE4263 **Page 1**: AEC certified statement added **Page 1** and **Page 16** ff: RoHS compliance statement and Green product feature added **Page 1** and **Page 16** ff: Package changed to RoHS compliant version Legal Disclaimer updated

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