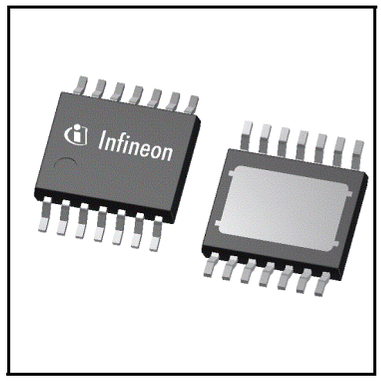
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LITIX™ Power

TLD5099EP - Multitopology LITIX™ Power DC/DC Controller IC

AEC Qualified RoHS



1 Overview

Description

The TLD5099EP is a flexibly usable DC/DC boost controller with built in diagnosis and protection features especially designed to drive LEDs. It also includes a pulse width modulator to easily implement a dimming function with reduced color shifting and a spread spectrum modulator to improve the EMI performance.

It is designed to support fixed current and fixed voltage configurations in multiple topologies such as Boost, Buck, Buck-Boost, SEPIC and Flyback by simply adjusting the external components. The TLD5099EP drives a low side n-channel power MOSFET from an internal 5 V linear regulator.

The switching frequency is adjustable in the range of 100 kHz to 500 kHz and can also be synchronized to an external clock source. A spread spectrum modulator can be activated to improve the EMI, by moving the energy of narrow harmonics peaks over a broadband spectrum.

The TLD5099EP can be flexibly dimmed by means of analog and/or PWM dimming. The enable function reduces the shut-down current consumption to I_{Q_OFF} < 15 µA at 105°C.

The current mode control scheme of this device provides a stable regulation loop maintained by small external compensation components. Additionally an integrated soft start feature limits the current peak as well as voltage overshoot at start-up. This IC is suited for use in the harsh automotive environments.

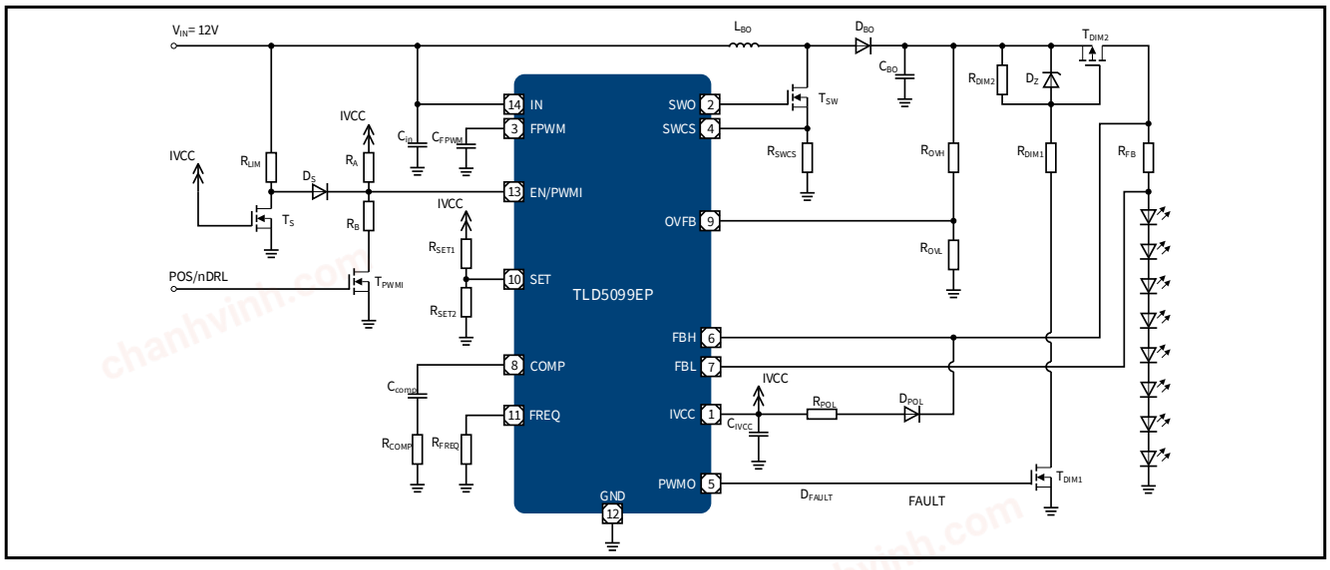


Figure 1 Typical application: Boost LED driver with short circuit protection circuitry

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Potential applications

Type	Package	Marking
TLD5099EP	PG-TSDSO-14	TLD5099

Potential applications

- Automotive exterior and interior lighting
- General illumination
- General purpose current/voltage controlled DC/DC driver

Features

- Fixed current or fixed voltage configuration in Boost, Buck, Buck-Boost, SEPIC and Flyback topology
- Drives low-side external n-channel switching MOSFET from internal 5 V voltage regulator
- Flexible switching frequency range from 100 kHz to 500 kHz with spread spectrum modulator
- Synchronization with external clock source
- Wide input voltage range from 4.5 V to 45 V
- Enable & PWM functions with very low shutdown current: I_{Q_OFF} < 15 µA at 105°C
- Analog dimming and PWM dimming feature (embedded or external) to adjust average LED current
- PWMO gate driver for PWM dimming and output disconnection

Table 1 Product summary

Feature	Symbol	Range
Nominal supply voltage range	V_{IN}	8 V ... 34 V
Extended supply voltage range	V_{IN}	4.5 V ... 45 V $V_{IVCC} > V_{IVCC,RTH,d}$; parameter deviations possible
Switching frequency range	f_{FREQ}	100 kHz ... 500 kHz oscillator frequency adjustment range 250 kHz ... 500 kHz synchronization frequency capture range
Maximum duty cycle	$D_{max,fixed}$	91% fixed frequency mode
	$D_{max,sync}$	88% synchronization mode
Gate driver peak sourcing current	$I_{SWO,SRC}$	380 mA (typical)
Gate driver peak sinking current	$I_{SWO,SNK}$	550 mA (typical)

Protection and diagnostic functions

- Open circuit and short-to-ground detection
- Output overvoltage protection
- Short to GND protection
- Overtemperature shutdown
- Electrostatic discharge (ESD) protection

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

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2 Block diagram

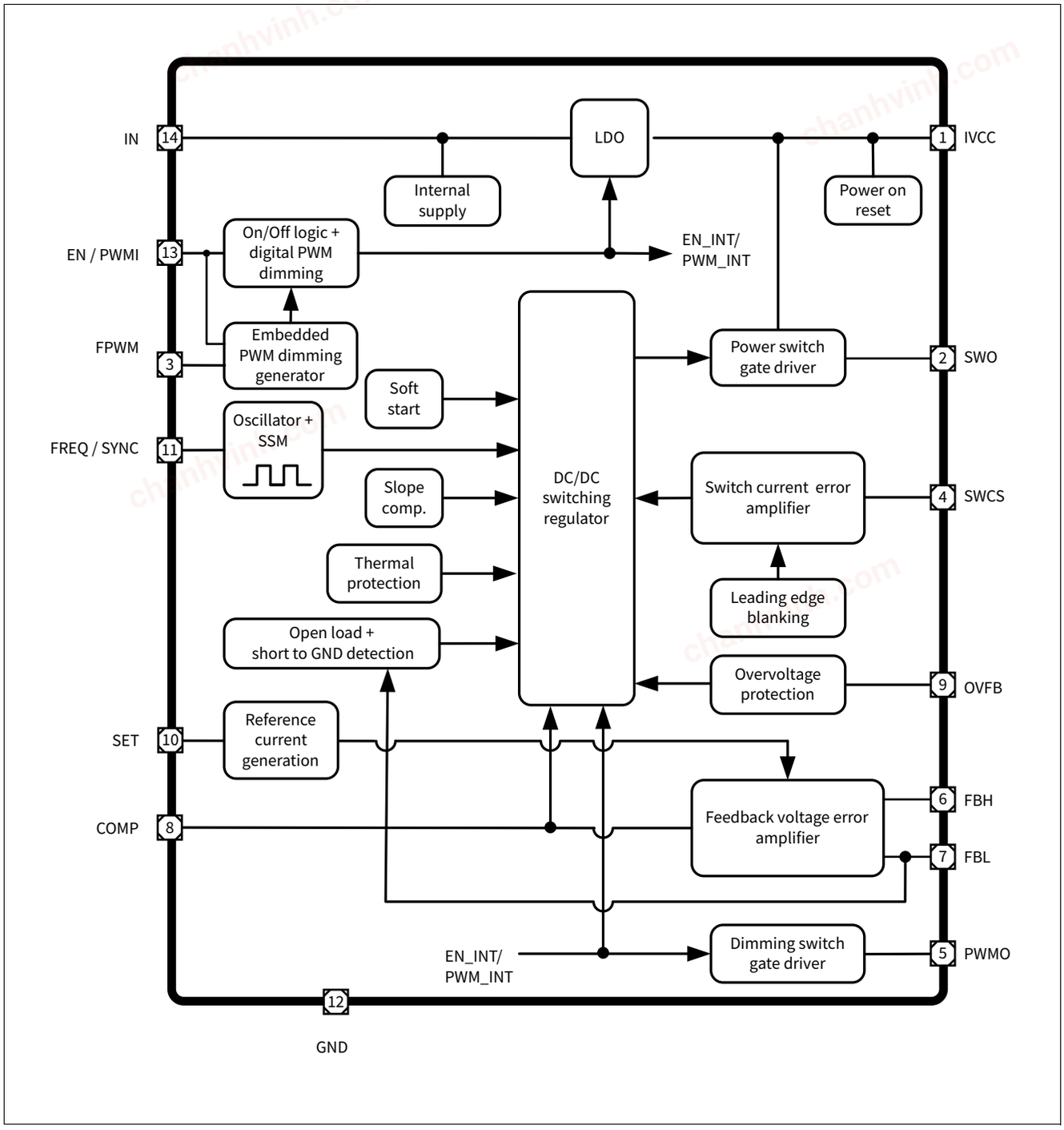


Figure 2 Block diagram of TLD5099EP

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3 Pin configuration

3.1 Pin assignment

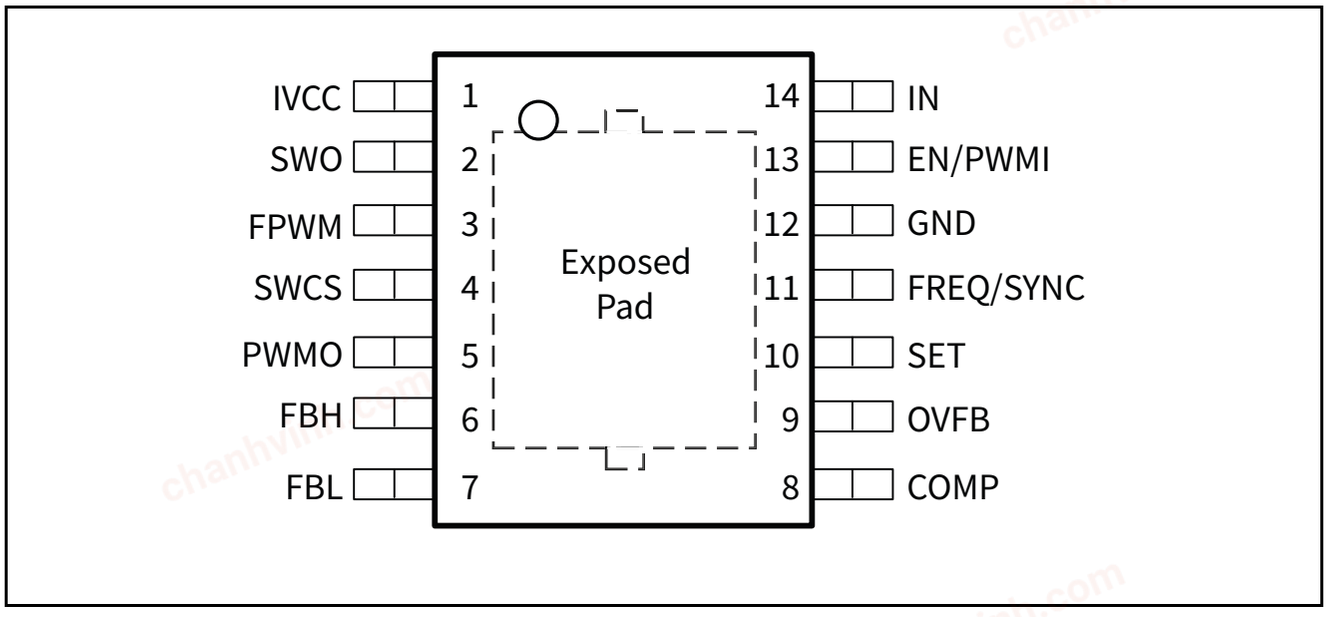


Figure 3 Pin configuration TLD5099EP

3.2 Pin definitions and functions

Table 2 Pin definition and function

#	Symbol	Direction	Function
1	IVCC	Output	**Internal LDO** Used for internal biasing and gate drive. Bypass with external capacitor. Pin must not be left open
2	SWO	Output	**Switch gate driver** Connect to gate of external switching MOSFET
3	FPWM	Output	**PWM frequency selector** Connect external capacitor to set PWM frequency
4	SWCS	Input	**Current sense** Detects the peak current through switch
5	PWMO	Output	**PWM dimming** Connect to gate of external MOSFET
6	FBH	Input	**Voltage feedback positive** Non inverting Input (+)
7	FBL	Input	**Voltage feedback negative** Inverting Input (-)
8	COMP	Input	**Compensation** Connect R and C network to pin for control loop stability

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Pin configuration

Table 2 Pin definition and function

#	Symbol	Direction	Function
9	OVFB	Input	**Overvoltage protection feedback** Connect to resistive voltage divider to set overvoltage threshold
10	SET	Input	**Analog dimming** Load current adjustment Pin. Pin must not be left open. If analog dimming feature is not used connect to IVCC pin
11	FREQ / SYNC	Input	**Frequency select or synchronization** Connect external resistor to GND to set frequency (two resistor sets are defined for activating or deactivating the Spread Spectrum Modulator)
12	GND	–	**Ground** Connect to system ground
13	EN / PWMI	Input	**Enable or PWM** Apply logic “low” signal to disable device and put it in low current consumption. Apply logic “high” signal to enable device or PWM signal for dimming LED. Apply an analog signal (in a proper range) to enable a PWM engine which works at a defined duty cycle
14	IN	Input	**Supply** Supply for internal biasing
	EP	–	**Exposed Pad** Connect to external heat spreading GND Cu area (e.g. inner GND layer of multilayer PCB with thermal vias)

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4 General product characteristics

4.1 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 3 Absolute maximum ratings[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage							
IN Supply input	V_{IN}	-0.3	–	45	V	–	P_4.1.1
EN / PWMI Enable or PWM input	V_{EN}	-40	–	45	V	–	P_4.1.2
FBH-FBL Feedback error amplifier differential	V_{FBH}-V_{FBL}	-40	–	61	V	The maximum delta must not exceed 61 V Differential signal (not referred to GND)	P_4.1.3
FBH Feedback error amplifier positive input	V_{FBH}	-40	–	61	V	The difference between V_{FBH} and V_{FBL} must not exceed 61 V, refer to P_4.1.3	P_4.1.4
FBL Feedback error amplifier negative input	V_{FBL}	-40	–	61	V	The difference between V_{FBH} and V_{FBL} must not exceed 61 V, refer to P_4.1.3	P_4.1.5
FBH and FBL current Feedback error amplifier inputs	I_{FBL}, I_{FBH}	–	1	–	mA	t < 100 ms, V_{FBH} - V_{FBL} = 0.3 V	P_4.1.6
OVFB Overvoltage feedback input	V_{OVFB}	-0.3	–	5.5	V	–	P_4.1.7
OVFB Overvoltage feedback input	V_{OVFB}	-0.3	–	6.2	V	t < 10 s	P_4.1.8
SWCS Switch current sense Input	V_{SWCS}	-0.3	–	5.5	V	–	P_4.1.9
SWCS Switch current sense input	V_{SWCS}	-0.3	–	6.2	V	t < 10 s	P_4.1.10
SWO Switch gate drive output	V_{SWO}	-0.3	–	5.5	V	–	P_4.1.11

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Table 3 Absolute maximum ratings[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SWO Switch gate drive output	V_{SWO}	-0.3	–	6.2	V	t < 10 s	P_4.1.12
FPWM PWM frequency selector	V_{FPWM}	-0.3	–	5.5	V	–	P_4.1.13
FPWM PWM frequency selector	V_{FPWM}	-0.3	–	6.2	V	t < 10 s	P_4.1.14
COMP Compensation input	V_{COMP}	-0.3	–	5.5	V	–	P_4.1.15
COMP Compensation input	V_{COMP}	-0.3	–	6.2	V	t < 10 s	P_4.1.16
FREQ / SYNC Frequency and synchronization input	V_{FREQ} / V_{SYNC}	-0.3	–	5.5	V	–	P_4.1.17
FREQ / SYNC Frequency and synchronization input	V_{FREQ} / V_{SYNC}	-0.3	–	6.2	V	t < 10 s	P_4.1.18
PWMO PWM dimming output	V_{PWMO}	-0.3	–	5.5	V	–	P_4.1.19
PWMO PWM dimming output	V_{PWMO}	-0.3	–	6.2	V	t < 10 s	P_4.1.20
SET Analog dimming	V_{SET}	-0.3	–	45	V	–	P_4.1.21
IVCC Internal linear voltage regulator output	V_{IVCC}	-0.3	–	5.5	V	–	P_4.1.23
IVCC Internal linear voltage regulator output	V_{IVCC}	-0.3	–	6.2	V	t < 10 s	P_4.1.24
Temperature							
Junction temperature	T_J	-40	–	150	°C	–	P_4.1.25
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.26
ESD susceptibility							
ESD resistivity of all pins	V_{ESD_HBM}	-2	–	2	kV	HBM[2)]	P_4.1.27
ESD resistivity of IN, EN/PWMI, FBH, FBL and SET pin to GND	V_{ESD_HBM}	-4	–	4	kV	HBM[2)]	P_4.1.28
ESD resistivity	V_{ESD_CDM}	-500		500	V	CDM[3)]	P_4.1.29
ESD resistivity corner pins	V_{ESD_CDM}	-750		750	V	CDM[3)]	P_4.1.30

1) Not subject to production test, specified by design

2) ESD susceptibility, Human Body Model “HBM” according to AEC Q100-002

3) ESD susceptibility, Charged Device Mode “CDM” according to AECQ100-011 Rev D

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Note:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 4 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Extended supply voltage range	V_{IN}	4.5	–	45	V	1) $V_{IVCC} > V_{IVCC,RTH,d}$; parameter deviations possible	P_4.2.1
Nominal supply voltage range	V_{IN}	8	–	34	V	–	P_4.2.2
Feedback voltage input	V_{FBH}; V_{FBL}	3	–	60	V	–	P_4.2.3
Junction temperature	T_J	-40	–	150	°C	–	P_4.2.4

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For further information visit ***https://www.jedec.org***

Table 5 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	16	–	K/W	1)2)	P_4.3.1
Junction to Ambient	R_{thJA}	–	53	–	K/W	1)3) 2s2p	P_4.3.2
Junction to Ambient	R_{thJA}	–	71	–	K/W	1)3) 1s0p + 600 mm^2	P_4.3.3
Junction to Ambient	R_{thJA}	–	83	–	K/W	1)3) 1s0p + 300 mm^2	P_4.3.4

1) Not subject to production test, specified by design

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). T_A = 25°C dissipates 1 W

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3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 µm Cu) and 2 inner copper layers (2 x 35 µm Cu), A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. T_A = 25°C, IC dissipates 1 W

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5 Switching regulator

5.1 Description

The TLD5099EP regulator is suitable for Boost, Buck, Buck-Boost, SEPIC and Flyback configurations. The constant output current is especially useful for light emitting diode (LED) applications. The switching regulator function is implemented by a pulse width modulated (PWM) current mode controller.

The switching current mode controller uses the peak current through the external power switch and error in the output current to determine the appropriate pulse width duty cycle (on time) for constant output current. The current mode controller provides a modulated signal to an internal gate driver which drives an external n-channel enhancement mode metal oxide field effect transistor (MOSFET) power switch.

The current mode controller also has built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty).

An additional built-in feature is an integrated soft start that limits the current through the inductor and external power switch during initialization. The soft start function gradually increases the inductor and switch current over t_{SS} (P_5.2.9) to minimize potential overvoltage at the output.

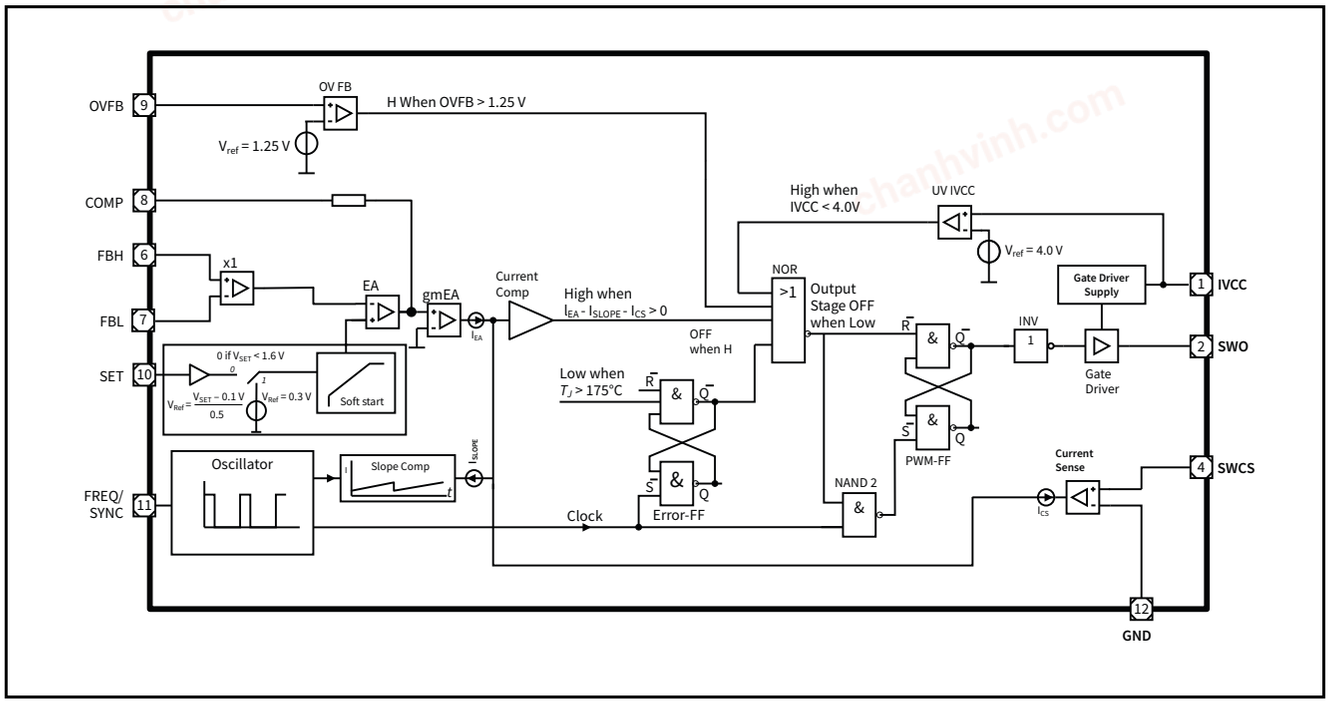


Figure 4 Switching regulator block diagram

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5.2 Electrical characteristics

V_{IN} = 8 V to 34 V; T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 6 Electrical characteristics: Switching regulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Regulator							
Feedback reference voltage	V_{REF}	0.29	0.30	0.31	V	refer to **Figure 36** V_{REF}= V_{FBH} -V_{FBL} V_{SET} = 5 V I_{LED} = 350 mA Differential signal (not referred to GND)	P_5.2.1
Feedback reference voltage	V_{REF}	0.057	0.06	0.063	V	refer to **Figure 36** V_{REF} = V_{FBH} -V_{FBL} V_{SET} = 0.4 V I_{LED} = 70 mA Differential signal (not referred to GND)	P_5.2.2
Feedback reference voltage offset	V_{REF_offset}	–	–	5	mV	refer to **Figure 24** and **Figure 36** V_{REF} = V_{FBH} - V_{FBL} V_{SET} = 0.1 V V_{OUT} > V_{IN} Differential signal (not referred to GND)	P_5.2.3
Voltage line regulation	(ΔV_{REF}/ V_{REF}) / ΔV_{IN}	–	–	0.15	%/V	refer to **Figure 36** V_{IN} = 8 V to 19 V; V_{SET} = 5 V; I_{LED} = 350 mA	P_5.2.4
Voltage load regulation	(ΔV_{REF}/V_{REF}) / ΔI_{BO}	–	–	5	%/A	refer to **Figure 36** V_{SET} = 5 V; I_{LED} = 100 to 500 mA	P_5.2.5
Switch peak overcurrent threshold	V_{SWCS}	125	150	175	mV	V_{FBH} = V_{FBL} = 5 V V_{COMP} = 3.5 V	P_5.2.6
Maximum duty cycle	$D_{MAX,fixed}$	91	–	–	%	Fixed frequency mode	P_5.2.7
Maximum duty cycle	$D_{MAX,sync}$	88	–	–	%	Synchronization mode	P_5.2.8
Soft start ramp	t_{SS}	350	1000	1500	µs	refer to **Figure 36** V_{SET} = 5 V; V_{REF} rising from 5% to 95% of typ. V_{REF}	P_5.2.9

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Table 6 Electrical characteristics: Switching regulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IFBH Feedback high input current	I_{FBH}	38	46	54	µA	V_{FBH} - V_{FBL}= 0.3 V	P_5.2.10
IFBL Feedback low input current	I_{FBL}	15	21	27	µA	V_{FBH} -V_{FBL} = 0.3 V	P_5.2.11
Switch current sense input current	I_{SWCS}	10	50	100	µA	V_{SWCS}= 150 mV	P_5.2.12
Input undervoltage shutdown	$V_{IN,off}$	3.5	–	4.5	V	V_{IN} decreasing	P_5.2.13
Input voltage startup	$V_{IN,on}$	–	–	4.85	V	V_{IN} increasing	P_5.2.14
Gate driver for external switch							
Gate driver peak sourcing current	$I_{SWO,SRC}$	–	380	–	mA	1) V_{SWO} = 1 V to 4 V Current flows out of pin	P_5.2.15
Gate driver peak sinking current	$I_{SWO,SNK}$	–	550	–	mA	1) V_{SWO} = 4 V to 1 V	P_5.2.16
Gate driver output rise time	$t_{R,SWO}$	–	30	60	ns	1) $C_{L,SWO}$ = 3.3 nF; V_{SWO} = 1 V to 4 V	P_5.2.17
Gate driver output fall time	$t_{F,SWO}$	–	20	40	ns	1) $C_{L,SWO}$ = 3.3 nF; V_{SWO}= 4 V to 1 V	P_5.2.18
Gate driver output voltage	V_{SWO}	4.5	–	5.5	V	1) $C_{L,SWO}$ = 3.3 nF	P_5.2.19

1) Not subject to production test, specified by design

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6 Switching oscillator and synchronization

6.1 Description

RFREQ vs. switching frequency

The internal oscillator is used to determine the switching frequency of the regulator. The switching frequency (from 100 kHz to 500 kHz) and the status of spread spectrum modulator can be selected with an external resistor referred to GND.

The range scale of the usable resistor is divided in two sections; for lower values of resistor it selects the switching frequency with the spread spectrum modulator “on”, while for higher values of the range it selects the switching frequency with the spread spectrum modulator “off”.

To set the desired switching frequency with spread spectrum modulator “off”, the external resistor value is calculated by means of the formula shown below and is summarized in **Figure 7**.

(6.1)

$$R_{FREQ-SSMoff} = \frac{1}{\left(340 \cdot 10^{-12} \cdot f_{FREQ}\right)^{1.13}}$$

To set the desired switching frequency with spread spectrum modulator “on”, the external resistor value is calculated by means of the formula shown below.

(6.2)

$$R_{FREQ-SSMon} = \frac{1}{\left(600 \cdot 10^{-12} \cdot f_{FREQ}\right)^{0.943}} - (600)$$

In addition, the oscillator is capable of changing from the frequency set by the external resistor to a synchronized frequency from an external clock source. If an external clock source is provided on the pin FREQ/SYNC, then the internal oscillator synchronizes to this external clock frequency and the boost regulator switches at the synchronized frequency. The synchronization frequency capture range is 250 kHz to 500 kHz.

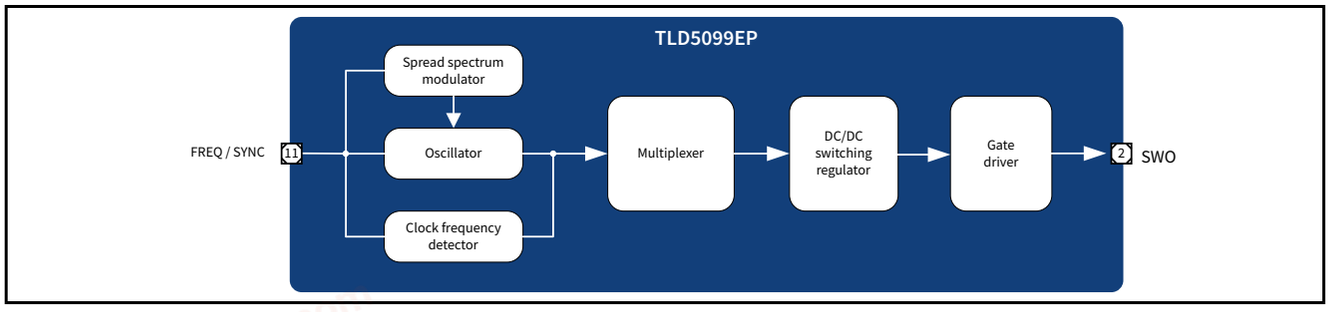


Figure 5 Oscillator and synchronization block diagram

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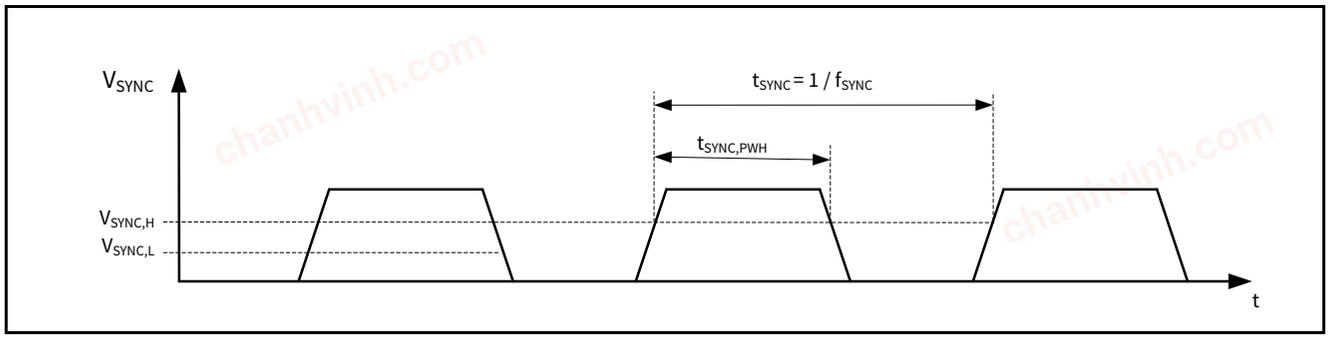


Figure 6 Synchronization timing diagram

6.2 Electrical characteristics

V_{IN} = 8 V to 34 V; T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 7 Electrical characteristics: Oscillator and synchronization

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Oscillator							
Oscillator frequency	f_{FREQ}	250	300	350	kHz	R_{FREQ} = 33 kΩ	P_6.2.1
Oscillator frequency adjustment range	f_{FREQ}	100	–	500	kHz	–	P_6.2.2
FREQ / SYNC supply current	I_{FREQ}	–	–	3	mA	V_{FREQ} = 0 V	P_6.2.3
Frequency voltage	V_{FREQ}	0.56	0.6	0.64	V	R_{FREQ} = 33 kΩ (f_{FREQ} = 300 kHz)	P_6.2.4
Synchronization							
Synchronization frequency capture range	f_{SYNC}	250	–	500	kHz	–	P_6.2.5
Synchronization signal high logic level valid	$V_{SYNC,H}$	3.0	–	–	V	1)2)	P_6.2.6
Synchronization signal low logic level valid	$V_{SYNC,L}$	–	–	0.8	V	1)2)	P_6.2.7
Synchronization signal logic high pulse width	$t_{SYNC,PWM}$	200	–	–	ns	1)2)	P_6.2.8

1) Synchronization of external PWM “on” signal to falling edge
2) Not subject to production test, specified by design

Note: Maximum capacitor on pin FREQ / SYNC has to be less than 150 pF (including parasitics effect)

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6.3 Typical performance characteristics of oscillator

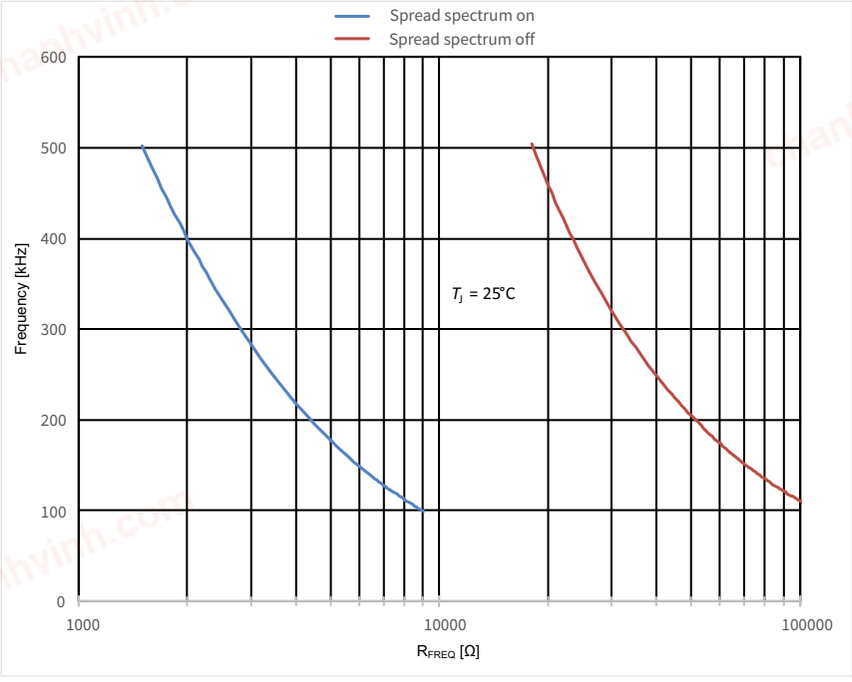


Figure 7 Switching frequency f_{SW} versus frequency select resistor to GND R_{FREQ}

Table 8 Switching frequency f_{SW} versus frequency select resistor to GND R_{FREQ}

R_{FREQ} [kΩ]	f_{SW} [kHz]	Spread spectrum
1.8	435	ON
2.2	370	
2.7	311	
3.3	260	
3.9	224	
4.7	188	
5.6	159	
6.8	132	
8.2	110	
22	422	OFF
27	352	
33	295	
39	254	
47	216	
56	185	
68	156	
82	132	

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6.4 Spread spectrum

The spread spectrum modulation technique significantly improves the EMI performance in the lower frequency range of the spectrum (e.g. f < 30 MHz).

By using the spread spectrum technique, it is possible to optimize the input and output filters to fulfill the EMC requirements. Moreover, the need for low ESR input capacitors is relaxed because the input capacitor series resistor is important for the low frequency filter characteristic. This can be an economic benefit if there is a strong requirement for average limits.

The modulation frequency f_{FM}, (P_6.4.1) is internally fixed, while the modulation depth is a fraction of the switching frequency f_{DEV}, (P_6.4.2).

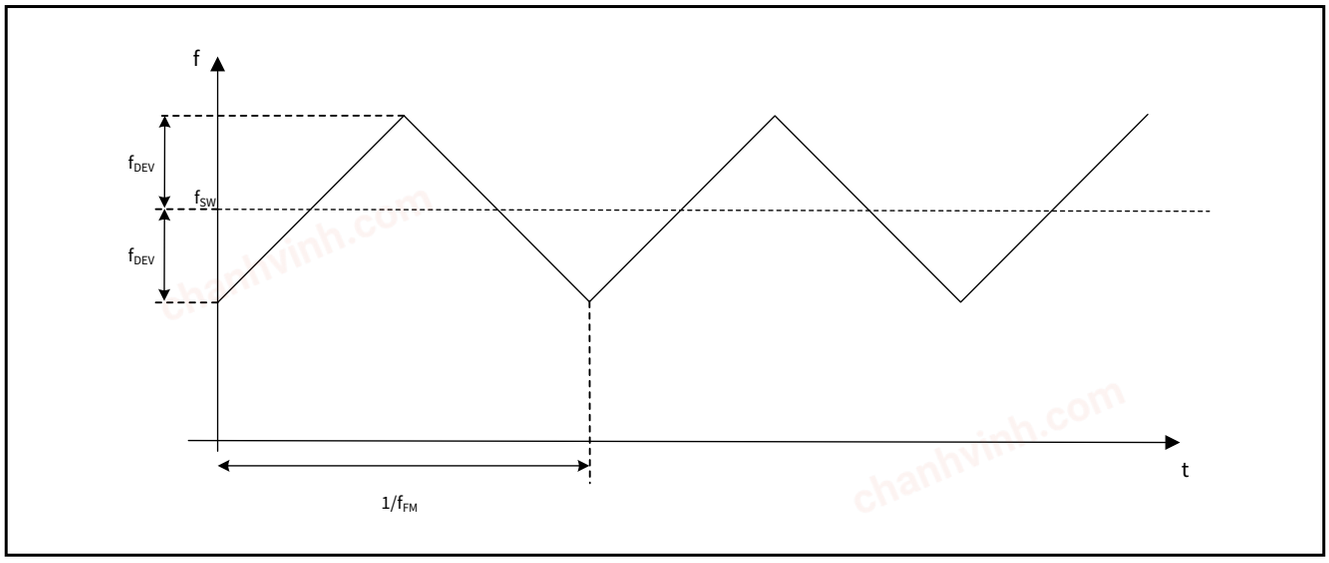


Figure 8 Spread spectrum modulator

Table 9 Electrical characteristics: Spread spectrum modulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Modulation frequency	f_{FM}	–	7	–	kHz	1) 1.5 kΩ ≤ R_{FREQ} ≤ 9 kΩ	P_6.4.1
Modulation depth	f_{DEV}	–	15	–	%	1) Related to switching frequency f_{FREQ} 1.5 kΩ ≤ R_{FREQ} ≤ 9 kΩ	P_6.4.2

1) Not subject to production test, specified by design

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7 Enable and dimming function

7.1 Description

Enable and dimming functions are related on the status of the pin **EN / PWMI**.

For different values of the voltage on this pin, the device has different behaviors as described below:

- If a valid logic “low” is present (it means $V_{EN/PWMI} < V_{EN/PWMI,OFF}$), the device is powered off (refer to **Chapter 7.2**)
- If a valid logic “high” is present (it means $V_{EN/PWMI} > V_{EN/PWMI,ON}$), the device is powered on and it can accept a digital PWM (refer to **Chapter 7.3**)
- If an analog signal is in between $V_{EN/PWMI,DC_0}$ and $V_{EN/PWMI,DC_100}$, the device and the embedded PWM engine are powered on (refer to **Chapter 7.4**)

7.2 Enable function

The enable function powers the device on or off. At the start-up or if a valid logic low signal on enable pin **EN / PWMI** for a time longer than $t_{EN,OFF,DEL}$ (P_7.5.5) powers off the device; in this case, the current consumption is less than I_{Q_OFF} (P_7.5.23).

At the start-up, to fully activate the device, a valid logic high has to be present while the **IVCC** reaches the level $V_{IVCC,RTH,i}$ (P_8.2.8)

The enable function features an integrated pull down resistor R_{EN_INT} (P_7.5.12), which ensures that the IC is shut down and the power switch is off in case the enable pin EN is left open.

7.3 Digital PWM dimming function

The digital PWM dimming function is activated when a valid logic high/low pattern is present on **EN / PWMI**. The **EN / PWMI** signal enables and disable the gate drivers (in accordance with the logic signal present in the pin) and modulates the average current on the load. The internal blocks involved in this function are shown in **Figure 9**.

When PWM logic is activated, the device differentiates between enable off and PWM dimming signal by requiring the enable off at the **EN / PWMI** pin to stay low for the **Enable turn off delay time** (P_7.5.5). The pattern and the timing constraints are shown in **Figure 10**.

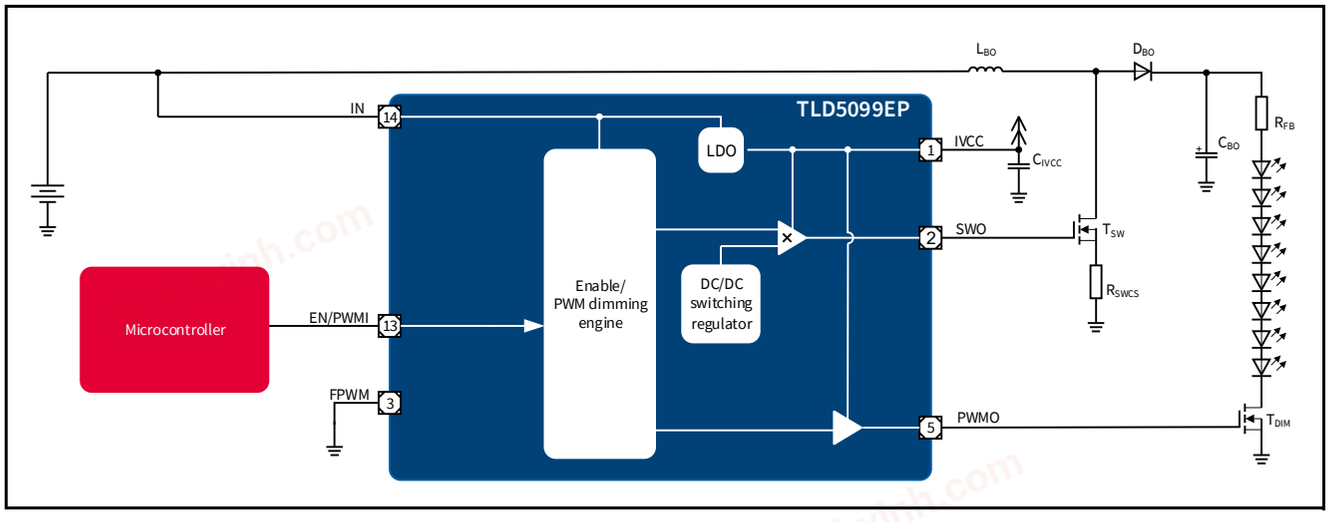


Figure 9 Block diagram and simplified application circuit enable and LED dimming

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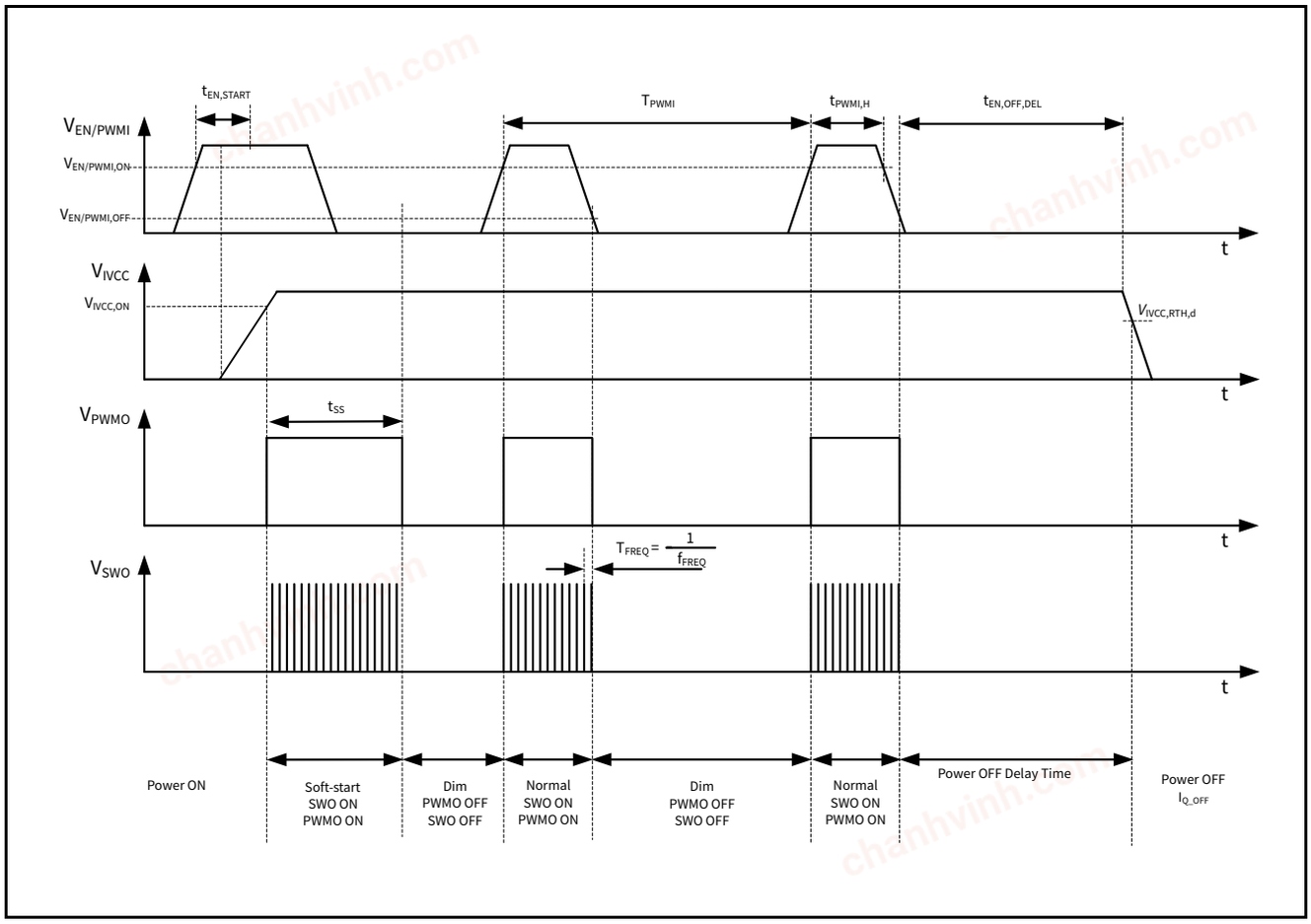


Figure 10 Timing diagram enable and LED dimming

Note: The slope of the V_{IVCC} is related to the filter capacitor. Therefore its steady state condition can be achieved after $t_{EN,START}$.

7.4 Embedded PWM dimming function

The embedded PWM dimming function (PWM engine) is activated in the voltage window in between a valid logic “low” level and a valid logic “high” level (P_7.5.8. and P_7.5.9, respectively). In this voltage window, a duty cycle (DC) on PWMO output is generated according to the analog voltage applied on the pin. The desired DC value can be calculated by the following formula:

(7.1)

$$DC[\%] = \frac{V_{EN/PWMI} - 0.32 \cdot V_{IVCC}}{0.24 \cdot V_{IVCC}} \cdot 100[\%]$$

On calculation of the $V_{EN/PWMI}$ voltage, the pull-down resistor (P_7.5.12) that features the shut down when the pin is left open, has to be taken into account. If this value is taken into account and a voltage divider between IVCC and ground is used (**Figure 12**), the DC can be described by the following formula:

(7.2)

$$DC[\%] = \frac{\frac{R_B \parallel R_{EN_INT}}{R_B \parallel R_{EN_INT} + R_A} - 0.32}{0.24} \cdot 100[\%]$$

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Enable and dimming function

The frequency of PWMO signal is also programmable by changing the value of the capacitor on the pin **FPWM**; two internal current generators charge and discharge the capacitor and this signal supplies an internal divider to produce the desired frequency (**Figure 12**).

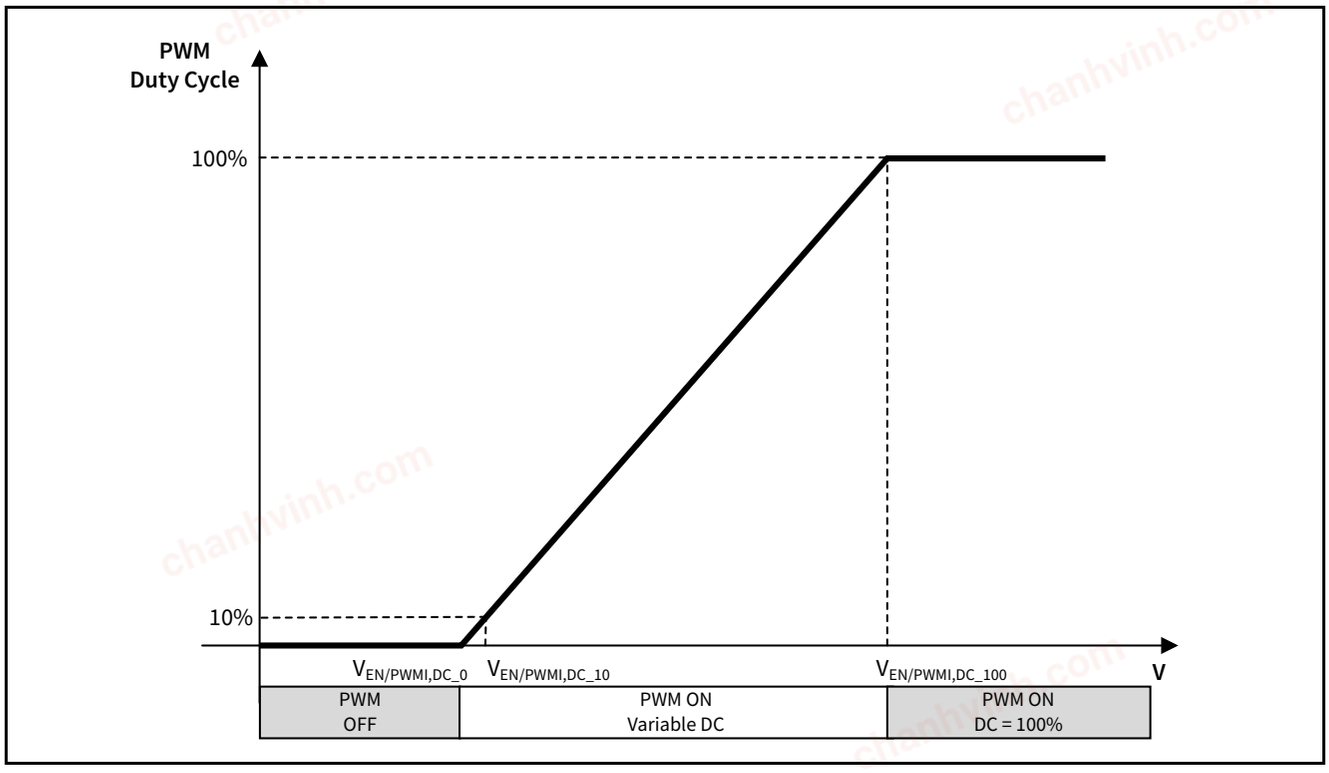


Figure 11 Duty cycle variation as a function of $V_{EN/PWMI}$

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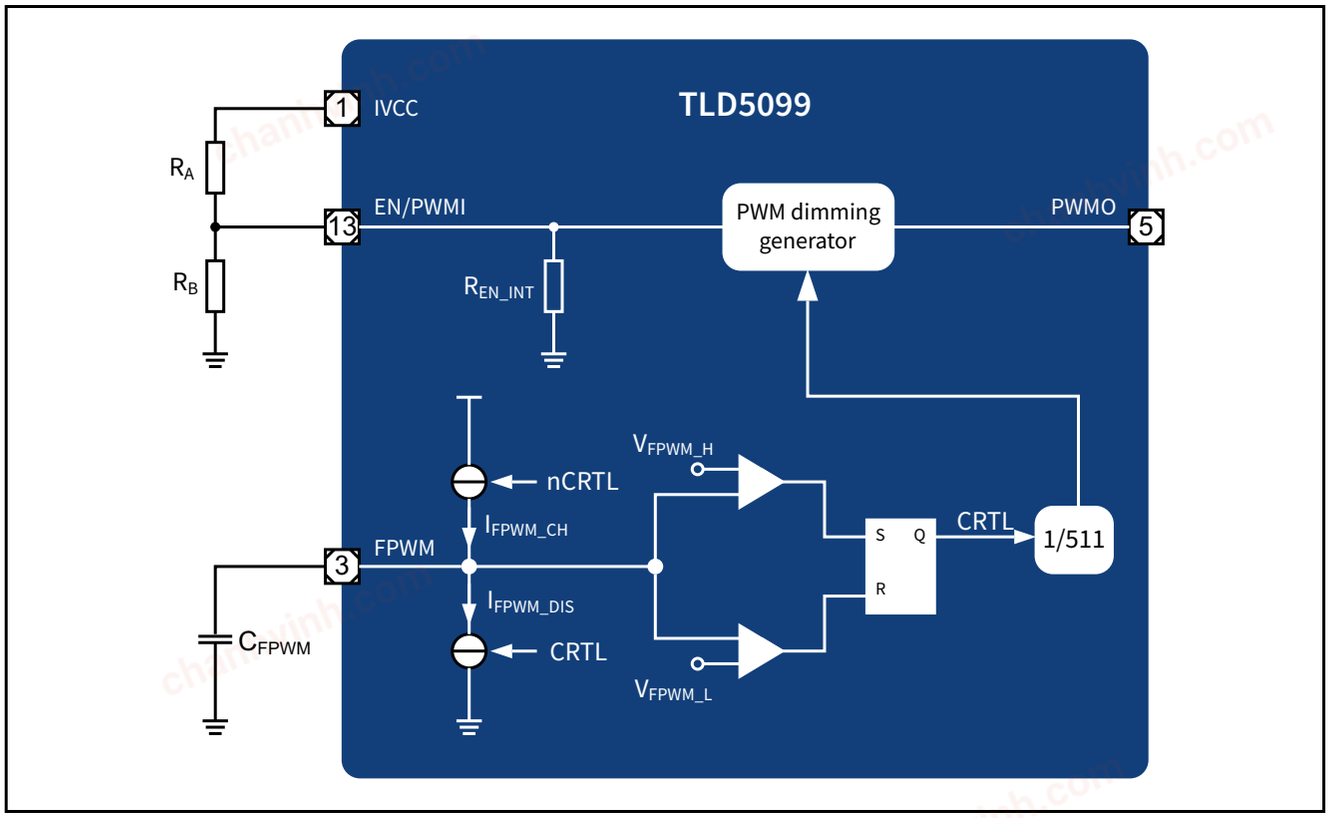


Figure 12 Block diagram of PWM engine

The relation between PWM frequency and the capacitor is described by the following formula:

(7.3)

$$f_{PWMO} = \frac{1}{511 \cdot C_{FPWM} \cdot (V_{FPWM_H} - V_{FPWM_L}) \cdot \left(\frac{1}{|I_{FPWM_CH}|} + \frac{1}{|I_{FPWM_DIS}|} \right)}$$

In the typical case, the variation of f_{PWMO} as a function of C_{FPWM} is shown in **Figure 13**. To have a small impact of parasitic capacitance, it is suggested to put this capacitor quite close to the pin **FPWM**. The signal produced by the PWM engine (with the desired DC and frequency) enables and disables the gate drivers and modulates the average current on the load.

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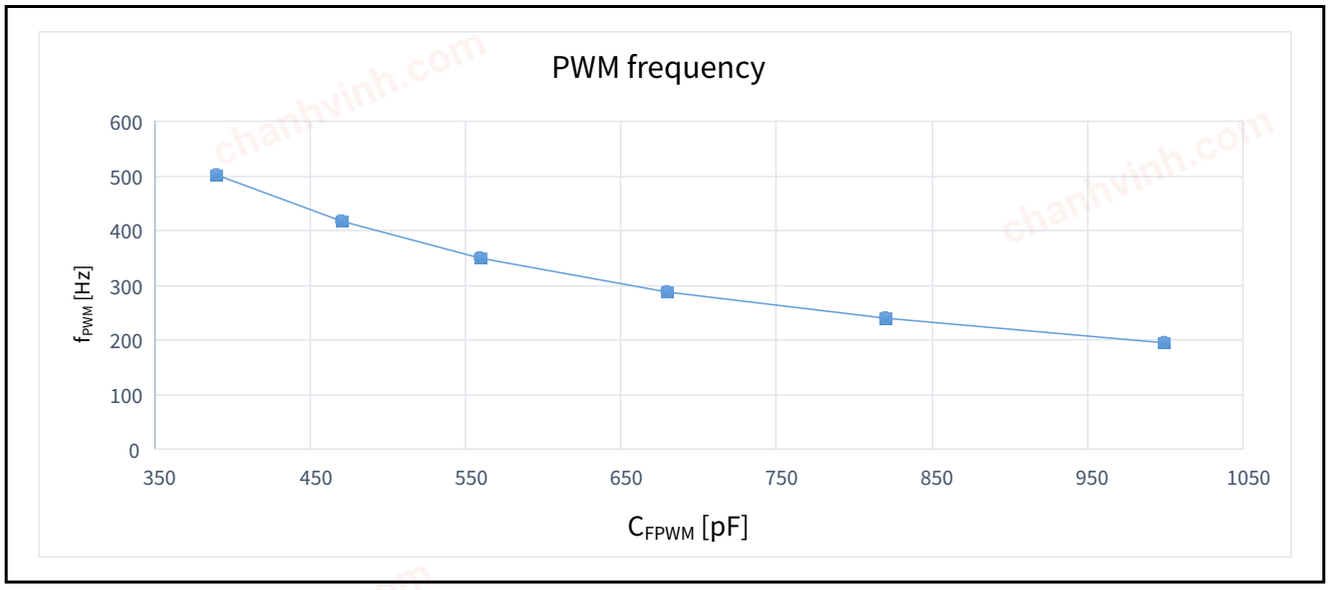


Figure 13 PWM frequency variation as a function of C_{FPWM}

Table 10 Commercial capacitor C_{FPWM} values vs. PWM frequency f_{FPWMO}

C_{FPWM} [pF]	f_{FPWMO} [Hz]
390	502
470	416
560	349
680	288
820	239
1000	196

As reported in **Chapter 7.2**, during the start-up (and only during this phase), the device needs a valid logic high on the pin **EN / PWMI** to wake-up the internal logic. The valid logic high on pin EN/PWMI has to be granted until the voltage of IVCC reaches its steady state (P_8.2.8). A proposal circuit to obtain this behavior is shown in **Figure 14** and the necessary added components are highlighted in the blue box.

It acts as follows:

- at start-up Q1 is off and V_{IN} supplies pin **EN / PWMI** through R_{LIM} and it starts up the circuit
- when the TLD5099EP is ready to work (e.g. the IVCC has reached its steady state), the IVCC switches on Q1 (the current through Q1 is limited by R_{LIM})
- then, the voltage on pin **EN / PWMI** given by the resistor divider R_A, R_B provides the desired duty cycle

The diode D1 ensures the proper behavior for the biasing.

This start-up circuit is needed only if embedded PWM dimming function is used. Proper dimensioning of R_{LIM} and voltage divider (R_A and R_B) resistors is needed to ensure the start-up of the device. As described above, $V_{EN/PWMI}$ has to be higher than $V_{EN/PWMI,ON}$ during start-up. Fixing R_{LIM}, R_B can be calculated as follows:

(7.4)

$$R_B > \frac{V_{EN/PWMI,ON}}{(V_{IN} - V_{D1} - V_{EN/PWMI,ON})} \cdot R_{LIM}$$

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Enable and dimming function

Then, R_A has to be calculated in accordance with the desired duty cycle.

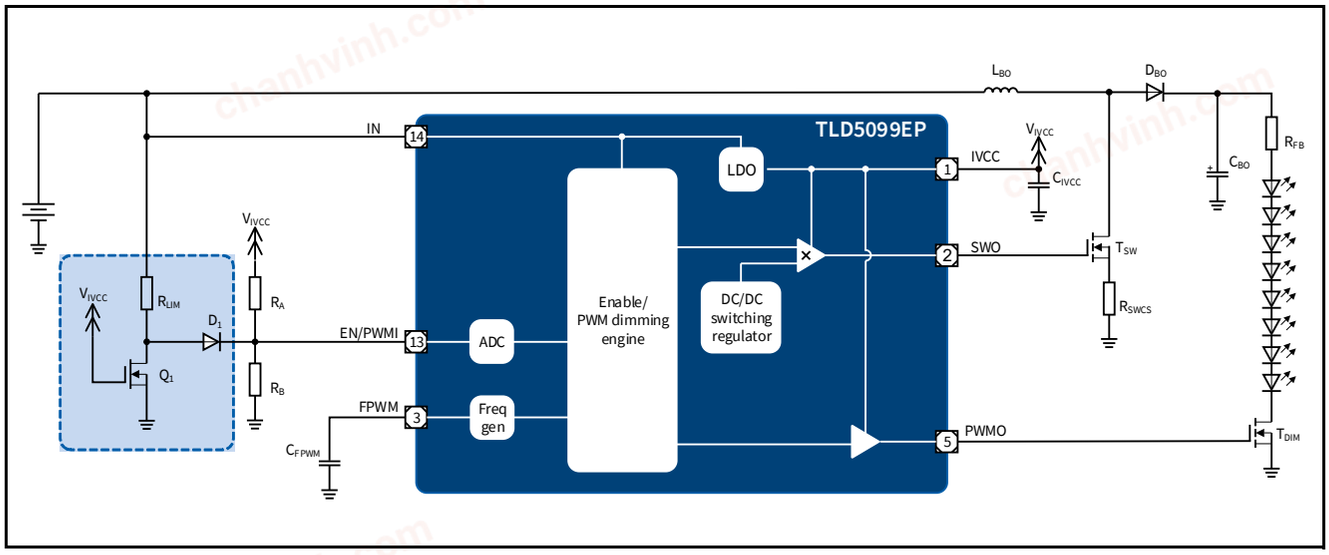


Figure 14 Block diagram of analog PWM dimming with simplified application circuit

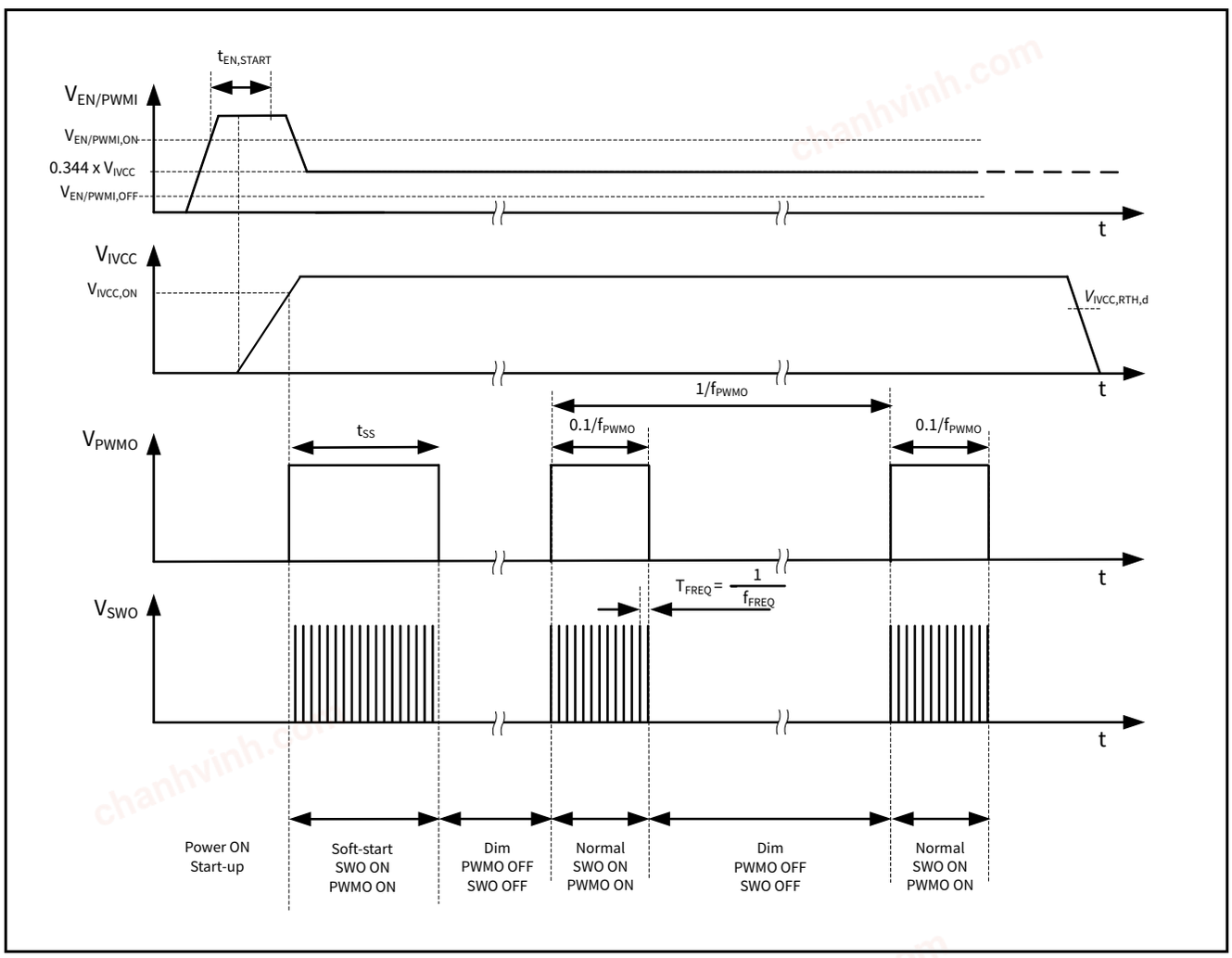


Figure 15 Timing diagram enable and LED dimming with PWM engine

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7.5 Electrical characteristics

V_{IN} = 8 V to 34 V; T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 11 Electrical characteristics: Enable and dimming

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable / PWM Input							
Enable/PWMI turn on threshold	$V_{EN/PWMI,ON}$	3	–	–	V	–	P_7.5.1
Enable/PWMI turn off threshold	$V_{EN/PWMI,OFF}$	–	–	0.8	V	–	P_7.5.2
Enable/PWMI high input current	$I_{EN/PWMI,H}$	–	–	100	µA	$V_{EN/PWMI}$ = 16.0 V	P_7.5.3
Enable/PWMI low input current	$I_{EN/PWMI,L}$	–	0.1	1	µA	$V_{EN/PWMI}$ = 0.5 V	P_7.5.4
Enable turn off delay time	$t_{EN,OFF,DEL}$	8	10	12	ms	–	P_7.5.5
PWMI min. duty time	$t_{PWMI,H}$	6	–	–	µs	–	P_7.5.6
Enable startup time	$t_{EN,START}$	100	–	–	µs	1)	P_7.5.7
PWM engine min. voltage	$V_{EN/PWM,DC_0}$	0.313 *V_{IVCC}	0.32 *V_{IVCC}	–	V	PWM engine sets DC PWMO = 0%	P_7.5.8
PWM engine max. voltage	$V_{EN/PWM,DC_100}$	–	0.56 *V_{IVCC}	0.571 *V_{IVCC}	V	PWM engine sets DC PWMO = 100%	P_7.5.9
PWM engine DC	$DC_{PWMO,DC_10\%}$	8.5	10	11.5	%	$V_{EN/PWM}$ = 0.344*V_{IVCC}	P_7.5.10
PWM frequency range	f_{PWMO}	100	–	500	Hz	1)	P_7.5.11
Enable / PWMI internal pull-down resistor	R_{EN_INT}	0.7	1.35	2	MΩ	1) $V_{EN/PWMI}$ = 1.5 V .. 3 V	P_7.5.12
FPWM charging current	I_{FPWM_CH}	-150	-200	-250	µA	1)	P_7.5.13
FPWM discharging current	I_{FPWM_DIS}	150	200	250	µA	1)	P_7.5.14
FPWM voltage rising threshold	V_{FPWM_H}	1.9	2	2.1	V	1)	P_7.5.15
FPWM voltage falling threshold	V_{FPWM_L}	0.9	1	1.1	V	1)	P_7.5.16
PWM frequency	f_{PWMO}	265	350	435	Hz	1) C_{FPWM} = 560 pF	P_7.5.17
Gate driver for dimming switch							
PWMO gate driver peak sourcing current	$I_{PWMO,SRC}$	–	230	–	mA	1) V_{PWMO} = 1 V to 4 V Current flows out of pin	P_7.5.18
PWMO gate driver peak sinking current	$I_{PWMO,SNK}$	–	370	–	mA	1) V_{PWMO} = 4 V to 1 V	P_7.5.19

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Enable and dimming function

Table 11 Electrical characteristics: Enable and dimming

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWMO gate driver output rise time	$t_{R,PWMO}$	–	50	100	ns	[1] $C_{L,PWMO}$ = 3.3 nF; V_{PWMO} = 1 V to 4 V	P_7.5.20
PWMO gate driver output fall time	$t_{F,PWMO}$	–	30	60	ns	[1] $C_{L,PWMO}$ = 3.3 nF; V_{PWMO} = 4 V to 1 V	P_7.5.21
PWMO gate driver output voltage	V_{PWMO}	4.5	–	5.5	V	[1] $C_{L,PWMO}$ = 3.3 nF	P_7.5.22
Current consumption							
Current consumption, shutdown mode	I_{Q_OFF}	–	–	15	µA	$V_{EN/PWMI}$ = 0.5 V; $T_J \leq$ 105°C; V_{IN} = 16 V	P_7.5.23
Current consumption, active mode[2]	I_{Q_ON}	–	–	7	mA	[2] $V_{EN/PWMI} \geq$ 4.75 V; R_{FREQ} = 33 kΩ I_{BO} = 0 mA; V_{SWO} = 0% duty cycle	P_7.5.24

1) Not subject to production test, specified by design
2) Dependency on switching frequency and gate charge of external switches

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8 Linear regulator

8.1 Description

The internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to $I_{LIM,min}$ (P_8.2.2). An external output capacitor with ESR lower than $R_{IVCC,ESR}$ (P_8.2.5) is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches.

Integrated undervoltage protection for the external switching MOSFET

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage (V_{IVCC}) and resets the device in case the output voltage falls below the IVCC undervoltage reset switch off threshold ($V_{IVCC,RTH,d}$). The undervoltage reset threshold for the IVCC pin helps to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level n-channel MOSFET.

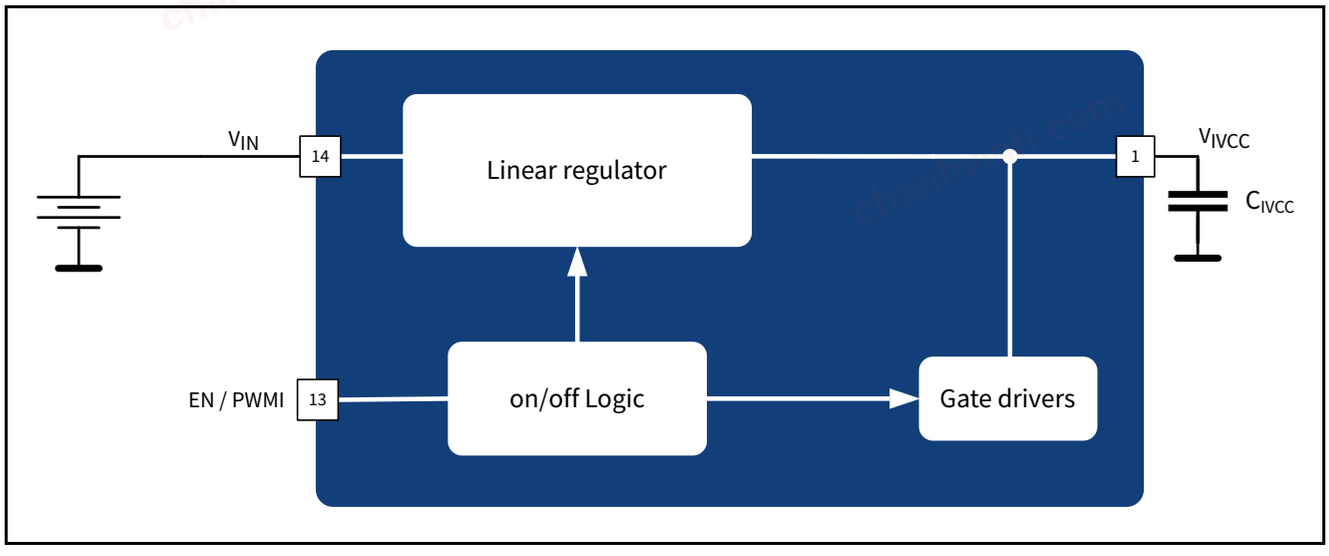


Figure 16 Voltage regulator block diagram and simplified application circuit

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8.2 Electrical characteristics

V_{IN} = 8 V to 34 V; T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 12 Electrical characteristics: Line regulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage	V_{IVCC}	4.85	5	5.15	V	6 V ≤ V_{IN} ≤ 45 V 0.1 mA ≤ I_{IVCC} ≤ 40 mA	P_8.2.1
Output current limitation	I_{LIM}	51	–	90	mA	V_{IN} = 13.5 V V_{IVCC} = 4.5 V Current flows out of pin	P_8.2.2
Drop out voltage	V_{DR}	–	–	0.5	V	V_{IN} = 4.5 V V_{IVCC} = 25 mA	P_8.2.3
IVCC buffer capacitor	C_{IVCC}	0.47	1	100	µF	1)2)3)	P_8.2.4
IVCC buffer capacitor ESR	$R_{IVCC, ESR}$	–	–	0.5	Ω	1)2)	P_8.2.5
Undervoltage reset headroom	$V_{IVCC,HDRM}$	100	–	–	mV	V_{IVCC} decreasing V_{IVCC} - $V_{IVCC,RTH,d}$	P_8.2.6
IVCC undervoltage reset switch-off threshold	$V_{IVCC,RTH,d}$	3.6	–	4.0	V	4)V_{IVCC} decreasing	P_8.2.7
IVCC undervoltage reset switch-on threshold	$V_{IVCC,RTH,i}$	–	–	4.5	V	V_{IVCC} increasing	P_8.2.8

1) Not subject to production test, specified by design
2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum
3) If embedded PWM engine is used, a 4.7 µF value has to be chosen as a minimum
4) Selection of external switching MOSFET is crucial and the $V_{IVCC,RTH,d\,min}$. as worst case the threshold voltage of MOSFET must be considered

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9 Protection and diagnostic functions

9.1 Description

The TLD5099EP has integrated circuits to diagnose and protect against output overvoltage, open load, open feedback and overtemperature faults. Additionally the FBH and FBL potential is monitored and in case the LED load is shorted to GND (see description **Figure 22**) the regulator stops the operation and protects the system. In case any of the six fault conditions occur the PWMO and SWO signal will change to an active logic “low” signal to communicate that a fault has occurred, while IVCC shutdown occurs only in case of overtemperature or input undervoltage (detailed overview in **Figure 17** and **Table 13** below). **Figure 18** illustrates the various open load and open feedback conditions. In case of an overtemperature condition the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator. The typical junction shutdown temperature is 175°C ($T_{J,SD}$ P_9.2.2). After cooling down the IC will automatically restart. Thermal shutdown is an integrated protection function designed to prevent IC destruction and is not intended for continuous use in normal operation (**Figure 20**). To calculate the proper overvoltage protection resistor values an example is given in **Figure 21**.

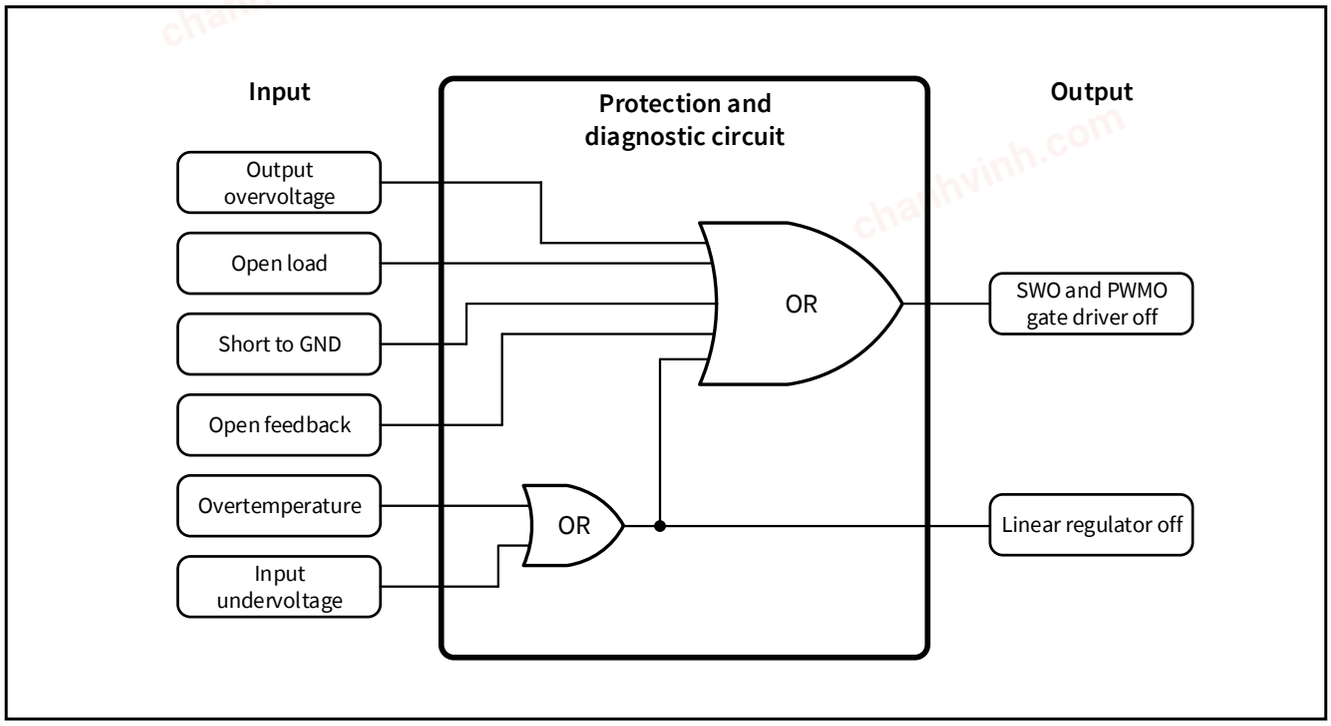


Figure 17 Protection and diagnostic function block diagram

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Table 13 Diagnosis truth table[1)]

Input		Output		
Condition	**Level**	**SWO**	**PWMO**	**IVCC**
Overvoltage at output	False	Sw	High or Sw	Active
	True	Low	Low	Active
Open load	False	Sw	High or Sw	Active
	True	Low	Low	Active
Short to GND at LED chain	False	Sw	High or Sw	Active
	True	Low	Low	Active
Open feedback	False	Sw	High or Sw	Active
	True	Low	Low	Active
Overtemperature	False	Sw	High or Sw	Active
	True	Low	Low	Shutdown
Undervoltage at input	False	Sw	High or Sw	Active
	True	Low	Low	Shutdown

1) Sw = Switching; False = Condition does NOT exist; True = Condition does exist

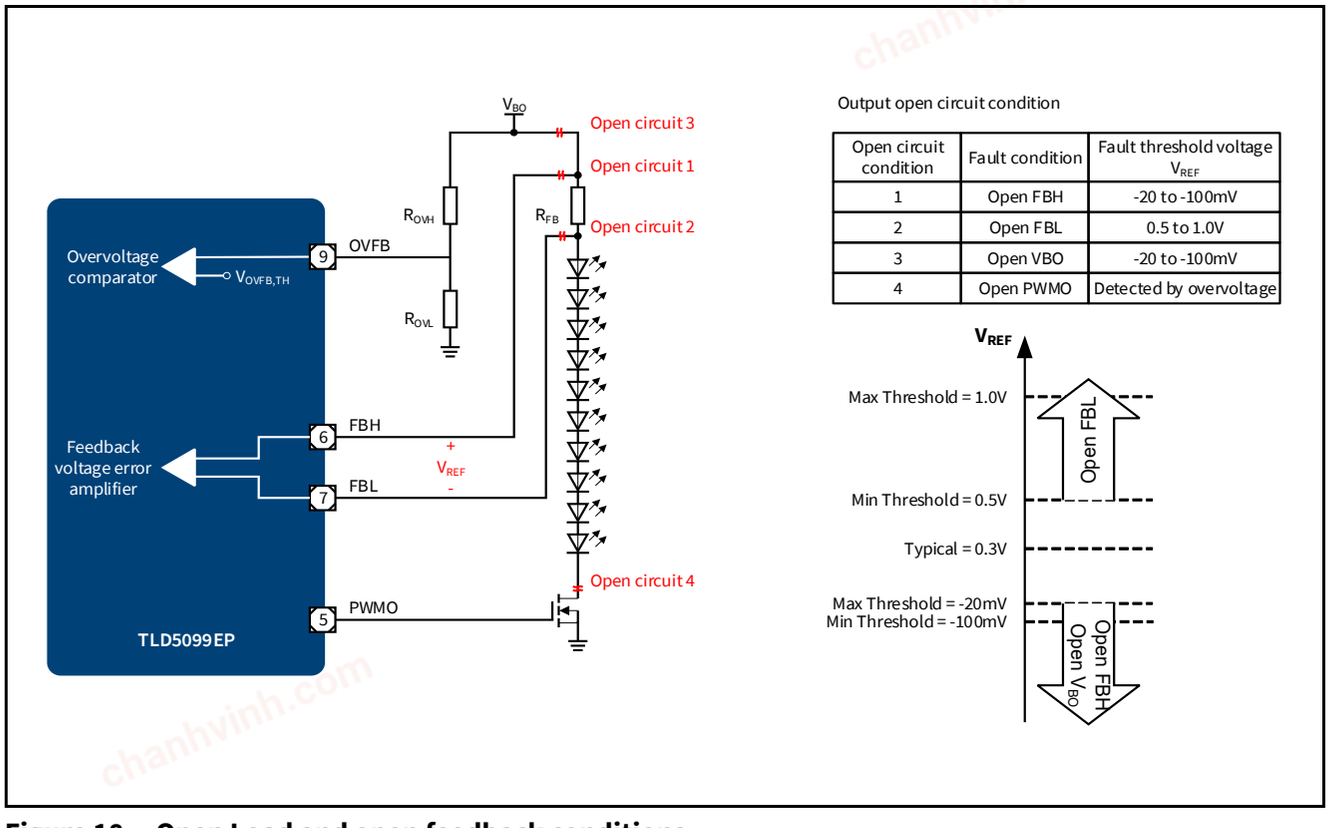


Figure 18 Open Load and open feedback conditions

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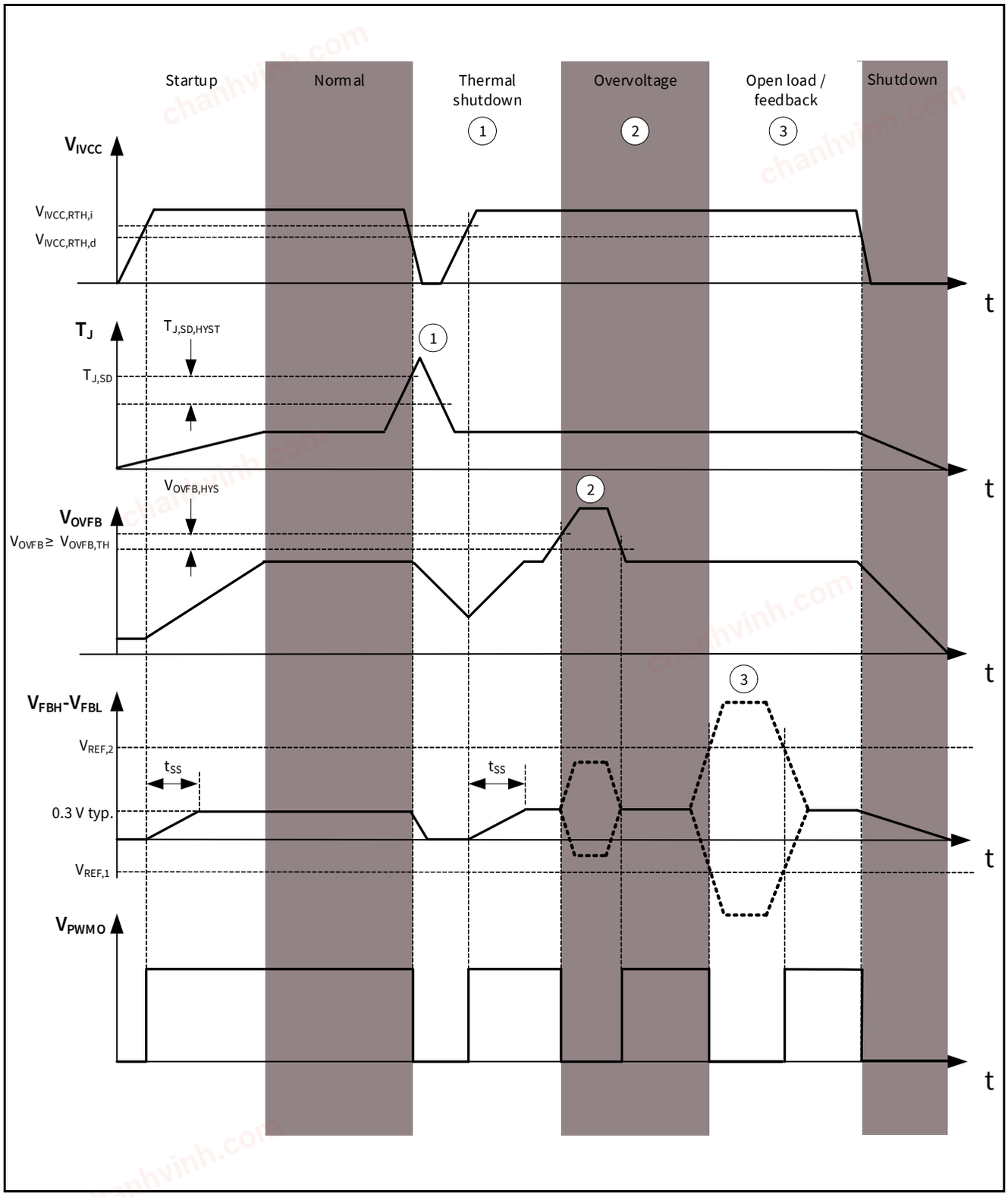


Figure 19 Open load, overvoltage and overtemperature timing diagram

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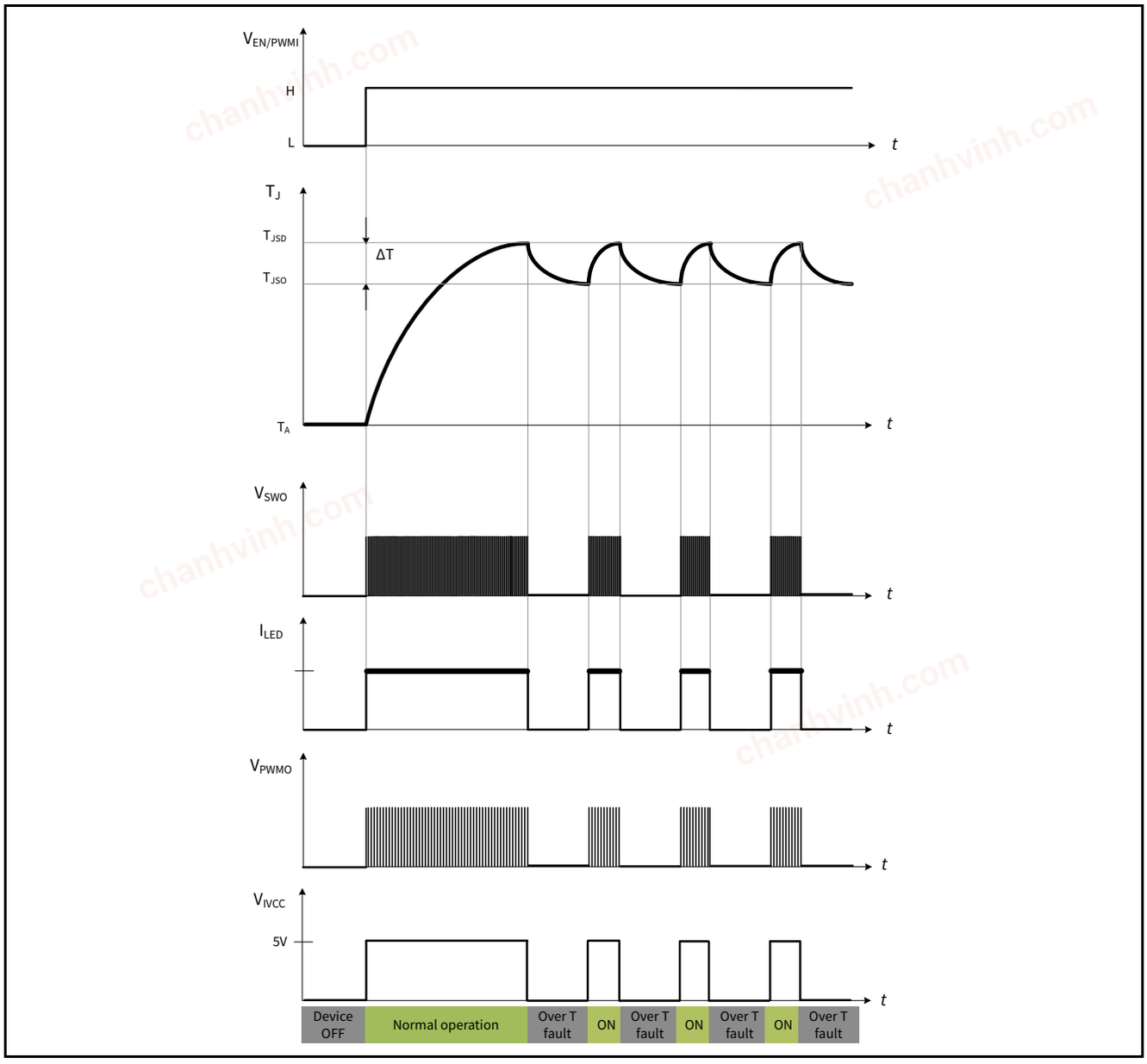


Figure 20 Device overtemperature protection behavior

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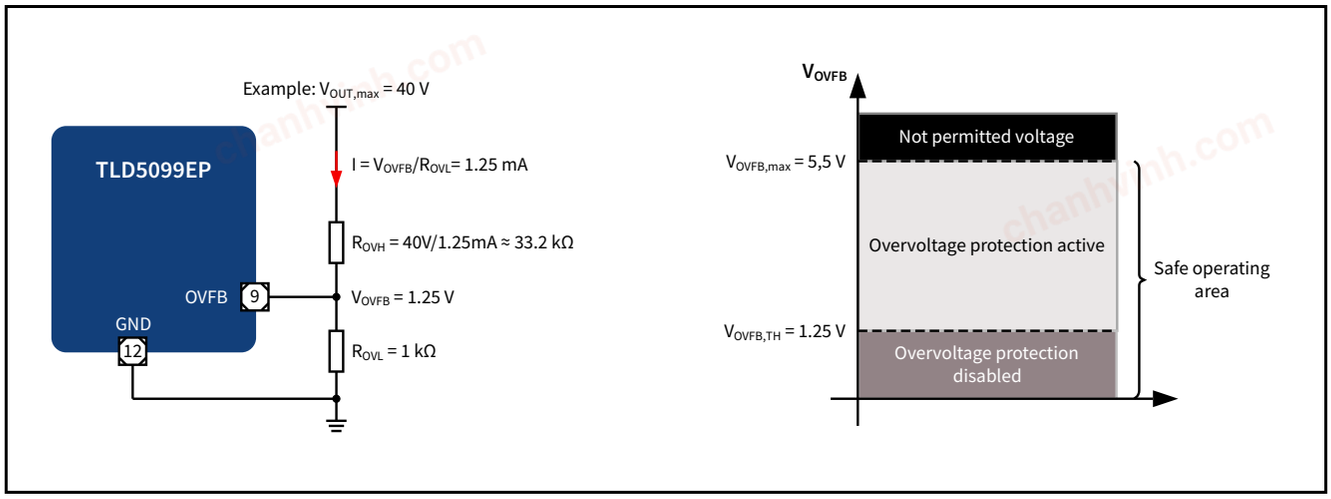


Figure 21 Overvoltage protection description

Short to GND protection for high-side return applications (B2B) from Figure 32 and Figure 33

The FBH and FBL pins features a short to GND detection threshold (V_{FBL,FBH_S2G}). If the potential on these pins is below this threshold the device stops its operation. This means that the PWMO signal changes to inactive state (“low” potential) and the corresponding p-channel (T_{DIM2}) is switched off accordingly and protects the LED chain. For the B2B application some external components are needed to ensure a “low” potential during a short circuit event. D_1 and D_2 are low power diodes (BAS70) and the resistor R_{PROT} (10 kΩ) is needed to limit the current through this path. The diode D_3 should be a high power diode and is needed to protect the R_{FB} and the FBH and FBL pins in case of an short circuit to GND event. This short circuit detection and protection concept considers potential faults for LED chains (LED modules) which are separated from the ECU via two wires (at the beginning and at the end of the LED chain). If the short circuit condition disappears, the device will re-start with a soft start.

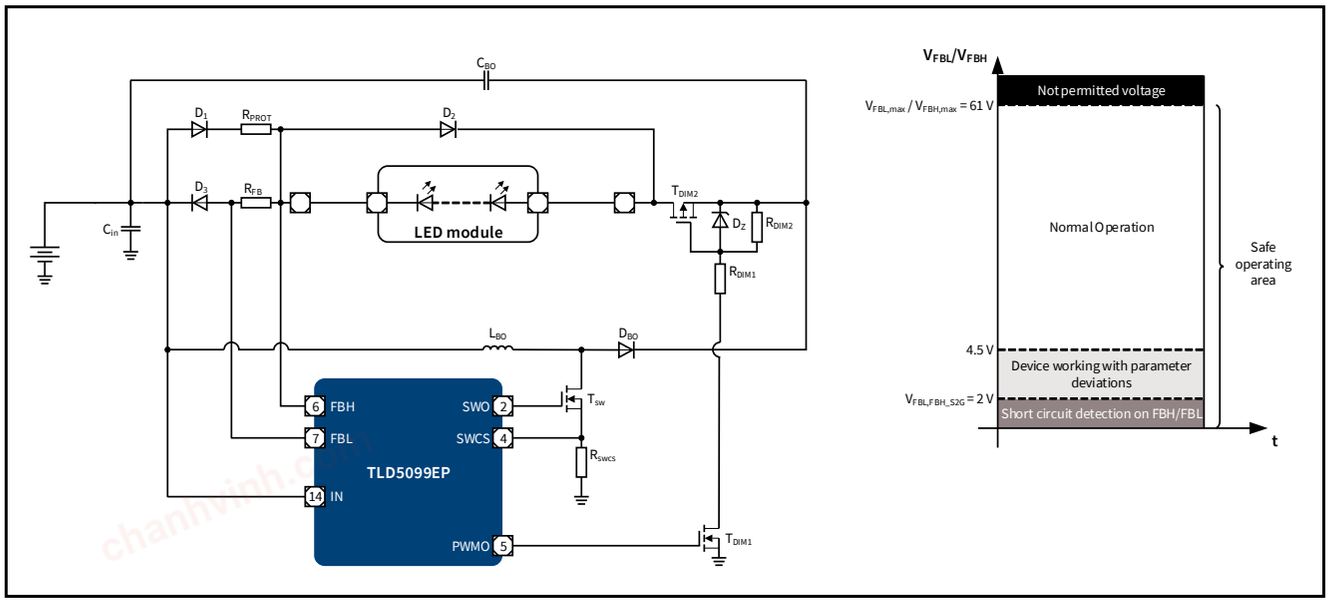


Figure 22 Short circuit to GND protection

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9.2 Electrical characteristics

V_{IN} = 8 V to 34 V; T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 14 Electrical characteristics: Protection and diagnosis

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Short circuit protection							
FBH and FBL short-circuit fault sensing common mode range	V_{FBL,FBH_S2G}	1.5	–	2	V	refer to **Figure 22** $V_{FBH} = V_{FBL}$ decreasing	P_9.2.1
Temperature protection							
Overtemperature shutdown	$T_{J,SD}$	160	175	190	°C	1) refer to **Figure 20**	P_9.2.2
Overtemperature shutdown hystereses	$T_{J,SD,HYST}$	–	15	–	°C	1)	P_9.2.3
Overvoltage protection							
Output overvoltage feedback threshold increasing	$V_{OVFB,TH}$	1.21	1.25	1.29	V	refer to **Figure 21**	P_9.2.4
Output overvoltage feedback hysteresis	$V_{OVFB,HYS}$	50	–	150	mV	1) Output voltage decreasing	P_9.2.5
Overvoltage reaction time	t_{OVPRR}	2	–	10	µs	Output voltage decreasing	P_9.2.6
Overvoltage feedback input current	I_{OVFB}	-1	0.1	1	µA	V_{OVFB} = 1.25 V	P_9.2.7
Open load and open feedback diagnostics							
Open load/feedback threshold	$V_{REF,1,3}$	-100	–	-20	mV	refer to **Figure 18** $V_{REF} = V_{FBH} - V_{FBL}$ Open circuit 1 or 3	P_9.2.8
Open feedback threshold	$V_{REF,2}$	0.5	–	1	V	$V_{REF} = V_{FBH} - V_{FBL}$ Open circuit 2	P_9.2.9

1) Specified by design; not subject to production test

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

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10 Analog Dimming

The SET pin influences the feedback voltage error amplifier by generating an internal current accordingly to its voltage (V_{SET}). If the analog dimming feature is not needed, this pin must be connected to IVCC or external voltage supply higher than 1.6 V. Different application scenarios are described in **Figure 25**. This pin can also go outside of the ECU for instance if a thermistor is connected on a separated LED module and the analog dimming input is used to thermally protect the LEDs. For reverse battery protection of this pin an external series resistor should be placed to limit the current.

10.1 Purpose of Analog Dimming

1. It is difficult for LED manufacturers to deliver LEDs which have the same brightness, colorpoint and forward voltage class. Due to this relatively wide spread of the crucial LED parameters automotive customers order LEDs from one or maximum two different colorpoint classes. The LED manufacturer must preselect the LEDs to deliver the requested colorpoint class. These preselected LEDs are matched in terms of the colorpoint but a variation of the brightness remains. To correct the brightness deviation an analog dimming feature is needed. The mean LED current can be adjusted by applying an external voltage V_{SET} at the SET pin.
2. If the DC/DC application is separated from the LED loads the ECU manufacturers aim is to develop one hardware which should be able to handle different load current conditions (e.g. 80 mA to 400 mA) to cover different applications. To achieve this average LED current adjustment the analog dimming is a crucial feature.

10.2 Description

Application Example

Desired LED current = 400 mA. For the calculation of the correct feedback resistor R_{FB} the following equation can be used: This formula is valid if the analog dimming feature is disabled and V_{SET} > 1.6 V.

(10.1)

$$I_{LED} = \frac{V_{REF}}{R_{FB}} \rightarrow R_{FB} = \frac{V_{REF}}{I_{LED}} \rightarrow R_{FB} = \frac{0.3V}{400mA} = 750m\Omega$$

Related electrical parameter is guaranteed with V_{SET} = 5 V (P_5.2.1) A decrease of the average LED current can be achieved by controlling the voltage at the SET pin (V_{SET}) between 0.1 V and 1.6 V. The mathematical relation is given in the formula below:

(10.2)

$$I_{LED} = \frac{V_{SET} - 0.1V}{5 \cdot R_{FB}}$$

Refer to the concept drawing in **Figure 24**.

If V_{SET} is equal to or smaller than 50 mV, the switching activity is stopped and I_{LED} = 0 A

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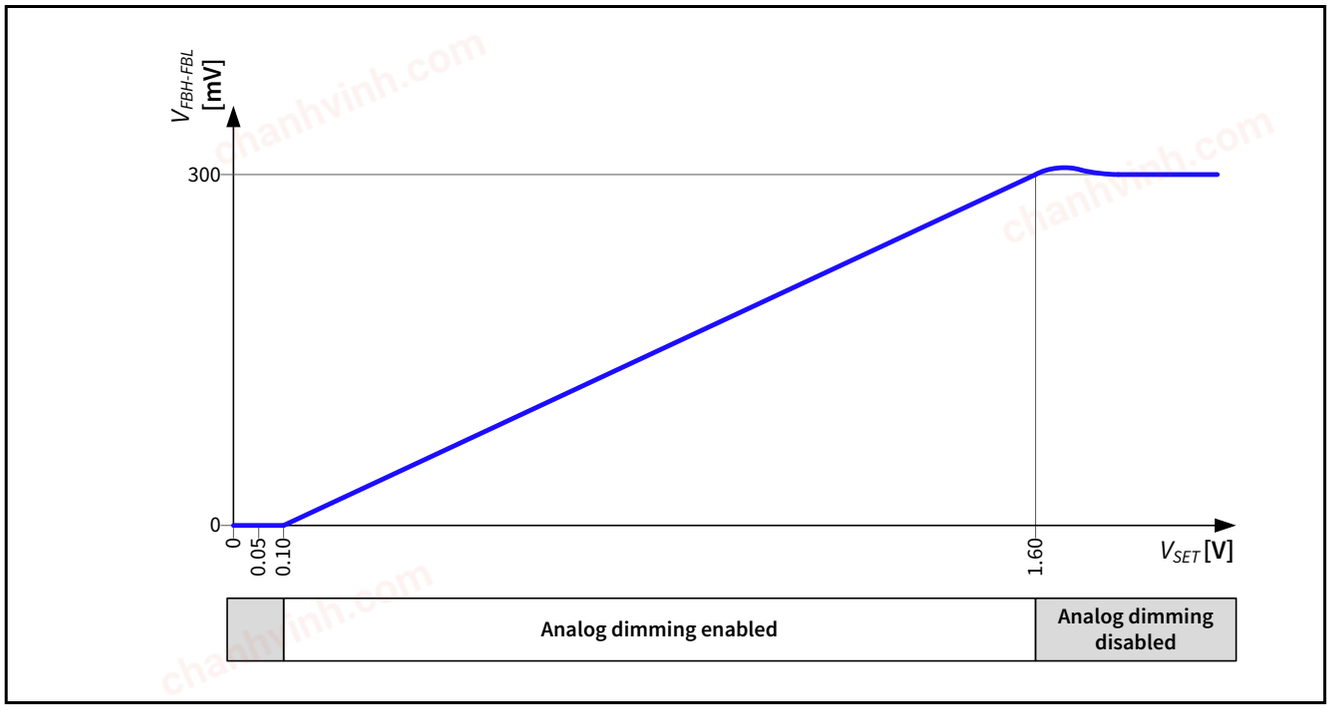


Figure 23 Basic relationship between V_{REF} and V_{SET} voltage

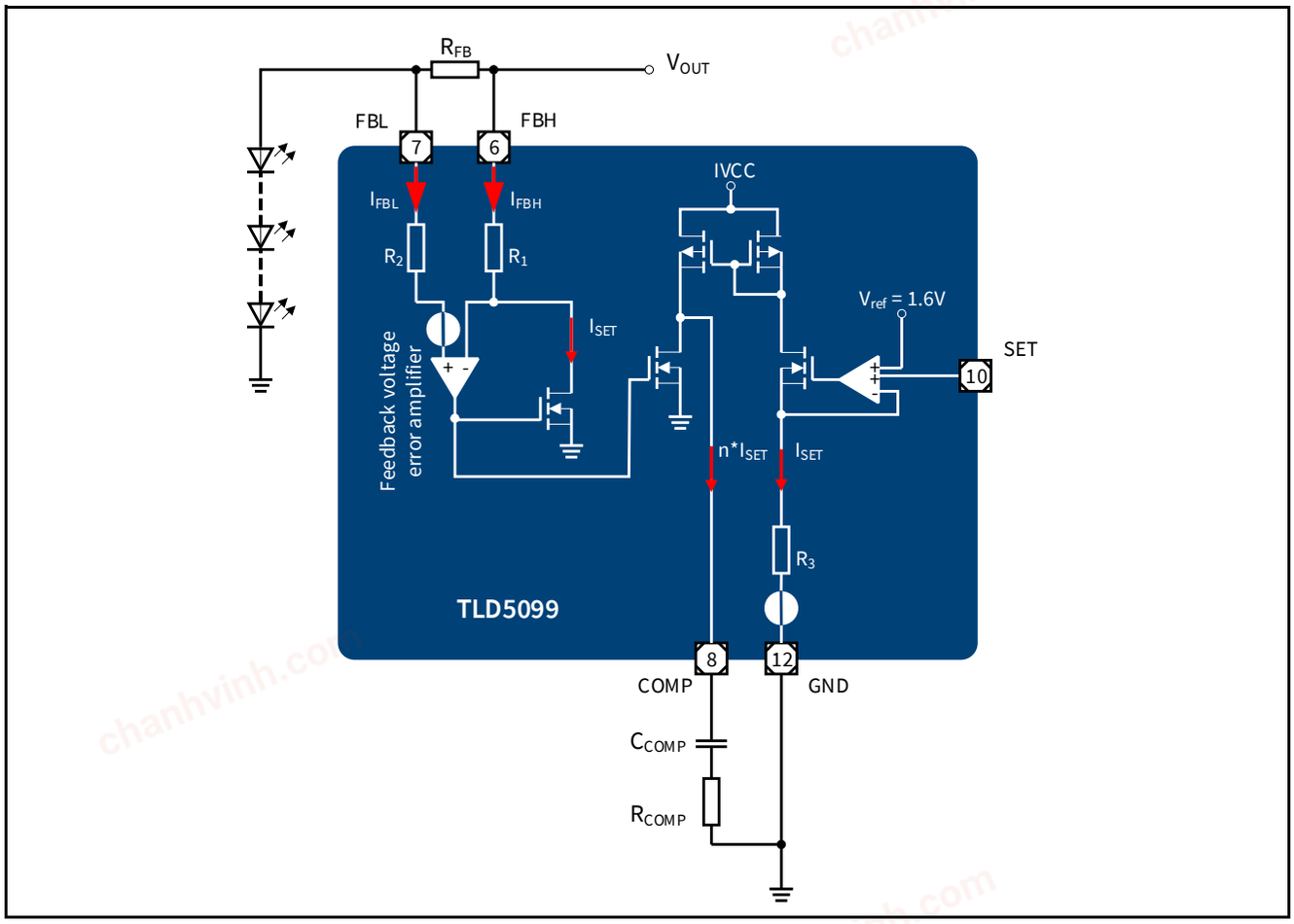


Figure 24 Concept drawing analog dimming

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Analog Dimming

Multi-purpose usage of the analog dimming feature

1. A µC integrated digital analog converter (DAC) output or a stand alone DAC can be used to supply the SET pin of the TLD5099EP. The integrated voltage regulator (V_{IVCC}) can be used to supply the µC or external components if the current consumption does not exceed 20 mA.
2. The analog dimming feature is directly connected to the input voltage of the system. In this configuration the LED current is reduced if the input voltage V_{IN} is decreased. The DC/DC boost converter increases the duty cycle of SWO if V_{IN} drops to a lower potential. This causes an increase of the input current consumption. If applications require a decrease of the LED current in respect to V_{IN} variations, this setup can be chosen.
3. The usage of an external resistor divider connected between IVCC (integrated 5 V regulator output and gate buffer pin) SET and GND can be chosen for systems without µC on board. The concept allows to control the LED current via placing cheap low power resistors. Furthermore a temperature sensitive resistor (thermistor) to protect the LED loads from thermal destruction can be connected additionally.
4. If the analog dimming feature is not needed the SET pin must be connected directly to higher than 1.6 V potential (e.g. IVCC potential)
5. Instead of an DAC the µC can provide a PWM signal and an external R-C filter produces a constant voltage for the analog dimming. The voltage level depends on the PWM frequency (f_{PWM}) and duty cycle (DC) which can be controlled by the µC software after reading the coding resistor placed at the LED module.

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Analog Dimming

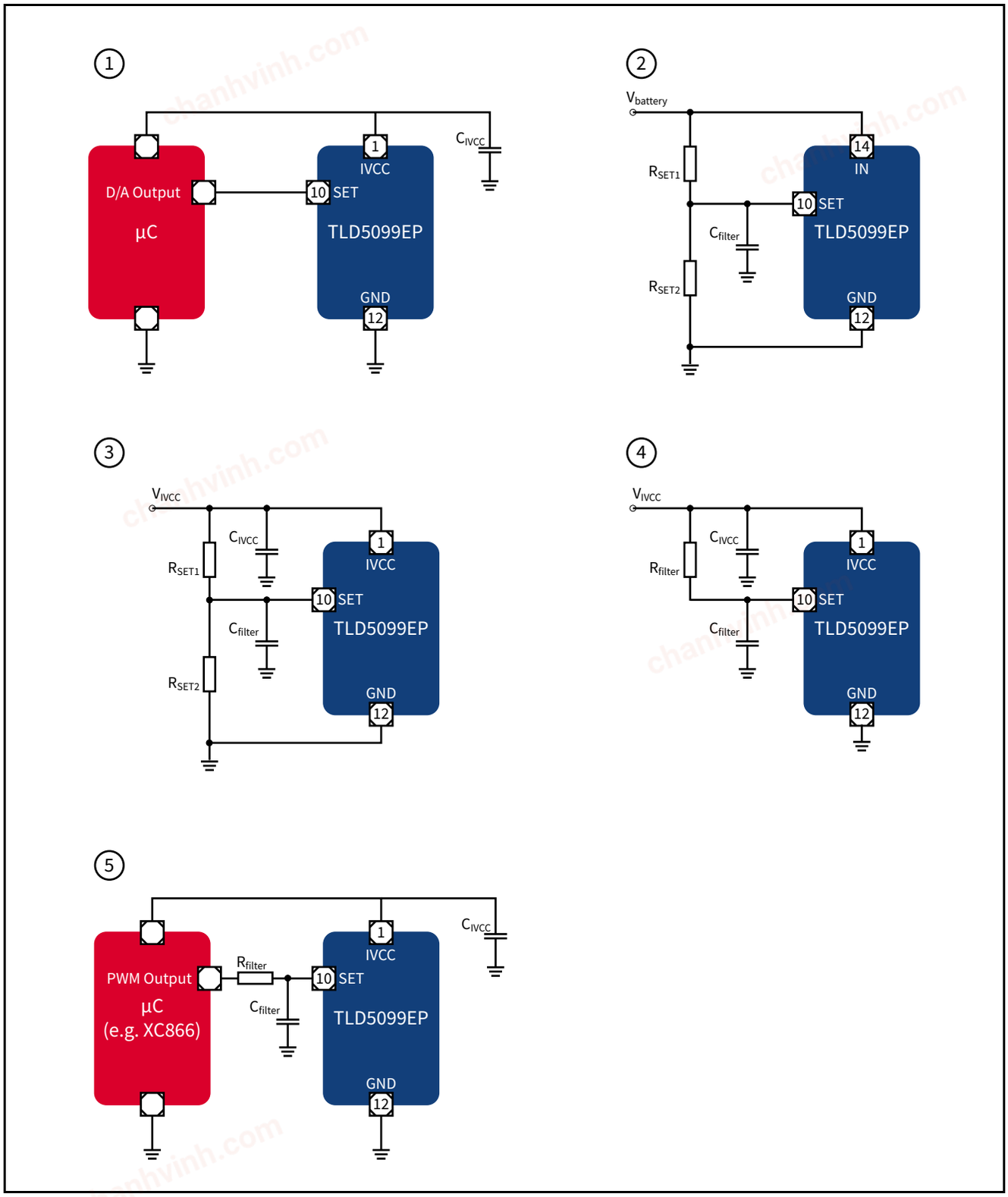


Figure 25 Analog dimming in various applications

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10.3 Electrical characteristics

V_{IN} = 8 V to 34 V; T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 15 Electrical characteristics: Protection and diagnosis

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SET programming range	V_{SET}	0	–	1.6	V	1) refer to **Figure 23**	P_10.3.1

1) Specified by design; not subject to production test.

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11 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

POS/nDRL is the signal that indicates which function is activated (position light or daytime running light).

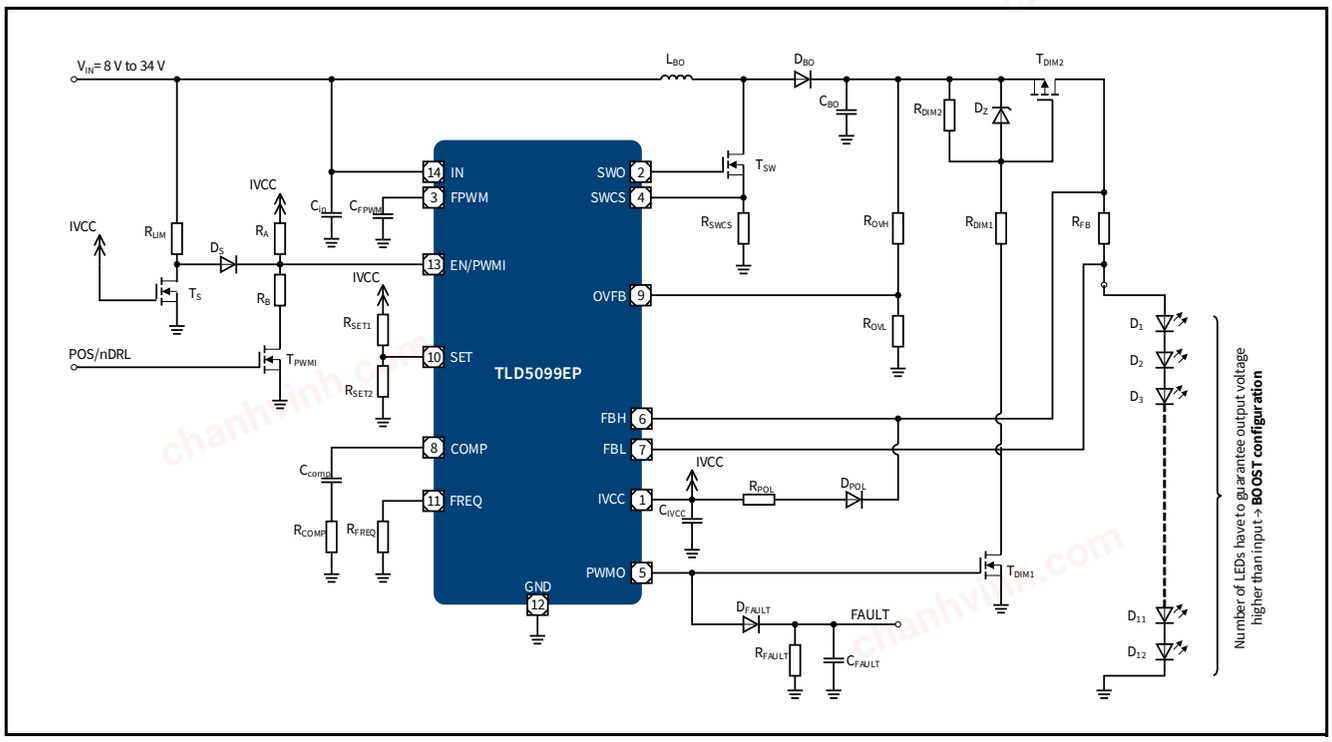


Figure 26 Boost to ground using embedded PWM engine application circuit - B2G (Boost configuration)

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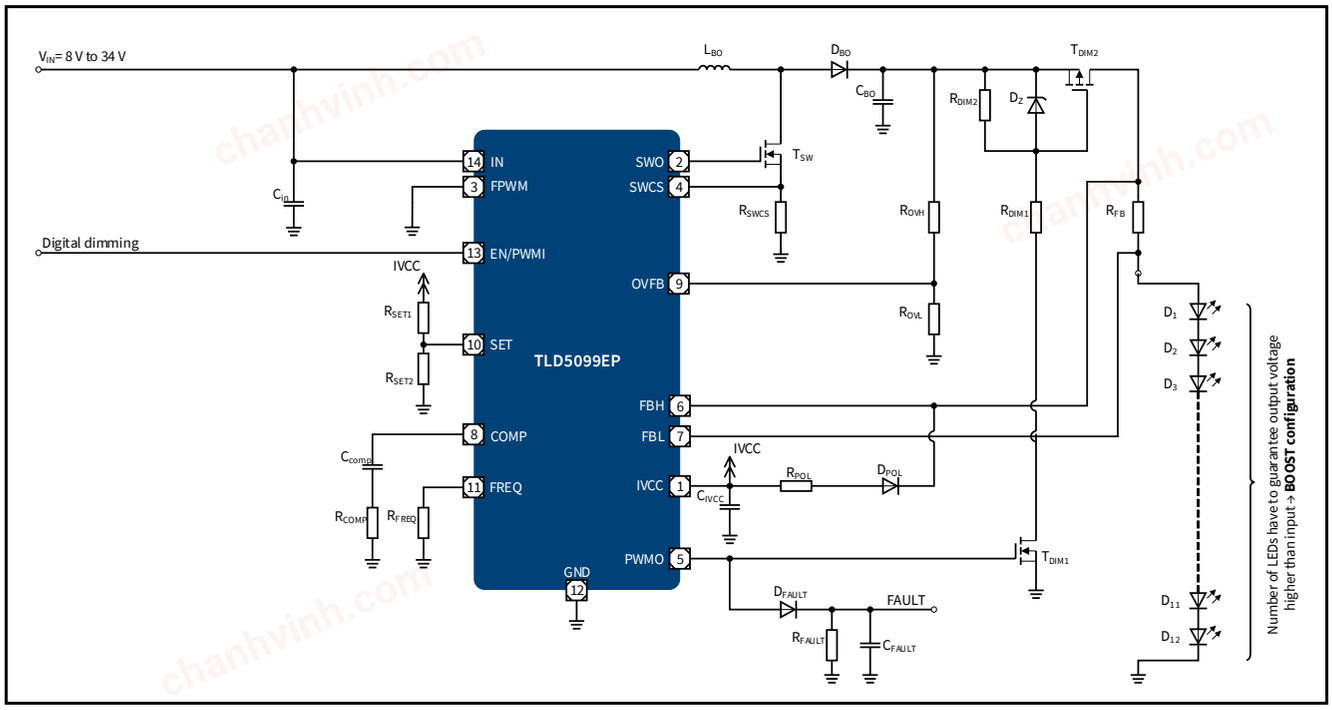


Figure 27 Boost to ground using digital dimming application circuit - B2G (Boost configuration)

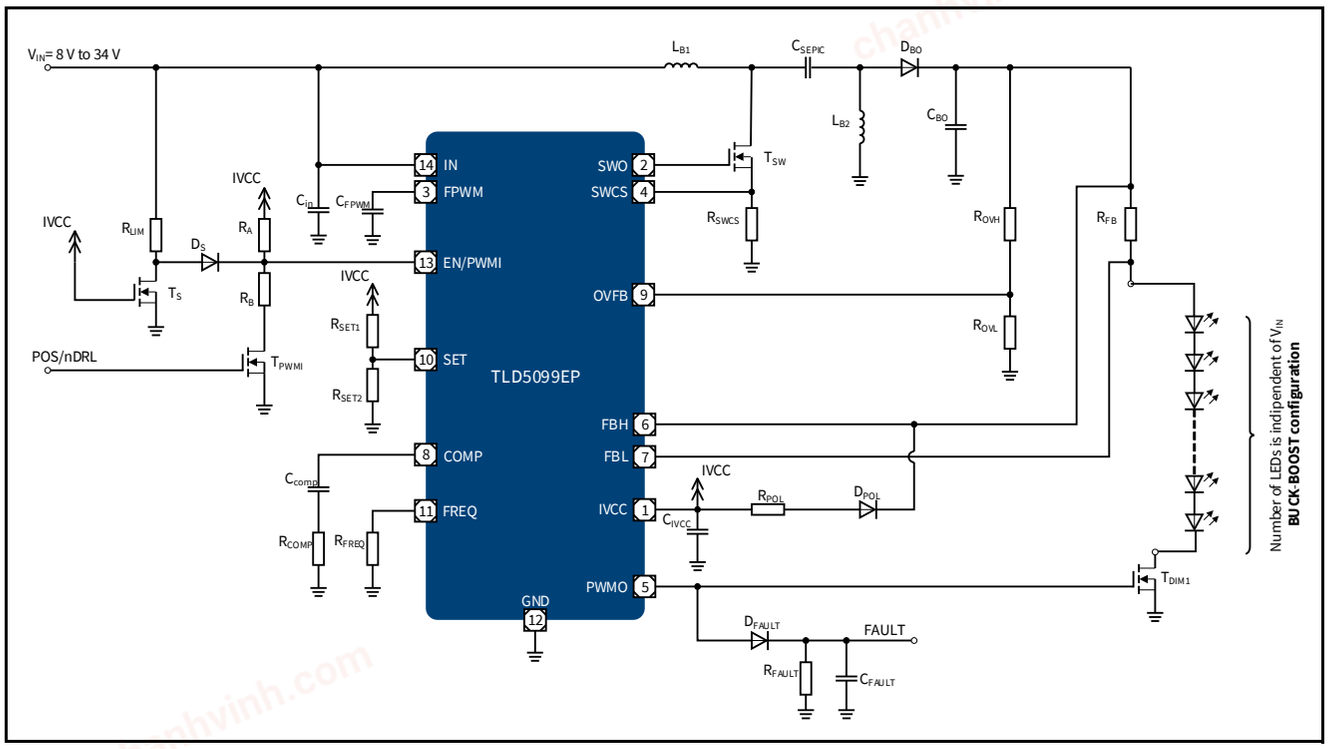


Figure 28 SEPIC using embedded PWM engine application circuit (Buck - Boost configuration)

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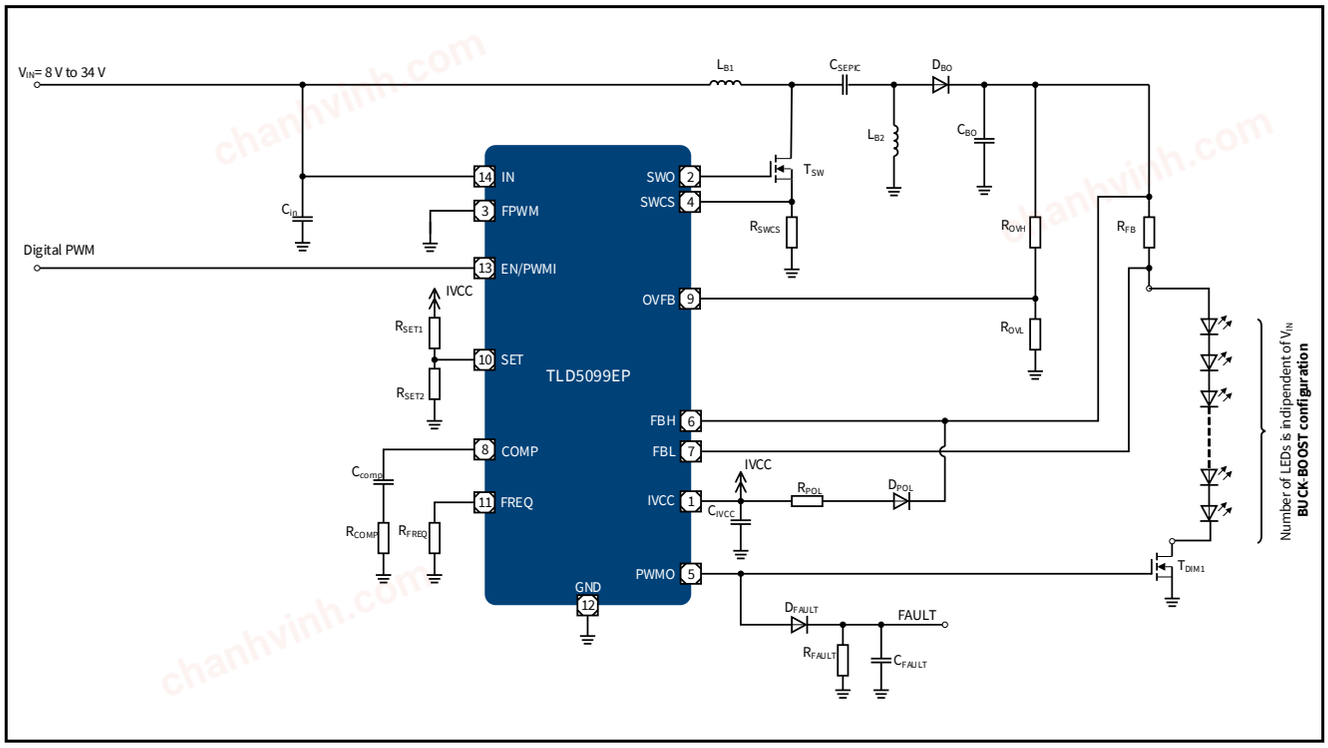


Figure 29 SEPIC using digital dimming application circuit (Buck - Boost configuration)

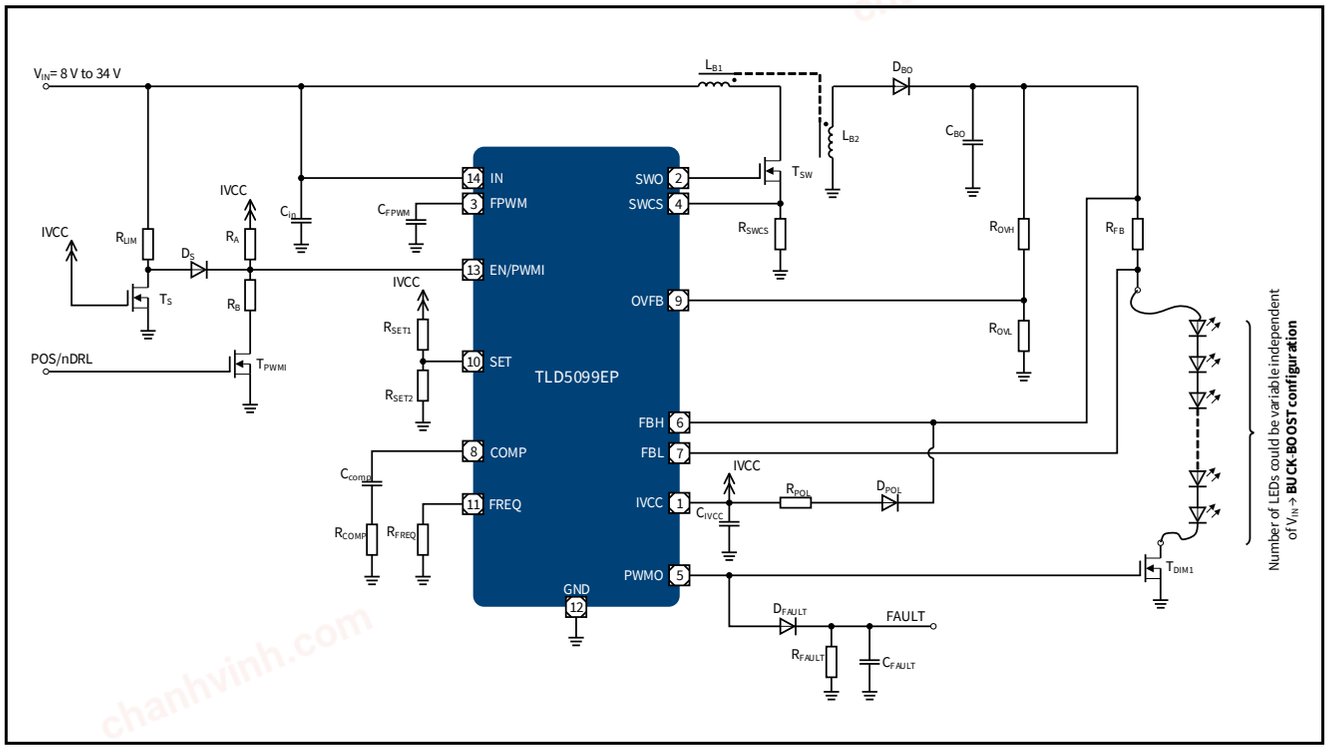


Figure 30 Flyback using embedded PWM engine application circuit (Buck - Boost configuration)

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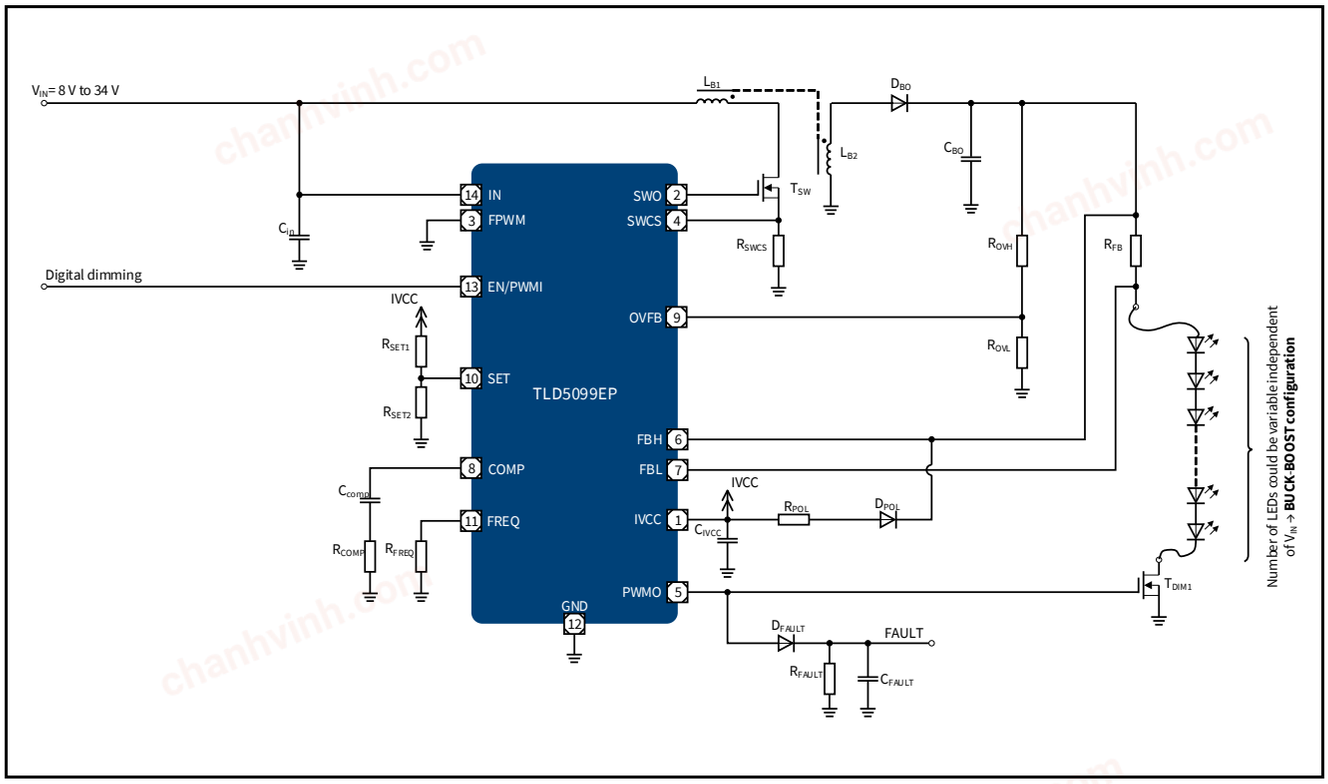


Figure 31 Flyback using digital dimming application circuit (Buck - Boost configuration)

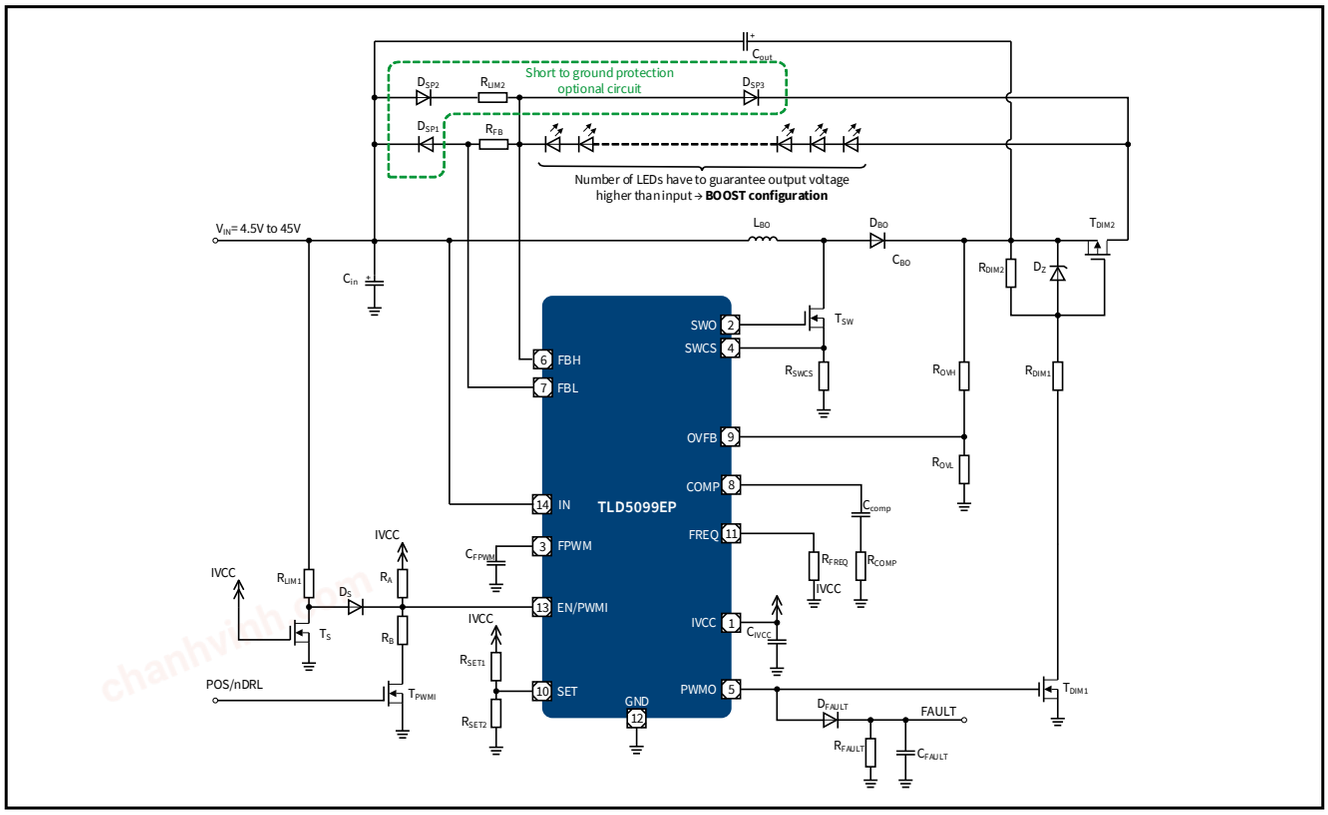


Figure 32 Boost to battery using embedded PWM engine application circuit - B2B (Buck - Boost configuration)

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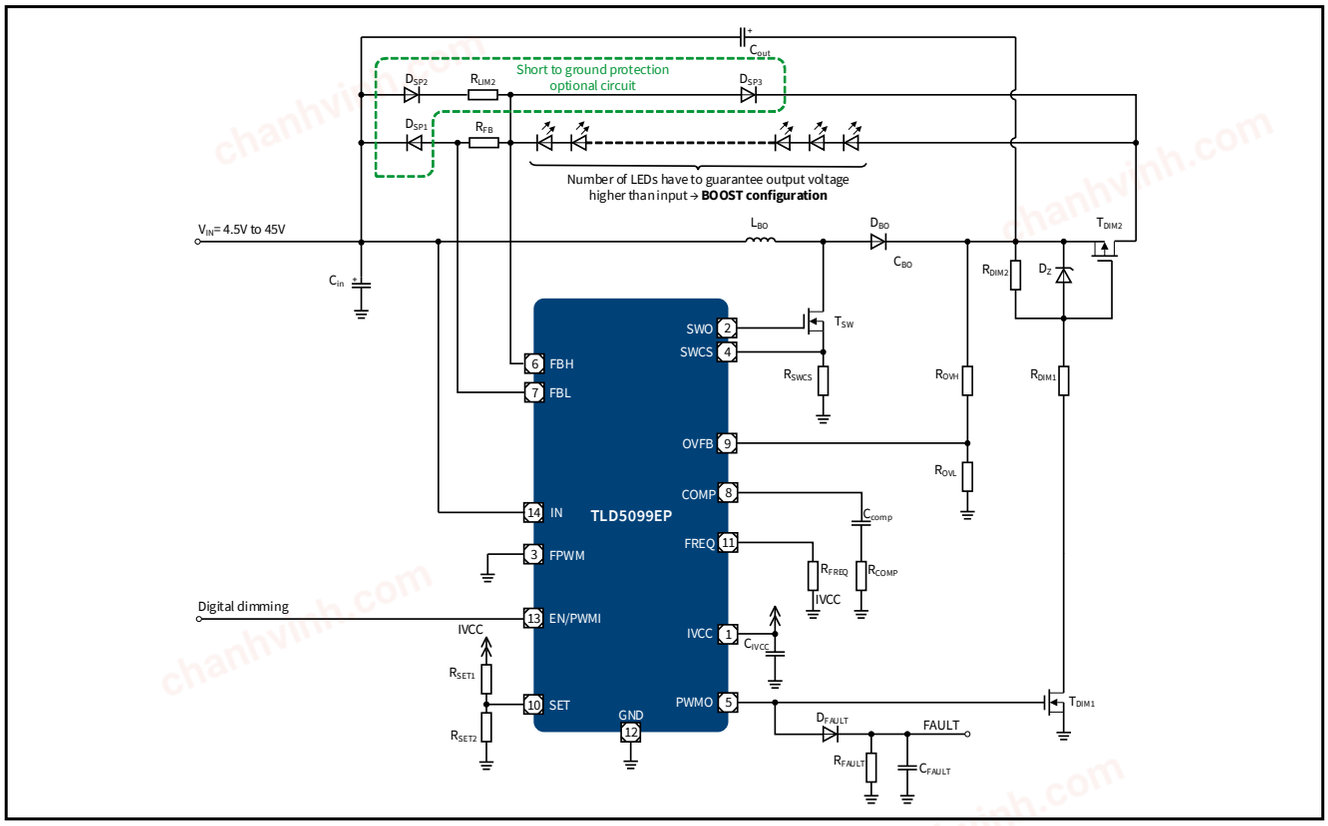


Figure 33 Boost to battery using digital dimming application circuit - B2B (Buck - Boost configuration)

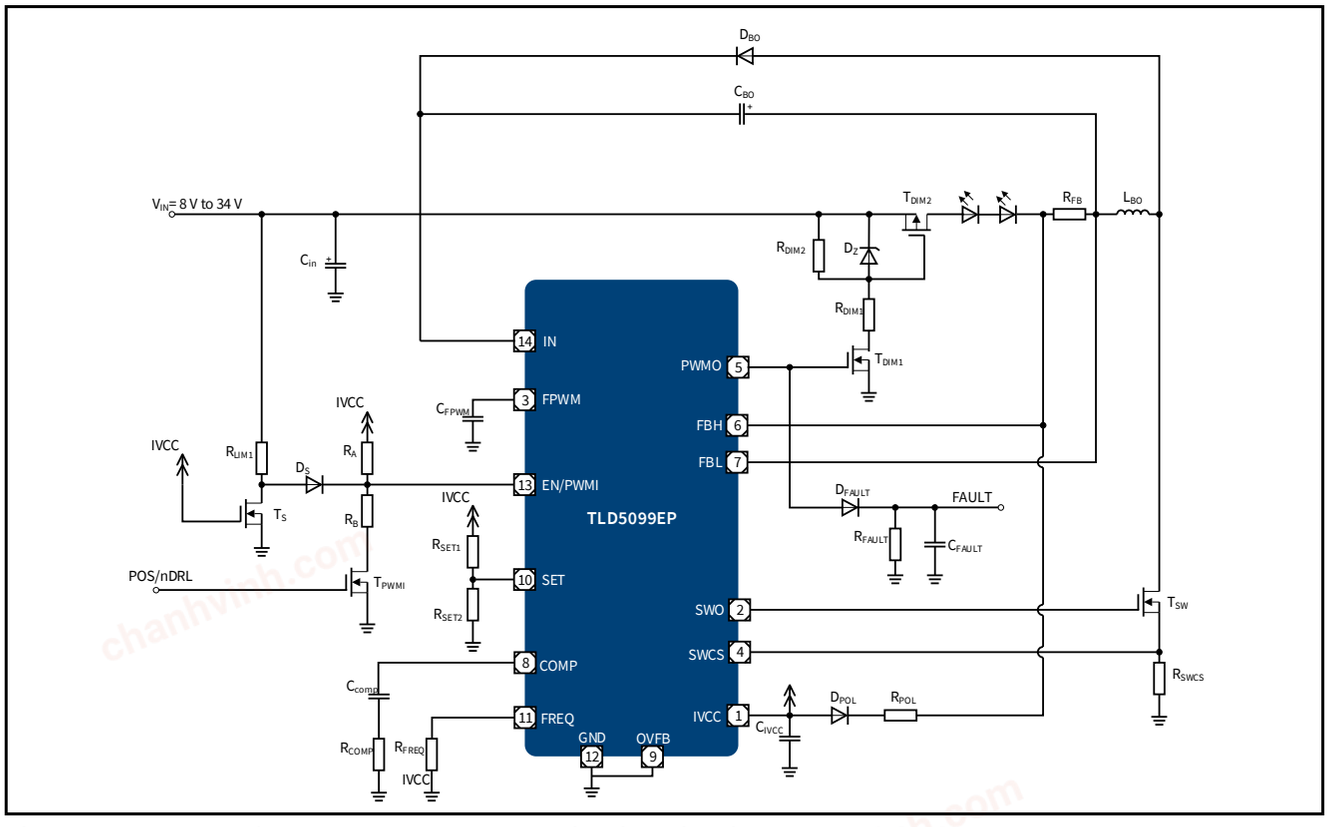


Figure 34 Buck using embedded PWM application circuit

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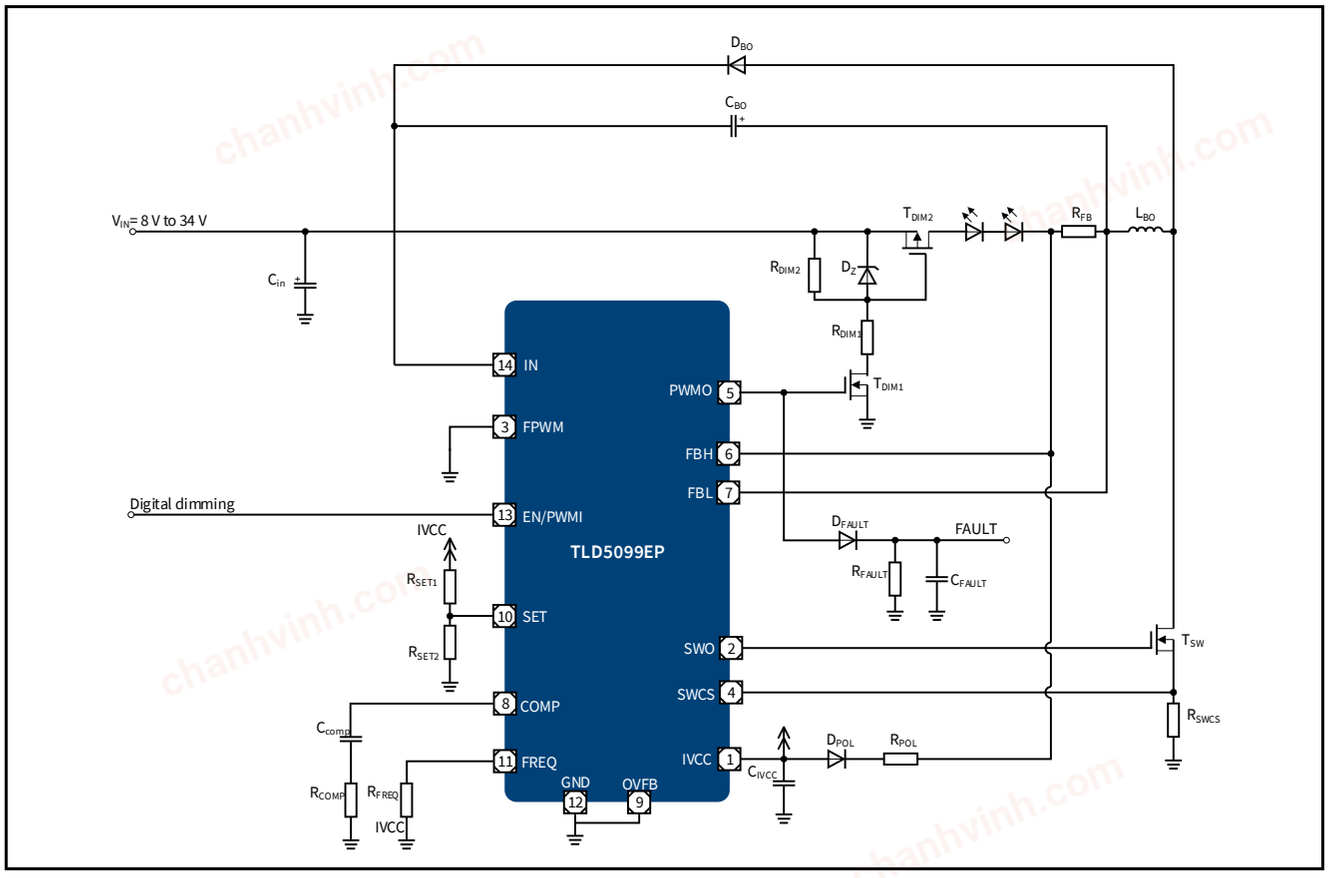


Figure 35 Buck using digital dimming application circuit

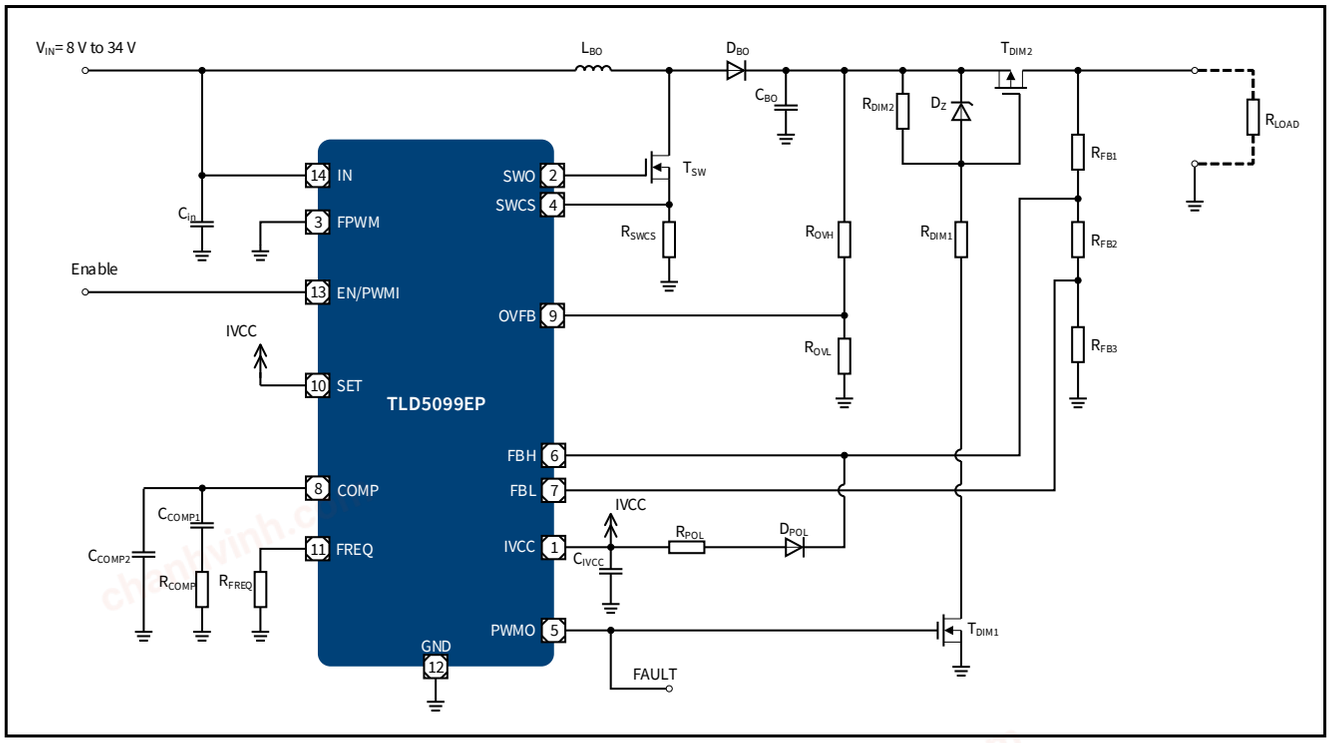


Figure 36 Boost voltage application circuit

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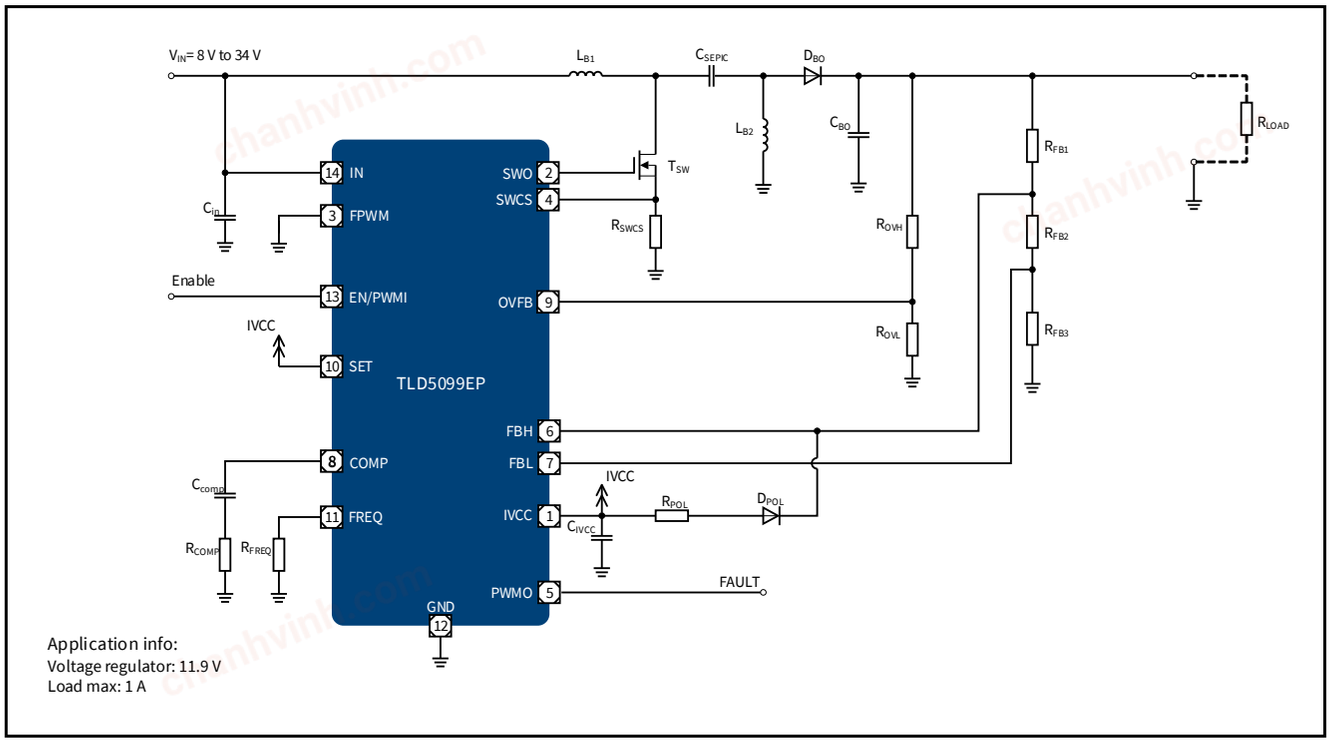


Figure 37 SEPIC voltage application circuit

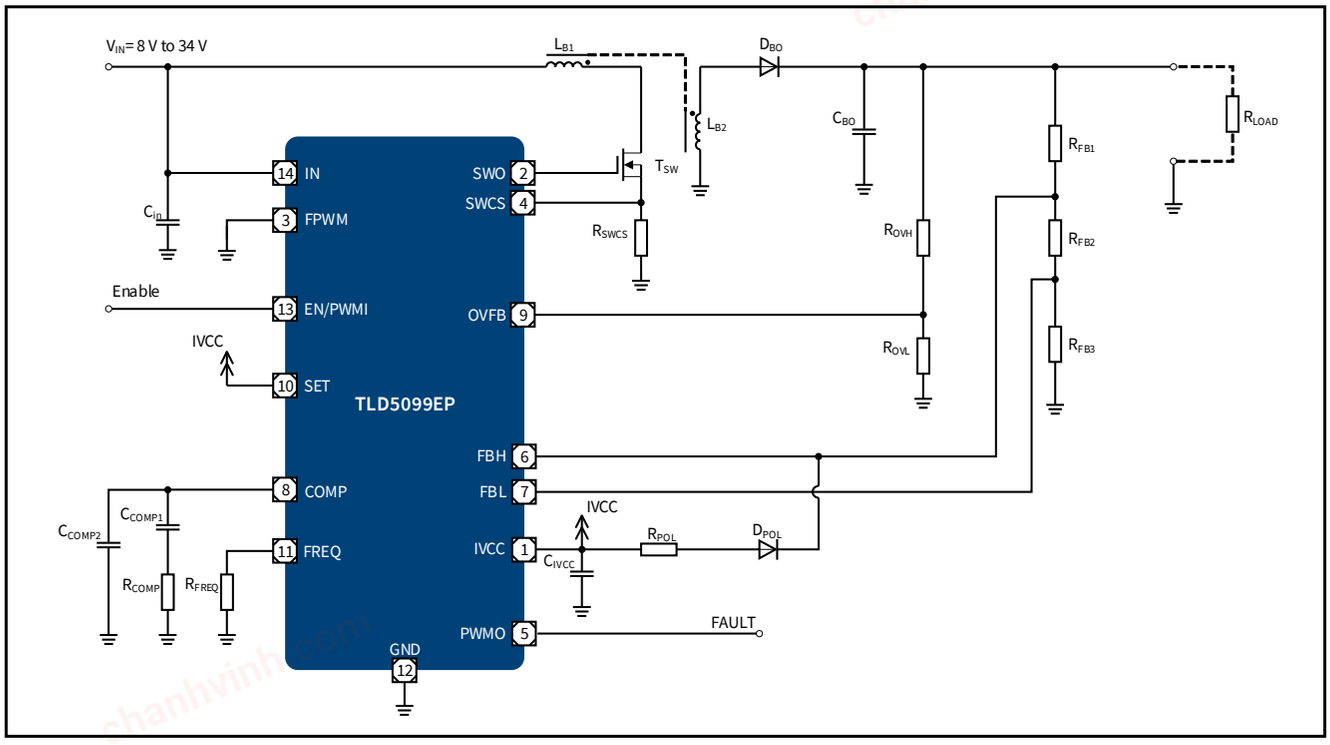


Figure 38 Flyback voltage application circuit

Note: The application drawings and corresponding bill of materials are simplified examples. Optimization of the external components must be done according to specific application requirements.

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11.1 Further application information

- For further information you may contact **http://www.infineon.com/**
- Application Note: TLD509x DC-DC Multitopology Controller IC “Dimensioning and Stability Guideline - Theory and Practice”

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12 Package outlines

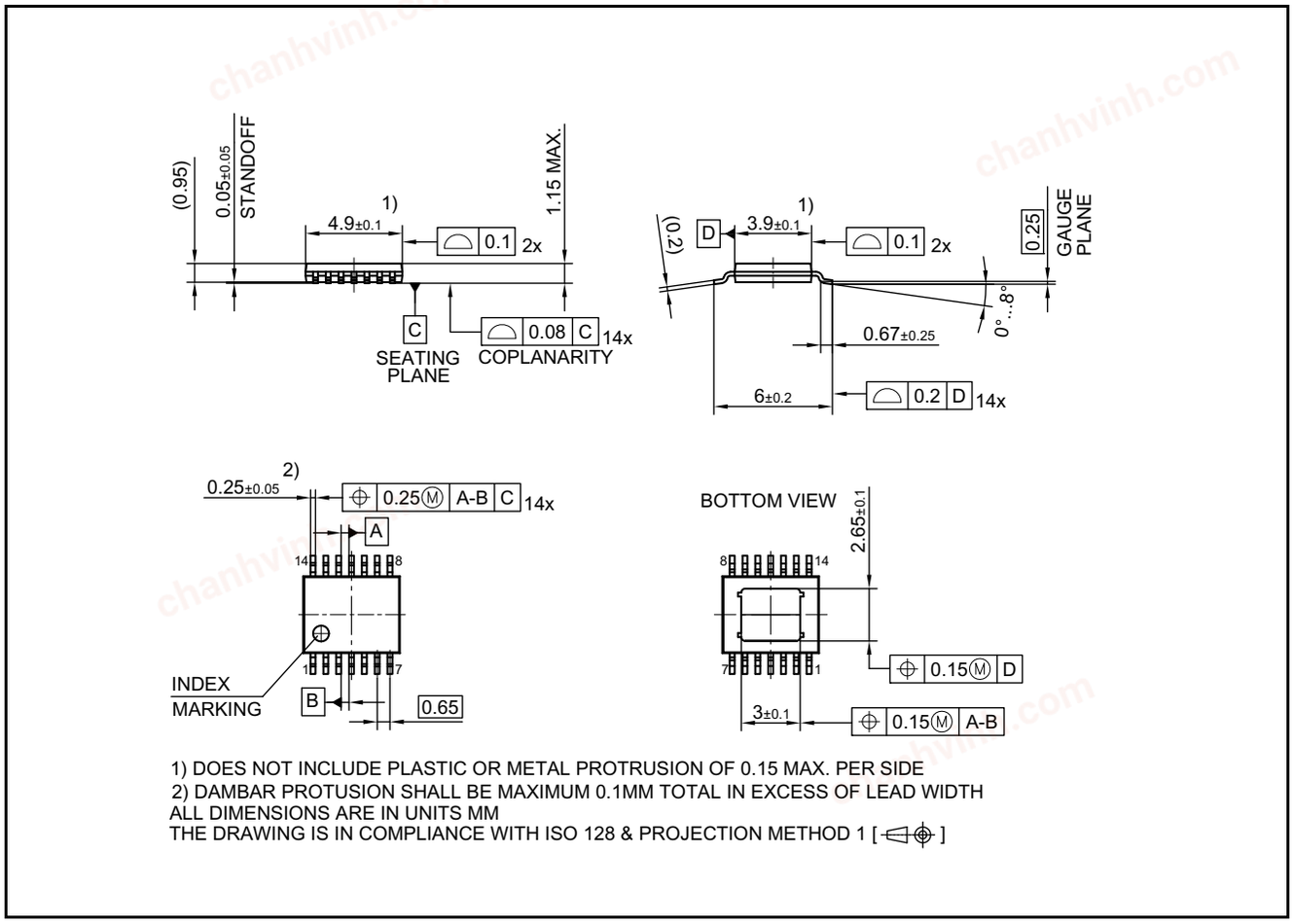


Figure 39 Outline PG-TSDSO-14

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

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13 Revision history

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Rev.1.00; 2019-12-16	
Datasheet	Intial release

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