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LITIX™ Power

TLD5045EJ - 700 mA High integration - DC/DC step-down converter

AEC Qualified RoHS



1 Overview

Description

The TLD5045EJ is a highly integrated smart LED buck controller with built in protection functions. The main function of this device is to drive single or multiple series connected LEDs efficiently from a voltage source (V_S) higher than the LED forward voltage by regulating a constant LED current (I_{LED}). The constant current regulation is especially beneficial for LED color accuracy and long LED lifetime. The built in freewheeling diode and switching transistor with current sense requires fewer external components and saves system costs. High flexibility is achieved by placing low power resistors to adjust output currents up to 700 mA and the regulator switching frequency (typ. 200 kHz). An integrated PWM dimming engine provides an LED dimming function by placing a simple RC network to GND. This feature is dedicated for decentralized light modules without microcontroller involvement. In addition to this, an integrated status pull-down transistor can be used to simulate a minimum current flow for decentralized modules to avoid a wrong open load detection by a high-side switch located in the body control module (BCM).

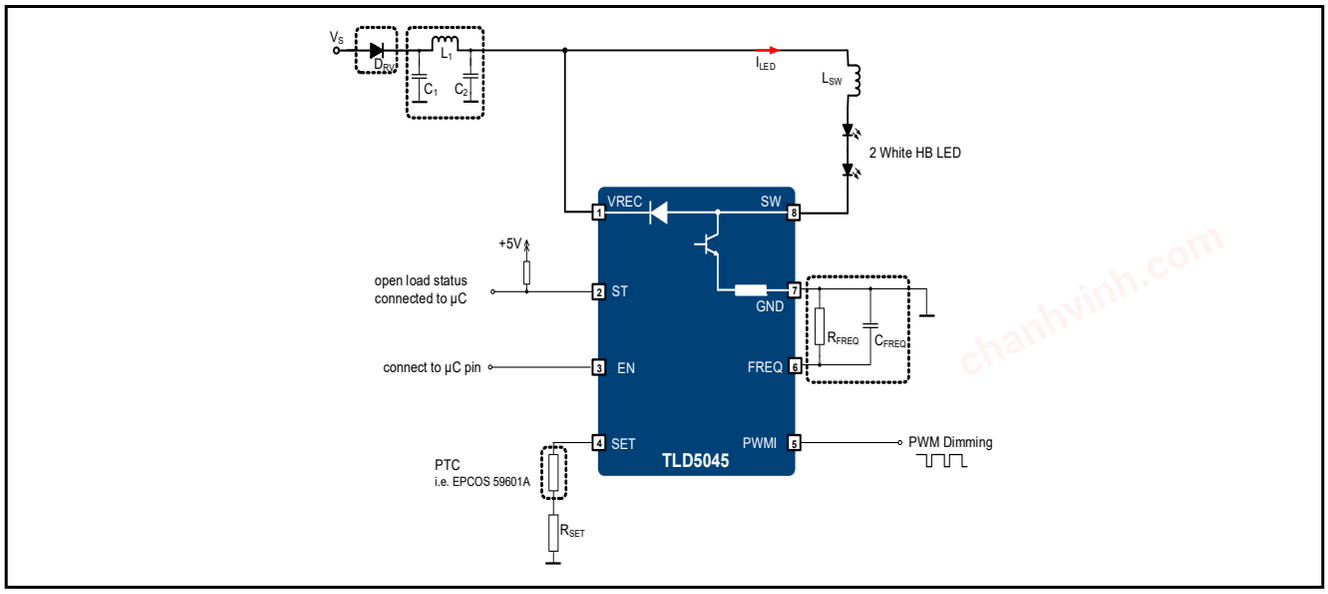


Figure 1 Simplified typical application

Type	Package	Marking
TLD5045EJ	PG-DSO-8 EP	TLD5045

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Potential applications

- Automotive LED driven exterior lighting: brake, tail, CHMSL, daytime running light, position light
- Automotive LED driven interior lighting: reading light, dome light, display backlighting

Features

- Constant current generation
- Wide input voltage range from 5 V to 40 V
- Peak current regulation
- Very low current consumption (< 2 µA) in sleep mode
- Integrated power transistor with low saturation voltage
- Integrated fast freewheeling diode
- Integrated load current sense resistor
- Integrated status pull-down transistor
- Overtemperature protection
- Switching frequency (typ. 200 kHz) adjustable via external RC network
- External PWM dimming input
- Integrated PWM dimming engine
- Analog dimming (output current adjustable via external low power resistor and possibility to connect PTC resistor for LED protection during overtemperature conditions)
- Stable switching frequency due to fix off-time concept with V_{REC} (supply voltage) feedforward
- Undervoltage and overvoltage shutdown with hysteresis
- Small thermally enhanced exposed heatslug SMD package
- Green product (RoHS) compliant

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

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Table of Contents

1 Overview ... 1
2 Block diagram ... 4
3 Pin configuration ... 5
3.1 Pin assignment ... 5
3.2 Pin definitions and functions ... 5
4 General product characteristics ... 7
4.1 Absolute maximum ratings ... 7
4.2 Functional range ... 8
4.3 Thermal resistance ... 8
5 General product characteristics ... 9
5.1 General parameters ... 9
5.2 Power supply monitoring ... 11
6 Enable, Dimming function and Thermal protection ... 12
6.1 Description ... 12
6.2 Electrical characteristics: Enable, Bias, Dimming function and Thermal protection ... 13
6.2.1 PWM dimming with µC connected to TLD5045EJ PWMI pin ... 14
6.2.2 Internal PWM dimming function ... 15
6.3 Overtemperature protection of the device ... 16
7 Open load diagnosis ... 17
7.1 Description ... 17
7.2 Electrical characteristics: Open load diagnosis ... 17
7.3 Open load diagnosis under different application conditions ... 18
7.3.1 Light module application without µC ... 18
7.4 Application with µC connected to TLD5045EJ IC ... 19
8 Application information ... 20
8.1 Output peak current adjustment via R_{SET} ... 20
8.2 Switching frequency determination ... 21
8.3 TLD5045EJ in different LED applications ... 23
8.3.1 TLD5045EJ in a Body Control Module (BCM) with µC Interface ... 23
8.3.2 Decentralized Light Module application - DLM (Input configuration 1) ... 24
8.3.3 Decentralized Light Module application - DLM (Input configuration 2) ... 25
8.3.4 Decentralized Light Module application - DLM (Input configuration 3) ... 26
9 Package outlines ... 27
10 Revision history ... 28

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2 Block diagram

The TLD5045EJ regulates the LED current by monitoring the load current (Peak current measurement) through the internal switch, cycle by cycle. When the current through the switch reaches the threshold I_{peak} the switch is shut off and it is kept off for a time equal to t_{OFF}. Both I_{peak} and t_{OFF} can be fixed through few external components.

The peak current I_{peak} is fixed by a resistor connected to the SET pin while the t_{OFF} is fixed by RC network. As t_{OFF} is fixed and the duty cycle depends on VREC, the frequency depends on VREC as well. Refer to **Chapter 8.2** for the evaluation of the switching frequency.

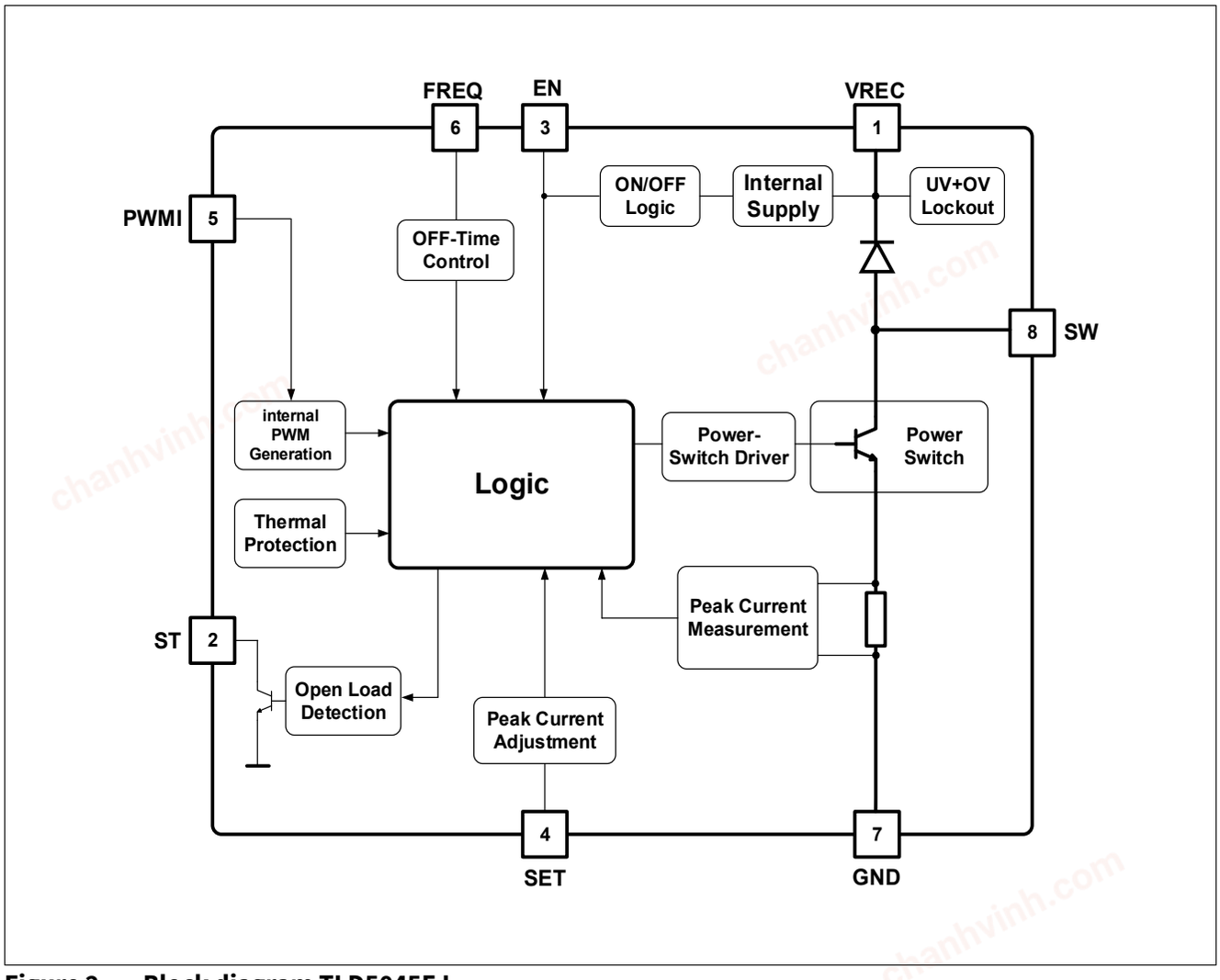


Figure 2 Block diagram TLD5045EJ

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3 Pin configuration

3.1 Pin assignment

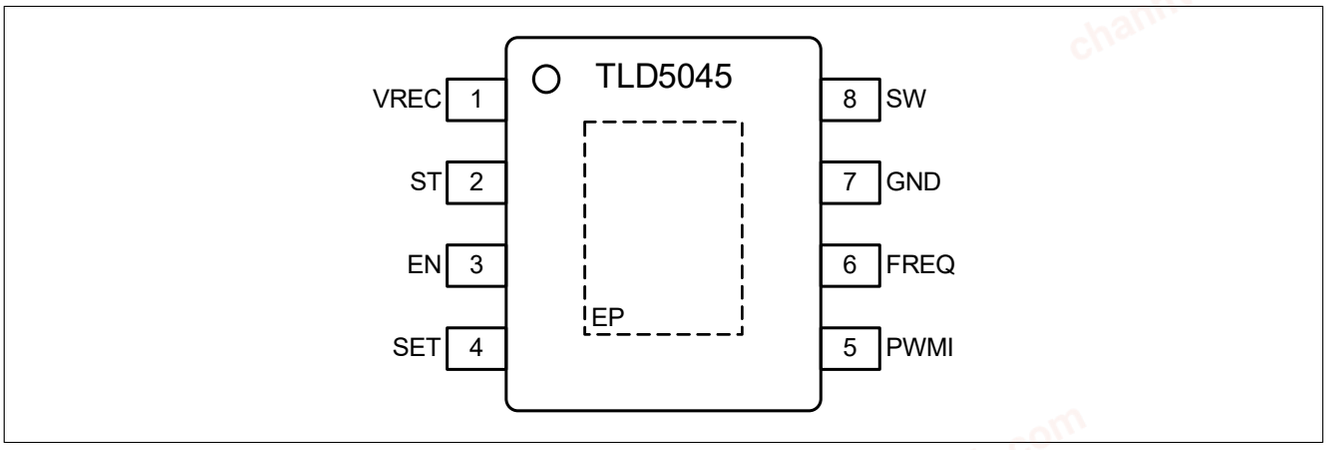


Figure 3 Pin configuration TLD5045EJ

3.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	VREC	**Voltage recirculation output and internal supply input** This pin is the supply pin of the IC (see **Figure 2**). Furthermore the cathode of the integrated fast freewheeling diode is connected to this pin as well
2	ST	**Status output** Open collector diagnostic output to indicate an open load failure Refer to **Chapter 7** for more details
3	EN	**Enable input** Apply logic “high” signal to enable the device
4	SET	**SET input** Connect a low power resistor to adjust the output current
5	PWMI	**PWM input** PWM signal for dimming LEDs. Connect external R and C combination to achieve an auto PWM-dimming function with defined frequency and duty cycle 1) internal PWM dimming function (external RC connected to GND) 2) external PWM dimming function (µC controls this pin) Refer to **Chapter 6** for more details
6	FREQ	**FREQuency select input** Connect external resistor and capacitor to GND to set the off-time of the switching frequency
7	GND	**Ground** Connect to system ground

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Pin configuration

Table 1 Pin definitions and functions

Pin	Symbol	Function
8	SW	**Integrated power-switch output** Collector of the integrated NPN-power transistor
EP		**Exposed pad** Connect to external heatspreading copper area with electrically GND (e.g. inner GND layer of the PCB via thermal vias)

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4 General product characteristics

4.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1)]

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage							
VREC (Pin 1) Recirculation and supply Input	V_{REC}	-0.3	–	45	V	–	P_4.1.1
ST (Pin 2) Diagnostic status output voltage	V_{ST}	-0.3	–	45	V	–	P_4.1.2
ST (Pin 2) Diagnostic status current	I_{ST}	–	–	150	mA	–	P_4.1.3
EN (Pin 3) Enable input voltage	V_{EN}	-0.3	–	45	V	–	P_4.1.4
SET (Pin 4) Peak current adjust input voltage	V_{SET}	-0.3	–	6	V	–	P_4.1.5
PWMI (Pin 5) PWM input voltage	V_{PWMI}	-0.3	–	6	V	–	P_4.1.6
FREQ (Pin 6) Off-time adjustment Input	V_{FREQ}	-0.3	–	6	V	–	P_4.1.7
SW (Pin 8) Switch output	V_{SW}	-0.3	–	45	V	–	P_4.1.8
Temperature							
Junction temperature	T_J	-40	–	150	°C	–	P_4.1.9
Storage temperature	T_{STG}	-55	–	150	°C	–	P_4.1.10
ESD Susceptibility							
ESD resistivity all pins to GND	$V_{ESD, HBM}$	-2	–	2	kV	HBM[2)]	P_4.1.11
ESD resistivity to GND	V_{ESD}	-500		500	V	CDM[3)]	P_4.1.12
ESD resistivity corner pins to GND	V_{ESD}	-750		750	V	CDM[3)]	P_4.1.13

1) Not subject to production test, specified by design.
2) ESD susceptibility HBM according to EIA/JESD 22-A 114B
3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

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2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 3 Functional range

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Extended supply voltage	V_{REC}	5	–	40	V	1) Parameter deviations possible	P_4.2.1
Nominal supply voltage range	V_{REC}	8	–	36	V	–	P_4.2.2
Output current range	I_{OUT}	100	–	700	mA	–	P_4.2.3
Switching frequency	f_{SW}	50	–	300	kHz	1) T_J = 25°C to 150°C	P_4.2.4
Junction temperature	T_J	-40	–	150	°C	–	P_4.2.5

1) Not subject to production test, specified by design

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

4.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For further information visit **https://www.jedec.org**.*

Table 4 Thermal resistance

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	10	–	K/W	1)2)	P_4.3.1
Junction to ambient (2s2p)	R_{thJA}	–	40	–	K/W	1)3)	P_4.3.2

1) Not subject to production test, specified by design

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are ambient temperature) T_A = 25°C. Power switch and freewheeling diode dissipate 1 W

3) Specified R_{thJA} value is according to JEDEC JESD51-2,-7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu)

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5 General product characteristics

5.1 General parameters

Table 5 Electrical characteristics: Buck regulator

V_{REC} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage drop over power transistor	$V_{Drop,100}$	–	0.8	–	V	I_{peak}=100 mA	P_5.1.1
Voltage drop over power transistor	$V_{Drop,700}$	–	1.4	–	V	I_{peak}=700 mA	P_5.1.2
Freewheeling diode forward voltage	$V_{fw,100}$	–	0.8	–	V	I_{peak}=100 mA	P_5.1.3
Freewheeling diode forward voltage	$V_{fw,700}$	–	1.4	–	V	I_{peak}=700 mA	P_5.1.4
Peak overcurrent limit	I_{peak_lim}	–	1.4	–	A	–	P_5.1.5
Peak current accuracy	I_{peak_acc}	450	500	550	mA	V_{REC} = 12 V V_{EN} = 5 V V_{LED} = 7.2 V R_{SET} = 14 kΩ L_{SW} = 220 µH f_{SW} = 200 kHz	P_5.1.6
Input undervoltage shutdown threshold	$V_{REC,UVOFF}$	–	–	5	V	V_{EN} = 5 V V_{REC} decreasing; see **Figure 4**	P_5.1.7
Input voltage startup threshold	$V_{REC,UVON}$	–	–	6	V	V_{EN} = 5 V V_{REC} increasing; see **Figure 4**	P_5.1.8
Input undervoltage shutdown hysteresis	$V_{REC,UVhyst}$	–	1	–	V	V_{EN} = 5 V	P_5.1.9
Input overvoltage shutdown threshold	$V_{REC,OVOFF}$	40.5	–	–	V	V_{EN} = 5 V V_{REC} increasing; see **Figure 4**	P_5.1.10
Input overvoltage startup threshold	$V_{REC,OVON}$	40	–	–	V	V_{EN} = 5 V V_{REC} decreasing; see **Figure 4**	P_5.1.11
Input overvoltage shutdown hysteresis	$V_{REC,OVhyst}$	–	1.5	–	V	V_{EN} = 5 V	P_5.1.12
Switch-on delay	t_{dON}	–	400	600	ns	[1] –	P_5.1.13
Switch-off delay	t_{dOFF}	–	500	850	ns	[1] –	P_5.1.14
Reference voltage at SET pin	V_{SET}	1.16	1.225	1.29	V	–	P_5.1.15

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Table 5 Electrical characteristics: Buck regulator (continued)

V_{REC} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Pull-up current for FREQ pin	I_{FREQ}	5	–	–	mA	V_{FREQ} = 0 V Current flows out of pin	P_5.1.16
Oscillator switch-off threshold	$V_{FREQ,HIGH}$	–	3.2	–	V	–	P_5.1.17
Oscillator switch-on threshold	$V_{FREQ,LOW}$	–	1.2	–	V	–	P_5.1.18

1) The minimum switching “on” time t_{ON} must be greater than $t_{dON} + t_{dOFF}$

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5.2 Power supply monitoring

Overvoltage and undervoltage shutdown

If the supply voltage V_{REC} drops below the input undervoltage threshold voltage ($V_{REC,UVOFF}$), the power stage is switched off.

If V_{REC} rises again and reaches the input undervoltage startup threshold $V_{REC,UVON}$ the power stage is restarted and the device is back to normal operation mode.

Same behaviour applies to overvoltage.

The internal status transistor switches off during an overvoltage or undervoltage event on V_{REC}.

A detailed description of the under and overvoltage behaviour is displayed in **Figure 4** below.

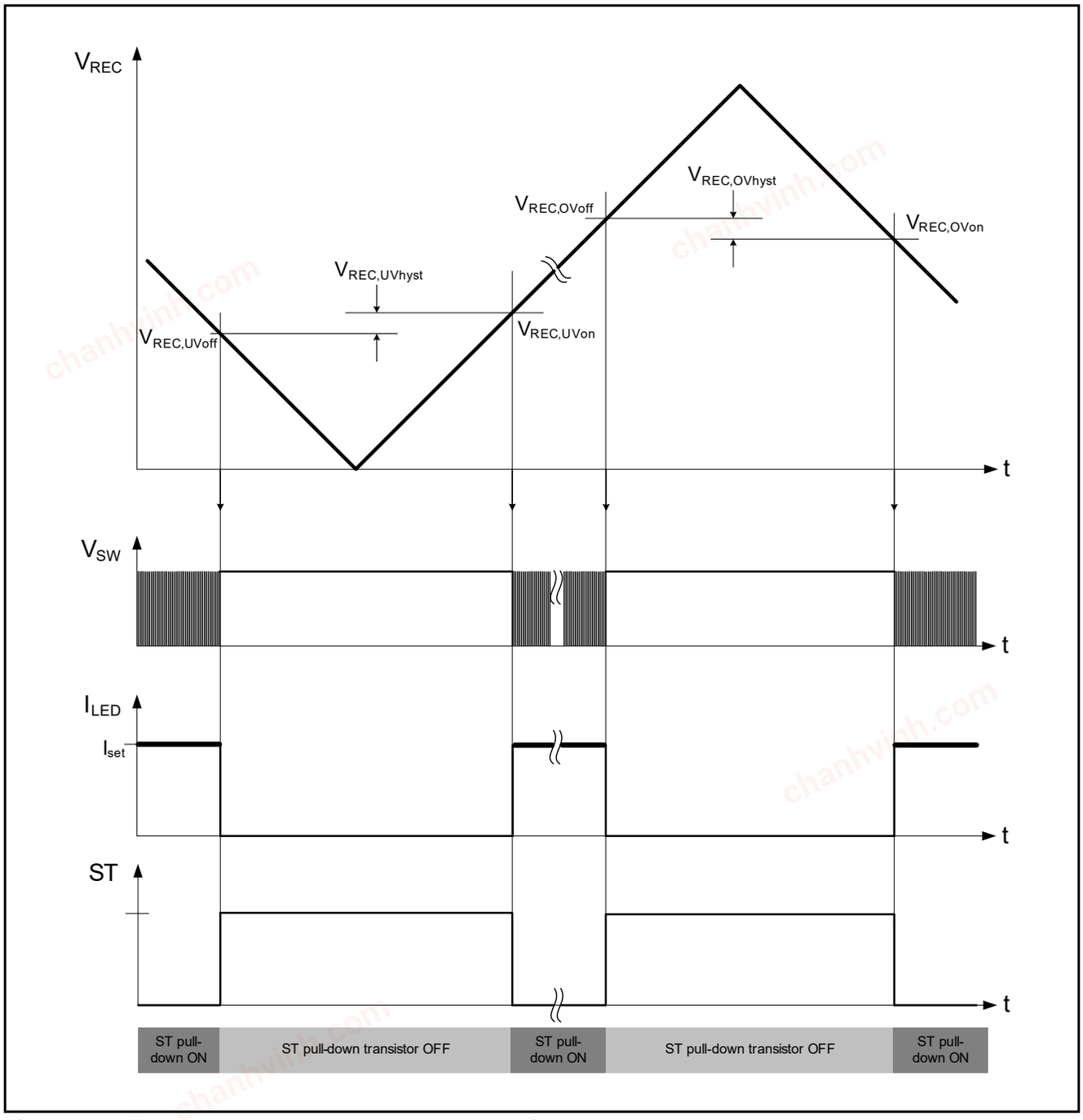


Figure 4 Overvoltage and undervoltage protection

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6 Enable, Dimming function and Thermal protection

6.1 Description

Enable function

A logic high signal on the EN pin turns the device on. A logic low signal on enable pin EN brings the device into sleep mode. The current consumption is typically 0.1 µA ($I_{q,OFF}$, see P_6.2.1). The EN pin has an internal pull-down resistor which ensures that the IC is in sleep mode and the power stage is switched off in case the pin EN is externally not connected.

Dimming function

The PWMI pin combines two functions:

1. PWM dimming via a µC (3.3 V and 5 V µC)
2. Integrated PWM dimming engine for standalone solutions in decentralized light module (frequency and duty cycle adjustable via external RC network)

A detailed description of the PWMI pin is displayed in **Figure 5**, below.

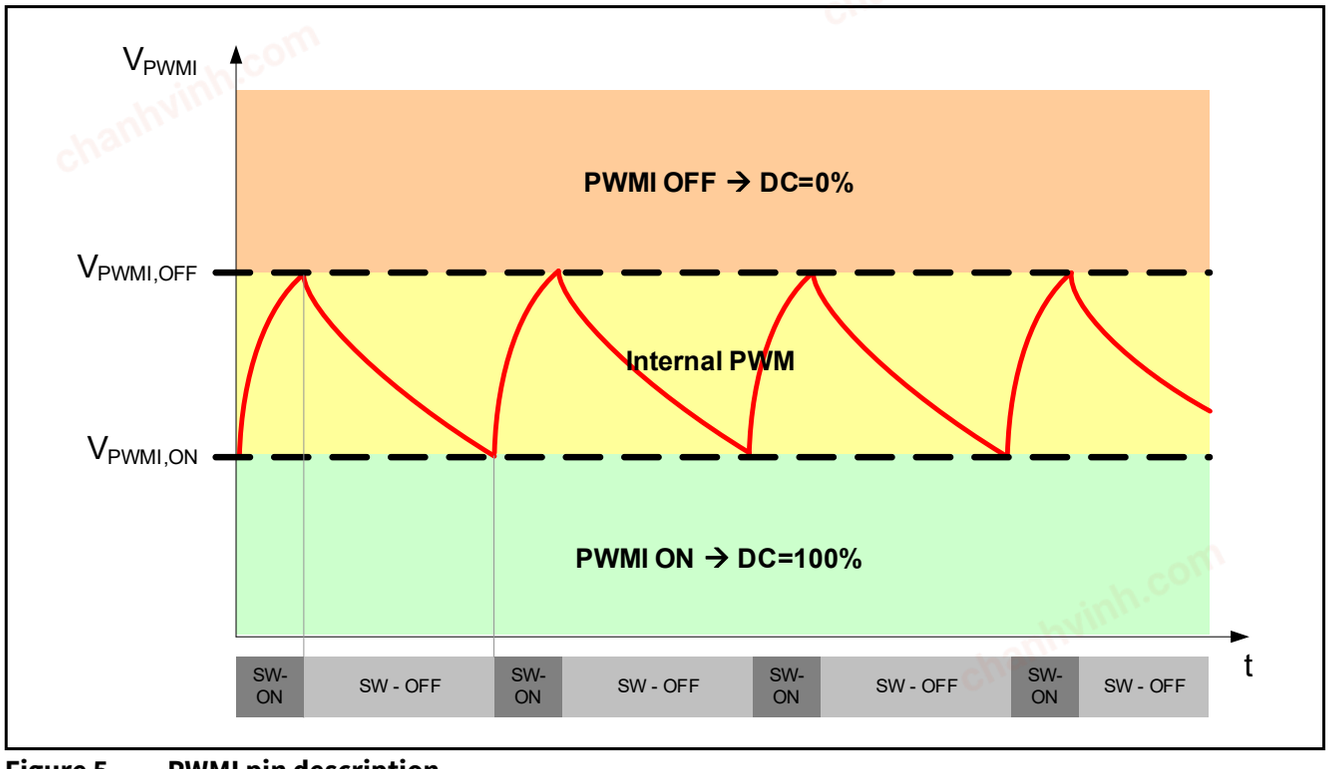


Figure 5 PWMI pin description

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6.2 Electrical characteristics: Enable, Bias, Dimming function and Thermal protection

Table 6 Electrical characteristics: Enable, Bias, Dimming function and Thermal protection

V_{REC} = 8 V to 36 V, T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption, sleep mode	$I_{q,OFF}$	–	0.1	2	µA	V_{EN} = 0 V; V_{REC} = 16 V	P_6.2.1
Current Consumption, active mode (Open Load)	$I_{q,OL}$	–	–	5	mA	V_{EN} = 5 V; I_{peak} = 0 mA (open load); V_{REC} = 16 V	P_6.2.2
Current Consumption, active mode	$I_{q,ON}$	–	–	10	mA	V_{EN} = 5 V; I_{peak} = 700 mA V_{REC} = 16 V	P_6.2.3
EN Turn on threshold	$V_{EN,ON}$	2.8	–	–	V	–	P_6.2.4
EN Turn off threshold	$V_{EN,OFF}$	–	–	0.8	V	–	P_6.2.5
EN high input current	$I_{EN,hi}$	–	100	–	µA	V_{EN} = 5 V	P_6.2.6
EN low input current	$I_{EN,lo}$	0	–	20	µA	V_{EN} = 0.5 V	P_6.2.7
PWMI Turn on threshold	$V_{PWMI,ON}$	–	1	–	V	see **Figure 5**	P_6.2.8
PWMI Turn off threshold	$V_{PWMI,OFF}$	–	2	–	V	see **Figure 5**	P_6.2.9
PWMI source current	I_{PWMI}	–	250	–	µA	R_{set} = 10 kΩ V_{PWMI}= 0.5 V Current flows out of pin	P_6.2.10
Overtemperature shutdown	$T_{J,sd}$	150	175	–	°C	1)	P_6.2.11
Overtemperature shutdown hysteresis	T_{J,sd_hyst}	–	15	–	°C	1)	P_6.2.12

1) Specified by design. Not subject to production test.

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6.2.1 PWM dimming with µC connected to TLD5045EJ PWMI pin

The PWMI pin can be used for PWM dimming. It is a commonly practiced dimming method to prevent color shift in LED light applications.

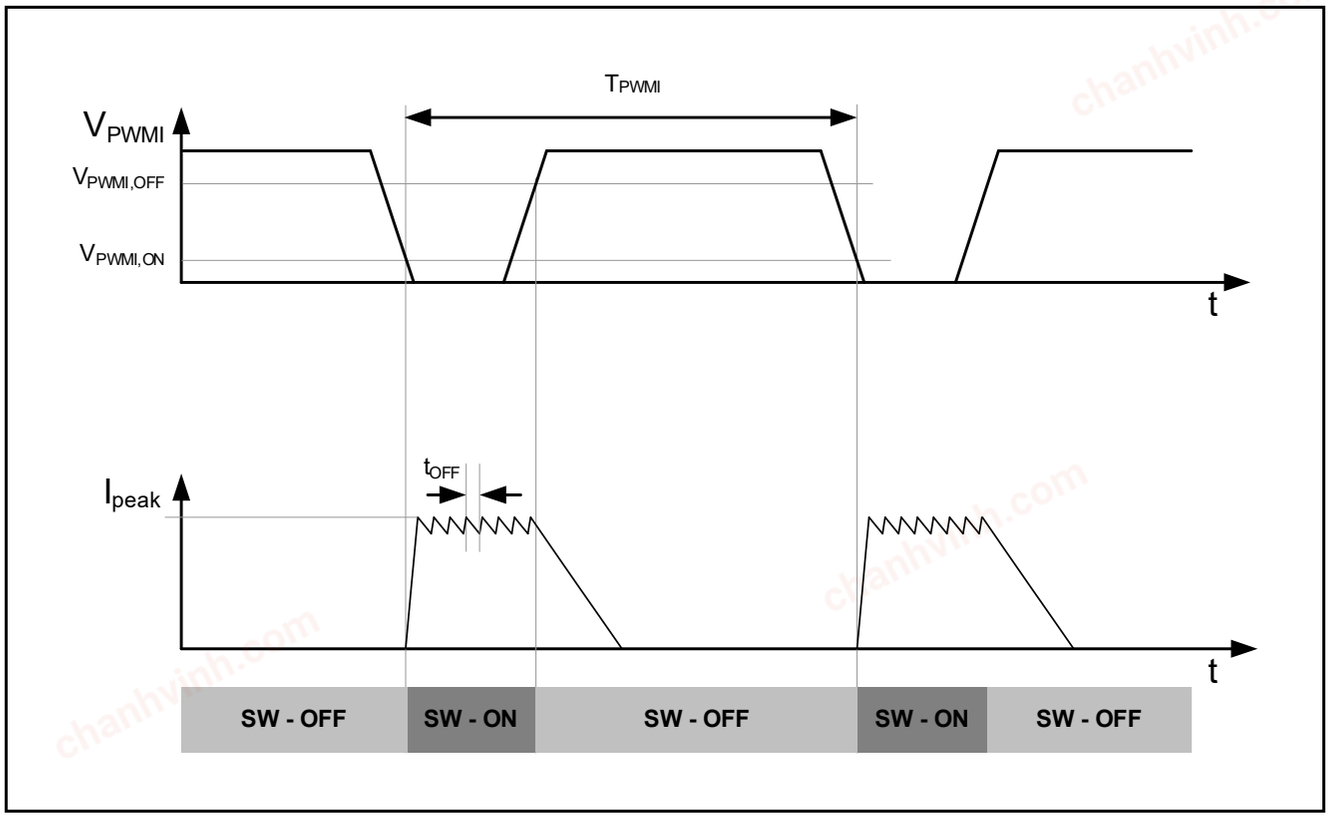


Figure 6 Timing diagram for LED dimming with µC

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6.2.2 Internal PWM dimming function

The TLD5045EJ has an integrated PWM dimming engine. Via an external R_{PWM} and C_{PWM} network it is possible to achieve a PWM LED current waveform. The duty cycle and dimming frequency depends on the size of the external components (see **Table 7**). This feature is specially designed to achieve a standalone PWM dimming function without the usage of microcontrollers or external logic. This allows a flexible and cost effective usage of the device in a decentralized light module application (refer to application drawing **Figure 14**).

The advantage of a PWM dimming (to reduce the LED load current) is the change of light intensity only, at constant light color.

With an external RC network a PWM programming between 100 Hz and 1200 Hz and duty cycles between 4% and a maximum of 20% is possible. **Table 7** displays the external components corresponding to the desired PWM frequency and duty cycle.

The following setup applies for **Table 7**:

- V_{REC} = 12 V
- V_{LED} = 7.2 V
- L_{SW} = 220 µH
- R_{SET} = 14 kΩ

Table 7 R_{PWMI} and C_{PWMI} versus f_{PWMI} and DC

R_{PWMI} [kΩ]	C_{PWMI} [nF]	f_{PWMI} [Hz]	DC [%]
216	64	100	4
216	32	200	4
216	21	300	4
216	16	400	4
87	150	100	10
87	75	200	10
87	50	300	10
87	37	400	10
44	265	100	20
44	132	200	20
44	88	300	20
44	66	400	20

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6.3 Overtemperature protection of the device

A temperature sensor at the power stage causes the overheated device to switch off to prevent destruction. During overtemperature condition the internal ST transistor is switched off. Due to the autorestart function of the device the status signal will toggle accordingly. The timing of this pattern is dependant on the thermal capability of the application and can be used to distinguish between open load error and overtemperature condition. More details on the overtemperature behavior is displayed in **Figure 7** below.

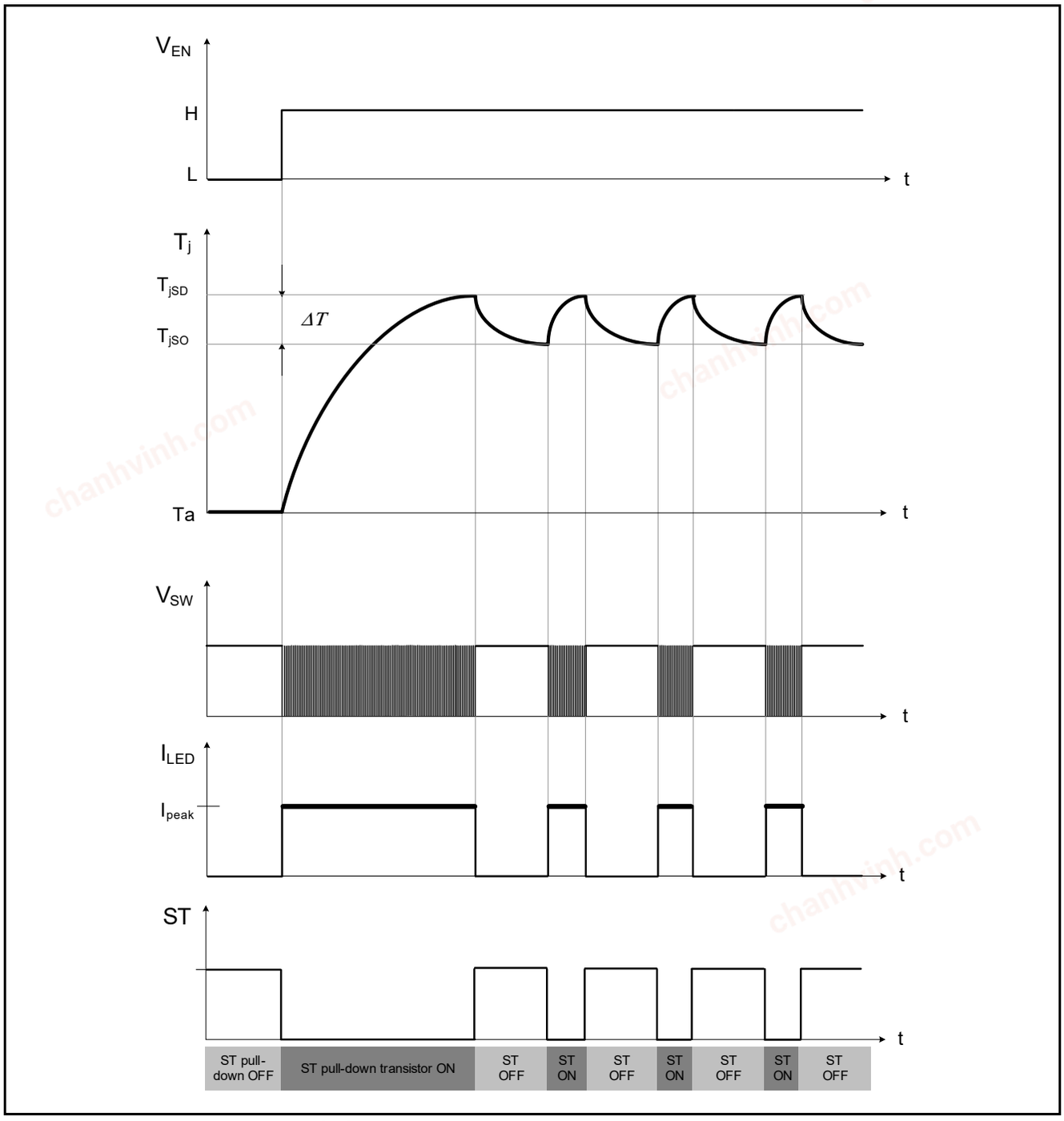


Figure 7 Overtemperature behavior

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7 Open load diagnosis

7.1 Description

The TLD5045EJ has an integrated open load during “on” diagnosis. During normal operation the ST pin (open collector output) is pulled to GND (internal transistor is on). The open load detection is realized by monitoring the switching behavior at the SW pin. During an open load event the integrated power stage at the SW pin will be statically turned on. If the output stage is turned on for more than the open load diagnosis delay time (t_{OL}) an open load condition is detected. An open load event will switch off the internal transistor. If a µC is connected to the ST pin an external pull-up resistor should be placed to achieve a logic “high” level for the proper open load error signalling reporting. For a timing diagram on the functionality of the open load diagnosis please refer to **Figure 8** and **Figure 9**.

7.2 Electrical characteristics: Open load diagnosis

Table 8 Functional Range

V_{REC} = 8 V to 36 V, T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Open load diagnosis delay time	t_{OL}	20	–	–	µs	–	P_7.2.1
Voltage drop over internal ST transistor	$V_{Drop,ST}$	–	0.3	–	V	I_{ST} = 150 mA	P_7.2.2
Open Load diagnosis current	I_{OL}	–	50	–	mA	V_{EN} = 4.5 V	P_7.2.3

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7.3 Open load diagnosis under different application conditions

7.3.1 Light module application without µC

Most of the time, the open load diagnosis of the whole light module is done via the current sense of the driver IC (e.g. PROFET) located in the light control module (or BCM module). See **Figure 14** for a simplified application schematic. The light module needs to sink to a specified minimum current (e.g. 100 mA) to indicate normal operation. To guarantee this minimum current also under light load conditions (e.g. high efficiency LED bin at high supply voltages = min. load current required) system designers often have to place resistors in parallel to the application circuit (see resistors connected to supply lines in **Figure 14**). When using such resistors connected between Vs and GND, an open LED diagnosis is not possible anymore. To overcome this issue an internal transistor (open collector) is connected to the ST pin of the TLD5045EJ. During normal operation the ST pin is low and a minimum module current can be guaranteed.

As soon as an open load occurs the internal ST transistor switches off. Due to this, the current on the VREC pin decreases below the open load detection threshold of the driver IC located in the light control module.

Note: Open Load is only detected during the “on” cycle of the switching transistor. During the “off”state the ST signal displays what was detected in the previous “on”state.

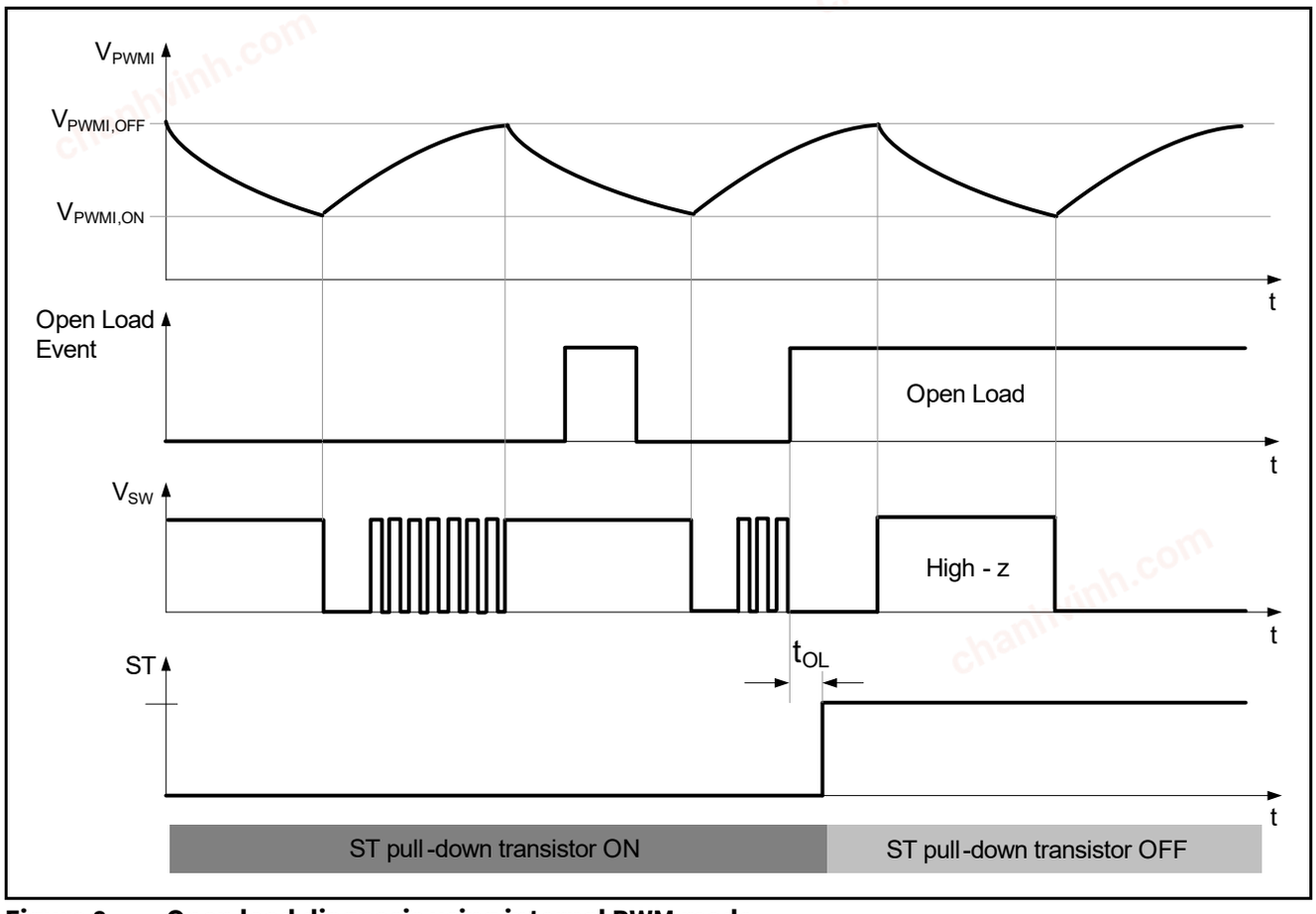


Figure 8 Open load diagnosis using internal PWM mode

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7.4 Application with µC connected to TLD5045EJ IC

The ST pin can be connected directly to a µC input. During an open load condition the ST transistor is off. An external pull-up resistor connected to V_{DD} is required to signal a logic high signal on the ST pin during an open load error. Please consider that this diagnosis functionality is only active if the device is in active mode (high potential at the EN pin).

Refer to application drawing **Figure 13**.

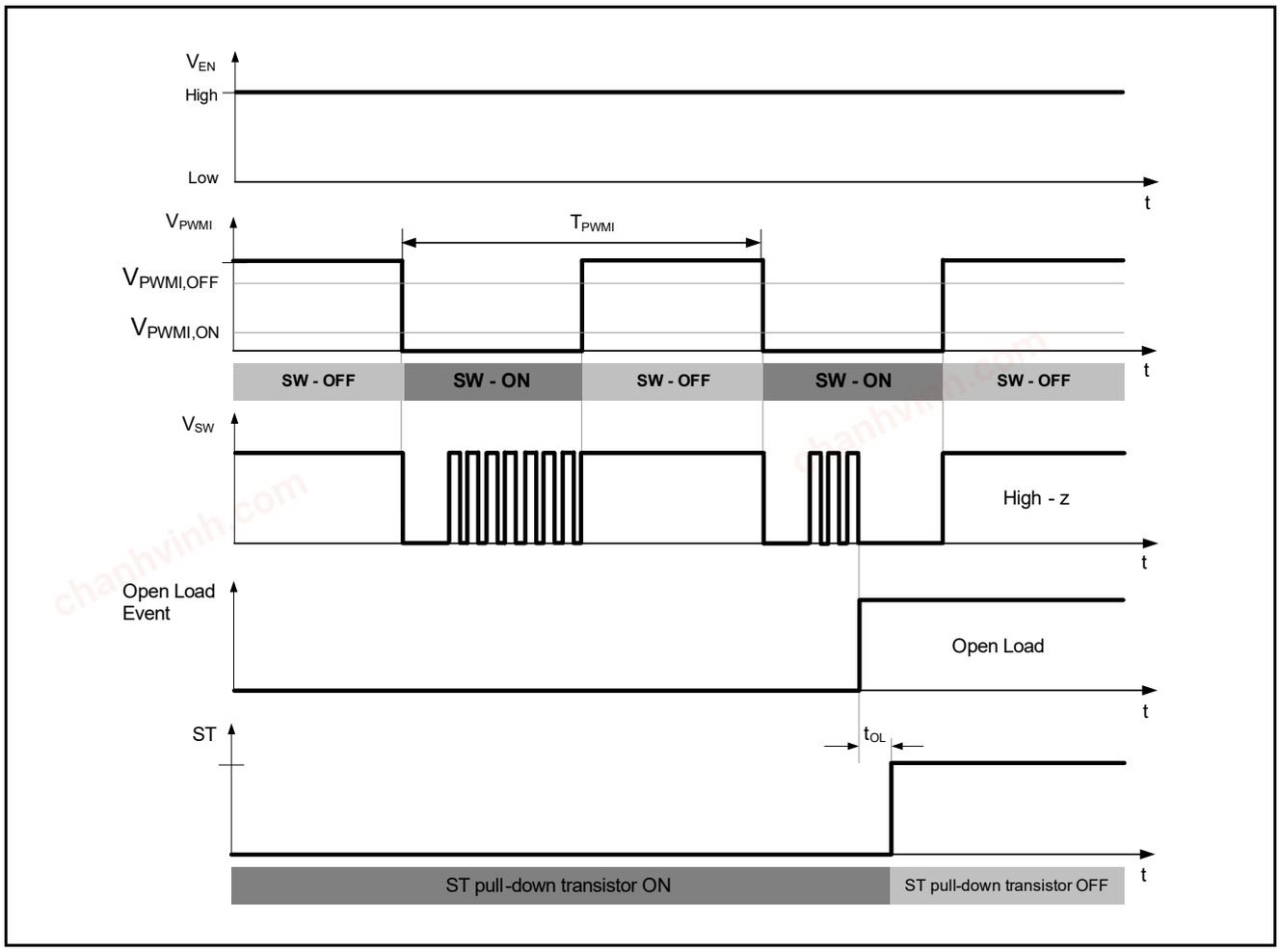


Figure 9 Open load diagnosis via µC connected to ST pin

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8 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

8.1 Output peak current adjustment via R_{SET}

The external resistor R_{SET} is used to adjust the peak current of the regulator. Maximum achievable peak current is 700 mA and minimum achievable peak current is 100 mA. The SET pin provides an internally fixed voltage level at typically 1.225 V. The following equation can be deduced:

(8.1)

$$Ipeak = \left(\frac{1.225\ V}{R_{SET}} \right) \cdot 5710$$

The factor 5710 is derived from following considerations:

- $I_{peak,\ max}$ = 700 mA (R_{SET} = 10 kΩ)
- $I_{peak,\ min}$ = 100mA (R_{SET} = 70 kΩ)

Internal comparator voltage at SET pin = 1.225 V.

The circuitry behind the SET pin adjusts higher peak currents with lower R_{SET} values.

The R_{SET} value should be in the range from 10 kΩ to 70 kΩ to achieve the requested peak current range.

The following setup applies for the values displayed in **Figure 10**:

- V_{REC} = 12 V
- V_{LED} = 7.2 V
- L_{SW} = 220 µH

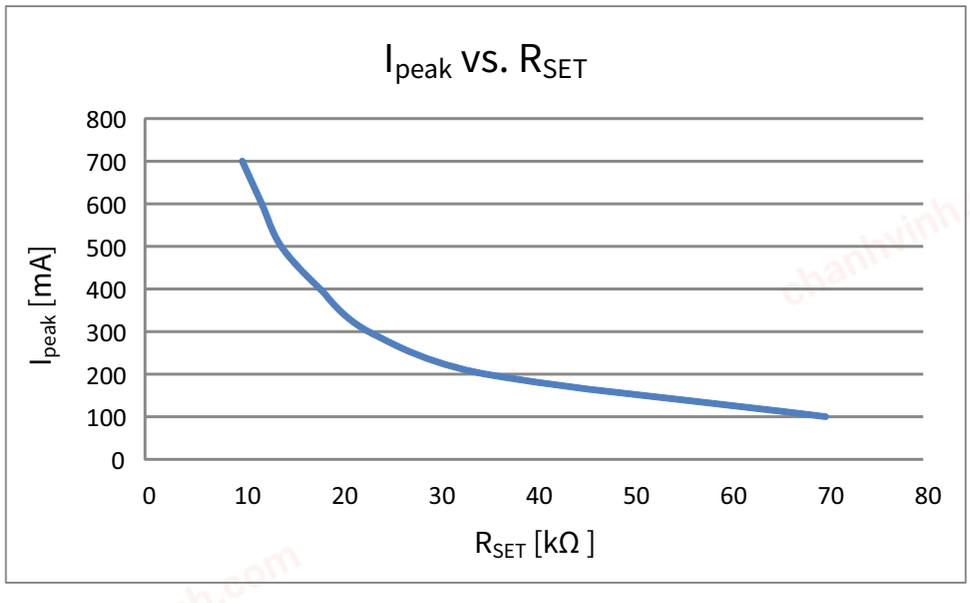


Figure 10 R_{SET} resistor selection

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8.2 Switching frequency determination

With the external R_{FREQ}, C_{FREQ} and R_{COMP} network, it is possible to adjust the switching frequency of the regulator. To ensure a stable frequency over a broad range of input voltage V_{REC} an external resistor R_{COMP} can be used.

The following setup applies to **Table 9**:

- V_{REC} = 12 V,
- V_{LED} =7.2V
- L_{SW} = 220 µH
- R_{SET} = 14 kΩ

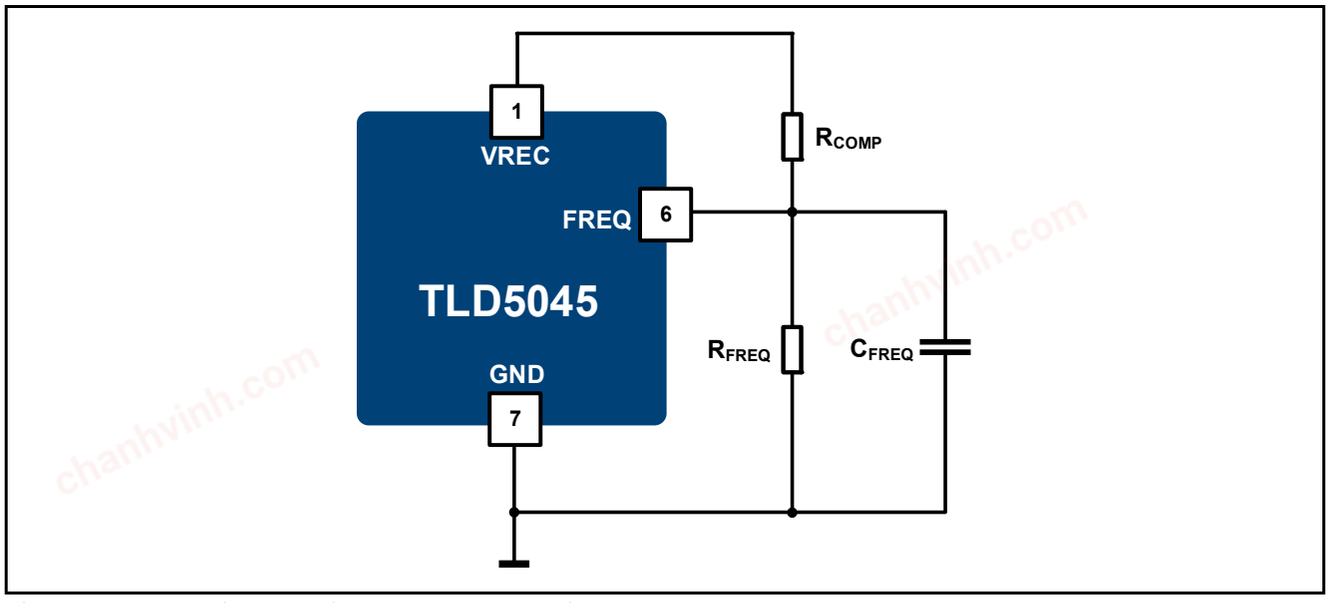


Figure 11 Setting t_{OFF} time of regulator with external R_{FREQ}, C_{FREQ} network

Table 9 R_{comp}, R_{freq}, C_{freq}, F_{SW}, t_{off} table

R_{comp} [kΩ]	R_{freq} [kΩ]	C_{freq} [pF]	f_{SW} [kHz]	t_{off} [µs]
255.8	17.1	220	50	6.47
115.8	7.7	220	100	3.19
69.7	4.6	220	150	2.12
46.8	3.1	220	200	1.59
72.8	4.9	100	250	1.27
52.7	3.5	100	300	1.06

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Application information

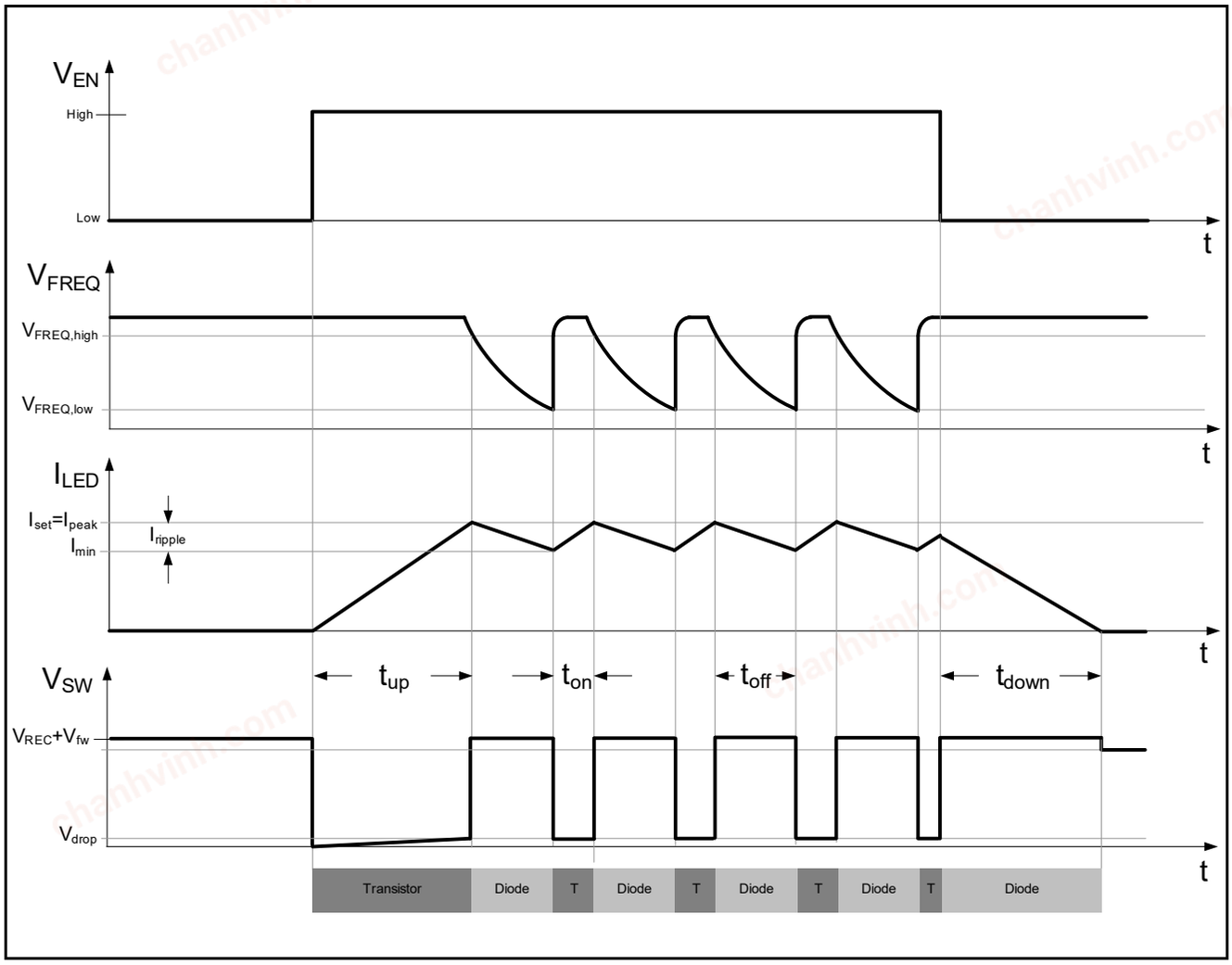


Figure 12 Theoretical operating waveforms

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8.3 TLD5045EJ in different LED applications

8.3.1 TLD5045EJ in a Body Control Module (BCM) with µC Interface

Figure 13 provides a simplified application with two high brightness LEDs in series. A µC controls the EN pin to put the device into sleep/active mode. Also the PWMI pin can be directly controlled via a µC port if PWM dimming of the LED current is required. The open load ST pin monitors the load condition of the application and gives feedback to the µC. An external pull-up resistor is recommended to achieve a logic “high” signal during an open load error (internal status transistor is switched off and the ST pin is high, external pull-up resistor ensures a logic “high” signal).

The external low power resistor R_{SET} is used to set the required peak current for the LED load (refer to **Figure 10** for more details).

To set the desired switching frequency of the buck regulator the external R_{FREQ} and C_{FREQ} network must be connected to GND (reference values are given in **Table 9**).

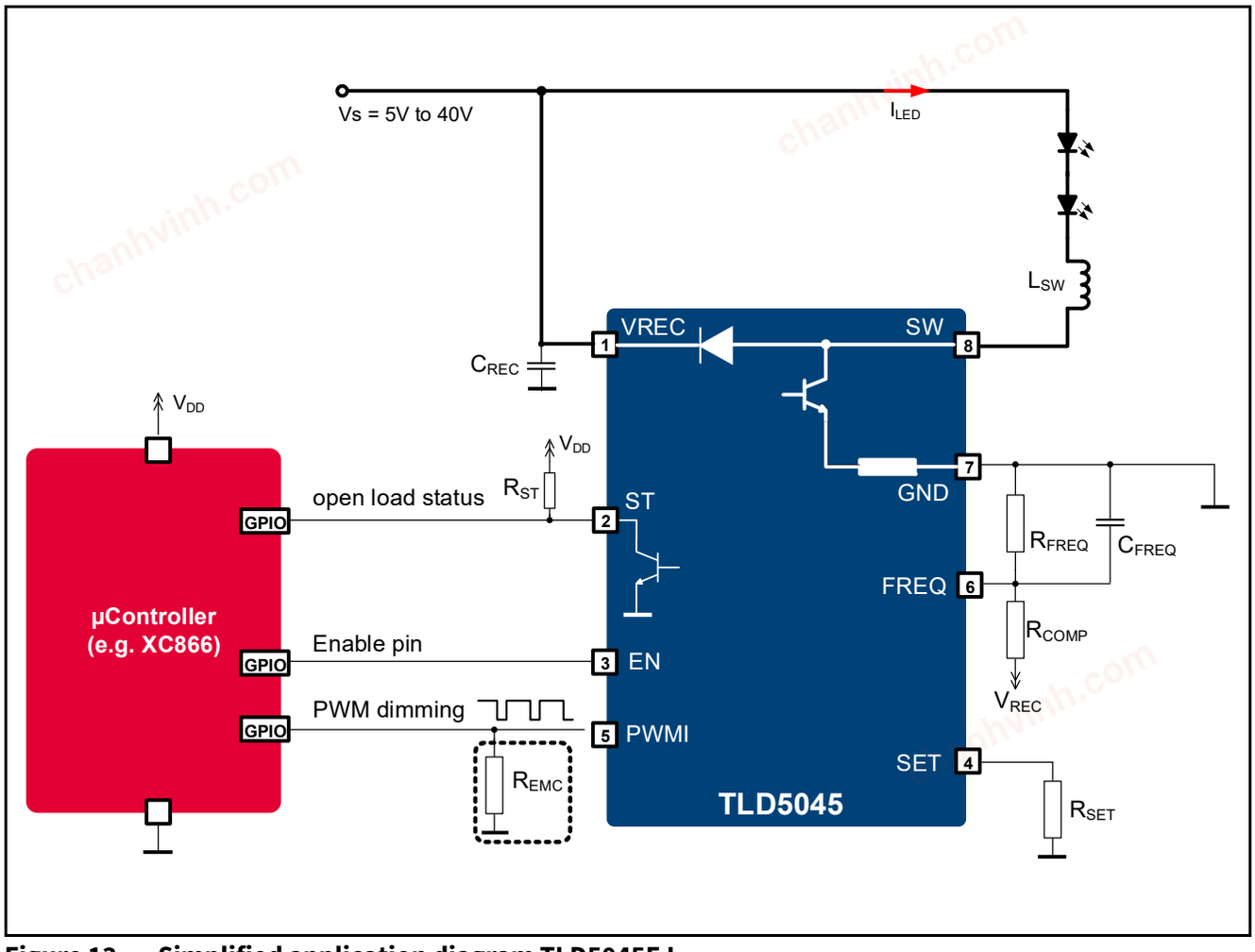


Figure 13 Simplified application diagram TLD5045EJ

Note: This is a very simplified example of an application circuit. The function must be verified in the real application

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8.3.2 Decentralized Light Module application - DLM (Input configuration 1)

The connection between the body control module (BCM), supplied by Vbat and the decentralized light module, supplied by V_S, is realized via only power line and one GND connection.

The supply line could change between two different operation modes:

1. **Light Function 1 - Daytime Running Light (DRL) mode:** If the supply line is permanently “on”, the DRL application which requires higher LED current (e.g. 400 mA) is active. The proper R_{SET} resistor should be placed to achieve the desired load current (e.g 18 kΩ).
2. **Light Function 2 - Position Light (PL) mode:** During a PWM signal (e.g. 200 Hz) on the supply line the mean LED current is reduced to a lower level (e.g. 50 mA) and the application enters into PL mode. The enable pin of the TLD5045EJ is a high voltage pin (max. 45 V) and can be directly connected via a resistor R_{EN} before the reverse polarity protection diode of the module to achieve a fast capture of the PWM signal. The PWMI pin is connected to GND (inverse logic = “on”).

To simulate a module current during light load conditions, the ST pin can be connected via a resistor to the supply voltage line. (refer to **Chapter 7** for a detailed description of the ST behavior)

For a decentralized solution without microcontroller involvement the possibility to connect a PTC resistor at the SET pin is a cost effective solution to protect the LED load from thermal destruction.

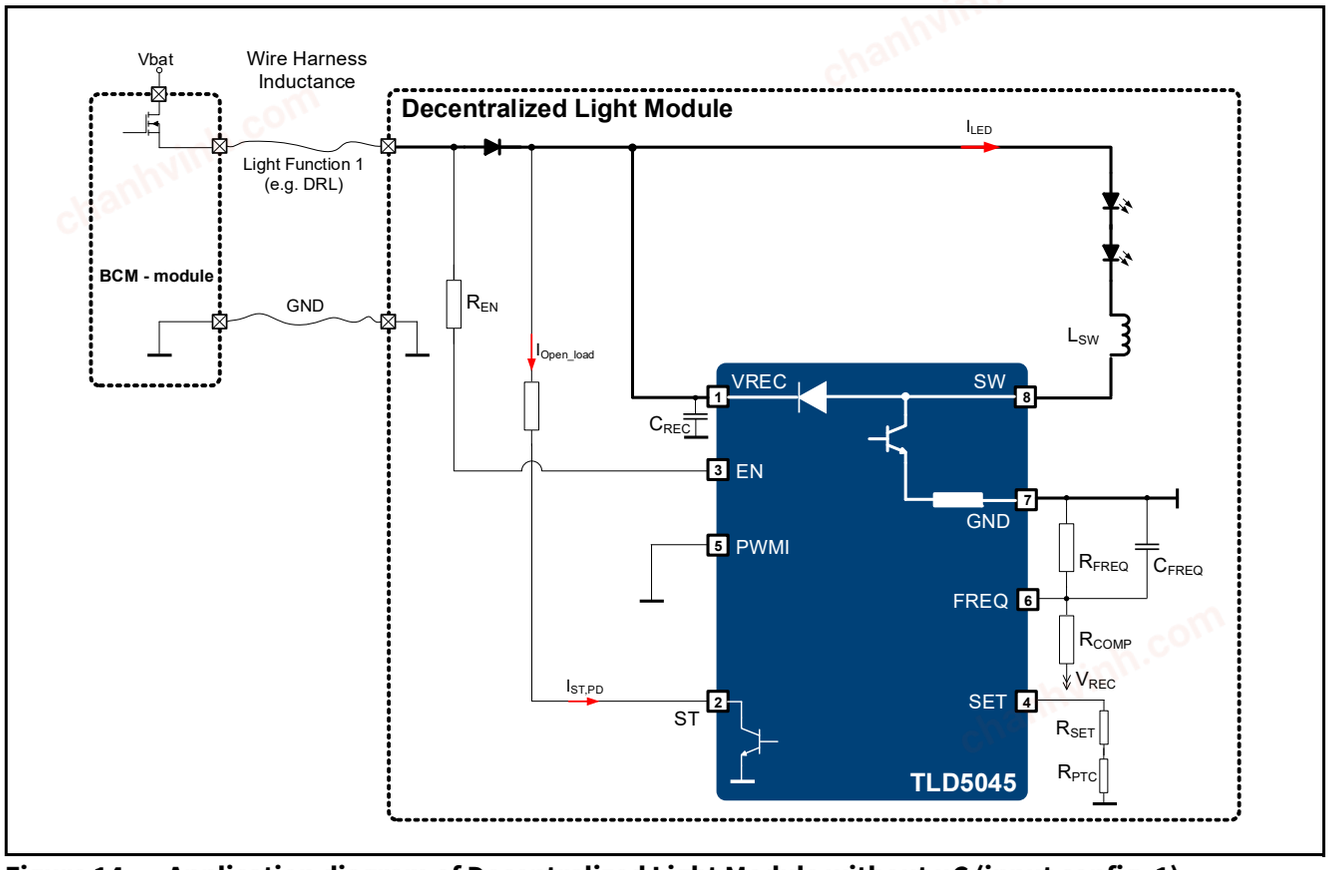


Figure 14 Application diagram of Decentralized Light Module without µC (input config. 1)

Note: This is a very simplified example of an application circuit. The function must be verified in the real application

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8.3.3 Decentralized Light Module application - DLM (Input configuration 2)

In this particular input configuration two supply lines are tied together on the DLM. The following input states must be considered to distinguish between Light Function 1 (DRL mode) and Light Function 2 (PL mode).

1. Condition: DRL = ON, PL = OFF. Desired function: DRL mode (e.g. 400 mA LED load current)
2. Condition: DRL = OFF, PL = ON. Desired function: PL mode (e.g. 50 mA LED load current)
3. Condition: DRL = ON, PL =ON. Desired function: PL mode (e.g. 50 mA LED load current)

To achieve a lower mean LED load current during the PL mode the integrated PWM engine is a useful feature. The external RPWM and CPWM circuit predefines a dedicated PWM frequency and duty cycle. (for details refer to **Table 7**)

To simulate a module current during light load conditions the ST pin can be connected via resistors to both supply voltage lines. (refer to **Chapter 7** for a detailed description of the ST behavior)

For a decentralized solution without microcontroller involvement, the possibility to connect a PTC resistor at the SET pin is a cost effective solution to protect the LED load from thermal destruction.

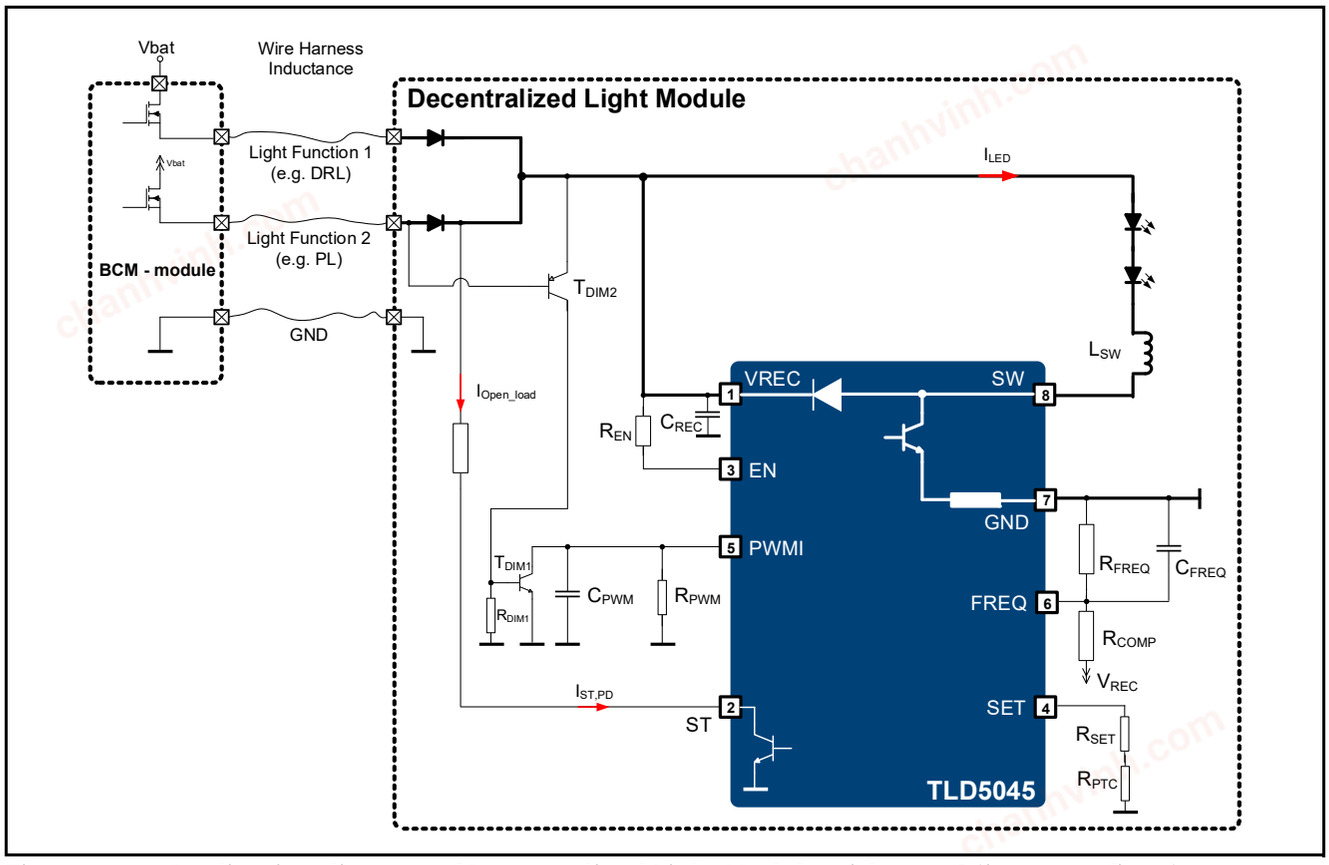


Figure 15 Application diagram of Decentralized Light Module without µC (input config. 2)

Note: This is a very simplified example of an application circuit. The function must be verified in the real application

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8.3.4 Decentralized Light Module application - DLM (Input configuration 3)

A permanent supply chooses the Light Function 1 (DRL mode) and a second dedicated PWM supply between 100 Hz and 200 Hz switches to Light Function 2 (PL mode). For this input configuration, it is possible to connect the PWM dimming output of the BCM directly to the PWMI input of the TLD5045EJ. To simulate a module current during light load conditions the ST pin can be connected via a resistor to the permanent supply voltage line. (refer to **Chapter 7** for a detailed description of the ST behavior)

For a decentralized solution without microcontroller involvement the possibility to connect a PTC resistor at the SET pin is a cost effective solution to protect the LED load from thermal destruction. (for details refer to **Figure 14**)

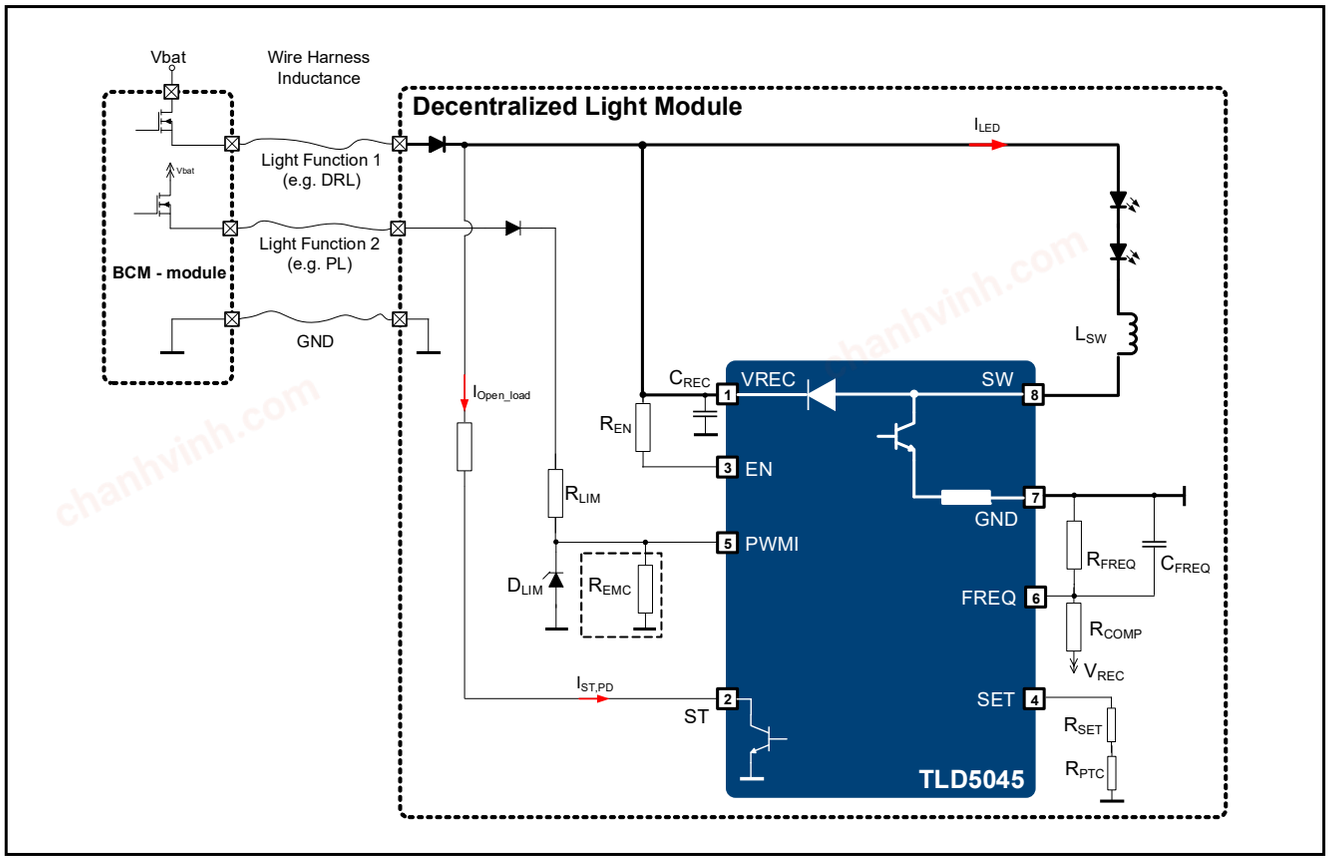


Figure 16 Application Diagram of Decentralized Light Module without µC (input config. 3)

Note: This is a very simplified example of an application circuit. The function must be verified in the real application

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9 Package outlines

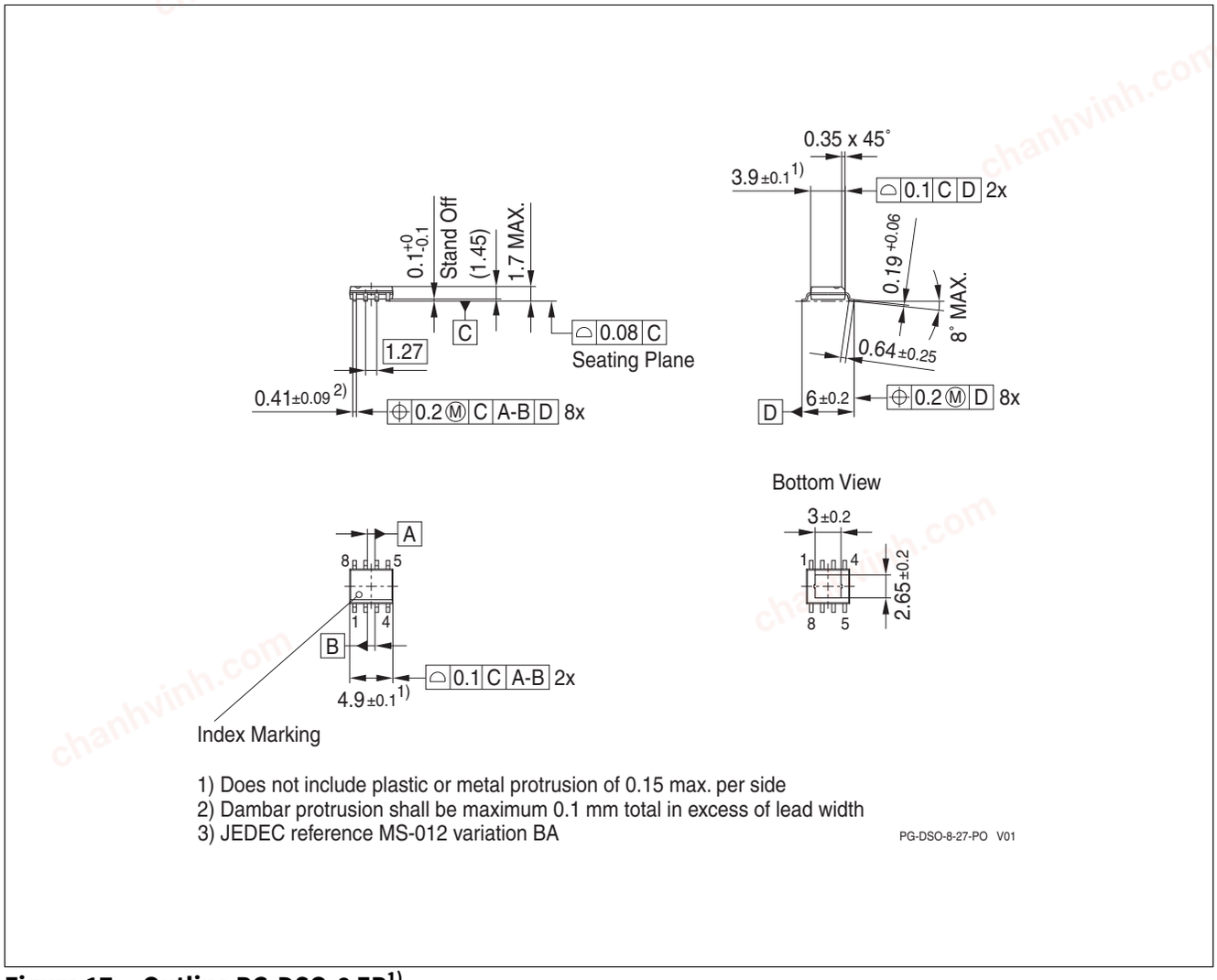


Figure 17 Outline PG-DSO-8 EP[1)]

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimesions in mm

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10 Revision history

Revision	Date	Changes
1.2	2018-09-12	Revision history from 2015-05-28 updated, revision number corrected (1.0 -> 1.1) P_4.1.2: removed P_4.2.3: removed **Table 5**: inserted test conditions P_5.1.12 updated (typ 0.5 → 1.5)
1.1	2015-05-28	Brand name change to LITIX™ Power
1.0	2011-05-27	Initial datasheet for TLD5045EJ available

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