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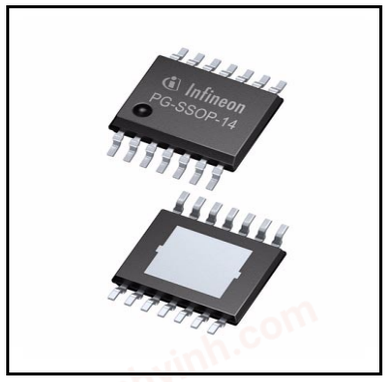
LITIX™ Basic

TLD1124EL

1 Channel High-Side Current Source

AEC Qualified RoHS

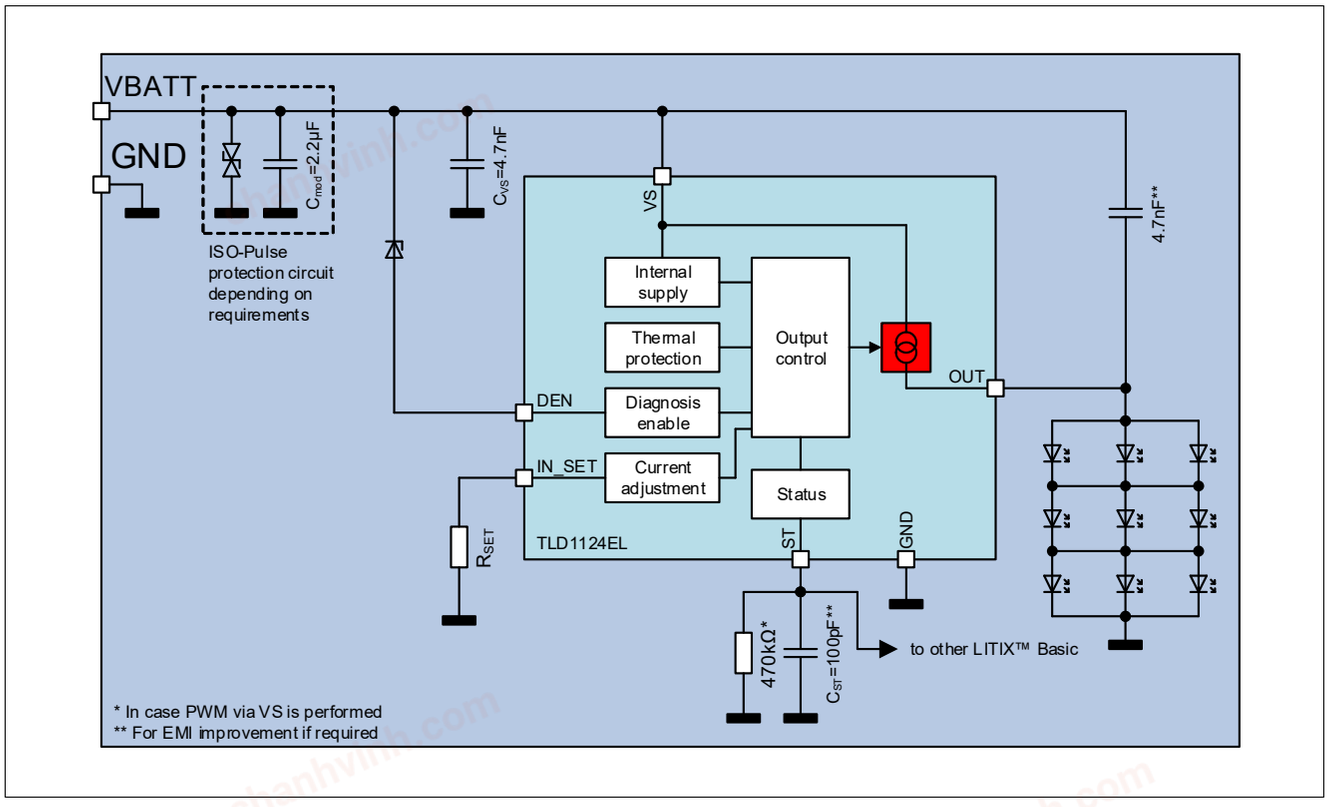
Package	PG-SSOP-14
Marking	TLD1124



1 Overview

Applications

- Exterior LED lighting applications such as tail/brake light, turn indicator, position light, side marker,...
- Interior LED lighting applications such as ambient lighting, interior illumination and dash board lighting.



Application Diagram with TLD1124EL

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Overview

Basic Features

- 1 Channel device with integrated output stage (current source), optimized to drive LEDs with output current up to 360 mA
- Low current consumption
- PWM-operation supported via VS-pin
- Output current adjustable via external low power resistor and possibility to connect PTC resistor for LED protection during over temperature conditions
- Reverse polarity protection and overload protection
- Undervoltage detection
- Open load and short circuit to GND diagnosis
- Wide temperature range: -40°C < T_j < 150°C
- PG-SSOP-14 package with exposed heatslug

Description

The LITIX™ Basic TLD1124EL is a one channel high side driver IC with integrated output stage. It is designed to control LEDs with a current up to 360 mA. In typical automotive applications the device is capable to drive i.e. 3 red LEDs with a current up to 180 mA, which is limited by thermal cooling aspects. The output current is controlled practically independent of load and supply voltage changes.

Table 1 Product Summary

Parameter	Symbol	Value
Operating voltage range	$V_{S(nom)}$	5.5 V ... 40 V
Maximum voltage	$V_{S(max)}$ $V_{OUT(max)}$	40 V
Nominal output (load) current	$I_{OUT(nom)}$	180 mA when using a supply voltage range of 8 V - 18 V (e.g. Automotive car battery). Currents up to $I_{OUT(max)}$ possible in applications with low thermal resistance R_{thJA}
Maximum output (load) current	$I_{OUT(max)}$	360 mA; depending on thermal resistance R_{thJA}
Output current accuracy at R_{SET} = 12 kΩ	k_{LT}	2250 ± 7%

Protective Functions

- ESD protection
- Under voltage lock out
- Over Load protection
- Over Temperature protection
- Reverse Polarity protection

Diagnostic Functions

- Diagnosis enable function
- OL detection
- SC to Vs (indicated by OL diagnosis)
- SC to GND detection

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2 Block Diagram

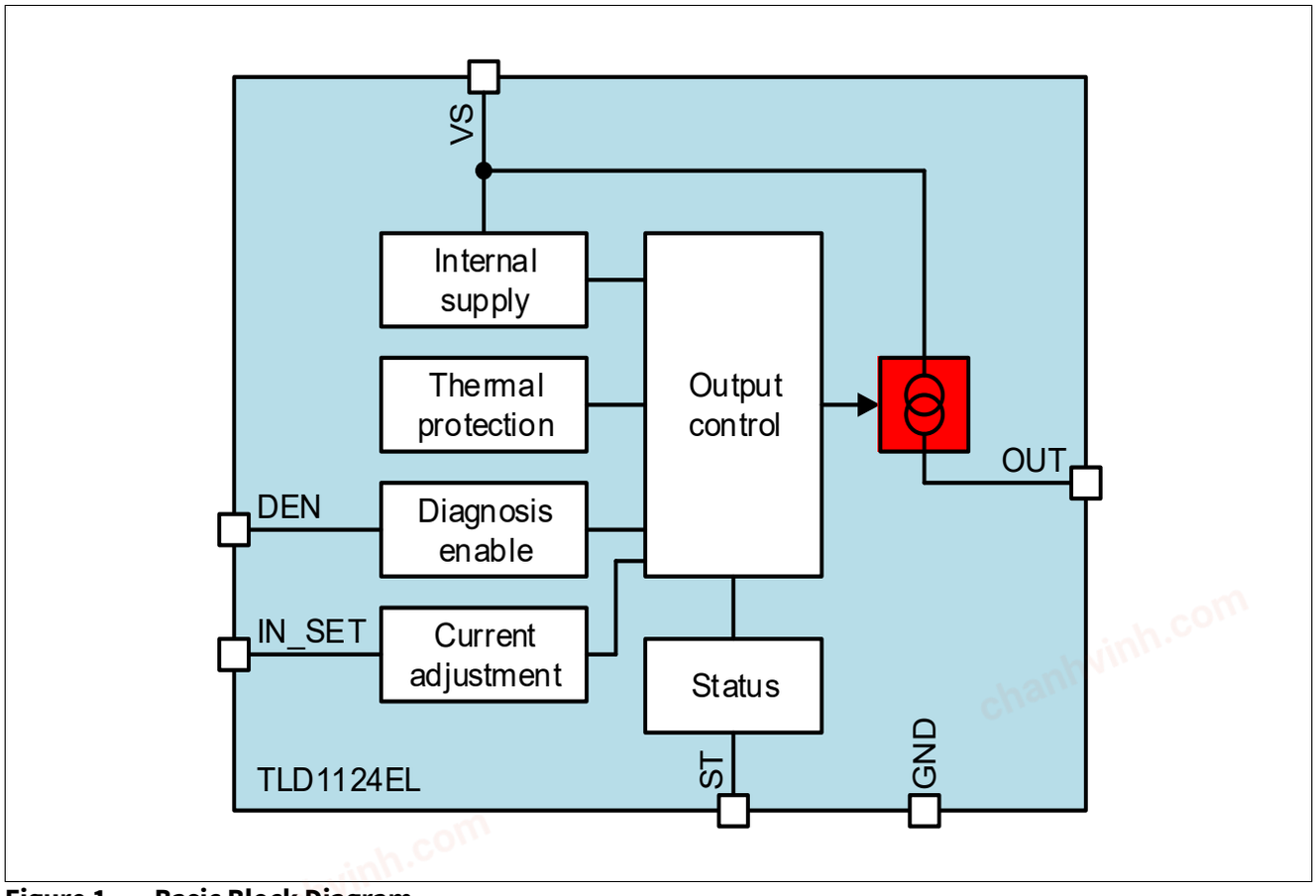

Figure 1 Basic Block Diagram

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3 Pin Configuration

3.1 Pin Assignment

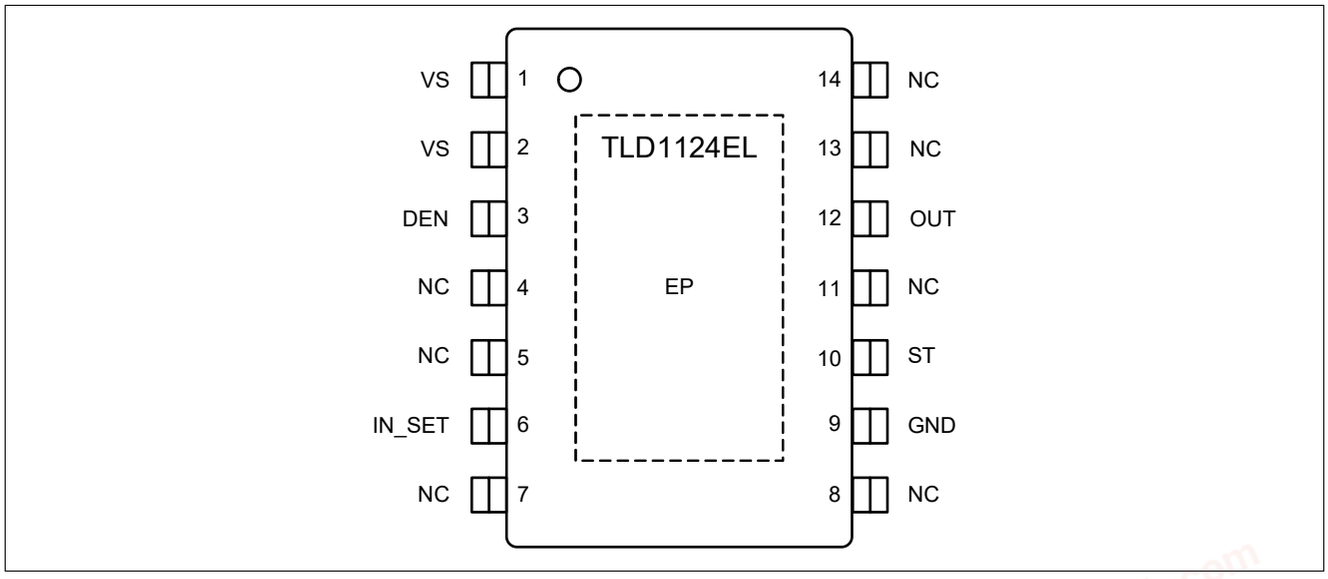

Figure 2 Pin Configuration

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3.2 Pin Definitions and Functions

Pin	Symbol	Input/ Output	Function
1, 2	VS	–	**Supply Voltage;** battery supply, connect a decoupling capacitor (100 nF - 1 µF) to GND
3	DEN	I	**Diagnosis enable pin**
4	NC	–	**Pin not connected**
5	NC	–	**Pin not connected**
6	IN_SET	I/O	**Input / SET pin;** Connect a low power resistor to adjust the output current
7	NC	–	**Pin not connected**
8	NC	–	**Pin not connected**
9	GND	–	[1] **Ground**
10	ST	I/O	**Status pin**
11	NC	–	**Pin not connected**
12	OUT	O	**Output**
13	NC	–	**Pin not connected**
14	NC	–	**Pin not connected**
Exposed Pad	GND	–	[1] **Exposed Pad;** connect to GND in application

1) Connect all GND-pins together.

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4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-16	40	V	–
4.1.2	Diagnosis enable voltage DEN	V_{DEN}	-16	40	V	–
4.1.3	Diagn. enable voltage DEN related to V_S	$V_{DEN(VS)}$	V_S - 40	V_S + 16	V	–
4.1.4	Diagn. enable voltage DEN related to V_{OUT} V_{DEN} - V_{OUT}	V_{DEN} - V_{OUT}	-16	40	V	–
4.1.5	Output voltage	V_{OUT}	-1	40	V	–
4.1.6	Power stage voltage $V_{PS} = V_S - V_{OUT}$	V_{PS}	-16	40	V	–
4.1.7	IN_SET voltage	V_{IN_SET}	-0.3	6	V	–
4.1.8	Status voltage	V_{ST}	-0.3	6	V	–
Currents						
4.1.9	IN_SET current	I_{IN_SET}	– –	2 8	mA	– Diagnosis output
4.1.10	Output current	I_{OUT}	–	390	mA	–
Temperatures						
4.1.11	Junction temperature	T_j	-40	150	°C	–
4.1.12	Storage temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.13	ESD resistivity to GND	V_{ESD}	-2	2	kV	Human Body Model (100 pF via 1.5 kΩ)[2]
4.1.14	ESD resistivity all pins to GND	V_{ESD}	-500	500	V	CDM[3]
4.1.15	ESD resistivity corner pins to GND	V_{ESD}	-750	750	V	CDM[3]

1) Not subject to production test, specified by design
2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001-2011
3) ESD susceptibility, Charged Device Model “CDM” according to JESD22-C101E

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

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4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.16	Supply voltage range for normal operation	$V_{S(nom)}$	5.5	40	V	–
4.2.17	Power on reset threshold	$V_{S(POR)}$	–	5	V	R_{SET} = 12 kΩ I_{OUT} = 80% $I_{OUT(nom)}$ V_{OUT} = 2.5 V
4.2.18	Junction temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	R_{thJC}	–	8	10	K/W	1) 2)
4.3.2	Junction to Ambient 1s0p board	R_{thJA1}				K/W	1) 3)
			–	61	–		T_a = 85 °C
			–	56	–		T_a = 135 °C
4.3.3	Junction to Ambient 2s2p board	R_{thJA2}				K/W	1) 4)
			–	45	–		T_a = 85 °C
			–	43	–		T_a = 135 °C

1) Not subject to production test, specified by design. Based on simulation results.
2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed Pad are fixed to ambient temperature). T_a = 85°C, Total power dissipation 1.5 W.
3) The R_{thJA} values are according to Jedec JESD51-3 at natural convection on 1s0p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 70 µm Cu, 300 mm^2 cooling area. Total power dissipation 1.5 W distributed statically and homogenously over power stage.
4) The R_{thJA} values are according to Jedec JESD51-5,-7 at natural convection on 2s2p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 2 inner copper layers (outside 2 x 70 µm Cu, inner 2 x 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5 W distributed statically and homogenously over power stage.

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5 DEN Pin

The DEN pin is a single function pin:

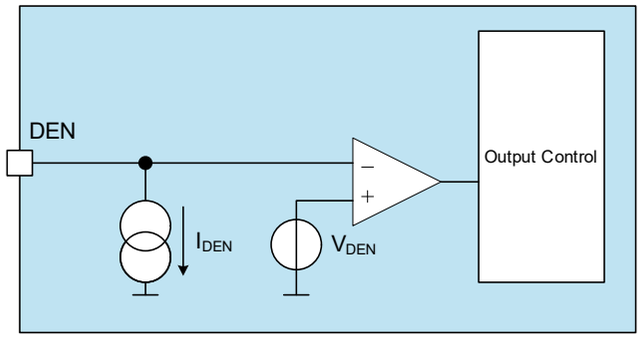

Figure 3 Block Diagram DEN pin

This pin is used to activate or deactivate the device internal diagnosis functions. The diagnostic functions are described in **Chapter 6.2**, **Chapter 7** and **Chapter 8**. The diagnosis is activated, if the voltage applied at the DEN pin V_{DEN} is higher than $V_{DEN(act)}$. The diagnosis is disabled for voltages below $V_{DEN(dis)}$.

A possibility to use the DEN pin is via a Zener diode, which is connected between VS and DEN pin. A circuit example is shown in the application information section **Chapter 10**.

The diagnosis is activated, if the following condition is fulfilled:

$$V_S \geq V_{DEN(act)} + V_{ZD} \quad (1)$$

The current consumption on the DEN pin has to be considered for the total device current consumption. The current is specified in **Pos. 5.1.8**. The typical current consumption $I_{DEN(H)}$ as a function of the supply voltage V_S for a Zener diode voltage of V_{ZD} = 6 V is shown in the following diagram.

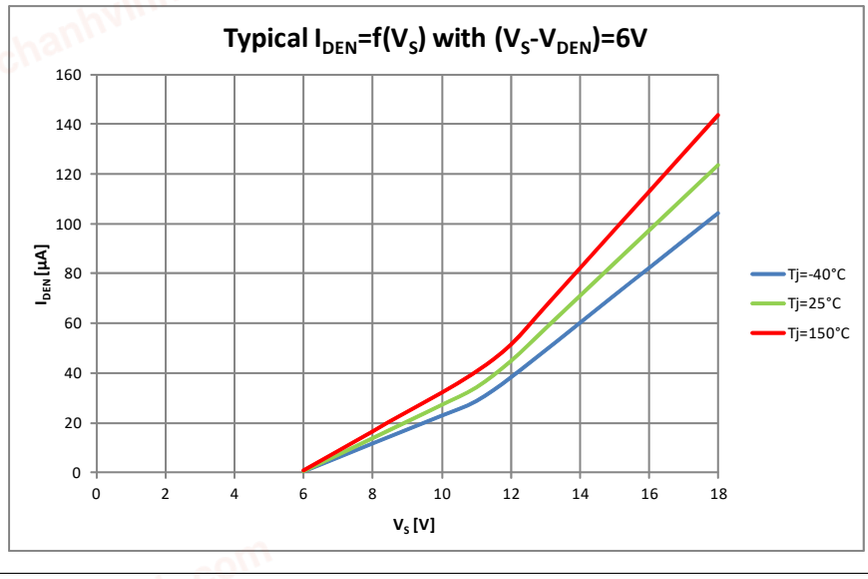

Figure 4 Typical $I_{DEN(H)}$ current for a Zener diode voltage of 6 V

The device and channel turn on is independent of the V_{DEN}-voltage. After applying a supply voltage the device is activated after the power on reset time t_{POR}.

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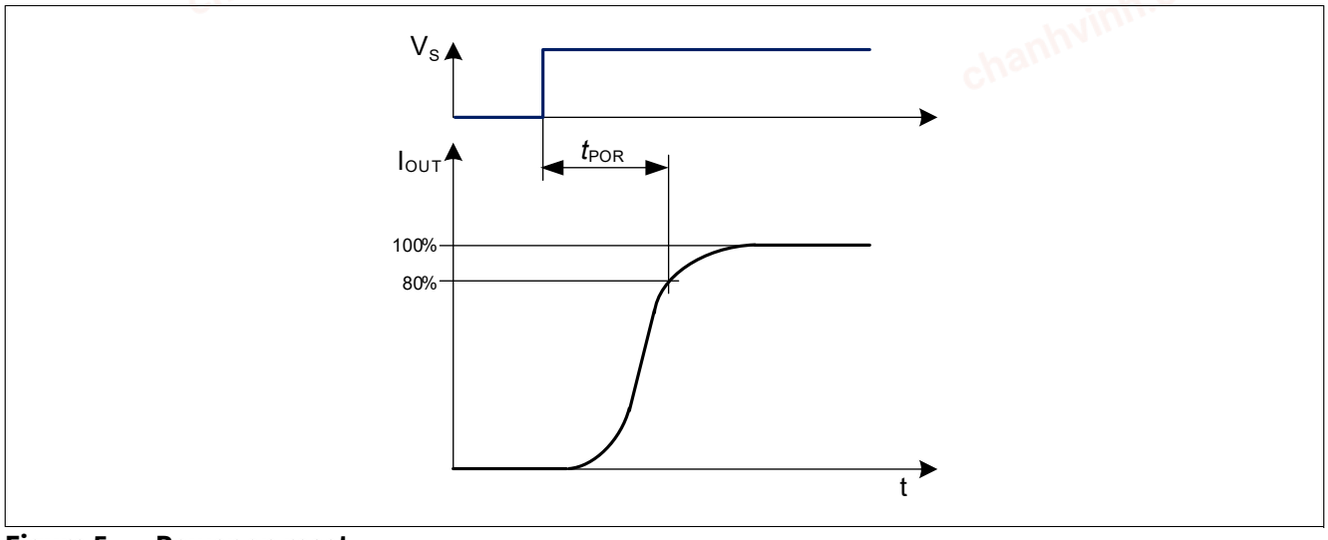

Figure 5 Power on reset

The DEN voltage V_{DEN} does not influence the disable function via the ST pin. If $V_{DEN} < V_{DEN(dis)}$ the device can still be disabled via the ST pin, if $V_{ST} > V_{ST(H)}$. For details, please refer to **Chapter 7.3**.

5.1 Electrical Characteristics Internal Supply / DEN Pin

Electrical Characteristics Internal Supply / DEN pin

Unless otherwise specified: V_S = 5.5 V to 40 V, T_j = -40°C to +150°C, R_{SET} = 12 kΩ all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Current consumption, active mode	$I_{S(on)}$	–	–	1.9	mA	[1] I_{IN_SET} = 0 µA T_j < 105 °C V_S = 18 V V_{OUT} = 3.6V
5.1.2	Current consumption, device disabled via ST	$I_{S(dis,ST)}$	–	–	1.7	mA	[1] V_S = 18 V T_j < 105 °C V_{ST} = 5 V
5.1.3	Current consumption, device disabled via IN_SET	$I_{S(dis,IN_SET)}$	–	–	1.7	mA	[1] V_S = 18 V T_j < 105 °C V_{IN_SET} = 5 V
5.1.4	Current consumption, active mode in fault detection condition with ST-pin unconnected	$I_{S(fault,STu)}$	–	–	2.1	mA	[1] V_S = 18 V T_j < 105 °C R_{SET} = 12 kΩ V_{OUT} = 18 V or 0 V

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DEN Pin

Electrical Characteristics Internal Supply / DEN pin (cont'd)

Unless otherwise specified: V_S = 5.5 V to 40 V, T_j = -40°C to +150°C, R_{SET} = 12 kΩ all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.5	Current consumption, active mode in fault detection condition with ST-pin connected to GND	$I_{S(fault,STG)}$	–	–	6.2	mA	[1] V_S = 18 V T_j < 105 °C R_{SET} = 12 kΩ V_{OUT} = 18 V or 0 V V_{ST} = 0 V
5.1.6	Power-on reset delay time [2]	t_{POR}	–	–	25	µs	[3] V_S = 0 →13.5 V $V_{OUT(nom)}$ = 3.6 ± 0.3V I_{OUT} = 80% $I_{OUT(nom)}$
5.1.7	Required supply voltage for current control	$V_{S(CC)}$	–	–	5.5	V	V_{OUT} = 3.6 V I_{OUT} ≥ 90% $I_{OUT(nom)}$
5.1.8	DEN high input current	$I_{DEN(H)}$	 – – – –	 – – – –	 0.1 0.1 0.2 0.4	mA	T_j < 105 °C V_S = 13.5 V, V_{DEN} = 5.5 V V_S = 18 V, V_{DEN} = 5.5 V V_S = 18 V, V_{DEN} = 12 V V_S = V_{DEN} = 18 V
5.1.9	DEN activation threshold (diagnosis enabled above $V_{DEN(act)}$)	$V_{DEN(act)}$	2.45	–	3.2	V	V_S = 8...18 V
5.1.10	DEN deactivation threshold (diagnosis disabled below $V_{DEN(dis)}$)	$V_{DEN(dis)}$	1.5	–	2.3	V	V_S = 8...18 V

1) The total device current consumption is the sum of the currents I_S and $I_{DEN(H)}$, please refer to **Pos. 5.1.8**
2) See also **Figure 5**
3) Not subject to production test, specified by design

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6 IN_SET Pin

The IN_SET pin is a multiple function pin for output current definition, input and diagnostics:

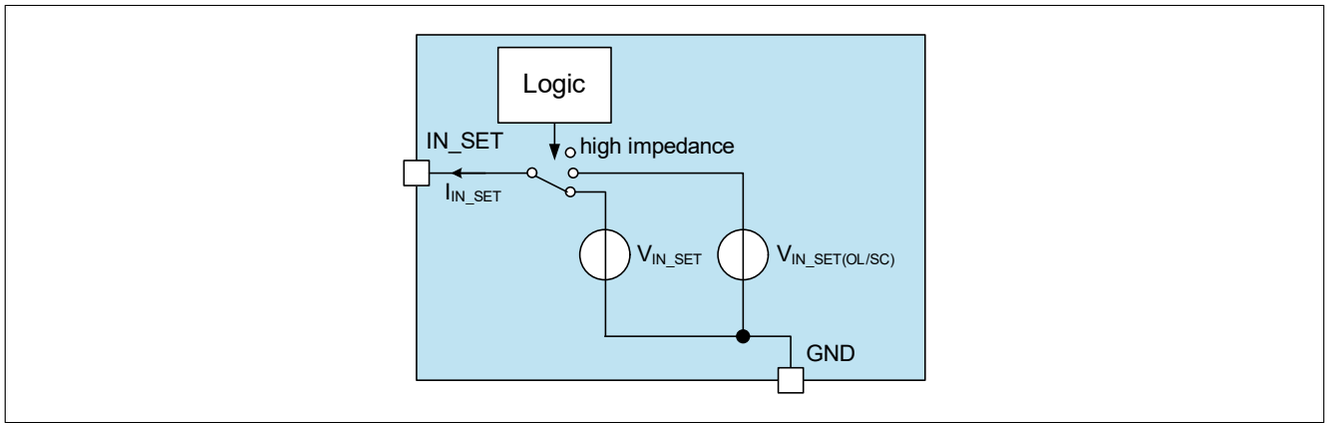

Figure 6 Block Diagram IN_SET pin

6.1 Output Current Adjustment via RSET

The current adjustment can be done by placing a low power resistor (R_{SET}) at the IN_SET pin to ground. The dimensioning of the resistor can be done using the formula below:

$$R_{SET} = \frac{k}{I_{OUT}} \quad (2)$$

The gain factor k (R_{SET} * output current) is specified in **Pos. 9.2.4** and **Pos. 9.2.5**. The current through the R_{SET} is defined by the resistor itself and the reference voltage $V_{IN_SET(ref)}$, which is applied to the IN_SET during supplied device.

6.2 Smart Input Pin

The IN_SET pin can be connected via R_{SET} to the open-drain output of a µC or to an external NMOS transistor as described in **Figure 7** This signal can be used to turn off the output stage of the IC. A minimum IN_SET current of $I_{IN_SET(act)}$ is required to turn on the output stage. This feature is implemented to prevent glimming of LEDs caused by leakage currents on the IN_SET pin, see **Figure 10** for details. In addition, the IN_SET pin offers the diagnostic feedback information, if the status pin is connected to GND and $V_{DEN} > V_{DEN(act)}$ (refer to **Chapter 5**). Another diagnostic possibility is shown in **Figure 8**, where the diagnosis information is provided via the ST pin (refer to **Chapter 7** and **Chapter 8**) to a micro controller In case of a fault event with the ST pin connected to GND the IN_SET voltage is increased to $V_{IN_SET(OL/SC)}$ **Pos. 8.3.2**. Therefore, the device has two voltage domains at the IN_SET-pin, which is shown in **Figure 11**.

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IN_SET Pin

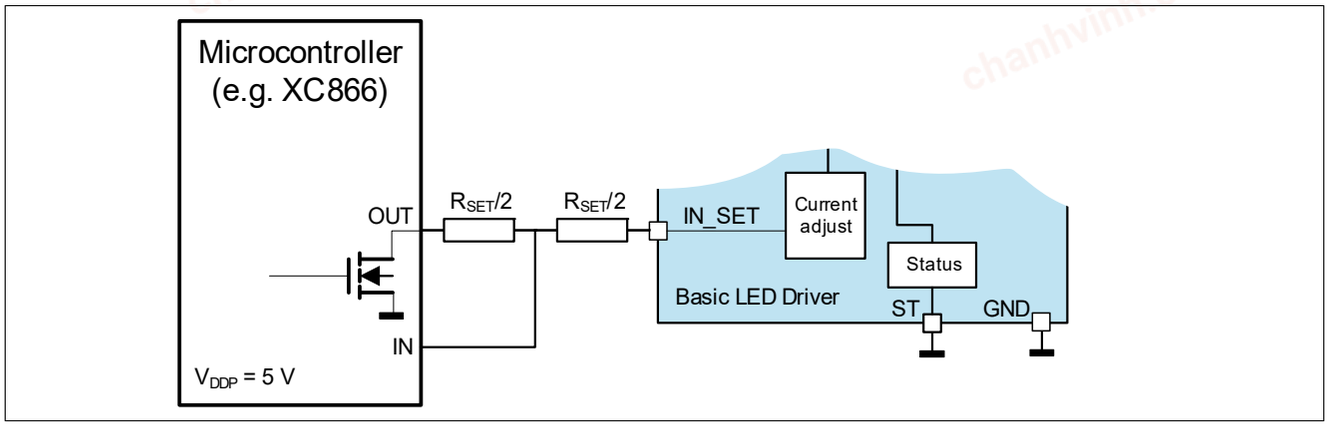

Figure 7 Schematics IN_SET interface to µC, diagnosis via IN_SET pin

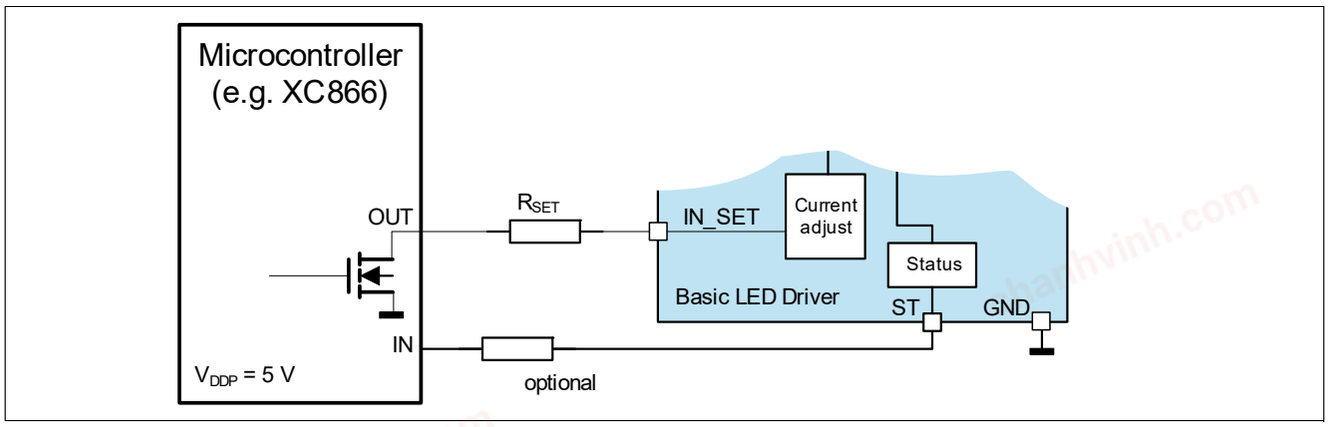

Figure 8 Schematics IN_SET interface to µC, diagnosis via ST pin

The resulting switching times are shown in **Figure 9**:

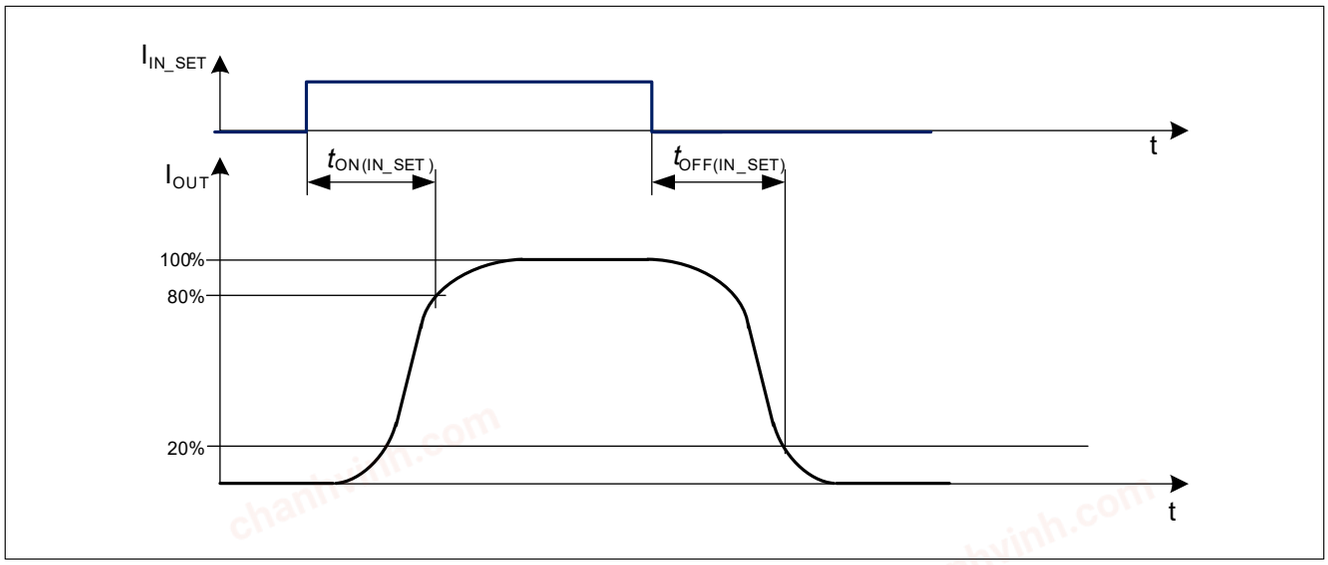

Figure 9 Switching times via IN_SET

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IN_SET Pin

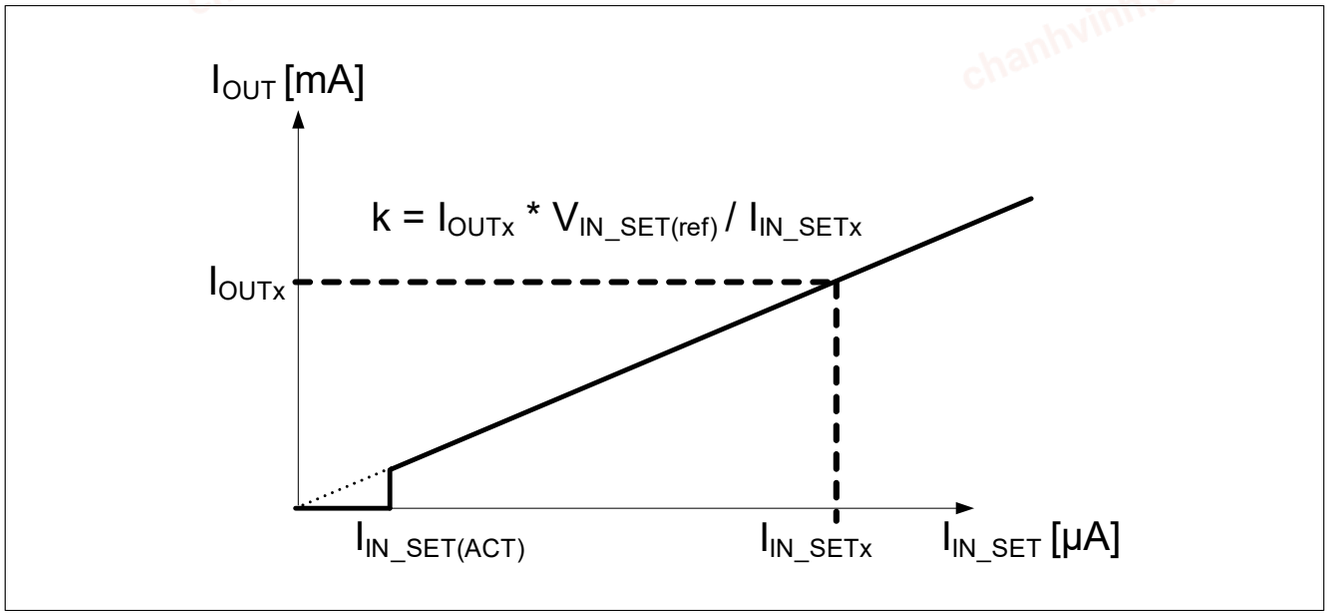

Figure 10 I_{OUT} versus I_{INSET}

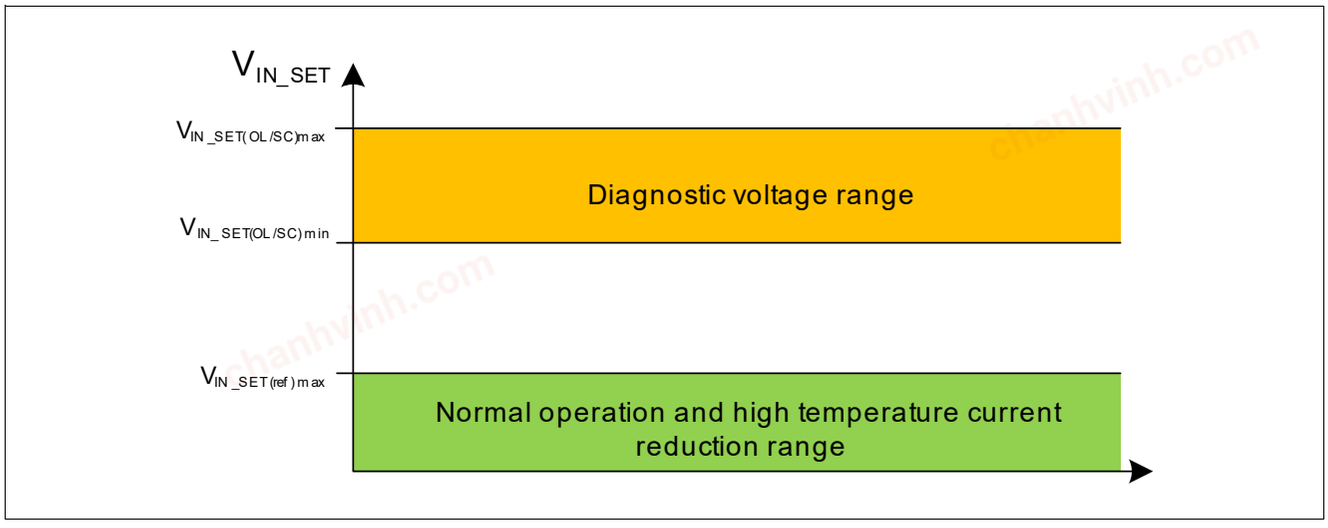

Figure 11 Voltage domains for IN_SET pin, if ST pin is connected to GND

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7 ST Pin

The ST pin is a multiple function pin.

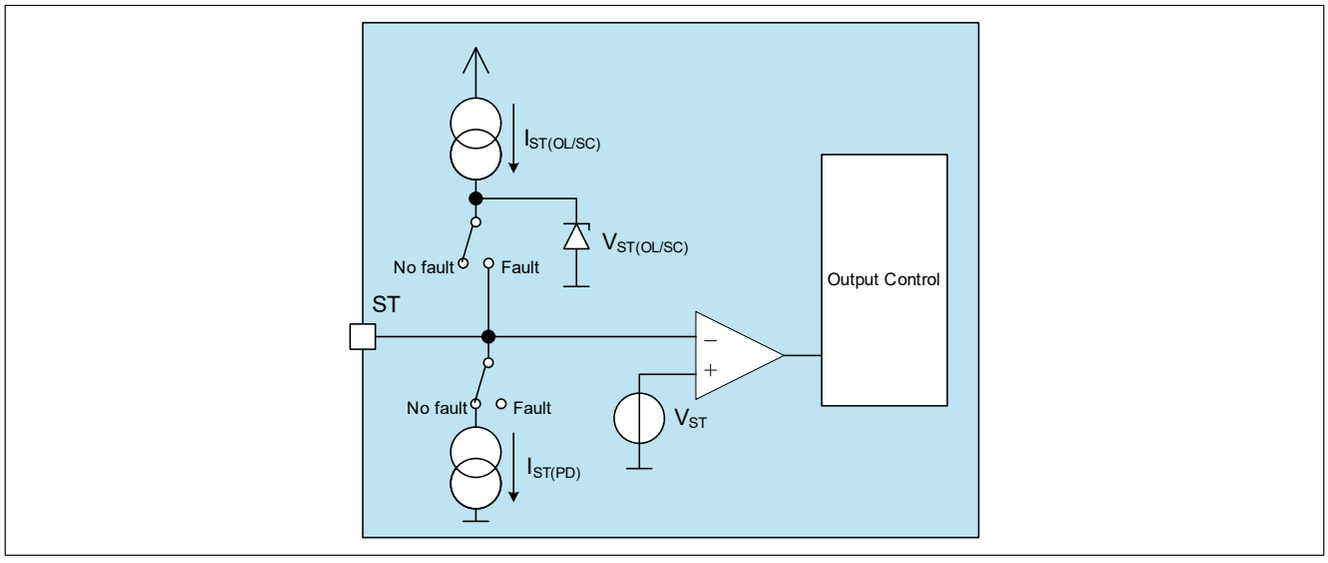

Figure 12 Block Diagram ST pin

7.1 Diagnosis Selector

If the voltage at the DEN pin V_{DEN} is higher than $V_{DEN(act)}$, the diagnosis is activated. For details, please refer to **Chapter 5**. If the status pin is unconnected or connected to GND via a high ohmic resistor (V_{ST} to be below $V_{ST(L)}$), the ST pin acts as diagnosis output pin. In normal operation (device is activated) the ST pin is pulled to GND via the internal pull down current $I_{ST(PD)}$. In case of an open load or short circuit to GND condition the ST pin is switched to $V_{ST(OL/SC)}$ after the open load or short circuit detection filter time (**Pos. 8.3.9**, **Pos. 8.3.12**).

If the device is operated in PWM operation via the VS pin the ST pin should be connected to GND via a high ohmic resistor (e.g. 470 kΩ) to ensure proper device behavior during fast rising VS slope.

If the ST pin is shorted to GND the diagnostic feedback is performed via the IN_SET-pin, which is shown in **Chapter 6.2** and **Chapter 8**.

7.2 Diagnosis Output

If the status pin is unconnected or connected to GND via a high ohmic resistor (V_{ST} to be below $V_{ST(L)}$), it acts as a diagnostic output, if the voltage at the DEN pin is above $V_{DEN(act)}$. In case of a fault condition the ST pin rises its voltage to $V_{ST(OL/SC)}$ (**Pos. 8.3.7**). Details are shown in **Chapter 8**.

7.3 Disable Input

If an external voltage higher than $V_{ST(H)}$ (**Pos. 8.3.5**) is applied to the ST pin, the device is switched off. This function is working independently of the voltage at the DEN pin. Even if the diagnosis is disabled via $V_{DEN} < V_{DEN(dis)}$ the disable function of the ST pin is working. This function is used for applications, where multiple drivers should be used for one light function. It is possible to combine the drivers' fault diagnosis via the ST pins. If a single LED chain fails, the entire light function is switched off. In this scenario e.g. the diagnostic circuit on the body control module can easily distinguish between the two cases (normal load or load fault), because nearly no current is flowing into the LED module during the fault scenario - the drivers consume a current of $I_{S(fault,STu)}$ (**Pos. 5.1.4**) or $I_{S(dis,ST)}$ (**Pos. 5.1.2**).

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ST Pin

As soon as one LED chain fails, the ST-pin of this device is switched to $V_{ST(OL/SC)}$. The other devices used for the same light function can be connected together via the ST pins. This leads to a switch off of all devices connected together. Application examples are shown in **Chapter 10**.

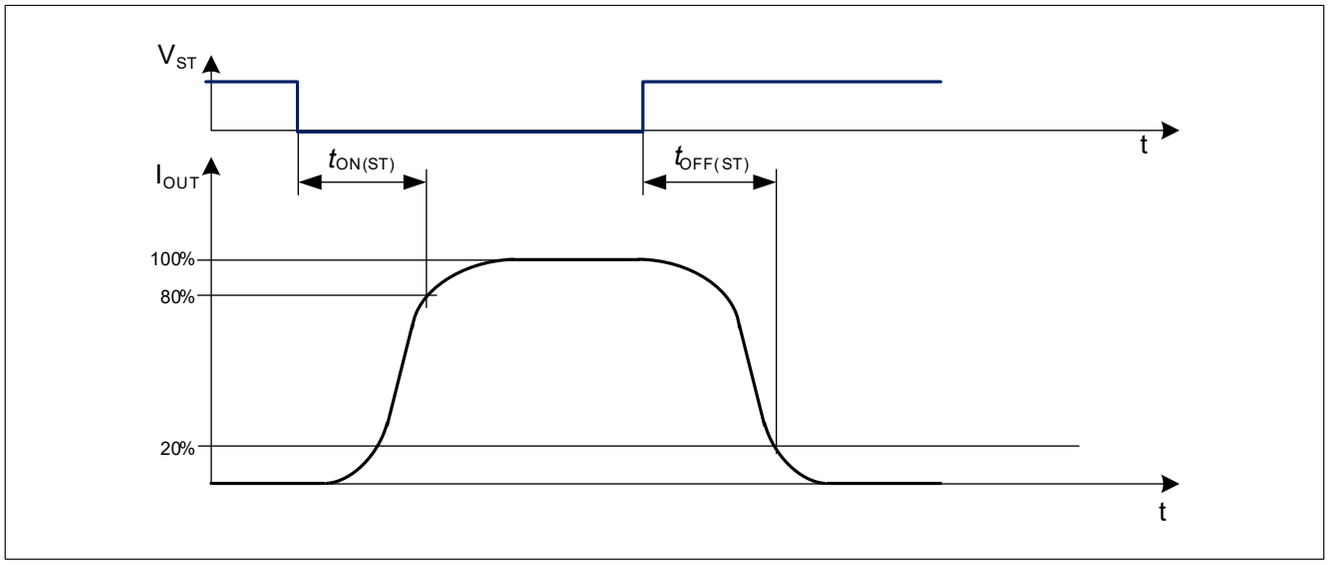

Figure 13 Switching times via ST Pin

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8 Load Diagnosis

The diagnosis function is enabled, if the voltage at the DEN pin V_{DEN} is above $V_{DEN(act)}$ as described in **Chapter 5**.

8.1 Open Load

An open load diagnosis feature is integrated in the TLD1124EL driver IC. If there is an open load on the output, the output is turned off. The potential on the IN_SET pin rises up to $V_{IN_SET(OL/SC)}$. This high voltage can be used as input signal for an µC as shown in **Figure 8**. The open load status is not latched, as soon as the open load condition is no longer present, the output stage will be turned on again. An open load condition is detected, if the voltage drop over the output stage V_{PS} is below the threshold according **Pos. 8.3.10** and a filter time of t_{OL} is passed.

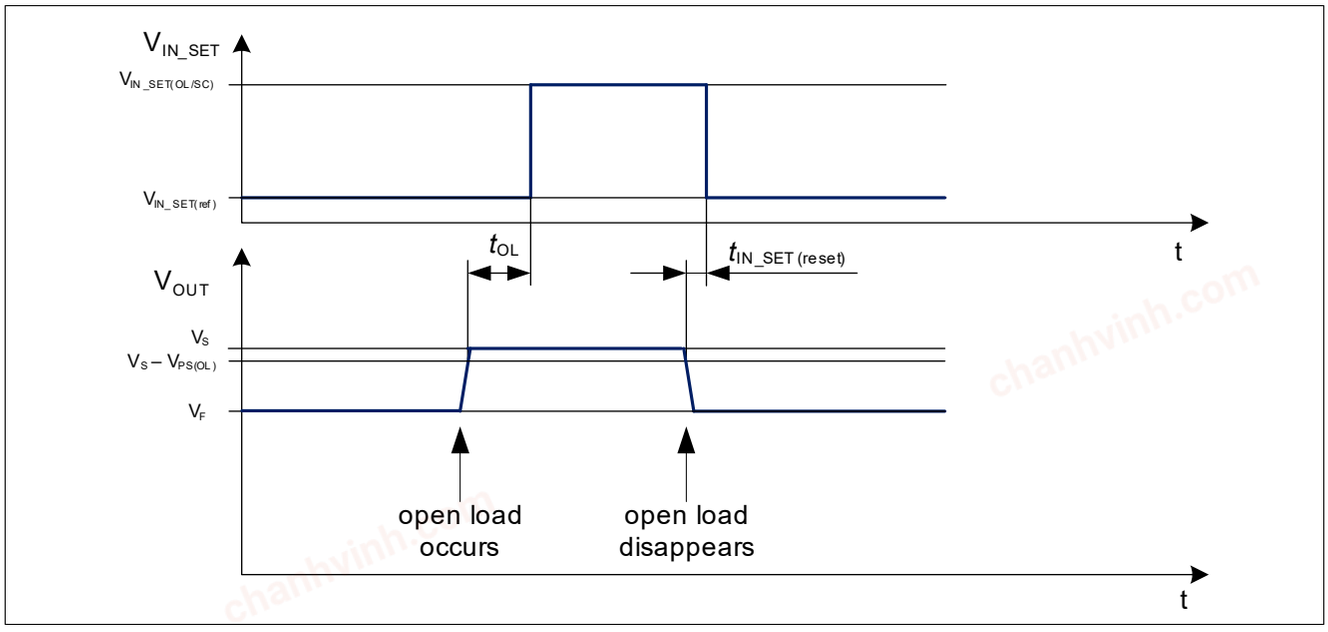

Figure 14 IN_SET behavior during open load condition with ST pin connected to GND and $V_{DEN} > V_{DEN(act)}$

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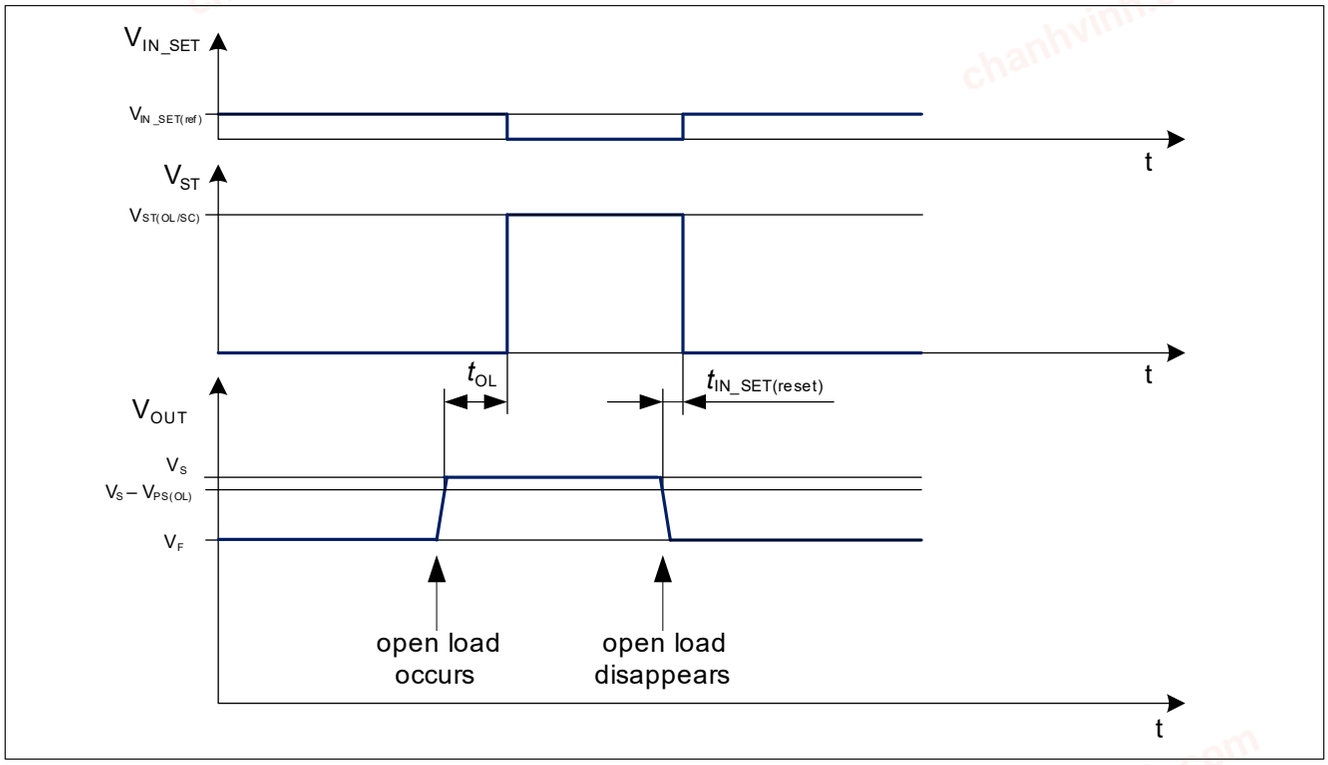

Figure 15 IN_SET and ST behavior during open load condition (ST unconnected) and $V_{DEN} > V_{DEN(act)}$

8.2 Short Circuit to GND detection

The TLD1124EL has an integrated SC to GND detection. If the output stage is turned on and the voltage at the output falls below $V_{OUT(SC)}$ the potential on the IN_SET pin is increased up to $V_{IN_SET(OL/SC)}$ after t_{SC}, if the ST pin is connected to GND. If the ST is open or connected to GND via a high ohmic resistor the fault is indicated on the ST pin according to **Chapter 7** after t_{SC}. More details are shown in **Figure 17**. This condition is not latched. For detecting a normal condition after a short circuit detection an output current according to $I_{OUT(SC)}$ is driven by the channel.

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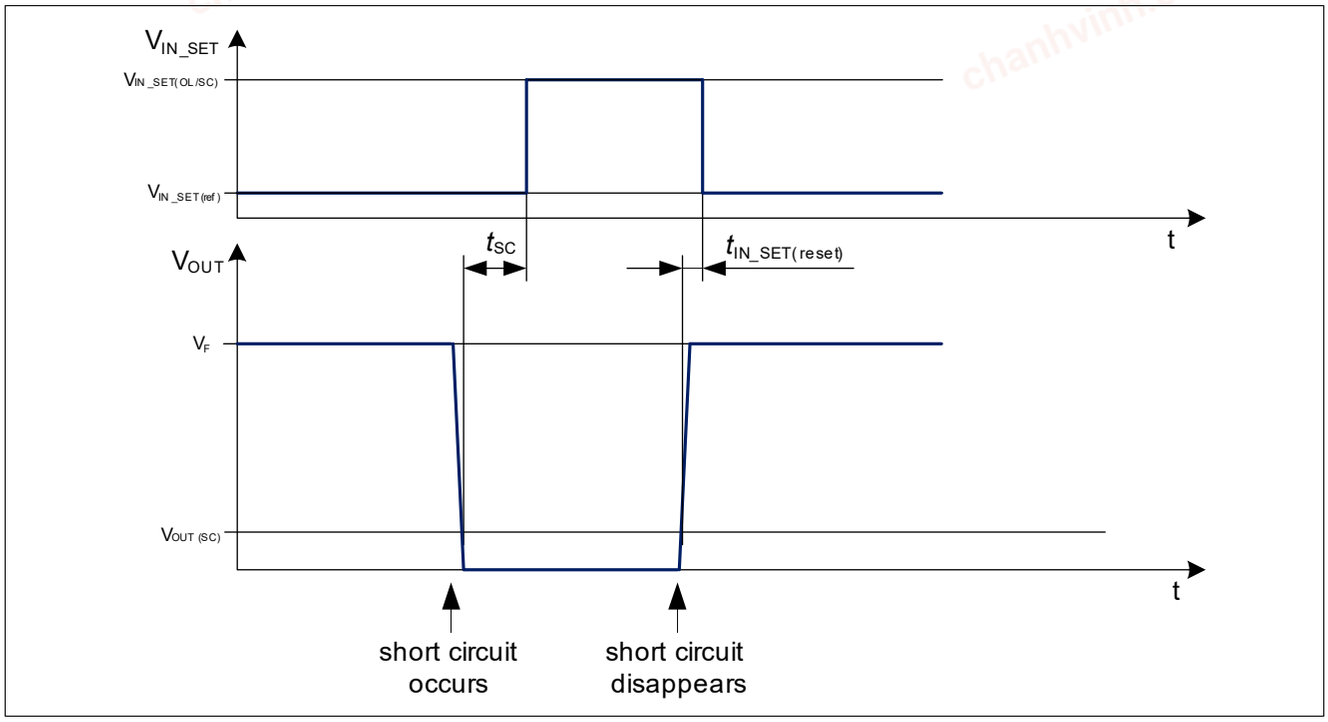

Figure 16 IN_SET behavior during short circuit to GND condition with ST connected to GND and V_{DEN} > $V_{DEN(act)}$

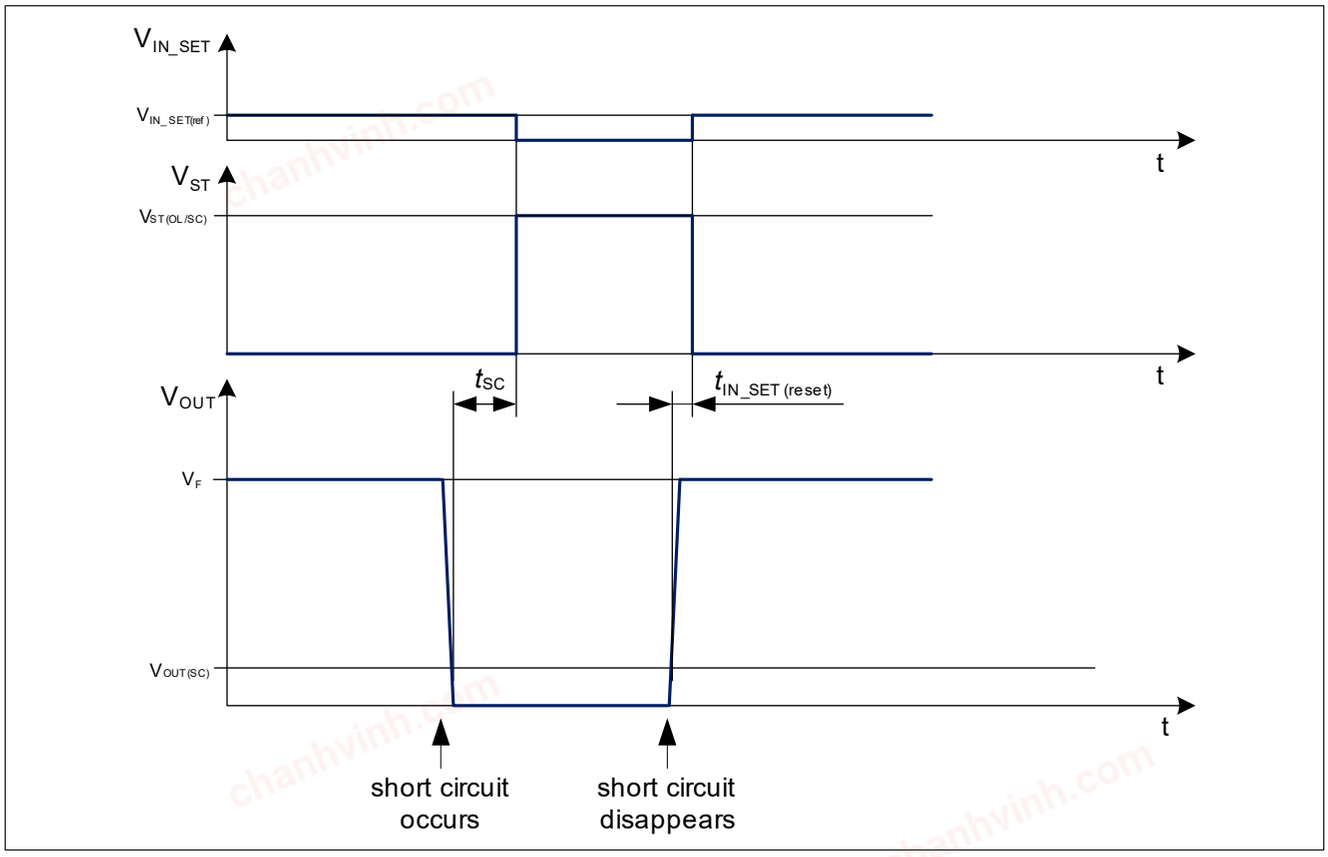

Figure 17 IN_SET and ST behavior during short circuit to GND condition (ST unconnected) and V_{DEN} > $V_{DEN(act)}$

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8.3 Electrical Characteristics IN_SET Pin and Load Diagnosis

Electrical Characteristics IN_SET pin and Load Diagnosis

Unless otherwise specified: V_S = 5.5 V to 40 V, T_j = -40°C to +150°C, R_{SET} = 12 kΩ, V_{DEN} = 5.5 V, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.3.1	IN_SET reference voltage	$V_{IN_SET(ref)}$	1.19	1.23	1.27	V	1) V_{OUT} = 3.6 V T_j = 25...115 °C
8.3.2	IN_SET open load/short circuit voltage	$V_{IN_SET(OL/SC)}$	4	–	5.5	V	1) V_S > 8 V T_j = 25...150 °C V_S = V_{OUT} (OL) or V_{OUTx} = 0 V (SC)
8.3.3	IN_SET open load/short circuit current	$I_{IN_SET(OL/SC)}$	1.5	–	7.4	mA	1) V_S > 8 V T_j = 25...150 °C V_{IN_SET} = 4 V V_S = V_{OUT} (OL) or V_{OUT} = 0 V (SC)
8.3.4	ST device turn on threshold (active low) in case of voltage applied from external (ST-pin acting as input)	$V_{ST(L)}$	0.8	–	–	V	–
8.3.5	ST device turn off threshold (active low) in case of voltage applied from external (ST-pin acting as input)	$V_{ST(H)}$	–	–	2.5	V	–
8.3.6	ST pull down current	$I_{ST(PD)}$	–	–	15	µA	V_{ST}= 0.8 V
8.3.7	ST open load/short circuit voltage (ST-pin acting as diagnosis output)	$V_{ST(OL/SC)}$	4	–	5.5	V	1) V_S > 8 V T_j = 25...150 °C R_{ST} = 470 kΩ V_S = V_{OUT} (OL) or V_{OUT} = 0 V (SC)
8.3.8	ST open load/short circuit current (ST-pin acting as diagnosis output)	$I_{ST(OL/SC)}$	100	–	220	µA	1) V_S > 8 V T_j = 25...150 °C V_{ST} = 2.5 V V_S = V_{OUT} (OL) or V_{OUT} = 0 V (SC)
8.3.9	OL detection filter time	t_{OL}	10	22	35	µs	1) V_S > 8 V
8.3.10	OL detection voltage $V_{PS(OL)} = V_S - V_{OUT}$	$V_{PS(OL)}$	0.2	–	0.4	V	V_S > 8 V
8.3.11	Short circuit to GND detection threshold	$V_{OUT(SC)}$	0.8	–	1.4	V	V_S > 8 V
8.3.12	SC detection filter time	t_{SC}	10	22	35	µs	1) V_S > 8 V

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Load Diagnosis

Electrical Characteristics IN_SET pin and Load Diagnosis (cont'd)

Unless otherwise specified: V_S = 5.5 V to 40 V, T_j = -40°C to +150°C, R_{SET} = 12 kΩ, V_{DEN} = 5.5 V, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.3.13	IN_SET diagnosis reset time	$t_{IN_SET(reset)}$	–	5	20	µs	[1] V_S > 8 V
8.3.14	SC detection current in case of unconnected ST-pin	$I_{OUT(SC,STu)}$	100	200	300	µA	V_S > 8 V V_{OUT} = 0 V
8.3.15	SC detection current in case of ST-pin shorted to GND	$I_{OUT(SC,STG)}$	0.1	2	4.75	mA	V_S > 8 V V_{OUT} = 0 V V_{ST} = 0 V
8.3.16	IN_SET activation current without turn on of output stage	$I_{IN_SET(act)}$	2	–	15	µA	See **Figure 10**

1) Not subject to production test, specified by design

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9 Power Stage

The output stage is realized as high side current source with a current of 360 mA. During off state the leakage current at the output stage is minimized in order to prevent a slightly glowing LED.

The maximum current of the channel is limited by the power dissipation and used PCB cooling areas (which results in the applications R_{thJA}).

For an operating current control loop the supply and output voltages according to the following parameters have to be considered:

- Required supply voltage for current control $V_{S(CC)}$, **Pos. 5.1.7**
- Voltage drop over output stage during current control $V_{PS(CC)}$, **Pos. 9.2.6**
- Required output voltage for current control $V_{OUT(CC)}$, **Pos. 9.2.7**

9.1 Protection

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

9.1.1 Over Load Behavior

An over load detection circuit is integrated in the LITIX™ Basic IC. It is realized by a temperature monitoring of the output stage (OUT).

As soon as the junction temperature exceeds the current reduction temperature threshold $T_{j(CRT)}$ the output current will be reduced by the device by reducing the IN_SET reference voltage $V_{IN_SET(ref)}$. This feature avoids LED’s flickering during static output overload conditions. Furthermore, it protects LEDs against over temperature, which are mounted thermally close to the device. If the device temperature still increases, the output current decreases close to 0 A. As soon as the device cools down the output current rises again.

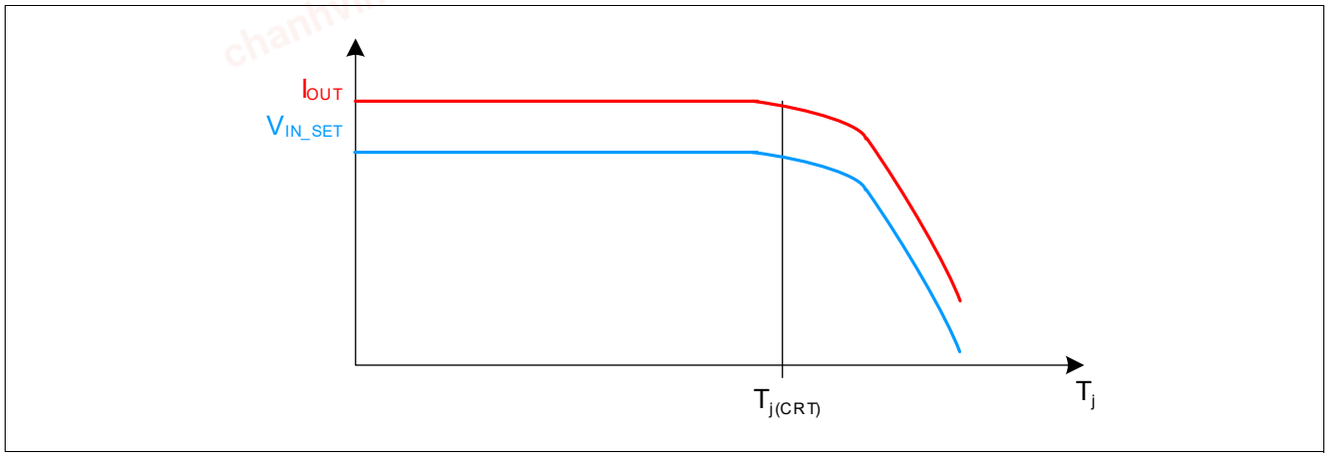

Figure 18 Output current reduction at high temperature

*Note: This high temperature output current reduction is realized by reducing the IN_SET reference voltage voltage (**Pos. 8.3.1**). In case of very high power loss applied to the device and very high junction temperature the output current may drop down to I_{OUT} = 0 mA, after a slight cooling down the current increases again.*

9.1.2 Reverse Battery Protection

The TLD1124EL has an integrated reverse battery protection feature. This feature protects the driver IC itself, but also connected LEDs. The output reverse current is limited to $I_{OUTx(rev)}$ by the reverse battery protection.

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Note: Due to the reverse battery protection a reverse protection diode for the light module may be obsolete. In case of high ISO-pulse requirements and only minor protecting components like capacitors a reverse protection diode may be reasonable. The external protection circuit needs to be verified in the application.

9.2 Electrical Characteristics Power Stage

Electrical Characteristics Power Stage

Unless otherwise specified: V_S = 5.5 V to 18 V, T_j = -40°C to +150°C, V_{OUT} = 3.6 V, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.2.1	Output leakage current	$I_{OUT(leak)}$	 – –	 – –	 21 9	µA	I_{IN_SET} = 0 µA V_{OUT} = 2.5 V T_j = 150 °C 1) T_j = 85 °C
9.2.2	Output leakage current in boost over battery setup	$-I_{OUT(leak,B2B)}$	–	–	150	µA	1) I_{IN_SET} = 0 µA V_{OUT} = V_S = 40 V
9.2.3	Reverse output current	$-I_{OUT(rev)}$	–	–	3	µA	1) V_S = -16 V Output load: LED with break down voltage < -0.6 V
9.2.4	Output current accuracy limited temperature range	k_{LT}	 2092 1935	 2250 2250	 2408 2565		1) T_j = 25...115 °C V_S = 8...18 V V_{PS} = 2 V R_{SET} = 6...12 kΩ R_{SET} = 30 kΩ
9.2.5	Output current accuracy over temperature	k_{ALL}	 2092 1935	 2250 2250	 2408 2565		1) T_j = -40...115 °C V_S = 8...18 V V_{PS} = 2 V R_{SET} = 6...12 kΩ R_{SET} = 30 kΩ
9.2.6	Voltage drop over power stage during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	0.75	–	–	V	1) V_S = 13.5 V R_{SET} = 12 kΩ I_{OUT} ≥ 90% of ($k_{LT(typ)}/R_{SET}$)
9.2.7	Required output voltage for current control	$V_{OUT(CC)}$	2.3	–	–	V	1) V_S = 13.5 V R_{SET} = 12 kΩ I_{OUT} ≥ 90% of ($k_{LT(typ)}/R_{SET}$)

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Electrical Characteristics Power Stage (cont'd)

Unless otherwise specified: V_S = 5.5 V to 18 V, T_j = -40°C to +150°C, V_{OUT} = 3.6 V, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.2.8	Maximum output current	$I_{OUT(max)}$	360	–	–	mA	R_{SET} = 4.7 kΩ The maximum output current is limited by the thermal conditions. Please refer to **Pos. 4.3.1** - **Pos. 4.3.3**
9.2.9	ST turn on time	$t_{ON(ST)}$	–	–	15	µs	[2] V_S = 13.5 V R_{SET} = 12 kΩ ST → L I_{OUT} = 80% of ($k_{LT(typ)}/R_{SET}$)
9.2.10	ST turn off time	$t_{OFF(ST)}$	–	–	10	µs	[2] V_S = 13.5 V R_{SET} = 12 kΩ ST →H I_{OUT} = 20% of ($k_{LT(typ)}/R_{SET}$)
9.2.11	IN_SET turn on time	$t_{ON(IN_SET)}$	–	–	15	µs	V_S = 13.5 V I_{IN_SET} = 0 → 100 µA I_{OUT} = 80% of ($k_{LT(typ)}/R_{SET}$)
9.2.12	IN_SET turn off time	$t_{OFF(IN_SET)}$	–	–	10	µs	V_S = 13.5 V I_{IN_SET} = 100 → 0 µA I_{OUT} = 20% of ($k_{LT(typ)}/R_{SET}$)
9.2.13	Current reduction temperature threshold	$T_{j(CRT)}$	–	140	–	°C	[1] I_{OUT} = 95% of ($k_{LT(typ)}/R_{SET}$)
9.2.14	Output current during current reduction at high temperature	$I_{OUT(CRT)}$	85% of ($k_{LT(typ)}/R_{SET}$)	–	–	A	[1] R_{SET} = 12 kΩ T_j = 150 °C

1) Not subject to production test, specified by design

2) see also **Figure 13**

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10 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

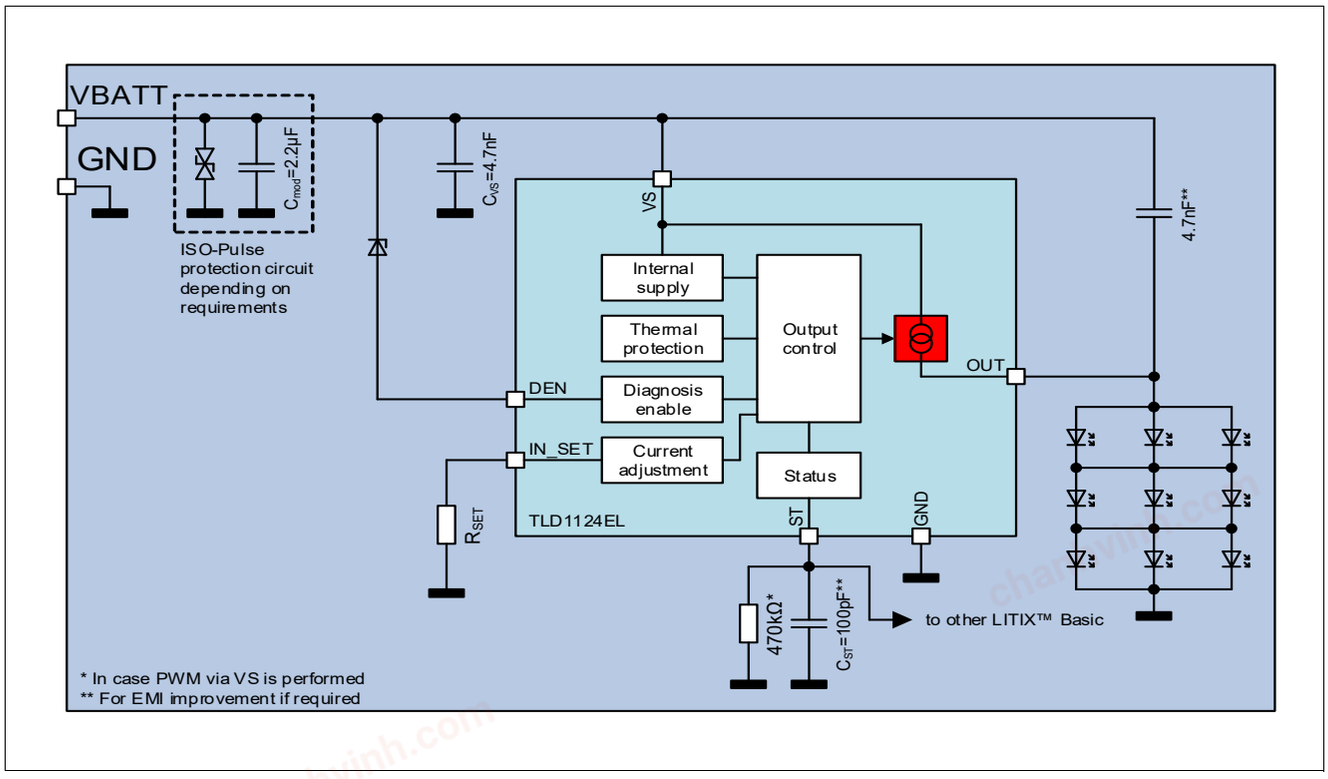

Figure 19 Application Diagram

Note: This is a very simplified example of an application circuit. In case of high ISO-pulse requirements a reverse protection diode may be used for LED protection. The function must be verified in the real application.

10.1 Further Application Information

- For further information you may contact **http://www.infineon.com/**

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11 Package Outlines

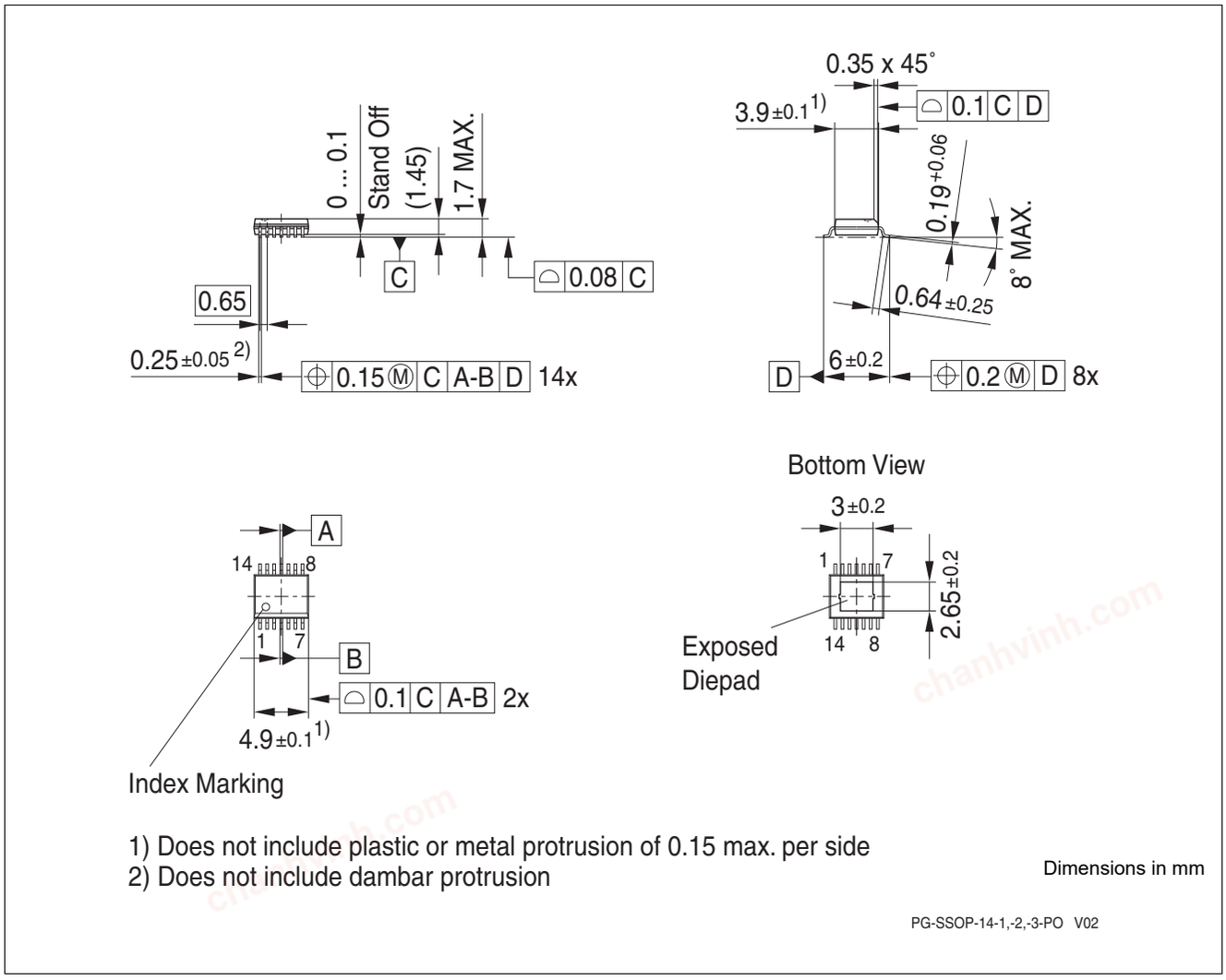

Figure 20 PG-SSOP-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

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12 Revision History

Revision	Date	Changes
1.0	2013-08-08	Inital revision of data sheet
1.1	2015-03-19	Updated parameters K_{LT} and K_{ALL} in the chapter Power Stage
1.2	2018-04-26	Updated to latest template
1.2	2018-04-26	Updated application drawing
1.2	2018-04-26	Updated package marking
1.2	2018-04-26	Updated package figure
1.21	2021-07-05	Corrected cross references in **Chapter 5.1** Footnote[2)]

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