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TDM3885 IPOL

4 A IPOL Synchronous Buck Voltage Regulator with Integrated Inductor

Features

- Optimized Module with inductor included
- Micro Sized 3.1mm x 3.8mm x 2.3mm
- Continuous 4A Load Capability
- Single Input Voltage Range (4.7V to 14V)
- 600kHz Switching Frequency
- 10uA Supply Current at Shutdown
- Enhanced Stability IPOL Engine Stable with Ceramic Capacitors and no External Compensation
- Enhanced Light Load Efficiency with Reduced Switching Frequency and Diode Emulation
- Forced Continuous Conduction Mode Option
- Thermally Compensated Internal Over-Current Protection
- Internal Soft-Start, Enable Input , PreBias Start Up, Thermal Shut Down, Power Good Output
- Precision Reference Voltage (0.5V+/-1.0%)
- Lead-free, Halogen-free and RoHS6 Compliant

Potential applications

- Server and Computing
- Storage and Applications
- Communications Infrastructure
- General DC-DC Converters.
- Distributed Point of Load Power Architectures.

Product validation

Qualified for Industrial Applications

Description

The TDM3885 4A Point of Load Module is an easy-to-use, fully integrated and highly efficient DC/DC module. The module's PWM controller, MOSFETs and inductor make TDM3885 a space-efficient solution, providing accurate power delivery. The TDM3885 employs an Enhanced Stability Engine that makes it stable with ceramic capacitors without compensation.

TDM3885 can operate in Forced Continuous Conduction Mode (FCCM) or can enter Diode Emulation Mode (DEM) during light loads to save power. With ultra-light loads, TDM3885 can enter a low quiescent current mode making it ideal for Standby power supplies. The switching frequency is 600kHz for an optimum solution.

It also features important protection functions, such as Pre-Bias startup, internal Soft-start, hiccup over-current protection and thermal shutdown to give required system level security in the event of fault conditions.

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1 Ordering Information

Table 1 Ordering Information

Base Part and Number	Package Type	Standard Pack Form and Qty		Orderable Part Number
TDM3885	PG-LGA-15-2 3.1 mm x 3.8 mm	Tape and Reel	2500	TDM3885XUMA1

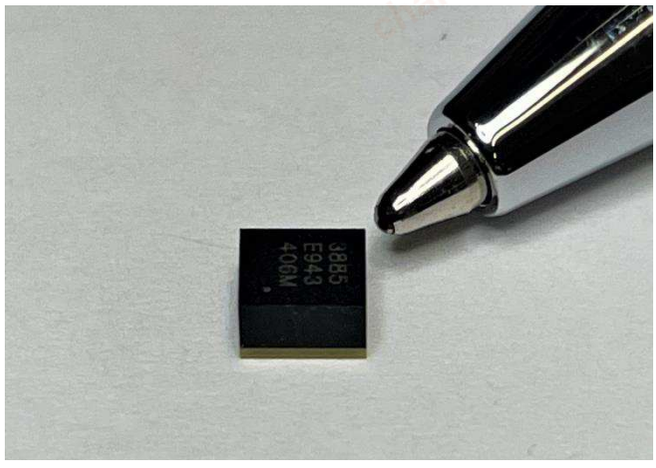


Figure 1 Picture of the Product

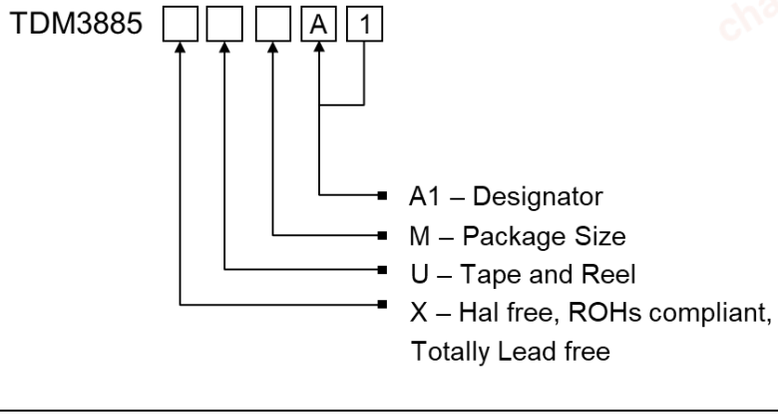


Figure 2 TDM3885 Part Number Configuration

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2 Description

2.1 PinOut

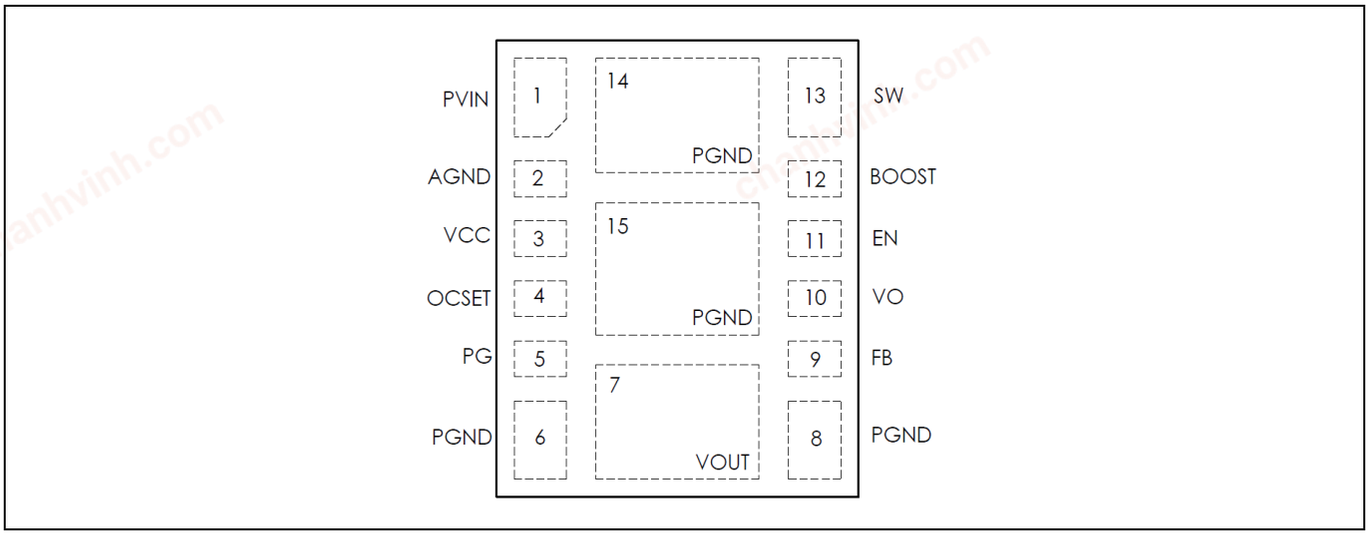


Figure 3 Pinout, Numbering and Name of Pins (transparent top view)

Table 2 Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Description
1	PV_{in}	S	Input supply for the power stage.
2	AGND	S	Signal ground for the internal reference and control circuitry.
3	Vcc	S	Input bias for the internal control circuitry and driver. Generated by internal LDO via PV_{in}. A 2.2 µF ceramic capacitor is recommended between Vcc and the Power ground (PGND).
4	OCSET	I	Over-Current Protection (OCP) limit set point. Three user selectable OCP limits are available by floating this pin, connecting it to Vcc or connecting it to PGND.
5	PG	O	Power Good status pin. Output is an open Drain. Connect a pull up resistor from this pin to Vcc or an external bias voltage.
6, 8, 14, 15	PGND	S	Power Ground. These pins serve as a separate ground for the MOSFET drivers and should be connected to the system's power ground plane.
7	V_{out}	O	Output voltage. Connect this pin to the load and decoupling capacitors.
9	FB	I	Output voltage feedback pin. Connect this pin to the output of the regulator via a resistor divider to set the output voltage.
10	Vo	I	Vo sense pin. Connect this pin directly to the output of the regulator to set the on-time.
11	En/FCCM	I	Multifunction pin: (1) Enable pin to turn the IC on and off. (2) Enable Diode Emulation (DEM) Mode operation or Forced Continuous Conduction (FCCM) Mode operation.
12	BOOST	I	Supply voltage for the high side driver. Connect this pin to the SW node of the regulator through a bootstrap capacitor.
13	SW	O	Switch Node. This pin is connected to the integrated output inductor.

Note:

I = Input, O = Output, S = Signal

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2.2 Block Diagram

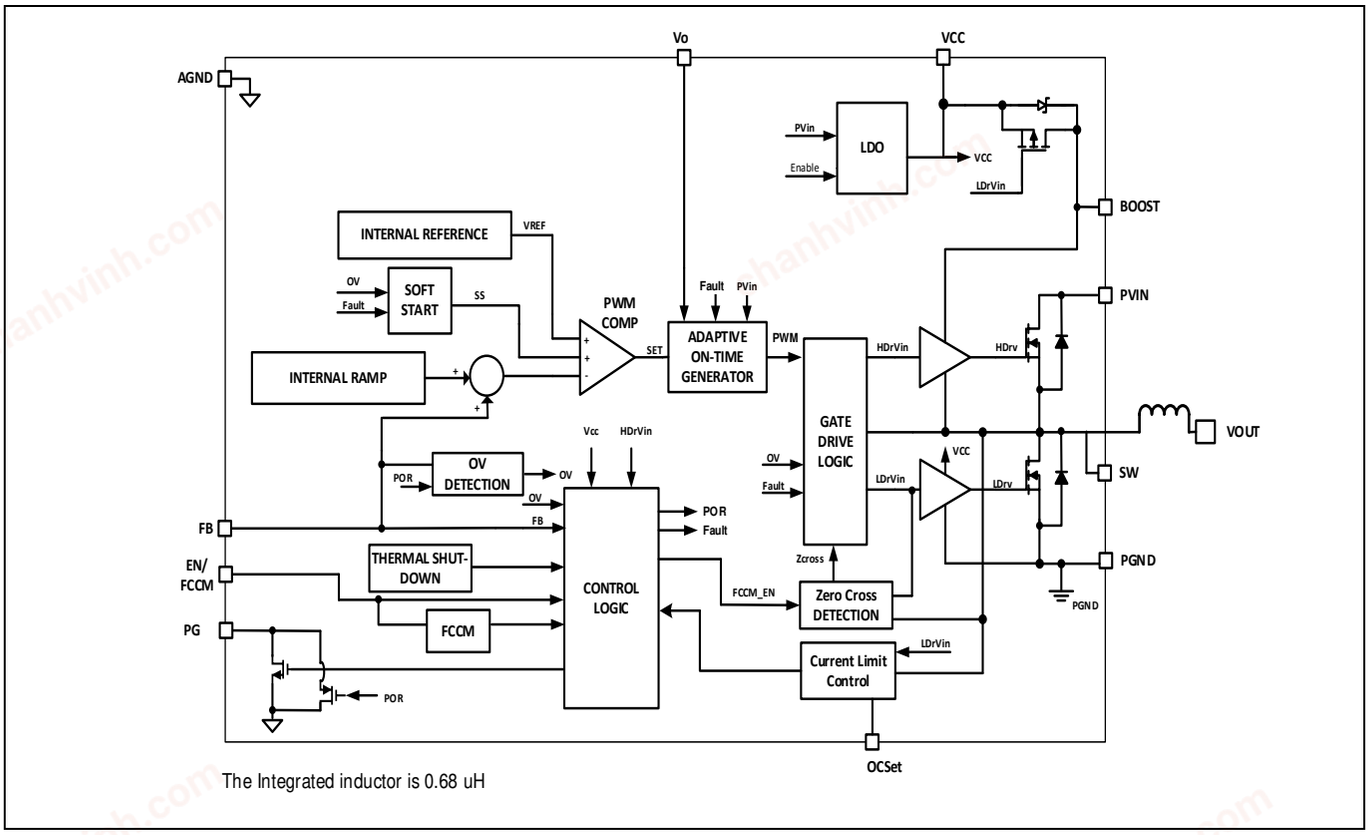


Figure 4 TDM3885 Block Diagram

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3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses beyond these listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Table 3 TDM3885 Absolute Maximum Ratings

PV_{in}, En/FCCM to PGND (Note **2**, Note **3**)	-0.3 V to 14 V (dc), 16 V (ac, 2 µs)
Vcc to PGND (Note **2**)	-0.3 V to 6 V
Boost to PGND (Note **2**)	-0.3 V to 22 V(dc), 24 V (ac, 10 ns)
SW to PGND (Note **2**)	-0.3 V to 16 V (dc), -4 V to 18 V (ac, 10 ns)
Boost to SW	-0.3 V to Vcc+0.3 V (Note **1**)
Vo, Fb to AGND (Note **2**)	-0.3 V to 6 V(dc), 6.5 V (ac, 10 µs)
OCSet, PG to AGND (Note **2**)	-0.3 V to 6 V
PGND to AGND	-0.3 V to +0.3 V
Thermal Information	
Junction to Ambient Thermal Resistance Θ_{JA}	40.5 °C/W (Note **12**)
Junction-to-top Thermal characterization parameter Ψ_{JT}	8.0 °C/W (Note **12**)
Junction-to-board Thermal characterization parameter Ψ_{JB}	12.0 °C/W (Note **12**)
Storage Temperature Range	-55 °C ≤Ta ≤ 125 °C
Junction Temperature Range	-40 °C ≤ Tj ≤ 125 °C

Note:

1. *Must not exceed 6 V.*
2. *PGND pin and AGND pin are connected together.*
3. *SW node voltage should not exceed the max voltage defined in **Table 3***

3.2 Maximum Operating Conditions

Table 4 Maximum Operating Conditions

Definitions	Symbol	Min	Max	Units
Input Voltage Range (Note **4**, Note **5**)	PV_{in}	4.7	14	V
Supply Voltage Range (Note **5**)	Vcc	4.4	5.5	
Output Voltage Range (PV_{in} =4.7 to 8V, I_{out}=0 to 3A)	Vo	0.5	3.3	
Output Voltage Range (PV_{in} =8 to 14V, I_{out} =0 to 4A)	Vo	0.5	5.0	
Continuous Output Current Range (PV_{in} =4.7 to 8V)	Io	0	3	A
Continuous Output Current Range (PV_{in} =8 to 14V)	Io	0	4	A
Operating Junction Temperature	T_j	-40	125	°C

Note:

4. *External Vcc supply voltage is not supported to bypass the internal LDO.*
5. *Maximum SW node voltage should not exceed the max voltage defined in **Table 3**.*

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3.3 Electrical Characteristics

Unless otherwise specified, these specifications apply over, 5.5 V < PV_{in} < 14 V, 0 °C < Tj < 125 °C. Typical values are specified at Ta = 25 °C.

Table 5 Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Top Switch	$R_{ds\ (on)_Top}$	V_{Boot} –V_{sw} = 5.2 V, T_j = 25 °C		82	106.4	mΩ
Bottom Switch	$R_{ds\ (on)_Bot}$	V_{cc} = 5.2 V, T_j = 25 °C		26	33.9	
Boot Diode Forward Voltage		I_{Boot}=10 mA		200	300	mV
Supply Current						
PV_{in} Supply Current (Standby)	$I_{in\ (Standby)}$	Enable low		0.22	10	µA
PV_{in} Supply Current (Static)	$I_{in\ (Static)}$	En = 2 V, No switching	0.5	0.7	2	mA
PV_{in} Supply Current (Dyn)	$I_{in\ (Dyn)}$	Enable high, PV_{in} = 12 V, Fs = 600 kHz	5	11	20	mA
Soft Start						
Soft Start Ramp Rate	SS_{rate}		0.16	0.2	0.24	mV/µs
V_{FB} Voltage						
Feedback Voltage	V_{FB}			0.5		V
Accuracy		0˚C < T_j < 85 ˚C	-0.6		+0.6	%
		-40 ˚C < T_j < 125 ˚C (Note **6**)	-1		+1	
V_{FB} Input Current	I_{VFB}	V_{FB} = 0.5 V, T_j = 25 °C	-0.4	0	+0.4	µA
On-Time Timer Control						
On Time	T_{on}	PV_{in} = 12 V, V_{out} = 1.05 V		146		ns
Minimum On-Time	$T_{on(Min)}$	Note **7**, PV_{in} = 12 V, V_{out} = 0 V		20	50	ns
Minimum Off-Time	$T_{off(Min)}$	T_j = 25 °C, V_{FB} = 0 V		240	300	ns
Thermal Shutdown						
Thermal Shutdown		Note **7**		145		°C
Hysteresis		Note **7**		25		
Under Voltage Lockout						
V_{cc}-Start-Threshold	$V_{CC_UVLO_Start}$	Vcc Rising Trip Level	4	4.2	4.4	V
V_{CC}-Stop-Threshold	$V_{CC_UVLO_Stop}$	Vcc Falling Trip Level	3.6	3.8	4.1	
Enable Threshold	Enable_High	Ramping up	1.14	1.2	1.36	V
	Enable_Low	Ramping down	0.9	1	1.06	
Input Impedance	R_{EN}		500	1000	1500	kΩ
FCCM Start Threshold	V_{FCCM_start}		2.6			V
FCCM Stop Threshold	V_{FCCM_stop}				2.3	
Current Limit						
Current Limit Threshold	Ioc	0 °C<Tj< 125 °C, OCSet = PGND	4.4	6.5	6.9	A
		0 °C <Tj< 125 °C, OCSet = Floating	3.4	5.4	5.7	
		0 °C <Tj< 125 °C, OCSet = Vcc	2.4	4.3	4.6	
Hiccup Blanking Time	Tblk_Hiccup	Note **7**		20		ms

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OV Protection						
Output OV Protection Threshold	V_{ovp}	OVP detect	115	120	125	%
Output OV Protection Delay	T_{OVPDEL}			5		µS
PGood						
Power Good Upper Threshold	$V_{PG(upper)}$	Fb Rising	85	90	95	%
Power Good Lower Threshold	$V_{PG(lower)}$	Fb Falling	80	85	90	
Power Good Sink Current	I_{PG}	PG = 0.5 V, En = 2 V	2.5	5		mA
Power Good Voltage Low when no supply	$V_{PG(low)}$	PV_{in} = Vcc = 0 V, $R_{pull-up}$=50 kΩ to 3.3 V		0.3	0.5	V

Note:

6. *Cold & hot temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.*
7. *Guaranteed by design but not tested in production.*

3.4 Typical Operating Characteristics

Unless otherwise specified, typical curves are generated at room temperature.

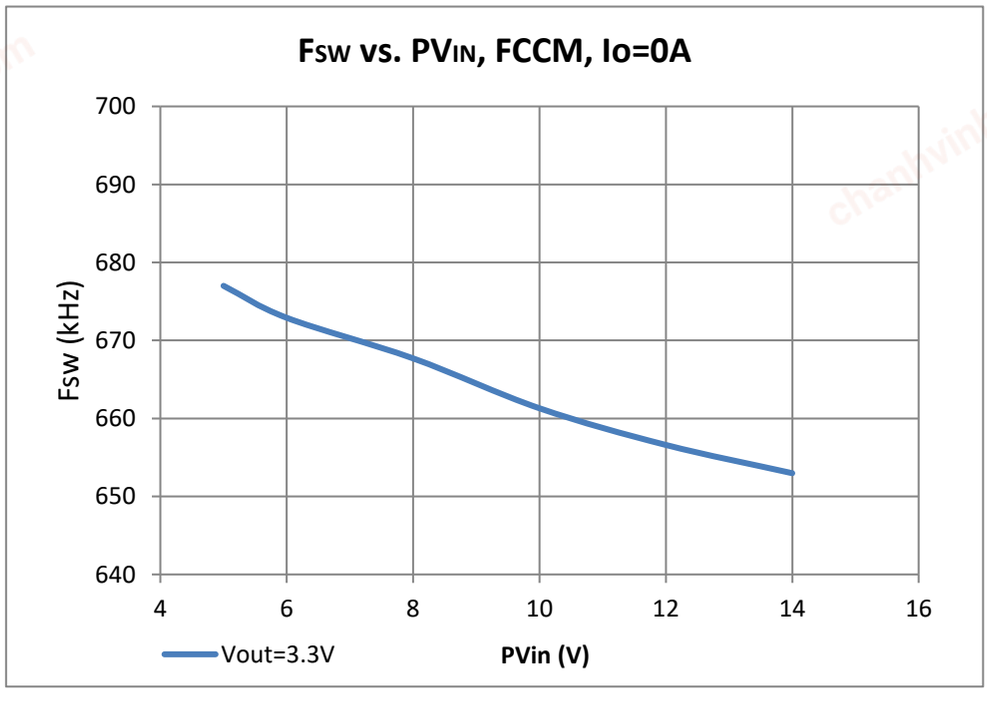


Figure 5 Switching Frequency vs. Input Voltage in FCCM, V_{out} = 3.3 V

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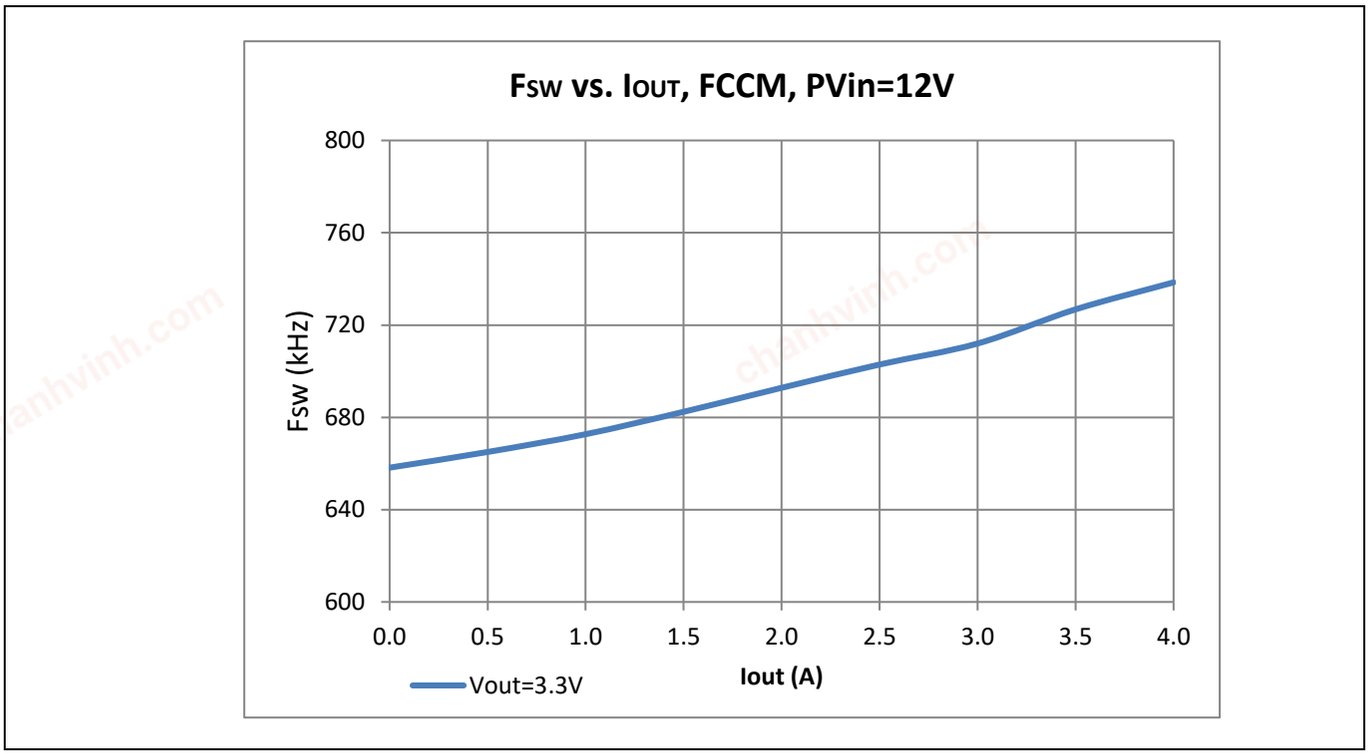


Figure 6 Switching Frequency vs. Output Current in FCCM, V_{out} = 3.3 V

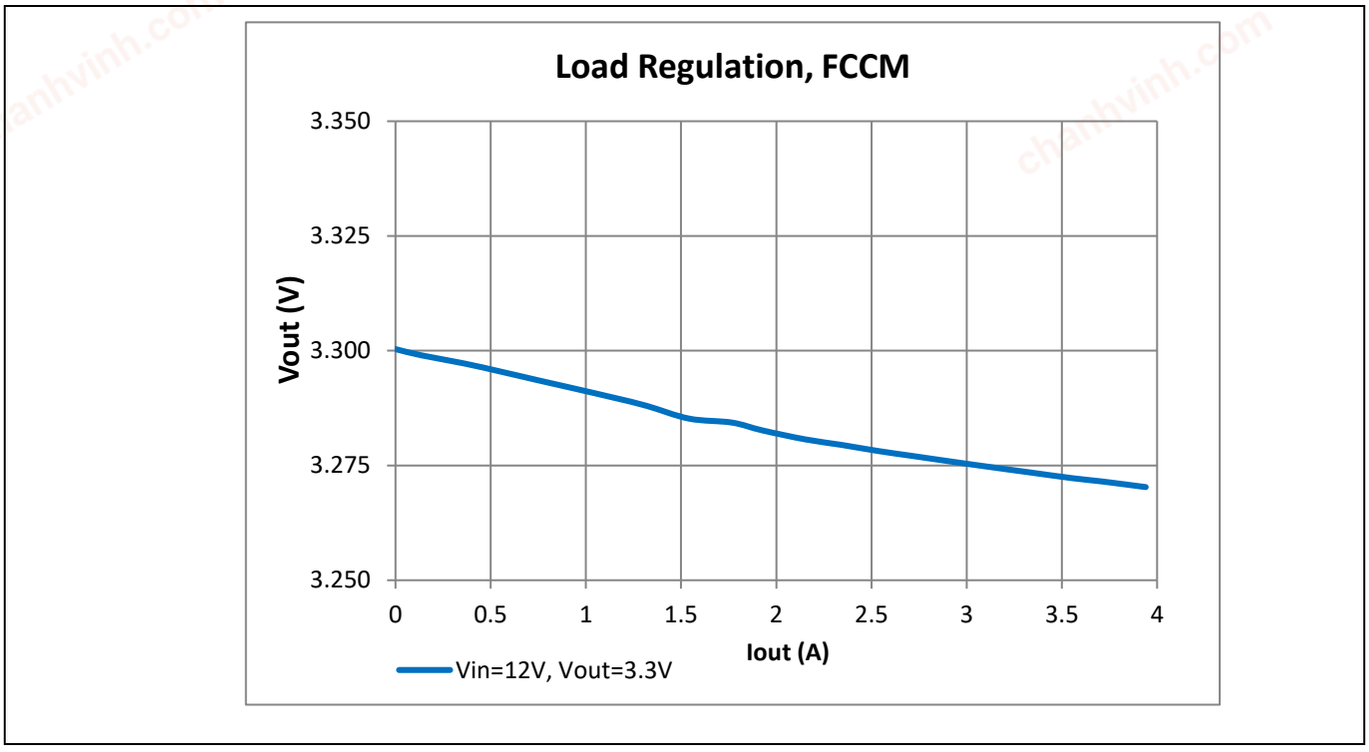


Figure 7 Load Regulation for Vo = 3.3 V

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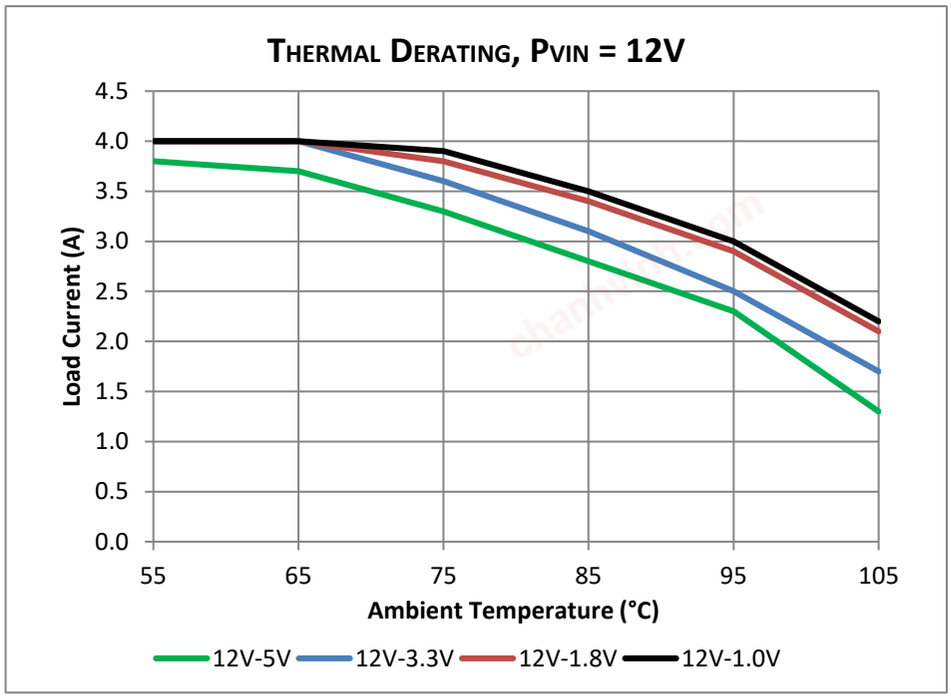


Figure 8 **TDM3885 Thermal Derating, Tested at 0LFM, Climate chamber, the Case Temperature was monitored with a 125C limit.**

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3.5 Typical Efficiency Curves

PV_{in} = 12 V [Io = 0 A – 4 A] and PV_{in} = 5 V [Io = 0 A – 3 A], Room Temperature, No Air Flow. Note that the efficiency curves include the losses of TDM3885 and the inductor losses.

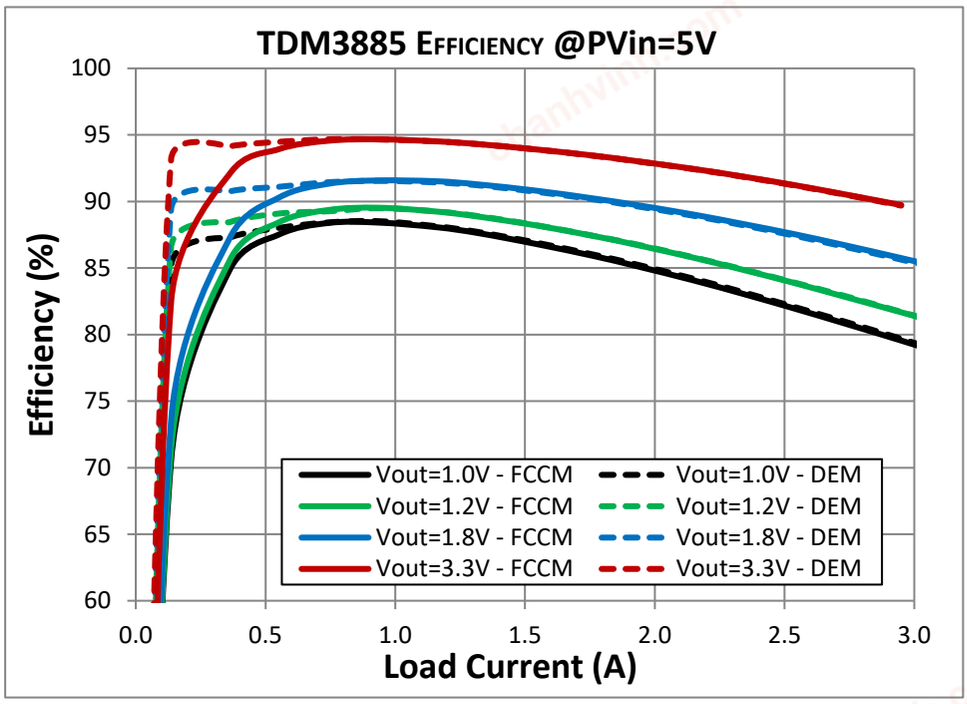


Figure 9 Efficiency Curves for PV_{in} = 5 V

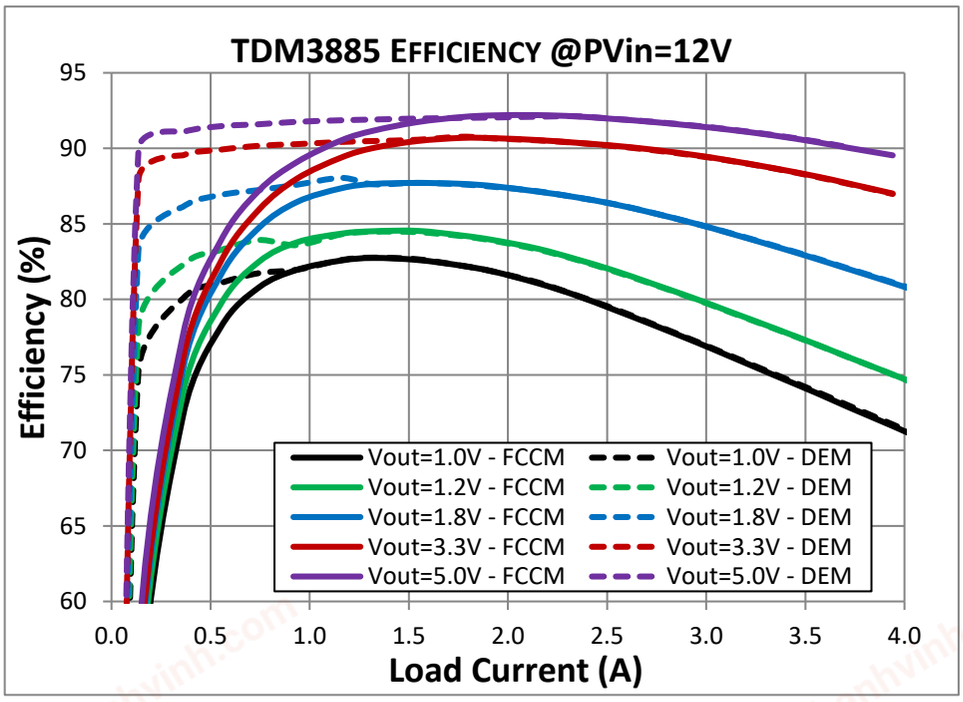


Figure 10 Efficiency Curves for PV_{in} = 12 V

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4 Theory of Operation

4.1 Description

The TDM3885 is an easy-to-use, fully integrated and highly efficient monolithic dc-dc regulator. The on-chip PWM controller, MOSFETs and integrated inductor make TDM3885 a space-efficient solution, providing accurate power delivery.

The TDM3885 offers two different operation modes: Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DEM). With FCCM, the device always operates as a synchronous buck converter with a pseudo- constant switching frequency of 600 kHz and small output voltage ripples. In DEM, the synchronous FET is turned off when the inductor current drops to zero, which provides better efficiency at light load.

4.2 Enhanced Stability IPOL Engine

The TDM3885 uses the Enhanced Stability IPOL engine that comprises Constant On-Time (COT) control with proprietary internal ramp compensation to offer stability across a wide range of conditions.

Unlike conventional COT devices, which usually require a certain amount of output ripple voltage to ensure stability, the TDM3885 includes proprietary internal ramp compensation, facilitating the use of low ESR ceramic output capacitors.

In addition, the internal ramp implements the input voltage feed-forward feature, which helps to preserve the same loop response with a wide input voltage range.

The operation of TDM3885 is described as follows. The output voltage of the regulator is fed to the FB pin through a resistor divider. Combined with the proprietary internal ramp, the FB voltage is then compared to an internal reference voltage. If the combined voltage is lower than the reference voltage, the control FET is turned on for a fixed duration to charge the output capacitor. When the on-time of the control FET is finished, the synchronous FET is turned on. In FCCM, synchronous FET stays on until the combination of FB voltage and the internal ramp drops below the reference voltage and a new PWM pulse is initiated. In DEM, synchronous FET will be turned off when the inductor current drops to zero.

4.3 Pseudo-Constant Switching Frequency

The TDM3885 operates with a pseudo-constant frequency of 600 kHz within the recommended operation range. To achieve constant switching frequency, the on-time of the control FET is automatically adjusted for different input and output voltages.

The on-time is determined by the ratio of the voltages at the V_0 pin and the PV_{in} pin, and can be calculated as follows:

$$T_{on} = \frac{V_o}{PV_{in}} \times \frac{1}{600\ kHz}$$

4.4 Soft-Start

The TDM3885 has an internal digital soft-start circuit to control the output voltage rise time, and to limit the current surge at start-up. To ensure correct start-up, the soft-start sequence initiates when Enable and Vcc voltages rise above their UVLO thresholds and the internal Power On Ready (POR) signal is asserted. The internal soft-start signal linearly rises at the rate of 0.2 mV/µs. The normal V_{out} start-up time is fixed, as shown below.

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$$T_{start} = \frac{0.5\ V}{0.2\ mV/\ us} = 2.5\ ms$$

The over-current protection (OCP) and over-voltage protection (OVP) are enabled during soft-start to protect the device against any short circuit or over-voltage condition. **Figure 11** illustrates the theoretical operation waveforms during the start-up.

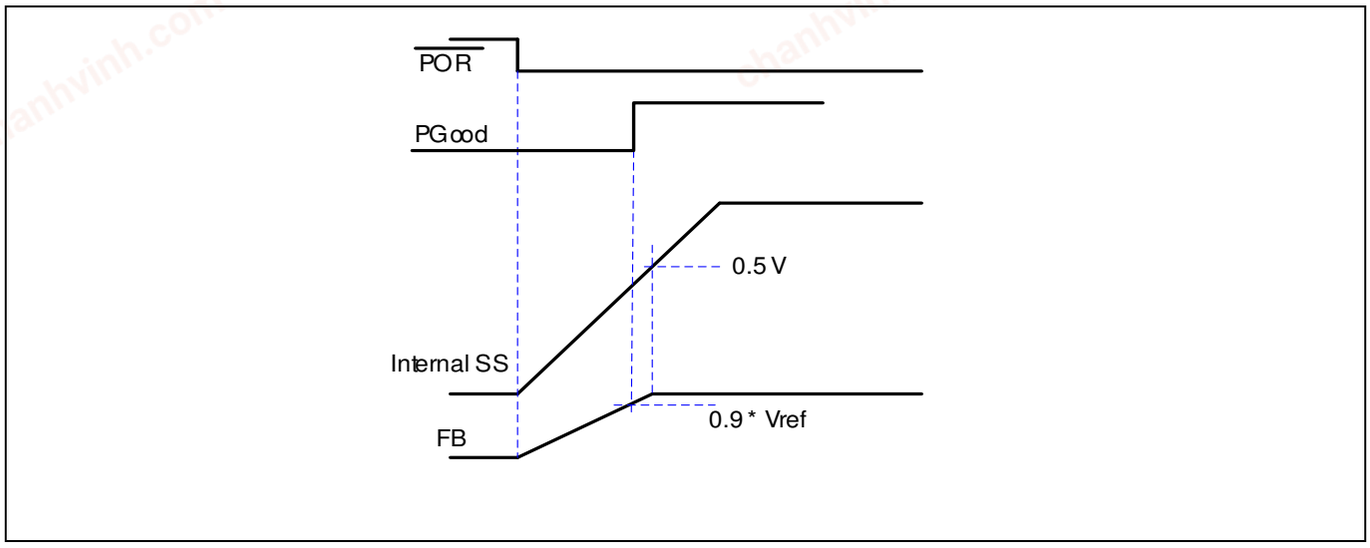


Figure 11 Theoretical operation waveforms during soft-start

4.5 En/FCCM

En/FCCM is a multi-function pin. It can be used to:

- Turn the TDM3885 on and off
- Select the operation mode: FCCM or DEM
- Implement Under-Voltage Lockout of the Input Voltage

When En/FCCM voltage is higher than the Enable_high threshold (1.2 V typical), the TDM3885 is turned on with DEM. In order to operate in FCCM, the En/FCCM voltage needs to be above 2.6 V. The Enable/FCCM thresholds are designed to be compatible with 3.3 V logic.

The TDM3885 has a precise Enable_high threshold voltage, which is internally monitored by the Under-Voltage Lockout (UVLO) circuit. As shown in **Figure 12**, the input of the Enable pin can be derived from the PV_{in} voltage by a resistor divider, R_{EN1} and R_{EN2}. By selecting different divider ratios, users can program the UVLO threshold voltage. The bus voltage UVLO is a very useful feature. It prevents the TDM3885 from operating when PV_{in} is lower than the desired voltage level.

For some space-constrained designs, the En/FCCM pin can be directly connected to PV_{in} without using an external resistor divider.

The En/FCCM pin should not be left floating. A pull-down resistor in the range of tens of kilohms is recommended.

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Figure 13 shows the connections of En/FCCM without using the external resistor divider. **Figure 14** and **Figure 15** illustrate the theoretical start-up waveforms.

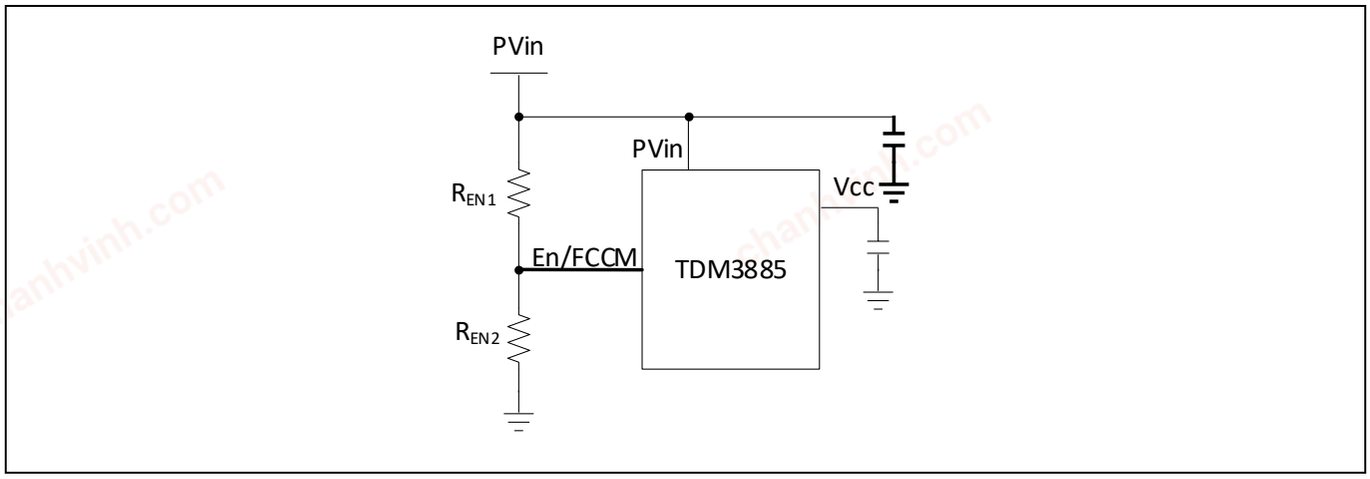


Figure 12 Single supply configuration with adjustable PV_{in} UVLO and optional FCCM or DEM

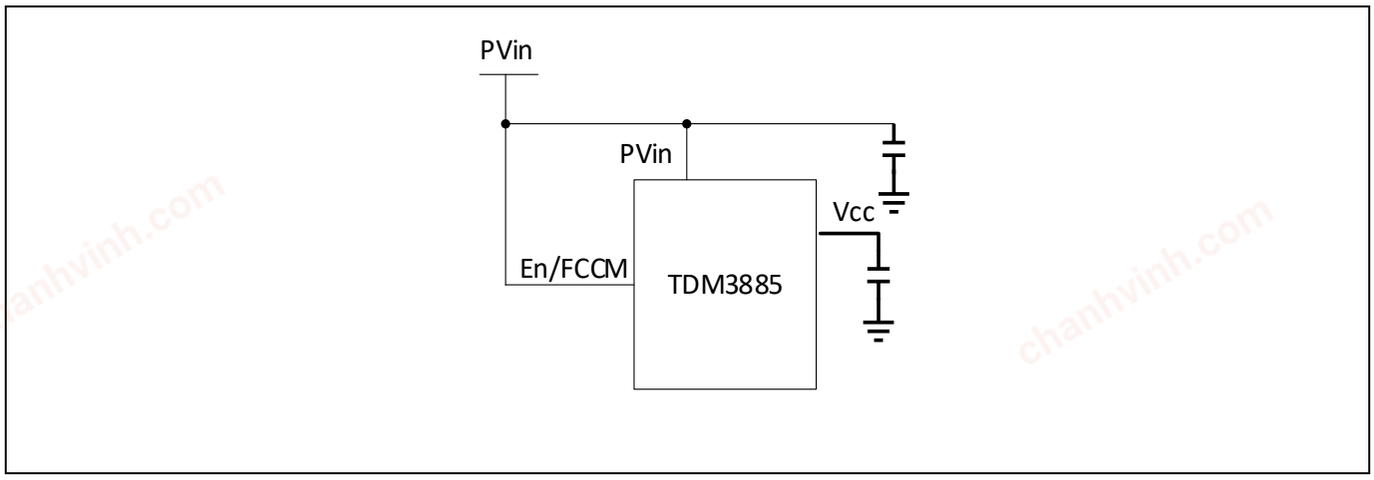


Figure 13 Single supply configuration with FCCM operation

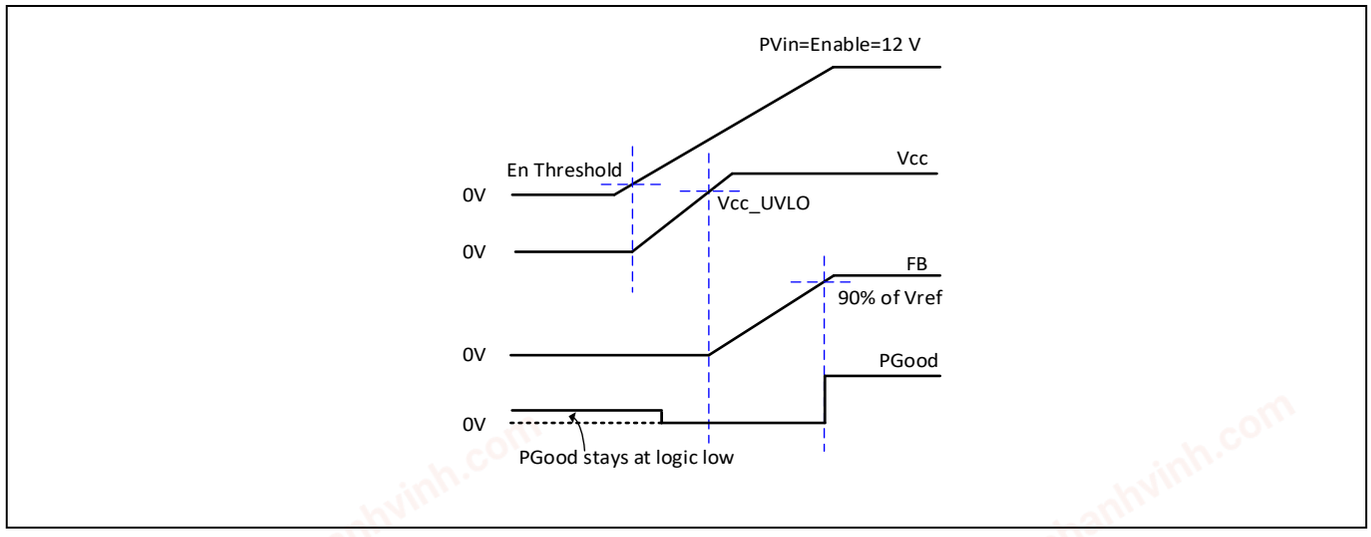


Figure 14 Start-up with PV_{in} and Enable tied together. PGood is pulled up to an external supply

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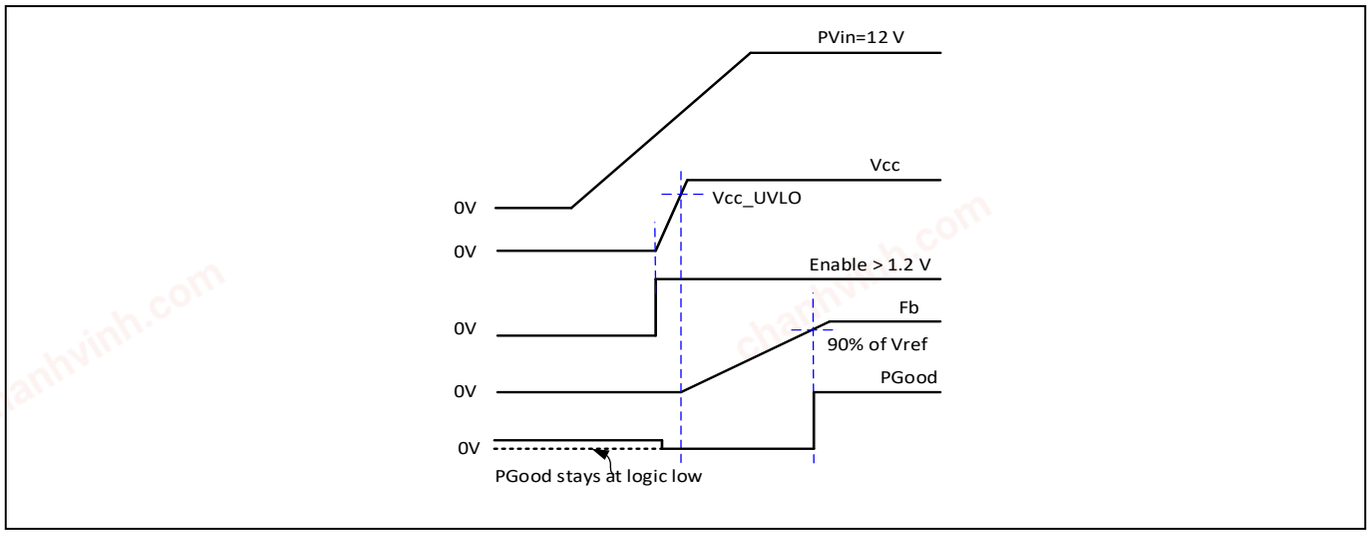


Figure 15 Start-up with Enable up after PV_{in}. PGood is pulled up to an external supply

4.6 Pre-Bias Start-Up

The TDM3885 is able to start up into a pre-charged output without causing oscillation and disturbances of the output voltage. When TDM3885 starts up with a pre-biased output voltage, both control FET and Synch FET are kept off until the internal soft-start signal exceeds the FB voltage.

During pre-bias start-up, the PGood signal is held low until the first gate signal for the control FET is generated.

4.7 Over-Current Protection

TDM3885 has three selectable Over-Current Protection (OCP) thresholds determined by the voltage level of the OCSet pin. The OCP is performed by sensing the current through the $R_{DS(on)}$ of the Sync MOSFET. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and mitigates layout-related noise issues. The current limit is pre-set internally and is thermally compensated to minimize OCP limit variation.

The OCP circuit senses the current of the Sync MOSFET 100 ns after the Control FET is turned off. If the current exceeds the OCP limit, PGood and soft start signals will be pulled low. The Sync FET remains on until the current is decreased to zero. The TDM3885 then enters hiccup mode. Both Control FET and Sync FET remain off during the hiccup blanking time. After the hiccup blanking time expires, the TDM3885 will try to restart. If the over-current fault is still detected, the preceding actions will be repeated. The TDM3885 stays in hiccup mode until the over-current fault is removed. **Figure 16** illustrates the operation of OCP.

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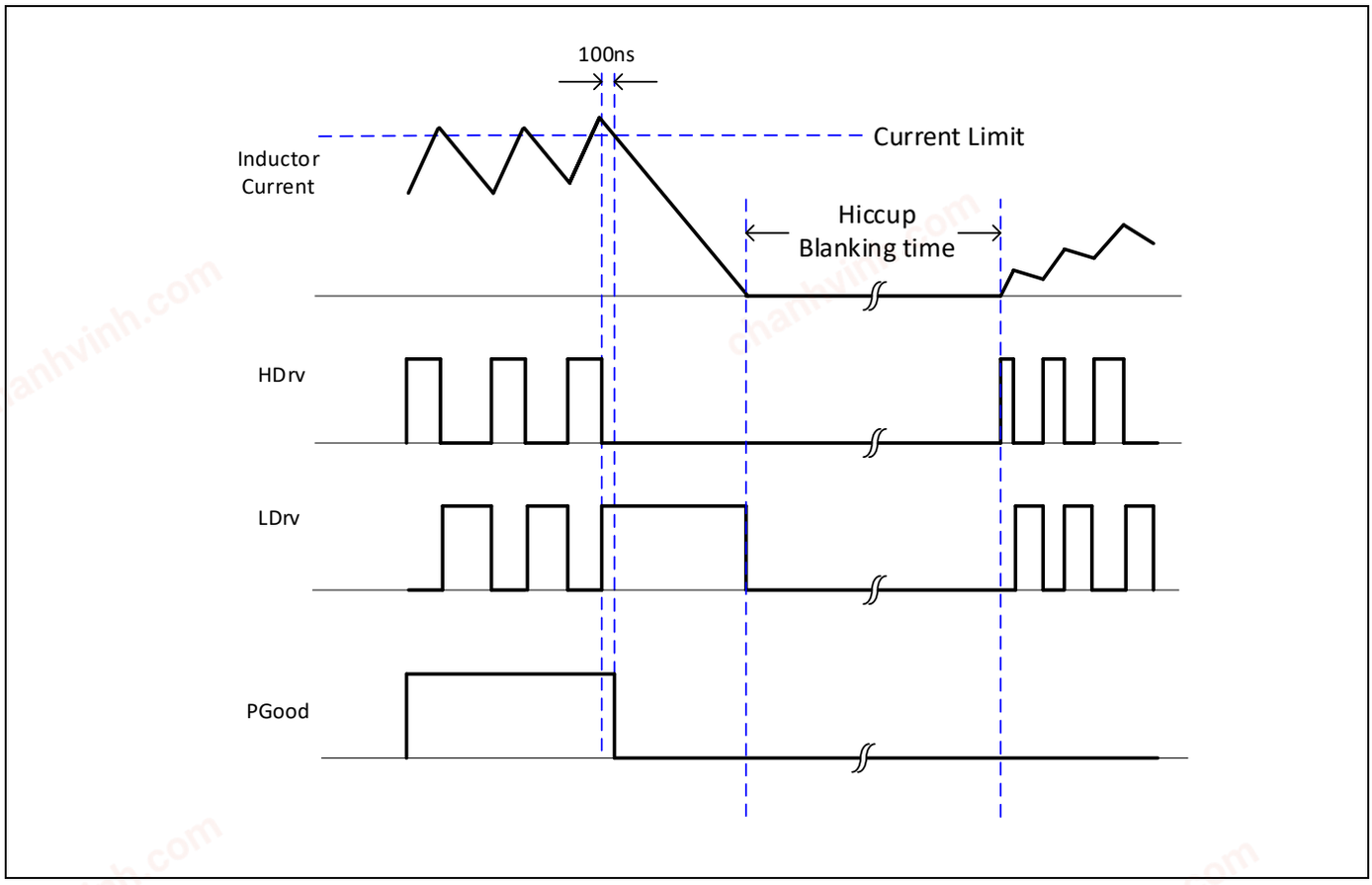


Figure 16 Illustration of OCP with hiccup Mode

4.8 Minimum On-Time and Off-Time

The minimum on-time refers to the shortest time for control FET to be reliably turned on. Typically, it is 20 ns.

In both DEM and FCCM, the Sync FET stays on for at least 240 ns, which is referred to as the minimum off-time. The minimum off-time is needed to charge the bootstrap capacitor and to monitor the current of the Sync FET for OCP.

4.9 Over-Voltage Protection

The TDM3885 senses voltage at the FB pin for Over-Voltage Protection (OVP). When FB voltage exceeds the OVP threshold for longer than the output OV protection delay (typical value is 5 µs), the OVP circuitry is tripped. The Control FET is turned off immediately and PGood is pulled low. The Sync FET is turned on to discharge the output capacitor until the FB voltage drops below the OVP threshold.

Once OVP is tripped, the Control FET remains latched off until a reset is performed by cycling either P_{Vin} voltage or the Enable signal. **Figure 17** illustrates the operation of over-voltage protection.

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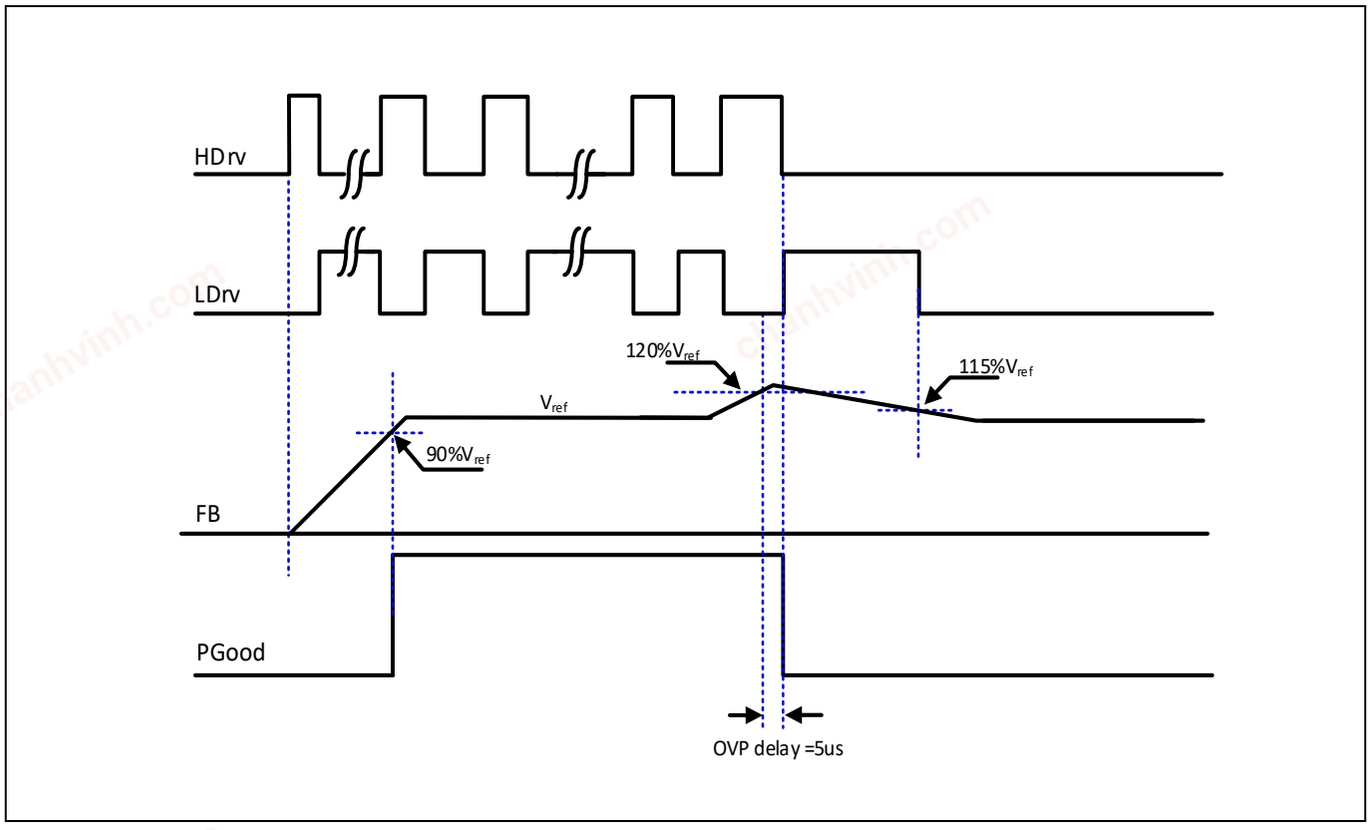


Figure 17 Operation of Over-Voltage Protection

4.10 PGood

The PGood pin is the open drain of an internal NFET and needs to be externally pulled high through a pull-up resistor, e.g., 49.9 kΩ.

The PGood signal is high when three criteria are satisfied:

1. Enable and VCC UVLO voltage are above their respective thresholds;
2. No fault occurs including over-current, over-voltage and over-temperature;
3. Output voltage (V_{out}) is in regulation.

In order to detect if V_{out} is in regulation, the PGood comparator continuously monitors the FB pin voltage. When FB voltage ramps up above the upper threshold (90% of Vref), the PGood signal is pulled high. When FB voltage ramps down below the lower threshold (85% of Vref), the PGood signal is pulled low. **Figure 18** illustrates the PGood upper and lower thresholds.

For pre-biased start-up, PGood is not active until the first gate signal of the control FET is initiated.

TDM3885 also integrates a PFET in parallel with the PGood NFET, as shown in **Figure 4**. This PFET allows the PGood signal to stay at logic low when the bias voltage of TDM3885 is low, and/or if the En is low. Please refer to **Figure 14** and **Figure 15**.

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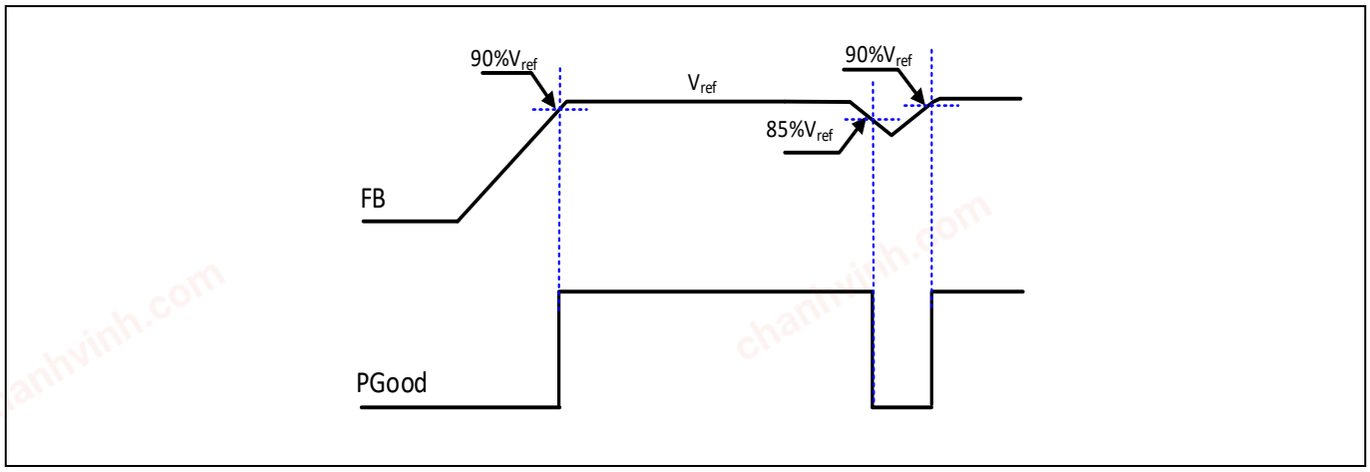


Figure 18 Power Good Thresholds

4.11 Over-Temperature Protection

Temperature sensing is provided by the TDM3885. The Over-Temperature Protection (OTP) threshold is typically set to 145 °C. When the OTP threshold is exceeded, both MOSFETs are turned off and the internal soft start is reset. The internal LDO is still in operation when OTP is tripped.

Automatic restart is initiated when the sensed temperature drops below the OTP threshold. The hysteresis of the OTP threshold is 25 °C.

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5 Application

5.1 Application Information

The following example is a typical application for TDM3885. The application circuit is shown in **Figure 19**.

- PV_{in} =12 V
- V_0 = 3.3 V
- I_0 = 4 A
- V_0 Ripple voltage = ± 1% of V_0
- Transient response = ± 3% of V_0 for 30% Load transient

ENABLE TDM3885

To enable TDM3885 in Diode Emulation Mode (DEM), the voltage at the EN/FCCM pin should be higher than the Enable threshold, but lower than FCCM stop threshold. If a resistor divider is used to generate the Enable voltage from PV_{in} as shown in **Figure 12**, the resistor divider can be selected as follows.

$$PV_{in(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq 1.36$$

$$PV_{in(\max)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \leq 2.3$$

Where $PV_{in\,(min)}$ and $PV_{in\,(max)}$ are the minimum and maximum input voltages respectively.

To enable TDM3885 in FCCM, the voltage at EN/FCCM pin should be no less than the FCCM start threshold. The EN/FCCM pin can be connected directly to PV_{in} as shown in **Figure 13**, or a resistor divider can be used, **Figure 12**. The following criterion should be satisfied when selecting the resistor divider for FCCM.

$$PV_{in(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq 2.6$$

INPUT CAPACITOR SELECTION

Without input capacitors, the pulse current of the control FET is provided directly from the input power supply. Due to the impedance on the input power supply cabling, the pulse current can disturb the input voltage and potential EMI issues can result. The input capacitors filter the pulse current of the control FET, reducing these risks and resulting in almost constant current from the input supply.

The input capacitors should be selected to tolerate the input pulse current, and to reduce input voltage ripple. The RMS value of the input ripple current can be expressed as:

$$I_{RMS} = I_0 \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_0}{V_{in}}$$

Where I_{RMS} is the RMS value of the input capacitor current. I_0 is the output current. D is the duty ratio.

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Application

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

$$C_{in(\min)} > \frac{I_0 \times D \times (1-D)}{f_{sw} \times \Delta V_{in(\max)}}$$

Where $\Delta V_{in(max)}$ is the maximum allowable peak-to-peak input ripple voltage.

Ceramic capacitors are recommended as input capacitors due to low ESR, ESL and high RMS current capability. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

OUTPUT CAPACITOR SELECTION

To ensure loop stability, a minimum of one 22 µF output capacitor is suggested. The voltage ripple and transient requirements determine the output capacitor selection.

The following formula calculates the peak-to-peak output voltage ripple due to the inductor ripple current charging the output capacitor.

$$\Delta V_0 = \frac{\Delta i_{L\max}}{8 \times C_0 \times f_{sw}}$$

Therefore,

$$C_0 > \frac{\Delta i_{L\max}}{8 \times \Delta V_{0\min} \times f_{sw}}$$

Where ΔV_{0min} is the minimum allowable peak-peak output ripple voltage. Δi_{Lmax} is the maximum inductor ripple current.

The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. For most applications, it is suggested to use Multi-Layer Ceramic Capacitors (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion.

$$C_0 > \frac{L \times \Delta I_{0\max}^2}{2 \times \Delta V_{0L_\max} \times V_0}$$

Where ΔV_{0L_max} is the max allowable Vo deviation during the load transient. ΔI_{0max} is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet transient response requirements.

OUTPUT VOLTAGE PROGRAMMING

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.5 V. The divider ratio is set to provide 0.5 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_0 = V_{ref} \times (1 + \frac{R_1}{R_2})$$

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Application

The bottom feedback resistor is recommended not to exceed 20 kΩ, in order to avoid interference with the internal circuitry.

FEEDFORWARD CAPACITOR

A small MLCC capacitor C_{ff}, can be placed in parallel with the top feedback resistor to improve transient response. As a general rule of thumb, for a fixed top feedback resistor of 39.2 kΩ, 100 pF can be used for C_{ff}.

BOOTSTRAP CAPACITOR

For most applications, a 0.1 µF ceramic capacitor is recommended for the bootstrap capacitor placed between the SW node and the Boot pin.

VCC BYPASS CAPACITOR

A 2.2 µF ceramic capacitor should be placed between VCC and PGND.

5.2 Typical Application Diagrams

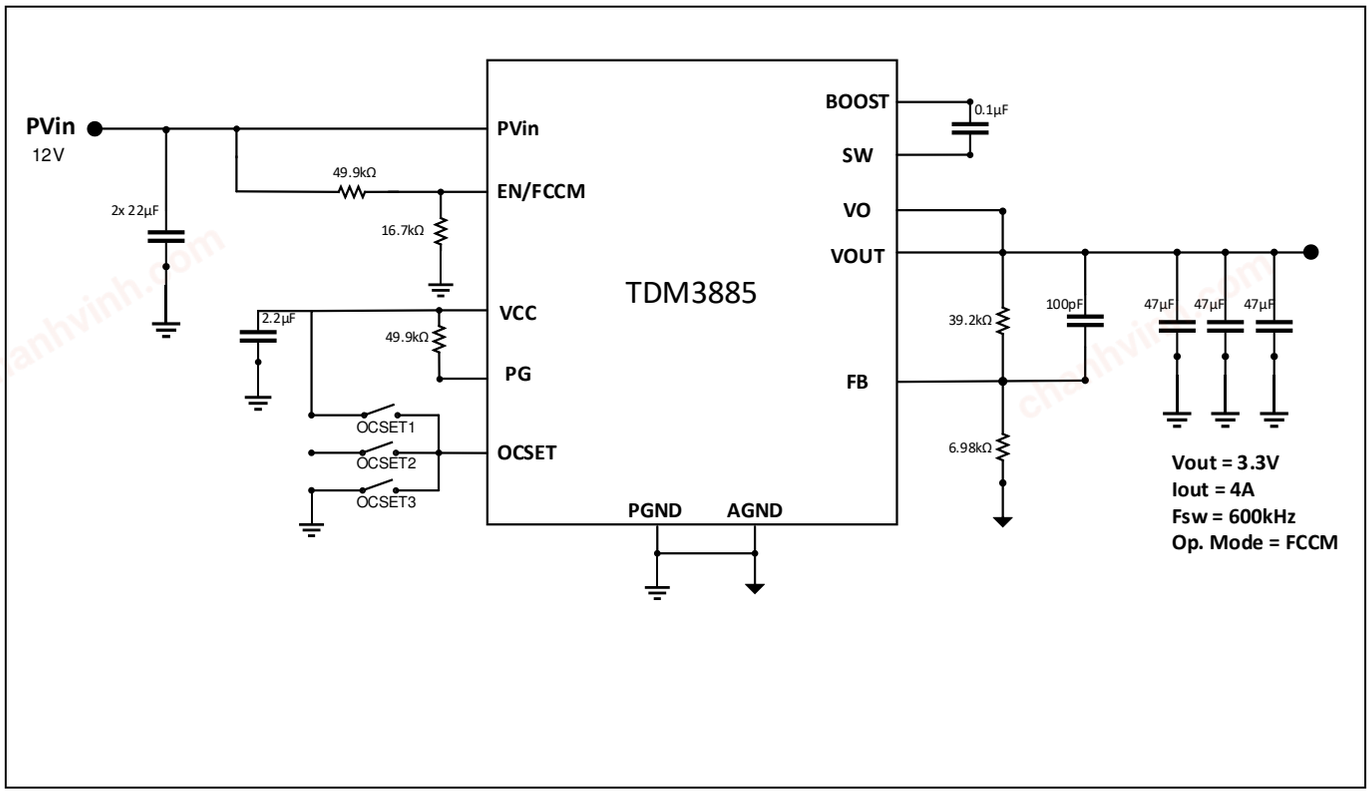


Figure 19 Application Diagram PV_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 4 A, FCCM

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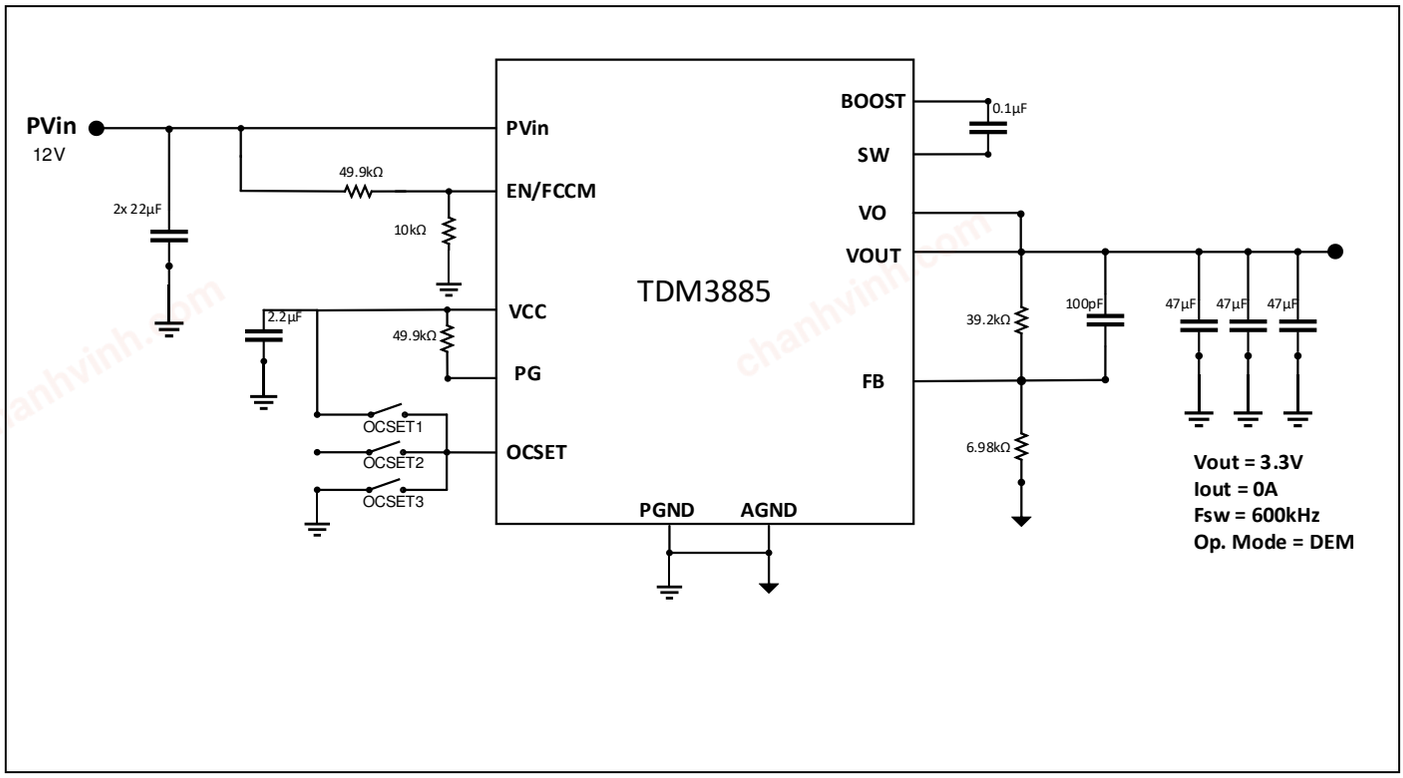


Figure 20 Application Diagram PV_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 0 A, DEM

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5.3 Recommended configurations

Table 6 lists recommended configurations for a few commonly used output voltages.

Table 6 Recommended configurations

PV_{in} (V)	V_{out} (V)	Upper FB Resistor kΩ	Lower FB Resistor kΩ	Cff (pF)	Minimum Co (µF) Note 9	Maximum Co (µF) Note 9
12	5.0	39.2	4.32	100	3 x 47µF	14 x 47µF
	3.3	39.2	6.98	100	3 x 47µF	14 x 47µF
	2.5	39.2	9.76	100	3 x 47µF	12 x 47µF
	1.8	39.2	15.0	100	3 x 47µF	10 x 47µF
	1.2	16.5	11.8	100	3 x 47µF	10 x 47µF
	1.0	16.5	16.5	100	3 x 47µF	10 x 47µF
5	3.3	39.2	6.98	100	3 x 47µF	14 x 47µF
	2.5	39.2	9.76	100	3 x 47µF	12 x 47µF
	1.8	39.2	15.0	100	3 x 47µF	10 x 47µF
	1.2	16.5	11.8	100	3 x 47µF	10 x 47µF
	1.0	16.5	16.5	100	3 x 47µF	10 x 47µF

Note:

8. *All resistors are 0402, E96 series, 1% standard*
9. *The output capacitors are selected to meet ±1% output ripple voltage and ±3% undershoot/overshoot at 30% of max load transient with 2.5A/µs slew rate. Please note that 47µF is rated capacitance at 0V DC bias voltage.*
10. *Application should not exceed the max operating conditions defined in **Table 4**.*

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5.4 Typical Operating Waveforms

PVin = 12.0V, Vo=3.3V, Io=0A - 4A, No airflow, room temperature

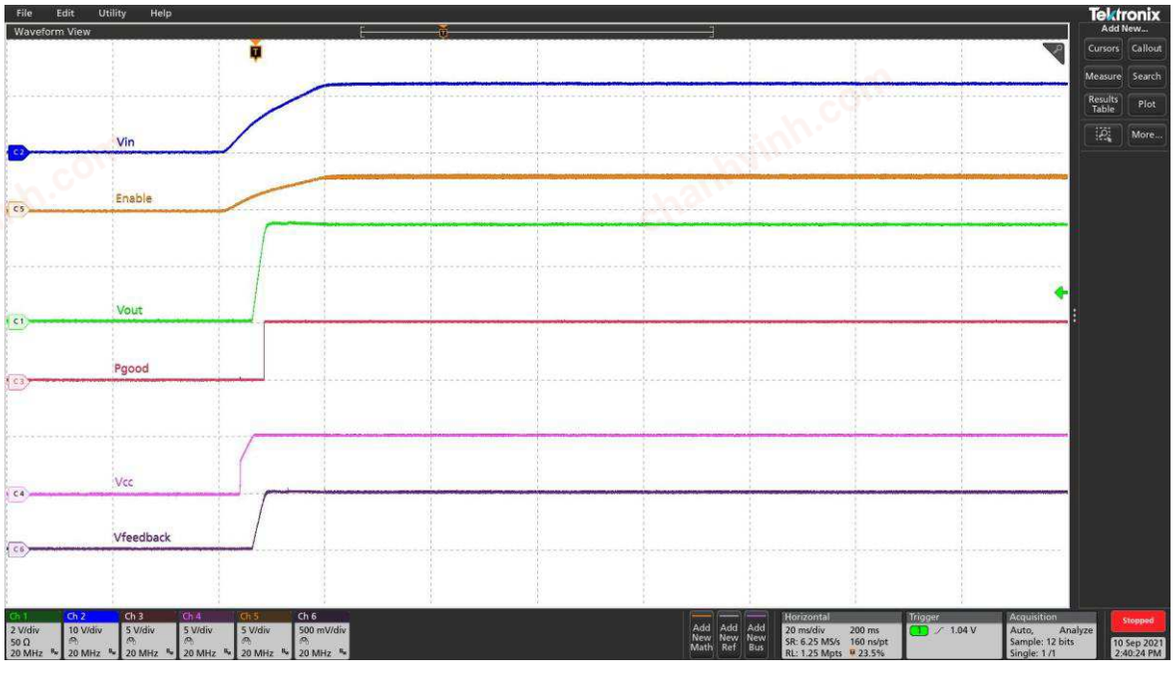


Figure 21 Start-up, PV_{in} =12V, V_{out} = 3.3V, I_{out} = 0A, FCCM. C_{H1} = V_{out}, C_{H2} = PV_{in}, C_{H3} = P_{GOOD}, C_{H4} = V_{CC}, C_{H5} = Enable, C_{H6} = $V_{FEEDBACK}$

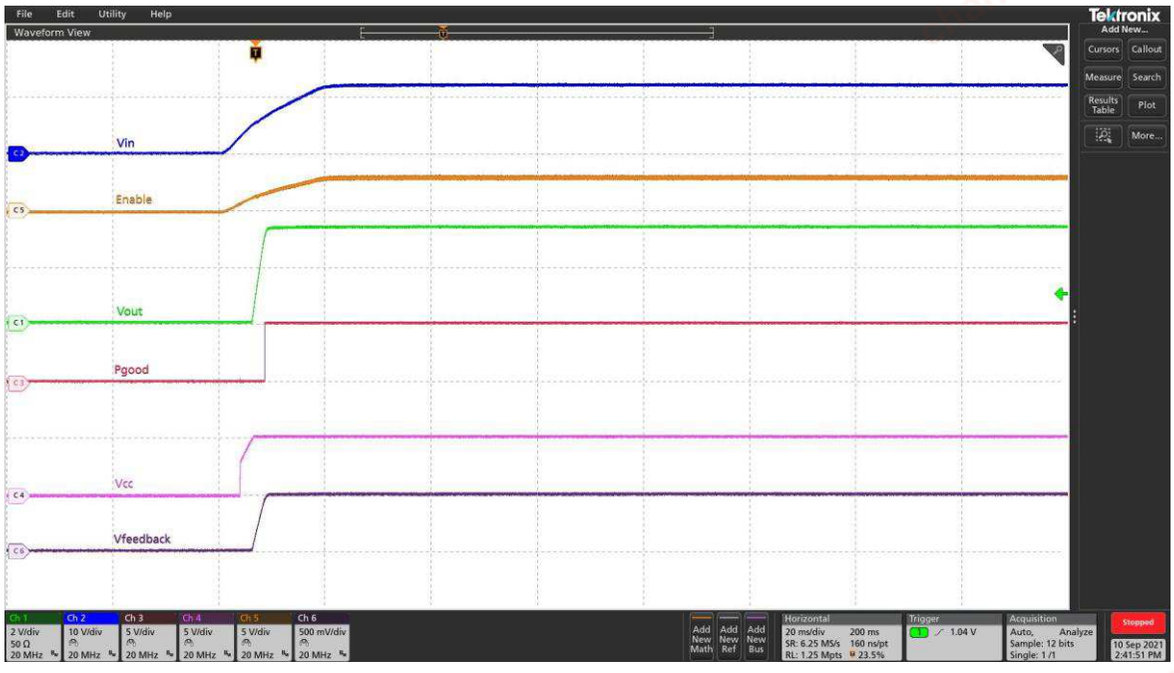


Figure 22 Start-up, PV_{in} =12V, V_{out} = 3.3V, I_{out} = 4A, FCCM. C_{H1} = V_{out}, C_{H2} = PV_{in}, C_{H3} = P_{GOOD}, C_{H4} = V_{CC}, C_{H5} = Enable, C_{H6} = $V_{FEEDBACK}$

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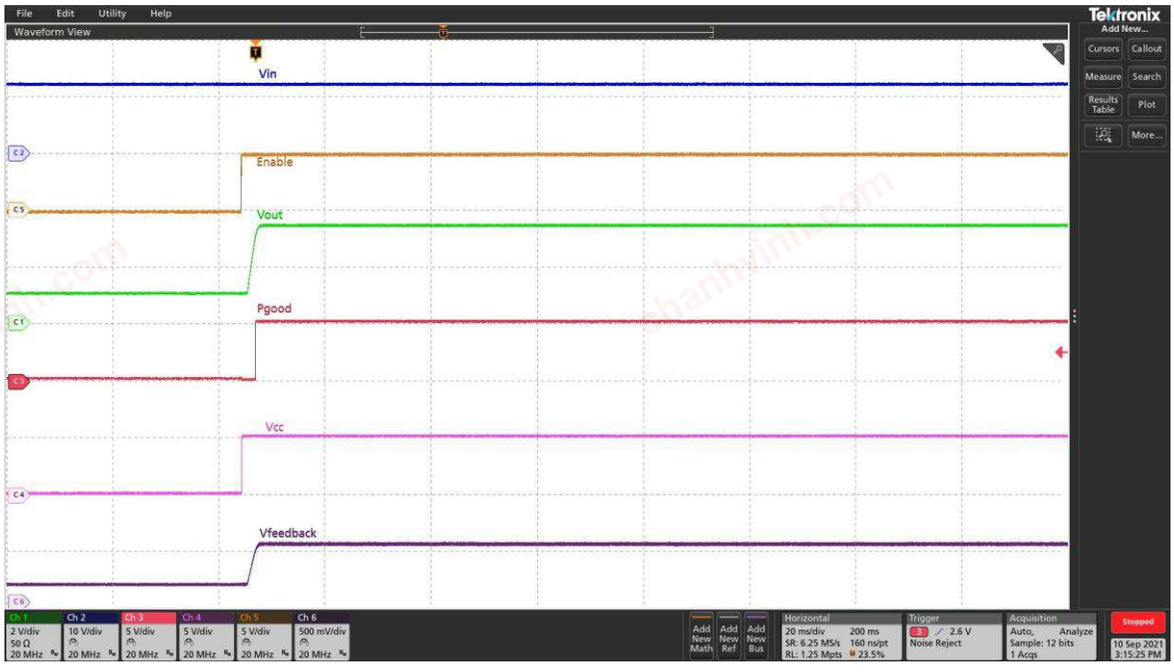


Figure 23 Start-up Prebias [1V], PV_{in} =12V, V_{out} = 3.3V, I_{out} = 0A, FCCM. C_{H1} = V_{out}, C_{H2} = PV_{in}, C_{H3} = P_{GOOD}, C_{H4} = V_{CC}, C_{H5} = Enable, C_{H6} = $V_{FEEDBACK}$

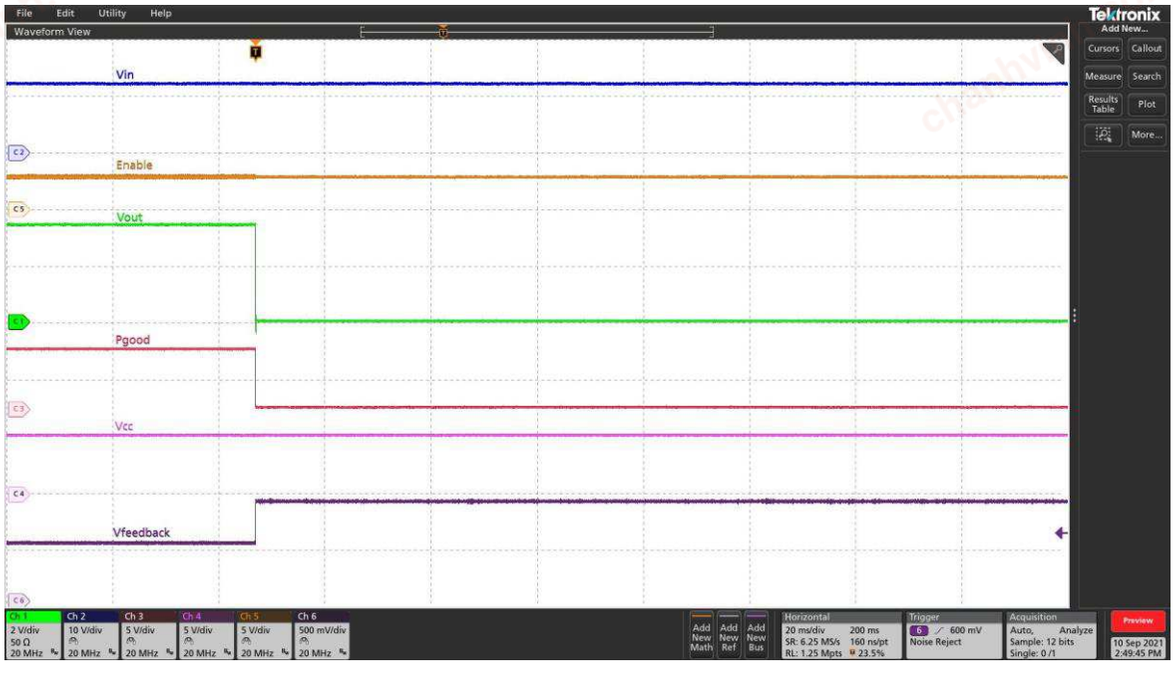


Figure 24 OVP, PV_{in} =12V, V_{out} = 3.3V, I_{out} = 0A, FCCM. C_{H1} = V_{out}, C_{H2} = PV_{in}, C_{H3} = P_{GOOD}, C_{H4} = V_{CC}, C_{H5} = Enable, C_{H6} = $V_{FEEDBACK}$

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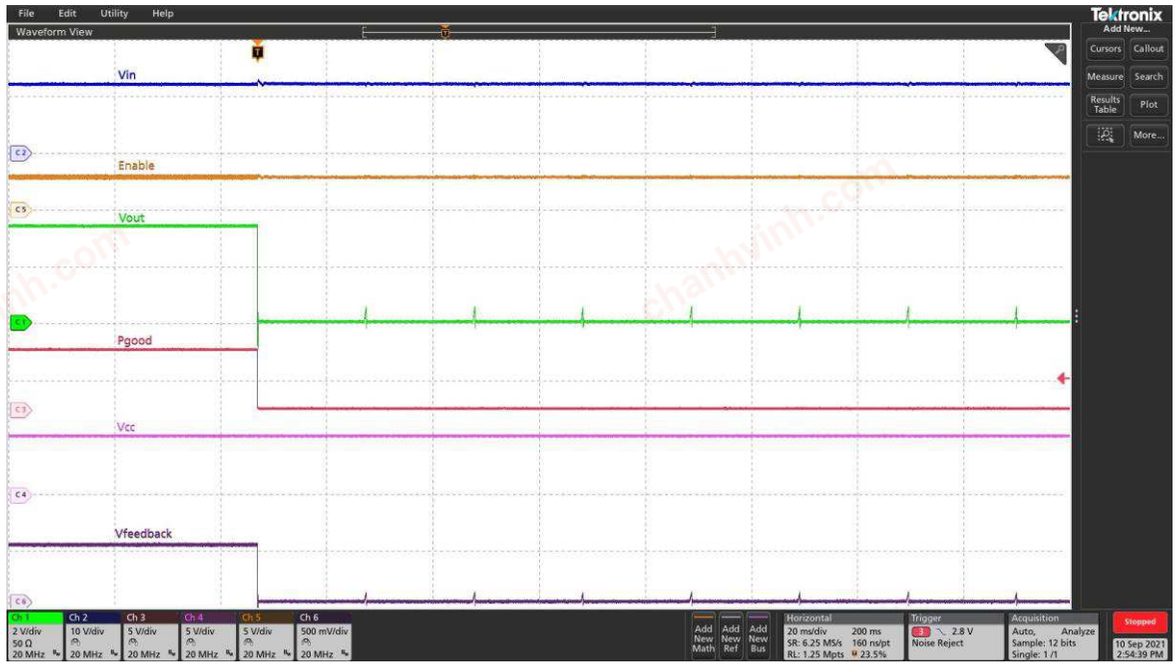


Figure 25 Short Circuit, PV_{in} =12V, V_{out} = 3.3V, I_{out} = 4A, FCCM. C_{H1} = V_{out}, C_{H2} = PV_{in}, C_{H3} = P_{GOOD}, C_{H4} = V_{CC}, C_{H5} = Enable, C_{H6} = $V_{FEEDBACK}$

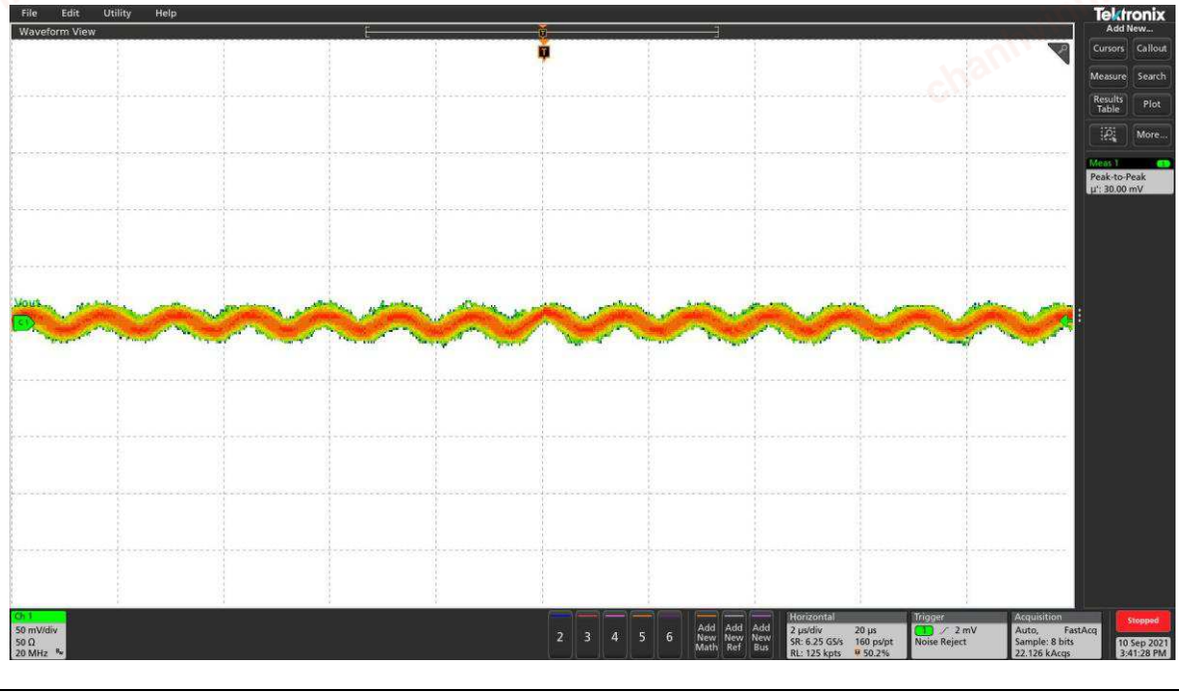


Figure 26 V_{out} ripple, PV_{in} =12V, V_{out} = 3.3V, I_{out} = 4A, FCCM. C_{H1} = V_{out}

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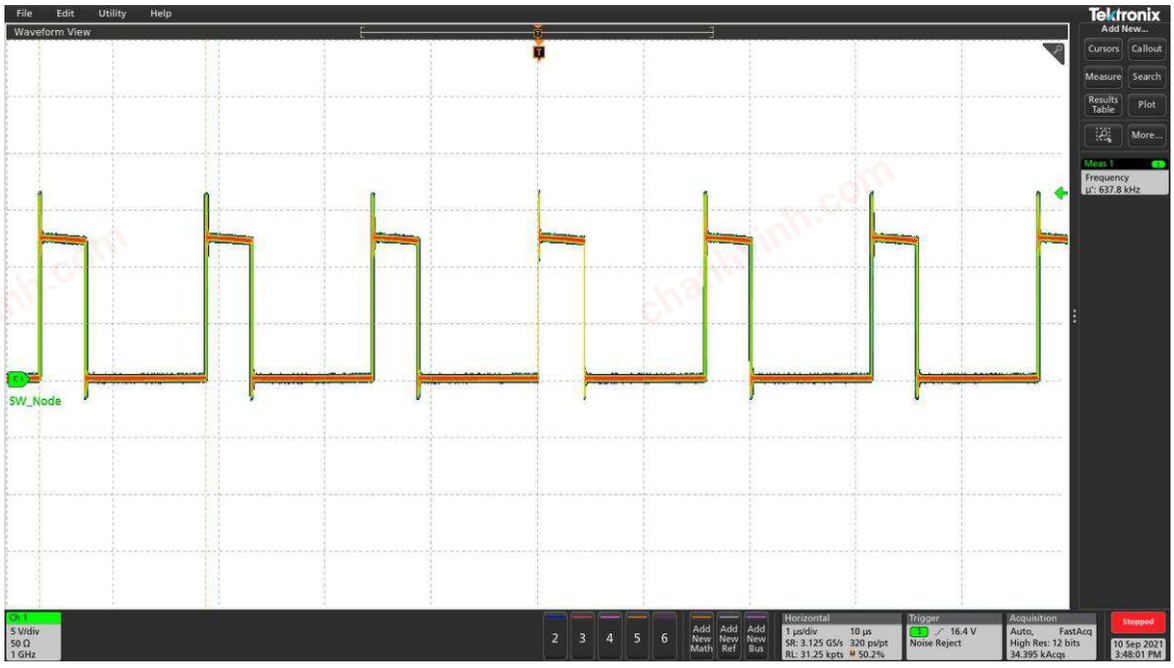


Figure 27 SW node, PV_{in} =12V, V_{out} = 3.3V, I_{out} = 0A, FCCM. C_{H1} = SW

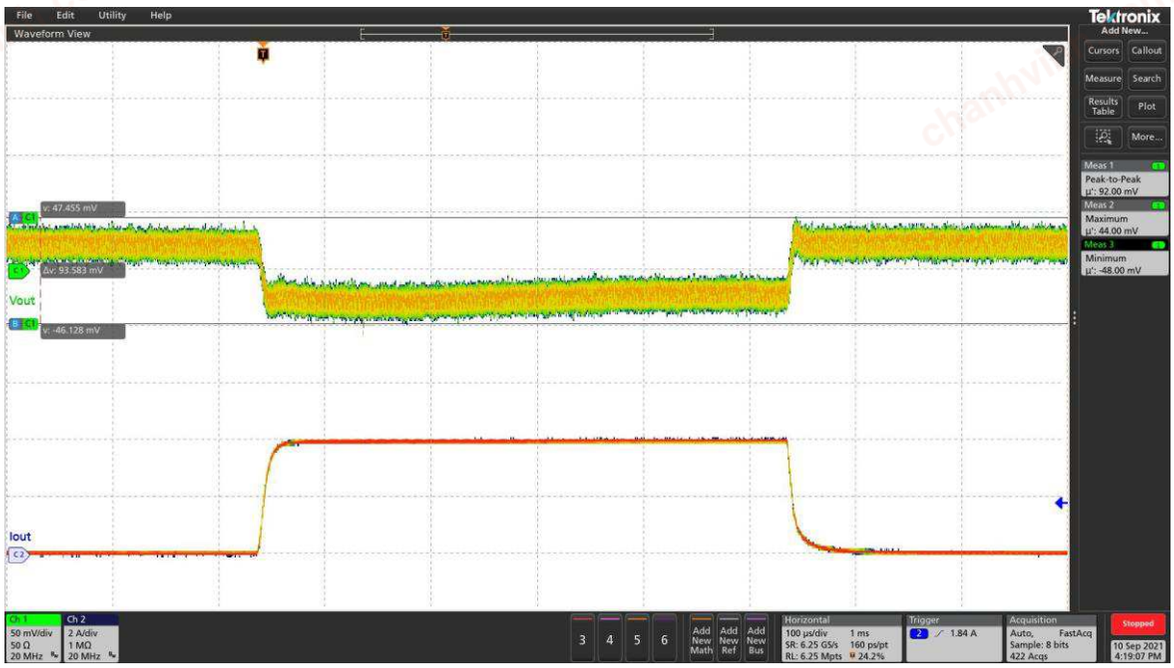


Figure 28 Transient Response, PV_{in} =12V, V_{out} = 3.3V, I_{out} = 0A to 4A, FCCM. C_{H1} = V_{out}, C_{H2} = I_{out}. Slew rate = 5A/μS.

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6 Marking Information

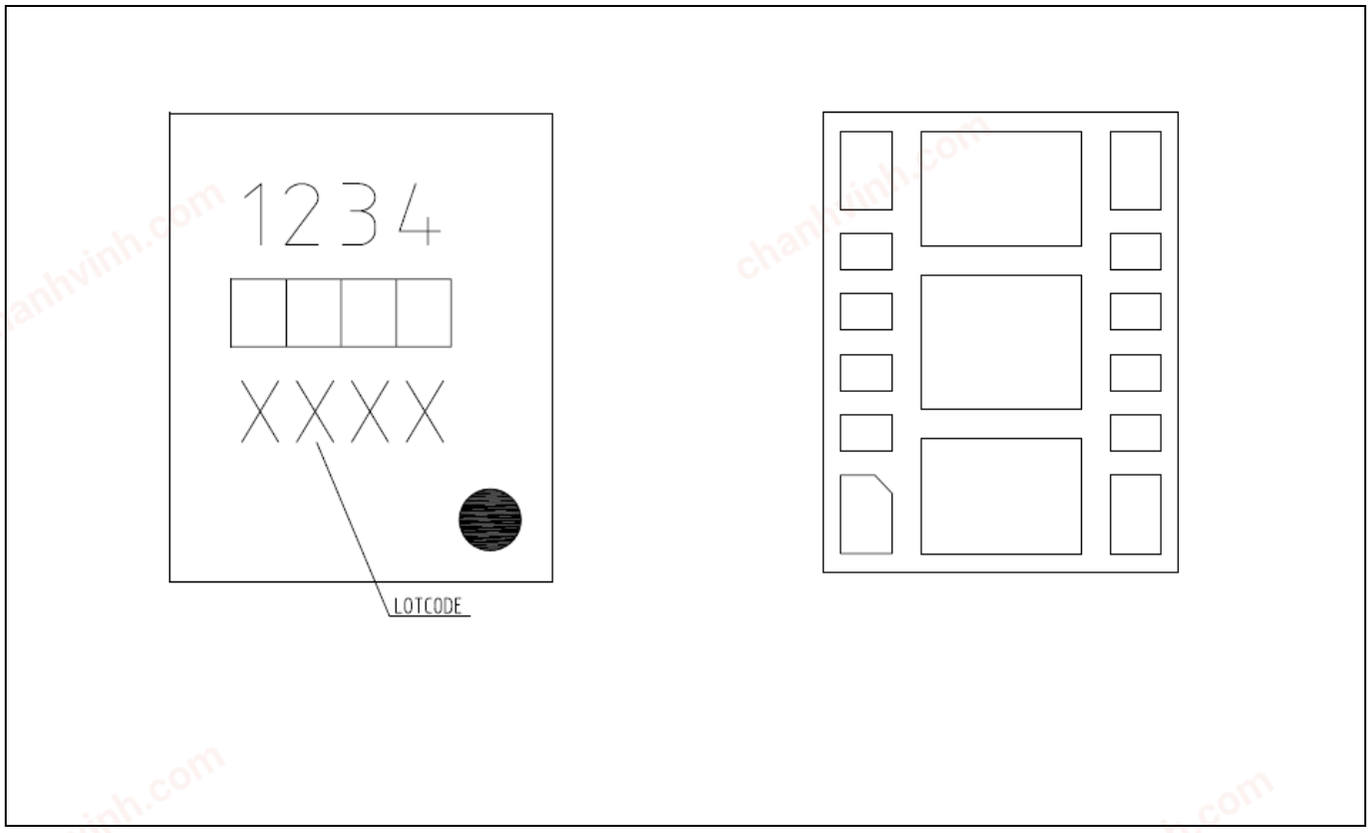


Figure 29 Package Marking, Left (Front side), Right (Rear side)

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7 Tape and Reel Information

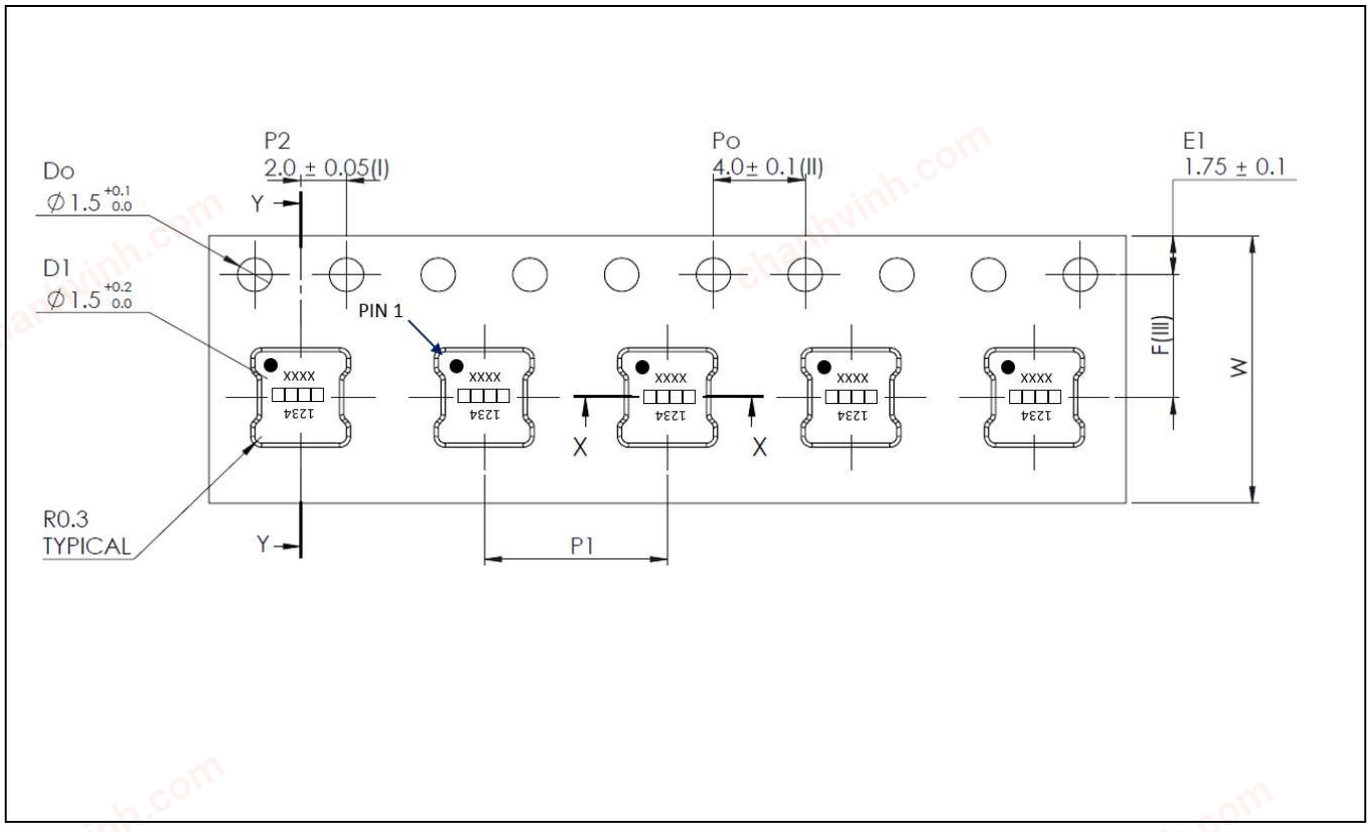


Figure 30 Pin 1 orientation in the tape

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8 Mechanical Pad Drawing

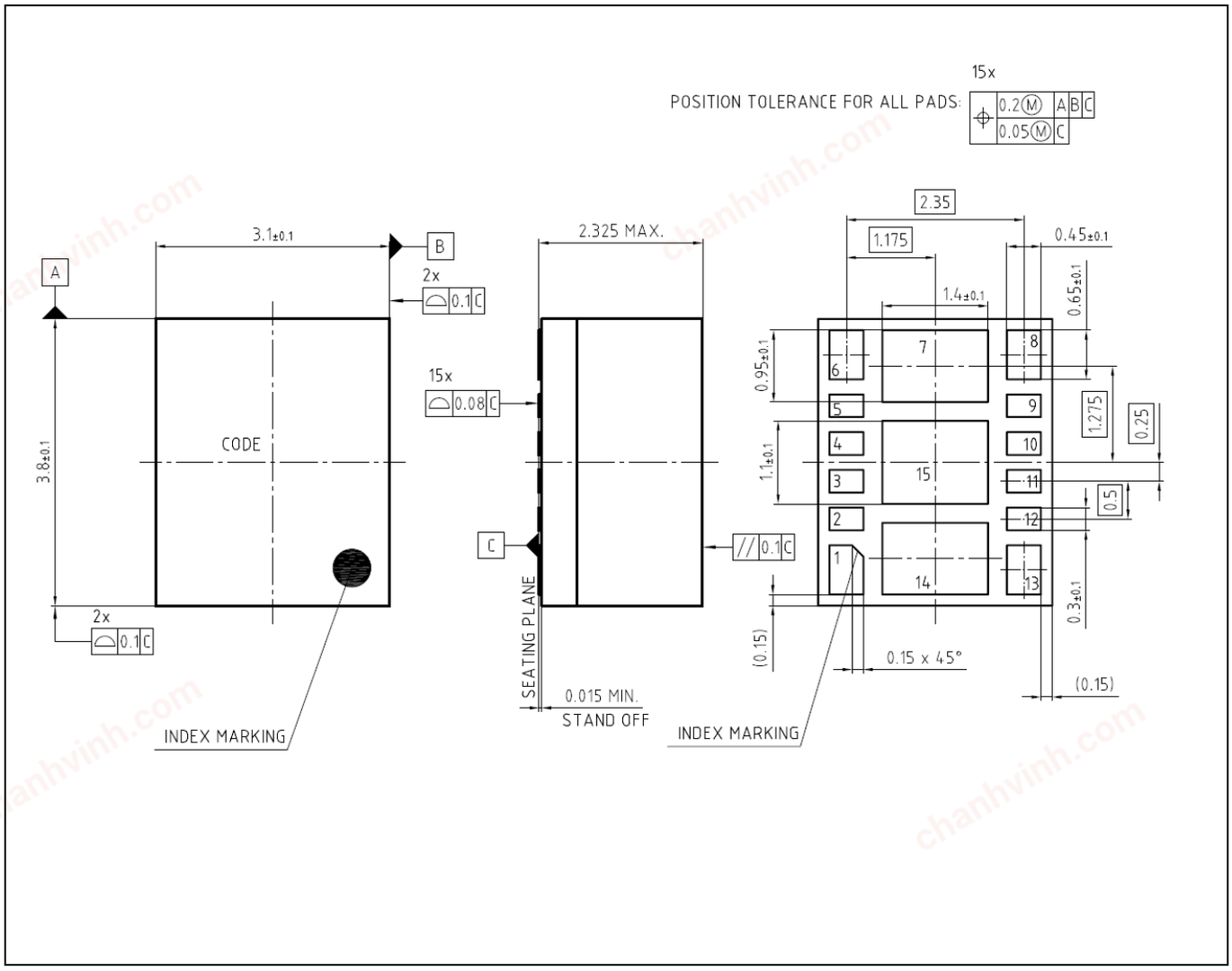


Figure 31 Mechanical Pad Drawing (all dimensions in mm), Tolerances are as per ISO 2768-mK.

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9 PCB Metal and Component Placement

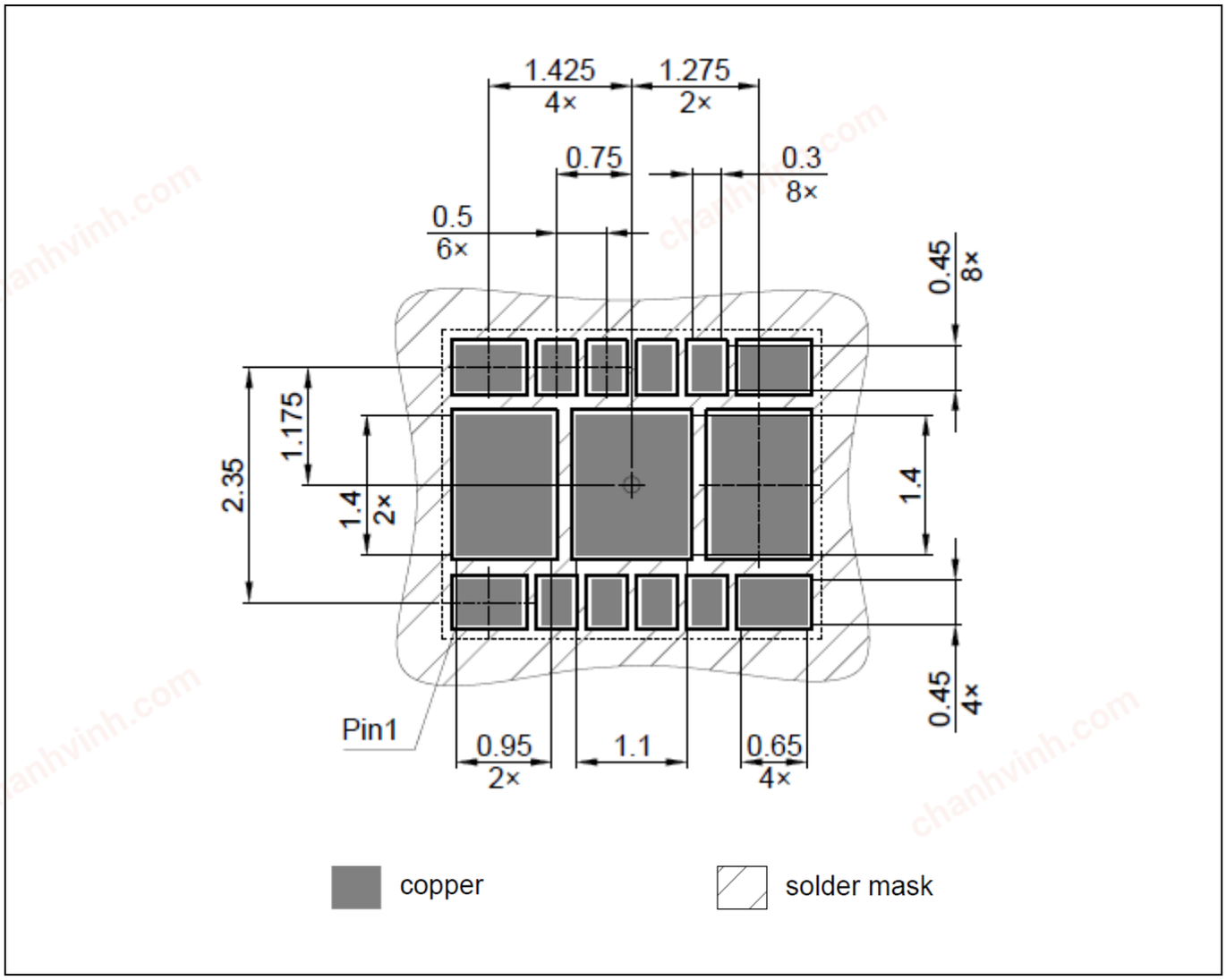


Figure 32 PCB Metal Pad Sizing and Spacing (all dimensions in mm)

9.1 Reflow guideline

Infineon does not recommend specific reflow profiles for our products. Multiple factors influence the reflow profile: PCB size, thermal mass of the board, layers, copper thickness, etc. The optimum reflow profile should be generated initially by referring to the solder paste manufacturer's technical datasheet, and then should be further optimized for the assembly.

For Maximum reflow temperature and time according to J-STD-020 standard, please refer to the reflow soldering section in the following application note.

For further information, please refer to "Recommendations for Board Assembly of Infineon Packages with Land Grid Array Configuration" application note.

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10 Stencil Design

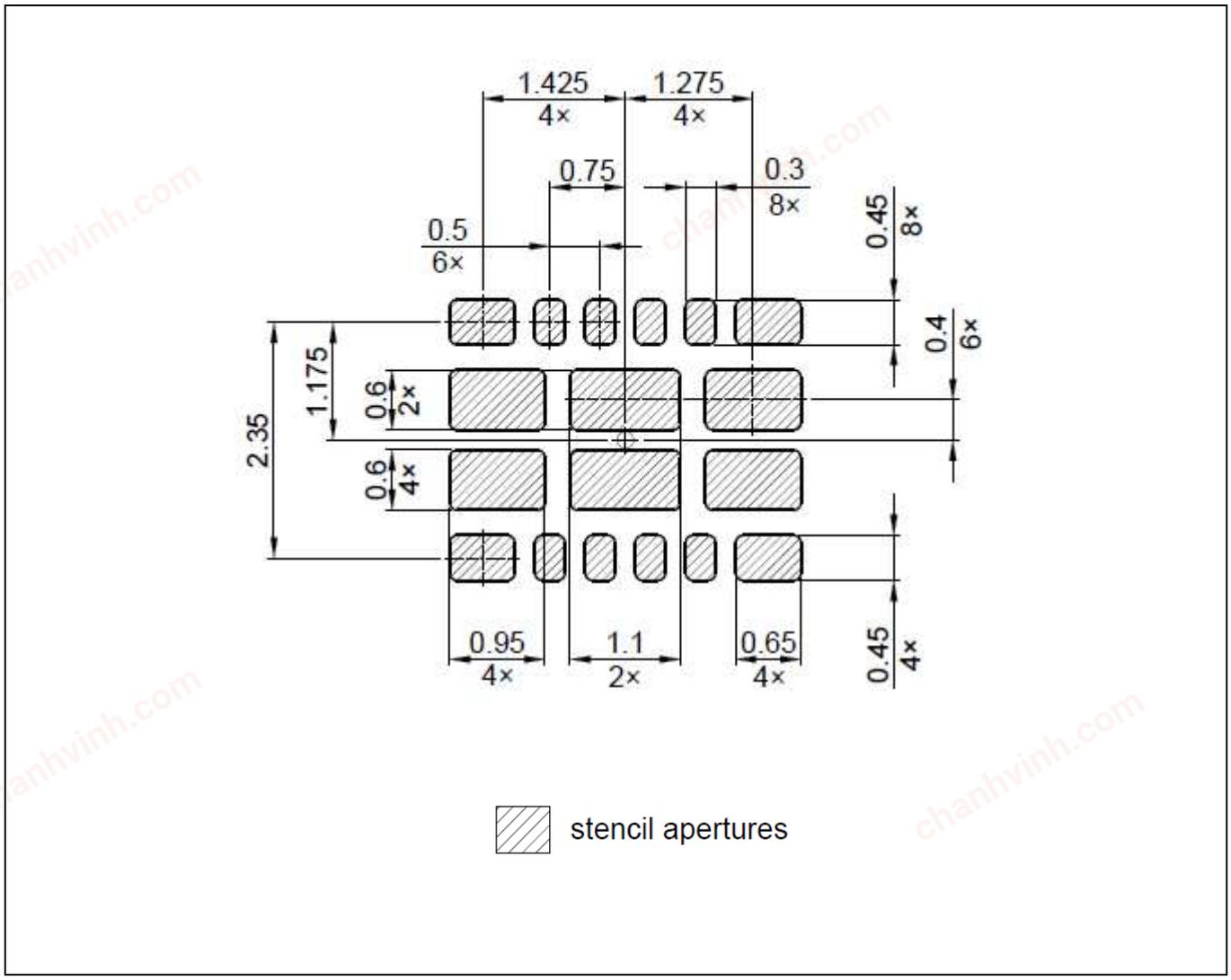


Figure 33 Stencil Pad Spacing (all dimensions in mm)

Note:

11. *Contact Infineon Technologies to receive an electronic PCB Library file in your preferred format.*
12. *This evaluation board is not according to the JEDEC standard. Evaluation Board Description: DB310 REV5B - The PCB is a six-layer board (40 x 40 mm) using FR4 material. Top and bottom layers use 0.5 oz. base copper plus 1.5 oz. plating. Inner layers use 2 oz. copper. The PCB thickness is 1.57 mm. Layer stack-up is top – GND1 – GND2 – signal – GND3 – bottom.*

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11 Layout Recommendations

The pinout of TDM3885 makes it easy to route the PCB layout. General PCB design guidelines should be followed to achieve the best performance.

- Bypass capacitors, including input/output capacitors and Vcc bypass capacitor, should be placed as close as possible to the corresponding pins.
- SW node area should be minimized and be limited to the top layer only.
- Output voltage should be sensed with a separate trace directly from the output capacitor. The sensing trace should be away from the inductor and SW node to avoid interference from switching noise.
- The exposed pad can be connected to the power ground plane through via holes to aid thermal dissipation.
- Wide copper polygons are best practice for input and output power connections. This provides power loss reduction and improved thermal performance. Sufficient via holes should be used to connect the power traces between different layers.

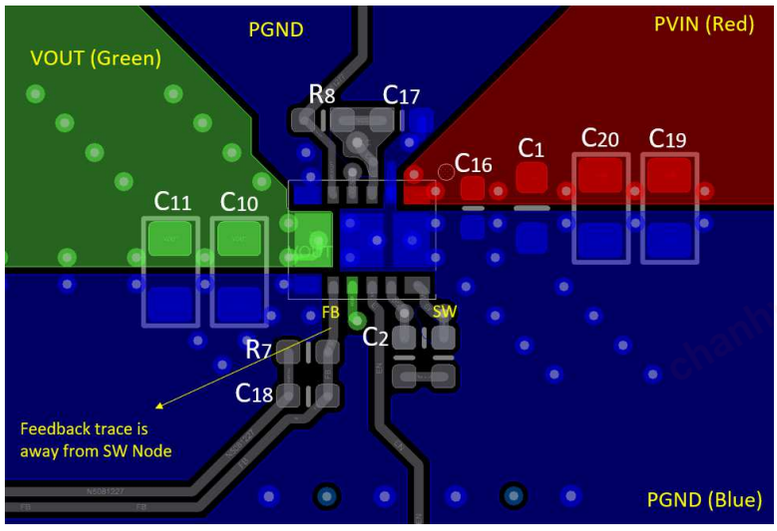


Figure 34 Demo Board Layout – Top layer

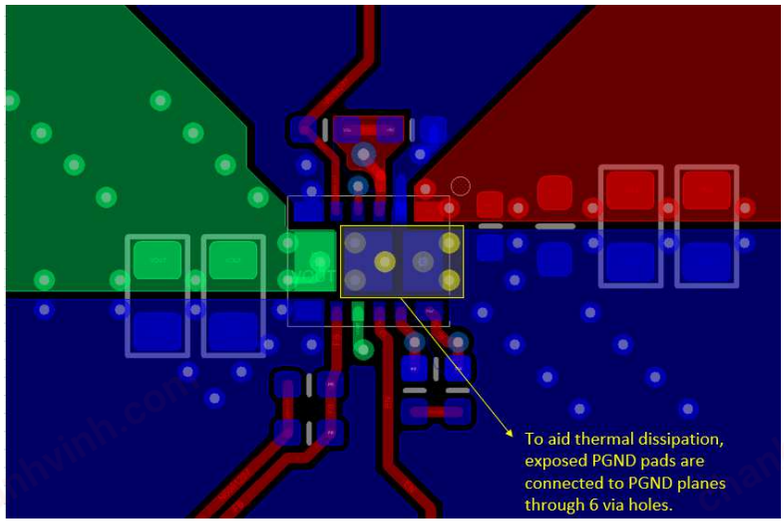


Figure 35 Demo Board Layout – PGND pads

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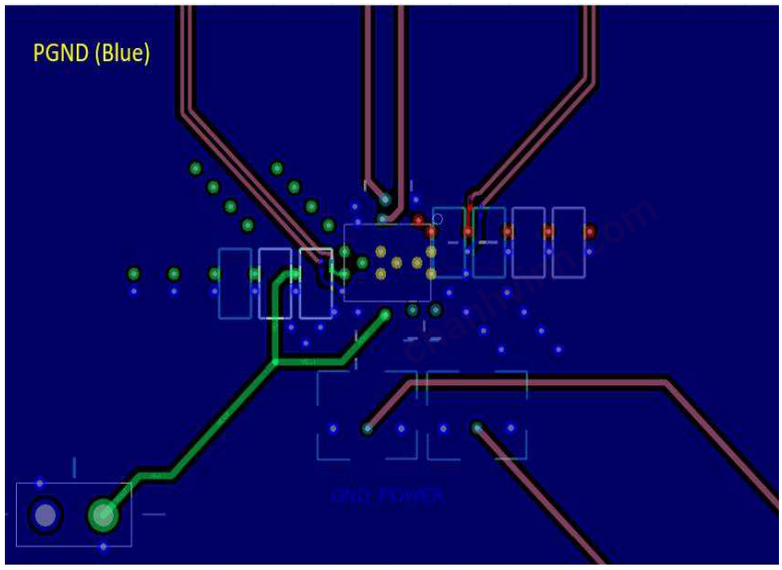


Figure 36 Demo Board Layout – Signal layer

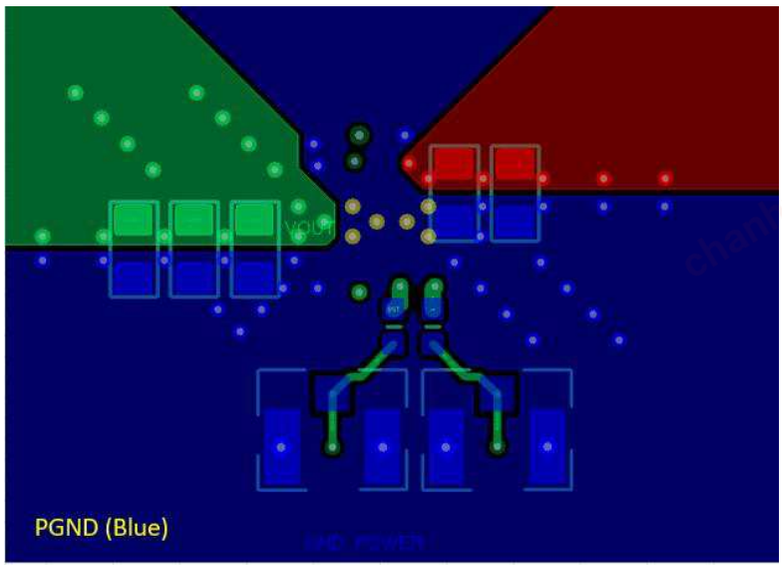


Figure 37 Demo Board Layout – Bottom layer

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12 Environmental Qualifications

Table 7 Environmental Qualifications

Qualification Level		**Industrial**	
Moisture Sensitivity Level		3.1 mm x 3.8 mm PG-LGA-15-2	JEDEC Level 3 @ 260 °C
ESD	[HBM] Human Body Model	ANSI/ESDA/JEDEC JS-001, Class 2, (2000V to <4000V)	
	[CDM] Charge Device Model	ANSI/ESDA/JEDEC JS-002, Class C2A (500 to <750)	
RoHS6 Compliant		Yes	

† Qualification standards can be found at Infineon Technologies web site: www.infineon.com

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13 Evaluation Board and Support Documentation

Table 8 TDM3883 Evaluation Boards and User Guides

Evaluation board	Specifications	Website Address
EVAL_TDM3883_3.3Vout	12 V±10%, 3.3 V, 4 A	www.infineon.com/eval-tdm3885-3.3vout

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Revision History

TDM3885

Revision: 2022-07-20, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-03-09	Initial release
2.1	2022-04-29	(1) Table 3, update Rth_JA = 40.5 °C/W, Psi_JT = 8.0°C/W, Psi_JB = 12.0°C/W. (2) Update section 5.3 title, and table 6: Cff, Cout_min and Cout_max. (3) Add section 9.1, Reflow guideline.
2.2	2022-07-06	Ordering information update. Tape & reel qty = 2500 units.
2.3	2022-07-20	Fix page footer typo.

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