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1 Description

- High frequency, low profile DC-DC converters;
- Voltage Regulators for DDR memory arrays, and low current voltage rails;

The TDA21520 integrated power-stage contains a low quiescent current synchronous buck gate-driver IC which is co-packed with control and synchronous MOSFETs along with an active diode structure that achieves low Vsd similar to a schottky with very little reverse recovery charge. The package is optimized for PCB layout, heat transfer, driver/MOSFET control timing, and minimal switch node ringing when layout guidelines are followed. The paired gate driver and MOSFET combination enables higher efficiency at lower output voltages.

The internal MOSFET sensing achieves superior current sense accuracy vs. best-in-class controller-based Inductor DCR sense methods.

Protection includes IC temperature reporting and over temperature protection feature (OTP with thermal shutdown), cycle-by-cycle over current protection (OCP), control MOSFET short detection (HSS - High side short detection), VDRV and bootstrap under-voltage protection. The TDA21520 also features "refreshing" of bootstrap capacitor to prevent the bootstrap capacitor from over-discharging.

Operation of up to 1.5 MHz switching frequency enables high performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry leading efficiency.

Features

- Integrated driver, active diode, high-side MOSFET and low-side MOSFET
- Input voltage range of 4.25 V to 16 V
- VCC supply of 4.25 V to 5.5 V
- Output voltage range from 0.225 V up to 5.5 V
- Output current capability of 20 A
- Operation up to 1.5 MHz
- VCC under voltage lockout (UVLO)
- Bootstrap under voltage protection
- On-chip MOSFET current sensing and reporting with 5 µA/A gain
- Over temperature protection and thermal shutdown
- Cycle-by-cycle over current protection and flag
- High-side MOSFET short detection and flag
- Auto-replenishment on bootstrap capacitor
- Compatible with 3.3 V tri-state PWM Input
- Auto SLEEP mode after 20 µs of PWM Tri-state (1.7 mA typ)
- DEEP SLEEP mode for power saving via EN= low (32 µA typ)
- Small 4 mm x 5 mm x 0.9 mm PQFN package
- Lead free RoHS compliant package

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Table 1 Product Identification

Part Number	Temp Range	Package	Orderable Part Number
TDA21520	-40 to 125°C	PQFN 4 mm x 5 mm	TDA21520AUMA1

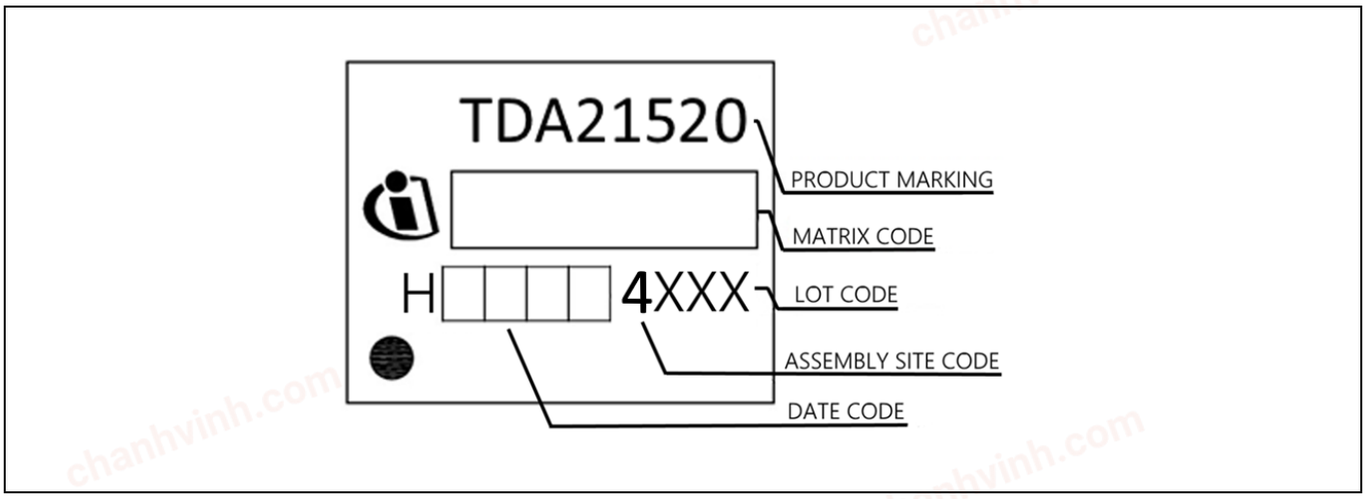


Figure 1 Picture of the Product

2 Description

2.1 Pinout

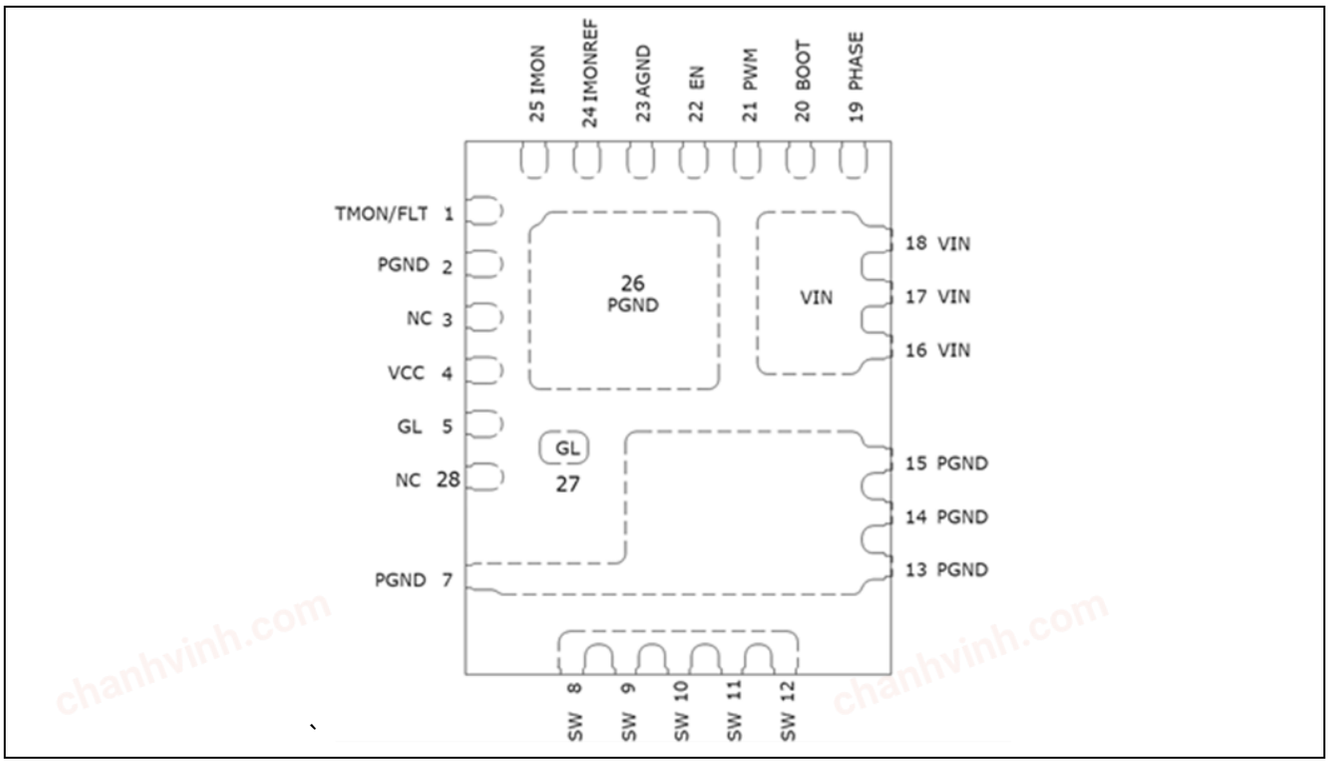


Figure 2 Pinout, Numbering and Name of Pins (transparent top view)

Table 2 I/O Signals

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Description

Pin No.	Name	Pin Type	Buffer Type	Function
1	TMON / FLT	O	Analog	The voltage at this pin is defined by the equation 8mV * (Celsius Temperature) + 0.6 V. This pin will be pulled up to 3.3 V under severe over-temperature, over-current, high-side MOSFET short or Bootstrap under voltage condition.
5, 27	GL	I/O	Analog	Low-side MOSFET driver pin that can be connected to a test point in order to observe the waveform.
8, 9, 10, 11, 12	SW	O	Analog	Switching node of synchronous buck converter.
19	PHASE	I	Analog	Switching node. For bootstrap capacitor connection only.
20	BOOT	I	Analog	Bootstrap capacitor connection. Connect an X7R ceramic capacitor with value between 0.22uF to 0.56uF from BOOT to PHASE pin. The bootstrap capacitor provides the charge to turn on the high-side MOSFET.
21	PWM	I/O	+3.3 V logic	3.3 V logic level PWM input. PWM input: “High” turns high-side MOSFET on; “Tri-state” turns both MOSFETs off; “Low” turns low-side MOSFET on.
22	EN	I	+3.3 V logic	Pulling EN high enables the driver; pulling EN low disables the driver and enters ultra-low quiescent current mode. Floating this pin is not recommended, however a pull-down resistor is embedded to keep the driver off if the pin is floating. This pin is VCC tolerant.
24	IMONREF	I/O	Analog	This pin provides a system reference for the IMON information and can be tied to a fixed voltage between 1.1 V and 1.9 V such as bias rails of a PWM controller.
25	IMON	O	Analog	Sensed current output signal proportional to high-/low-side MOSFET currents referenced to the IMONREF pin through an external resistor. V (IMON – IMONREF) voltage across the external resistor represents current information.

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Table 3 Power Supply

Pin No.	Name	Pin Type	Buffer Type	Function
4	VCC	POWER	–	Bias voltage for control logic and supply of gate driver. Connect a 1 uF cap between VCC and PGND. VCC should be connected to +5 V power supply.
16, 17, 18	VIN	POWER	–	4.25 V to 16 V high current input voltage connection.

Table 4 Not Connected

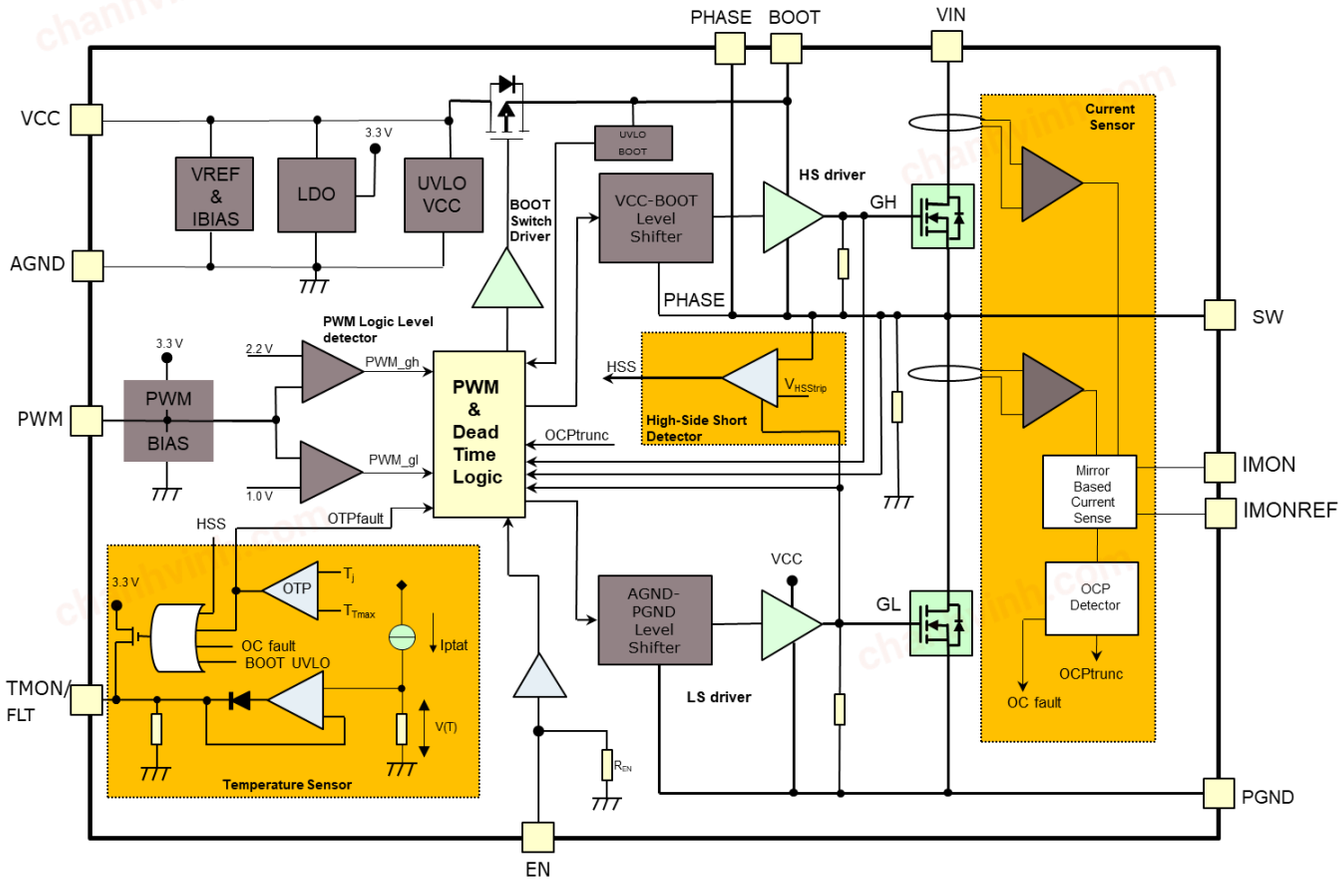
Pin No.	Name	Pin Type	Buffer Type	Function
3	NC	–	–	Leave the pin unconnected.
28	NC	–	–	For internal test only, no PCB pad recommended for this pin

Table 5 Ground Pins

Pin No.	Name	Pin Type	Buffer Type	Function
23	AGND	GND	–	Signal ground. All interface signals are referenced to this pin.
2, 7, 13, 14, 15, 26	PGND	GND	–	Power ground. It is also the power ground of the low-side MOSFET.

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3 Simplified Block Diagram



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4 Electrical Specification

4.1 Absolute Maximum Ratings

Note: T_A = 25 °C

Stresses above those listed in Table 6 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure over values of the recommended ratings for extended periods may adversely affect the operation and reliability of the device.

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency of the PWM input	f_{SW}	0.1	–	1.5	MHz	
Maximum average load current	IMON	–	–	20	A	
Input Voltage	V_{IN}	-0.30	–	25	V	Pin VIN
Logic and driver supply voltage	V_{CC}	-0.3	–	6.5	V	Pin VCC
Switch node voltage	V_{SW} (DC)	-1	–	25	V	Pin SW
	V_{SW} (AC)	-8 for 10ns	–	34 for 1 ns		
PHASE voltage	V_{PHASE} (DC)	-1	–	25	V	Pin PHASE
	V_{PHASE} (AC)	-8 for 10ns	–	34 for 1 ns		
VIN – PHASE voltage	V_{VIN} - V_{PHASE} (DC)	-1	–	25	V	VIN – PHASE
	V_{VIN} - V_{PHASE} (AC)	-8 for 10ns	–	34 for 1 ns		
BOOT voltage	V_{BOOT} (DC)	-0.3	–	29	V	Pin BOOT
	V_{BOOT} (AC)	Below -0.3V for 5ns	–		V	
	$V_{BOOT-PHASE}$	-0.3	–	6.5V (DC), 7.5V for 3ns		
GL voltage	V_{GL}	-0.3	–	6.5	V	Pin GL
EN voltage	V_{EN}	-0.3	–	6.5	V	Pin EN
PWM voltage	V_{PWM}	-0.3	–	4.0	V	Pin PWM
TMON voltage	V_{TMON}	-0.3	–	3.6	V	Pin TMON / FLT
IMON voltage	V_{IMON}	-0.3	–	3.6	V	Pin IMON
IMONREF voltage	$V_{IMONREF}$	-0.3	–	3.6	V	Pin IMONREF
NC pin 28 voltage	V_{28}	-0.3	–	0.3	V	Pin 28
Junction temperature	T_{Jmax}	-40	–	150	°C	–
Storage temperature	T_{STG}	-55	–	150	°C	–

Note: All rated voltages are relative to voltages on the AGND and PGND pins unless otherwise specified.

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4.2 Thermal Characteristics

Table 7 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance-Junction to PCB (pin 15)	θ_{JC_PCB}	–	2.3	–	K/W	–
Thermal resistance-Junction to top of package	θ_{JC_Top}	–	22.2	–		–
Thermal resistance to ambient	θ_{JA} Note	–	21.5	–		–

Note: Thermal Resistance (θ_{JA}) is measured with the component mounted on a high effective thermal conductivity test board in free air.

4.3 Recommended Operating Conditions

Table 8 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	4.25	–	16	V	–
Logic and driver supply voltage	V_{CC}	4.25	–	5.5	V	–
Frequency of the PWM	f_{sw}	100	–	1500	KHz	-
EN voltage	V_{EN}	–	–	5.5	V	Pin EN
PWM voltage	V_{PWM}	–	–	3.6	V	Pin PWM
Current Sense reference voltage	$V_{IMONREF}$	1.1	–	1.9	V	Pins IMON, IMONREF
Junction temperature	T_{jOP}	-40	–	+125	°C	–

4.4 Electrical Characteristics

Note: Typical values represent the median values, which are related to 25°C,V_{CC} = 5 V, $V_{IMONREF}$ = 1.2V

Table 9 Voltage Supply, Biasing Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO VCC rising	V_{UVLO_R}	-	4.05	-	V	
UVLO VCC falling	V_{UVLO_F}	–	3.85	–		
Bootstrap Under-voltage rising threshold	V_{UVBOOT_R}	–	3.82	–		
Bootstrap Under-voltage falling threshold	V_{UVBOOT_F}	–	3.61	–		
Supply Current	I_{Vcc}	-	22	-	mA	EN = H, f_{SW} = 600 kHz, D=10%
		–	1.6	–	mA	EN = H, PWM floating
		–	35	–	µA	EN = L
VIN Current	I_{VIN}	–	-	1	nA	No switching, EN = L

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Table 10 Current Sense

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
IMON	IMON Voltage range	V_{IMON}	0.8	–	2.35	V	DC + AC components
	IMONREF reference voltage range	V_{IMON_CM}	1.1	–	1.9	V	Reference Voltage connected externally for the current sense signal
	Current sense gain	A_{cs}	–	5	–	µA/A	
	IMON Gain resistor range	R_{IMON}	-	1	-	kΩ	Resistor to be connected between IMON and IMONREF. For 5mV/A, recommended 1kΩ R_{IMON}

Table 11 Temperature Sense and FLT Communication

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TMON / FLT	Temperature Sense Slope	$A_{TMPGAIN}$	-	8.0	-	mV/°C	25°C ≤ T_J ≤ 125°C, Note 1
	Temperature Sense Offset Voltage	$V_{TMPOFFSET}$	-	800	-	mV	T_J = 25°C, 0.6 V + 8 mV/°C * T_J

Table 12 Other Logic Functions, Inputs/Outputs And Thresholds

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
EN	Input High Voltage	V_{EN_H}	2.0	–	–	V	
	Input Low Voltage	V_{EN_L}	–	–	0.8	V	
	Enable Power-on Delay	$t_{EN_ondelay}$	–	17	-	µs	PWM=0. Measured from EN rising edge to V_{GL}> 1 V. Note 1
	Enable Power-off Delay	$t_{EN_offdelay}$	–	-	1	us	PWM=0. Measured from EN falling edge to V_{GL} < 4 V. Note 1
	Internal Pull down Resistance	R_{PULLDN_EN}	210	280	340	kΩ	When EN is floating
PWM	PWM Input High Threshold	V_{IH}	2.4	–	–	V	PWM Low or Tri-state to High
	PWM Input Low Threshold	V_{IL}	–	–	0.8	V	PWM High or Tri-state to Low
	PWM Hysteresis	I_{PWM_HYS}	–	40	–	mV	Active to Tri-state or Tri-state to Active

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Table 13 Protection

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
OTP	Over Temp Rising Threshold	T_{RISE}	–	140	–	°C	TMON/FLT pulled up high Note 1
	Over Temp Falling Threshold	T_{FALL}	–	128	–	°C	TMON/FLT released Note 1
HSS FLT	High-side MOSFET Short Threshold	V_{HSS_TH}	-	560	-	mV	$V_{SW} – V_{PGND}$
	TMON/FLT Delay	T_{HSS_DEL}	–	150	–	ns	After V_{HSS_TH} is detected and TMON/FLT is pulled high
OCP	Over-Current Threshold	I_{OCP_TH}	–	36	–	A	
	Over-Current Delay	T_{OCP_DEL}	10	–	–	Cycle	PWM High-Low Cycles to TMON/FLT is pulled high

Notes

1. Guaranteed by design but not tested in production

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5 Typical operating conditions

Single Phase Circuit of Figure 18, V_{IN} = 12 V, V_{OUT} = 1 V, f_{SW} = 600 kHz, L = 120 nH, VCC = VDRV = 5 V, $T_{AMBIENT}$ = 25 °C, no heat sink, no air flow, 8-layer PCB board of 3.7”(L) x 2.6”(W), no PWM controller loss, no inductor loss, unless specified otherwise.

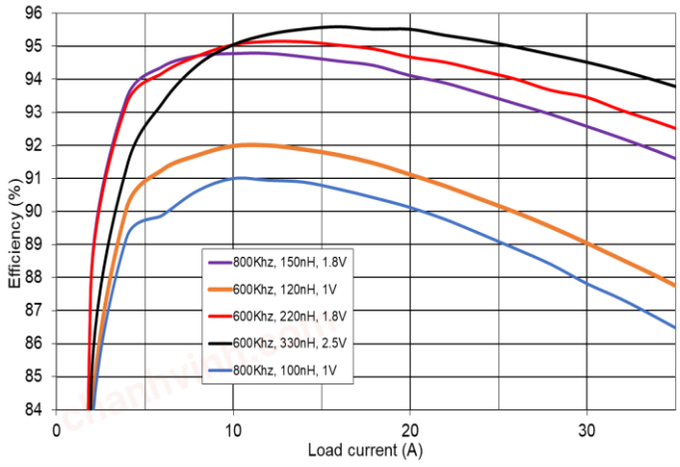


Figure 3 Powerstage Efficiency

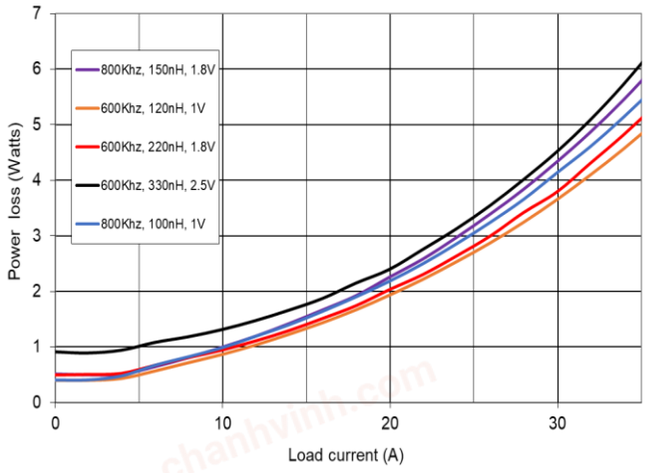


Figure 4 Power stage Loss

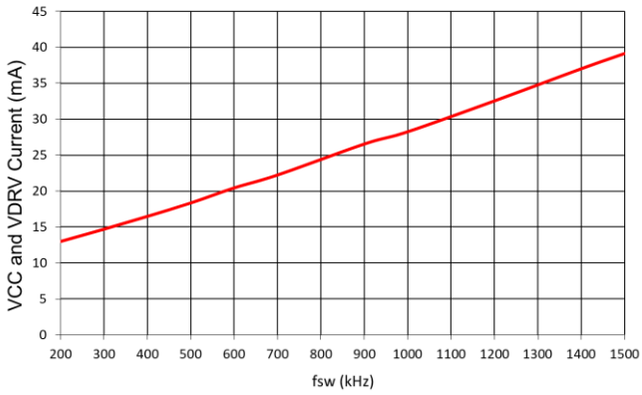


Figure 5 VCC current v/s Frequency

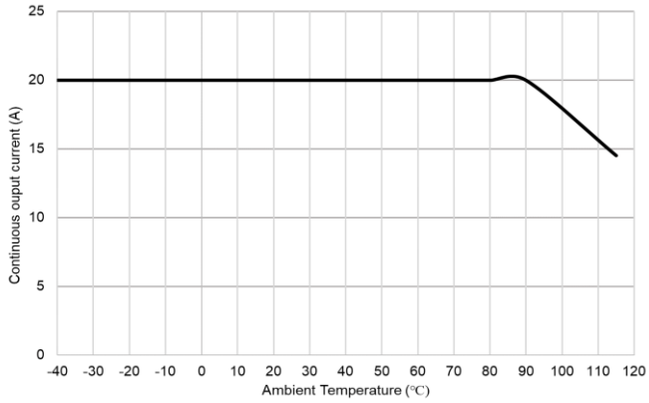


Figure 6 Thermal derating, Tcase <= 125°C

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6 Theory of Operation

6.1 Description

The TDA21520 contains an improved high speed MOSFET driver optimized to drive a pair of co-packaged high-side and low-side OptiMOS MOSFETs at frequency up to 1.5 MHz. Dc-dc controllers using traditional current sense methods like DCR sensing and Rdson sensing typically have limitations. DCR current sensing is sensitive to temperature changes of the inductor and needs temperature compensation either implemented externally using a thermos-couple or inside the power stage. Rdson current sensing, on the other hand, is not dependent on the inductor but there is a temperature co-efficient associated with the MOSFET rdson. Besides, it is difficult to implement rdson current sensing for high-side MOSFET which is therefore replaced by emulated current while the low-side current is sensed across the MOSFET. With the advanced current-mirror sensing in TDA21520, all these limitations are eliminated while achieving superior accuracy. Current on both high-side as well as low-side MOSFET is mirrored on a sense MOSFET which is a part of the main MOSFET device, and hence comes with an inherent temperature compensation without the need for an additional circuitry. Real current-sensing on both MOSFET ensures that the system is always monitoring the real output current and can immediately react to any critical events like load step or over-current fault.

The TDA21520 reports accurate temperature with the gain of 8 mV / °C, which helps the system to actively monitor the temperature in real time. Temperature outputs from multiple power stages can be connected together to report the highest temperature to Infineon’s digital PWM controller.

The TDA21520 PWM input is compatible with industry standard 3.3V PWM input with tri-state.

The TDA21520 can enable Body-Braking mode by responding to PWM tri-state signals sent from the controller, quickly disabling both MOSFETs in the power stage in order to enhance transient performance or provide a high impedance output.

The TDA21520 supports diode emulation mode through the PWM tri-state signal. Controlled by Infineon’s digital PWM controller, the PWM tri-state signal will force the low-side FET to be off when the inductor current is about to go negative. The light-load efficiency then can be increased by preventing conduction loss caused by negative inductor current.

The TDA21520 also supports deep-sleep power saving mode. When in deep-sleep mode, the driver will disable most of the function circuitry to greatly reduce power consumption.

The TDA21520 features a full-range of protection, including VCC/VDRV Under-Voltage-Lockout (UVLO), thermal shutdown against an internal over-temperature condition, phase fault detection of a shorted high-side MOSFET,

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and programmable cycle-by-cycle over-current protection due to an overload condition or saturated output inductor.

The TDA21520 also features internal protection circuitry to automatically replenish the voltage across the bootstrap capacitor. It avoids the gradual depletion of capacitor energy when the power stage sits in tri-state for a long period of time.

6.2 Sleep Modes

When EN is pulled low, the power stage enters deep-sleep mode. The gate driver circuitry will be turned off immediately and most of the logic circuitry will be shut down to reduce the bias current to less than 32 µA. The IMON output will be shorted to IMONREF in deep sleep mode.

When EN toggles from low to high, the power stage will be active and able to accept PWM signals after a delay of 17 µs.

6.3 Current Sensing and Reporting

The TDA21520 features a very accurate current mirror architecture on both high-side as well as low-side MOSFET, thus reporting the real time current information. The current information is reported using the IMON and IMONREF pins. A differential connection between IMON and IMONREF pins is connected to the PWM controller to report the powerstage current information to the controller. The reported current is in the form of current output with the gain of 5µA /A. In order to convert this into voltage, a 1KΩ, 0.1% resistor is recommended to be connected between the IMON and IMONREF pins, close to the controller. The converted voltage signal at the controller side has an effective gain of 5mV/A i.e. for every 1 A load, the controller will read 5mV from the power stage. The current-output differential signal from the power stage provides excellent noise immunity to the reported current information.

6.4 Temperature Sensing, Reporting and Flag

An internal temperature-sense circuit monitors the temperature of the TDA21520. The sensed temperature is reported at the TMON/FAULT pin with a linear voltage slope of 8mV/°C and a 0.6V offset at 0°C, as shown in equation (1).

$$V_{TMON/FAULT}(V) = 0.6V + 0.008V/°C \ x \ T_j(°C) \quad \text{.....(1)}$$

The TMON/FAULT pin also serves as a FAULT pin that is pulled to 3.3V in case of any catastrophic faults and is pulled down to 0V in case of any non-catastrophic faults. When there is no fault, it continues reporting temperature as long as the VCC supply is connected to a voltage in the recommended operating range.

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Once the temperature rises above the OTP rising threshold (140 °C), the TMON/FAULT output will be pulled high immediately, and the driver will stop switching. The HS and LS MOSFETs are tri-stated and driver stops responding to the PWM signal input from the controller. The TMON/FAULT will remain high until temperature falls below the falling threshold (128 °C).

6.5 Over Current Protection and Flag

This feature protects the power stage from self-destruction from repetitive high current events such as saturated inductors due to poor component selection or by incorrectly optimized control loops. These high current events could eventually lead to a shorted high-side MOSFET failure.

With cycle-by-cycle self-preservation, the current is monitored every cycle. If the over-current threshold has been exceeded, the PWM high pulse will be truncated so that the inductor current is allowed to relax. When TDA21520 detects 10 consecutive PWM cycle over-current events, the TMON/FAULT pin is flagged high to indicate the controller of the fault.

6.6 Bootstrap Capacitor Under-Voltage Flag

TDA21520 features a bootstrap capacitor under voltage circuitry that detects a missing bootstrap capacitor before powering up or a damaged bootstrap capacitor during normal operation. Once bootstrap capacitor under voltage is determined (10 Bootstrap undervoltage events), the TMON/FAULT pin will pulled high to report a catastrophic fault to the PWM controller.

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7 Application

7.1 Typical Application

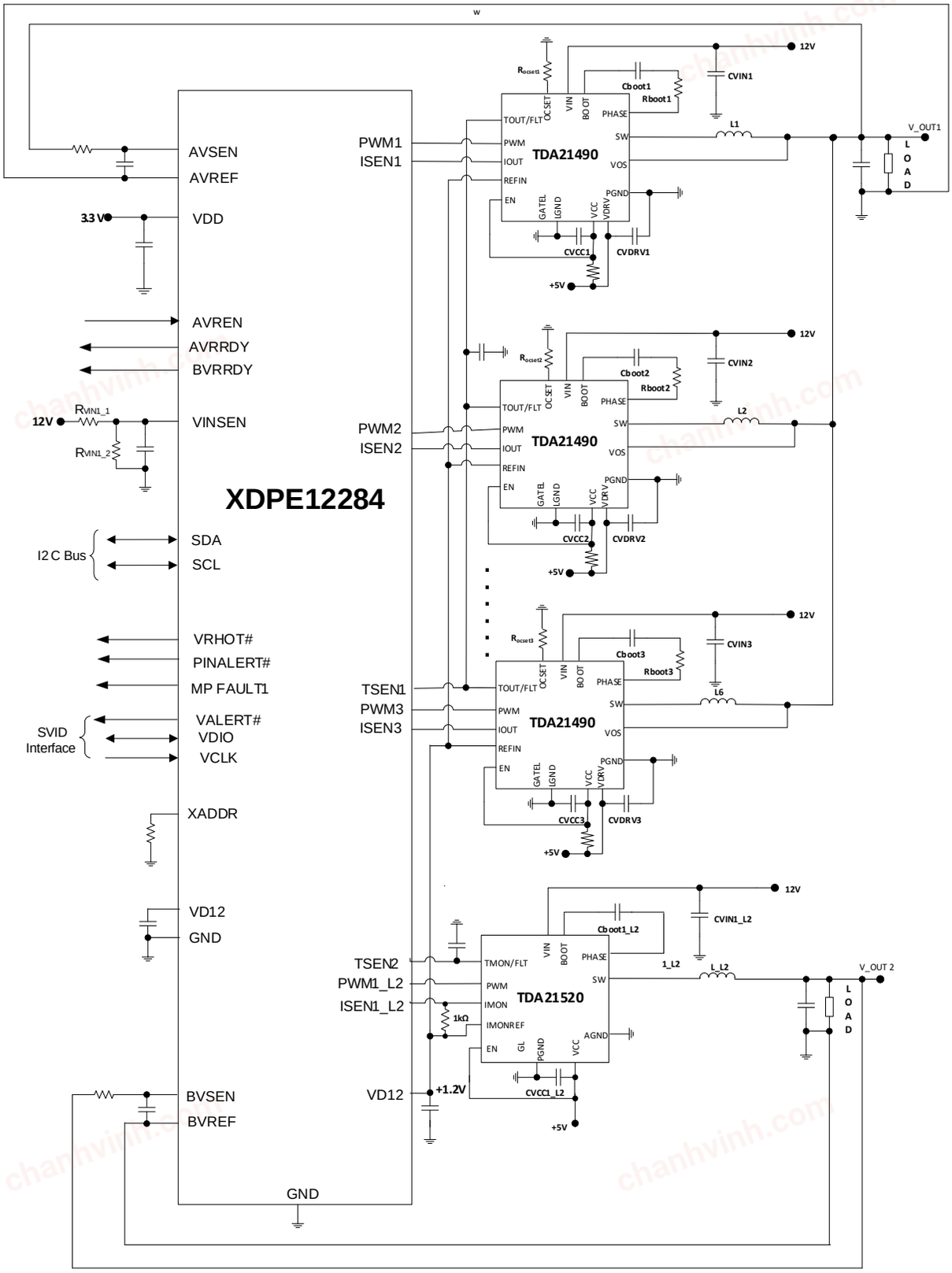


Figure 8 3+1 - Phase Voltage Regulator - Typical Application (simplified schematic)

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8 Mechanical Drawing PQFN

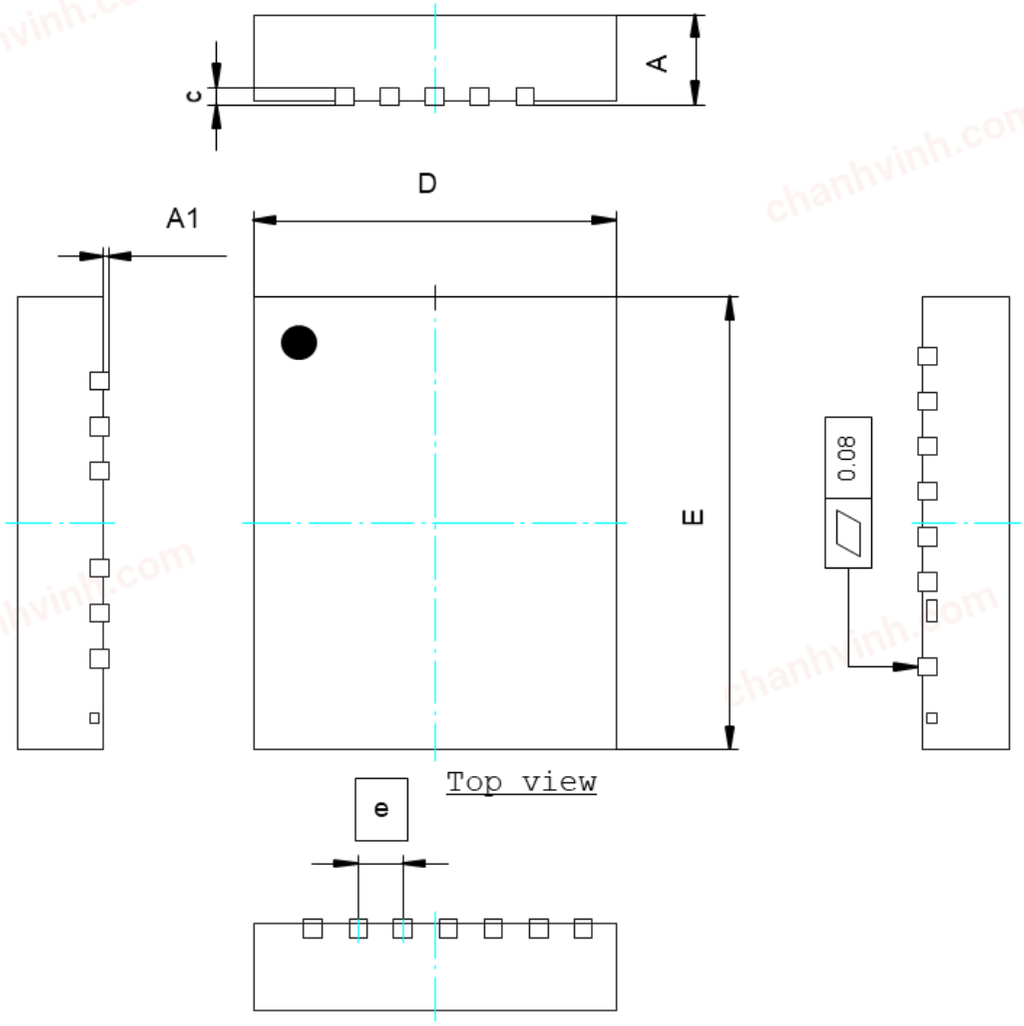
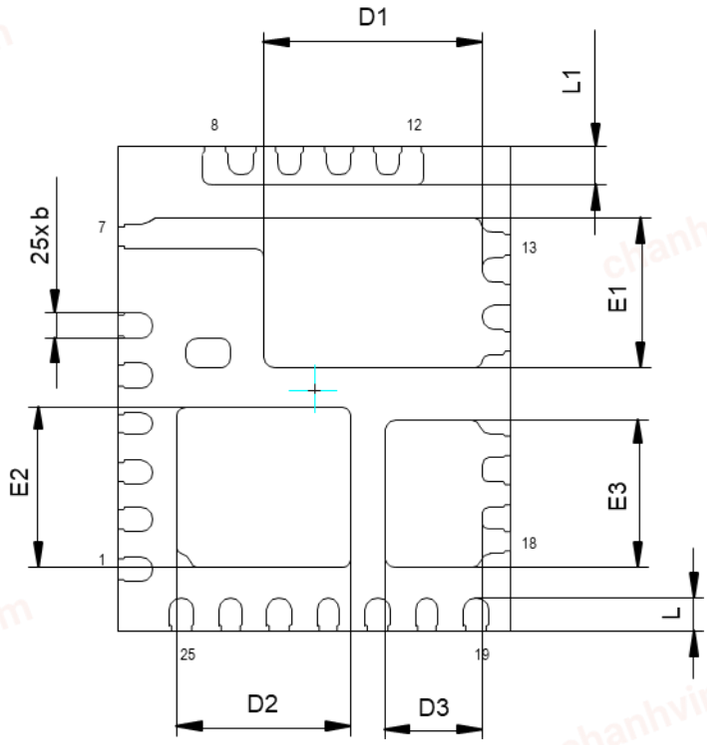


Figure 9 Mechanical Dimensions of Package (Top View and Side View) in mm

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	Millimeters	
DIM	MIN	MAX
A	0.80	1.10
A1	0.00	0.05
b	0.18	0.30
c	0.20	
D	3.90	4.10
E	4.90	5.10
e	0.50 BSC	
D1	2.09	2.29
E1	1.42	1.62
D2	1.68	1.88
E2	1.57	1.77
D3	0.88	1.08
E3	1.42	1.62
L	0.25	0.45
L1	0.30	0.50

Figure 10 Mechanical Dimensions of Package (Bottom View) in mm

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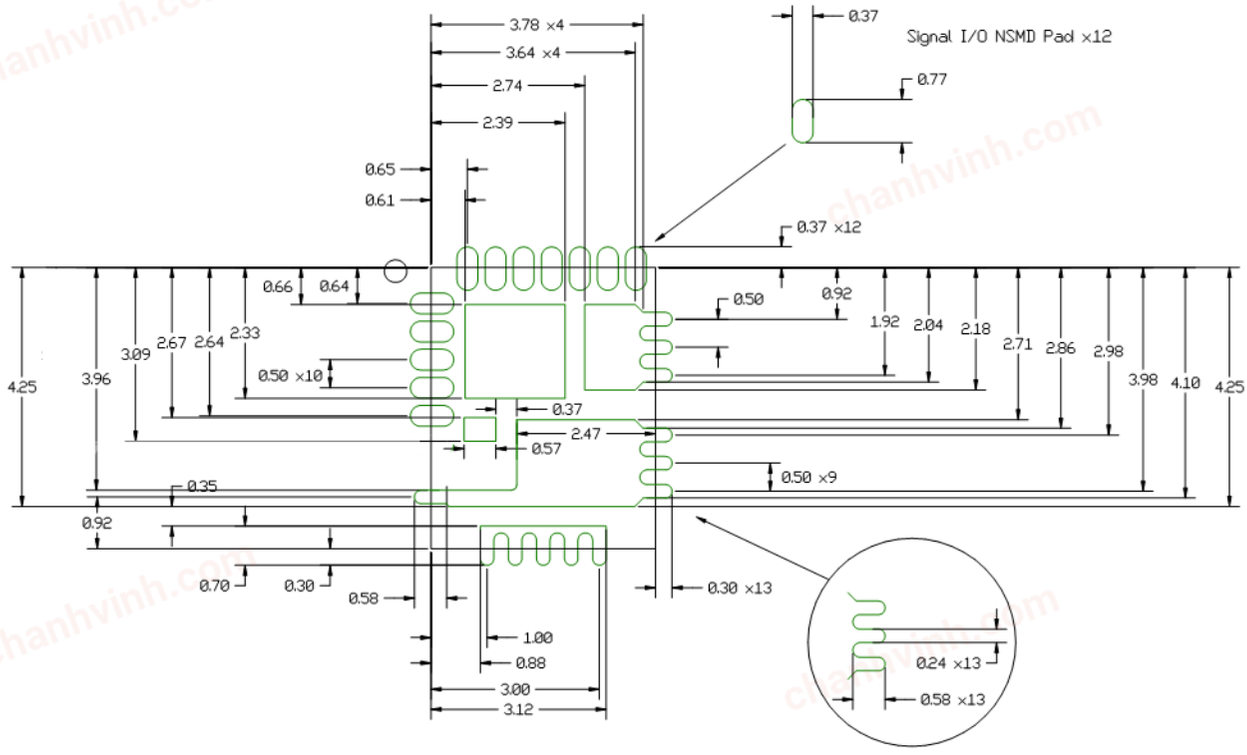


Figure 11 Solder Resist

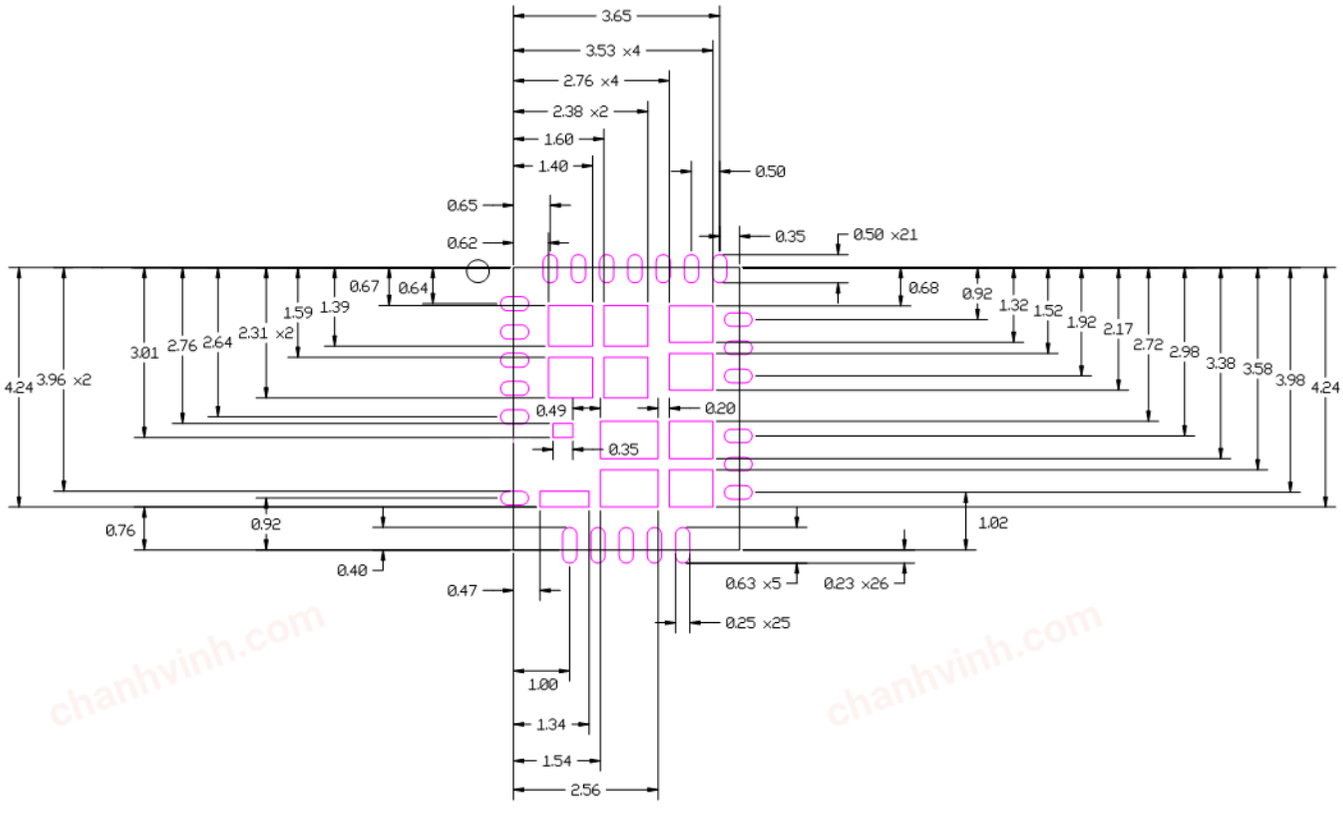


Figure 12 Recommended Stencil Design

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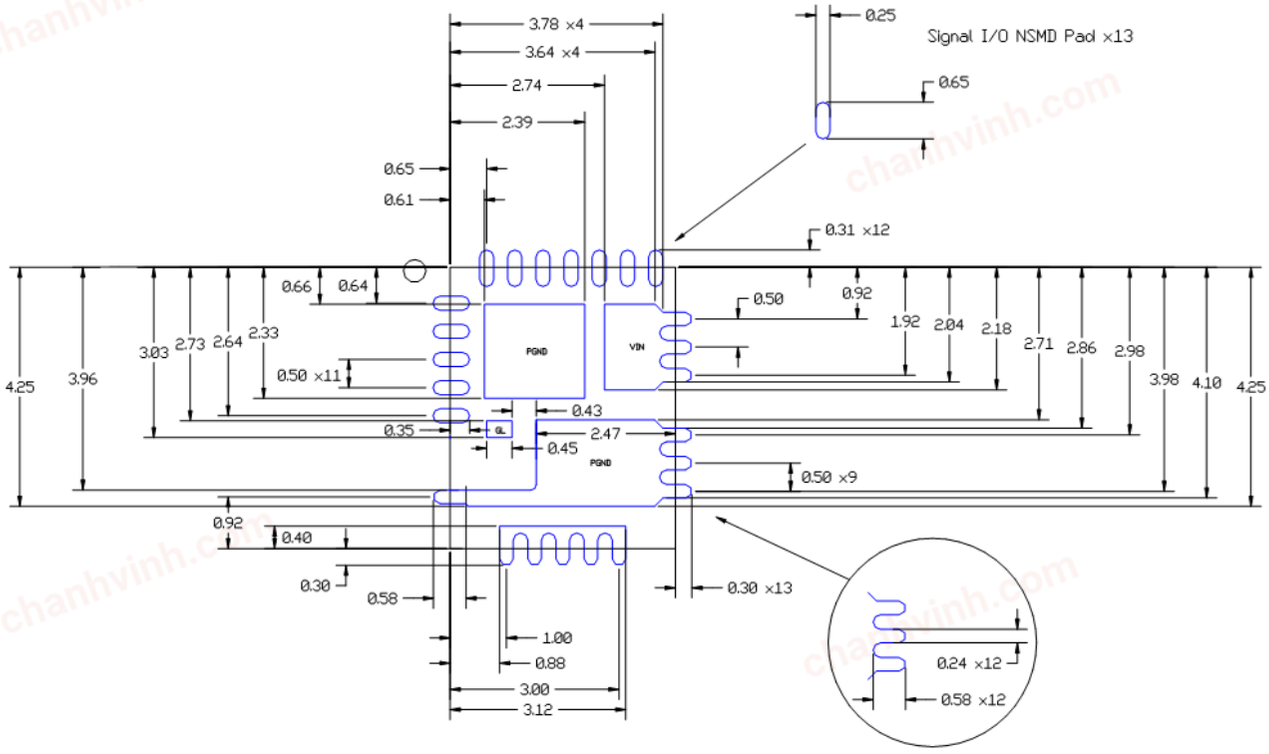


Figure 13 Metal and Component Placement

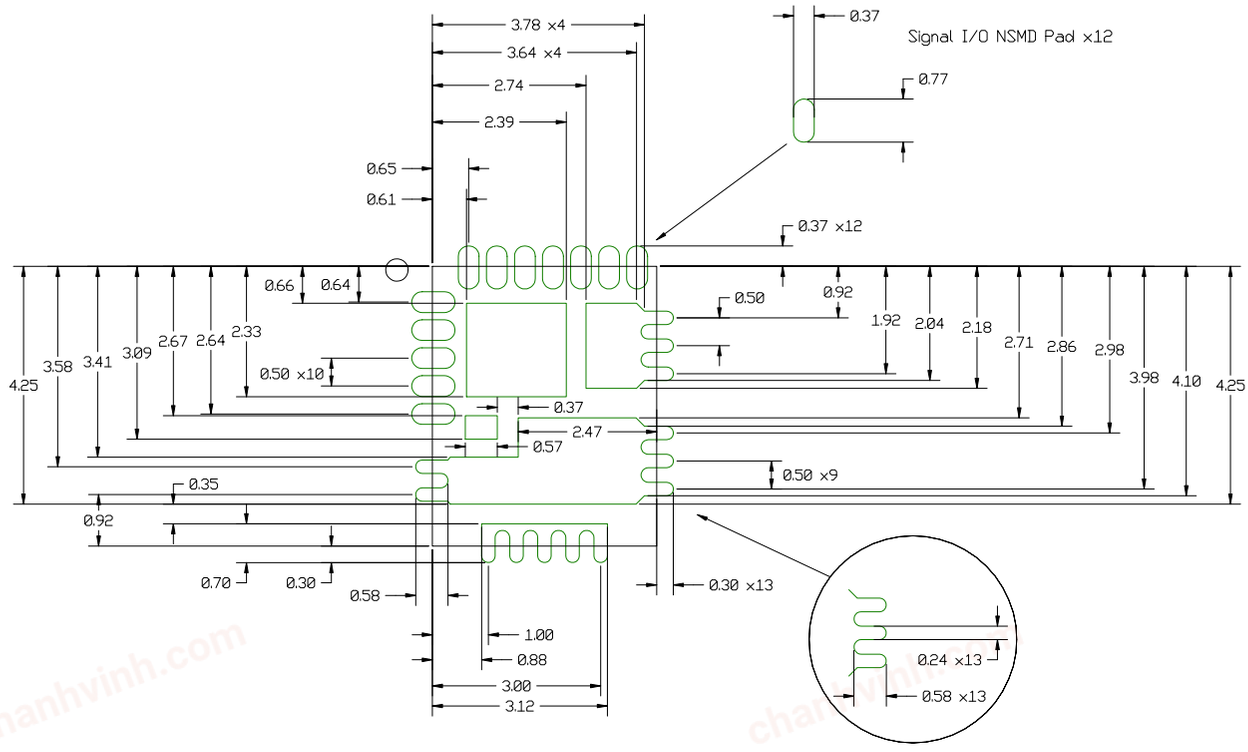


Figure 14 Solder Resist Compatible with IR35401

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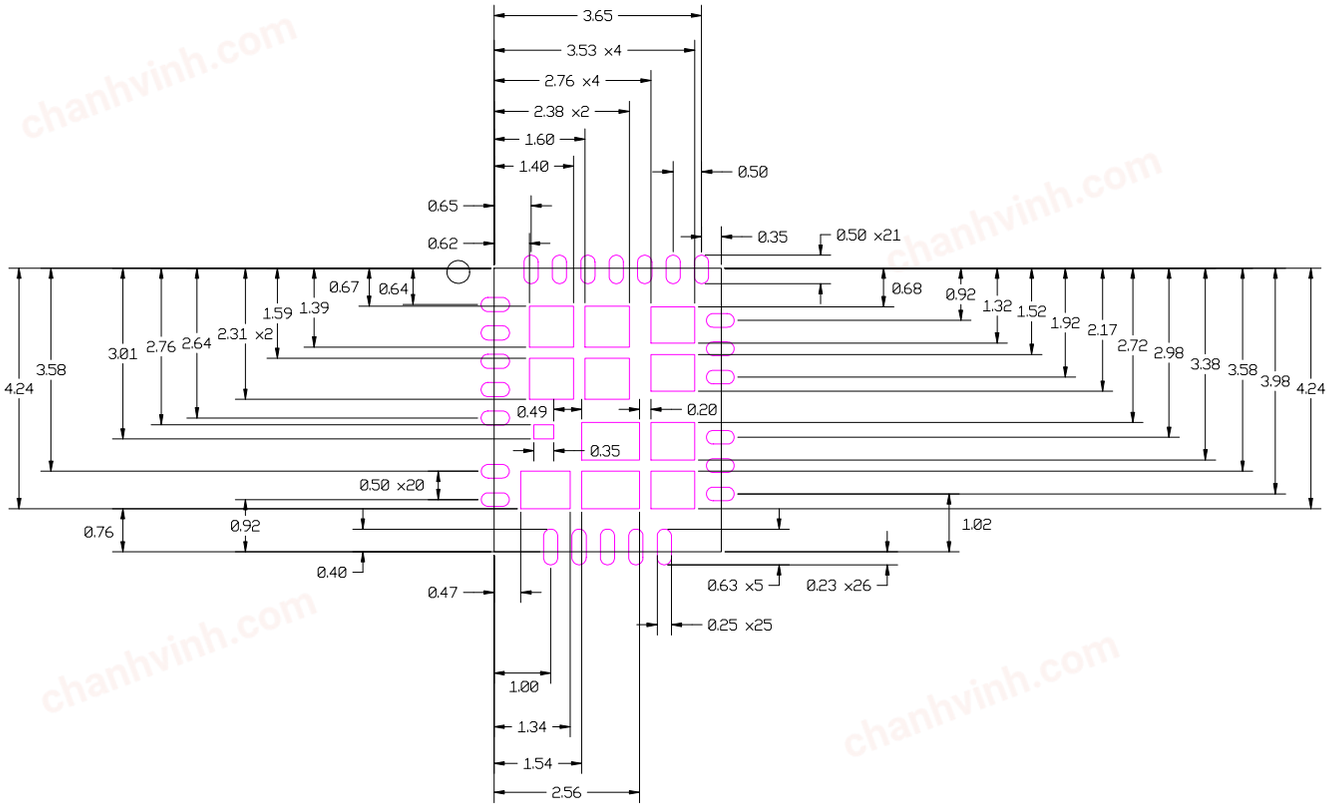


Figure 15 Recommended Stencil Design Compatible with IR35401

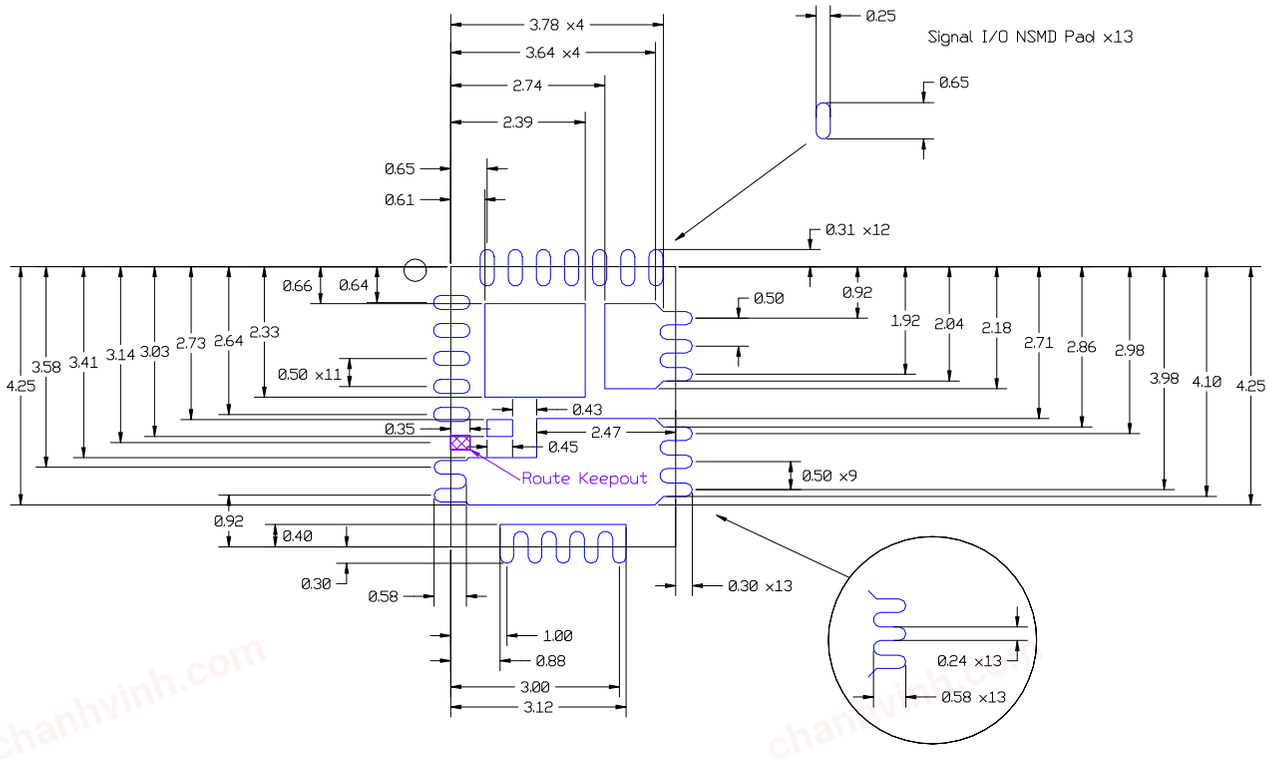


Figure 16 Metal and Component Placement Compatible with IR35401

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