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# 32-Bit

Microcontroller

# TC270 / TC275 / TC277

32-Bit Single-Chip Micocontroller
DC-Step

# 32-Bit Single-Chip Micocontroller

## Data Sheet

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Microcontrollers

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# 1 Summary of Features

The TC27x product family has the following features:

- High Performance Microcontroller with three CPU cores
- Two 32-bit super-scalar TriCore CPUs (TC1.6P), each having the following features:
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - up to 200 MHz operation at full temperature range
  - up to 120 Kbyte Data Scratch-Pad RAM (DSPR)
  - up to 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 8 Kbyte Data Cache (DCACHE)
- Power Efficient scalar TriCore CPU (TC1.6E), having the following features:
  - Binary code compatibility with TC1.6P
  - up to 200 MHz operation at full temperature range
  - up to 112 Kbyte Data Scratch-Pad RAM (DSPR)
  - up to 24 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 8 Kbyte Instruction Cache (ICACHE)
  - 0.125Kbyte Data Read Buffer (DRB)
- Lockstepped shadow cores for one TC1.6P and for TC1.6E
- Multiple on-chip memories
  - All embedded NVM and SRAM are ECC protected
  - up to 4 Mbyte Program Flash Memory (PFLASH)
  - up to 384 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 32 Kbyte Memory (LMU)
  - BootROM (BROM)
- 64-Channel DMA Controller with safe data transfer
- Sophisticated interrupt system (ECC protected)
- High performance on-chip bus structure
  - 64-bit Cross Bar Interconnect (SRI) giving fast parallel access between bus masters, CPUs and memories
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Optional Hardware Security Module (HSM) on some variants
- Safety Management Unit (SMU) handling safety monitor alarms
- Memory Test Unit with ECC, Memory Initialization and MBIST functions (MTU)
- Hardware I/O Monitor (IOM) for checking of digital I/O
- Versatile On-chip Peripheral Units
  - Four Asynchronous/Synchronous Serial Channels (ASCLIN) with hardware LIN support (V1.3, V2.0, V2.1 and J2602) up to 50 MBaud

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  - Four Queued SPI Interface Channels (QSPI) with master and slave capability up to 50 Mbit/s
  - High Speed Serial Link (HSSL) for serial inter-processor communication up to 320 Mbit/s
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - One MultiCAN+ Module with 4 CAN nodes and 256 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - 10 Single Edge Nibble Transmission (SENT) channels for connection to sensors
  - One FlexRay™ module with 2 channels (E-Ray) supporting V2.1
  - One Generic Timer Module (GTM) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One Capture / Compare 6 module (Two kernels CCU60 and CCU61)
  - One General Purpose 12 Timer Unit (GPT120)
  - Three channel Peripheral Sensor Interface conforming to V1.3 (PSI5)
  - Peripheral Sensor Interface with Serial PHY (PSI5-S)
  - Optional Inter-Integrated Circuit Bus Interface (I2C) conforming to V2.1
  - Optional IEEE802.3 Ethernet MAC with RMII and MII interfaces (ETH)
- Versatile Successive Approximation ADC (VADC)
  - Cluster of 8 independent ADC kernels
  - Input voltage range from 0 V to 5.5V (ADC supply)
- Delta-Sigma ADC (DSADC)
  - Six channels
- Digital programmable I/O ports
- On-chip debug support for OCDS Level 1 (CPUs, DMA, On Chip Buses)
- multi-core debugging, real time tracing, and calibration
- four/five wire JTAG (IEEE 1149.1) or DAP (Device Access Port) interface
- Power Management System and on-chip regulators
- Clock Generation Unit with System PLL and Flexray PLL
- Embedded Voltage Regulator

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### Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC270 / TC275 / TC277 please refer to the **“AURIX TC27x Microcontrollers Variant Overview”**, which summarizes all available variants.

**Table 1-1 Overview of TC27x Functions**

| Feature | | |
|---|---|---|
| CPU Core | Type | TC1.6P / TC1.6E |
| | P Cores / Checker Cores / E Cores / Checker Cores | 2 / 1 / 1 / 1 |
| | Max. Freq. | 200 MHz |
| | FPU | yes |
| Program Flash | Size | 4 Mbyte |
| Data Flash | Size | 384 Kbyte |
| Cache | Instruction (P / E) | 16 Kbyte / 8 Kbyte |
| | Data (P / E) | 8 Kbyte / - |
| SRAM | Size TC1.6P (DSPR/PSPR) | 120 Kbyte / 32 Kbyte [2] |
| | Size TC1.6E (DSPR/PSPR) | 112 Kbyte / 24 Kbyte [1] [2] |
| | Size LMU | 32 Kbyte |
| DMA | Channels | 64 |
| ADC | Channels | 48 + 12 |
| | Converter | 8 |
| DSADC | Channels | 6 |
| GTM | TIM | 4 |
| | TOM | 3 |
| | ATOM / MCS | 5 / 4 |
| | CMU / ICM | 1 / 1 |
| | PSM | 1 |
| | TBU | 1 |
| | SPE | 2 |
| | CMP / MON | 1 / 1 |
| | BRC / DPLL | 1 / 1 |
| Timer | GPT12 | 2 |
| | CCU6 | 2 |
| STM | Modules | 3 |
| FlexRay | Modules | 1 |
| | Channels | 2 |

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**Table 1-1 Overview of TC27x Functions** (cont'd)

| Feature | | |
|---|---|---|
| CAN | Nodes | 4 |
| | Message Objects | 256 |
| QSPI | Channels | 4 |
| ASCLIN | Interfaces | 4 |
| I2C | Interfaces | 1 |
| SENT | Channels | 10 |
| PSI5 | Modules | 3 |
| PSI5-S | Modules | 1 |
| HSSL | Channels | 1 |
| MSC | Channels | 2 |
| Ethernet | Channels | 1 |
| ASIL | Level | up to ASIL-D |
| FCE | Modules | 1 |
| Safety support | SMU | 1 |
| | IOM | 1 |
| Security | HSM | 1 |
| Embedded Voltage Regulator | DCDC from 5 V / 3.3 V to 1.3 V | Yes |
| Embedded Voltage Regulator | LDO from 5 V / 3.3 V to 1.3 V | Yes |
| Embedded Voltage Regulator | LDO from 5 V to 3.3 V | Yes |
| Low Power Feature | Standby RAM | Yes |
| Packages | Type | LF-BGA-292-6 / PG-LQFP-176-22 |
| I/O | Type | 5 V CMOS / 3.3 V CMOS / LVDS |
| $T_{ambient}$ | Range | −40 … +125°C |

1) Address range starts at lowest address defined in the User's Manual. For reference see the Memory Maps chapter of the User's Manual.

2) To ensure the processor cores are provided with a constant stream of instructions the Instruction Fetch Units will speculatively fetch instructions from the up to 64 bytes ahead of the current PC.
If the current PC is within 64 bytes of the top of an instruction memory the Instruction Fetch Unit may attempt to speculatively fetch instruction from beyond the physical range. This may then lead to error conditions and alarms being triggered by the bus and memory systems.
It is therefore recommended that the upper 64 bytes of any memory be unused for instruction storage.

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# 2 Package and Pinning Definitions

This chapter gives a pinning of the different packages of the TC270 / TC275 / TC277.

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## 2.1 TC275x Pin Definition and Functions: LQFP176

**Figure 2-1** is showing the TC275x Logic Symbol for the package variant: QFP176.

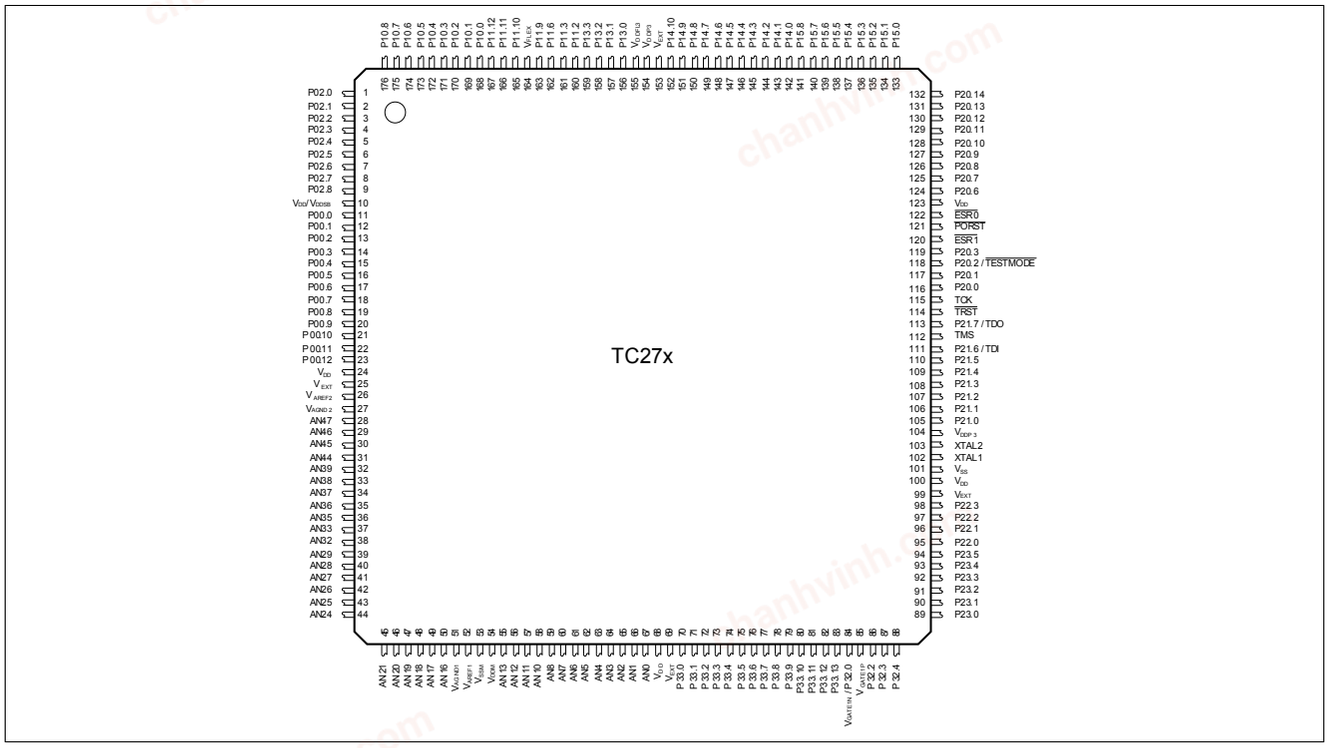



**Figure 2-1 TC275x Logic Symbol for the package variant LQFP176.**

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### 2.1.1 TC275x LQFP176 Package Variant Pin Configuration'

**Table 2-1 Port 00 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **11** | P00.0 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN9 | | | GTM input |
| | $\overline{\text{CTRAPA}}$ | | | CCU61 input |
| | T12HRE | | | CCU60 input |
| | INJ00 | | | MSC0 input |
| | CIFD9 | | | CIF input |
| | P00.0 | O0 | | General-purpose output |
| | TOUT9 | O1 | | GTM output |
| | ASCLK3 | O2 | | ASCLIN3 output |
| | ATX3 | O3 | | ASCLIN3 output |
| | – | O4 | | Reserved |
| | TXDCAN1 | O5 | | CAN node 1 output |
| | – | O6 | | Reserved |
| | COUT63 | O7 | | CCU60 output |
| | ETHMDIOA | HWOUT | | ETH input/output |
| **12** | P00.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN10 | | | GTM input |
| | ARX3E | | | ASCLIN3 input |
| | RXDCAN1D | | | CAN node 1 input |
| | PSIRX0A | | | PSI5 input |
| | SENT0B | | | SENT input |
| | CC60INB | | | CCU60 input |
| | CC60INA | | | CCU61 input |
| | DSCIN5A | | | DSADC channel 5 input A |
| | DS5NA | | | DSADC negative analog input of channel 5, pin A |
| | VADCG7.5 | | | VADC analog input channel 5 of group 7 |
| | CIFD10 | | | CIF input |
| | P00.1 | O0 | | General-purpose output |
| | TOUT10 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | DSCOUT5 | O4 | | DSADC channel 5 output |
| | – | O5 | | Reserved |
| | SPC0 | O6 | | SENT output |
| | CC60 | O7 | | CCU61 output |

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**Table 2-1 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **13** | P00.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN11 | | | GTM input |
| | SENT1B | | | SENT input |
| | DSDIN5A | | | DSADC channel 5 input A |
| | DS5PA | | | DSADC positive analog input of channel 5, pin A |
| | VADCG7.4 | | | VADC analog input channel 4 of group 7 |
| | CIFD11 | | | CIF input |
| | P00.2 | O0 | | General-purpose output |
| | TOUT11 | O1 | | GTM output |
| | ASCLK3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | PSITX0 | O4 | | PSI5 output |
| | TXDCAN3 | O5 | | CAN node 3 output |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU61 output |
| **14** | P00.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN12 | | | GTM input |
| | RXDCAN3A | | | CAN node 3 input |
| | PSIRX1A | | | PSI5 input |
| | PSISRXA | | | PSI5-S input |
| | SENT2B | | | SENT input |
| | CC61INB | | | CCU60 input |
| | CC61INA | | | CCU61 input |
| | DSCIN3A | | | DSADC channel 3 input A |
| | VADCG7.3 | | | VADC analog input channel 3 of group 7 |
| | DSITR5F | | | DSADC channel 5 input F |
| | CIFD12 | | | CIF input |
| | P00.3 | O0 | | General-purpose output |
| | TOUT12 | O1 | | GTM output |
| | ASLSO3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | DSCOUT3 | O4 | | DSADC channel 3 output |
| | – | O5 | | Reserved |
| | SPC2 | O6 | | SENT output |
| | CC61 | O7 | | CCU61 output |

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**Table 2-1 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **15** | P00.4 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN13 | | | GTM input |
| | REQ7 | | | SCU input |
| | SENT3B | | | SENT input |
| | DSDIN3A | | | DSADC channel 3 input A |
| | DSSGNA | | | DSADC input |
| | VADCG7.2 | | | VADC analog input channel 2 of group 7 (MD) |
| | CIFD13 | | | CIF input |
| | P00.4 | O0 | | General-purpose output |
| | TOUT13 | O1 | | GTM output |
| | PSISTX | O2 | | PSI5-S output |
| | – | O3 | | Reserved |
| | PSITX1 | O4 | | PSI5 output |
| | VADCG4BFL0 | O5 | | VADC output |
| | SPC3 | O6 | | SENT output |
| | COUT61 | O7 | | CCU61 output |
| **16** | P00.5 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN14 | | | GTM input |
| | PSIRX2A | | | PSI5 input |
| | SENT4B | | | SENT input |
| | CC62INB | | | CCU60 input |
| | CC62INA | | | CCU61 input |
| | DSCIN2A | | | DSADC channel 2 input A |
| | VADCG7.1 | | | VADC analog input channel 1 of group 7 (MD) |
| | CIFD14 | | | CIF input |
| | P00.5 | O0 | | General-purpose output |
| | TOUT14 | O1 | | GTM output |
| | DSCGPWMN | O2 | | DSADC output |
| | – | O3 | | Reserved |
| | DSCOUT2 | O4 | | DSADC channel 2 output |
| | VADCG4BFL1 | O5 | | VADC output |
| | SPC4 | O6 | | SENT output |
| | CC62 | O7 | | CCU61 output |

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**Table 2-1 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **17** | P00.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN15 | | | GTM input |
| | SENT5B | | | SENT input |
| | DSDIN2A | | | DSADC channel 2 input A |
| | VADCG7.0 | | | VADC analog input channel 0 of group 7 |
| | DSITR4F | | | DSADC channel 4 input F |
| | CIFD15 | | | CIF input |
| | P00.6 | O0 | | General-purpose output |
| | TOUT15 | O1 | | GTM output |
| | DSCGPWMP | O2 | | DSADC output |
| | VADCG4BFL2 | O3 | | VADC output |
| | PSITX2 | O4 | | PSI5 output |
| | VADCEMUX10 | O5 | | VADC output |
| | SPC5 | O6 | | SENT output |
| | COUT62 | O7 | | CCU61 output |
| **18** | P00.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN16 | | | GTM input |
| | SENT6B | | | SENT input |
| | CC60INC | | | CCU61 input |
| | CCPOS0A | | | CCU61 input |
| | T12HRB | | | CCU60 input |
| | T2INA | | | GPT120 input |
| | DSCIN4A | | | DSADC channel 4 input A |
| | DS4NA | | | DSADC negative analog input of channel 4, pin A |
| | VADCG6.5 | | | VADC analog input channel 5 of group 6 |
| | CIFCLK | | | CIF input |
| | P00.7 | O0 | | General-purpose output |
| | TOUT16 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | VADCG4BFL3 | O3 | | VADC output |
| | DSCOUT4 | O4 | | DSADC channel 4 output |
| | VADCEMUX11 | O5 | | VADC output |
| | SPC6 | O6 | | SENT output |
| | CC60 | O7 | | CCU61 output |

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**Table 2-1 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **19** | P00.8 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN17 | | | GTM input |
| | SENT7B | | | SENT input |
| | CC61INC | | | CCU61 input |
| | CCPOS1A | | | CCU61 input |
| | T13HRB | | | CCU60 input |
| | T2EUDA | | | GPT120 input |
| | DSDIN4A | | | DSADC channel 4 input A |
| | DS4PA | | | DSADC channel 4 input A |
| | VADCG6.4 | | | VADC analog input channel 4 of group 6 |
| | CIFVSNC | | | CIF input |
| | P00.8 | O0 | | General-purpose output |
| | TOUT17 | O1 | | GTM output |
| | SLSO36 | O2 | | QSPI3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | VADCEMUX12 | O5 | | VADC output |
| | SPC7 | O6 | | SENT output |
| | CC61 | O7 | | CCU61 output |

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**Table 2-1 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **20** | P00.9 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN18 | | | GTM input |
| | SENT8B | | | SENT input |
| | CC62INC | | | CCU61 input |
| | CCPOS2A | | | CCU61 input |
| | T13HRC | | | CCU60 input |
| | T12HRC | | | CCU60 input |
| | T4EUDA | | | GPT120 input |
| | DSCIN1A | | | DSADC channel 1 input A |
| | VADCG6.3 | | | VADC analog input channel 3 of group 6 |
| | DSITR3F | | | DSADC channel 3 input F |
| | CIFHSNC | | | CIF input |
| | P00.9 | O0 | | General-purpose output |
| | TOUT18 | O1 | | GTM output |
| | SLSO37 | O2 | | QSPI3 output |
| | ARTS3 | O3 | | ASCLIN3 output |
| | DSCOUT1 | O4 | | DSADC channel 1 output |
| | – | O5 | | Reserved |
| | SPC8 | O6 | | SENT output |
| | CC62 | O7 | | CCU61 output |
| **21** | P00.10 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN19 | | | GTM input |
| | SENT9B | | | SENT input |
| | DSDIN1A | | | DSADC channel 1 input A |
| | VADCG6.2 | | | VADC analog input channel 2 of group 6 (MD) |
| | P00.10 | O0 | | General-purpose output |
| | TOUT19 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | SPC9 | O6 | | SENT output |
| | COUT63 | O7 | | CCU61 output |

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**Table 2-1 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **22** | P00.11 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN20 | | | GTM input |
| | $\overline{\text{CTRAPA}}$ | | | CCU60 input |
| | T12HRE | | | CCU61 input |
| | DSCIN0A | | | DSADC channel 0 input A |
| | VADCG6.1 | | | VADC analog input channel 1 of group 6 (MD) |
| | P00.11 | O0 | | General-purpose output |
| | TOUT20 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | DSCOUT0 | O4 | | DSADC channel 0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **23** | P00.12 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN21 | | | GTM input |
| | ACTS3A | | | ASCLIN3 input |
| | DSDIN0A | | | DSADC channel 0 input A |
| | VADCG6.0 | | | VADC analog input channel 0 of group 6 |
| | P00.12 | O0 | | General-purpose output |
| | TOUT21 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT63 | O7 | | CCU61 output |

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**Table 2-2 Port 02 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **1** | P02.0 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN0 | | | GTM input |
| | ARX2G | | | ASCLIN2 input |
| | REQ6 | | | SCU input |
| | CC60INA | | | CCU60 input |
| | CC60INB | | | CCU61 input |
| | CIFD0 | | | CIF input |
| | P02.0 | O0 | | General-purpose output |
| | TOUT0 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO31 | O3 | | QSPI3 output |
| | DSCGPWMN | O4 | | DSADC output |
| | TXDCAN0 | O5 | | CAN node 0 output |
| | TXDA | O6 | | ERAY output |
| | CC60 | O7 | | CCU60 output |
| **2** | P02.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN1 | | | GTM input |
| | REQ14 | | | SCU input |
| | ARX2B | | | ASCLIN2 input |
| | RXDCAN0A | | | CAN node 0 input |
| | RXDA2 | | | ERAY input |
| | CIFD1 | | | CIF input |
| | P02.1 | O0 | | General-purpose output |
| | TOUT1 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO32 | O3 | | QSPI3 output |
| | DSCGPWMP | O4 | | DSADC output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU60 output |

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**Table 2-2 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **3** | P02.2 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN2 | | | GTM input |
| | CC61INA | | | CCU60 input |
| | CC61INB | | | CCU61 input |
| | CIFD2 | | | CIF input |
| | P02.2 | O0 | | General-purpose output |
| | TOUT2 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | SLSO33 | O3 | | QSPI3 output |
| | PSITX0 | O4 | | PSI5 output |
| | TXDCAN2 | O5 | | CAN node 2 output |
| | TXDB | O6 | | ERAY output |
| | CC61 | O7 | | CCU60 output |
| **4** | P02.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN3 | | | GTM input |
| | ARX1G | | | ASCLIN1 input |
| | RXDCAN2B | | | CAN node 2 input |
| | RXDB2 | | | ERAY input |
| | PSIRX0B | | | PSI5 input |
| | DSCIN5B | | | DSADC channel 5 input B |
| | SDI11 | | | MSC1 input |
| | CIFD3 | | | CIF input |
| | P02.3 | O0 | | General-purpose output |
| | TOUT3 | O1 | | GTM output |
| | ASLSO2 | O2 | | ASCLIN2 output |
| | SLSO34 | O3 | | QSPI3 output |
| | DSCOUT5 | O4 | | DSADC channel 5 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT61 | O7 | | CCU60 output |

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**Table 2-2 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **5** | P02.4 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN4 | | | GTM input |
| | SLSI3A | | | QSPI3 input |
| | ECTT1 | | | TTCAN input |
| | RXDCAN0D | | | CAN node 0 input |
| | CC62INA | | | CCU60 input |
| | CC62INB | | | CCU61 input |
| | DSDIN5B | | | DSADC channel 5 input B |
| | SDA0A | | | I2C0 input |
| | CIFD4 | | | CIF input |
| | P02.4 | O0 | | General-purpose output |
| | TOUT4 | O1 | | GTM output |
| | ASCLK2 | O2 | | ASCLIN2 output |
| | SLSO30 | O3 | | QSPI3 output |
| | PSISCLK | O4 | | PSI5-S output |
| | SDA0 | O5 | | I2C0 output |
| | TXENA | O6 | | ERAY output |
| | CC62 | O7 | | CCU60 output |
| **6** | P02.5 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN5 | | | GTM input |
| | MRST3A | | | QSPI3 input |
| | ECTT2 | | | TTCAN input |
| | PSIRX1B | | | PSI5 input |
| | PSISRXB | | | PSI5-S input |
| | SENT3C | | | SENT input |
| | DSCIN4B | | | DSADC channel 4 input B |
| | SCL0A | | | I2C0 input |
| | CIFD5 | | | CIF input |
| | P02.5 | O0 | | General-purpose output |
| | TOUT5 | O1 | | GTM output |
| | TXDCAN0 | O2 | | CAN node 0 output |
| | MRST3 | O3 | | QSPI3 output |
| | DSCOUT4 | O4 | | DSADC channel 4 output |
| | SCL0 | O5 | | I2C0 output |
| | TXENB | O6 | | ERAY output |
| | COUT62 | O7 | | CCU60 output |

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**Table 2-2 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **7** | P02.6 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN6 | | | GTM input |
| | MTSR3A | | | QSPI3 input |
| | SENT2C | | | SENT input |
| | CC60INC | | | CCU60 input |
| | CCPOS0A | | | CCU60 input |
| | T12HRB | | | CCU61 input |
| | T3INA | | | GPT120 input |
| | CIFD6 | | | CIF input |
| | DSDIN4B | | | DSADC channel 4 input B |
| | DSITR5E | | | DSADC channel 5 input E |
| | P02.6 | O0 | | General-purpose output |
| | TOUT6 | O1 | | GTM output |
| | PSISTX | O2 | | PSI5-S output |
| | MTSR3 | O3 | | QSPI3 output |
| | PSITX1 | O4 | | PSI5 output |
| | VADCEMUX00 | O5 | | VADC output |
| | – | O6 | | Reserved |
| | CC60 | O7 | | CCU60 output |

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**Table 2-2 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **8** | P02.7 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN7 | | | GTM input |
| | SCLK3A | | | QSPI3 input |
| | PSIRX2B | | | PSI5 input |
| | SENT1C | | | SENT input |
| | CC61INC | | | CCU60 input |
| | CCPOS1A | | | CCU60 input |
| | T13HRB | | | CCU61 input |
| | T3EUDA | | | GPT120 input |
| | CIFD7 | | | CIF input |
| | DSCIN3B | | | DSADC channel 3 input B |
| | DSITR4E | | | DSADC channel 4 input E |
| | P02.7 | O0 | | General-purpose output |
| | TOUT7 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK3 | O3 | | QSPI3 output |
| | DSCOUT3 | O4 | | DSADC channel 3 output |
| | VADCEMUX01 | O5 | | VADC output |
| | SPC1 | O6 | | SENT output |
| | CC61 | O7 | | CCU60 output |

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**Table 2-2 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **9** | P02.8 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN8 | | | GTM input |
| | SENT0C | | | SENT input |
| | CC62INC | | | CCU60 input |
| | CCPOS2A | | | CCU60 input |
| | T12HRC | | | CCU61 input |
| | T13HRC | | | CCU61 input |
| | T4INA | | | GPT120 input |
| | CIFD8 | | | CIF input |
| | DSDIN3B | | | DSADC channel 3 input B |
| | DSITR3E | | | DSADC channel 3 input E |
| | P02.8 | O0 | | General-purpose output |
| | TOUT8 | O1 | | GTM output |
| | SLSO35 | O2 | | QSPI3 output |
| | – | O3 | | Reserved |
| | PSITX2 | O4 | | PSI5 output |
| | VADCEMUX02 | O5 | | VADC output |
| | ETHMDC | O6 | | ETH output |
| | CC62 | O7 | | CCU60 output |

**Table 2-3 Port 10 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **168** | P10.0 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN102 | | | GTM input |
| | T6EUDB | | | GPT120 input |
| | P10.0 | O0 | | General-purpose output |
| | TOUT102 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO110 | O3 | | QSPI1 output |
| | – | O4 | | Reserved |
| | VADCG6BFL0 | O5 | | VADC output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-3 Port 10 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **169** | P10.1 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN103 | | | GTM input |
| | MRST1A | | | QSPI1 input |
| | T5EUDB | | | GPT120 input |
| | P10.1 | O0 | | General-purpose output |
| | TOUT103 | O1 | | GTM output |
| | MTSR1 | O2 | | QSPI1 output |
| | MRST1 | O3 | | QSPI1 output |
| | EN01 | O4 | | MSC0 output |
| | VADCG6BFL1 | O5 | | VADC output |
| | END03 | O6 | | MSC0 output |
| | – | O7 | | Reserved |
| **170** | P10.2 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN104 | | | GTM input |
| | SCLK1A | | | QSPI1 input |
| | T6INB | | | GPT120 input |
| | REQ2 | | | SCU input |
| | RXDCAN2E | | | CAN node 2 input |
| | SDI01 | | | MSC0 input |
| | P10.2 | O0 | | General-purpose output |
| | TOUT104 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK1 | O3 | | QSPI1 output |
| | EN00 | O4 | | MSC0 output |
| | VADCG6BFL2 | O5 | | VADC output |
| | END02 | O6 | | MSC0 output |
| | – | O7 | | Reserved |

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**Table 2-3 Port 10 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **171** | P10.3 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN105 | | | GTM input |
| | MTSR1A | | | QSPI1 input |
| | REQ3 | | | SCU input |
| | T5INB | | | GPT120 input |
| | P10.3 | O0 | | General-purpose output |
| | TOUT105 | O1 | | GTM output |
| | VADCG6BFL3 | O2 | | VADC output |
| | MTSR1 | O3 | | QSPI1 output |
| | EN00 | O4 | | MSC0 output |
| | END02 | O5 | | MSC0 output |
| | TXDCAN2 | O6 | | CAN node 2 output |
| | – | O7 | | Reserved |
| **172** | P10.4 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN106 | | | GTM input |
| | MTSR1C | | | QSPI1 input |
| | CCPOS0C | | | CCU60 input |
| | T3INB | | | GPT120 input |
| | P10.4 | O0 | | General-purpose output |
| | TOUT106 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO18 | O3 | | QSPI1 output |
| | MTSR1 | O4 | | QSPI1 output |
| | EN00 | O5 | | MSC0 output |
| | END02 | O6 | | MSC0 output |
| | – | O7 | | Reserved |
| **173** | P10.5 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN107 | | | GTM input |
| | HWCFG4 | | | SCU input |
| | INJ01 | | | MSC0 input |
| | P10.5 | O0 | | General-purpose output |
| | TOUT107 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO38 | O3 | | QSPI3 output |
| | SLSO19 | O4 | | QSPI1 output |
| | T6OUT | O5 | | GPT120 output |
| | ASLSO2 | O6 | | ASCLIN2 output |
| | - | O7 | | Reserved |

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**Table 2-3 Port 10 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **174** | P10.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN108 | | | GTM input |
| | ARX2D | | | ASCLIN2 input |
| | MTSR3B | | | QSPI3 input |
| | HWCFG5 | | | SCU input |
| | P10.6 | O0 | | General-purpose output |
| | TOUT108 | O1 | | GTM output |
| | ASCLK2 | O2 | | ASCLIN2 output |
| | MTSR3 | O3 | | QSPI3 output |
| | T3OUT | O4 | | GPT120 output |
| | - | O5 | | Reserved |
| | MRST1 | O6 | | QSPI1 output |
| | VADCG7BFL0 | O7 | | VADC output |
| **175** | P10.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN109 | | | GTM input |
| | ACTS2A | | | ASCLIN2 input |
| | MRST3B | | | QSPI3 input |
| | REQ4 | | | SCU input |
| | CCPOS1C | | | CCU60 input |
| | T3EUDB | | | GPT120 input |
| | P10.7 | O0 | | General-purpose output |
| | TOUT109 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MRST3 | O3 | | QSPI3 output |
| | VADCG7BFL1 | O4 | | VADC output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-3 Port 10 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **176** | P10.8 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN110 | | | GTM input |
| | SCLK3B | | | QSPI3 input |
| | REQ5 | | | SCU input |
| | CCPOS2C | | | CCU60 input |
| | T4INB | | | GPT120 input |
| | P10.8 | O0 | | General-purpose output |
| | TOUT110 | O1 | | GTM output |
| | ARTS2 | O2 | | ASCLIN2 output |
| | SCLK3 | O3 | | QSPI3 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

**Table 2-4 Port 11 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **160** | P11.2 | I | **MPR / PU1 / VFLEX** | General-purpose input |
| | TIN95 | | | GTM input |
| | P11.2 | O0 | | General-purpose output |
| | TOUT95 | O1 | | GTM output |
| | END03 | O2 | | MSC0 output |
| | SLSO05 | O3 | | QSPI0 output |
| | SLSO15 | O4 | | QSPI1 output |
| | EN01 | O5 | | MSC0 output |
| | ETHTXD1 | O6 | | ETH output |
| | COUT63 | O7 | | CCU60 output |

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**Table 2-4 Port 11 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **161** | P11.3 | I | **MPR / PU1 / VFLEX** | General-purpose input |
| | TIN96 | | | GTM input |
| | MRST1B | | | QSPI1 input |
| | SDI03 | | | MSC0 input |
| | P11.3 | O0 | | General-purpose output |
| | TOUT96 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MRST1 | O3 | | QSPI1 output |
| | TXDA | O4 | | ERAY output |
| | – | O5 | | Reserved |
| | ETHTXD0 | O6 | | ETH output |
| | COUT62 | O7 | | CCU60 output |
| **162** | P11.6 | I | **MPR / PU1 / VFLEX** | General-purpose input |
| | TIN97 | | | GTM input |
| | SCLK1B | | | QSPI1 input |
| | P11.6 | O0 | | General-purpose output |
| | TOUT97 | O1 | | GTM output |
| | $\overline{\text{TXENB}}$ | O2 | | ERAY output |
| | SCLK1 | O3 | | QSPI1 output |
| | $\overline{\text{TXENA}}$ | O4 | | ERAY output |
| | FCLP0 | O5 | | MSC0 output |
| | ETHTXEN | O6 | | ETH output |
| | COUT61 | O7 | | CCU60 output |
| **163** | P11.9 | I | **MP+ / PU1 / VFLEX** | General-purpose input |
| | TIN98 | | | GTM input |
| | MTSR1B | | | QSPI1 input |
| | RXDA1 | | | ERAY input |
| | ETHRXD1 | | | ETH input |
| | P11.9 | O0 | | General-purpose output |
| | TOUT98 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MTSR1 | O3 | | QSPI1 output |
| | – | O4 | | Reserved |
| | SOP0 | O5 | | MSC0 output |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU60 output |

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**Table 2-4 Port 11 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **165** | P11.10 | I | **LP / PU1 / VFLEX** | General-purpose input |
| | TIN99 | | | GTM input |
| | REQ12 | | | SCU input |
| | ARX1E | | | ASCLIN1 input |
| | $\overline{\text{SLSI1A}}$ | | | QSPI1 input |
| | RXDCAN3D | | | CAN node 3 input |
| | RXDB1 | | | ERAY input |
| | ETHRXD0 | | | ETH input |
| | SDI00 | | | MSC0 input |
| | P11.10 | O0 | | General-purpose output |
| | TOUT99 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO03 | O3 | | QSPI0 output |
| | SLSO13 | O4 | | QSPI1 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | CC62 | O7 | | CCU60 output |
| **166** | P11.11 | I | **MP+ / PU1 / VFLEX** | General-purpose input |
| | TIN100 | | | GTM input |
| | ETHCRSDVA | | | ETH input |
| | ETHRXDVA | | | ETH input |
| | ETHCRSB | | | ETH input |
| | P11.11 | O0 | | General-purpose output |
| | TOUT100 | O1 | | GTM output |
| | END02 | O2 | | MSC0 output |
| | SLSO04 | O3 | | QSPI0 output |
| | SLSO14 | O4 | | QSPI1 output |
| | EN00 | O5 | | MSC0 output |
| | $\overline{\text{TXENB}}$ | O6 | | ERAY output |
| | CC61 | O7 | | CCU60 output |

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**Table 2-4 Port 11 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **167** | P11.12 | I | **MPR / PU1 / VFLEX** | General-purpose input |
| | TIN101 | | | GTM input |
| | ETHREFCLK | | | ETH input |
| | ETHTXCLKB | | | ETH input<br>(Not for productive purposes) |
| | ETHRXCLKA | | | ETH input<br>(Not for productive purposes) |
| | P11.12 | O0 | | General-purpose output |
| | TOUT101 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | GTMCLK2 | O3 | | GTM output |
| | TXDB | O4 | | ERAY output |
| | TXDCAN3 | O5 | | CAN node 3 output |
| | EXTCLK1 | O6 | | SCU output |
| | CC60 | O7 | | CCU60 output |

**Table 2-5 Port 13 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **156** | P13.0 | I | **LVDSM_N / PU1 / VEXT** | General-purpose input |
| | TIN91 | | | GTM input |
| | P13.0 | O0 | | General-purpose output |
| | TOUT91 | O1 | | GTM output |
| | END03 | O2 | | MSC0 output |
| | SCLK2N | O3 | | QSPI2 output (LVDS) |
| | EN01 | O4 | | MSC0 output |
| | FCLN0 | O5 | | MSC0 output (LVDS) |
| | FCLND0 | O6 | | MSC0 output (LVDS) |
| | – | O7 | | Reserved |
| **157** | P13.1 | I | **LVDSM_P / PU1 / VEXT** | General-purpose input |
| | TIN92 | | | GTM input |
| | SCL0B | | | I2C0 input |
| | P13.1 | O0 | | General-purpose output |
| | TOUT92 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK2P | O3 | | QSPI2 output (LVDS) |
| | – | O4 | | Reserved |
| | FCLP0 | O5 | | MSC0 output (LVDS) |
| | SCL0 | O6 | | I2C0 output |
| | – | O7 | | Reserved |

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**Table 2-5 Port 13 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **158** | P13.2 | I | **LVDSM_N / PU1 / VEXT** | General-purpose input |
| | TIN93 | | | GTM input |
| | CAPINA | | | GPT120 input |
| | SDA0B | | | I2C0 input |
| | P13.2 | O0 | | General-purpose output |
| | TOUT93 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MTSR2N | O3 | | QSPI2 output (LVDS) |
| | FCLP0 | O4 | | MSC0 output |
| | SON0 | O5 | | MSC0 output (LVDS) |
| | SDA0 | O6 | | I2C0 output |
| | SOND0 | O7 | | MSC0 output (LVDS) |
| **159** | P13.3 | I | **LVDSM_P / PU1 / VEXT** | General-purpose input |
| | TIN94 | | | GTM input |
| | P13.3 | O0 | | General-purpose output |
| | TOUT94 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MTSR2P | O3 | | QSPI2 output (LVDS) |
| | – | O4 | | Reserved |
| | SOP0 | O5 | | MSC0 output (LVDS) |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

**Table 2-6 Port 14 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **142** | P14.0 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN80 | | | GTM input |
| | P14.0 | O0 | | General-purpose output |
| | TOUT80 | O1 | | GTM output |
| | ATX0 | O2 | | ASCLIN0 output<br>Recommended as Boot loader pin. |
| | TXDA | O3 | | ERAY output |
| | TXDB | O4 | | ERAY output |
| | TXDCAN1 | O5 | | CAN node 1 output<br>Used for single pin DAP (SPD) function. |
| | ASCLK0 | O6 | | ASCLIN0 output |
| | COUT62 | O7 | | CCU60 output |

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**Table 2-6 Port 14 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **143** | P14.1 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN81 | | | GTM input |
| | REQ15 | | | SCU input |
| | ARX0A | | | ASCLIN0 input<br>Recommended as Boot loader pin. |
| | RXDCAN1B | | | CAN node 1 input<br>Used for single pin DAP (SPD) function. |
| | RXDA3 | | | ERAY input |
| | RXDB3 | | | ERAY input |
| | EVRWUPA | | | SCU input |
| | P14.1 | O0 | | General-purpose output |
| | TOUT81 | O1 | | GTM output |
| | ATX0 | O2 | | ASCLIN0 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT63 | O7 | | CCU60 output |
| **144** | P14.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN82 | | | GTM input |
| | HWCFG2<br>EVR13 | | | SCU input<br>Latched at cold power on reset to decide EVR13 activation. |
| | P14.2 | O0 | | General-purpose output |
| | TOUT82 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO21 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ASCLK2 | O6 | | ASCLIN2 output |
| | – | O7 | | Reserved |

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**Table 2-6 Port 14 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **145** | P14.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN83 | | | GTM input |
| | ARX2A | | | ASCLIN2 input |
| | REQ10 | | | SCU input |
| | HWCFG3_BMI | | | SCU input |
| | SDI02 | | | MSC0 input |
| | P14.3 | O0 | | General-purpose output |
| | TOUT83 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO23 | O3 | | QSPI2 output |
| | ASLSO1 | O4 | | ASCLIN1 output |
| | ASLSO3 | O5 | | ASCLIN3 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **146** | P14.4 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN84 | | | GTM input |
| | HWCFG6 | | | SCU input<br>Latched at cold power on reset to decide default pad reset state (PU or HighZ). |
| | P14.4 | O0 | | General-purpose output |
| | TOUT84 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-6 Port 14 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **147** | P14.5 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN85 | | | GTM input |
| | HWCFG1<br>EVR33 | | | SCU input<br>Latched at cold power on reset to decide EVR33 activation. |
| | P14.5 | O0 | | General-purpose output |
| | TOUT85 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | TXDB | O6 | | ERAY output |
| | – | O7 | | Reserved |
| **148** | P14.6 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN86 | | | GTM input |
| | HWCFG0<br>DCLDO | | | SCU input<br>If EVR13 active, latched at cold power on reset to decide between LDO and SMPS mode. |
| | P14.6 | O0 | | General-purpose output |
| | TOUT86 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO22 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | $\overline{\text{TXENB}}$ | O6 | | ERAY output |
| | – | O7 | | Reserved |
| **149** | P14.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN87 | | | GTM input |
| | RXDB0 | | | ERAY input |
| | P14.7 | O0 | | General-purpose output |
| | TOUT87 | O1 | | GTM output |
| | ARTS0 | O2 | | ASCLIN0 output |
| | SLSO24 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-6 Port 14 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **150** | P14.8 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN88 | | | GTM input |
| | ARX1D | | | ASCLIN1 input |
| | RXDCAN2D | | | CAN node 2 input |
| | RXDA0 | | | ERAY input |
| | P14.8 | O0 | | General-purpose output |
| | TOUT88 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **151** | P14.9 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN89 | | | GTM input |
| | ACTS0A | | | ASCLIN0 input |
| | P14.9 | O0 | | General-purpose output |
| | TOUT89 | O1 | | GTM output |
| | END03 | O2 | | MSC0 output |
| | EN01 | O3 | | MSC0 output |
| | – | O4 | | Reserved |
| | $\overline{\text{TXENB}}$ | O5 | | ERAY output |
| | $\overline{\text{TXENA}}$ | O6 | | ERAY output |
| | – | O7 | | Reserved |
| **152** | P14.10 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN90 | | | GTM input |
| | P14.10 | O0 | | General-purpose output |
| | TOUT90 | O1 | | GTM output |
| | END02 | O2 | | MSC0 output |
| | EN00 | O3 | | MSC0 output |
| | ATX1 | O4 | | ASCLIN1 output |
| | TXDCAN2 | O5 | | CAN node 2 output |
| | TXDA | O6 | | ERAY output |
| | – | O7 | | Reserved |

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**Table 2-7 Port 15 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **133** | P15.0 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN71 | | | GTM input |
| | P15.0 | O0 | | General-purpose output |
| | TOUT71 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | SLSO013 | O3 | | QSPI0 output |
| | – | O4 | | Reserved |
| | TXDCAN2 | O5 | | CAN node 2 output |
| | ASCLK1 | O6 | | ASCLIN1 output |
| | – | O7 | | Reserved |
| **134** | P15.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN72 | | | GTM input |
| | REQ16 | | | SCU input |
| | ARX1A | | | ASCLIN1 input |
| | RXDCAN2A | | | CAN node 2 input |
| | $\overline{\text{SLSI2B}}$ | | | QSPI2 input |
| | EVRWUPB | | | SCU input |
| | P15.1 | O0 | | General-purpose output |
| | TOUT72 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | SLSO25 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **135** | P15.2 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN73 | | | GTM input |
| | $\overline{\text{SLSI2A}}$ | | | QSPI2 input |
| | MRST2E | | | QSPI2 input |
| | P15.2 | O0 | | General-purpose output |
| | TOUT73 | O1 | | GTM output |
| | ATX0 | O2 | | ASCLIN0 output |
| | SLSO20 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | TXDCAN1 | O5 | | CAN node 1 output |
| | ASCLK0 | O6 | | ASCLIN0 output |
| | – | O7 | | Reserved |

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**Table 2-7 Port 15 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **136** | P15.3 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN74 | | | GTM input |
| | ARX0B | | | ASCLIN0 input |
| | SCLK2A | | | QSPI2 input |
| | RXDCAN1A | | | CAN node 1 input |
| | P15.3 | O0 | | General-purpose output |
| | TOUT74 | O1 | | GTM output |
| | ATX0 | O2 | | ASCLIN0 output |
| | SCLK2 | O3 | | QSPI2 output |
| | END03 | O4 | | MSC0 output |
| | EN01 | O5 | | MSC0 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **137** | P15.4 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN75 | | | GTM input |
| | MRST2A | | | QSPI2 input |
| | REQ0 | | | SCU input |
| | SCL0C | | | I2C0 input |
| | P15.4 | O0 | | General-purpose output |
| | TOUT75 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | MRST2 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | SCL0 | O6 | | I2C0 output |
| | CC62 | O7 | | CCU60 output |

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**Table 2-7 Port 15 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **138** | P15.5 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN76 | | | GTM input |
| | ARX1B | | | ASCLIN1 input |
| | MTSR2A | | | QSPI2 input |
| | REQ13 | | | SCU input |
| | SDA0C | | | I2C0 input |
| | P15.5 | O0 | | General-purpose output |
| | TOUT76 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | MTSR2 | O3 | | QSPI2 output |
| | END02 | O4 | | MSC0 output |
| | EN00 | O5 | | MSC0 output |
| | SDA0 | O6 | | I2C0 output |
| | CC61 | O7 | | CCU60 output |
| **139** | P15.6 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN77 | | | GTM input |
| | MTSR2B | | | QSPI2 input |
| | P15.6 | O0 | | General-purpose output |
| | TOUT77 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | MTSR2 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | SCLK2 | O5 | | QSPI2 output |
| | ASCLK3 | O6 | | ASCLIN3 output |
| | CC60 | O7 | | CCU60 output |
| **140** | P15.7 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN78 | | | GTM input |
| | ARX3A | | | ASCLIN3 input |
| | MRST2B | | | QSPI2 input |
| | P15.7 | O0 | | General-purpose output |
| | TOUT78 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | MRST2 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU60 output |

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**Table 2-7 Port 15 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **141** | P15.8 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN79 | | | GTM input |
| | SCLK2B | | | QSPI2 input |
| | REQ1 | | | SCU input |
| | P15.8 | O0 | | General-purpose output |
| | TOUT79 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK2 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ASCLK3 | O6 | | ASCLIN3 output |
| | COUT61 | O7 | | CCU60 output |

**Table 2-8 Port 20 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **116** | P20.0 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN59 | | | GTM input |
| | RXDCAN3C | | | CAN node 3 input |
| | T6EUDA | | | GPT120 input |
| | REQ9 | | | SCU input |
| | SYSCLK | | | HSCT input |
| | $\overline{\text{TGI0}}$ | | | OCDS input |
| | P20.0 | O0 | | General-purpose output |
| | TOUT59 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | ASCLK3 | O3 | | ASCLIN3 output |
| | – | O4 | | Reserved |
| | SYSCLK | O5 | | HSCT output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | $\overline{\text{TGO0}}$ | HWOUT | | OCDS; ENx |

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**Table 2-8 Port 20 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **117** | P20.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN60 | | | GTM input |
| | $\overline{\text{TGI1}}$ | | | OCDS input |
| | P20.1 | O0 | | General-purpose output |
| | TOUT60 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | $\overline{\text{TGO1}}$ | HWOUT | | OCDS; ENx |
| **118** | P20.2 | I | **LP / PU / VEXT** | General-purpose input<br>This pin is latched at power on reset release to enter test mode. |
| | $\overline{\text{TESTMODE}}$ | | | OCDS input |
| | P20.2 | O0 | | Output function not available |
| | – | O1 | | Output function not available |
| | – | O2 | | Output function not available |
| | – | O3 | | Output function not available |
| | – | O4 | | Output function not available |
| | – | O5 | | Output function not available |
| | – | O6 | | Output function not available |
| | – | O7 | | Output function not available |
| **119** | P20.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN61 | | | GTM input |
| | T6INA | | | GPT120 input |
| | ARX3C | | | ASCLIN3 input |
| | P20.3 | O0 | | General-purpose output |
| | TOUT61 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | SLSO09 | O3 | | QSPI0 output |
| | SLSO29 | O4 | | QSPI2 output |
| | TXDCAN3 | O5 | | CAN node 3 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-8 Port 20 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **124** | P20.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN62 | | | GTM input |
| | P20.6 | O0 | | General-purpose output |
| | TOUT62 | O1 | | GTM output |
| | ARTS1 | O2 | | ASCLIN1 output |
| | SLSO08 | O3 | | QSPI0 output |
| | SLSO28 | O4 | | QSPI2 output |
| | – | O5 | | Reserved |
| | WDT2LCK | O6 | | SCU output |
| | – | O7 | | Reserved |
| **125** | P20.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN63 | | | GTM input |
| | ACTS1A | | | ASCLIN1 input |
| | RXDCAN0B | | | CAN node 0 input |
| | P20.7 | O0 | | General-purpose output |
| | TOUT63 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | WDT1LCK | O6 | | SCU output |
| | COUT63 | O7 | | CCU61 output |
| **126** | P20.8 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN64 | | | GTM input |
| | P20.8 | O0 | | General-purpose output |
| | TOUT64 | O1 | | GTM output |
| | ASLSO1 | O2 | | ASCLIN1 output |
| | SLSO00 | O3 | | QSPI0 output |
| | SLSO10 | O4 | | QSPI1 output |
| | TXDCAN0 | O5 | | CAN node 0 output |
| | WDT0LCK | O6 | | SCU output |
| | CC60 | O7 | | CCU61 output |

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**Table 2-8 Port 20 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **127** | P20.9 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN65 | | | GTM input |
| | ARX1C | | | ASCLIN1 input |
| | RXDCAN3E | | | CAN node 3 input |
| | REQ11 | | | SCU input |
| | $\overline{\text{SLSI0B}}$ | | | QSPI0 input |
| | P20.9 | O0 | | General-purpose output |
| | TOUT65 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO01 | O3 | | QSPI0 output |
| | SLSO11 | O4 | | QSPI1 output |
| | – | O5 | | Reserved |
| | WDTSLCK | O6 | | SCU output |
| | CC61 | O7 | | CCU61 output |
| **128** | P20.10 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN66 | | | GTM input |
| | P20.10 | O0 | | General-purpose output |
| | TOUT66 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | SLSO06 | O3 | | QSPI0 output |
| | SLSO27 | O4 | | QSPI2 output |
| | TXDCAN3 | O5 | | CAN node 3 output |
| | ASCLK1 | O6 | | ASCLIN1 output |
| | CC62 | O7 | | CCU61 output |
| **129** | P20.11 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN67 | | | GTM input |
| | SCLK0A | | | QSPI0 input |
| | P20.11 | O0 | | General-purpose output |
| | TOUT67 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK0 | O3 | | QSPI0 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU61 output |

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**Table 2-8 Port 20 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **130** | P20.12 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN68 | | | GTM input |
| | MRST0A | | | QSPI0 input |
| | P20.12 | O0 | | General-purpose output |
| | TOUT68 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MRST0 | O3 | | QSPI0 output |
| | MTSR0 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT61 | O7 | | CCU61 output |
| **131** | P20.13 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN69 | | | GTM input |
| | $\overline{\text{SLSI0A}}$ | | | QSPI0 input |
| | P20.13 | O0 | | General-purpose output |
| | TOUT69 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO02 | O3 | | QSPI0 output |
| | SLSO12 | O4 | | QSPI1 output |
| | SCLK0 | O5 | | QSPI0 output |
| | – | O6 | | Reserved |
| | COUT62 | O7 | | CCU61 output |
| **132** | P20.14 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN70 | | | GTM input |
| | MTSR0A | | | QSPI0 input |
| | P20.14 | O0 | | General-purpose output |
| | TOUT70 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MTSR0 | O3 | | QSPI0 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-9 Port 21 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **105** | P21.0 | I | **A2 / PU1 / VDDP3** | General-purpose input |
| | TIN51 | | | GTM input |
| | P21.0 | O0 | | General-purpose output |
| | TOUT51 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ETHMDC | O6 | | ETH output |
| | – | O7 | | Reserved |
| | HSM1 | HWOUT | | HSM output 1 |
| **106** | P21.1 | I | **A2 / PU1 / VDDP3** | General-purpose input |
| | TIN52 | | | GTM input |
| | ETHMDIOB | | | ETH input<br>(Not for production purposes) |
| | P21.1 | O0 | | General-purpose output |
| | TOUT52 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ETHMDIO | O6 | | ETH output<br>(Not for production purposes) |
| | – | O7 | | Reserved |
| | HSM2 | HWOUT | | HSM output 2 |

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**Table 2-9 Port 21 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **107** | P21.2 | I | **LVDSH_N/ PU1 / VDDP3** | General-purpose input |
| | TIN53 | | | GTM input |
| | MRST2CN | | | QSPI2 input (LVDS) |
| | MRST3FN | | | QSPI3 input (LVDS) |
| | ARX3GN | | | ASCLIN3 input (LVDS) |
| | EMGSTOPB | | | SCU input |
| | RXDN | | | HSCT input (LVDS) |
| | P21.2 | O0 | | General-purpose output |
| | TOUT53 | O1 | | GTM output |
| | ASLSO3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | ETHMDC | O5 | | ETH output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **108** | P21.3 | I | **LVDSH_P/ PU1 / VDDP3** | General-purpose input |
| | TIN54 | | | GTM input |
| | MRST2CP | | | QSPI2 input (LVDS) |
| | MRST3FP | | | QSPI3 input (LVDS) |
| | ARX3GP | | | ASCLIN3 input (LVDS) |
| | RXDP | | | HSCT input (LVDS) |
| | P21.3 | O0 | | General-purpose output |
| | TOUT54 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | ETHMDIOD | HWOUT | | ETH input/output |

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**Table 2-9 Port 21 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **109** | P21.4 | I | **LVDSH_N/ PU1 / VDDP3** | General-purpose input |
| | TIN55 | | | GTM input |
| | P21.4 | O0 | | General-purpose output |
| | TOUT55 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | TXDN | HSCT | | HSCT output (LVDS) |
| **110** | P21.5 | I | **LVDSH_P/ PU1 / VDDP3** | General-purpose input |
| | TIN56 | | | GTM input |
| | P21.5 | O0 | | General-purpose output |
| | TOUT56 | O1 | | GTM output |
| | ASCLK3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | TXDP | HSCT | | HSCT output (LVDS) |
| **111**[1)] | P21.6 | I | **A2 / PU / VDDP3** | General-purpose input |
| | TIN57 | | | GTM input |
| | ARX3F | | | ASCLIN3 input |
| | $\overline{\text{TGI2}}$ | | | OCDS input |
| | TDI | | | OCDS (JTAG) input |
| | T5EUDA | | | GPT120 input |
| | P21.6 | O0 | | General-purpose output |
| | TOUT57 | O1 | | GTM output |
| | ASLSO3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | SYSCLK | O5 | | HSCT output |
| | – | O6 | | Reserved |
| | T3OUT | O7 | | GPT120 output |
| | $\overline{\text{TGO2}}$ | HWOUT | | OCDS; ENx |

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**Table 2-9 Port 21 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **113** | P21.7 | I | **A2 / PU / VDDP3** | General-purpose input |
| | TIN58 | | | GTM input |
| | DAP2 | | | OCDS input |
| | $\overline{\text{TGI3}}$ | | | OCDS input |
| | TDO | | | OCDS (JTAG) input<br>The JTAG TDO function is overlayed with P21.7 via a double bond.<br>In JTAG mode this pin is used as TDO, after power-on reset it is HighZ. In DAP mode this pin is used as P21.7 and controlled by the related port control logic |
| | ETHRXERB | | | ETH input |
| | T5INA | | | GPT120 input |
| | P21.7 | O0 | | General-purpose output |
| | TOUT58 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | ASCLK3 | O3 | | ASCLIN3 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | T6OUT | O7 | | GPT120 output |
| | $\overline{\text{TGO3}}$ | HWOUT | | OCDS; ENx |
| | TDO | | | OCDS (JTAG); ENx<br>The JTAG TDO function is overlayed with P21.7 via a double bond.<br>In JTAG mode this pin is used as TDO, after power-on reset it is HighZ. In DAP mode this pin is used as P21.7 and controlled by the related port control logic |

1) For an Emulation Device in a non Fusion Quad package this pin is used as VDDPSB (3.3V)

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**Table 2-10 Port 22 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **95** | P22.0 | I | **LVDSM_N / PU1 / VEXT** | General-purpose input |
| | TIN47 | | | GTM input |
| | MTSR3E | | | QSPI3 input |
| | P22.0 | O0 | | General-purpose output |
| | TOUT47 | O1 | | GTM output |
| | ATX3N | O2 | | ASCLIN3 output (LVDS) |
| | MTSR3 | O3 | | QSPI3 output |
| | SCLK3N | O4 | | QSPI3 output (LVDS) |
| | FCLN1 | O5 | | MSC1 output (LVDS) |
| | FCLND1 | O6 | | MSC1 output (LVDS) |
| | – | O7 | | Reserved |
| **96** | P22.1 | I | **LVDSM_P / PU1 / VEXT** | General-purpose input |
| | TIN48 | | | GTM input |
| | MRST3E | | | QSPI3 input |
| | P22.1 | O0 | | General-purpose output |
| | TOUT48 | O1 | | GTM output |
| | ATX3P | O2 | | ASCLIN3 output (LVDS) |
| | MRST3 | O3 | | QSPI3 output |
| | SCLK3P | O4 | | QSPI3 output (LVDS) |
| | FCLP1 | O5 | | MSC1 output (LVDS) |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **97** | P22.2 | I | **LVDSM_N / PU1 / VEXT** | General-purpose input |
| | TIN49 | | | GTM input |
| | $\overline{\text{SLSI3D}}$ | | | QSPI3 input |
| | P22.2 | O0 | | General-purpose output |
| | TOUT49 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO312 | O3 | | QSPI3 output |
| | MTSR3N | O4 | | QSPI3 output (LVDS) |
| | SON1 | O5 | | MSC1 output (LVDS) |
| | SOND1 | O6 | | MSC1 output (LVDS) |
| | – | O7 | | Reserved |

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**Table 2-10 Port 22 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **98** | P22.3 | I | **LVDSM_P / PU1 / VEXT** | General-purpose input |
| | TIN50 | | | GTM input |
| | SCLK3E | | | QSPI3 input |
| | P22.3 | O0 | | General-purpose output |
| | TOUT50 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK3 | O3 | | QSPI3 output |
| | MTSR3P | O4 | | QSPI3 output (LVDS) |
| | SOP1 | O5 | | MSC1 output (LVDS) |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

**Table 2-11 Port 23 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **89** | P23.0 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN41 | | | GTM input |
| | P23.0 | O0 | | General-purpose output |
| | TOUT41 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **90** | P23.1 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN42 | | | GTM input |
| | SDI10 | | | MSC1 input |
| | P23.1 | O0 | | General-purpose output |
| | TOUT42 | O1 | | GTM output |
| | ARTS1 | O2 | | ASCLIN1 output |
| | SLSO313 | O3 | | QSPI3 output |
| | GTMCLK0 | O4 | | GTM output |
| | – | O5 | | Reserved |
| | EXTCLK0 | O6 | | SCU output |
| | – | O7 | | Reserved |

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**Table 2-11 Port 23 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **91** | P23.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN43 | | | GTM input |
| | P23.2 | O0 | | General-purpose output |
| | TOUT43 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **92** | P23.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN44 | | | GTM input |
| | INJ10 | | | MSC1 input |
| | P23.3 | O0 | | General-purpose output |
| | TOUT44 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **93** | P23.4 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN45 | | | GTM input |
| | P23.4 | O0 | | General-purpose output |
| | TOUT45 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO35 | O3 | | QSPI3 output |
| | END12 | O4 | | MSC1 output |
| | EN10 | O5 | | MSC1 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-11 Port 23 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **94** | P23.5 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN46 | | | GTM input |
| | P23.5 | O0 | | General-purpose output |
| | TOUT46 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO34 | O3 | | QSPI3 output |
| | END13 | O4 | | MSC1 output |
| | EN11 | O5 | | MSC1 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

**Table 2-12 Port 32 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **84** | P32.0 | I | **LP / EVR13 SMPS -> PD, GPIO - > PU / VEXT** | General-purpose input |
| | TIN36 | | | GTM input |
| | FDEST | | | PMU input |
| | VGATE1N | | | SMPS mode: analog output. External Pass Device gate control for EVR13 |
| | P32.0 | O0 | | General-purpose output |
| | TOUT36 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **86** | P32.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN38 | | | GTM input |
| | ARX3D | | | ASCLIN3 input |
| | RXDCAN3B | | | CAN node 3 input |
| | P32.2 | O0 | | General-purpose output |
| | TOUT38 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | DCDCSYNC | O6 | | SCU output |
| | – | O7 | | Reserved |

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**Table 2-12 Port 32 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **87** | P32.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN39 | | | GTM input |
| | P32.3 | O0 | | General-purpose output |
| | TOUT39 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | ASCLK3 | O4 | | ASCLIN3 output |
| | TXDCAN3 | O5 | | CAN node 3 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **88** | P32.4 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN40 | | | GTM input |
| | ACTS1B | | | ASCLIN1 input |
| | SDI12 | | | MSC1 input |
| | P32.4 | O0 | | General-purpose output |
| | TOUT40 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | END12 | O3 | | MSC1 output |
| | GTMCLK1 | O4 | | GTM output |
| | EN10 | O5 | | MSC1 output |
| | EXTCLK1 | O6 | | SCU output |
| | COUT63 | O7 | | CCU60 output |

**Table 2-13 Port 33 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **70** | P33.0 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN22 | | | GTM input |
| | DSITR0E | | | DSADC channel 0 input E |
| | P33.0 | O0 | | General-purpose output |
| | TOUT22 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | VADCG2BFL0 | O6 | | VADC output |
| | – | O7 | | Reserved |

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**Table 2-13 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **71** | P33.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN23 | | | GTM input |
| | PSIRX0C | | | PSI5 input |
| | SENT9C | | | SENT input |
| | DSCIN2B | | | DSADC channel 2 input B |
| | DSITR1E | | | DSADC channel 1 input E |
| | P33.1 | O0 | | General-purpose output |
| | TOUT23 | O1 | | GTM output |
| | ASLSO3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | DSCOUT2 | O4 | | DSADC channel 2 output |
| | VADCEMUX02 | O5 | | VADC output |
| | VADCG2BFL1 | O6 | | VADC output |
| | – | O7 | | Reserved |
| **72** | P33.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN24 | | | GTM input |
| | SENT8C | | | SENT input |
| | DSDIN2B | | | DSADC channel 2 input B |
| | DSITR2E | | | DSADC channel 2 input E |
| | P33.2 | O0 | | General-purpose output |
| | TOUT24 | O1 | | GTM output |
| | ASCLK3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | PSITX0 | O4 | | PSI5 output |
| | VADCEMUX01 | O5 | | VADC output |
| | VADCG2BFL2 | O6 | | VADC output |
| | – | O7 | | Reserved |

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**Table 2-13 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **73** | P33.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN25 | | | GTM input |
| | PSIRX1C | | | PSI5 input |
| | SENT7C | | | SENT input |
| | DSCIN1B | | | DSADC channel 1 input B |
| | P33.3 | O0 | | General-purpose output |
| | TOUT25 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | DSCOUT1 | O4 | | DSADC channel 1 output |
| | VADCEMUX00 | O5 | | VADC output |
| | VADCG2BFL3 | O6 | | VADC output |
| | – | O7 | | Reserved |
| **74** | P33.4 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN26 | | | GTM input |
| | SENT6C | | | SENT input |
| | $\overline{\text{CTRAPC}}$ | | | CCU61 input |
| | DSDIN1B | | | DSADC channel 1 input B |
| | DSITR0F | | | DSADC channel 0 input F |
| | P33.4 | O0 | | General-purpose output |
| | TOUT26 | O1 | | GTM output |
| | ARTS2 | O2 | | ASCLIN2 output |
| | – | O3 | | Reserved |
| | PSITX1 | O4 | | PSI5 output |
| | VADCEMUX12 | O5 | | VADC output |
| | VADCG0BFL0 | O6 | | VADC output |
| | – | O7 | | Reserved |

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**Table 2-13 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **75** | P33.5 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN27 | | | GTM input |
| | ACTS2B | | | ASCLIN2 input |
| | PSIRX2C | | | PSI5 input |
| | PSISRXC | | | PSI5-S input |
| | SENT5C | | | SENT input |
| | CCPOS2C | | | CCU61 input |
| | T4EUDB | | | GPT120 input |
| | DSCIN0B | | | DSADC channel 0 input B |
| | DSITR1F | | | DSADC channel 1 input F |
| | P33.5 | O0 | | General-purpose output |
| | TOUT27 | O1 | | GTM output |
| | SLSO07 | O2 | | QSPI0 output |
| | SLSO17 | O3 | | QSPI1 output |
| | DSCOUT0 | O4 | | DSADC channel 0 output |
| | VADCEMUX11 | O5 | | VADC output |
| | VADCG0BFL1 | O6 | | VADC output |
| | – | O7 | | Reserved |
| **76** | P33.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN28 | | | GTM input |
| | SENT4C | | | SENT input |
| | CCPOS1C | | | CCU61 input |
| | T2EUDB | | | GPT120 input |
| | DSDIN0B | | | DSADC channel 0 input B |
| | DSITR2F | | | DSADC channel 2 input F |
| | P33.6 | O0 | | General-purpose output |
| | TOUT28 | O1 | | GTM output |
| | ASLSO2 | O2 | | ASCLIN2 output |
| | - | O3 | | Reserved |
| | PSITX2 | O4 | | PSI5 output |
| | VADCEMUX10 | O5 | | VADC output |
| | VADCG1BFL0 | O6 | | VADC output |
| | PSISTX | O7 | | PSI5-S output |

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**Table 2-13 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **77** | P33.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN29 | | | GTM input |
| | RXDCAN0E | | | CAN node 0 input |
| | REQ8 | | | SCU input |
| | CCPOS0C | | | CCU61 input |
| | T2INB | | | GPT120 input |
| | P33.7 | O0 | | General-purpose output |
| | TOUT29 | O1 | | GTM output |
| | ASCLK2 | O2 | | ASCLIN2 output |
| | SLSO37 | O3 | | QSPI3 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | VADCG1BFL1 | O6 | | VADC output |
| | – | O7 | | Reserved |
| **78** | P33.8 | I | **MP / HighZ/ VEXT** | General-purpose input |
| | TIN30 | | | GTM input |
| | ARX2E | | | ASCLIN2 input |
| | EMGSTOPA | | | SCU input |
| | P33.8 | O0 | | General-purpose output |
| | TOUT30 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO32 | O3 | | QSPI3 output |
| | – | O4 | | Reserved |
| | TXDCAN0 | O5 | | CAN node 0 output |
| | – | O6 | | Reserved |
| | COUT62 | O7 | | CCU61 output |
| | SMUFSP | HWOUT | | SMU |
| **79** | P33.9 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN31 | | | GTM input |
| | P33.9 | O0 | | General-purpose output |
| | TOUT31 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO31 | O3 | | QSPI3 output |
| | ASCLK2 | O4 | | ASCLIN2 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | CC62 | O7 | | CCU61 output |

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**Table 2-13 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **80** | P33.10 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN32 | | | GTM input |
| | $\overline{\text{SLSI3C}}$ | | | QSPI3 input |
| | P33.10 | O0 | | General-purpose output |
| | TOUT32 | O1 | | GTM output |
| | SLSO16 | O2 | | QSPI1 output |
| | SLSO311 | O3 | | QSPI3 output |
| | ASLSO1 | O4 | | ASCLIN1 output |
| | PSISCLK | O5 | | PSI5-S output |
| | – | O6 | | Reserved |
| | COUT61 | O7 | | CCU61 output |
| **81** | P33.11 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN33 | | | GTM input |
| | SCLK3D | | | QSPI3 input |
| | P33.11 | O0 | | General-purpose output |
| | TOUT33 | O1 | | GTM output |
| | ASCLK1 | O2 | | ASCLIN1 output |
| | SCLK3 | O3 | | QSPI3 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | DSCGPWMN | O6 | | DSADC output |
| | CC61 | O7 | | CCU61 output |
| **82** | P33.12 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN34 | | | GTM input |
| | MTSR3D | | | QSPI3 input |
| | P33.12 | O0 | | General-purpose output |
| | TOUT34 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | MTSR3 | O3 | | QSPI3 output |
| | ASCLK1 | O4 | | ASCLIN1 output |
| | – | O5 | | Reserved |
| | DSCGPWMP | O6 | | DSADC output |
| | COUT60 | O7 | | CCU61 output |

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**Table 2-13 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **83** | P33.13 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN35 | | | GTM input |
| | ARX1F | | | ASCLIN1 input |
| | MRST3D | | | QSPI3 input |
| | DSSGNB | | | DSADC input |
| | INJ11 | | | MSC1 input |
| | P33.13 | O0 | | General-purpose output |
| | TOUT35 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | MRST3 | O3 | | QSPI3 output |
| | SLSO26 | O4 | | QSPI2 output |
| | – | O5 | | Reserved |
| | DCDCSYNC | O6 | | SCU output |
| | CC60 | O7 | | CCU61 output |

**Table 2-14 Port 40 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **44** | P40.0 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG3.0 | | | VADC analog input channel 0 of group 3 |
| | DS2PB | | | DSADC: positive analog input channe of DSADC 2, pin B |
| | CCPOS0D | | | CCU60 input |
| | SENT0A | | | SENT input |
| **43** | P40.1 | I | **S / HighZ / VDDM** | General-purpose inpu.t |
| | VADCG3.1 | | | VADC analog input channel 1 of group 3 (MD) |
| | DS2NB | | | DSADC: negative analog of input channel 2, pin B |
| | CCPOS1B | | | CCU60 input |
| | SENT1A | | | SENT input |
| **42** | P40.2 | I | **S / HighZ / VDDM** | General-purpose inpu.t |
| | VADCG3.2 | | | VADC analog input channel 2 of group 3 (MD) |
| | CCPOS1D | | | CCU60 input |
| | SENT2A | | | SENT input |
| **41** | P40.3 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG3.3 | | | VADC analog input channel 3 of group 3 |
| | CCPOS2B | | | CCU60 input |
| | SENT3A | | | SENT input |

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**Table 2-14 Port 40 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **38** | P40.4 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.0 | | | VADC analog input channel 0 of group 4 |
| | CCPOS2D | | | CCU60 input |
| | SENT4A | | | SENT input |
| **37** | P40.5 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.1 | | | VADC analog input channel 1 of group 4 (MD) |
| | CCPOS0D | | | CCU61 input |
| | SENT5A | | | SENT input |
| **35** | P40.6 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.4 | | | VADC analog input channel 4 of group 4 |
| | DS3PA | | | DSADC: positive analog input of channel 3, pin A |
| | CCPOS1B | | | CCU61 input |
| | SENT6A | | | SENT input |
| **34** | P40.7 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.5 | | | VADC analog input channel 5 of group 4 |
| | DS3NA | | | DSADC: negative analog input of channel 3, pin A |
| | CCPOS1D | | | CCU61 input |
| | SENT7A | | | SENT input |
| **33** | P40.8 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.6 | | | VADC analog input channel 6 of group 4 |
| | DS3PB | | | DSADC: positive analog input of channel 3, pin B |
| | CCPOS2B | | | CCU61 input |
| | SENT8A | | | SENT input |
| **32** | P40.9 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.7 | | | VADC analog input channel 7 of group 4 |
| | DS3NB | | | DSADC: negative analog input of channel 3, pin B |
| | CCPOS2D | | | CCU61 input |
| | SENT9A | | | SENT input |

**Table 2-15 Analog Inputs**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **67** | AN0 | I | **D / HighZ / VDDM** | Analog input 0 |
| | VADCG0.0 | | | VADC analog input channel 0 of group 0 |
| | DS1PA | | | DSADC: positive analog of input channel 1, pin A |
| **66** | AN1 | I | **D / HighZ / VDDM** | Analog input 1 |
| | VADCG0.1 | | | VADC analog input channel 1 of group 0 (MD) |
| | DS1NA | | | DSADC: negative analog input of channel 1, pin A |

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**Table 2-15 Analog Inputs** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **65** | AN2 | I | **D / HighZ / VDDM** | Analog input 2 |
| | VADCG0.2 | | | VADC analog input channel 2 of group 0 (MD) |
| | DS0PA | | | DSADC: positive analog input of channel 0, pin A |
| **64** | AN3 | I | **D / HighZ / VDDM** | Analog input 3 |
| | VADCG0.3 | | | VADC analog input channel 3 of group 0 |
| | DS0NA | | | DSADC: negative analog input of channel 0, pin A |
| **63** | AN4 | I | **D / HighZ / VDDM** | Analog input 4 |
| | VADCG0.4 | | | VADC analog input channel 4 of group 0 |
| **62** | AN5 | I | **D / HighZ / VDDM** | Analog input 5 |
| | VADCG0.5 | | | VADC analog input channel 5 of group 0 |
| **61** | AN6 | I | **D / HighZ / VDDM** | Analog input 6 |
| | VADCG0.6 | | | VADC analog input channel 6 of group 0 |
| **60** | AN7 | I | **D / HighZ / VDDM** | Analog input 7 |
| | VADCG0.7 | | | VADC analog input channel 7 of group 0 (with pull down diagnostics) |
| **59** | AN8 | I | **D / HighZ / VDDM** | Analog input 8 |
| | VADCG1.0 | | | VADC analog input channel 0 of group 1 |
| **58** | AN10 | I | **D / HighZ / VDDM** | Analog input 10 |
| | VADCG1.2 | | | VADC analog input channel 2 of group 1 (MD) |
| **57** | AN11 | I | **D / HighZ / VDDM** | Analog input 11 |
| | VADCG1.3 | | | VADC analog input channel 3 of group 1 (with pull down diagnostics) |
| **56** | AN12 | I | **D / HighZ / VDDM** | Analog input 12 |
| | VADCG1.4 | | | VADC analog input channel 4 of group 1 |
| **55** | AN13 | I | **D / HighZ / VDDM** | Analog input 13 |
| | VADCG1.5 | | | VADC analog input channel 5 of group 1 |
| **50** | AN16 | I | **D / HighZ / VDDM** | Analog input 16 |
| | VADCG2.0 | | | VADC analog input channel 0 of group 2 |
| **49** | AN17 | I | **D / HighZ / VDDM** | Analog input 17 |
| | VADCG2.1 | | | VADC analog input channel 1 of group 2 (MD) |
| **48** | AN18 | I | **D / HighZ / VDDM** | Analog input 18 |
| | VADCG2.2 | | | VADC analog input channel 2 of group 2 (MD) |

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**Table 2-15 Analog Inputs** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **47** | AN19 | I | **D / HighZ / VDDM** | Analog input 19 |
| | VADCG2.3 | | | VADC analog input channel 3 of group 2 (with pull down diagnostics) |
| **46** | AN20 | I | **D / HighZ / VDDM** | Analog input 20 |
| | VADCG2.4 | I | | VADC analog input channel 4 of group 2 |
| | DS2PA | I | | DSADC: positive analog input of channel 2, pin A |
| **45** | AN21 | I | **D / HighZ / VDDM** | Analog input 21 |
| | VADCG2.5 | I | | VADC analog input channel 5 of group 2 |
| | DS2NA | I | | DSADC: negative analog input of channel of DSADC 2, pin A |
| **44** | AN24 | I | **S / HighZ / VDDM** | Analog input 24 |
| | VADCG3.0 | | | VADC analog input channel 0 of group 3 |
| | DS2PB | | | DSADC: positive analog input of channel 2, pin B |
| | SENT0A | | | SENT input channel 0, pin A |
| **43** | AN25 | I | **S / HighZ / VDDM** | Analog input 24 |
| | VADCG3.1 | | | VADC analog input channel 1 of group 3 (MD) |
| | DS2NB | | | DSADC: negative analog input of channel 2, pin B |
| | SENT1A | | | SENT input channel 1, pin A |
| **42** | AN26 | I | **S / HighZ / VDDM** | Analog input 26 |
| | VADCG3.2 | | | VADC analog input channel 2 of group 3 (MD) |
| | SENT2A | | | SENT input channel 2, pin A |
| **41** | AN27 | I | **S / HighZ / VDDM** | Analog input 27 |
| | VADCG3.3 | | | VADC analog input channel 3 of group 3 (with pull down diagnostics) |
| | SENT3A | | | SENT input channel 3, pin A |
| **40** | AN28 | I | **D / HighZ / VDDM** | Analog input 28 |
| | VADCG3.4 | | | VADC analog input channel 4 of group 3 |
| **39** | AN29 | I | **D / HighZ / VDDM** | Analog input 29 |
| | VADCG3.5 | | | VADC analog input channel 5 of group 3 |
| **38** | AN32 | I | **S / HighZ / VDDM** | Analog input 32 |
| | VADCG4.0 | | | VADC analog input channel 0 of group 4 |
| | SENT4A | | | SENT input channel 4, pin A |
| **37** | AN33 | I | **S / HighZ / VDDM** | Analog input 33 |
| | VADCG4.1 | | | VADC analog input channel 1 of group 4 (MD) |
| | SENT5A | | | SENT input channel 5, pin A |
| **36** | AN35 | I | **D / HighZ / VDDM** | Analog input 35 |
| | VADCG4.3 | | | VADC analog input channel 3 of group 4 (with pull down diagnostics) |

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**Table 2-15 Analog Inputs** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **35** | AN36 | I | **S / HighZ / VDDM** | Analog input 34 |
| | VADCG4.4 | | | VADC analog input channel 4 of group 4 |
| | DS3PA | | | DSADC: positive analog input of channel of DSADC 3, pin A |
| | SENT6A | | | SENT input channel 6, pin A |
| **34** | AN37 | I | **S / HighZ / VDDM** | Analog input 37 |
| | VADCG4.5 | | | VADC analog input channel 5 of group 4 |
| | DS3NA | | | DSADC: negative analog input of channel of DSADC 3, pin A |
| | SENT7A | | | SENT input channel 7, pin A |
| **33** | AN38 | I | **S / HighZ / VDDM** | Analog input 38 |
| | VADCG4.6 | | | VADC analog input channel 6 of group 4 |
| | DS3PB | | | DSADC: positive analog input of channel of DSADC 3, pin B |
| | SENT8A | | | SENT input channel 8, pin A |
| **32** | AN39 | I | **S / HighZ / VDDM** | Analog input 39 |
| | VADCG4.7 | | | VADC analog input channel 7 of group 4 |
| | DS3NB | | | DSADC: negative analog input of channel of DSADC 3, pin B |
| | SENT9A | | | SENT input channel 9, pin A |
| **31** | AN44 | I | **D / HighZ / VDDM** | Analog input 44 |
| | VADCG5.4 | | | VADC analog input channel 4 of group 5 |
| | DS3PC | | | DSADC: positive analog input of channel of DSADC 3, pin C |
| **30** | AN45 | I | **D / HighZ / VDDM** | Analog input 45 |
| | VADCG5.5 | | | VADC analog input channel 5 of group 5 |
| | DS3NC | | | DSADC: negative analog input of channel of DSADC 3, pin C |
| **29** | AN46 | I | **D / HighZ / VDDM** | Analog input 46 |
| | VADCG5.6 | | | VADC analog input channel 6 of group 5 |
| | DS3PD | | | DSADC: positive analog input of channel of DSADC 3, pin D |
| **28** | AN47 | I | **D / HighZ / VDDM** | Analog input 47 |
| | VADCG5.7 | | | VADC analog input channel 7 of group 5 |
| | DS3ND | | | DSADC: negative analog input of channel of DSADC 3, pin D |

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**Table 2-16 System I/O**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **121** | $\overline{\text{PORST}}$ | I | **I / PD / VEXT** | Power On Reset Input<br>Additional strong PD in case of power fail. |
| **122** | $\overline{\text{ESR0}}$ | I/O | **MP / OD / VEXT** | External System Request Reset 0<br>Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of $\overline{\text{PORST}}$ until the internal reset phase has finished. See also SCU chapter for details.<br>Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. |
| | EVRWUP | I | | EVR Wakeup Pin |
| **120** | $\overline{\text{ESR1}}$ | I/O | **MP / PU1 / VEXT** | External System Request Reset 1<br>Default NMI function.<br>See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. |
| | EVRWUP | I | | EVR Wakeup Pin |
| **85** | VGATE1P | O | **VGATE1P / - / VEXT** | External Pass Device gate control for EVR13 |
| **112** | TMS | I | **A2 / PD / VDDP3** | JTAG Module State Machine Control Input |
| | DAP1 | I/O | | Device Access Port Line 1 |
| **114** | $\overline{\text{TRST}}$ | I | **A2 / PD / VDDP3** | JTAG Module Reset/Enable Input |
| **115** | TCK | I | **A2 / PD / VDDP3** | JTAG Module Clock Input |
| | DAP0 | I | | Device Access Port Line 0 |
| **102** | XTAL1 | I | **XTAL1 / - / VDDP3** | Main Oscillator/PLL/Clock Generator Input |
| **103** | XTAL2 | O | **XTAL2 / - / VDDP3** | Main Oscillator/PLL/Clock Generator Output |

**Table 2-17 Supply**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **52** | VAREF1 | I | **Vx** | Positive Analog Reference Voltage 1 |
| **51** | VAGND1 | I | **Vx** | Negative Analog Reference Voltage 1 |

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**Table 2-17 Supply** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **26** | VAREF2 | I | **Vx** | Positive Analog Reference Voltage 2 |
| **27** | VAGND2 | I | **Vx** | Negative Analog Reference Voltage 2 |
| **54** | VDDM | I | **Vx** | ADC Analog Power Supply (3.3V / 5V) |
| **101** | VSS | I | **Vx** | Digital Ground |
| **10** | VDD / VDDSB | I | **Vx** | Emulation Device: Emulation SRAM Standby Power Supply (1.3V) (Emulation Device only).<br>Production Device: VDD (1.3V). |
| **123, 68, 24** | VDD | I | **Vx** | Digital Core Power Supply (1.3V) |
| **100** | VDD | I | **Vx** | Digital Core Power Supply (1.3V).<br>The supply pin inturn supplies the main XTAL Oscillator/PLL (1.3V) . A higher decoupling capacitor is therefore recommended to the VSS pin for better noise immunity. |
| **153, 99, 69, 25** | VEXT | I | **Vx** | External Power Supply (5V / 3.3V) |
| **154** | VDDP3 | I | **Vx** | Digital Power Supply for Flash (3.3V).<br>Can be also used as external 3.3V Power Supply for VFLEX. |
| **104** | VDDP3 | I | **Vx** | Digital Power Supply for Oscillator, LVDSH and A2 pads (3.3V).<br>The supply pin inturn supplies the main XTAL Oscillator/PLL (3.3V) . A higher decoupling capacitor is therefore recommended to the VSS pin for better noise immunity. |
| **155** | VDDFL3 | I | **Vx** | Flash Power Supply (3.3V) |
| **164** | VFLEX | I | **Vx** | Digital Power Supply for Flex Port Pads (5V / 3.3V) |
| **53** | VSSM | I | **Vx** | Analog Ground for VDDM |

**Legend:**

Column "**Ctrl.**":

I = Input (for GPIO port Lines with IOCR bit field Selection PCx = $0XXX_B$)

O = Output

O0 = Output with IOCR bit field selection PCx = $1X000_B$

O1 = Output with IOCR bit field selection PCx = $1X001_B$ (ALT1)

O2 = Output with IOCR bit field selection PCx = $1X010_B$ (ALT2)

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O3 = Output with IOCR bit field selection PCx = $1X011_B$ (ALT3)
O4 = Output with IOCR bit field selection PCx = $1X100_B$ (ALT4)
O5 = Output with IOCR bit field selection PCx = $1X101_B$ (ALT5)
O6 = Output with IOCR bit field selection PCx = $1X110_B$ (ALT6)
O7 = Output with IOCR bit field selection PCx = $1X111_B$ (ALT7)

Column “**Type**”:

LP = Pad class LP (5V/3.3V, LVTTL)
MP = Pad class MP (5V/3.3V, LVTTL)
MP+ = Pad class MP+ (5V/3.3V, LVTTL)
MPR = Pad class MPR (5V/3.3V, LVTTL)
A2 = Pad class A2 (3.3V, LVTTL)
LVDSM = Pad class LVDSM (LVDS/CMOS 5V/3.3V)
LVDSH = Pad class LVDSH (LVDS/CMOS 3.3V)
S = Pad class S (ADC overlayed with General Purpose Input)
D = Pad class D (ADC)
PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PU1 = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
PD1 = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PX = Behavior depends on usage: PD in EVR13 SMPS Mode and PU1 in GPIO Mode
OD = open drain during reset ($\overline{\text{PORST}}$ = 0)
HighZ = tri-state during reset ($\overline{\text{PORST}}$ = 0)
$\overline{\text{PORST}}$ = $\overline{\text{PORST}}$ input pad
XTAL1 = XTAL1 input pad
XTAL2 = XTAL2 input pad
VGATE1P = VGATE1P
VGATE3P = VGATE3P
Vx = Supply (the Exposed Pad is also considered as VSS and shall be connected to ground)
NC = These pins are reserved for future extensions and shall not be connected externally
NC1 = These pins are not connected on package level and will not be used for future extensions
NCVDDPSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.
NCVDDSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.

### 2.1.2 Emergency Stop Function

The Emergency Stop function can be used to force GPIOs (General Purpose Inputs/Outputs) via an external input signal (EMGSTOPA or EMGSTOPB) into a defined state:

- Input state and
- PU or High-Z depending on HWCFG[6] level latched during $\overline{\text{PORST}}$ active

Control of the Emergency Stop function:

1)The default state of GPIOs (Px.y) during and after $\overline{\text{PORST}}$ active is controllled via HWCFG[6] (P14.4). HWCFG[6] has a weak internal pull-up active at start-up if the pin is left unconnected.See also User´s Manual, “Introduction Chapter”, “General Purpose I/O Ports and Peripheral I/O Lines”, Figure: “Default state of port pins during and after reset”.

2) If HWCFG[6] is left unconnected or is externally pulled high, weak internal pull-ups (PU1) / pull-downs (PD1) are active during and after reset.

3) If HWCFG[6] is connected to ground, the PD1 / PU1 pins are predominantly in HighZ during and after reset.

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- The Emergency Stop function can be enabled/disabled in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- The Emergency Stop input signal, EMGSTOPA (P33.8) / EMGSTOPB (P21.2) , can selected in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- On port level, each GPIO can be enabled/disabled for the Emergency Stop function via the Px_ESR (Port x Emergency Stop) registers in the port control logic (see chapter “General Purpose I/O Ports and Peripheral I/O Lines”, “Emergency Stop Register”).

The Emergency Stop function is available for all GPIO Ports with the following exceptions:

- Not available for P20.2 (General Purpose Input/GPI only, overlayed with Testmode)
- Not available for P40.x (analoge input ANx overlayed with GPI)
- Not available for P32.0 EVR13 SMPS mode.
- Not available for dedicated I/O without General Purpose Output function (e.g ESRx, TMS, TCK)

The Emergency Stop function can be overruled on the following GPIO Ports:

- P00.x: Emergency Stop can be overruled by the VADC. Overruling can be disabled via the control register P00_SCR (see chapter “General Purpose I/O Ports and Peripheral I/O Lines”, P00)
- P14.0 and P14.1: Emergency Stop can be overruled in the DXCPL mode (DAP over can physical layer mode). No Overruling in the DXCM (Debug over can message) mode
- P21.6: Emergency Stop can be overruled in JTAG mode if this pin is used as TDI
- P21.7: Emergency Stop can be overruled in JTAG or Three Pin DAP mode
- P20.0: Emergency Stop can be overruled in JTAG mode if this GPIO is used as TDI

### 2.1.3 Pull-Up/Pull-Down Reset Behavior of the Pins

**Table 2-18 List of Pull-Up/Pull-Down Reset Behavior of the Pins**

| Pins | $\overline{\text{PORST}}$ = 0 | $\overline{\text{PORST}}$ = 1 |
|---|---|---|
| $\overline{\text{all GPIOs}}$ | Pull-up if HWCFG[6] = 1 or High-Z if HWCFG[6] = 0 | |
| $\overline{\text{TDI}}$, $\overline{\text{TESTMODE}}$ | Pull-up | |
| $\overline{\text{PORST}}$[1)] | Pull-down with $I_{PORST}$ relevant | Pull-down with $I_{PDLI}$ relevant |
| $\overline{\text{TRST}}$, TCK, TMS | Pull-down | |
| $\overline{\text{ESR0}}$ | The open-drain driver is used to drive low.[2)] | Pull-up[3)] |
| $\overline{\text{ESR1}}$ | Pull-up[3)] | |
| TDO | Pull-up | High-Z/Pull-up[4)] |

1) Pull-down with $I_{PORST}$ relevant is always activated when a primary supply monitor detects a violation.
2)Valid additionally after deactivation of $\overline{\text{PORST}}$ until the internal reset phase has finished. See the SCU chapter for details.
3) See the SCU_IOCR register description.
4) Depends on JTAG/DAP selection with $\overline{\text{TRST}}$.

In case of leakage test ($\overline{\text{PORST}}$ = 0 and $\overline{\text{TESTMODE}}$ = 0), the pull-down of the $\overline{\text{TRST}}$ pin is switched off. In case of an user application ($\overline{\text{TESTMODE}}$ = 1), the pull-down of the $\overline{\text{TRST}}$ is always switched on.

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## 2.2 TC277x Pin Definition and Functions: BGA292

**Figure 2-2** is showing the TC277x Logic Symbol for the package variant: BGA292.

| | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Y | VSS | P32.3 | P32.2 | P32.0 | P33.13 | P33.11 | P33.9 | P33.7 | P33.5 | P33.3 | P33.1 | AN5 | AN10 | VAGND1 | VAREF1 | VDDM | VSSM | AN20 | AN21 | NC | Y |
| W | VEXT | VSS | P32.4 | VGATE1P | P33.12 | P33.10 | P33.8 | P33.6 | P33.4 | P33.2 | P33.0 | AN2 | AN8 | AN11 | AN13 | AN16 | AN18 | AN19 | AN24 | AN25 | W |
| V | P23.0 | VEXT | | | | | | | | | | | | | | | | | AN26 | AN27 | V |
| U | P23.2 | P23.1 | U | VSS | P32.7 | P32.6 | P33.15 | P34.5 | P34.3 | P34.1 | AN1 | AN3 | AN7 | AN9 | AN14 | AN17 | NC | U | AN28 | AN29 | U |
| T | P23.4 | P23.3 | T | P23.5 | VSS | P32.5 | P33.14 | P34.4 | P34.2 | VEVRSB | AN0 | AN4 | AN6 | AN12 | AN15 | AN22 | AN30 | T | VAGND2 | VAREF2 | T |
| R | P22.2 | P22.3 | R | P23.6 | P23.7 | Top-View | | | | | | | | | | AN23 | AN31 | R | AN35 | AN33 | R |
| P | P22.0 | P22.1 | P | P22.5 | P22.4 | | | VDD | VSS | VSS (AGBT TXDP) | VSS (AGBT TXDN) | VSS | VDD | | | AN34 | AN32 | P | AN37 | AN39 | P |
| N | VDDP3 | VDD | N | P22.7 | P22.6 | | VDD | | VSS | VSS | VSS | VSS | | VDD | | AN38 | AN36 | N | AN45 | AN44 | N |
| M | XTAL1 | XTAL2 | M | P22.9 | P22.8 | | VSS | VSS | | VSS | VSS | | VSS | VSS | | AN40 | AN41 | M | AN47 | AN46 | M |
| L | VSS | TRST | L | P22.11 | P22.10 | | VSS (AGBT ERR) | VSS | VSS | VSS | VSS | VSS | VSS | VSS (AGBT CLKN) | | AN42 | AN43 | L | P00.12 | P00.11 | L |
| K | P21.4 | P21.2 | K | P21.0 | TMS | | NC (VDDPSB) | VSS | VSS | VSS | VSS | VSS | VSS | VSS (AGBT CLKP) | | P00.10 | P00.8 | K | P00.9 | P00.7 | K |
| J | P21.5 | P21.3 | J | P21.1 | TCK | | VSS | VSS | | VSS | VSS | | VSS | VSS | | P01.7 | P00.6 | J | P00.5 | P00.4 | J |
| H | P20.0 | P20.2 | H | P21.6 | P21.7 | | VDD | | VSS | VSS | VSS | VSS | | VDD (VDDSB) | | P01.5 | P01.6 | H | P00.3 | P00.2 | H |
| G | P20.3 | P20.1 | G | PORST | ESR1 | | | VDD | VSS | VSS | VSS | VSS | VDD (VDDSB) | | | P01.3 | P01.4 | G | P00.1 | P00.0 | G |
| F | P20.8 | P20.7 | F | P20.6 | ESR0 | | | | | | | | | | | P02.10 | P02.11 | F | P02.7 | P02.8 | F |
| E | P20.11 | P20.10 | E | P20.9 | VSS | VDDFL3 | P15.5 | P14.2 | P12.0 | P12.1 | P11.0 | P11.1 | P11.7 | P11.8 | P11.13 | VSS | P02.9 | E | P02.5 | P02.6 | E |
| D | P20.13 | P20.12 | D | VSS | VDDFL3 | P15.7 | P15.8 | P14.7 | P14.9 | P14.10 | P11.4 | P11.6 | P11.5 | P11.14 | P11.15 | VFLEX | VSS | D | P02.3 | P02.4 | D |
| | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | | | | | | | |
| C | P20.14 | P15.2 | | | | | | | | | | | | | | | | | P02.1 | P02.2 | C |
| B | P15.0 | VSS | VDDP3 | P15.3 | P14.0 | P14.4 | P14.3 | P14.6 | P13.0 | P13.2 | P11.3 | P11.10 | P11.12 | P10.1 | P10.4 | P10.5 | P10.8 | VEXT | VSS | P02.0 | B |
| A | VSS | VDDP3 | P15.1 | P15.4 | P15.6 | P14.1 | P14.5 | P14.8 | P13.1 | P13.3 | P11.2 | P11.9 | P11.11 | P10.0 | P10.3 | P10.2 | P10.6 | P10.7 | VEXT | NC | A |
| | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |

**Figure 2-2 TC277x Logic Symbol for the package variant BGA292.**

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### 2.2.1 TC277xBGA292 Package Variant Pin Configuration

**Table 2-19 Port 00 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **G1** | P00.0 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN9 | | | GTM input |
| | $\overline{\text{CTRAPA}}$ | | | CCU61 input |
| | T12HRE | | | CCU60 input |
| | INJ00 | | | MSC0 input |
| | CIFD9 | | | CIF input |
| | P00.0 | O0 | | General-purpose output |
| | TOUT9 | O1 | | GTM output |
| | ASCLK3 | O2 | | ASCLIN3 output |
| | ATX3 | O3 | | ASCLIN3 output |
| | – | O4 | | Reserved |
| | TXDCAN1 | O5 | | CAN node 1 output |
| | – | O6 | | Reserved |
| | COUT63 | O7 | | CCU60 output |
| | ETHMDIOA | HWOUT | | ETH input/output |
| **G2** | P00.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN10 | | | GTM input |
| | ARX3E | | | ASCLIN3 input |
| | RXDCAN1D | | | CAN node 1 input |
| | PSIRX0A | | | PSI5 input |
| | SENT0B | | | SENT input |
| | CC60INB | | | CCU60 input |
| | CC60INA | | | CCU61 input |
| | DSCIN5A | | | DSADC channel 5 input A |
| | DS5NA | | | DSADC negative analog input of channel 5, pin A |
| | VADCG7.5 | | | VADC analog input channel 5 of group 7 |
| | CIFD10 | | | CIF input |
| | P00.1 | O0 | | General-purpose output |
| | TOUT10 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | DSCOUT5 | O4 | | DSADC channel 5 output |
| | – | O5 | | Reserved |
| | SPC0 | O6 | | SENT output |
| | CC60 | O7 | | CCU61 output |

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**Table 2-19 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **H1** | P00.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN11 | | | GTM input |
| | SENT1B | | | SENT input |
| | DSDIN5A | | | DSADC channel 5 input A |
| | DS5PA | | | DSADC positive analog input of channel 5, pin A |
| | VADCG7.4 | | | VADC analog input channel 4 of group 7 |
| | CIFD11 | | | CIF input |
| | P00.2 | O0 | | General-purpose output |
| | TOUT11 | O1 | | GTM output |
| | ASCLK3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | PSITX0 | O4 | | PSI5 output |
| | TXDCAN3 | O5 | | CAN node 3 output |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU61 output |
| **H2** | P00.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN12 | | | GTM input |
| | RXDCAN3A | | | CAN node 3 input |
| | PSIRX1A | | | PSI5 input |
| | PSISRXA | | | PSI5-S input |
| | SENT2B | | | SENT input |
| | CC61INB | | | CCU60 input |
| | CC61INA | | | CCU61 input |
| | DSCIN3A | | | DSADC channel 3 input A |
| | VADCG7.3 | | | VADC analog input channel 3 of group 7 |
| | DSITR5F | | | DSADC channel 5 input F |
| | CIFD12 | | | CIF input |
| | P00.3 | O0 | | General-purpose output |
| | TOUT12 | O1 | | GTM output |
| | ASLSO3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | DSCOUT3 | O4 | | DSADC channel 3 output |
| | – | O5 | | Reserved |
| | SPC2 | O6 | | SENT output |
| | CC61 | O7 | | CCU61 output |

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**Table 2-19 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **J1** | P00.4 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN13 | | | GTM input |
| | REQ7 | | | SCU input |
| | SENT3B | | | SENT input |
| | DSDIN3A | | | DSADC channel 3 input A |
| | DSSGNA | | | DSADC input |
| | VADCG7.2 | | | VADC analog input channel 2 of group 7 (MD) |
| | CIFD13 | | | CIF input |
| | P00.4 | O0 | | General-purpose output |
| | TOUT13 | O1 | | GTM output |
| | PSISTX | O2 | | PSI5-S output |
| | – | O3 | | Reserved |
| | PSITX1 | O4 | | PSI5 output |
| | VADCG4BFL0 | O5 | | VADC output |
| | SPC3 | O6 | | SENT output |
| | COUT61 | O7 | | CCU61 output |
| **J2** | P00.5 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN14 | | | GTM input |
| | PSIRX2A | | | PSI5 input |
| | SENT4B | | | SENT input |
| | CC62INB | | | CCU60 input |
| | CC62INA | | | CCU61 input |
| | DSCIN2A | | | DSADC channel 2 input A |
| | VADCG7.1 | | | VADC analog input channel 1 of group 7 (MD) |
| | CIFD14 | | | CIF input |
| | P00.5 | O0 | | General-purpose output |
| | TOUT14 | O1 | | GTM output |
| | DSCGPWMN | O2 | | DSADC output |
| | – | O3 | | Reserved |
| | DSCOUT2 | O4 | | DSADC channel 2 output |
| | VADCG4BFL1 | O5 | | VADC output |
| | SPC4 | O6 | | SENT output |
| | CC62 | O7 | | CCU61 output |

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**Table 2-19 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **J4** | P00.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN15 | | | GTM input |
| | SENT5B | | | SENT input |
| | DSDIN2A | | | DSADC channel 2 input A |
| | VADCG7.0 | | | VADC analog input channel 0 of group 7 |
| | DSITR4F | | | DSADC channel 4 input F |
| | CIFD15 | | | CIF input |
| | P00.6 | O0 | | General-purpose output |
| | TOUT15 | O1 | | GTM output |
| | DSCGPWMP | O2 | | DSADC output |
| | VADCG4BFL2 | O3 | | VADC output |
| | PSITX2 | O4 | | PSI5 output |
| | VADCEMUX10 | O5 | | VADC output |
| | SPC5 | O6 | | SENT output |
| | COUT62 | O7 | | CCU61 output |
| **K1** | P00.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN16 | | | GTM input |
| | SENT6B | | | SENT input |
| | CC60INC | | | CCU61 input |
| | CCPOS0A | | | CCU61 input |
| | T12HRB | | | CCU60 input |
| | T2INA | | | GPT120 input |
| | DSCIN4A | | | DSADC channel 4 input A |
| | DS4NA | | | DSADC negative analog input of channel 4, pin A |
| | VADCG6.5 | | | VADC analog input channel 5 of group 6 |
| | CIFCLK | | | CIF input |
| | P00.7 | O0 | | General-purpose output |
| | TOUT16 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | VADCG4BFL3 | O3 | | VADC output |
| | DSCOUT4 | O4 | | DSADC channel 4 output |
| | VADCEMUX11 | O5 | | VADC output |
| | SPC6 | O6 | | SENT output |
| | CC60 | O7 | | CCU61 output |

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**Table 2-19 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **K4** | P00.8 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN17 | | | GTM input |
| | SENT7B | | | SENT input |
| | CC61INC | | | CCU61 input |
| | CCPOS1A | | | CCU61 input |
| | T13HRB | | | CCU60 input |
| | T2EUDA | | | GPT120 input |
| | DSDIN4A | | | DSADC channel 4 input A |
| | DS4PA | | | DSADC channel 4 input A |
| | VADCG6.4 | | | VADC analog input channel 4 of group 6 |
| | CIFVSNC | | | CIF input |
| | P00.8 | O0 | | General-purpose output |
| | TOUT17 | O1 | | GTM output |
| | SLSO36 | O2 | | QSPI3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | VADCEMUX12 | O5 | | VADC output |
| | SPC7 | O6 | | SENT output |
| | CC61 | O7 | | CCU61 output |

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**Table 2-19 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **K2** | P00.9 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN18 | | | GTM input |
| | SENT8B | | | SENT input |
| | CC62INC | | | CCU61 input |
| | CCPOS2A | | | CCU61 input |
| | T13HRC | | | CCU60 input |
| | T12HRC | | | CCU60 input |
| | T4EUDA | | | GPT120 input |
| | DSCIN1A | | | DSADC channel 1 input A |
| | VADCG6.3 | | | VADC analog input channel 3 of group 6 |
| | DSITR3F | | | DSADC channel 3 input F |
| | CIFHSNC | | | CIF input |
| | P00.9 | O0 | | General-purpose output |
| | TOUT18 | O1 | | GTM output |
| | SLSO37 | O2 | | QSPI3 output |
| | ARTS3 | O3 | | ASCLIN3 output |
| | DSCOUT1 | O4 | | DSADC channel 1 output |
| | – | O5 | | Reserved |
| | SPC8 | O6 | | SENT output |
| | CC62 | O7 | | CCU61 output |
| **K5** | P00.10 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN19 | | | GTM input |
| | SENT9B | | | SENT input |
| | DSDIN1A | | | DSADC channel 1 input A |
| | VADCG6.2 | | | VADC analog input channel 2 of group 6 (MD) |
| | P00.10 | O0 | | General-purpose output |
| | TOUT19 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | SPC9 | O6 | | SENT output |
| | COUT63 | O7 | | CCU61 output |

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**Table 2-19 Port 00 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **L1** | P00.11 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN20 | | | GTM input |
| | $\overline{\text{CTRAPA}}$ | | | CCU60 input |
| | T12HRE | | | CCU61 input |
| | DSCIN0A | | | DSADC channel 0 input A |
| | VADCG6.1 | | | VADC analog input channel 1 of group 6 (MD) |
| | P00.11 | O0 | | General-purpose output |
| | TOUT20 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | DSCOUT0 | O4 | | DSADC channel 0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **L2** | P00.12 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN21 | | | GTM input |
| | ACTS3A | | | ASCLIN3 input |
| | DSDIN0A | | | DSADC channel 0 input A |
| | VADCG6.0 | | | VADC analog input channel 0 of group 6 |
| | P00.12 | O0 | | General-purpose output |
| | TOUT21 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT63 | O7 | | CCU61 output |

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**Table 2-20 Port 01 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **G5** | P01.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN111 | | | GTM input |
| | $\overline{\text{SLSI3B}}$ | | | QSPI3 input |
| | P01.3 | O0 | | General-purpose output |
| | TOUT111 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | SLSO39 | O4 | | QSPI3 output |
| | TXDCAN1 | O5 | | CAN node 1 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **G4** | P01.4 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN112 | | | GTM input |
| | RXDCAN1C | | | CAN node 1 input |
| | P01.4 | O0 | | General-purpose output |
| | TOUT112 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | SLSO310 | O4 | | QSPI3 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **H5** | P01.5 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN113 | | | GTM input |
| | MRST3C | | | QSPI3 input |
| | P01.5 | O0 | | General-purpose output |
| | TOUT113 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | MRST3 | O4 | | QSPI3 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-20 Port 01 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **H4** | P01.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN114 | | | GTM input |
| | MTSR3C | | | QSPI3 input |
| | P01.6 | O0 | | General-purpose output |
| | TOUT114 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | MTSR3 | O4 | | QSPI3 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **J5** | P01.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN115 | | | GTM input |
| | SCLK3C | | | QSPI3 input |
| | P01.7 | O0 | | General-purpose output |
| | TOUT115 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | SCLK3 | O4 | | QSPI3 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-21 Port 02 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **B1** | P02.0 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN0 | | | GTM input |
| | ARX2G | | | ASCLIN2 input |
| | REQ6 | | | SCU input |
| | CC60INA | | | CCU60 input |
| | CC60INB | | | CCU61 input |
| | CIFD0 | | | CIF input |
| | P02.0 | O0 | | General-purpose output |
| | TOUT0 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO31 | O3 | | QSPI3 output |
| | DSCGPWMN | O4 | | DSADC output |
| | TXDCAN0 | O5 | | CAN node 0 output |
| | TXDA | O6 | | ERAY output |
| | CC60 | O7 | | CCU60 output |
| **C2** | P02.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN1 | | | GTM input |
| | REQ14 | | | SCU input |
| | ARX2B | | | ASCLIN2 input |
| | RXDCAN0A | | | CAN node 0 input |
| | RXDA2 | | | ERAY input |
| | CIFD1 | | | CIF input |
| | P02.1 | O0 | | General-purpose output |
| | TOUT1 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO32 | O3 | | QSPI3 output |
| | DSCGPWMP | O4 | | DSADC output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU60 output |

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**Table 2-21 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **C1** | P02.2 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN2 | | | GTM input |
| | CC61INA | | | CCU60 input |
| | CC61INB | | | CCU61 input |
| | CIFD2 | | | CIF input |
| | P02.2 | O0 | | General-purpose output |
| | TOUT2 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | SLSO33 | O3 | | QSPI3 output |
| | PSITX0 | O4 | | PSI5 output |
| | TXDCAN2 | O5 | | CAN node 2 output |
| | TXDB | O6 | | ERAY output |
| | CC61 | O7 | | CCU60 output |
| **D2** | P02.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN3 | | | GTM input |
| | ARX1G | | | ASCLIN1 input |
| | RXDCAN2B | | | CAN node 2 input |
| | RXDB2 | | | ERAY input |
| | PSIRX0B | | | PSI5 input |
| | DSCIN5B | | | DSADC channel 5 input B |
| | SDI11 | | | MSC1 input |
| | CIFD3 | | | CIF input |
| | P02.3 | O0 | | General-purpose output |
| | TOUT3 | O1 | | GTM output |
| | ASLSO2 | O2 | | ASCLIN2 output |
| | SLSO34 | O3 | | QSPI3 output |
| | DSCOUT5 | O4 | | DSADC channel 5 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT61 | O7 | | CCU60 output |

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**Table 2-21 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **D1** | P02.4 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN4 | | | GTM input |
| | SLSI3A | | | QSPI3 input |
| | ECTT1 | | | TTCAN input |
| | RXDCAN0D | | | CAN node 0 input |
| | CC62INA | | | CCU60 input |
| | CC62INB | | | CCU61 input |
| | DSDIN5B | | | DSADC channel 5 input B |
| | SDA0A | | | I2C0 input |
| | CIFD4 | | | CIF input |
| | P02.4 | O0 | | General-purpose output |
| | TOUT4 | O1 | | GTM output |
| | ASCLK2 | O2 | | ASCLIN2 output |
| | SLSO30 | O3 | | QSPI3 output |
| | PSISCLK | O4 | | PSI5-S output |
| | SDA0 | O5 | | I2C0 output |
| | TXENA | O6 | | ERAY output |
| | CC62 | O7 | | CCU60 output |
| **E2** | P02.5 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN5 | | | GTM input |
| | MRST3A | | | QSPI3 input |
| | ECTT2 | | | TTCAN input |
| | PSIRX1B | | | PSI5 input |
| | PSISRXB | | | PSI5-S input |
| | SENT3C | | | SENT input |
| | DSCIN4B | | | DSADC channel 4 input B |
| | SCL0A | | | I2C0 input |
| | CIFD5 | | | CIF input |
| | P02.5 | O0 | | General-purpose output |
| | TOUT5 | O1 | | GTM output |
| | TXDCAN0 | O2 | | CAN node 0 output |
| | MRST3 | O3 | | QSPI3 output |
| | DSCOUT4 | O4 | | DSADC channel 4 output |
| | SCL0 | O5 | | I2C0 output |
| | TXENB | O6 | | ERAY output |
| | COUT62 | O7 | | CCU60 output |

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**Table 2-21 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **E1** | P02.6 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN6 | | | GTM input |
| | MTSR3A | | | QSPI3 input |
| | SENT2C | | | SENT input |
| | CC60INC | | | CCU60 input |
| | CCPOS0A | | | CCU60 input |
| | T12HRB | | | CCU61 input |
| | T3INA | | | GPT120 input |
| | CIFD6 | | | CIF input |
| | DSDIN4B | | | DSADC channel 4 input B |
| | DSITR5E | | | DSADC channel 5 input E |
| | P02.6 | O0 | | General-purpose output |
| | TOUT6 | O1 | | GTM output |
| | PSISTX | O2 | | PSI5-S output |
| | MTSR3 | O3 | | QSPI3 output |
| | PSITX1 | O4 | | PSI5 output |
| | VADCEMUX00 | O5 | | VADC output |
| | – | O6 | | Reserved |
| | CC60 | O7 | | CCU60 output |

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**Table 2-21 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **F2** | P02.7 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN7 | | | GTM input |
| | SCLK3A | | | QSPI3 input |
| | PSIRX2B | | | PSI5 input |
| | SENT1C | | | SENT input |
| | CC61INC | | | CCU60 input |
| | CCPOS1A | | | CCU60 input |
| | T13HRB | | | CCU61 input |
| | T3EUDA | | | GPT120 input |
| | CIFD7 | | | CIF input |
| | DSCIN3B | | | DSADC channel 3 input B |
| | DSITR4E | | | DSADC channel 4 input E |
| | P02.7 | O0 | | General-purpose output |
| | TOUT7 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK3 | O3 | | QSPI3 output |
| | DSCOUT3 | O4 | | DSADC channel 3 output |
| | VADCEMUX01 | O5 | | VADC output |
| | SPC1 | O6 | | SENT output |
| | CC61 | O7 | | CCU60 output |

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**Table 2-21 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **F1** | P02.8 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN8 | | | GTM input |
| | SENT0C | | | SENT input |
| | CC62INC | | | CCU60 input |
| | CCPOS2A | | | CCU60 input |
| | T12HRC | | | CCU61 input |
| | T13HRC | | | CCU61 input |
| | T4INA | | | GPT120 input |
| | CIFD8 | | | CIF input |
| | DSDIN3B | | | DSADC channel 3 input B |
| | DSITR3E | | | DSADC channel 3 input E |
| | P02.8 | O0 | | General-purpose output |
| | TOUT8 | O1 | | GTM output |
| | SLSO35 | O2 | | QSPI3 output |
| | – | O3 | | Reserved |
| | PSITX2 | O4 | | PSI5 output |
| | VADCEMUX02 | O5 | | VADC output |
| | ETHMDC | O6 | | ETH output |
| | CC62 | O7 | | CCU60 output |
| **E4** | P02.9 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN116 | | | GTM input |
| | P02.9 | O0 | | General-purpose output |
| | TOUT116 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | TXDCAN1 | O5 | | CAN node 1 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-21 Port 02 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **F5** | P02.10 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN117 | | | GTM input |
| | ARX2C | | | ASCLIN2 input |
| | RXDCAN1E | | | CAN node 1 input |
| | P02.10 | O0 | | General-purpose output |
| | TOUT117 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **F4** | P02.11 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN118 | | | GTM input |
| | P02.11 | O0 | | General-purpose output |
| | TOUT118 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

**Table 2-22 Port 10 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **A7** | P10.0 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN102 | | | GTM input |
| | T6EUDB | | | GPT120 input |
| | P10.0 | O0 | | General-purpose output |
| | TOUT102 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO110 | O3 | | QSPI1 output |
| | – | O4 | | Reserved |
| | VADCG6BFL0 | O5 | | VADC output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-22 Port 10 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **B7** | P10.1 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN103 | | | GTM input |
| | MRST1A | | | QSPI1 input |
| | T5EUDB | | | GPT120 input |
| | P10.1 | O0 | | General-purpose output |
| | TOUT103 | O1 | | GTM output |
| | MTSR1 | O2 | | QSPI1 output |
| | MRST1 | O3 | | QSPI1 output |
| | EN01 | O4 | | MSC0 output |
| | VADCG6BFL1 | O5 | | VADC output |
| | END03 | O6 | | MSC0 output |
| | – | O7 | | Reserved |
| **A5** | P10.2 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN104 | | | GTM input |
| | SCLK1A | | | QSPI1 input |
| | T6INB | | | GPT120 input |
| | REQ2 | | | SCU input |
| | RXDCAN2E | | | CAN node 2 input |
| | SDI01 | | | MSC0 input |
| | P10.2 | O0 | | General-purpose output |
| | TOUT104 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK1 | O3 | | QSPI1 output |
| | EN00 | O4 | | MSC0 output |
| | VADCG6BFL2 | O5 | | VADC output |
| | END02 | O6 | | MSC0 output |
| | – | O7 | | Reserved |

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**Table 2-22 Port 10 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **A6** | P10.3 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN105 | | | GTM input |
| | MTSR1A | | | QSPI1 input |
| | REQ3 | | | SCU input |
| | T5INB | | | GPT120 input |
| | P10.3 | O0 | | General-purpose output |
| | TOUT105 | O1 | | GTM output |
| | VADCG6BFL3 | O2 | | VADC output |
| | MTSR1 | O3 | | QSPI1 output |
| | EN00 | O4 | | MSC0 output |
| | END02 | O5 | | MSC0 output |
| | TXDCAN2 | O6 | | CAN node 2 output |
| | – | O7 | | Reserved |
| **B6** | P10.4 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN106 | | | GTM input |
| | MTSR1C | | | QSPI1 input |
| | CCPOS0C | | | CCU60 input |
| | T3INB | | | GPT120 input |
| | P10.4 | O0 | | General-purpose output |
| | TOUT106 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO18 | O3 | | QSPI1 output |
| | MTSR1 | O4 | | QSPI1 output |
| | EN00 | O5 | | MSC0 output |
| | END02 | O6 | | MSC0 output |
| | – | O7 | | Reserved |
| **B5** | P10.5 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN107 | | | GTM input |
| | HWCFG4 | | | SCU input |
| | INJ01 | | | MSC0 input |
| | P10.5 | O0 | | General-purpose output |
| | TOUT107 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO38 | O3 | | QSPI3 output |
| | SLSO19 | O4 | | QSPI1 output |
| | T6OUT | O5 | | GPT120 output |
| | ASLSO2 | O6 | | ASCLIN2 output |
| | - | O7 | | Reserved |

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**Table 2-22 Port 10 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **A4** | P10.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN108 | | | GTM input |
| | ARX2D | | | ASCLIN2 input |
| | MTSR3B | | | QSPI3 input |
| | HWCFG5 | | | SCU input |
| | P10.6 | O0 | | General-purpose output |
| | TOUT108 | O1 | | GTM output |
| | ASCLK2 | O2 | | ASCLIN2 output |
| | MTSR3 | O3 | | QSPI3 output |
| | T3OUT | O4 | | GPT120 output |
| | - | O5 | | Reserved |
| | MRST1 | O6 | | QSPI1 output |
| | VADCG7BFL0 | O7 | | VADC output |
| **A3** | P10.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN109 | | | GTM input |
| | ACTS2A | | | ASCLIN2 input |
| | MRST3B | | | QSPI3 input |
| | REQ4 | | | SCU input |
| | CCPOS1C | | | CCU60 input |
| | T3EUDB | | | GPT120 input |
| | P10.7 | O0 | | General-purpose output |
| | TOUT109 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MRST3 | O3 | | QSPI3 output |
| | VADCG7BFL1 | O4 | | VADC output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-22 Port 10 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **B4** | P10.8 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN110 | | | GTM input |
| | SCLK3B | | | QSPI3 input |
| | REQ5 | | | SCU input |
| | CCPOS2C | | | CCU60 input |
| | T4INB | | | GPT120 input |
| | P10.8 | O0 | | General-purpose output |
| | TOUT110 | O1 | | GTM output |
| | ARTS2 | O2 | | ASCLIN2 output |
| | SCLK3 | O3 | | QSPI3 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

**Table 2-23 Port 11 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **E10** | P11.0 | I | **MP+ / PU1 / VFLEX** | General-purpose input |
| | TIN119 | | | GTM input |
| | ARX3B | | | ASCLIN3 input |
| | P11.0 | O0 | | General-purpose output |
| | TOUT119 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ETHTXD3 | O6 | | ETH output |
| | – | O7 | | Reserved |
| **E9** | P11.1 | I | **MP+ / PU1 / VFLEX** | General-purpose input |
| | TIN120 | | | GTM input |
| | P11.1 | O0 | | General-purpose output |
| | TOUT120 | O1 | | GTM output |
| | ASCLK3 | O2 | | ASCLIN3 output |
| | ATX3 | O3 | | ASCLIN3 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ETHTXD2 | O6 | | ETH output |
| | – | O7 | | Reserved |

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**Table 2-23 Port 11 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **A10** | P11.2 | I | **MPR / PU1 / VFLEX** | General-purpose input |
| | TIN95 | | | GTM input |
| | P11.2 | O0 | | General-purpose output |
| | TOUT95 | O1 | | GTM output |
| | END03 | O2 | | MSC0 output |
| | SLSO05 | O3 | | QSPI0 output |
| | SLSO15 | O4 | | QSPI1 output |
| | EN01 | O5 | | MSC0 output |
| | ETHTXD1 | O6 | | ETH output |
| | COUT63 | O7 | | CCU60 output |
| **B10** | P11.3 | I | **MPR / PU1 / VFLEX** | General-purpose input |
| | TIN96 | | | GTM input |
| | MRST1B | | | QSPI1 input |
| | SDI03 | | | MSC0 input |
| | P11.3 | O0 | | General-purpose output |
| | TOUT96 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MRST1 | O3 | | QSPI1 output |
| | TXDA | O4 | | ERAY output |
| | – | O5 | | Reserved |
| | ETHTXD0 | O6 | | ETH output |
| | COUT62 | O7 | | CCU60 output |
| **D10** | P11.4 | I | **MP+ / PU1 / VFLEX** | General-purpose input |
| | TIN121 | | | GTM input |
| | ETHRXCLKB | | | ETH input |
| | P11.4 | O0 | | General-purpose output |
| | TOUT121 | O1 | | GTM output |
| | ASCLK3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ETHTXER | O6 | | ETH output |
| | – | O7 | | Reserved |

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**Table 2-23 Port 11 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **D8** | P11.5 | I | **LP / PU1 / VFLEX** | General-purpose input |
| | TIN122 | | | GTM input |
| | ETHTXCLKA | | | ETH input |
| | P11.5 | O0 | | General-purpose output |
| | TOUT122 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **D9** | P11.6 | I | **MPR / PU1 / VFLEX** | General-purpose input |
| | TIN97 | | | GTM input |
| | SCLK1B | | | QSPI1 input |
| | P11.6 | O0 | | General-purpose output |
| | TOUT97 | O1 | | GTM output |
| | $\overline{\text{TXENB}}$ | O2 | | ERAY output |
| | SCLK1 | O3 | | QSPI1 output |
| | $\overline{\text{TXENA}}$ | O4 | | ERAY output |
| | FCLP0 | O5 | | MSC0 output |
| | ETHTXEN | O6 | | ETH output |
| | COUT61 | O7 | | CCU60 output |
| **E8** | P11.7 | I | **LP / PU1 / VFLEX** | General-purpose input |
| | TIN123 | | | GTM input |
| | ETHRXD3 | | | ETH input |
| | P11.7 | O0 | | General-purpose output |
| | TOUT123 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-23 Port 11 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **E7** | P11.8 | I | **LP / PU1 / VFLEX** | General-purpose input |
| | TIN124 | | | GTM input |
| | ETHRXD2 | | | ETH input |
| | P11.8 | O0 | | General-purpose output |
| | TOUT124 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **A9** | P11.9 | I | **MP+ / PU1 / VFLEX** | General-purpose input |
| | TIN98 | | | GTM input |
| | MTSR1B | | | QSPI1 input |
| | RXDA1 | | | ERAY input |
| | ETHRXD1 | | | ETH input |
| | P11.9 | O0 | | General-purpose output |
| | TOUT98 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MTSR1 | O3 | | QSPI1 output |
| | – | O4 | | Reserved |
| | SOP0 | O5 | | MSC0 output |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU60 output |

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**Table 2-23 Port 11 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **B9** | P11.10 | I | **LP / PU1 / VFLEX** | General-purpose input |
| | TIN99 | | | GTM input |
| | REQ12 | | | SCU input |
| | ARX1E | | | ASCLIN1 input |
| | $\overline{\text{SLSI1A}}$ | | | QSPI1 input |
| | RXDCAN3D | | | CAN node 3 input |
| | RXDB1 | | | ERAY input |
| | ETHRXD0 | | | ETH input |
| | SDI00 | | | MSC0 input |
| | P11.10 | O0 | | General-purpose output |
| | TOUT99 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO03 | O3 | | QSPI0 output |
| | SLSO13 | O4 | | QSPI1 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | CC62 | O7 | | CCU60 output |
| **A8** | P11.11 | I | **MP+ / PU1 / VFLEX** | General-purpose input |
| | TIN100 | | | GTM input |
| | ETHCRSDVA | | | ETH input |
| | ETHRXDVA | | | ETH input |
| | ETHCRSB | | | ETH input |
| | P11.11 | O0 | | General-purpose output |
| | TOUT100 | O1 | | GTM output |
| | END02 | O2 | | MSC0 output |
| | SLSO04 | O3 | | QSPI0 output |
| | SLSO14 | O4 | | QSPI1 output |
| | EN00 | O5 | | MSC0 output |
| | $\overline{\text{TXENB}}$ | O6 | | ERAY output |
| | CC61 | O7 | | CCU60 output |

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**Table 2-23 Port 11 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **B8** | P11.12 | I<br>O0 | **MPR / PU1 / VFLEX** | General-purpose input |
| | TIN101 | | | GTM input |
| | ETHREFCLK | | | ETH input |
| | ETHTXCLKB | | | ETH input<br>(Not for productive purposes) |
| | P11.12 | | | General-purpose output |
| | TOUT101 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | GTMCLK2 | O3 | | GTM output |
| | TXDB | O4 | | ERAY output |
| | TXDCAN3 | O5 | | CAN node 3 output |
| | EXTCLK1 | O6 | | SCU output |
| | CC60 | O7 | | CCU60 output |
| **E6** | P11.13 | I | **LP / PU1 / VFLEX** | General-purpose input |
| | TIN125 | | | GTM input |
| | ETHRXERA | | | ETH input |
| | P11.13 | O0 | | General-purpose output |
| | TOUT125 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **D7** | P11.14 | I | **LP / PU1 / VFLEX** | General-purpose input |
| | TIN126 | | | GTM input |
| | ETHCRSDVB | | | ETH input |
| | ETHRXDVB | | | ETH input |
| | ETHCRSA | | | ETH input |
| | P11.14 | O0 | | General-purpose output |
| | TOUT126 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-23 Port 11 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **D6** | P11.15 | I | **LP / PU1 / VFLEX** | General-purpose input |
| | TIN127 | | | GTM input |
| | ETHCOL | | | ETH input |
| | P11.15 | O0 | | General-purpose output |
| | TOUT127 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

**Table 2-24 Port 12 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **E12** | P12.0 | I | **LP / PU1 / VFLEX** | General-purpose input |
| | TIN128 | | | GTM input |
| | ETHRXCLKC | | | ETH input |
| | RXDCAN0C | | | CAN node 0 input |
| | P12.0 | O0 | | General-purpose output |
| | TOUT128 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ETHMDC | O6 | | ETH output |
| | – | O7 | | Reserved |
| **E11** | P12.1 | I | **LP / PU1 / VFLEX** | General-purpose input |
| | TIN129 | | | GTM input |
| | P12.1 | O0 | | General-purpose output |
| | TOUT129 | O1 | | GTM output |
| | ASLSO3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | TXDCAN0 | O5 | | CAN node 0 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | ETHMDIOC | HWOUT | | ETH input/output |

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**Table 2-25 Port 13 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **B12** | P13.0 | I | **LVDSM_N / PU1 / VEXT** | General-purpose input |
| | TIN91 | | | GTM input |
| | P13.0 | O0 | | General-purpose output |
| | TOUT91 | O1 | | GTM output |
| | END03 | O2 | | MSC0 output |
| | SCLK2N | O3 | | QSPI2 output (LVDS) |
| | EN01 | O4 | | MSC0 output |
| | FCLN0 | O5 | | MSC0 output (LVDS) |
| | FCLND0 | O6 | | MSC0 output (LVDS) |
| | – | O7 | | Reserved |
| **A12** | P13.1 | I | **LVDSM_P / PU1 / VEXT** | General-purpose input |
| | TIN92 | | | GTM input |
| | SCL0B | | | I2C0 input |
| | P13.1 | O0 | | General-purpose output |
| | TOUT92 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK2P | O3 | | QSPI2 output (LVDS) |
| | – | O4 | | Reserved |
| | FCLP0 | O5 | | MSC0 output (LVDS) |
| | SCL0 | O6 | | I2C0 output |
| | – | O7 | | Reserved |
| **B11** | P13.2 | I | **LVDSM_N / PU1 / VEXT** | General-purpose input |
| | TIN93 | | | GTM input |
| | CAPINA | | | GPT120 input |
| | SDA0B | | | I2C0 input |
| | P13.2 | O0 | | General-purpose output |
| | TOUT93 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MTSR2N | O3 | | QSPI2 output (LVDS) |
| | FCLP0 | O4 | | MSC0 output |
| | SON0 | O5 | | MSC0 output (LVDS) |
| | SDA0 | O6 | | I2C0 output |
| | SOND0 | O7 | | MSC0 output (LVDS) |

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**Table 2-25 Port 13 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **A11** | P13.3 | I | **LVDSM_P / PU1 / VEXT** | General-purpose input |
| | TIN94 | | | GTM input |
| | P13.3 | O0 | | General-purpose output |
| | TOUT94 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MTSR2P | O3 | | QSPI2 output (LVDS) |
| | – | O4 | | Reserved |
| | SOP0 | O5 | | MSC0 output (LVDS) |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

**Table 2-26 Port 14 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **B16** | P14.0 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN80 | | | GTM input |
| | P14.0 | O0 | | General-purpose output |
| | TOUT80 | O1 | | GTM output |
| | ATX0 | O2 | | ASCLIN0 output<br>Recommended as Boot loader pin. |
| | TXDA | O3 | | ERAY output |
| | TXDB | O4 | | ERAY output |
| | TXDCAN1 | O5 | | CAN node 1 output<br>Used for single pin DAP (SPD) function. |
| | ASCLK0 | O6 | | ASCLIN0 output |
| | COUT62 | O7 | | CCU60 output |

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**Table 2-26 Port 14 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **A15** | P14.1 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN81 | | | GTM input |
| | REQ15 | | | SCU input |
| | ARX0A | | | ASCLIN0 input<br>Recommended as Boot loader pin. |
| | RXDCAN1B | | | CAN node 1 input<br>Used for single pin DAP (SPD) function. |
| | RXDA3 | | | ERAY input |
| | RXDB3 | | | ERAY input |
| | EVRWUPA | | | SCU input |
| | P14.1 | O0 | | General-purpose output |
| | TOUT81 | O1 | | GTM output |
| | ATX0 | O2 | | ASCLIN0 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT63 | O7 | | CCU60 output |
| **E13** | P14.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN82 | | | GTM input |
| | HWCFG2<br>EVR13 | | | SCU input<br>Latched at cold power on reset to decide EVR13 activation. |
| | P14.2 | O0 | | General-purpose output |
| | TOUT82 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO21 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ASCLK2 | O6 | | ASCLIN2 output |
| | – | O7 | | Reserved |

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**Table 2-26 Port 14 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **B14** | P14.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN83 | | | GTM input |
| | ARX2A | | | ASCLIN2 input |
| | REQ10 | | | SCU input |
| | HWCFG3_BMI | | | SCU input |
| | SDI02 | | | MSC0 input |
| | P14.3 | O0 | | General-purpose output |
| | TOUT83 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO23 | O3 | | QSPI2 output |
| | ASLSO1 | O4 | | ASCLIN1 output |
| | ASLSO3 | O5 | | ASCLIN3 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **B15** | P14.4 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN84 | | | GTM input |
| | HWCFG6 | | | SCU input<br>Latched at cold power on reset to decide default pad reset state (PU or HighZ). |
| | P14.4 | O0 | | General-purpose output |
| | TOUT84 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-26 Port 14 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **A14** | P14.5 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN85 | | | GTM input |
| | HWCFG1<br>EVR33 | | | SCU input<br>Latched at cold power on reset to decide EVR33 activation. |
| | P14.5 | O0 | | General-purpose output |
| | TOUT85 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | TXDB | O6 | | ERAY output |
| | – | O7 | | Reserved |
| **B13** | P14.6 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN86 | | | GTM input |
| | HWCFG0<br>DCLDO | | | SCU input<br>If EVR13 active, latched at cold power on reset to decide between LDO and SMPS mode. |
| | P14.6 | O0 | | General-purpose output |
| | TOUT86 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO22 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | $\overline{\text{TXENB}}$ | O6 | | ERAY output |
| | – | O7 | | Reserved |
| **D13** | P14.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN87 | | | GTM input |
| | RXDB0 | | | ERAY input |
| | P14.7 | O0 | | General-purpose output |
| | TOUT87 | O1 | | GTM output |
| | ARTS0 | O2 | | ASCLIN0 output |
| | SLSO24 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-26 Port 14 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **A13** | P14.8 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN88 | | | GTM input |
| | ARX1D | | | ASCLIN1 input |
| | RXDCAN2D | | | CAN node 2 input |
| | RXDA0 | | | ERAY input |
| | P14.8 | O0 | | General-purpose output |
| | TOUT88 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **D12** | P14.9 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN89 | | | GTM input |
| | ACTS0A | | | ASCLIN0 input |
| | P14.9 | O0 | | General-purpose output |
| | TOUT89 | O1 | | GTM output |
| | END03 | O2 | | MSC0 output |
| | EN01 | O3 | | MSC0 output |
| | – | O4 | | Reserved |
| | $\overline{\text{TXENB}}$ | O5 | | ERAY output |
| | $\overline{\text{TXENA}}$ | O6 | | ERAY output |
| | – | O7 | | Reserved |
| **D11** | P14.10 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN90 | | | GTM input |
| | P14.10 | O0 | | General-purpose output |
| | TOUT90 | O1 | | GTM output |
| | END02 | O2 | | MSC0 output |
| | EN00 | O3 | | MSC0 output |
| | ATX1 | O4 | | ASCLIN1 output |
| | TXDCAN2 | O5 | | CAN node 2 output |
| | TXDA | O6 | | ERAY output |
| | – | O7 | | Reserved |

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**Table 2-27 Port 15 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **B20** | P15.0 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN71 | | | GTM input |
| | P15.0 | O0 | | General-purpose output |
| | TOUT71 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | SLSO013 | O3 | | QSPI0 output |
| | – | O4 | | Reserved |
| | TXDCAN2 | O5 | | CAN node 2 output |
| | ASCLK1 | O6 | | ASCLIN1 output |
| | – | O7 | | Reserved |
| **A18** | P15.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN72 | | | GTM input |
| | REQ16 | | | SCU input |
| | ARX1A | | | ASCLIN1 input |
| | RXDCAN2A | | | CAN node 2 input |
| | $\overline{\text{SLSI2B}}$ | | | QSPI2 input |
| | EVRWUPB | | | SCU input |
| | P15.1 | O0 | | General-purpose output |
| | TOUT72 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | SLSO25 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **C19** | P15.2 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN73 | | | GTM input |
| | $\overline{\text{SLSI2A}}$ | | | QSPI2 input |
| | MRST2E | | | QSPI2 input |
| | P15.2 | O0 | | General-purpose output |
| | TOUT73 | O1 | | GTM output |
| | ATX0 | O2 | | ASCLIN0 output |
| | SLSO20 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | TXDCAN1 | O5 | | CAN node 1 output |
| | ASCLK0 | O6 | | ASCLIN0 output |
| | – | O7 | | Reserved |

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**Table 2-27 Port 15 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **B17** | P15.3 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN74 | | | GTM input |
| | ARX0B | | | ASCLIN0 input |
| | SCLK2A | | | QSPI2 input |
| | RXDCAN1A | | | CAN node 1 input |
| | P15.3 | O0 | | General-purpose output |
| | TOUT74 | O1 | | GTM output |
| | ATX0 | O2 | | ASCLIN0 output |
| | SCLK2 | O3 | | QSPI2 output |
| | END03 | O4 | | MSC0 output |
| | EN01 | O5 | | MSC0 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **A17** | P15.4 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN75 | | | GTM input |
| | MRST2A | | | QSPI2 input |
| | REQ0 | | | SCU input |
| | SCL0C | | | I2C0 input |
| | P15.4 | O0 | | General-purpose output |
| | TOUT75 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | MRST2 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | SCL0 | O6 | | I2C0 output |
| | CC62 | O7 | | CCU60 output |

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**Table 2-27 Port 15 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **E14** | P15.5 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN76 | | | GTM input |
| | ARX1B | | | ASCLIN1 input |
| | MTSR2A | | | QSPI2 input |
| | REQ13 | | | SCU input |
| | SDA0C | | | I2C0 input |
| | P15.5 | O0 | | General-purpose output |
| | TOUT76 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | MTSR2 | O3 | | QSPI2 output |
| | END02 | O4 | | MSC0 output |
| | EN00 | O5 | | MSC0 output |
| | SDA0 | O6 | | I2C0 output |
| | CC61 | O7 | | CCU60 output |
| **A16** | P15.6 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN77 | | | GTM input |
| | MTSR2B | | | QSPI2 input |
| | P15.6 | O0 | | General-purpose output |
| | TOUT77 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | MTSR2 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | SCLK2 | O5 | | QSPI2 output |
| | ASCLK3 | O6 | | ASCLIN3 output |
| | CC60 | O7 | | CCU60 output |
| **D15** | P15.7 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN78 | | | GTM input |
| | ARX3A | | | ASCLIN3 input |
| | MRST2B | | | QSPI2 input |
| | P15.7 | O0 | | General-purpose output |
| | TOUT78 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | MRST2 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU60 output |

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**Table 2-27 Port 15 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **D14** | P15.8 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN79 | | | GTM input |
| | SCLK2B | | | QSPI2 input |
| | REQ1 | | | SCU input |
| | P15.8 | O0 | | General-purpose output |
| | TOUT79 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK2 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ASCLK3 | O6 | | ASCLIN3 output |
| | COUT61 | O7 | | CCU60 output |

**Table 2-28 Port 20 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **H20** | P20.0 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN59 | | | GTM input |
| | RXDCAN3C | | | CAN node 3 input |
| | T6EUDA | | | GPT120 input |
| | REQ9 | | | SCU input |
| | SYSCLK | | | HSCT input |
| | $\overline{\text{TGI0}}$ | | | OCDS input |
| | P20.0 | O0 | | General-purpose output |
| | TOUT59 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | ASCLK3 | O3 | | ASCLIN3 output |
| | – | O4 | | Reserved |
| | SYSCLK | O5 | | HSCT output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | $\overline{\text{TGO0}}$ | HWOUT | | OCDS; ENx |

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**Table 2-28 Port 20 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **G19** | P20.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN60 | | | GTM input |
| | $\overline{\text{TGI1}}$ | | | OCDS input |
| | P20.1 | O0 | | General-purpose output |
| | TOUT60 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | $\overline{\text{TGO1}}$ | HWOUT | | OCDS; ENx |
| **H19** | P20.2 | I | **LP / PU / VEXT** | General-purpose input<br>This pin is latched at power on reset release to enter test mode. |
| | $\overline{\text{TESTMODE}}$ | | | OCDS input |
| | P20.2 | O0 | | Output function not available |
| | – | O1 | | Output function not available |
| | – | O2 | | Output function not available |
| | – | O3 | | Output function not available |
| | – | O4 | | Output function not available |
| | – | O5 | | Output function not available |
| | – | O6 | | Output function not available |
| | – | O7 | | Output function not available |
| **G20** | P20.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN61 | | | GTM input |
| | T6INA | | | GPT120 input |
| | ARX3C | | | ASCLIN3 input |
| | P20.3 | O0 | | General-purpose output |
| | TOUT61 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | SLSO09 | O3 | | QSPI0 output |
| | SLSO29 | O4 | | QSPI2 output |
| | TXDCAN3 | O5 | | CAN node 3 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-28 Port 20 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **F17** | P20.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN62 | | | GTM input |
| | P20.6 | O0 | | General-purpose output |
| | TOUT62 | O1 | | GTM output |
| | ARTS1 | O2 | | ASCLIN1 output |
| | SLSO08 | O3 | | QSPI0 output |
| | SLSO28 | O4 | | QSPI2 output |
| | – | O5 | | Reserved |
| | WDT2LCK | O6 | | SCU output |
| | – | O7 | | Reserved |
| **F19** | P20.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN63 | | | GTM input |
| | ACTS1A | | | ASCLIN1 input |
| | RXDCAN0B | | | CAN node 0 input |
| | P20.7 | O0 | | General-purpose output |
| | TOUT63 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | WDT1LCK | O6 | | SCU output |
| | COUT63 | O7 | | CCU61 output |
| **F20** | P20.8 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN64 | | | GTM input |
| | P20.8 | O0 | | General-purpose output |
| | TOUT64 | O1 | | GTM output |
| | ASLSO1 | O2 | | ASCLIN1 output |
| | SLSO00 | O3 | | QSPI0 output |
| | SLSO10 | O4 | | QSPI1 output |
| | TXDCAN0 | O5 | | CAN node 0 output |
| | WDT0LCK | O6 | | SCU output |
| | CC60 | O7 | | CCU61 output |

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**Table 2-28 Port 20 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **E17** | P20.9 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN65 | | | GTM input |
| | ARX1C | | | ASCLIN1 input |
| | RXDCAN3E | | | CAN node 3 input |
| | REQ11 | | | SCU input |
| | $\overline{\text{SLSI0B}}$ | | | QSPI0 input |
| | P20.9 | O0 | | General-purpose output |
| | TOUT65 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO01 | O3 | | QSPI0 output |
| | SLSO11 | O4 | | QSPI1 output |
| | – | O5 | | Reserved |
| | WDTSLCK | O6 | | SCU output |
| | CC61 | O7 | | CCU61 output |
| **E19** | P20.10 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN66 | | | GTM input |
| | P20.10 | O0 | | General-purpose output |
| | TOUT66 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | SLSO06 | O3 | | QSPI0 output |
| | SLSO27 | O4 | | QSPI2 output |
| | TXDCAN3 | O5 | | CAN node 3 output |
| | ASCLK1 | O6 | | ASCLIN1 output |
| | CC62 | O7 | | CCU61 output |
| **E20** | P20.11 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN67 | | | GTM input |
| | SCLK0A | | | QSPI0 input |
| | P20.11 | O0 | | General-purpose output |
| | TOUT67 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK0 | O3 | | QSPI0 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU61 output |

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**Table 2-28 Port 20 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **D19** | P20.12 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN68 | | | GTM input |
| | MRST0A | | | QSPI0 input |
| | P20.12 | O0 | | General-purpose output |
| | TOUT68 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MRST0 | O3 | | QSPI0 output |
| | MTSR0 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT61 | O7 | | CCU61 output |
| **D20** | P20.13 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN69 | | | GTM input |
| | $\overline{\text{SLSI0A}}$ | | | QSPI0 input |
| | P20.13 | O0 | | General-purpose output |
| | TOUT69 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO02 | O3 | | QSPI0 output |
| | SLSO12 | O4 | | QSPI1 output |
| | SCLK0 | O5 | | QSPI0 output |
| | – | O6 | | Reserved |
| | COUT62 | O7 | | CCU61 output |
| **C20** | P20.14 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN70 | | | GTM input |
| | MTSR0A | | | QSPI0 input |
| | P20.14 | O0 | | General-purpose output |
| | TOUT70 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | MTSR0 | O3 | | QSPI0 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-29 Port 21 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **K17** | P21.0 | I | **A2 / PU1 / VDDP3** | General-purpose input |
| | TIN51 | | | GTM input |
| | P21.0 | O0 | | General-purpose output |
| | TOUT51 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ETHMDC | O6 | | ETH output |
| | – | O7 | | Reserved |
| | HSM1 | HWOUT | | HSM output 1 |
| **J17** | P21.1 | I | **A2 / PU1 / VDDP3** | General-purpose input |
| | TIN52 | | | GTM input |
| | ETHMDIOB | | | ETH input<br>(Not for production purposes) |
| | P21.1 | O0 | | General-purpose output |
| | TOUT52 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | ETHMDIO | O6 | | ETH output<br>(Not for production purposes) |
| | – | O7 | | Reserved |
| | HSM2 | HWOUT | | HSM output 2 |

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**Table 2-29 Port 21 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **K19** | P21.2 | I | **LVDSH_N/ PU1 / VDDP3** | General-purpose input |
| | TIN53 | | | GTM input |
| | MRST2CN | | | QSPI2 input (LVDS) |
| | MRST3FN | | | QSPI3 input (LVDS) |
| | ARX3GN | | | ASCLIN3 input (LVDS) |
| | EMGSTOPB | | | SCU input |
| | RXDN | | | HSCT input (LVDS) |
| | P21.2 | O0 | | General-purpose output |
| | TOUT53 | O1 | | GTM output |
| | ASLSO3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | ETHMDC | O5 | | ETH output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **J19** | P21.3 | I | **LVDSH_P/ PU1 / VDDP3** | General-purpose input |
| | TIN54 | | | GTM input |
| | MRST2CP | | | QSPI2 input (LVDS) |
| | MRST3FP | | | QSPI3 input (LVDS) |
| | ARX3GP | | | ASCLIN3 input (LVDS) |
| | RXDP | | | HSCT input (LVDS) |
| | P21.3 | O0 | | General-purpose output |
| | TOUT54 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | ETHMDIOD | HWOUT | | ETH input/output |

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**Table 2-29 Port 21 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **K20** | P21.4 | I | **LVDSH_N/ PU1 / VDDP3** | General-purpose input |
| | TIN55 | | | GTM input |
| | P21.4 | O0 | | General-purpose output |
| | TOUT55 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | TXDN | HSCT | | HSCT output (LVDS) |
| **J20** | P21.5 | I | **LVDSH_P/ PU1 / VDDP3** | General-purpose input |
| | TIN56 | | | GTM input |
| | P21.5 | O0 | | General-purpose output |
| | TOUT56 | O1 | | GTM output |
| | ASCLK3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | TXDP | HSCT | | HSCT output (LVDS) |
| **H17** | P21.6 | I | **A2 / PU / VDDP3** | General-purpose input |
| | TIN57 | | | GTM input |
| | ARX3F | | | ASCLIN3 input |
| | $\overline{\text{TGI2}}$ | | | OCDS input |
| | TDI | | | OCDS (JTAG) input |
| | T5EUDA | | | GPT120 input |
| | P21.6 | O0 | | General-purpose output |
| | TOUT57 | O1 | | GTM output |
| | ASLSO3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | SYSCLK | O5 | | HSCT output |
| | – | O6 | | Reserved |
| | T3OUT | O7 | | GPT120 output |
| | $\overline{\text{TGO2}}$ | HWOUT | | OCDS; ENx |

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**Table 2-29 Port 21 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **H16** | P21.7 | I | **A2 / PU / VDDP3** | General-purpose input |
| | TIN58 | | | GTM input |
| | DAP2 | | | OCDS input |
| | $\overline{\text{TGI3}}$ | | | OCDS input |
| | TDO | | | OCDS (JTAG) input<br>The JTAG TDO function is overlayed with P21.7 via a double bond.<br>In JTAG mode this pin is used as TDO, after power-on reset it is HighZ. In DAP mode this pin is used as P21.7 and controlled by the related port control logic |
| | ETHRXERB | | | ETH input |
| | T5INA | | | GPT120 input |
| | P21.7 | O0 | | General-purpose output |
| | TOUT58 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | ASCLK3 | O3 | | ASCLIN3 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | T6OUT | O7 | | GPT120 output |
| | $\overline{\text{TGO3}}$ | HWOUT | | OCDS; ENx |
| | TDO | | | OCDS (JTAG); ENx<br>The JTAG TDO function is overlayed with P21.7 via a double bond.<br>In JTAG mode this pin is used as TDO, after power-on reset it is HighZ. In DAP mode this pin is used as P21.7 and controlled by the related port control logic |

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**Table 2-30 Port 22 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **P20** | P22.0 | I | **LVDSM_N / PU1 / VEXT** | General-purpose input |
| | TIN47 | | | GTM input |
| | MTSR3E | | | QSPI3 input |
| | P22.0 | O0 | | General-purpose output |
| | TOUT47 | O1 | | GTM output |
| | ATX3N | O2 | | ASCLIN3 output (LVDS) |
| | MTSR3 | O3 | | QSPI3 output |
| | SCLK3N | O4 | | QSPI3 output (LVDS) |
| | FCLN1 | O5 | | MSC1 output (LVDS) |
| | FCLND1 | O6 | | MSC1 output (LVDS) |
| | – | O7 | | Reserved |
| **P19** | P22.1 | I | **LVDSM_P / PU1 / VEXT** | General-purpose input |
| | TIN48 | | | GTM input |
| | MRST3E | | | QSPI3 input |
| | P22.1 | O0 | | General-purpose output |
| | TOUT48 | O1 | | GTM output |
| | ATX3P | O2 | | ASCLIN3 output (LVDS) |
| | MRST3 | O3 | | QSPI3 output |
| | SCLK3P | O4 | | QSPI3 output (LVDS) |
| | FCLP1 | O5 | | MSC1 output (LVDS) |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **R20** | P22.2 | I | **LVDSM_N / PU1 / VEXT** | General-purpose input |
| | TIN49 | | | GTM input |
| | $\overline{\text{SLSI3D}}$ | | | QSPI3 input |
| | P22.2 | O0 | | General-purpose output |
| | TOUT49 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO312 | O3 | | QSPI3 output |
| | MTSR3N | O4 | | QSPI3 output (LVDS) |
| | SON1 | O5 | | MSC1 output (LVDS) |
| | SOND1 | O6 | | MSC1 output (LVDS) |
| | – | O7 | | Reserved |

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**Table 2-30 Port 22 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **R19** | P22.3 | I | **LVDSM_P / PU1 / VEXT** | General-purpose input |
| | TIN50 | | | GTM input |
| | SCLK3E | | | QSPI3 input |
| | P22.3 | O0 | | General-purpose output |
| | TOUT50 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK3 | O3 | | QSPI3 output |
| | MTSR3P | O4 | | QSPI3 output (LVDS) |
| | SOP1 | O5 | | MSC1 output (LVDS) |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **P16** | P22.4 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN130 | | | GTM input |
| | P22.4 | O0 | | General-purpose output |
| | TOUT130 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | SLSO012 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **P17** | P22.5 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN131 | | | GTM input |
| | MTSR0C | | | QSPI0 input |
| | P22.5 | O0 | | General-purpose output |
| | TOUT131 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | MTSR0 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-30 Port 22 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **N16** | P22.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN132 | | | GTM input |
| | MRST0C | | | QSPI0 input |
| | P22.6 | O0 | | General-purpose output |
| | TOUT132 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | MRST0 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **N17** | P22.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN133 | | | GTM input |
| | SCLK0C | | | QSPI0 input |
| | P22.7 | O0 | | General-purpose output |
| | TOUT133 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | SCLK0 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **M16** | P22.8 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN134 | | | GTM input |
| | SCLK0B | | | QSPI0 input |
| | P22.8 | O0 | | General-purpose output |
| | TOUT134 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | SCLK0 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-30 Port 22 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **M17** | P22.9 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN135 | | | GTM input |
| | MRST0B | | | QSPI0 input |
| | P22.9 | O0 | | General-purpose output |
| | TOUT135 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | MRST0 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **L16** | P22.10 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN136 | | | GTM input |
| | MTSR0B | | | QSPI0 input |
| | P22.10 | O0 | | General-purpose output |
| | TOUT136 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | MTSR0 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **L17** | P22.11 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN137 | | | GTM input |
| | P22.11 | O0 | | General-purpose output |
| | TOUT137 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | SLSO010 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-31 Port 23 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **V20** | P23.0 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN41 | | | GTM input |
| | P23.0 | O0 | | General-purpose output |
| | TOUT41 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **U19** | P23.1 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN42 | | | GTM input |
| | SDI10 | | | MSC1 input |
| | P23.1 | O0 | | General-purpose output |
| | TOUT42 | O1 | | GTM output |
| | ARTS1 | O2 | | ASCLIN1 output |
| | SLSO313 | O3 | | QSPI3 output |
| | GTMCLK0 | O4 | | GTM output |
| | – | O5 | | Reserved |
| | EXTCLK0 | O6 | | SCU output |
| | – | O7 | | Reserved |
| **U20** | P23.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN43 | | | GTM input |
| | P23.2 | O0 | | General-purpose output |
| | TOUT43 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-31 Port 23 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **T19** | P23.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN44 | | | GTM input |
| | INJ10 | | | MSC1 input |
| | P23.3 | O0 | | General-purpose output |
| | TOUT44 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **T20** | P23.4 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN45 | | | GTM input |
| | P23.4 | O0 | | General-purpose output |
| | TOUT45 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO35 | O3 | | QSPI3 output |
| | END12 | O4 | | MSC1 output |
| | EN10 | O5 | | MSC1 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **T17** | P23.5 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN46 | | | GTM input |
| | P23.5 | O0 | | General-purpose output |
| | TOUT46 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO34 | O3 | | QSPI3 output |
| | END13 | O4 | | MSC1 output |
| | EN11 | O5 | | MSC1 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-31 Port 23 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **R17** | P23.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN138 | | | GTM input |
| | P23.6 | O0 | | General-purpose output |
| | TOUT138 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | SLSO011 | O4 | | QSPI0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **R16** | P23.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN139 | | | GTM input |
| | P23.7 | O0 | | General-purpose output |
| | TOUT139 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

**Table 2-32 Port 32 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **Y17** | P32.0 | I | **LP / EVR13 SMPS -> PD, GPIO - > PU / VEXT** | General-purpose input |
| | TIN36 | | | GTM input |
| | FDEST | | | PMU input |
| | VGATE1N | | | SMPS mode: analog output. External Pass Device gate control for EVR13 |
| | P32.0 | O0 | | General-purpose output |
| | TOUT36 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |

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**Table 2-32 Port 32 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **Y18** | P32.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN38 | | | GTM input |
| | ARX3D | | | ASCLIN3 input |
| | RXDCAN3B | | | CAN node 3 input |
| | P32.2 | O0 | | General-purpose output |
| | TOUT38 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | DCDCSYNC | O6 | | SCU output |
| | – | O7 | | Reserved |
| **Y19** | P32.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN39 | | | GTM input |
| | P32.3 | O0 | | General-purpose output |
| | TOUT39 | O1 | | GTM output |
| | ATX3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | ASCLK3 | O4 | | ASCLIN3 output |
| | TXDCAN3 | O5 | | CAN node 3 output |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| **W18** | P32.4 | I | **MP+ / PU1 / VEXT** | General-purpose input |
| | TIN40 | | | GTM input |
| | ACTS1B | | | ASCLIN1 input |
| | SDI12 | | | MSC1 input |
| | P32.4 | O0 | | General-purpose output |
| | TOUT40 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | END12 | O3 | | MSC1 output |
| | GTMCLK1 | O4 | | GTM output |
| | EN10 | O5 | | MSC1 output |
| | EXTCLK1 | O6 | | SCU output |
| | COUT63 | O7 | | CCU60 output |

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**Table 2-32 Port 32 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **T15** | P32.5 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN140 | | | GTM input |
| | P32.5 | O0 | | General-purpose output |
| | TOUT140 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | TXDCAN2 | O6 | | CAN node 2 output |
| | – | O7 | | Reserved |
| **U15** | P32.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | $\overline{\text{TGI4}}$ | | | OCDS input |
| | TIN141 | | | GTM input |
| | RXDCAN2C | | | CAN node 2 input |
| | ARX2F | | | ASCLIN2 input |
| | P32.6 | O0 | | General-purpose output |
| | TOUT141 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | SLSO212 | O4 | | QSPI2 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | $\overline{\text{TGO4}}$ | HWOUT | | OCDS; ENx |
| **U16** | P32.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN142 | | | GTM input |
| | $\overline{\text{TGI5}}$ | | | OCDS input |
| | P32.7 | O0 | | General-purpose output |
| | TOUT142 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | – | O7 | | Reserved |
| | $\overline{\text{TGO5}}$ | HWOUT | | OCDS; ENx |

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**Table 2-33 Port 33 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **W10** | P33.0 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN22 | | | GTM input |
| | DSITR0E | | | DSADC channel 0 input E |
| | P33.0 | O0 | | General-purpose output |
| | TOUT22 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | VADCG2BFL0 | O6 | | VADC output |
| | – | O7 | | Reserved |
| **Y10** | P33.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN23 | | | GTM input |
| | PSIRX0C | | | PSI5 input |
| | SENT9C | | | SENT input |
| | DSCIN2B | | | DSADC channel 2 input B |
| | DSITR1E | | | DSADC channel 1 input E |
| | P33.1 | O0 | | General-purpose output |
| | TOUT23 | O1 | | GTM output |
| | ASLSO3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | DSCOUT2 | O4 | | DSADC channel 2 output |
| | VADCEMUX02 | O5 | | VADC output |
| | VADCG2BFL1 | O6 | | VADC output |
| | – | O7 | | Reserved |
| **W11** | P33.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN24 | | | GTM input |
| | SENT8C | | | SENT input |
| | DSDIN2B | | | DSADC channel 2 input B |
| | DSITR2E | | | DSADC channel 2 input E |
| | P33.2 | O0 | | General-purpose output |
| | TOUT24 | O1 | | GTM output |
| | ASCLK3 | O2 | | ASCLIN3 output |
| | – | O3 | | Reserved |
| | PSITX0 | O4 | | PSI5 output |
| | VADCEMUX01 | O5 | | VADC output |
| | VADCG2BFL2 | O6 | | VADC output |
| | – | O7 | | Reserved |

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**Table 2-33 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **Y11** | P33.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN25 | | | GTM input |
| | PSIRX1C | | | PSI5 input |
| | SENT7C | | | SENT input |
| | DSCIN1B | | | DSADC channel 1 input B |
| | P33.3 | O0 | | General-purpose output |
| | TOUT25 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | DSCOUT1 | O4 | | DSADC channel 1 output |
| | VADCEMUX00 | O5 | | VADC output |
| | VADCG2BFL3 | O6 | | VADC output |
| | – | O7 | | Reserved |
| **W12** | P33.4 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN26 | | | GTM input |
| | SENT6C | | | SENT input |
| | $\overline{\text{CTRAPC}}$ | | | CCU61 input |
| | DSDIN1B | | | DSADC channel 1 input B |
| | DSITR0F | | | DSADC channel 0 input F |
| | P33.4 | O0 | | General-purpose output |
| | TOUT26 | O1 | | GTM output |
| | ARTS2 | O2 | | ASCLIN2 output |
| | – | O3 | | Reserved |
| | PSITX1 | O4 | | PSI5 output |
| | VADCEMUX12 | O5 | | VADC output |
| | VADCG0BFL0 | O6 | | VADC output |
| | – | O7 | | Reserved |

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**Table 2-33 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **Y12** | P33.5 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN27 | | | GTM input |
| | ACTS2B | | | ASCLIN2 input |
| | PSIRX2C | | | PSI5 input |
| | PSISRXC | | | PSI5-S input |
| | SENT5C | | | SENT input |
| | CCPOS2C | | | CCU61 input |
| | T4EUDB | | | GPT120 input |
| | DSCIN0B | | | DSADC channel 0 input B |
| | DSITR1F | | | DSADC channel 1 input F |
| | P33.5 | O0 | | General-purpose output |
| | TOUT27 | O1 | | GTM output |
| | SLSO07 | O2 | | QSPI0 output |
| | SLSO17 | O3 | | QSPI1 output |
| | DSCOUT0 | O4 | | DSADC channel 0 output |
| | VADCEMUX11 | O5 | | VADC output |
| | VADCG0BFL1 | O6 | | VADC output |
| | – | O7 | | Reserved |
| **W13** | P33.6 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN28 | | | GTM input |
| | SENT4C | | | SENT input |
| | CCPOS1C | | | CCU61 input |
| | T2EUDB | | | GPT120 input |
| | DSDIN0B | | | DSADC channel 0 input B |
| | DSITR2F | | | DSADC channel 2 input F |
| | P33.6 | O0 | | General-purpose output |
| | TOUT28 | O1 | | GTM output |
| | ASLSO2 | O2 | | ASCLIN2 output |
| | - | O3 | | Reserved |
| | PSITX2 | O4 | | PSI5 output |
| | VADCEMUX10 | O5 | | VADC output |
| | VADCG1BFL0 | O6 | | VADC output |
| | PSISTX | O7 | | PSI5-S output |

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**Table 2-33 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **Y13** | P33.7 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN29 | | | GTM input |
| | RXDCAN0E | | | CAN node 0 input |
| | REQ8 | | | SCU input |
| | CCPOS0C | | | CCU61 input |
| | T2INB | | | GPT120 input |
| | P33.7 | O0 | | General-purpose output |
| | TOUT29 | O1 | | GTM output |
| | ASCLK2 | O2 | | ASCLIN2 output |
| | SLSO37 | O3 | | QSPI3 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | VADCG1BFL1 | O6 | | VADC output |
| | – | O7 | | Reserved |
| **W14** | P33.8 | I | **MP / HighZ/ VEXT** | General-purpose input |
| | TIN30 | | | GTM input |
| | ARX2E | | | ASCLIN2 input |
| | EMGSTOPA | | | SCU input |
| | P33.8 | O0 | | General-purpose output |
| | TOUT30 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO32 | O3 | | QSPI3 output |
| | – | O4 | | Reserved |
| | TXDCAN0 | O5 | | CAN node 0 output |
| | – | O6 | | Reserved |
| | COUT62 | O7 | | CCU61 output |
| | SMUFSP | HWOUT | | SMU |
| **Y14** | P33.9 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN31 | | | GTM input |
| | P33.9 | O0 | | General-purpose output |
| | TOUT31 | O1 | | GTM output |
| | ATX2 | O2 | | ASCLIN2 output |
| | SLSO31 | O3 | | QSPI3 output |
| | ASCLK2 | O4 | | ASCLIN2 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | CC62 | O7 | | CCU61 output |

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**Table 2-33 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **W15** | P33.10 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN32 | | | GTM input |
| | $\overline{\text{SLSI3C}}$ | | | QSPI3 input |
| | P33.10 | O0 | | General-purpose output |
| | TOUT32 | O1 | | GTM output |
| | SLSO16 | O2 | | QSPI1 output |
| | SLSO311 | O3 | | QSPI3 output |
| | ASLSO1 | O4 | | ASCLIN1 output |
| | PSISCLK | O5 | | PSI5-S output |
| | – | O6 | | Reserved |
| | COUT61 | O7 | | CCU61 output |
| **Y15** | P33.11 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN33 | | | GTM input |
| | SCLK3D | | | QSPI3 input |
| | P33.11 | O0 | | General-purpose output |
| | TOUT33 | O1 | | GTM output |
| | ASCLK1 | O2 | | ASCLIN1 output |
| | SCLK3 | O3 | | QSPI3 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | DSCGPWMN | O6 | | DSADC output |
| | CC61 | O7 | | CCU61 output |
| **W16** | P33.12 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN34 | | | GTM input |
| | MTSR3D | | | QSPI3 input |
| | P33.12 | O0 | | General-purpose output |
| | TOUT34 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | MTSR3 | O3 | | QSPI3 output |
| | ASCLK1 | O4 | | ASCLIN1 output |
| | – | O5 | | Reserved |
| | DSCGPWMP | O6 | | DSADC output |
| | COUT60 | O7 | | CCU61 output |

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**Table 2-33 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **Y16** | P33.13 | I | **MP / PU1 / VEXT** | General-purpose input |
| | TIN35 | | | GTM input |
| | ARX1F | | | ASCLIN1 input |
| | MRST3D | | | QSPI3 input |
| | DSSGNB | | | DSADC input |
| | INJ11 | | | MSC1 input |
| | P33.13 | O0 | | General-purpose output |
| | TOUT35 | O1 | | GTM output |
| | ATX1 | O2 | | ASCLIN1 output |
| | MRST3 | O3 | | QSPI3 output |
| | SLSO26 | O4 | | QSPI2 output |
| | – | O5 | | Reserved |
| | DCDCSYNC | O6 | | SCU output |
| | CC60 | O7 | | CCU61 output |
| **T14** | P33.14 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN143 | | | GTM input |
| | $\overline{\text{TGI6}}$ | | | OCDS input |
| | SCLK2D | | | QSPI2 input |
| | P33.14 | O0 | | General-purpose output |
| | TOUT143 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SCLK2 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | CC62 | O7 | | CCU60 output |
| | $\overline{\text{TGO6}}$ | HWOUT | | OCDS; ENx |

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**Table 2-33 Port 33 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **U14** | P33.15 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN144 | | | GTM input |
| | $\overline{\text{TGI7}}$ | | | OCDS input |
| | P33.15 | O0 | | General-purpose output |
| | TOUT144 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | SLSO211 | O3 | | QSPI2 output |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT62 | O7 | | CCU60 output |
| | $\overline{\text{TGO7}}$ | HWOUT | | OCDS; ENx |

**Table 2-34 Port 34 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **U11** | P34.1 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN146 | | | GTM input |
| | P34.1 | O0 | | General-purpose output |
| | TOUT146 | O1 | | GTM output |
| | ATX0 | O2 | | ASCLIN0 output |
| | – | O3 | | Reserved |
| | TXDCAN0 | O4 | | CAN node 0 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT63 | O7 | | CCU60 output |
| **T12** | P34.2 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN147 | | | GTM input |
| | ARX0D | | | ASCLIN0 input |
| | RXDCAN0G | | | CAN node 0 input |
| | P34.2 | O0 | | General-purpose output |
| | TOUT147 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | – | O4 | | Reserved |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | CC60 | O7 | | CCU60 output |

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**Table 2-34 Port 34 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **U12** | P34.3 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN148 | | | GTM input |
| | P34.3 | O0 | | General-purpose output |
| | TOUT148 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | SLSO210 | O4 | | QSPI2 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT60 | O7 | | CCU60 output |
| **T13** | P34.4 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN149 | | | GTM input |
| | MRST2D | | | QSPI2 input |
| | P34.4 | O0 | | General-purpose output |
| | TOUT149 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | MRST2 | O4 | | QSPI2 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | CC61 | O7 | | CCU60 output |
| **U13** | P34.5 | I | **LP / PU1 / VEXT** | General-purpose input |
| | TIN150 | | | GTM input |
| | MTSR2D | | | QSPI2 input |
| | P34.5 | O0 | | General-purpose output |
| | TOUT150 | O1 | | GTM output |
| | – | O2 | | Reserved |
| | – | O3 | | Reserved |
| | MTSR2 | O4 | | QSPI2 output |
| | – | O5 | | Reserved |
| | – | O6 | | Reserved |
| | COUT61 | O7 | | CCU60 output |

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**Table 2-35 Port 40 Functions**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **W2** | P40.0 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG3.0 | | | VADC analog input channel 0 of group 3 |
| | DS2PB | | | DSADC: positive analog input channe of DSADC 2, pin B |
| | CCPOS0D | | | CCU60 input |
| | SENT0A | | | SENT input |
| **W1** | P40.1 | I | **S / HighZ / VDDM** | General-purpose inpu.t |
| | VADCG3.1 | | | VADC analog input channel 1 of group 3 (MD) |
| | DS2NB | | | DSADC: negative analog of input channel 2, pin B |
| | CCPOS1B | | | CCU60 input |
| | SENT1A | | | SENT input |
| **V2** | P40.2 | I | **S / HighZ / VDDM** | General-purpose inpu.t |
| | VADCG3.2 | | | VADC analog input channel 2 of group 3 (MD) |
| | CCPOS1D | | | CCU60 input |
| | SENT2A | | | SENT input |
| **V1** | P40.3 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG3.3 | | | VADC analog input channel 3 of group 3 (with pull down diagnostics) |
| | CCPOS2B | | | CCU60 input |
| | SENT3A | | | SENT input |
| **P4** | P40.4 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.0 | | | VADC analog input channel 0 of group 4 |
| | CCPOS2D | | | CCU60 input |
| | SENT4A | | | SENT input |
| **R1** | P40.5 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.1 | | | VADC analog input channel 1 of group 4 (MD) |
| | CCPOS0D | | | CCU61 input |
| | SENT5A | | | SENT input |
| **N4** | P40.6 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.4 | | | VADC analog input channel 4 of group 4 |
| | DS3PA | | | DSADC: positive analog input of channel 3, pin A |
| | CCPOS1B | | | CCU61 input |
| | SENT6A | | | SENT input |
| **P2** | P40.7 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.5 | | | VADC analog input channel 5 of group 4 |
| | DS3NA | | | DSADC: negative analog input of channel 3, pin A |
| | CCPOS1D | | | CCU61 input |
| | SENT7A | | | SENT input |

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**Table 2-35 Port 40 Functions** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **N5** | P40.8 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.6 | | | VADC analog input channel 6 of group 4 |
| | DS3PB | | | DSADC: positive analog input of channel 3, pin B |
| | CCPOS2B | | | CCU61 input |
| | SENT8A | | | SENT input |
| **P1** | P40.9 | I | **S / HighZ / VDDM** | General-purpose input |
| | VADCG4.7 | | | VADC analog input channel 7 of group 4 |
| | DS3NB | | | DSADC: negative analog input of channel 3, pin B |
| | CCPOS2D | | | CCU61 input |
| | SENT9A | | | SENT input |

**Table 2-36 Analog Inputs**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **T10** | AN0 | I | **D / HighZ / VDDM** | Analog input 0 |
| | VADCG0.0 | | | VADC analog input channel 0 of group 0 |
| | DS1PA | | | DSADC: positive analog of input channel 1, pin A |
| **U10** | AN1 | I | **D / HighZ / VDDM** | Analog input 1 |
| | VADCG0.1 | | | VADC analog input channel 1 of group 0 (MD) |
| | DS1NA | | | DSADC: negative analog input of channel 1, pin A |
| **W9** | AN2 | I | **D / HighZ / VDDM** | Analog input 2 |
| | VADCG0.2 | | | VADC analog input channel 2 of group 0 (MD) |
| | DS0PA | | | DSADC: positive analog input of channel 0, pin A |
| **U9** | AN3 | I | **D / HighZ / VDDM** | Analog input 3 |
| | VADCG0.3 | | | VADC analog input channel 3 of group 0 |
| | DS0NA | | | DSADC: negative analog input of channel 0, pin A |
| **T9** | AN4 | I | **D / HighZ / VDDM** | Analog input 4 |
| | VADCG0.4 | | | VADC analog input channel 4 of group 0 |
| **Y9** | AN5 | I | **D / HighZ / VDDM** | Analog input 5 |
| | VADCG0.5 | | | VADC analog input channel 5 of group 0 |
| **T8** | AN6 | I | **D / HighZ / VDDM** | Analog input 6 |
| | VADCG0.6 | | | VADC analog input channel 6 of group 0 |
| **U8** | AN7 | I | **D / HighZ / VDDM** | Analog input 7 |
| | VADCG0.7 | | | VADC analog input channel 7 of group 0 (with pull down diagnostics) |
| **W8** | AN8 | I | **D / HighZ / VDDM** | Analog input 8 |
| | VADCG1.0 | | | VADC analog input channel 0 of group 1 |

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**Table 2-36 Analog Inputs** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **U7** | AN9 | I | **D / HighZ / VDDM** | Analog input 9 |
| | VADCG1.1 | | | VADC analog input channel 1 of group 1 (MD) |
| **Y8** | AN10 | I | **D / HighZ / VDDM** | Analog input 10 |
| | VADCG1.2 | | | VADC analog input channel 2 of group 1 (MD) |
| **W7** | AN11 | I | **D / HighZ / VDDM** | Analog input 11 |
| | VADCG1.3 | | | VADC analog input channel 3 of group 1 (with pull down diagnostics) |
| **T7** | AN12 | I | **D / HighZ / VDDM** | Analog input 12 |
| | VADCG1.4 | | | VADC analog input channel 4 of group 1 |
| **W6** | AN13 | I | **D / HighZ / VDDM** | Analog input 13 |
| | VADCG1.5 | | | VADC analog input channel 5 of group 1 |
| **U6** | AN14 | I | **D / HighZ / VDDM** | Analog input 14 |
| | VADCG1.6 | | | VADC analog input channel 6 of group 1 |
| **T6** | AN15 | I | **D / HighZ / VDDM** | Analog input 15 |
| | VADCG1.7 | | | VADC analog input channel 7 of group 1 |
| **W5** | AN16 | I | **D / HighZ / VDDM** | Analog input 16 |
| | VADCG2.0 | | | VADC analog input channel 0 of group 2 |
| **U5** | AN17 | I | **D / HighZ / VDDM** | Analog input 17 |
| | VADCG2.1 | | | VADC analog input channel 1 of group 2 (MD) |
| **W4** | AN18 | I | **D / HighZ / VDDM** | Analog input 18 |
| | VADCG2.2 | | | VADC analog input channel 2 of group 2 (MD) |
| **W3** | AN19 | I | **D / HighZ / VDDM** | Analog input 19 |
| | VADCG2.3 | | | VADC analog input channel 3 of group 2 (with pull down diagnostics) |
| **Y3** | AN20 | I | **D / HighZ / VDDM** | Analog input 20 |
| | VADCG2.4 | I | | VADC analog input channel 4 of group 2 |
| | DS2PA | I | | DSADC: positive analog input of channel 2, pin A |
| **Y2** | AN21 | I | **D / HighZ / VDDM** | Analog input 21 |
| | VADCG2.5 | I | | VADC analog input channel 5 of group 2 |
| | DS2NA | I | | DSADC: negative analog input of channel of DSADC 2, pin A |
| **T5** | AN22 | I | **D / HighZ / VDDM** | Analog input 22 |
| | VADCG2.6 | | | VADC analog input channel 6 of group 2 |

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**Table 2-36 Analog Inputs** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **R5** | AN23 | I | **D / HighZ / VDDM** | Analog input 23 |
| | VADCG2.7 | | | VADC analog input channel 7 of group 2 |
| **W2** | AN24 | I | **S / HighZ / VDDM** | Analog input 24 |
| | VADCG3.0 | | | VADC analog input channel 0 of group 3 |
| | DS2PB | | | DSADC: positive analog input of channel 2, pin B |
| | SENT0A | | | SENT input channel 0, pin A |
| **W1** | AN25 | I | **S / HighZ / VDDM** | Analog input 24 |
| | VADCG3.1 | | | VADC analog input channel 1 of group 3 (MD) |
| | DS2NB | | | DSADC: negative analog input of channel 2, pin B |
| | SENT1A | | | SENT input channel 1, pin A |
| **V2** | AN26 | I | **S / HighZ / VDDM** | Analog input 26 |
| | VADCG3.2 | | | VADC analog input channel 2 of group 3 (MD) |
| | SENT2A | | | SENT input channel 2, pin A |
| **V1** | AN27 | I | **S / HighZ / VDDM** | Analog input 27 |
| | VADCG3.3 | | | VADC analog input channel 3 of group 3 (with pull down diagnostics) |
| | SENT3A | | | SENT input channel 3, pin A |
| **U2** | AN28 | I | **D / HighZ / VDDM** | Analog input 28 |
| | VADCG3.4 | | | VADC analog input channel 4 of group 3 |
| **U1** | AN29 | I | **D / HighZ / VDDM** | Analog input 29 |
| | VADCG3.5 | | | VADC analog input channel 5 of group 3 |
| **T4** | AN30 | I | **D / HighZ / VDDM** | Analog input 30 |
| | VADCG3.6 | | | VADC analog input channel 6 of group 3 |
| **R4** | AN31 | I | **D / HighZ / VDDM** | Analog input 31 |
| | VADCG3.7 | | | VADC analog input channel 7 of group 3 |
| **P4** | AN32 | I | **S / HighZ / VDDM** | Analog input 32 |
| | VADCG4.0 | | | VADC analog input channel 0 of group 4 |
| | SENT4A | | | SENT input channel 4, pin A |
| **R1** | AN33 | I | **S / HighZ / VDDM** | Analog input 33 |
| | VADCG4.1 | | | VADC analog input channel 1 of group 4 (MD) |
| | SENT5A | | | SENT input channel 5, pin A |
| **P5** | AN34 | I | **D / HighZ / VDDM** | Analog input 34 |
| | VADCG4.2 | | | VADC analog input channel 2 of group 4 (MD) |

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**Table 2-36 Analog Inputs** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **R2** | AN35 | I | **D / HighZ / VDDM** | Analog input 35 |
| | VADCG4.3 | | | VADC analog input channel 3 of group 4 (with pull down diagnostics) |
| **N4** | AN36 | I | **S / HighZ / VDDM** | Analog input 34 |
| | VADCG4.4 | | | VADC analog input channel 4 of group 4 |
| | DS3PA | | | DSADC: positive analog input of channel of DSADC 3, pin A |
| | SENT6A | | | SENT input channel 6, pin A |
| **P2** | AN37 | I | **S / HighZ / VDDM** | Analog input 37 |
| | VADCG4.5 | | | VADC analog input channel 5 of group 4 |
| | DS3NA | | | DSADC: negative analog input of channel of DSADC 3, pin A |
| | SENT7A | | | SENT input channel 7, pin A |
| **N5** | AN38 | I | **S / HighZ / VDDM** | Analog input 38 |
| | VADCG4.6 | | | VADC analog input channel 6 of group 4 |
| | DS3PB | | | DSADC: positive analog input of channel of DSADC 3, pin B |
| | SENT8A | | | SENT input channel 8, pin A |
| **P1** | AN39 | I | **S / HighZ / VDDM** | Analog input 39 |
| | VADCG4.7 | | | VADC analog input channel 7 of group 4 |
| | DS3NB | | | DSADC: negative analog input of channel of DSADC 3, pin B |
| | SENT9A | | | SENT input channel 9, pin A |
| **M5** | AN40 | I | **D / HighZ / VDDM** | Analog input 40 |
| | VADCG5.0 | | | VADC analog input channel 0 of group 5 |
| **M4** | AN41 | I | **D / HighZ / VDDM** | Analog input 41 |
| | VADCG5.1 | | | VADC analog input channel 1 of group 5 (MD) |
| **L5** | AN42 | I | **D / HighZ / VDDM** | Analog input 42 |
| | VADCG5.2 | | | VADC analog input channel 2 of group 5 (MD) |
| **L4** | AN43 | I | **D / HighZ / VDDM** | Analog input 43 |
| | VADCG5.3 | | | VADC analog input channel 3 of group 5 (with pull down diagnostics) |
| **N1** | AN44 | I | **D / HighZ / VDDM** | Analog input 44 |
| | VADCG5.4 | | | VADC analog input channel 4 of group 5 |
| | DS3PC | | | DSADC: positive analog input of channel of DSADC 3, pin C |

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**Table 2-36 Analog Inputs** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **N2** | AN45 | I | **D / HighZ / VDDM** | Analog input 45 |
| | VADCG5.5 | | | VADC analog input channel 5 of group 5 |
| | DS3NC | | | DSADC: negative analog input of channel of DSADC 3, pin C |
| **M1** | AN46 | I | **D / HighZ / VDDM** | Analog input 46 |
| | VADCG5.6 | | | VADC analog input channel 6 of group 5 |
| | DS3PD | | | DSADC: positive analog input of channel of DSADC 3, pin D |
| **M2** | AN47 | I | **D / HighZ / VDDM** | Analog input 47 |
| | VADCG5.7 | | | VADC analog input channel 7 of group 5 |
| | DS3ND | | | DSADC: negative analog input of channel of DSADC 3, pin D |

**Table 2-37 System I/O**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **G17** | $\overline{\text{PORST}}$ | I | **I / PD / VEXT** | Power On Reset Input<br>Additional strong PD in case of power fail. |
| **F16** | $\overline{\text{ESR0}}$ | I/O | **MP / OD / VEXT** | External System Request Reset 0<br>Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of $\overline{\text{PORST}}$ until the internal reset phase has finished. See also SCU chapter for details.<br>Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. |
| | EVRWUP | I | | EVR Wakeup Pin |
| **G16** | $\overline{\text{ESR1}}$ | I/O | **MP / PU1 / VEXT** | External System Request Reset 1<br>Default NMI function.<br>See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. |
| | EVRWUP | I | | EVR Wakeup Pin |
| **W17** | VGATE1P | O | **VGATE1P / - / VEXT** | External Pass Device gate control for EVR13 |
| **K16** | TMS | I | **A2 / PD / VDDP3** | JTAG Module State Machine Control Input |
| | DAP1 | I/O | | Device Access Port Line 1 |
| **L19** | $\overline{\text{TRST}}$ | I | **A2 / PD / VDDP3** | JTAG Module Reset/Enable Input |

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**Table 2-37 System I/O** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **J16** | TCK | I | **A2 / PD / VDDP3** | JTAG Module Clock Input |
| | DAP0 | I | | Device Access Port Line 0 |
| **M20** | XTAL1 | I | **XTAL1 / - / VDDP3** | Main Oscillator/PLL/Clock Generator Input |
| **M19** | XTAL2 | O | **XTAL2 / - / VDDP3** | Main Oscillator/PLL/Clock Generator Output |

**Table 2-38 Supply**

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **Y6** | VAREF1 | I | **Vx** | Positive Analog Reference Voltage 1 |
| **Y7** | VAGND1 | I | **Vx** | Negative Analog Reference Voltage 1 |
| **T1** | VAREF2 | I | **Vx** | Positive Analog Reference Voltage 2 |
| **T2** | VAGND2 | I | **Vx** | Negative Analog Reference Voltage 2 |
| **Y5** | VDDM | I | **Vx** | ADC Analog Power Supply (3.3V / 5V) |
| **G8, H7** | VDD / VDDSB | I | **Vx** | Emulation Device: Emulation SRAM Standby Power Supply (1.3V) (Emulation Device only).<br>Production Device: VDD (1.3V). |
| **P8, P13, N7, N14, H14, G13** | VDD | I | **Vx** | Digital Core Power Supply (1.3V) |
| **N19** | VDD | I | **Vx** | Digital Core Power Supply (1.3V).<br>The supply pin inturn supplies the main XTAL Oscillator/PLL (1.3V) . A higher decoupling capacitor is therefore recommended to the VSS pin for better noise immunity. |
| **A2, B3, V19, W20** | VEXT | I | **Vx** | External Power Supply (5V / 3.3V) |
| **B18, A19** | VDDP3 | I | **Vx** | Digital Power Supply for Flash (3.3V).<br>Can be also used as external 3.3V Power Supply for VFLEX. |
| **N20** | VDDP3 | I | **Vx** | Digital Power Supply for Oscillator, LVDSH and A2 pads (3.3V).<br>The supply pin inturn supplies the main XTAL Oscillator/PLL (3.3V) . A higher decoupling capacitor is therefore recommended to the VSS pin for better noise immunity. |

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**Table 2-38 Supply** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **E15, D16** | VDDFL3 | I | **Vx** | Flash Power Supply (3.3V) |
| **D5** | VFLEX | I | **Vx** | Digital Power Supply for Flex Port Pads (5V / 3.3V) |
| **Y4** | VSSM | I | **Vx** | Analog Ground for VDDM |
| **T11** | VEVRSB | I | **Vx** | Standby Power Supply (3.3V/5V) for the Standby SRAM (CPU0.DSPR).<br>If Standby mode is not used: To be handled like VEXT (3.3V/5V). |
| **B2, D4, E5, L20, T16, U17, W19, Y20** | VSS | I | **Vx** | Digital Ground |
| **E16, D17, B19, A20** | VSS | I | **Vx** | Digital Ground (outer balls) |
| **P9, P12, N9, N10, N11, N12** | VSS | I | **Vx** | Digital Ground (center balls) |
| **M7, M8, M10, M11, M13, M14** | VSS | I | **Vx** | Digital Ground (center balls) |
| **L8, L9, L10, L11, L12, L13** | VSS | I | **Vx** | Digital Ground (center balls) |
| **K8, K9, K10, K11, K12, K13** | VSS | I | **Vx** | Digital Ground (center balls) |
| **J7, J8, J10, J11, J13, J14** | VSS | I | **Vx** | Digital Ground (center balls) |
| **H9, H10, H11, H12, G9, G10, G11, G12** | VSS | I | **Vx** | Digital Ground (center balls) |
| **P10** | VSS | I | **Vx** | Digital Ground (center balls)<br>This ball is used in the Emulation Device as AGBT TX0N |
| **P11** | VSS | I | **Vx** | Digital Ground (center balls)<br>This ball is used in the Emulation Device as AGBT TX0P |
| **L7** | VSS | I | **Vx** | Digital Ground (center balls)<br>This ball is used in the Emulation Device as AGBT CLKN |

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**Table 2-38 Supply** (cont'd)

| Pin | Symbol | Ctrl | Type | Function |
|---|---|---|---|---|
| **K7** | VSS | I | **Vx** | Digital Ground (center balls)<br>This ball is used in the Emulation Device as AGBT CLKP |
| **L14** | VSS | I | **Vx** | Digital Ground (center balls)<br>This ball is used in the Emulation Device as AGBT ERR |
| **K14** | NC / VDDPSB | I | **NCVDDPSB** | Emulation Device: Power Supply (3.3V) for DAP/JTAG pad group. Can be connected to VDDP or can be left unsupplied (see document ´AurixED´ / Aurix Emulation Devices specification).<br><br>Production Device:<br>This pin is not connected on package level. It can be connected on PCB level to VDDP or Ground or can be left unsupplied. |
| **A1, Y1, U4** | NC | I | **NC** | Not Connected.<br>These pins are not connected on package level and will not be used for future extensions. |

**Legend:**

Column "**Ctrl.**":

I = Input (for GPIO port Lines with IOCR bit field Selection PCx = $0XXX_B$)

O = Output
O0 = Output with IOCR bit field selection PCx = $1X000_B$
O1 = Output with IOCR bit field selection PCx = $1X001_B$ (ALT1)
O2 = Output with IOCR bit field selection PCx = $1X010_B$ (ALT2)
O3 = Output with IOCR bit field selection PCx = $1X011_B$ (ALT3)
O4 = Output with IOCR bit field selection PCx = $1X100_B$ (ALT4)
O5 = Output with IOCR bit field selection PCx = $1X101_B$ (ALT5)
O6 = Output with IOCR bit field selection PCx = $1X110_B$ (ALT6)
O7 = Output with IOCR bit field selection PCx = $1X111_B$ (ALT7)

Column "**Type**":

LP = Pad class LP (5V/3.3V, LVTTL)
MP = Pad class MP (5V/3.3V, LVTTL)
MP+ = Pad class MP+ (5V/3.3V, LVTTL)
MPR = Pad class MPR (5V/3.3V, LVTTL)
A2 = Pad class A2 (3.3V, LVTTL)
LVDSM = Pad class LVDSM (LVDS/CMOS 5V/3.3V)
LVDSH = Pad class LVDSH (LVDS/CMOS 3.3V)
S = Pad class S (ADC overlayed with General Purpose Input)
D = Pad class D (ADC)
PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PU1 = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]

1)The default state of GPIOs (Px.y) during and after $\overline{\text{PORST}}$ active is controllled via HWCFG[6] (P14.4). HWCFG[6] has a weak internal pull-up active at start-up if the pin is left unconnected.See also User´s Manual, "Introduction Chapter", "General Purpose I/O Ports and Peripheral I/O Lines", Figure: "Default state of port pins during and after reset".

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PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
PD1 = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PX = Behavior depends on usage: PD in EVR13 SMPS Mode and PU1 in GPIO Mode
OD = open drain during reset ($\overline{\text{PORST}}$ = 0)
HighZ = tri-state during reset ($\overline{\text{PORST}}$ = 0)
$\overline{\text{PORST}}$ = $\overline{\text{PORST}}$ input pad
XTAL1 = XTAL1 input pad
XTAL2 = XTAL2 input pad
VGATE1P = VGATE1P
VGATE3P = VGATE3P
Vx = Supply
NC = These pins are reserved for future extensions and shall not be connected externally
NC1 = These pins are not connected on package level and will not be used for future extensions
NCVDDPSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.
NCVDDSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.

### 2.2.2 Emergency Stop Function

The Emergency Stop function can be used to force GPIOs (General Purpose Inputs/Outputs) via an external input signal (EMGSTOPA or EMGSTOPB) into a defined state:

- Input state and
- PU or High-Z depending on HWCFG[6] level latched during $\overline{\text{PORST}}$ active

Control of the Emergency Stop function:

- The Emergency Stop function can be enabled/disabled in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- The Emergency Stop input signal, EMGSTOPA (P33.8) / EMGSTOPB (P21.2) , can selected in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- On port level, each GPIO can be enabled/disabled for the Emergency Stop function via the Px_ESR (Port x Emergency Stop) registers in the port control logic (see chapter “General Purpose I/O Ports and Peripheral I/O Lines”, “Emergency Stop Register”).

The Emergency Stop function is available for all GPIO Ports with the following exceptions:

- Not available for P20.2 (General Purpose Input/GPI only, overlayed with Testmode)
- Not available for P40.x (analoge input ANx overlayed with GPI)
- Not available for P32.0 EVR13 SMPS mode.
- Not available for dedicated I/O without General Purpose Output function (e.g ESRx, TMS, TCK)

The Emergency Stop function can be overruled on the following GPIO Ports:

- P00.x: Emergency Stop can be overruled by the VADC. Overruling can be disabled via the control register P00_SCR (see chapter “General Purpose I/O Ports and Peripheral I/O Lines”, P00)
- P14.0 and P14.1: Emergency Stop can be overruled in the DXCPL mode (DAP over can physical layer mode). No Overruling in the DXCM (Debug over can message) mode
- P21.6: Emergency Stop can be overruled in JTAG mode if this pin is used as TDI
- P21.7: Emergency Stop can be overruled in JTAG or Three Pin DAP mode

2) If HWCFG[6] is left unconnected or is externally pulled high, weak internal pull-ups (PU1) / pull-downs (PD1) are active during and after reset.

3) If HWCFG[6] is connected to ground, the PD1 / PU1 pins are predominantly in HighZ during and after reset.

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- P20.0: Emergency Stop can be overruled in JTAG mode if this GPIO is used as TDI

### 2.2.3 Pull-Up/Pull-Down Reset Behavior of the Pins

**Table 2-39 List of Pull-Up/Pull-Down Reset Behavior of the Pins**

| Pins | $\overline{\text{PORST}}$ = 0 | $\overline{\text{PORST}}$ = 1 |
|---|---|---|
| $\overline{\text{all GPIOs}}$ | Pull-up if HWCFG[6] = 1 or High-Z if HWCFG[6] = 0 | |
| $\overline{\text{TDI}}$, $\overline{\text{TESTMODE}}$ | Pull-up | |
| $\overline{\text{PORST}}$[1)] | Pull-down with $I_{PORST}$ relevant | Pull-down with $I_{PDLI}$ relevant |
| $\overline{\text{TRST}}$, TCK, TMS | Pull-down | |
| $\overline{\text{ESR0}}$ | The open-drain driver is used to drive low.[2)] | Pull-up[3)] |
| $\overline{\text{ESR1}}$ | Pull-up[3)] | |
| TDO | Pull-up | High-Z/Pull-up[4)] |

1) Pull-down with $I_{PORST}$ relevant is always activated when a primary supply monitor detects a violation.

2)Valid additionally after deactivation of $\overline{\text{PORST}}$ until the internal reset phase has finished. See the SCU chapter for details.

3) See the SCU_IOCR register description.

4) Depends on JTAG/DAP selection with $\overline{\text{TRST}}$.

In case of leakage test ($\overline{\text{PORST}}$ = 0 and $\overline{\text{TESTMODE}}$ = 0), the pull-down of the $\overline{\text{TRST}}$ pin is switched off. In case of an user application ($\overline{\text{TESTMODE}}$ = 1), the pull-down of the $\overline{\text{TRST}}$ is always switched on.

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## 2.3 TC270x Bare Die Pad Definition

The TC270x Bare Die Logic Symbol is shown in **Figure 2-3**.

**Table 2-40** describes the pads of the TC270x Bare Die. It describes also the mapping of VADC / DS-ADC channels to the analog inputs (ANx) and the mapping of Port functions to the pads.

*Note: The detailed description of the port functions (Px.y) can be found in the User's Manual chapter "General Purpose I/O Ports and Peripheral I/O LInes (Ports)".*

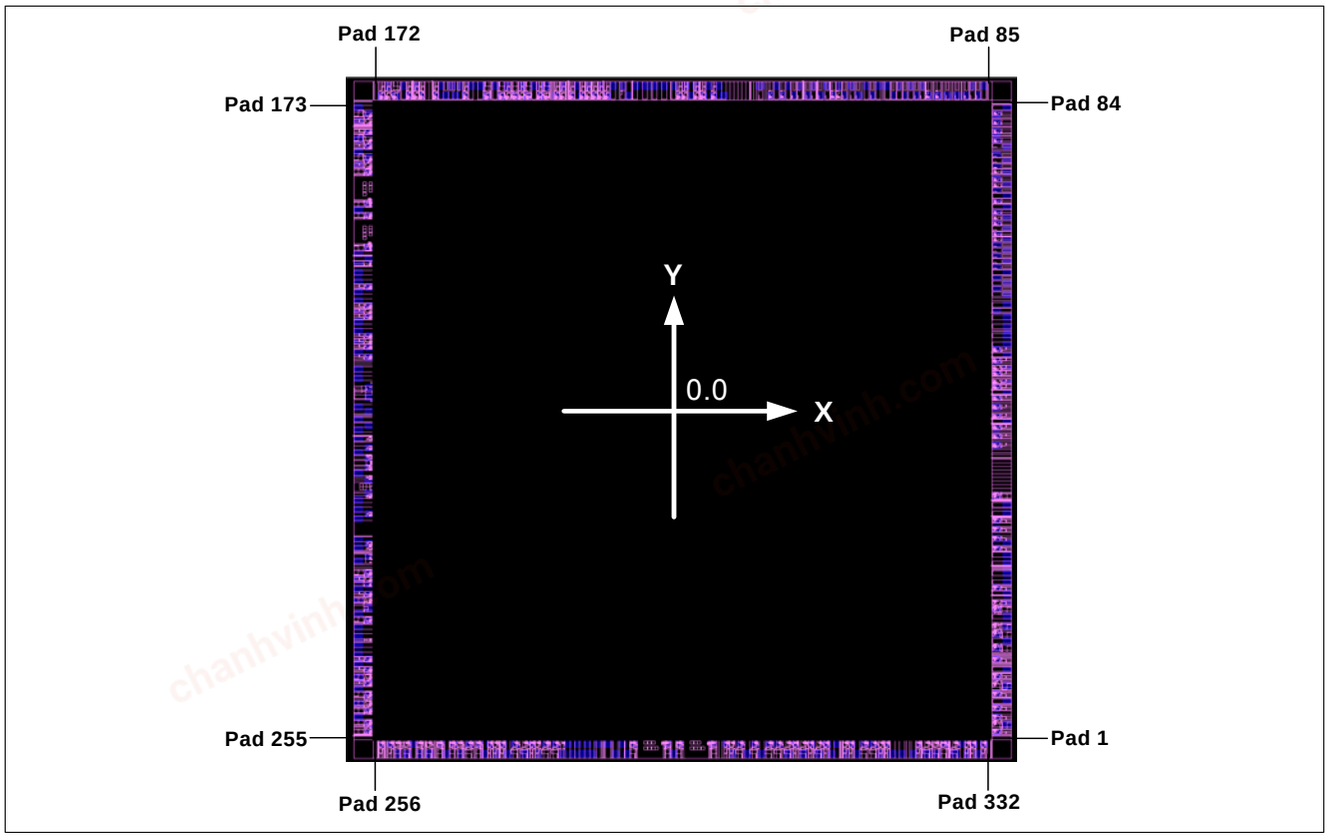



**Figure 2-3 TC270x Logic Symbol for the Bare Die.**

**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 1 | P10.8 | LP / PU1 / VEXT | 3265500 | -3460000 | GPIO |
| 2 | P02.0 | MP+ / PU1 / VEXT | 3374000 | -3380000 | GPIO |
| 3 | P02.9 | LP / PU1 / VEXT | 3265500 | -3300000 | GPIO |
| 4 | P02.1 | LP / PU1 / VEXT | 3265500 | -3200000 | GPIO |
| 5 | VSS | Vx | 3374000 | -3125000 | Must be bonded to VSS |
| 6 | P02.10 | LP / PU1 / VEXT | 3265500 | -3050000 | GPIO |
| 7 | P02.2 | MP+ / PU1 / VEXT | 3374000 | -2950000 | GPIO |
| 8 | P02.11 | LP / PU1 / VEXT | 3265500 | -2850000 | GPIO |
| 9 | VEXT | Vx | 3374000 | -2775000 | Must be bonded to VEXT |
| 10 | P02.3 | LP / PU1 / VEXT | 3265500 | -2670000 | GPIO |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 11 | P02.4 | MP+ / PU1 / VEXT | 3265500 | -2540000 | GPIO |
| 12 | VSS | Vx | 3374000 | -2465000 | Must be bonded to VSS |
| 13 | P02.5 | MP+ / PU1 / VEXT | 3265500 | -2390000 | GPIO |
| 14 | P02.6 | MP / PU1 / VEXT | 3374000 | -2300000 | GPIO |
| 15 | VEXT | Vx | 3374000 | -2195000 | Must be bonded to VEXT |
| 16 | P02.7 | MP / PU1 / VEXT | 3265500 | -2110000 | GPIO |
| 17 | P02.8 | LP / PU1 / VEXT | 3374000 | -2040000 | GPIO |
| 18 | VSS | Vx | 3374000 | -1940000 | Must be bonded to VSS |
| 19 | P01.3 | LP / PU1 / VEXT | 3265500 | -1883500 | GPIO |
| 20 | VDD | Vx | 3374000 | -1818500 | Must be bonded to VDD |
| 21 | VSS | Vx | 3374000 | -1688500 | Must be bonded to VSS |
| 22 | VSS | Vx | 3374000 | -1644500 | Must be bonded to VSS. Double Pad (Elephant Pad), shared with Pad Nr 22. |
| 23 | VDD | Vx | 3374000 | -1514500 | Must be bonded to VSS. Double Pad (Elephant Pad), shared with Pad Nr 21. |
| 24 | P01.4 | LP / PU1 / VEXT | 3265500 | -1449500 | GPIO |
| 25 | VSS | Vx | 3374000 | -1394500 | Must be bonded to VSS |
| 26 | P01.5 | LP / PU1 / VEXT | 3265500 | -1339500 | GPIO |
| 27 | P01.6 | LP / PU1 / VEXT | 3265500 | -1239500 | GPIO |
| 28 | P01.7 | LP / PU1 / VEXT | 3265500 | -1139500 | GPIO |
| 29 | VEXT | Vx | 3374000 | -1068500 | Must be bonded to VEXT |
| 30 | VSS | Vx | 3374000 | -968500 | Must be bonded to VSS |
| 31 | P00.0 | MP / PU1 / VEXT | 3265500 | -868500 | GPIO |
| 32 | P00.1 | LP / PU1 / VEXT | 3265500 | -241000 | GPIO |
| 33 | P00.2 | LP / PU1 / VEXT | 3265500 | -141000 | GPIO |
| 34 | P00.3 | LP / PU1 / VEXT | 3265500 | -41000 | GPIO |
| 35 | VSS | Vx | 3374000 | 19000 | Must be bonded to VSS |
| 36 | P00.4 | LP / PU1 / VEXT | 3265500 | 79000 | GPIO |
| 37 | P00.5 | LP / PU1 / VEXT | 3265500 | 179000 | GPIO |
| 38 | P00.6 | LP / PU1 / VEXT | 3265500 | 279000 | GPIO |
| 39 | VEXT | Vx | 3374000 | 339000 | Must be bonded to VEXT |
| 40 | P00.7 | LP / PU1 / VEXT | 3265500 | 399000 | GPIO |
| 41 | P00.8 | LP / PU1 / VEXT | 3374000 | 459000 | GPIO |
| 42 | P00.9 | LP / PU1 / VEXT | 3265500 | 549000 | GPIO |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 43 | P00.10 | LP / PU1 / VEXT | 3374000 | 609000 | GPIO |
| 44 | P00.11 | LP / PU1 / VEXT | 3265500 | 689000 | GPIO |
| 45 | VSS | Vx | 3374000 | 749000 | Must be bonded to VSS |
| 46 | P00.12 | LP / PU1 / VEXT | 3265500 | 809000 | GPIO |
| 47 | VDD | Vx | 3374000 | 864000 | Must be bonded to VDD |
| 48 | VSS | Vx | 3374000 | 964000 | Must be bonded to VSS |
| 49 | VSS | Vx | 3374000 | 1064000 | Must be bonded to VSS |
| 50 | VDD | Vx | 3374000 | 1164000 | Must be bonded to VDD |
| 51 | VEXT | Vx | 3265500 | 1239000 | Must be bonded to VEXT |
| 52 | VSS | Vx | 3374000 | 1299000 | Must be bonded to VSS |
| 53 | VAREF3 | Vx | 3374000 | 1419000 | Positive Analog Reference Voltage 3 |
| 54 | VAREF2 | Vx | 3265500 | 1479000 | Positive Analog Reference Voltage 2 |
| 55 | VAGND3 | Vx | 3374000 | 1539000 | Negative Analog Reference Voltage 3 |
| 56 | VAGND2 | Vx | 3265500 | 1599000 | Negative Analog Reference Voltage 2 |
| 57 | VDDM | Vx | 3374000 | 1659000 | Must be bonded to VEXT |
| 58 | AN47 (VADC5.7 / DS3ND) | D | 3265500 | 1719000 | Analog input |
| 59 | AN46 (VADC5.6 / DS3PD) | D | 3374000 | 1779000 | Analog input |
| 60 | AN45 (VADC5.5 / DS3NC) | D | 3265500 | 1839000 | Analog input |
| 61 | AN44 (VADC5.4 / DS3PC) | D | 3374000 | 1899000 | Analog input |
| 62 | AN43 (VADC5.3) | D | 3265500 | 1959000 | Analog input (with pull down diagnostics) |
| 63 | AN42 (VADC5.2) | D | 3374000 | 2019000 | Analog input |
| 64 | AN41 (VADC5.1) | D | 3265500 | 2079000 | Analog input |
| 65 | AN40 (VADC5.0) | D | 3374000 | 2139000 | Analog input |
| 66 | AN39 (VADC4.7 / DS3NB), P40.9 ( SENT9A) | S | 3265500 | 2199000 | Analog input, GPI (SENT) |
| 67 | AN38 (VADC4.6 / DS3PB), P40.8 ( SENT8A) | S | 3374000 | 2259000 | Analog input, GPI (SENT) |
| 68 | AN37 (VADC4.5 / DS3NA), P40.7 ( SENT7A) | S | 3265500 | 2319000 | Analog input, GPI (SENT) |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 69 | VDDM | Vx | 3374000 | 2379000 | Must be bonded to VEXT |
| 70 | AN36 (VADC4.4 / DS3PA), P40.6 ( SENT6A) | S | 3265500 | 2439000 | Analog input, GPI (SENT) |
| 71 | VSSM | Vx | 3374000 | 2499000 | Must be bonded to VSS |
| 72 | AN35 (VADC4.3) | D | 3265500 | 2559000 | Analog input (with pull down diagnostics) |
| 73 | AN34 (VADC4.2) | D | 3374000 | 2619000 | Analog input |
| 74 | AN33 (VADC4.1), P40.5 ( SENT5A) | S | 3265500 | 2679000 | Analog input, GPI (SENT) |
| 75 | AN32 (VADC4.0), P40.4 ( SENT4A) | S | 3374000 | 2765000 | Analog input, GPI (SENT) |
| 76 | AN31 (VADC3.7) | D | 3265500 | 2825000 | Analog input |
| 77 | AN30 (VADC3.6) | D | 3374000 | 2885000 | Analog input |
| 78 | AN29 (VADC3.5) | D | 3265500 | 2945000 | Analog input |
| 79 | AN28 (VADC3.4) | D | 3374000 | 3045000 | GPIO |
| 80 | AN27 (VADC3.3), P40.3 ( SENT3A) | S | 3265500 | 3105000 | Analog input (with pull down diagnostics), GPI (SENT) |
| 81 | AN26 (VADC3.2), P40.2 ( SENT2A) | S | 3265500 | 3205000 | Analog input, GPI (SENT) |
| 82 | AN25 (VADC3.1 / DS2NB), P40.1 ( SENT1A) | S | 3265500 | 3305000 | Analog input, GPI (SENT) |
| 83 | AN24 (VADC3.0 / DS2PB), P40.0 ( SENT0A) | S | 3265500 | 3405000 | Analog input, GPI (SENT) |
| 84 | VDDM | Vx | 3374000 | 3465000 | Must be bonded to VEXT |
| 85 | VSSM | Vx | 3134000 | 3705000 | Must be bonded to VSS |
| 86 | AN23 (VADC2.7) | D | 3074000 | 3596500 | Analog input |
| 87 | AN22 (VADC2.6) | D | 3014000 | 3705000 | Analog input |
| 88 | AN21 (VADC2.5 / DS2NA) | D | 2954000 | 3596500 | Analog input |
| 89 | AN20 (VADC2.4 / DS2PA) | D | 2854000 | 3596500 | Analog input |
| 90 | AN19 (VADC2.3) | D | 2754000 | 3596500 | Analog input (with pull down diagnostics) |
| 91 | AN18 (VADC2.2) | D | 2654000 | 3596500 | Analog input |
| 92 | AN17 (VADC2.1) | D | 2554000 | 3596500 | Analog input |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 93 | AN16 (VADC2.0) | D | 2494000 | 3705000 | Analog input |
| 94 | AN15 (VADC1.7) | D | 2434000 | 3596500 | Analog input |
| 95 | VAGND1 | Vx | 2374000 | 3705000 | Negative Analog Reference Voltage 1 |
| 96 | VAGND0 | Vx | 2314000 | 3596500 | Negative Analog Reference Voltage 0 |
| 97 | VAREF1 | Vx | 2254000 | 3705000 | Positive Analog Reference Voltage 1 |
| 98 | VAREF0 | Vx | 2194000 | 3596500 | Positive Analog Reference Voltage 0 |
| 99 | VSSM | Vx | 2134000 | 3705000 | Must be bonded to VSS |
| 100 | VSSM | Vx | 2074000 | 3596500 | Must be bonded to VSS |
| 101 | VSSMREF | Vx | 2014000 | 3705000 | Must be bonded to VSS |
| 102 | AN14 (VADC1.6) | D | 1954000 | 3596500 | Analog input |
| 103 | VDDM | Vx | 1894000 | 3705000 | Must be bonded to VEXT |
| 104 | VDDM | Vx | 1829000 | 3596500 | Must be bonded to VEXT |
| 105 | AN13 (VADC1.5) | D | 1724000 | 3596500 | Analog input |
| 106 | AN12 (VADC1.4) | D | 1664000 | 3705000 | Analog input |
| 107 | AN11 (VADC1.3) | D | 1604000 | 3596500 | Analog input (with pull down diagnostics) |
| 108 | AN10 (VADC1.2) | D | 1544000 | 3705000 | Analog input |
| 109 | AN9 (VADC1.1) | D | 1484000 | 3569500 | Analog input |
| 110 | AN8 (VADC1.0) | D | 1424000 | 3705000 | Analog input |
| 111 | AN7 (VADC0.7) | D | 1364000 | 3596500 | Analog input (with pull down diagnostics) |
| 112 | AN6 (VADC0.6) | D | 1304000 | 3705000 | Analog input |
| 113 | AN5 (VADC0.5) | D | 1244000 | 3596500 | Analog input |
| 114 | AN4 (VADC0.4) | D | 1184000 | 3705000 | Analog input |
| 115 | AN3 (VADC0.3 / DS0NA) | D | 1124000 | 3596500 | Analog input |
| 116 | VSSM | Vx | 1064000 | 3705000 | Must be bonded to VSS |
| 117 | AN2 (VADC0.2 / DS0PA) | D | 1004000 | 3596500 | Analog input |
| 118 | VDDM | Vx | 944000 | 3705000 | Must be bonded to VEXT |
| 119 | AN1 (VADC0.1 / DS1NA) | D | 884000 | 3596500 | Analog input |
| 120 | AN0 (VADC0.0 / DS1PA) | D | 807000 | 3705000 | Analog input |
| 121 | VEXT | Vx | 427000 | 3596500 | Must be bonded to VEXT |
| 122 | VSS | Vx | 377000 | 3705000 | Must be bonded to VSS |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 123 | P34.1 | LP / PU1 / VEXT | 322000 | 3596500 | GPIO |
| 124 | VSS | Vx | 267000 | 3705000 | Must be bonded to VSS |
| 125 | P34.2 | LP / PU1 / VEXT | 212000 | 3596500 | GPIO |
| 126 | P34.3 | LP / PU1 / VEXT | 142000 | 3705000 | GPIO |
| 127 | VEXT | Vx | 87000 | 3596500 | Must be bonded to VEXT |
| 128 | P34.4 | LP / PU1 / VEXT | 22000 | 3705000 | GPIO |
| 129 | P34.5 | LP / PU1 / VEXT | -38000 | 3596500 | GPIO |
| 130 | VSS | Vx | -93000 | 3705000 | Must be bonded to VSS |
| 131 | VDD | Vx | -193000 | 3705000 | Must be bonded to VDD |
| 132 | VSS | Vx | -323000 | 3705000 | Must be bonded to VSS. Double Pad (Elephant Pad), shared with Pad Nr 131. |
| 133 | VSS | Vx | -363000 | 3705000 | Must be bonded to VSS. Double Pad (Elephant Pad), shared with Pad Nr 130. |
| 134 | VDD | Vx | -493000 | 3705000 | Must be bonded to VDD |
| 135 | VEVRSB | Vx | -560000 | 3596500 | Must be bonded to VEXT |
| 136 | EVR_OFF | Vx | -625000 | 3705000 | Must be bonded to VSS+F178 |
| 137 | VEXT | Vx | -725000 | 3705000 | Must be bonded to VEXT |
| 138 | P33.0 | LP / PU1 / VEXT | -790000 | 3596500 | GPIO |
| 139 | P33.1 | LP / PU1 / VEXT | -855000 | 3705000 | GPIO |
| 140 | P33.2 | LP / PU1 / VEXT | -915000 | 3596500 | GPIO |
| 141 | P33.3 | LP / PU1 / VEXT | -985000 | 3705000 | GPIO |
| 142 | P33.4 | LP / PU1 / VEXT | -1045000 | 3596500 | GPIO |
| 143 | VSS | Vx | -1100000 | 3705000 | Must be bonded to VSS |
| 144 | P33.5 | LP / PU1 / VEXT | -1155000 | 3596500 | GPIO |
| 145 | P33.6 | LP / PU1 / VEXT | -1250000 | 3705000 | GPIO |
| 146 | P33.7 | LP / PU1 / VEXT | -1310000 | 3596500 | GPIO |
| 147 | P33.8 | MP / HighZ / VEXT | -1420000 | 3705000 | GPIO |
| 148 | P33.9 | LP / PU1 / VEXT | -1490000 | 3596500 | GPIO |
| 149 | VEXT | Vx | -1545000 | 3705000 | Must be bonded to VEXT |
| 150 | P33.10 | MP / PU1 / VEXT | -1610000 | 3596500 | GPIO |
| 151 | P33.14 | LP / PU1 / VEXT | -1680000 | 3705000 | GPIO |
| 152 | P33.11 | MP / PU1 / VEXT | -1750000 | 3596500 | GPIO |
| 153 | P33.15 | LP / PU1 / VEXT | -1820000 | 3705000 | GPIO |
| 154 | P33.12 | MP / PU1 / VEXT | -1890000 | 3596500 | GPIO |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 155 | VSS | Vx | -1955000 | 3705000 | Must be bonded to VSS |
| 156 | P33.13 | MP / PU1 / VEXT | -2040000 | 3596500 | GPIO |
| 157 | VSS | Vx | -2105000 | 3705000 | Must be bonded to VSS |
| 158 | VDD | Vx | -2205000 | 3705000 | Must be bonded to VDD |
| 159 | P32.0 | LP / EVR13 SMPS -> PD, GPIO -> PU1 / VEXT | -2260000 | 3596500 | GPIO |
| 160 | VGATE1N (SMPS) | VGATE1N | -2315000 | 3705000 | Must be bonded to VSS if EVR13 SMPS is not used. Must be bonded to NMOS gate if EVR13 SMPS used. |
| 161 | VGATE1P (SMPS) | VGATE1P | -2365000 | 3596500 | Must be bonded to VEXT if EVR13 SMPS is not used. Must be bonded to PMOS gate if EVR13 SMPS used. |
| 162 | VGATE3P (LDO) | VGATE3P | -2415000 | 3705000 | Must be bonded to VSS |
| 163 | VGATE1P (LDO) | VGATE1P | -2465000 | 3596500 | Must be bonded to VSS if no external P channel MOSFET used for EVR13 LDO generation. Must be bonded to external P channnel MOSFET if external LDO pass device used. |
| 164 | VEXT | Vx | -2515000 | 3705000 | Must be bonded to VEXT |
| 165 | P32.2 | LP / PU1 / VEXT | -2570000 | 3596500 | GPIO |
| 166 | P32.3 | LP / PU1 / VEXT | -2714000 | 3596500 | GPIO |
| 167 | P32.6 | LP / PU1 / VEXT | -2774000 | 3705000 | GPIO |
| 168 | P32.5 | LP / PU1 / VEXT | -2849000 | 3596500 | GPIO |
| 169 | VSS | Vx | -2904000 | 3705000 | Must be bonded to VSS |
| 170 | P32.4 | MP+ / PU1 / VEXT | -2989000 | 3596500 | GPIO |
| 171 | P32.7 | LP / PU1 / VEXT | -3069000 | 3705000 | GPIO |
| 172 | P23.0 | LP / PU1 / VEXT | -3129000 | 3596500 | GPIO |
| 173 | VSS | Vx | -3374000 | 3391000 | Must be bonded to VSS |
| 174 | P23.1 | MP+ / PU1 / VEXT | -3265500 | 3316000 | GPIO |
| 175 | P23.2 | LP / PU1 / VEXT | -3374000 | 3236000 | GPIO |
| 176 | P23.3 | LP / PU1 / VEXT | -3265500 | 3125000 | GPIO |
| 177 | P23.4 | MP+ / PU1 / VEXT | -3374000 | 3045000 | GPIO |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 178 | P23.6 | LP / PU1 / VEXT | -3265500 | 2965000 | GPIO |
| 179 | VEXT | Vx | -3374000 | 2910000 | Must be bonded to VEXT |
| 180 | P23.5 | MP+ / PU1 / VEXT | -3265500 | 2835000 | GPIO |
| 181 | P23.7 | LP / PU1 / VEXT | -3374000 | 2755000 | GPIO |
| 182 | P22.0 | MP / LVDSM_N / PU1 / VEXT | -3265500 | 2685000 | GPIO |
| 183 | P22.1 | MP / LVDS_P / PU1 / VEXT | -3265500 | 2335000 | GPIO |
| 184 | VSS | Vx | -3374000 | 2270000 | Must be bonded to VSS |
| 185 | P22.2 | MP / LVDSM_N / PU1 / VEXT | -3265500 | 2205000 | GPIO |
| 186 | P22.3 | MP / LVDS_P / PU1 / VEXT | -3265500 | 1855000 | GPIO |
| 187 | VEXT | Vx | -3374000 | 1790000 | Must be bonded to VEXT |
| 188 | VEXT | Vx | -3265500 | 1735000 | Must be bonded to VEXT |
| 189 | Reserved | Vx | -3374000 | 1680000 | Must be bonded to VSS |
| 190 | VDD | Vx | -3374000 | 1580000 | Must be bonded to VDD |
| 191 | VSS | Vx | -3374000 | 1480000 | Must be bonded to VSS |
| 192 | P22.4 | LP / PU1 / VEXT | -3265500 | 1425000 | GPIO |
| 193 | VSS | Vx | -3374000 | 1370000 | Must be bonded to VSS |
| 194 | VDD | Vx | -3374000 | 1270000 | Must be bonded to VDD |
| 195 | P22.5 | LP / PU1 / VEXT | -3265500 | 1215000 | GPIO |
| 196 | P22.6 | LP / PU1 / VEXT | -3374000 | 1155000 | GPIO |
| 197 | P22.7 | LP / PU1 / VEXT | -3265500 | 1095000 | GPIO |
| 198 | VSS | Vx | -3374000 | 1040000 | Must be bonded to VSS |
| 199 | VDD | Vx | -3374000 | 940000 | Must be bonded to VDD |
| 200 | P22.8 | LP / PU1 / VEXT | -3265500 | 885000 | GPIO |
| 201 | P22.9 | LP / PU1 / VEXT | -3374000 | 825000 | GPIO |
| 202 | P22.10 | LP / PU1 / VEXT | -3265500 | 765000 | GPIO |
| 203 | VSS | Vx | -3374000 | 710000 | Must be bonded to VSS |
| 204 | P22.11 | LP / PU1 / VEXT | -3265500 | 655000 | GPIO |
| 205 | VDDOSC | Vx | -3374000 | 520000 | Must be bonded to VDD |
| 206 | VSSOSC | Vx | -3374000 | 420000 | Must be bonded to VSS |
| 207 | XTAL1 | XTAL1 | -3265500 | 312500 | Main Oscillator/PLL/Clock Generator Input. Must be bonded to external quartz or resonator |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 208 | XTAL2 | XTAL2 | -3265500 | 212500 | Main Oscillator/PLL/Clock Generator Input. Must be bonded to external quartz or resonator |
| 209 | VSSOSC3 | Vx | -3374000 | 105000 | Must be bonded to VSS |
| 210 | VDDOSC3 | Vx | -3265500 | 55000 | Must be bonded to VDDP3 |
| 211 | VDDP3 | Vx | -3374000 | -35000 | Must be bonded to VDDP3 |
| 212 | VDDP3 | Vx | -3265500 | -95000 | Must be bonded to VDDP3 |
| 213 | VSS | Vx | -3374000 | -145000 | Must be bonded to VSS |
| 214 | P21.0 | A2 / PU1 / VDDP3 | -3374000 | -245000 | GPIO |
| 215 | P21.1 | A2 / PU1 / VDDP3 | -3265500 | -345000 | GPIO |
| 216 | VSS | Vx | -3374000 | -395000 | Must be bonded to VSS |
| 217 | P21.2 | LVDSH_N / PU1 / VDDP3 | -3265500 | -457500 | GPIO |
| 218 | P21.3 | LVDSH_P / PU1 / VDDP3 | -3265500 | -557500 | GPIO |
| 219 | VDDP3 | Vx | -3374000 | -620000 | Must be bonded to VDDP3 |
| 220 | P21.4 | LVDSH_N / PU1 / VDDP3 | -3265500 | -694500 | GPIO |
| 221 | P21.5 | LVDSH_P / PU1 / VDDP3 | -3265500 | -845500 | GPIO |
| 222 | VDD | Vx | -3374000 | -920000 | Must be bonded to VDD |
| 223 | VSS | Vx | -3374000 | -1020000 | Must be bonded to VSS |
| 224 | P21.6 | A2 / PU / VDDP3 | -3265500 | -1070000 | GPIO, TDI |
| 225 | VDDP3 | Vx | -3374000 | -1120000 | Must be bonded to VDDP3 |
| 226 | VSS | Vx | -3374000 | -1345000 | Must be bonded to VSS |
| 227 | TMS / DAP1 | A2 / PD / VDDP3 | -3265500 | -1395000 | JTAG Module State Machine Control Input / Device Access Port Line 1 |
| 228 | P21.7 | A2 / PU / VDDP3 | -3374000 | -1445000 | GPIO, TDO |
| 229 | TRST (N) | A2 / PU / VDDP3 | -3265500 | -1535000 | JTAG Module Reset/Enable Input |
| 230 | TCK / DAP0 | A2 / PU / VDDP3 | -3374000 | -1585000 | JTAG Module Clock Input / Device Access Port Line 0 |
| 231 | P20.0 | MP / PU1 / VEXT | -3265500 | -1720000 | GPIO |
| 232 | P20.1 | LP / PU1 / VEXT | -3374000 | -1790000 | GPIO |
| 233 | P20.2 | LP / PU / VEXT | -3265500 | -1845000 | Testmode pin must be bonded |
| 234 | VSS | Vx | -3374000 | -1895000 | Must be bonded to VSS |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 235 | P20.3 | LP / PU1 / VEXT | -3265500 | -1950000 | GPIO |
| 236 | ESR1 (N) / EVRWUP | MP / PU1 / VEXT | -3374000 | -2020000 | External System Request Reset 1. Default NMI function. EVR Wakeup Pin. |
| 237 | PORST (N) | I / PD1 / VEXT | -3265500 | -2102500 | Power On Reset Input. Additional strong PD in case of power fail. |
| 238 | VEXT | Vx | -3374000 | -2170000 | Must be bonded to VEXT |
| 239 | ESR0 (N) / EVRWUP | MP / OD | -3265500 | -2235000 | External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. EVR Wakeup Pin. |
| 240 | VDD | Vx | -3374000 | -2310000 | Must be bonded to VDD |
| 241 | VSS | Vx | -3374000 | -2440000 | Must be bonded to VSS. Double Pad (Elephant Pad), shared with Pad Nr 240. |
| 242 | VSS | Vx | -3374000 | -2480000 | Must be bonded to VSS. Double Pad (Elephant Pad), shared with Pad Nr 239. |
| 243 | VDD | Vx | -3374000 | -2610000 | Must be bonded to VDD |
| 244 | P20.6 | LP / PU1 / VEXT | -3265500 | -2665000 | GPIO |
| 245 | VSS | Vx | -3374000 | -2720000 | Must be bonded to VSS |
| 246 | P20.7 | LP / PU1 / VEXT | -3265500 | -2775000 | GPIO |
| 247 | P20.8 | MP / PU1 / VEXT | -3374000 | -2865000 | GPIO |
| 248 | P20.9 | LP / PU1 / VEXT | -3265500 | -2935000 | GPIO |
| 249 | VEXT | Vx | -3374000 | -2990000 | Must be bonded to VEXT |
| 250 | P20.10 | MP / PU1 / VEXT | -3265500 | -3055000 | GPIO |
| 251 | P20.11 | MP / PU1 / VEXT | -3374000 | -3155000 | GPIO |
| 252 | P20.12 | MP / PU1 / VEXT | -3265500 | -3235000 | GPIO |
| 253 | VSS | Vx | -3374000 | -3300000 | Must be bonded to VSS |
| 254 | P20.13 | MP / PU1 / VEXT | -3265500 | -3365000 | GPIO |
| 255 | P20.14 | MP / PU1 / VEXT | -3265500 | -3465000 | GPIO |
| 256 | P15.0 | LP / PU1 / VEXT | -3134000 | -3596500 | GPIO |
| 257 | P15.1 | LP / PU1 / VEXT | -3034000 | -3596500 | GPIO |
| 258 | P15.2 | MP / PU1 / VEXT | -2964000 | -3705000 | GPIO |
| 259 | P15.3 | MP / PU1 / VEXT | -2864000 | -3705000 | GPIO |
| 260 | VEXT | Vx | -2799000 | -3596500 | Must be bonded to VEXT |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 261 | P15.4 | MP / PU1 / VEXT | -2734000 | -3705000 | GPIO |
| 262 | P15.5 | MP / PU1 / VEXT | -2634000 | -3705000 | GPIO |
| 263 | P15.6 | MP / PU1 / VEXT | -2522000 | -3596500 | GPIO |
| 264 | VSS | Vx | -2457000 | -3705000 | Must be bonded to VSS |
| 265 | P15.7 | MP / PU1 / VEXT | -2392000 | -3596500 | GPIO |
| 266 | P15.8 | MP / PU1 / VEXT | -2312000 | -3705000 | GPIO |
| 267 | P14.0 | MP+ / PU1 / VEXT | -2222000 | -3596500 | GPIO |
| 268 | P14.1 | MP / PU1 / VEXT | -2122000 | -3596500 | GPIO |
| 269 | VEXT | Vx | -2057000 | -3705000 | Must be bonded to VEXT |
| 270 | P14.2 | LP / PU1 / VEXT | -2002000 | -3596500 | Must be bonded to VEXT if EVR13 active. Must be bonded to VSS if EVR13 inactive. |
| 271 | P14.3 | LP / PU1 / VEXT | -1942000 | -3705000 | GPIO |
| 272 | P14.4 | LP / PU1 / VEXT | -1872000 | -3596500 | GPIO |
| 273 | VSS | Vx | -1817000 | -3705000 | Must be bonded to VSS |
| 274 | P14.5 | MP+ / PU1 / VEXT | -1742000 | -3596500 | GPIO |
| 275 | P14.6 | MP+ / PU1 / VEXT | -1642000 | -3705000 | GPIO |
| 276 | P14.7 | LP / PU1 / VEXT | -1562000 | -3596500 | GPIO |
| 277 | P14.8 | LP / PU1 / VEXT | -1502000 | -3705000 | GPIO |
| 278 | P14.9 | MP+ / PU1 / VEXT | -1422000 | -3596500 | GPIO |
| 279 | P14.10 | MP+ / PU1 / VEXT | -1322000 | -3596500 | GPIO |
| 280 | Reserved | Vx | -1247000 | -3705000 | Must be bonded to VSS |
| 281 | VEXT | Vx | -1197000 | -3596500 | Must be bonded to VEXT |
| 282 | VSS | Vx | -1147000 | -3705000 | Must be bonded to VSS |
| 283 | VEXT | Vx | -1097000 | -3596500 | Must be bonded to VEXT |
| 284 | VSS | Vx | -1017000 | -3705000 | Must be bonded to VSS. Double Pad (Elephant Pad), shared with Pad Nr 284. |
| 285 | VDDP3 | Vx | -994500 | -3596500 | Must be bonded to VDDP3 |
| 286 | VSS | Vx | -972000 | -3705000 | Must be bonded to VSS. Double Pad (Elephant Pad), shared with Pad Nr 282. |
| 287 | VDDP3 | Vx | -877000 | -3596500 | Must be bonded to VDDP3 |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 288 | VDDFL3 | Vx | -777000 | -3596500 | Must be bonded to VDDP3 |
| 289 | VDDFL3 | Vx | -697000 | -3705000 | Must be bonded to VDDP3 |
| 290 | VDDFL3 | Vx | -629500 | -3596500 | Must be bonded to VDDP3 |
| 291 | VSS | Vx | -577000 | -3705000 | Must be bonded to VSS |
| 292 | P13.0 | MP / LVDSM_N / PU1 / VEXT | -512000 | -3596500 | GPIO |
| 293 | P13.1 | MP / LVDS_P / PU1 / VEXT | -162000 | -3596500 | GPIO |
| 294 | VEXT | Vx | -97000 | -3705000 | Must be bonded to VEXT |
| 295 | P13.2 | MP / LVDSM_N / PU1 / VEXT | -32000 | -3596500 | GPIO |
| 296 | P13.3 | MP / LVDS_P / PU1 / VEXT | 318000 | -3596500 | GPIO |
| 297 | P12.0 | LP / PU1 / VFLEX | 458000 | -3596500 | GPIO |
| 298 | P12.1 | LP / PU1 / VFLEX | 518000 | -3705000 | GPIO |
| 299 | P11.0 | MP+ / PU1 / VFLEX | 598000 | -3596500 | GPIO |
| 300 | VSSFLEX | Vx | 673000 | -3705000 | Must be bonded to VSS |
| 301 | P11.1 | MP+ / PU1 / VFLEX | 748000 | -3596500 | GPIO |
| 302 | VFLEX | Vx | 823000 | -3705000 | Must be bonded to VEXT or VDDP3 |
| 303 | P11.2 | MPR / PU1 / VFLEX | 898000 | -3596500 | GPIO |
| 304 | P11.3 | MPR / PU1 / VFLEX | 998000 | -3596500 | GPIO |
| 305 | P11.4 | MP+ / PU1 / VFLEX | 1098000 | -3705000 | GPIO |
| 306 | P11.5 | LP / PU1 / VFLEX | 1178000 | -3596500 | GPIO |
| 307 | P11.6 | MPR / PU1 / VFLEX | 1258000 | -3705000 | GPIO |
| 308 | P11.7 | LP / PU1 / VFLEX | 1338000 | -3596500 | GPIO |
| 309 | P11.9 | MP+ / PU1 / VFLEX | 1418000 | -3705000 | GPIO |
| 310 | P11.8 | LP / PU1 / VFLEX | 1498000 | -3596500 | GPIO |
| 311 | VSSFLEX | Vx | 1553000 | -3705000 | Must be bonded to VSS |

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**Table 2-40 List of the TC270x Bare Die Pads**

| Number | Pad Name | Pad Type | X | Y | Comment |
|---|---|---|---|---|---|
| 312 | VFLEX | Vx | 1603000 | -3596500 | Must be bonded to VEXT or VDDP3 |
| 313 | P11.10 | LP / PU1 / VFLEX | 1698000 | -3705000 | GPIO |
| 314 | P11.13 | LP / PU1 / VFLEX | 1758000 | -3596500 | GPIO |
| 315 | VSSFLEX | Vx | 1813000 | -3705000 | Must be bonded to VSS |
| 316 | P11.11 | MP+ / PU1 / VFLEX | 1888000 | -3596500 | GPIO |
| 317 | P11.12 | MPR / PU1 / VFLEX | 1988000 | -3596500 | GPIO |
| 318 | P11.14 | LP / PU1 / VFLEX | 2068000 | -3705000 | GPIO |
| 319 | P11.15 | LP / PU1 / VFLEX | 2128000 | -3596500 | GPIO |
| 320 | VDD | Vx | 2183000 | -3705000 | Must be bonded to VDD |
| 321 | VSS | Vx | 2283000 | -3705000 | Must be bonded to VSS |
| 322 | VSS | Vx | 2403000 | -3705000 | Must be bonded to VSS |
| 323 | P10.0 | LP / PU1 / VEXT | 2458000 | -3596500 | GPIO |
| 324 | P10.1 | MP+ / PU1 / VEXT | 2543000 | -3705000 | GPIO |
| 325 | P10.2 | MP / PU1 / VEXT | 2643000 | -3705000 | GPIO |
| 326 | P10.3 | MP / PU1 / VEXT | 2723000 | -3596500 | GPIO |
| 327 | P10.4 | MP+ / PU1 / VEXT | 2834000 | -3705000 | GPIO |
| 328 | VEXT | Vx | 2909000 | -3596500 | Must be bonded to VEXT |
| 329 | P10.5 | LP / PU1 / VEXT | 2964000 | -3705000 | GPIO |
| 330 | P10.6 | LP / PU1 / VEXT | 3024000 | -3596500 | GPIO |
| 331 | VSS | Vx | 3079000 | -3705000 | Must be bonded to VSS |
| 332 | P10.7 | LP / PU1 / VEXT | 3134000 | -3596500 | GPIO |

**Legend:**

Column “**Number**”:

Running number of pads in the pad frame

Column “**Name**”:

Symbolic name of the pad.

The functions mapped on GPIO pads “Px.y” are described in the User’s Manual chapter ”General Purpose I/O Ports and Peripheral I/O LInes (Ports)”

Column “**Type**”:

LP = Pad class LP (5V/3.3V, LVTTL)
MP = Pad class MP (5V/3.3V, LVTTL)
MP+ = Pad class MP+ (5V/3.3V, LVTTL)

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MPR = Pad class MPR (5V/3.3V, LVTTL)
A2 = Pad class A2 (3.3V, LVTTL)
LVDSM = Pad class LVDSM (LVDS/CMOS 5V/3.3V)
LVDSH = Pad class LVDSH (LVDS/CMOS 3.3V)
S = Pad class S (ADC overlayed with General Purpose Input)
D = Pad class D (ADC)
PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PU1 = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
PD1 = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PX = Behavior depends on usage: PD in EVR13 SMPS Mode and PU1 in GPIO Mode
OD = open drain during reset ($\overline{\text{PORST}}$ = 0)
HighZ = tri-state during reset ($\overline{\text{PORST}}$ = 0)
$\overline{\text{PORST}}$ = $\overline{\text{PORST}}$ input pad
XTAL1 = XTAL1 input pad
XTAL2 = XTAL2 input pad
VGATE1P = VGATE1P
VGATE3P = VGATE3P
Vx = Supply
NC = These pins are reserved for future extensions and shall not be connected externally
NC1 = These pins are not connected on package level and will not be used for future extensions
NCVDDPSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.
NCVDDSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.

Column “**X**” / “**Y**”:

Pad opening center coordinates (in nm)

### 2.3.1 Pad Openings

Two different pad openings are used:

- Standard Pad Opening is 70um x 75um where 70um is the width of the opening (width as seen from the die side) and 75um is the depth of the opening (from the die side into the silicon).
- Double Pad or Elephant Pad Opening is 130um x 75um where 130um is the width of the opening (width as seen from the die side) and 75um is the depth of the opening (from the die side into the silicon). The Double Pad openings are represented with two opening coordinates and two pad numbers. Double Pads are used only for supply and can be identified by the words ´Double Pad´ or ´Elephant Pad´ in the Comment column.

### 2.3.2 Emergency Stop Function

The Emergency Stop function can be used to force GPIOs (General Purpose Inputs/Outputs) via an external input signal (EMGSTOPA or EMGSTOPB) into a defined state:

1)The default state of GPIOs (Px.y) during and after $\overline{\text{PORST}}$ active is controllled via HWCFG[6] (P14.4). HWCFG[6] has a weak internal pull-up active at start-up if the pin is left unconnected.See also User´s Manual, “Introduction Chapter”, “General Purpose I/O Ports and Peripheral I/O Lines”, Figure: “Default state of port pins during and after reset”.

2) If HWCFG[6] is left unconnected or is externally pulled high, weak internal pull-ups are active at GPIOs (Px.y) pins during and after reset. Exceptions are P33.8 (HighZ), P40.x (default configuration during and after reset: analog inputs, port input funtion disabled), ESR0, P21.6 / P21.7 (port pins overlayed with JTAG functionality).

3) If HWCFG[6] is connected to ground, port pins are predominantly in HighZ during and after reset. Exceptions are P33.8 (HighZ), P40.x (default configuration during and after reset: analog inputs, port input funtion disabled), ESR0, P21.6 / P21.7 (port pins overlayed with JTAG functionality).

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- Input state and
- PU or HighZ depending on HWCFG[6] level latched during $\overline{\text{PORST}}$ active

Control of the Emergency Stop function:

- The Emergency Stop function can be enabled/disabled in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- The Emergency Stop input signal, EMGSTOPA (P33.8) / EMGSTOPB (P21.2) , can selected in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- On port level, each GPIO can be enabled/disabled for the Emergency Stop function via the Px_ESR (Port x Emergency Stop) registers in the port control logic (see chapter “General Purpose I/O Ports and Peripheral I/O Lines”, “Emergency Stop Register”).

The Emergency Stop function is available for all GPIO Ports with the following exceptions:

- Not available for P20.2 (General Purpose Input/GPI only, overlayed with Testmode)
- Not available for P40.x (analoge input ANx overlayed with GPI)
- Not available for P32.0 EVR13 SMPS mode.
- Not available for dedicated I/O without General Purpose Output function (e.g ESRx, TMS, TCK)

The Emergency Stop function can be overruled on the following GPIO Ports:

- P00.x: Emergency Stop can be overruled by the VADC. Overruling can be disabled via the control register P00_SCR (see chapter “General Purpose I/O Ports and Peripheral I/O Lines”, P00)
- P14.0 and P14.1: Emergency Stop can be overruled in the DXCPL mode (DAP over can physical layer mode). No Overruling in the DXCM (Debug over can message) mode
- P21.6: Emergency Stop can be overruled in JTAG mode if this pin is used as TDI
- P21.7: Emergency Stop can be overruled in JTAG or Three Pin DAP mode
- P20.0: Emergency Stop can be overruled in JTAG mode if this GPIO is used as TDI

### 2.3.3 Pull-Up/Pull-Down Reset Behavior of the Pins

**Table 2-41 List of Pull-Up/Pull-Down Reset Behavior of the Pins**

| Pins | $\overline{\text{PORST}}$ = 0 | $\overline{\text{PORST}}$ = 1 |
|---|---|---|
| $\overline{\text{all GPIOs}}$ | Pull-up if HWCFG[6] = 1 or High-Z if HWCFG[6] = 0 | |
| $\overline{\text{TDI}}$, $\overline{\text{TESTMODE}}$ | Pull-up | |
| $\overline{\text{PORST}}$[1)] | Pull-down with $I_{PORST}$ relevant | Pull-down with $I_{PDLI}$ relevant |
| $\overline{\text{TRST}}$, TCK, TMS | Pull-down | |
| $\overline{\text{ESR0}}$ | The open-drain driver is used to drive low.[2)] | Pull-up[3)] |
| $\overline{\text{ESR1}}$ | Pull-up[3)] | |
| TDO | Pull-up | High-Z/Pull-up[4)] |

1) Pull-down with $I_{PORST}$ relevant is always activated when a primary supply monitor detects a violation.
2) Valid additionally after deactivation of $\overline{\text{PORST}}$ until the internal reset phase has finished. See the SCU chapter for details.
3) See the SCU_IOCR register description.
4) Depends on JTAG/DAP selection with $\overline{\text{TRST}}$.

- In case of leakage test ($\overline{\text{PORST}}$ = 0 and $\overline{\text{TESTMODE}}$ = 0), the pull-down of the $\overline{\text{TRST}}$ pin is switched off. In case of an user application ($\overline{\text{TESTMODE}}$ = 1), the pull-down of the $\overline{\text{TRST}}$ is always switched on.

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# 3 Electrical Specification

## 3.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC270 / TC275 / TC277 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC270 / TC275 / TC277 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC270 / TC275 / TC277 designed in.

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## 3.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the Operational Conditions of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 3-1 Absolute Maximum Ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Storage Temperature | $T_{ST}$ SR | -65 | - | 170 | °C | upto 65h @ $T_J$ = 150°C; upto 15h @ $T_J$ = 170°C |
| Voltage at $V_{DD}$ power supply pins with respect to $V_{SS}$ 1) | $V_{DD}$ SR | - | - | 1.9 | V | |
| Voltage at $V_{DDP3}$ and $V_{DDFL3}$ power supply pins with respect to $V_{SS}$ 1) | $V_{DDP3}$ SR | - | - | 4.43 | V | |
| Voltage at $V_{DDM}$, $V_{EXT}$ and $V_{FLEX}$ power supply pins with respect to $V_{SS}$ 1) | $V_{DDM}$ SR | - | - | 7.0 | V | |
| Voltage on any class A2 and LVDSH input pin with respect to $V_{SS}$ 1)2) | $V_{IN}$ SR | -0.5 | - | min( $V_{DDP3}$ + 0.6 , 4.23 ) | V | Whatever is lower |
| Voltage on all other input pins with respect to $V_{SS}$ 1)2) | $V_{IN}$ SR | -0.5 | - | 7.0 | V | |
| Input current on any pin during overload condition 3) | $I_{IN}$ SR | -10 | - | 10 | mA | |
| Absolute maximum sum of all input circuit currents during overload condition 3) | $\Sigma I_{IN}$ SR | -100 | - | 100 | mA | |

1) Valid for cumulated for up to 2.8h and pulse forms following a power supply switch on phase, where the rise and fall times are releated to the system capacities and coils.

2) Voltages below $V_{INmin}$ have no Impact to the device reliabiltiy as Long as the times and currents defined in section Pin Reliability in Overload for the affected pad(s) are not violated.

3) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device.

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## 3.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The following table defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels
  - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

*Note: An overload condition on one or more pins does not require a reset.*

**Table 3-2 Overload Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input current on any digital pin during overload condition | $I_{IN}$ | -5 | - | 5 | mA | except LVDS pins |
| | | -15 [1] | - | 15 [1] | mA | except LVDS pins; limited to max. 20 pulses with 1ms pulse length |
| Input current on LVDS pin during overload condition | $I_{INLVDS}$ | -3 | - | 3 | mA | |
| Absolute maximum sum of all input circuit currents during overload condition | $I_{ING}$ | -50 | - | 50 | mA | |
| Input current on analog input pin during overload condition | $I_{INANA}$ | -3 | - | 3 | mA | |
| | | -5 | - | 5 | mA | limited to 60h over lifetime |
| Absolute sum of all ADC inputs during overload condition | $I_{INSCA}$ | -20 | - | 20 | mA | |
| Absolute maximum sum of all input circuit currents during overload condition | $\Sigma I_{INS}$ | -100 | - | 100 | mA | |
| Signal voltage over/undershoot at GPIOs | $V_{OUS}$ | $V_{SS}$ - 2 | - | $V_{EXT/FLEX}$ + 2 | V | limited to 60h over lifetime; Valid for LP, MP, MP+, and MPR pads |
| Inactive device pin current during overload condtion [2] | $I_{ID}$ | -1 | - | 1 | mA | All power supply voltages $V_{DDx}$ = 0 |
| Sum of all inactive device pin currents [2] | $I_{IDS}$ | -100 | - | 100 | mA | |

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**Table 3-2 Overload Parameters** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Overload coupling factor for digital inputs, negative [3] | $K_{OVDN}$ CC | - | $2*10^{-4}$ | $6*10^{-4}$ | | Overload injected on GPIO non LVDS pad and affecting neighbor LP and A2 pads; -2mA < $I_{IN}$ < 0mA |
| | | - | - | $1*10^{-2}$ | | Overload injected on GPIO non LVDS pad and affecting neighbor LP and A2 pads; -5mA < $I_{IN}$ < -2mA |
| | | - | - | $1.7*10^{-3}$ | | Overload injected on GPIO non LVDS pad and affecting neighbor MP, MP+, and MPR pads; -2mA < $I_{IN}$ < 0mA |
| | | - | - | $2*10^{-2}$ | | Overload injected on GPIO non LVDS pad and affecting neighbor MP, MP+, and MPR pads; -5mA < $I_{IN}$ < -2mA |
| | | - | - | 0.3 | | Overload injected on LVDS pad and affecting neighbor LVDS pads |
| | | - | - | 0.93 | | coupling between pads 21.2 and 21.3 |
| Overload coupling factor for digital inputs, positive [3] | $K_{OVDP}$ CC | - | - | $1*10^{-5}$ | | Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pads |
| | | - | - | $1*10^{-4}$ | | Overload injected on GPIO pad and affecting neighbor P32.0 pad |
| | | - | - | $5*10^{-4}$ | | Overload injected on LVDS pad and affecting neighbor LVDS pads |

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**Table 3-2 Overload Parameters** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Overload coupling factor for analog inputs, negative | $K_{OVAN}$ CC | - | - | $6*10^{-4}$ 4) | | Analog Inputs overlaid with class LP pads or pull down diagnostics; -1mA < $I_{IN}$ < 0mA |
| | | - | - | $1*10^{-2}$ | | Analog Inputs overlaid with class LP pads or pull down diagnostics; -5mA < $I_{IN}$ < -1mA |
| | | - | - | $1*10^{-4}$ | | else; -5mA < $I_{IN}$ < 0mA |
| Overload coupling factor for analog inputs, positive | $K_{OVAP}$ CC | - | - | $1*10^{-5}$ | | 5mA < $I_{IN}$ < 0mA |

1) Reduced VADC / DSADC result accuracy and / or GPIO input levels ($V_{IL}$ and $V_{IH}$) can differ from specified parameters.
2) Limitations for time and supply levels specified in this section are not valid for this parameter.
3) Overload is measured as increase of pad leakage caused by injection on neighbor pad.
4) For analogue inputs overlaid with DSADC function the VCM holdbuffer shall be enabled, in case DSADCs are enabled.

*Note: DSADC input pins count as analog pins as they are overlaid with VADC pins.*

**Table 3-3 PN-Junction Characteristics for positive Overload**

| Pad Type | $I_{IN}$ = 3 mA | $I_{IN}$ = 5 mA |
|---|---|---|
| F / A2 | $U_{IN} = V_{DDP3}$ + 0.5 V | $U_{IN} = V_{DDP3}$ + 0.6 V |
| LP / MP / MP+ / MPR | $U_{IN} = V_{EXT\,/\,FLEX}$ + 0.75 V | $U_{IN} = V_{EXT\,/\,FLEX}$ + 0.8 V |
| LVDSM | $U_{IN} = V_{EXT}$ + 0.75 V | - |
| LVDSH | $U_{IN} = V_{DDP3}$ + 0.5 V | - |
| D | $U_{IN} = V_{DDM}$ + 0.75 V | - |

**Table 3-4 PN-Junction Characteristics for negative Overload**

| Pad Type | $I_{IN}$ = -3 mA | $I_{IN}$ = -5 mA |
|---|---|---|
| F / A2 | $U_{IN} = V_{SS}$ - 0.5 V | $U_{IN} = V_{SS}$ - 0.6 V |
| LP / MP / MP+ / MPR | $U_{IN} = V_{SS}$ - 0.75 V | $U_{IN} = V_{SS}$ - 0.8 V |
| LVDSM | $U_{IN} = V_{SS}$ - 0.75 V | - |
| LVDSH | $U_{IN} = V_{SS}$ - 0.5 V | - |
| D | $U_{IN} = V_{SS}$ - 0.75 V | - |

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## 3.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC270 / TC275 / TC277. All parameters specified in the following tables refer to these operating conditions, unless otherwise noticed.

Digital supply voltages applied to the TC270 / TC275 / TC277 must be static regulated voltages.

All parameters specified in the following tables refer to these operating conditions (see table below), unless otherwise noticed in the Note / Test Condition column.

**Table 3-5 Operating Conditions**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SRI frequency | $f_{SRI}$ SR | - | - | 200 | MHz | |
| Max System Frequency | $f_{MAX}$ SR | - | - | 200 | MHz | |
| CPU0 Frequency | $f_{CPU0}$ SR | - | - | 200 | MHz | |
| CPU1 Frequency | $f_{CPU1}$ SR | - | - | 200 | MHz | |
| CPU2 Frequency | $f_{CPU2}$ SR | - | - | 200 | MHz | |
| PLL output frequency | $f_{PLL}$ SR | 20 | - | 200 | MHz | |
| PLL_ERAY output frequency | $f_{PLLERAY}$ SR | 20 | - | 400 | MHz | |
| SPB frequency | $f_{SPB}$ SR | - | - | 100 | MHz | |
| ASCLIN fast frequency | $f_{ASCLINF}$ SR | - | - | 200 | MHz | |
| ASCLIN slow frequency | $f_{ASCLINS}$ SR | - | - | 100 | MHz | |
| Baud2 frequency | $f_{BAUD2}$ SR | - | - | 200 | MHz | |
| Baud1 frequency | $f_{BAUD1}$ SR | - | - | 100 | MHz | |
| FSI2 frequency | $f_{FSI2}$ SR | - | - | 200 | MHz | |
| FSI frequency | $f_{FSI}$ SR | - | - | 100 | MHz | |
| GTM frequency | $f_{GTM}$ SR | - | - | 100 | MHz | |
| STM frequency | $f_{STM}$ SR | - | - | 100 | MHz | |
| ERAY frequency | $f_{ERAY}$ SR | - | - | 80 | MHz | |
| BBB frequency | $f_{BBB}$ SR | - | - | 100 | MHz | |
| MultiCAN frequency | $f_{CAN}$ SR | - | - | 100 | MHz | |
| Absolute sum of short circuit currents of the device | $\Sigma I_{SC_D}$ SR | - | - | 100 | mA | |
| Ambient Temperature | $T_A$ SR | -40 | - | 125 | °C | valid for all SAK products |
| | | -40 | - | 150 | °C | valid for all SAL products |
| | | -40 | - | 170 | °C | valid for all SAL products without package |
| Junction Temperature | $T_J$ SR | -40 | - | 150 | °C | valid for all SAK products |
| | | -40 | - | 170 | °C | valid for all SAL products |

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**Table 3-5 Operating Conditions** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Core Supply Voltage [1] | $V_{DD}$ SR | 1.17 | 1.3 | 1.43 [2] | V | Only required if externally supplied |
| ADC analog supply voltage | $V_{DDM}$ SR | 2.97 | 5.0 | 5.5 [3] | V | |
| Digital external supply voltage for LP, MP, MP+ and LVDSM pads and EVR [4] | $V_{EXT}$ SR | 2.97 | - | 4.5 | V | 3.3V pad parameters are valid |
| | | 4.5 | 5.0 | 5.5 [3] | V | 5V pad parameters are valid |
| Digital supply voltage for Flex port | $V_{FLEX}$ SR | 2.97 | - | 4.5 | V | 3.3V pad parameters are valid |
| | | 4.5 | 5.0 | 5.5 [3] | V | 5V pad parameters are valid |
| Digital supply voltage for LVDSH and A2 pads [5] | $V_{DDP3}$ SR | 2.97 | 3.3 | 3.63 [6] | V | 3.3V pad parameters are valid; only required if externally supplied |
| Flash supply voltage 3.3V [1] | $V_{DDFL3}$ SR | 2.97 | 3.3 | 3.63 | V | Only required if externally supplied |
| Digital ground voltage | $V_{SS}$ SR | 0 | - | - | V | |
| Analog ground voltage for $V_{DDM}$ | $V_{SSM}$ CC | -0.1 | 0 | 0.1 | V | |
| Voltage to ensure defined pad states [7] | $V_{DDPPA}$ CC | 0.72 | - | - | V | A2 and LVDSH |
| | | 1.4 | - | - | V | LP, MP, MP+, MPR and LVDSM |
| Digital external supply voltage for EVR and during Standby mode | $V_{EVRSB}$ SR | 2.97 | - | 5.5 | V | only available in BGA package. $V_{EVRSB}$ is bonded together with $V_{EXT}$ supply pin in LQFP package. |

1) No external inductive load permissible if EVR is used. All $V_{DD}$ pins shall be connected together externally on the PCB.
2) Voltage overshoot to 1.69V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
3) Voltage overshoot to 6.5V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
4) All $V_{EXT}$ pins shall be connected together externally on the PCB.
5) All $V_{DDP3}$ pins shall be connected together externally on the PCB.
6) Voltage overshoot to 4.29V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
7) This parameter is valid under the assumption the PORST signal is constantly at low level during the power-up/power-down of $V_{DDP3}$.

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## 3.5 5 V / 3.3 V switchable Pads

Pad classes LP, MP, MP+, and MPR support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degrade in TTL operation.

**Table 3-6 Standard_Pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pin capacitance (digital inputs/outputs) | $C_{IO}$ CC | - | 6 | 10 | pF | |
| Spike filter always blocked pulse duration | $t_{SF1}$ CC | - | - | 80 | ns | PORST only |
| Spike filter pass-through pulse duration | $t_{SF2}$ CC | 220 | - | - | ns | PORST only |
| PORST pad output current [1] | $I_{PORST}$ CC | 11 | - | - | mA | $V_{EXT}$ = 3.0V; $V_{PORST}$ = 0.9V; $T_J$ = 165°C |
| | | 13 | - | - | mA | $V_{EXT}$ = 4.5V; $V_{PORST}$ = 1.0V |

1) Pull-down with $I_{PORST}$ relevant is always activated when a primary supply monitor detects a violation.

**Table 3-7 Class LP 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 75 | MHz | Hysteresis active |
| | | - | - | 150 | MHz | Hysteresis inactive |
| Input Hysteresis for LP pad [1] | $HYSLP$ CC | 0.09 * $V_{EXT/FLEX}$ | - | - | V | AL |
| | | 0.075 * $V_{EXT/FLEX}$ | - | - | V | TTL |
| Input Leakage current for LP pad | $I_{OZLP}$ CC | -150 | - | 150 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$) |
| | | -350 | - | 350 | nA | else |
| Input leakage current for P32.0 | $I_{OZP320}$ CC | -4900 | - | 4900 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$) |
| | | -9400 | - | 9400 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$); for $T_J$ > 150°C |
| | | -5800 | - | 5800 | nA | else |
| | | -12000 | - | 12000 | nA | else; for $T_J$ > 150°C |
| Pull-up current for LP pad | $I_{PUHLP}$ CC | \|30\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|43\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|107\| | µA | $V_{ILmax}$; AL and TTL |

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**Table 3-7 Class LP 5V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pull-down current for LP pad | $I_{PDLLP}$ CC | - | - | \|100\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|46\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|21\| | - | - | µA | $V_{ILmax}$; TTL |
| On-Resistance for LP pad, weak driver [2] | $R_{DSONLPW}$ CC | 200 | 620 | 1040 | Ohm | PMOS/NMOS ; $I_{OH}$=0.5mA ; $I_{OL}$=0.5mA |
| On-Resistance for LP pad, medium driver [2] | $R_{DSONLPM}$ CC | 50 | 155 | 260 | Ohm | PMOS/NMOS ; $I_{OH}$=2mA ; $I_{OL}$=2mA |
| Rise / fall time for LP pad [3] | $t_{LP}$ CC | - | - | 95+2.1 * $C_L$ | ns | $C_L$≤50pF ; pin out driver=weak |
| | | - | - | 200+2.9 * ( $C_L$ - 50 ) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=weak |
| | | - | - | 25+0.5 * $C_L$ | ns | $C_L$≤50pF ; pin out driver=medium |
| | | - | - | 50+0.75 * ( $C_L$ - 50 ) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=medium |
| Input high voltage for LP pad | $V_{IHLP}$ SR | (0.73*$V_{EXT/FLEX}$)-0.25 | - | - | V | Hysteresis active, AL |
| | | 2.03 [4] | - | - | V | Hysteresis active, TTL |
| Input low voltage for LP pad | $V_{ILLP}$ SR | - | - | (0.52*$V_{EXT/FLEX}$)-0.25 | V | Hysteresis active, AL |
| | | - | - | 0.8 [5] | V | Hysteresis active, TTL |
| Input low / high voltage for LP pad | $V_{ILHLP}$ CC | 1.85 | - | 3.0 | V | Hysteresis inactive; not available for P14.2, P14.4, and P15.1 |
| Pad set-up time for LP pad | $t_{SET_LP}$ CC | - | - | 100 | ns | |
| Input leakage current for P02.1 | $I_{OZ021}$ CC | -150 | - | 1030 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$); $T_J$ > 150°C |
| | | -150 | - | 340 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$); $T_J$ = 150°C |
| | | -420 | - | 1100 | nA | else; $T_J$ > 150°C |
| | | -350 | - | 380 | nA | else; $T_J$ = 150°C |
| Pull down current for P32_0 pin | $I_{PDLP320}$ CC | - | - | \|105\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|41\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|16\| | - | - | µA | $V_{ILmax}$; TTL |

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**Table 3-7 Class LP 5V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pull Up Current for P32_0 pin | $I_{PUHP320}$ CC | \|25\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|38\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|112\| | µA | $V_{ILmax}$; AL and TTL |
| Short Circuit current for LP pad 6) | $I_{SC}$ SR | -10 | - | 10 | mA | absolute max value (PSI5) |
| Deviation of symmetry for rising and falling edges | $SYM$ CC | - | - | 20 | % | |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.
3) Rise / fall times are defined 10% - 90% of $V_{EXT/FLEX}$.
4) $V_{IHx}$ = 0.27 * $V_{EXT/FLEX}$ + 0.545V
5) $V_{ILx}$ = 0.17 * $V_{EXT/FLEX}$
6) The values are only valid if the pad is not used during operation, otherwise $I_{SC}$ defines the limits for operation.

**Table 3-8 Class LP 3.3V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 50 | MHz | Hysteresis active |
| | | - | - | 100 | MHz | Hysteresis inactive |
| Input Hysteresis for LP pad 1) | $HYSLP$ CC | 0.05 * $V_{EXT/FLEX}$ | - | - | V | AL and TTL |
| Input Leakage current for LP pad | $I_{OZLP}$ CC | -150 | - | 150 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$) |
| | | -350 | - | 350 | nA | else |
| Input leakage current for P32.0 | $I_{OZP320}$ CC | -4900 | - | 4900 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$) |
| | | -9400 | - | 9400 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$); for $T_J$ > 150 °C |
| | | -5800 | - | 5900 | nA | else |
| | | -12000 | - | 12000 | nA | else; for $T_J$ > 150°C |
| Pull-up current for LP pad | $I_{PUHLP}$ CC | \|17\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|19\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|75\| | µA | $V_{ILmax}$; AL and TTL |
| Pull-down current for LP pad | $I_{PDLLP}$ CC | - | - | \|75\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|22\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|11\| | - | - | µA | $V_{ILmax}$; TTL |
| On-Resistance for LP pad, weak driver 2) | $R_{DSONLPW}$ CC | 250 | 875 | 1500 | Ohm | ; NMOS/PMOS ; $I_{OH}$=0.25mA ; $I_{OL}$=0.25mA |

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**Table 3-8 Class LP 3.3V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| On-Resistance for LP pad, medium driver [2] | $R_{DSONLPM}$ CC | 70 | 235 | 400 | Ohm | ; NMOS/PMOS ; $I_{OH}$=1mA ; $I_{OL}$=1mA |
| Rise / fall time for LP pad [3] | $t_{LP}$ CC | - | - | 150+3.4 * $C_L$ | ns | $C_L$≤50pF ; pin out driver=weak |
| | | - | - | 320+4.5 * ( $C_L$ - 50 ) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=weak |
| | | - | - | 30+0.8*$C_L$ | ns | $C_L$≤50pF ; pin out driver=medium |
| | | - | - | 70+1.1 * ( $C_L$ - 50 ) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=medium |
| Input high voltage for LP pad | $V_{IHLP}$ SR | (0.73*$V_{EXT/FLEX}$)-0.25 | - | - | V | Hysteresis active, AL |
| | | 1.6 [4] | - | - | V | Hysteresis active, TTL |
| Input low voltage for LP pad | $V_{ILLP}$ SR | - | - | (0.52*$V_{EXT/FLEX}$)-0.25 | V | Hysteresis active, AL |
| | | - | - | 0.5 [5] | V | Hysteresis active, TTL |
| Input low / high voltage for LP pad | $V_{ILHLP}$ CC | 1.1 | - | 1.9 | V | Hysteresis inactive; not available for P14.2, P14.4, and P15.1 |
| Pad set-up time for LP pad | $t_{SET_LP}$ CC | - | - | 100 | ns | |
| Input leakage current for P02.1 | $I_{OZ021}$ CC | -150 | - | 920 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$); $T_J$ > 150°C |
| | | -150 | - | 330 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$); $T_J$ = 150°C |
| | | -360 | - | 1000 | nA | else; $T_J$ > 150°C |
| | | -350 | - | 375 | nA | else; $T_J$ = 150°C |
| Pull down current for P32_0 pin | $I_{PDLP320}$ CC | - | - | \|80\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|17\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|6\| | - | - | µA | $V_{ILmax}$; TTL |
| Pull Up Current for P32_0 pin | $I_{PUHP320}$ CC | \|12\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|14\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|80\| | µA | $V_{ILmax}$; AL and TTL |
| Short Circuit current for LP pad [6] | $I_{SC}$ SR | -10 | - | 10 | mA | absolute max value (PSI5) |
| Deviation of symmetry for rising and falling edges | $SYM$ CC | - | - | 20 | % | |

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1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.
3) Rise / fall times are defined 10% - 90% of $V_{EXT/FLEX}$.
4) $V_{IHx}$ = 0.27 * $V_{EXT/FLEX}$ + 0.545V
5) $V_{ILx}$ = 0.17 * $V_{EXT/FLEX}$
6) The values are only valid if the pad is not used during operation, otherwise $I_{SC}$ defines the limits for operation.

**Table 3-9 Class MP 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 75 | MHz | Hysteresis active |
| | | - | - | 150 | MHz | Hysteresis inactive |
| Input Hysteresis for MP pad [1] | $HYSMP$ CC | 0.09 * $V_{EXT/FLEX}$ | - | - | V | AL |
| | | 0.075 * $V_{EXT/FLEX}$ | - | - | V | TTL |
| Input Leakage current for MP pad | $I_{OZMP}$ CC | -500 | - | 500 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$) |
| | | -1000 | - | 1000 | nA | else |
| Pull-up current for MP pad | $I_{PUHMP}$ CC | \|30\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|43\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|107\| | µA | $V_{ILmax}$; AL and TTL |
| Pull-down current for MP pad | $I_{PDLMP}$ CC | - | - | \|100\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|46\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|21\| | - | - | µA | $V_{ILmax}$; TTL |
| On-Resistance for MP pad, weak driver [2] | $R_{DSONMPW}$ CC | 200 | 620 | 1040 | Ohm | PMOS/NMOS ; $I_{OH}$=0.5mA ; $I_{OL}$=0.5mA |
| On-Resistance for MP pad, medium driver [2] | $R_{DSONMPM}$ CC | 50 | 155 | 260 | Ohm | PMOS/NMOS ; $I_{OH}$=2mA ; $I_{OL}$=2mA |
| On-Resistance for MP pad, strong driver [2] | $R_{DSONMPS}$ CC | 20 | 75 | 130 | Ohm | PMOS/NMOS ; $I_{OH}$=8mA ; $I_{OL}$=8mA |

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**Table 3-9 Class MP 5V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Rise / fall time for MP pad [3] | $t_{MP}$ CC | - | - | 95+2.1*$C_L$ | ns | $C_L$≤50pF ; pin out driver=weak |
| | | - | - | 200+2.9*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=weak |
| | | - | - | 25+0.5*$C_L$ | ns | $C_L$≤50pF ; pin out driver=medium |
| | | - | - | 50 + 0.75 * ( CL - 50 ) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=medium |
| | | - | - | 17.5+0.25 *$C_L$ | ns | $C_L$≤50pF ; edge=medium ; pin out driver=strong |
| | | - | - | 30+0.3*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=medium ; pin out driver=strong |
| | | - | - | 7+0.2*$C_L$ | ns | $C_L$≤50pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 17+0.3*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=sharp ; pin out driver=strong |
| Input high voltage for MP pad | $V_{IHMP}$ SR | (0.73*$V_{EXT/FLEX}$)-0.25 | - | - | V | Hysteresis active, AL |
| | | 2.03 [4] | - | - | V | Hysteresis active, TTL |
| Input low voltage for MP pad | $V_{ILMP}$ SR | - | - | (0.52*$V_{EXT/FLEX}$)-0.25 | V | Hysteresis active, AL |
| | | - | - | 0.8 [5] | V | Hysteresis active, TTL |
| Input low / high voltage for MP pad | $V_{ILHMP}$ CC | 1.85 | - | 3.0 | V | Hysteresis inactive |
| Pad set-up time for MP pad | $t_{SET_MP}$ CC | - | - | 100 | ns | |
| Short Circuit current for MP pad [6] | $I_{SC}$ SR | -10 | - | 10 | mA | absolute max value (PSI5) |
| Deviation of symmetry for rising and falling edges | $SYM$ CC | - | - | 20 | % | |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.
3) Rise / fall times are defined 10% - 90% of $V_{EXT/FLEX}$.
4) $V_{IHx}$ = 0.27 * $V_{EXT/FLEX}$ + 0.545V
5) $V_{ILx}$ = 0.17 * $V_{EXT/FLEX}$
6) The values are only valid if the pad is not used during operation, otherwise $I_{SC}$ defines the limits for operation.

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**Table 3-10 Class MP 3.3V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 50 | MHz | Hysteresis active |
| | | - | - | 100 | MHz | Hysteresis inactive |
| Input Hysteresis for MP pad [1] | $HYSMP$ CC | 0.05 * $V_{EXT/FLEX}$ | - | - | V | AL and TTL |
| Input Leakage current for MP pad | $I_{OZMP}$ CC | -500 | - | 500 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$) |
| | | -1000 | - | 1000 | nA | else |
| Pull-up current for MP pad | $I_{PUHMP}$ CC | \|17\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|19\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|75\| | µA | $V_{ILmax}$; AL and TTL |
| Pull-down current for MP pad | $I_{PDLMP}$ CC | - | - | \|75\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|22\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|11\| | - | - | µA | $V_{ILmax}$; TTL |
| On-Resistance for MP pad, weak driver [2] | $R_{DSONMPW}$ CC | 250 | 875 | 1500 | Ohm | ; NMOS/PMOS ; $I_{OH}$=0.25mA ; $I_{OL}$=0.25mA |
| On-Resistance for MP pad, medium driver [2] | $R_{DSONMPM}$ CC | 70 | 235 | 400 | Ohm | ; NMOS/PMOS ; $I_{OH}$=1mA ; $I_{OL}$=1mA |
| On-Resistance for MP pad, strong driver [2] | $R_{DSONMPS}$ CC | 20 | 110 | 200 | Ohm | PMOS/NMOS ; $I_{OH}$=4mA ; $I_{OL}$=4mA |
| Rise / fall time for MP pad [3] | $t_{MP}$ CC | - | - | 150+3.4* $C_L$ | ns | $C_L$≤50pF ; pin out driver=weak |
| | | - | - | 320+4.5*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=weak |
| | | - | - | 30+0.8*$C_L$ | ns | $C_L$≤50pF ; pin out driver=medium |
| | | - | - | 70+1.1*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=medium |
| | | - | - | 32.5+0.35 *$C_L$ | ns | $C_L$≤50pF ; edge=medium ; pin out driver=strong |
| | | - | - | 50+0.45*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=medium ; pin out driver=strong |
| | | - | - | 14.5+0.35 *$C_L$ | ns | $C_L$≤50pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 32+0.5*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=sharp ; pin out driver=strong |

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**Table 3-10 Class MP 3.3V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input high voltage for MP pad | $V_{IHMP}$ SR | (0.73*$V_{EXT/FLEX}$)-0.25 | - | - | V | Hysteresis active, AL |
| | | 1.6 [4] | - | - | V | Hysteresis active, TTL |
| Input low voltage for MP pad | $V_{ILMP}$ SR | - | - | (0.52*$V_{EXT/FLEX}$)-0.25 | V | Hysteresis active, AL |
| | | - | - | 0.5 [5] | V | Hysteresis active, TTL |
| Input low / high voltage for MP pad | $V_{ILHMP}$ CC | 1.1 | - | 1.9 | V | Hysteresis inactive |
| Pad set-up time for MP pad | $t_{SET_MP}$ CC | - | - | 100 | ns | |
| Short Circuit current for MP pad [6] | $I_{SC}$ SR | -10 | - | 10 | mA | absolute max value (PSI5) |
| Deviation of symmetry for rising and falling edges | $SYM$ CC | - | - | 20 | % | |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.
3) Rise / fall times are defined 10% - 90% of $V_{EXT/FLEX}$.
4) $V_{IHx}$ = 0.27 * $V_{EXT/FLEX}$ + 0.545V
5) $V_{ILx}$ = 0.17 * $V_{EXT/FLEX}$
6) The values are only valid if the pad is not used during operation, otherwise $I_{SC}$ defines the limits for operation.

**Table 3-11 Class MP+ 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 75 | MHz | Hysteresis active |
| | | - | - | 150 | MHz | Hysteresis inactive |
| Input hysteresis for MP+ pad [1] | $HYSMPP$ CC | 0.09 * $V_{EXT/FLEX}$ | - | - | V | AL |
| | | 0.075 * $V_{EXT/FLEX}$ | - | - | V | TTL |
| Input leakage current for MP+ pad | $I_{OZMPP}$ CC | -750 | - | 750 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$) |
| | | -1500 | - | 1500 | nA | else |
| Pull-up current for MP+ pad | $I_{PUHMPP}$ CC | \|30\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|43\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|107\| | µA | $V_{ILmax}$; AL and TTL |
| Pull-down current for MP+ pad | $I_{PDLMPP}$ CC | - | - | \|100\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|46\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|21\| | - | - | µA | $V_{ILmax}$; TTL |

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**Table 3-11 Class MP+ 5V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| On-resistance for MP+ pad, weak driver [2] | $R_{DSONMPPW}$ CC | 200 | 620 | 1040 | Ohm | PMOS/NMOS ; $I_{OH}$=0.5mA ; $I_{OL}$=0.5mA |
| On-resistance for MP+ pad, medium driver [2] | $R_{DSONMPPM}$ CC | 50 | 155 | 260 | Ohm | PMOS/NMOS ; $I_{OH}$=2mA ; $I_{OL}$=2mA |
| On-resistance for MP+ pad, strong driver [2] | $R_{DSONMPPS}$ CC | 20 | 55 | 90 | Ohm | PMOS/NMOS ; $I_{OH}$=8mA ; $I_{OL}$=8mA |
| Rise/fall time for MP+ pad [3] | $t_{MPP}$ CC | - | - | 95+2.1*$C_L$ | ns | $C_L$≤50pF ; pin out driver=weak |
| | | - | - | 200+2.9*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=weak |
| | | - | - | 25+0.5*$C_L$ | ns | $C_L$≤50pF ; pin out driver=medium |
| | | - | - | 50+0.75*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=medium |
| | | - | - | 9+0.16*$C_L$ | ns | $C_L$≤50pF ; edge=medium ; pin out driver=strong |
| | | - | - | 17+0.2*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=medium ; pin out driver=strong |
| | | - | - | 4+0.16*$C_L$ | ns | $C_L$≤50pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 12+0.21*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 5 | ns | from 0.8V to 2.0V (RMII) ; $C_L$=25pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 4.5 | ns | $C_L$=15pF ; edge=sharp ; pin out driver=strong |
| Input high voltage for MP+ pad | $V_{IHMPP}$ SR | (0.73*$V_{EXT/FLEX}$)-0.25 | - | - | V | Hysteresis active, AL |
| | | 2.03 [4] | - | - | V | Hysteresis active, TTL |
| Input low voltage for MP+ pad | $V_{ILMPP}$ SR | - | - | (0.52*$V_{EXT/FLEX}$)-0.25 | V | Hysteresis active, AL |
| | | - | - | 0.8 [5] | V | Hysteresis active, TTL |
| Input low / high voltage for MP+ pad | $V_{ILHMPP}$ CC | 1.85 | - | 3.0 | V | Hysteresis inactive |

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**Table 3-11 Class MP+ 5V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pad set-up time for MP+ pad | $t_{SET_MPP}$ CC | - | - | 100 | ns | |
| Short circuit current for MP+ pad 6) | $I_{SCMPP}$ SR | -10 | - | 10 | mA | absolute max value (PSI5) |
| Deviation of symmetry for rising and falling edges | $SYM$ CC | - | - | 20 | % | |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.
3) Rise / fall times are defined 10% - 90% of $V_{EXT/FLEX}$.
4) $V_{IHx}$ = 0.27 * $V_{EXT/FLEX}$ + 0.545V
5) $V_{ILx}$ = 0.17 * $V_{EXT/FLEX}$
6) The values are only valid if the pad is not used during operation, otherwise $I_{SC}$ defines the limits for operation.

**Table 3-12 Class MP+ 3.3V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 50 | MHz | Hysteresis active |
| | | - | - | 100 | MHz | Hysteresis inactive |
| Input hysteresis for MP+ pad 1) | $HYSMPP$ CC | 0.05 * $V_{EXT/FLEX}$ | - | - | V | AL and TTL |
| Input leakage current for MP+ pad | $I_{OZMPP}$ CC | -750 | - | 750 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$) |
| | | -1500 | - | 1500 | nA | else |
| Pull-up current for MP+ pad | $I_{PUHMPP}$ CC | \|17\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|19\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|75\| | µA | $V_{ILmax}$; AL and TTL |
| Pull-down current for MP+ pad | $I_{PDLMPP}$ CC | - | - | \|75\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|22\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|11\| | - | - | µA | $V_{ILmax}$; TTL |
| On-resistance for MP+ pad, weak driver 2) | $R_{DSONMPPW}$ CC | 250 | 875 | 1500 | Ohm | ; NMOS/PMOS ; $I_{OH}$=0.25mA ; $I_{OL}$=0.25mA |
| On-resistance for MP+ pad, medium driver 2) | $R_{DSONMPPM}$ CC | 70 | 235 | 400 | Ohm | ; NMOS/PMOS ; $I_{OH}$=1mA ; $I_{OL}$=1mA |
| On-resistance for MP+ pad, strong driver 2) | $R_{DSONMPPS}$ CC | 20 | 75 | 130 | Ohm | PMOS/NMOS ; $I_{OH}$=4mA ; $I_{OL}$=4mA |

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**Table 3-12 Class MP+ 3.3V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Rise/fall time for MP+ pad [3] | $t_{MPP}$ CC | - | - | 150+3.4* $C_L$ | ns | $C_L$≤50pF ; pin out driver=weak |
| | | - | - | 320+4.5*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=weak |
| | | - | - | 30+0.8*$C_L$ | ns | $C_L$≤50pF ; pin out driver=medium |
| | | - | - | 70+1.1*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=medium |
| | | - | - | 20+0.2*$C_L$ | ns | $C_L$≤50pF ; edge=medium ; pin out driver=strong |
| | | - | - | 30+0.3*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=medium ; pin out driver=strong |
| | | - | - | 13+0.2*$C_L$ | ns | $C_L$≤50pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 23+0.3*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 5 | ns | from 0.8V to 2.0V (RMII) ; $C_L$=25pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 4.5 | ns | from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$; $C_L$=15pF ; edge=sharp ; pin out driver=strong |
| Input high voltage for MP+ pad | $V_{IHMPP}$ SR | (0.73*$V_{EXT/FLEX}$)-0.25 | - | - | V | Hysteresis active, AL |
| | | 1.6 [4] | - | - | V | Hysteresis active, TTL |
| Input low voltage for MP+ pad | $V_{ILMPP}$ SR | - | - | (0.52*$V_{EXT/FLEX}$)-0.25 | V | Hysteresis active, AL |
| | | - | - | 0.5 [5] | V | Hysteresis active, TTL |
| Input low / high voltage for MP+ pad | $V_{ILHMPP}$ CC | 1.1 | - | 1.9 | V | Hysteresis inactive |
| Pad set-up time for MP+ pad | $t_{SET_MPP}$ CC | - | - | 100 | ns | |
| Short circuit current for MP+ pad [6] | $I_{SCMPP}$ SR | -10 | - | 10 | mA | absolute max value (PSI5) |
| Deviation of symmetry for rising and falling edges | $SYM$ CC | - | - | 20 | % | |

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1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.
3) Rise / fall times are defined 10% - 90% of $V_{EXT/FLEX}$.
4) $V_{IHx}$ = 0.27 * $V_{EXT/FLEX}$ + 0.545V
5) $V_{ILx}$ = 0.17 * $V_{EXT/FLEX}$
6) The values are only valid if the pad is not used during operation, otherwise $I_{SC}$ defines the limits for operation.

**Table 3-13 Class MPR 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 75 | MHz | Hysteresis active |
| | | - | - | 150 | MHz | Hysteresis inactive |
| Input Hysteresis for MPR pads [1] | $HYSMPR$ CC | 0.09 * $V_{EXT/FLEX}$ | - | - | V | AL |
| | | 0.075* $V_{EXT/FLEX}$ | - | - | V | TTL |
| Input leakage current class MPR | $I_{OZMPR}$ CC | -750 | - | 750 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$) |
| | | -1500 | - | 1500 | nA | else |
| Pull-up current | $I_{PUHMPR}$ CC | \|30\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|43\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|107\| | µA | $V_{ILmax}$; AL and TTL |
| Pull-down current | $I_{PDLMPR}$ CC | - | - | \|100\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|46\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|21\| | - | - | µA | $V_{ILmax}$; TTL |
| On-resistance of the MPR pad, weak driver [2] | $R_{DSONMPRW}$ CC | 200 | 620 | 1040 | Ohm | PMOS/NMOS ; $I_{OH}$=0.5mA ; $I_{OL}$=0.5mA |
| On-resistance of the MPR pad, medium driver [2] | $R_{DSONMPRM}$ CC | 50 | 155 | 260 | Ohm | PMOS/NMOS ; $I_{OH}$=2mA ; $I_{OL}$=2mA |
| On-resistance of the MPR pad, strong driver [2] | $R_{DSONMPRS}$ CC | 20 | 55 | 90 | Ohm | PMOS/NMOS ; $I_{OH}$=8mA ; $I_{OL}$=8mA |

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**Table 3-13 Class MPR 5V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Rise/fall time [3] | $t_{MPR}$ CC | - | - | 95+2.1*$C_L$ | ns | $C_L$≤50pF ; pin out driver=weak |
| | | - | - | 200+2.9*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=weak |
| | | - | - | 25+0.5*$C_L$ | ns | $C_L$≤50pF ; pin out driver=medium |
| | | - | - | 50+0.75*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=medium |
| | | - | - | 9+0.16*$C_L$ | ns | $C_L$≥0pF ; $C_L$≤50pF ; edge=medium ; pin out driver=strong |
| | | - | - | 17+0.2*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=medium ; pin out driver=strong |
| | | - | - | 4+0.16*$C_L$ | ns | $C_L$≤50pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 12+0.21*($C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 5 | ns | from 0.8V to 2.0V (RMII) ; $C_L$=25pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 4.5 | ns | from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$; $C_L$=15pF ; edge=sharp ; pin out driver=strong |
| Input high voltage, class MPR pads | $V_{IHMPR}$ SR | (0.73*$V_{EXT/FLEX}$)-0.25 | - | - | V | Hysteresis active, AL |
| | | 2.03 [4] | - | - | V | Hysteresis active, TTL |
| Input low voltage, class MPR pads | $V_{ILMPR}$ SR | - | - | (0.52*$V_{EXT/FLEX}$)-0.25 | V | Hysteresis active, AL |
| | | - | - | 0.8 [5] | V | Hysteresis active, TTL |
| Input low / high voltage, class MPR pads | $V_{ILHMPR}$ SR | 1.2 | - | 2.3 | V | Hysteresis inactive |
| Pad set-up time | $t_{SET_MPR}$ CC | - | - | 100 | ns | |
| Short circuit current Class MPR | $I_{SC}$ SR | -10 | - | 10 | mA | absolute max value (PSI5) |
| Deviation of symmetry for rising and falling edges | $SYM$ CC | - | - | 20 | % | |

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1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.
3) Rise / fall times are defined 10% - 90% of $V_{EXT/FLEX}$.
4) $V_{IHx}$ = 0.27 * $V_{EXT/FLEX}$ + 0.545V
5) $V_{ILx}$ = 0.17 * $V_{EXT/FLEX}$

**Table 3-14 Class MPR 3.3V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 50 | MHz | Hysteresis active |
| | | - | - | 100 | MHz | Hysteresis inactive |
| Input Hysteresis for MPR pads 1) | $HYSMPR$ CC | 0.05 * $V_{EXT/FLEX}$ | - | - | V | AL and TTL |
| Input leakage current class MPR | $I_{OZMPR}$ CC | -750 | - | 750 | nA | (0.1*$V_{EXT/FLEX}$) < $V_{IN}$ < (0.9*$V_{EXT/FLEX}$) |
| | | -1500 | - | 1500 | nA | else |
| Pull-up current | $I_{PUHMPR}$ CC | \|17\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|19\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|75\| | µA | $V_{ILmax}$; AL and TTL |
| Pull-down current | $I_{PDLMPR}$ CC | - | - | \|75\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|22\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|11\| | - | - | µA | $V_{ILmax}$; TTL |
| On-resistance of the MPR pad, weak driver 2) | $R_{DSONMPRW}$ CC | 250 | 875 | 1500 | Ohm | ; NMOS/PMOS ; $I_{OH}$=0.25mA ; $I_{OL}$=0.25mA |
| On-resistance of the MPR pad, medium driver 2) | $R_{DSONMPRM}$ CC | 70 | 235 | 400 | Ohm | ; NMOS/PMOS ; $I_{OH}$=1mA ; $I_{OL}$=1mA |
| On-resistance of the MPR pad, strong driver 2) | $R_{DSONMPRS}$ CC | 20 | 75 | 130 | Ohm | PMOS/NMOS ; $I_{OH}$=4mA ; $I_{OL}$=4mA |

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**Table 3-14 Class MPR 3.3V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Rise/fall time [3] | $t_{MPR}$ CC | - | - | 150+3.4* $C_L$ | ns | $C_L$≤50pF ; pin out driver=weak |
| | | - | - | 320+4.5*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=weak |
| | | - | - | 30+0.8*$C_L$ | ns | $C_L$≤50pF ; pin out driver=medium |
| | | - | - | 70+1.1*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=medium |
| | | - | - | 20+0.2*$C_L$ | ns | $C_L$≥0pF ; $C_L$≤50pF ; edge=medium ; pin out driver=strong |
| | | - | - | 30+0.3*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=medium ; pin out driver=strong |
| | | - | - | 13+0.2*$C_L$ | ns | $C_L$≤50pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 23+0.3*( $C_L$-50) | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 5 | ns | from 0.8V to 2.0V (RMII) ; $C_L$=25pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 4.5 | ns | from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$; $C_L$=15pF ; edge=sharp ; pin out driver=strong |
| Input high voltage, class MPR pads | $V_{IHMPR}$ SR | (0.73*$V_{EXT/FLEX}$)-0.25 | - | - | V | Hysteresis active, AL |
| | | 1.6 [4] | - | - | V | Hysteresis active, TTL |
| Input low voltage, class MPR pads | $V_{ILMPR}$ SR | - | - | (0.52*$V_{EXT/FLEX}$)-0.25 | V | Hysteresis active, AL |
| | | - | - | 0.5 [5] | V | Hysteresis active, TTL |
| Input low / high voltage, class MPR pads | $V_{ILHMPR}$ SR | 0.8 | - | 1.7 | V | Hysteresis inactive |
| Pad set-up time | $t_{SET_MPR}$ CC | - | - | 100 | ns | |
| Short circuit current Class MPR | $I_{SC}$ SR | -10 | - | 10 | mA | absolute max value (PSI5) |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.

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3) Rise / fall times are defined 10% - 90% of $V_{EXT/FLEX}$.
4) $V_{IHx}$ = 0.27 * $V_{EXT/FLEX}$ + 0.545V
5) $V_{ILx}$ = 0.17 * $V_{EXT/FLEX}$

**Table 3-15 Class S**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 75 | MHz | Hysteresis active |
| | | - | - | 150 | MHz | Hysteresis inactive |
| Input Hysteresis for S pad [1] | *HYSS* CC | 0.3 | - | - | V | |
| Pull-up current for S pad | $I_{PUHS}$ CC | \|30\| | - | - | µA | $V_{IHmin}$ |
| | | - | - | \|107\| | µA | $V_{ILmax}$ |
| Pull-down current for S pad | $I_{PDLS}$ CC | - | - | \|100\| | µA | $V_{IHmin}$ |
| | | \|46\| | - | - | µA | $V_{ILmax}$ |
| Input Leakage current Class S | $I_{OZS}$ CC | -350 | - | 350 | nA | Analog Inputs with pull down diagnostics |
| | | -150 | - | 150 | nA | else |
| Input voltage high for S pad | $V_{IHS}$ SR | - | - | (0.73*$V_{DDM}$)-0.25 | V | Hysteresis active |
| Input voltage low for S pad | $V_{ILS}$ SR | (0.52*$V_{DDM}$)-0.25 | - | - | V | Hysteresis active |
| Input low threshold variation for S pad [2] | $V_{ILSD}$ SR | -50 | - | 50 | mV | max. variation of 1ms; $V_{DDM}$=constant |
| Input capacitance for S pad | $C_{INS}$ CC | - | - | 10 | pF | |
| Pad set-up time for S pad | $t_{SETS}$ CC | - | - | 100 | ns | |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) VILSD is implemented to ensure J2716 specification. For details of dedicated pins please see AP32286 for details.

**Table 3-16 Class I 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 75 | MHz | Hysteresis active |
| | | - | - | 150 | MHz | Hysteresis inactive |
| Input Hysteresis for I pad [1] | *HYSI* CC | 0.07 * $V_{EXT/FLEX}$ | - | - | V | $\overline{\text{PORST}}$ pad only |
| | | 0.09 * $V_{EXT/FLEX}$ | - | - | V | AL |
| | | 0.075 * $V_{EXT/FLEX}$ | - | - | V | TTL |
| Pull-up current for I pad | $I_{PUHI}$ CC | \|30\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|43\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|107\| | µA | $V_{ILmax}$; AL and TTL |

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**Table 3-16 Class I 5V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pull-down current for I pad | $I_{PDLI}$ CC | - | - | \|100\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|46\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|21\| | - | - | µA | $V_{ILmax}$; TTL |
| Input Leakage Current for I pad | $I_{OZI}$ CC | -150 | - | 150 | nA | $(0.1*V_{EXT/FLEX}) < V_{IN} < (0.9*V_{EXT/FLEX})$ |
| | | -350 | - | 350 | nA | else |
| Input high voltage for I pad | $V_{IHI}$ SR | 2.03 [2] | - | - | V | Hysteresis active, TTL |
| | | $(0.73*V_{EXT/FLEX})$-0.25 | - | - | V | Hysteresis active; AL; not available for the $\overline{\text{PORST}}$ pad |
| Input low voltage for I pad | $V_{ILI}$ SR | - | - | 0.8 [3] | V | Hysteresis active, TTL |
| | | - | - | $(0.52*V_{EXT/FLEX})$-0.25 | V | Hysteresis active; AL; not available for the $\overline{\text{PORST}}$ pad |
| Input low / high voltage for I pad | $V_{ILHI}$ CC | 1.85 | - | 3.0 | V | Hysteresis inactive |
| Pad set-up time for I pad | $t_{SETI}$ CC | - | - | 100 | ns | |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) $V_{IHx}$ = 0.27 * $V_{EXT/FLEX}$ + 0.545V
3) $V_{ILx}$ = 0.17 * $V_{EXT/FLEX}$

**Table 3-17 Class I 3.3V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 50 | MHz | Hysteresis active |
| | | - | - | 100 | MHz | Hysteresis inactive |
| Input Hysteresis for I pad [1] | *HYSI* CC | 0.045 * $V_{EXT/FLEX}$ | - | - | V | $\overline{\text{PORST}}$ pad only |
| | | 0.05 * $V_{EXT/FLEX}$ | - | - | V | AL and TTL |
| Pull-up current for I pad | $I_{PUHI}$ CC | \|17\| | - | - | µA | $V_{IHmin}$; AL |
| | | \|19\| | - | - | µA | $V_{IHmin}$; TTL |
| | | - | - | \|75\| | µA | $V_{ILmax}$; AL and TTL |
| Pull-down current for I pad | $I_{PDLI}$ CC | - | - | \|75\| | µA | $V_{IHmin}$; AL and TTL |
| | | \|22\| | - | - | µA | $V_{ILmax}$; AL |
| | | \|11\| | - | - | µA | $V_{ILmax}$; TTL |
| Input Leakage Current for I pad | $I_{OZI}$ CC | -150 | - | 150 | nA | $(0.1*V_{EXT/FLEX}) < V_{IN} < (0.9*V_{EXT/FLEX})$ |
| | | -350 | - | 350 | nA | else |

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**Table 3-17 Class I 3.3V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input high voltage for I pad | $V_{IHI}$ SR | 1.6 [2] | - | - | V | Hysteresis active, TTL |
| | | $(0.73*V_{EXT/FLEX})$-0.25 | - | - | V | Hysteresis active; AL; not available for the $\overline{\text{PORST}}$ pad |
| Input low voltage for I pad | $V_{ILI}$ SR | - | - | 0.5 [3] | V | Hysteresis active, TTL |
| | | - | - | $(0.52*V_{EXT/FLEX})$-0.25 | V | Hysteresis active; AL; not available for the $\overline{\text{PORST}}$ pad |
| Input low / high voltage for I pad | $V_{ILHI}$ CC | 1.1 | - | 1.9 | V | Hysteresis inactive |
| Pad set-up time for I pad | $t_{SETI}$ CC | - | - | 100 | ns | |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

2) $V_{IHx} = 0.27 * V_{EXT/FLEX} + 0.545V$

3) $V_{ILx} = 0.17 * V_{EXT/FLEX}$

**Table 3-18 Driver Mode Selection for LP Pads**

| PDx.2 | PDx.1 | PDx.0 | Port Functionality | Driver Setting |
|---|---|---|---|---|
| X | X | 0 | Speed grade 1 | medium (LPm) |
| X | X | 1 | Speed grade 2 | weak (LPw) |

**Table 3-19 Driver Mode Selection for MP / MP+ Pads**

| PDx.2 | PDx.1 | PDx.0 | Port Functionality | Driver Setting |
|---|---|---|---|---|
| X | 0 | 0 | Speed grade 1 | Strong sharp edge (MPss / MP+ss / MPRss) |
| X | 0 | 1 | Speed grade 2 | Strong medium edge (MPsm / MP+sm) |
| X | 1 | 0 | Speed grade 3 | medium (MPm / MP+m / MPRm) |
| X | 1 | 1 | Speed grade 4 | weak (MPw / MP+w / MPRw) |

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## 3.6 3.3 V only Pads

Pad classes LP, MP and MP+ support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degrade in TTL operation.

**Table 3-20 Class A2**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 160 | MHz | |
| Input Hysteresis for A2 pad [1] | $HYSA2$ CC | 0.1 * $V_{DDP3}$ | - | - | V | TTL;else |
| | | 0.06 * $V_{DDP3}$ | - | - | V | valid for P21.6 and P21.7 |
| Input Leakage current for A2 pad | $I_{OZA2}$ CC | -300 | - | 300 | nA | $(0.1*V_{EXT/FLEX}) < V_{IN} < (0.9*V_{EXT/FLEX})$ |
| | | -800 | - | 500 | nA | else |
| Pull-up current for A2 pad | $I_{PUHA2}$ CC | - | - | \|100\| | µA | $V_{IHmin}$ |
| | | \|25\| | - | - | µA | $V_{ILmax}$ |
| Pull-down current for A2 pad | $I_{PDLA2}$ CC | \|23\| | - | - | µA | $V_{IHmin}$ |
| | | - | - | \|100\| | µA | $V_{ILmax}$ |
| On-Resistance for A2 pad, weak driver [2] | $R_{DSONA2W}$ CC | 100 | 200 | 325 | Ohm | PMOS/NMOS ; $I_{OH}$=0.5mA ; $I_{OL}$=0.5mA |
| On-Resistance for A2 pad, medium driver [2] | $R_{DSONA2M}$ CC | 40 | 70 | 100 | Ohm | PMOS/NMOS ; $I_{OH}$=2mA ; $I_{OL}$=2mA |
| On-Resistance for A2 pad, strong driver [2] | $R_{DSONA2S}$ CC | 20 | 35 | 50 | Ohm | PMOS/NMOS ; $I_{OH}$=8mA ; $I_{OL}$=8mA |
| Rise/fall time for A2 pad [3] | $t_{A2}$ CC | - | - | 20+0.8*$C_L$ | ns | $C_L$≤50pF ; pin out driver=weak |
| | | - | - | 17.5+0.85 *$C_L$ | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=weak |
| | | - | - | 12+0.16* $C_L$ | ns | $C_L$≤50pF ; pin out driver=medium |
| | | - | - | 11.5+0.17 *$C_L$ | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=medium |
| | | - | - | 6+0.06*$C_L$ | ns | $C_L$≤50pF ; edge=medium ; pin out driver=strong |
| | | - | - | 5.5+0.07* $C_L$ | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=medium ; pin out driver=strong |
| | | - | - | 0.0+0.12* $C_L$ | ns | $C_L$≤50pF ; edge=sharp ; pin out driver=strong |
| | | - | - | 0.0+0.12* $C_L$ | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=sharp ; pin out driver=strong |

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**Table 3-20 Class A2** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input high voltage for A2 pad | $V_{IHA2}$ SR | 2.04 4) | - | - | V | TTL;valid for all A2 pads except TMS/DAP1, TRST, and TCK/DAP0 |
| | | 0.7 * $V_{DDP3}$ | - | - | V | valid for TMS/DAP1, TRST, and TCK/DAP0 |
| Input low voltage for A2 pad | $V_{ILA2}$ SR | - | - | 0.8 5) | V | TTL;valid for all A2 pads except TMS/DAP1, TRST, and TCK/DAP0 |
| | | - | - | 0.3 * $V_{DDP3}$ | V | valid for TMS/DAP1, TRST, and TCK/DAP0 |
| Pad set-up time for A2 pad | $t_{SETA2}$ CC | - | - | 100 | ns | |
| Deviation of symmetry for rising and falling edges | $SYM$ CC | - | - | 20 | % | |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.
3) Rise / fall times are defined 10% - 90% of $V_{DDP3}$.
4) $V_{IHx}$ = 0.57 * $V_{DDP3}$ - 0.03V
5) $V_{ILx}$ = 0.25 * $V_{DDP3}$ + 0.058V

**Table 3-21 Driver Mode Selection for A2 Pads**

| PDx.2 | PDx.1 | PDx.0 | Port Functionality | Driver Setting |
|---|---|---|---|---|
| X | 0 | 0 | Speed grade 1 | Strong sharp edge |
| X | 0 | 1 | Speed grade 2 | Strong medium edge |
| X | 1 | 0 | Speed grade 3 | medium |
| X | 1 | 1 | Speed grade 4 | weak |

**Table 3-22 Driver Mode Selection for F Pads**

| PDx.2 | PDx.1 | PDx.0 | Port Functionality | Driver Setting |
|---|---|---|---|---|
| X | 0 | 0 | Speed grade 1 | Reduced Strong sharp edge |
| X | 0 | 1 | Speed grade 2 | Reduced Strong medium edge |
| X | 1 | 0 | Speed grade 3 | medium |
| X | 1 | 1 | Speed grade 4 | weak |

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## 3.7 High performance LVDS Pads (LVDSH)

This LVDS pad type is used for the high speed chip to chip communication inferface of the new TC270 / TC275 / TC277. It compose out of a LVDSH pad and a Class F pad.

This pad combination is always supplied by the 3.3V supply rail.

**Table 3-23 Class F**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{IN}$ SR | - | - | 75 | MHz | |
| Input Hysteresis for F pad [1] | $HYSF$ CC | 0.1 * $V_{DDP3}$ | - | - | V | TTL |
| Input Leakage Current for F pad | $I_{OZF}$ CC | -1000 | - | 1000 | nA | (0.1*$V_{DDP3}$) < $V_{IN}$ < (0.9*$V_{DDP3}$); valid for P21.2 and P21.3; $T_J$ = 150°C |
| | | -1500 | - | 1500 | nA | (0.1*$V_{DDP3}$) < $V_{IN}$ < (0.9*$V_{DDP3}$); valid for P21.2 and P21.3; $T_J$ = 170°C |
| | | -300 | - | 300 | nA | (0.1*$V_{DDP3}$) < $V_{IN}$ < (0.9*$V_{DDP3}$); valid for P21.4 and P21.5 |
| | | -2000 | - | 2000 | nA | else; valid for P21.2 and P21.3; $T_J$ = 150°C |
| | | -3000 | - | 3000 | nA | else; valid for P21.2 and P21.3; $T_J$ = 170°C |
| | | -600 | - | 600 | nA | else; valid for P21.4 and P21.5 |
| Pull-up current for F pad | $I_{PUHF}$ CC | \|25\| | - | - | µA | $V_{IHmin}$ |
| | | - | - | \|100\| | µA | $V_{ILmax}$ |
| Pull-down current for class F pads | $I_{PDLF}$ CC | - | - | \|100\| | µA | $V_{IHmin}$ |
| | | \|25\| | - | - | µA | $V_{ILmax}$ |
| On resistance for F pad, weak driver [2] | $R_{DSONFW}$ CC | 100 | 200 | 325 | Ohm | PMOS/NMOS ; $I_{OH}$=0.5mA ; $I_{OL}$=0.5mA |
| On resistance for F pad, medium driver [2] | $R_{DSONFM}$ CC | 40 | 70 | 100 | Ohm | PMOS/NMOS ; $I_{OH}$=2mA ; $I_{OL}$=2mA |
| On resistance for F pad, strong driver [2] | $R_{DSONFS}$ CC | 20 | 50 | 80 | Ohm | PMOS/NMOS ; $I_{OH}$=4mA ; $I_{OL}$=4mA |

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**Table 3-23 Class F** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Rise/fall time for F pad [3] | $t_{rfF}$ CC | - | - | 20+0.8*$C_L$ | ns | $C_L$≤50pF ; pin out driver=weak |
| | | - | - | 17.5+0.85 *$C_L$ | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=weak |
| | | - | - | 12+0.16* $C_L$ | ns | $C_L$≤50pF ; pin out driver=medium |
| | | - | - | 11.5+0.17 *$C_L$ | ns | $C_L$≥50pF ; $C_L$≤200pF ; pin out driver=medium |
| | | - | - | 7+0.16*$C_L$ | ns | $C_L$≤50pF ; edge=medium ; pin out driver=reduced strong |
| | | - | - | 6.5+0.17* $C_L$ | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=meduim ; pin out driver>reduced strong |
| | | - | - | 4+0.16*$C_L$ | ns | $C_L$≤50pF ; edge=sharp ; pin out driver=reduced strong |
| | | - | - | 3.5+0.17* $C_L$ | ns | $C_L$≥50pF ; $C_L$≤200pF ; edge=sharp ; pin out driver=reduced strong |
| Input high voltage for F pad | $V_{IHF}$ SR | 2.04 [4] | - | - | V | TTL |
| Input low voltage for F pad | $V_{ILF}$ SR | - | - | 0.8 [5] | V | TTL |
| Pad set-up time for F pad | $t_{SETF}$ CC | - | - | 100 | ns | |
| Deviation of symmetry for rising and falling edges | $SYM$ CC | - | - | 20 | % | |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.
3) Rise / fall times are defined 10% - 90% of $V_{DDP3}$.
4) $V_{IHx}$ = 0.57 * $V_{DDP3}$ - 0.03V
5) $V_{ILx}$ = 0.25 * $V_{DDP3}$ + 0.058V

$C_L$ = 2.5 pF for all LVDSH parameters.

**Table 3-24 LVDSH - IEEE standard LVDS general purpose link (GPL)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output impedance | $R_0$ CC | 40 | - | 140 | Ohm | Vcm = 1.0 V and 1.4 V |
| Rise time [1] | $t_{rise20}$ CC | - | - | 0.5 | ns | ZL = 100 Ohm ±5% @2 pF |
| Fall time [1] | $t_{fall20}$ CC | - | - | 0.5 | ns | ZL = 100 Ohm ±5% @ 2 pF |
| Output differential voltage | $V_{OD}$ CC | 250 | - | 400 | mV | RT = 100 Ohm ±5% |

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**Table 3-24 LVDSH - IEEE standard LVDS general purpose link (GPL)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage high | $V_{OH}$ CC | - | - | 1475 | mV | RT = 100 Ohm ±5% (400 mV/2) + 1275 mV |
| Output voltage low | $V_{OL}$ CC | 925 | - | - | mV | RT = 100 Ohm ±5% |
| Output offset (Common mode) voltage | $V_{OS}$ CC | 1125 | - | 1275 | mV | RT = 100 Ohm ±5% |
| Input voltage range | $V_I$ SR | 0 | - | 1600 | mV | Driver ground potential difference < 925 mV; RT = 100 Ohm ±10% |
| | | 0 | - | 2000 | mV | Driver ground potential difference < 925 mV; RT = 100 Ohm ±20% |
| Input differential threshold | $V_{idth}$ SR | -100 | - | 100 | mV | Driver ground potential difference < 925 mV |
| Delta output impedance | $dR0$ SR | - | - | 10 | % | Vcm = 1.0 V and 1.4 V (mismatch Pd and Pn) |
| Change in VOS between 0 and 1 | $dVOS$ CC | - | - | 25 | mV | RT = 100 Ohm ±5% |
| Change in Vod between 0 and 1 | $dVod$ CC | - | - | 25 | mV | RT = 100 Ohm ±5% |
| Duty cycle | $t_{duty}$ CC | 45 | - | 55 | % | |

1) Rise / fall times are defined for 20% - 80% of $V_{OD}$

**Table 3-25 LVDSH - IEEE standard LVDS reduced link (REDL)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output impedance | $R_0$ CC | 40 | - | 140 | Ohm | Vcm = 1.0 V and 1.4 V |
| Output differential voltage | $V_{OD}$ CC | 150 | - | 250 | mV | RT = 100 Ohm ±5% |
| Output voltage high | $V_{OH}$ CC | - | - | 1375 | mV | RT = 100 Ohm ±5% |
| Output voltage low | $V_{OL}$ CC | 1025 | - | - | mV | RT = 100 Ohm ±5% |
| Output offset (Common mode) voltage | $V_{OS}$ CC | 1125 | - | 1275 | mV | RT = 100 Ohm ±5% |
| Input voltage range | $V_I$ SR | 825 | - | 1575 | mV | Driver ground potential difference < 50 mV |
| Input differential threshold | $V_{idth}$ SR | -100 | - | 100 | mV | Driver ground potential difference < 50 mV |
| Change in VOS between 0 and 1 | $dVOS$ CC | - | - | 25 | mV | RT = 100 Ohm ±5% |
| Change in Vod between 0 and 1 | $dVod$ CC | - | - | 25 | mV | RT = 100 Ohm ±5% |
| Duty cycle | $t_{duty}$ CC | 45 | - | 55 | % | |

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**Table 3-25 LVDSH - IEEE standard LVDS reduced link (REDL)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{OD}$ Fall time [1] | $t_{fall10}$ CC | - | - | 0.5 | ns | ZL = 100 Ohm ±5% @ 2pF |
| $V_{OD}$ Rise time [1] | $t_{rise10}$ CC | - | - | 0.5 | ns | ZL = 100 Ohm ±5% @ 2pF |

1) Rise / fall times are defined for 10% - 90% of $V_{OD}$

default after start-up = CMOS function

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## 3.8 Medium performance LVDS Pads (LVDSM)

This LVDS pad type is used for the medium speed chip to chip communication inferface of the new TC270 / TC275 / TC277. It compose out of a LVDSM pad and a MP pad.

This pad combination is always supplied by the 5V or 3.3V.

For the parameters of the MP pad please see **Chapter 3.5**.

**Table 3-26 LVDSM**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output impedance | $R_O$ CC | 40 | 100 | 140 | Ohm | |
| Fall time | $t_F$ CC | - | - | 2.5 | ns | $Z_{load}$ = 100 Ohm; termination 100 Ohm ±1% |
| Rise time | $t_R$ CC | - | - | 2.5 | ns | $Z_{load}$ = 100 Ohm; termination 100 Ohm ±1% |
| Pad set-up time | $t_{SET_LVDS}$ CC | - | 10 | 13 | µs | |
| Output Differential Voltage | $V_{OD}$ CC | 250 | - | 400 | mV | termination 100 Ohm ±1% |
| Output voltage high | $V_{OH}$ CC | - | - | 1475 | mV | termination 100 Ohm ±1% |
| Output voltage low | $V_{OL}$ CC | 925 | - | - | mV | termination 100 Ohm ±1% |
| Output Offset Voltage | $V_{OS}$ CC | 1125 | - | 1275 | mV | termination 100 Ohm ±1% |

default after start-up = CMOS function

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## 3.9 VADC Parameters

VADC parameter are valid for $V_{DDM}$ = 4.5 V to 5.5 V.

This tables also covers the parameters for Class D pads.

**Table 3-27 VADC**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Analog reference voltage [1] | $V_{AREF}$ SR | $V_{AGND}$ + 1.0 | - | $V_{DDM}$ + 0.05 | V | |
| Analog reference ground | $V_{AGND}$ SR | $V_{SSM}$ - 0.05 | - | $V_{SSM}$ + 0.05 | V | |
| Analog input voltage range | $V_{AIN}$ SR | $V_{AGND}$ | - | $V_{AREF}$ | V | |
| Converter reference clock | $f_{ADCI}$ SR | 2 | - | 20 | MHz | |
| Charge consumption per conversion [2] [3] | $Q_{CONV}$ CC | - | 50 | 75 | pC | $V_{AIN}$ = 5 V, charge consumed from reference pin, precharging disabled |
| | | - | 10 | 22 | pC | $V_{AIN}$ = 5 V, charge consumed from reference pin, precharging enabled |
| Conversion time for 12-bit result | $t_{C12}$ CC | - | (16 + STC) x $t_{ADCI}$ + 2 x $t_{VADC}$ | - | | Includes sample time and post calibration |
| Conversion time for 10-bit result | $t_{C10}$ CC | - | (14 + STC) x $t_{ADCI}$ + 2 x $t_{VADC}$ | - | | Includes sample time |
| Conversion time for 8-bit result | $t_{C8}$ CC | - | (12 + STC) x $t_{ADCI}$ + 2 x $t_{VADC}$ | - | | Includes sample time |
| Conversion time for fast compare mode | $t_{CF}$ CC | - | (4 + STC) x $t_{ADCI}$ + 2 x $t_{VADC}$ | - | | Includes sample time |
| Broken wire detection delay against $V_{AGND}$ [4] | $t_{BWG}$ CC | - | - | 120 | cycles | Result below 10% |
| Broken wire detection delay against $V_{AREF}$ [5] | $t_{BWR}$ CC | - | - | 60 | cycles | Result above 80% |
| Input leakage at analog inputs | $I_{OZ1}$ CC | -350 | - | 350 | nA | Analog Inputs overlaid with class LP pads or pull down diagnostics |
| | | -150 | - | 150 | nA | else |
| Total Unadjusted Error [1] | $TUE$ CC | -4 [6] | - | 4 [6] | LSB | 12-bit resolution |

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**Table 3-27 VADC** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| INL Error | $EA_{INL}$ CC | -3 | - | 3 | LSB | 12-bit resolution |
| Gain Error [1] | $EA_{GAIN}$ CC | -3.5 | - | 3.5 | LSB | 12-bit resolution |
| DNL error [1] | $EA_{DNL}$ CC | -3 | - | 3 | LSB | 12-bit resolution |
| Offset Error [1] | $EA_{OFF}$ CC | -4 | - | 4 | LSB | 12-bit resolution |
| Total capacitance of an analog input | $C_{AINT}$ CC | - | - | 30 | pF | |
| Switched capacitance of an analog input | $C_{AINS}$ CC | 2 | 4 | 7 | pF | |
| Resistance of the analog input path | $R_{AIN}$ CC | - | - | 1.5 | kOhm | else |
| | | - | - | 1.8 | kOhm | valid for analog inputs mapped to GPIOs |
| Switched capacitance of a reference input | $C_{AREFS}$ CC | - | - | 30 | pF | |
| RMS Noise [7] | $EN_{RMS}$ CC | - | 0.5 | 0.8 [6][8] | LSB | |
| Positive reference $V_{AREFx}$ pin leakage | $I_{OZ2}$ CC | -7 | - | 7 | µA | $V_{AREFx} = V_{AREF2}$; $V_{AREF} > V_{DDM}$V; $T_J$>150°C |
| | | -4 | - | 4 | µA | $V_{AREFx} = V_{AREF2}$; $V_{AREF} > V_{DDM}$V; $T_J$≤150°C |
| | | -2 | - | 3 | µA | $V_{AREFx} = V_{AREF2}$; $V_{AREF} \leq V_{DDM}$V; $T_J$>150°C |
| | | -1 | - | 1 | µA | $V_{AREFx} = V_{AREF2}$; $V_{AREF} \leq V_{DDM}$V; $T_J$≤150°C |
| Negative reference $V_{AGNDx}$ pin leakage | $I_{OZ3}$ CC | -13 | - | 13 | µA | $V_{AGNDx} = V_{AGND2}$; $V_{AGND} < V_{SSM}$V; $T_J$>150°C |
| | | -7 | - | 7 | µA | $V_{AGNDx} = V_{AGND2}$; $V_{AGND} < V_{SSM}$V; $T_J$≤150°C |
| | | -3.3 | - | 2.5 | µA | $V_{AGNDx} = V_{AGND2}$; $V_{AREF} \leq V_{DDM}$V; $T_J$>150°C |
| | | -2.85 | - | 1 | µA | $V_{AGNDx} = V_{AGND2}$; $V_{AREF} \leq V_{DDM}$V; $T_J$≤150°C |
| Resistance of the reference input path | $R_{AREF}$ CC | - | - | 1 | kOhm | |
| CSD resistance [9] | $R_{CSD}$ CC | - | - | 28 | kOhm | |

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**Table 3-27 VADC** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Resistance of the multiplexer diagnostics pull-down device | $R_{MDD}$ CC | 25 + 1*$V_{IN}$ | - | 35 - 8*$V_{IN}$ | kOhm | 0 V ≤ $V_{IN}$ ≤ 2.5 V |
| | | -5 + 13*$V_{IN}$ | - | 15 + 16*$V_{IN}$ | kOhm | 2.5 V ≤ $V_{IN}$ ≤ $V_{DDM}$ |
| Resistance of the multiplexer diagnostics pull-up device | $R_{MDU}$ CC | 45 - 6*$V_{IN}$ | - | 90 - 16*$V_{IN}$ | kOhm | 0 V ≥ $V_{IN}$ ≤ 2.5 V |
| | | 40 - 4*$V_{IN}$ | - | 65 - 6*$V_{IN}$ | kOhm | 2.5 V ≤ $V_{IN}$ ≤ $V_{DDM}$ |
| Resistance of the pull-down test device [10] | $R_{PDD}$ CC | - | - | 0.3 | kOhm | |
| CSD voltage accuracy [11] [12] | $dVCSD$ CC | - | - | 10 | % | |
| Wakeup time | $t_{WU}$ CC | - | - | 12 | µs | |

1) If the reference voltage is reduced by the factor k (k < 1), TUE,DNL,INL,Gain, and Offset errors increase also by the factor 1/k. $V_{AREF}$ must be decoupled with an external capacitor.
2) For QCONV = X pC and a conversion time of 1 µs a rms value of X µA results for $I_{AREFx}$.
3) For the details of the mapping for a VADC group to pin $V_{AREFx}$ please see the User's Manual.
4) The broken wire detection delay against $V_{AGND}$ is measured in numbers of consecutive precharge cycles at a conversion rate higher than 1 conversion per 500 ms.
5) The broken wire detection delay against $V_{AREF}$ is measured in numbers of consecutive precharge cycles at a conversion rate higher than 1 conversion per 10 ms. This function is influenced by leakage current, in particular at high temperature.
6) Resulting worst case combined error is arithmetic combination of TUE and $EN_{RMS}$.
7) This parameter is valid for soldered devices and requires careful analog board design.
8) Value is defined for one sigma Gauss distribution.
9) In order to avoid an additional error due to incomplete sampling, the sampling time shall be set greater than 5 * $R_{CSD}$ * $C_{AINS}$.
10) The pull-down resistor $R_{PDD}$ is connected between the input pad and the analog multiplexer. The input pad itself adds another 200-Ohm series resistance, when measuring through the pin.
11) CSD: Converter Self Diagnostics, for details please consult the User's Manual.
12) Note, that in case CSD voltage is chosen to nom. 1/3 or 2/3 of $V_{AREF}$ voltage, the reference voltage is loaded with a current of max. $V_{AREF}$ / 45 kOhm.

The following VADC parameter are valid for $V_{DDM}$ = 2.97 V to 3.63 V.

**Table 3-28 VADC_33V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Analog reference voltage [1] | $V_{AREF}$ SR | $V_{AGND}$ + 1.0 | - | $V_{DDM}$ + 0.05 | V | |
| Analog reference ground | $V_{AGND}$ SR | $V_{SSM}$ - 0.05 | - | $V_{SSM}$ + 0.05 | V | |
| Analog input voltage range | $V_{AIN}$ SR | $V_{AGND}$ | - | $V_{AREF}$ | V | |
| Converter reference clock | $f_{ADCI}$ SR | 2 | - | 20 | MHz | |

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**Table 3-28 VADC_33V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Charge consumption per conversion [2) 3)] | $Q_{CONV}$ CC | - | 35 | 50 | pC | $V_{AIN}$ = 3.3 V, charge consumed from reference pin, precharging disabled |
| | | - | 8 | 17 | pC | $V_{AIN}$ = 3.3 V, charge consumed from reference pin, precharging enabled |
| Conversion time for 12-bit result | $t_{C12}$ CC | - | (16 + STC) x $t_{ADCI}$ + 2 x $t_{VADC}$ | - | | Includes sample time and post calibration |
| Conversion time for 10-bit result | $t_{C10}$ CC | - | (14 + STC) x $t_{ADCI}$ + 2 x $t_{VADC}$ | - | | Includes sample time |
| Conversion time for 8-bit result | $t_{C8}$ CC | - | (12 + STC) x $t_{ADCI}$ + 2 x $t_{VADC}$ | - | | Includes sample time |
| Conversion time for fast compare mode | $t_{CF}$ CC | - | (4 + STC) x $t_{ADCI}$ + 2 x $t_{VADC}$ | - | | Includes sample time |
| Broken wire detection delay against $V_{AGND}$ [4)] | $t_{BWG}$ CC | - | - | 120 | cycles | Result below 10% |
| Broken wire detection delay against $V_{AREF}$ [5)] | $t_{BWR}$ CC | - | - | 60 | cycles | Result above 80% |
| Input leakage at analog inputs | $I_{OZ1}$ CC | -350 | - | 350 | nA | Analog Inputs overlaid with class LP pads or pull down diagnostics |
| | | -150 | - | 150 | nA | else |
| Total Unadjusted Error [1)] | $TUE$ CC | -12 [6)] | - | 12 [6)] | LSB | 12-bit Resolution; $T_J$ > 150 °C |
| | | -6 [6)] | - | 6 [6)] | LSB | 12-bit Resolution; $T_J$ ≤ 150 °C |
| INL Error | $EA_{INL}$ CC | -12 | - | 12 | LSB | 12-bit Resolution; $T_J$ > 150 °C |
| | | -5 | - | 5 | LSB | 12-bit Resolution; $T_J$ ≤ 150 °C |
| Gain Error [1)] | $EA_{GAIN}$ CC | -6 | - | 6 | LSB | 12-bit Resolution; $T_J$ > 150 °C |
| | | -5.5 | - | 5.5 | LSB | 12-bit Resolution; $T_J$ ≤ 150 °C |

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**Table 3-28 VADC_33V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DNL error [1] | $EA_{DNL}$ CC | -4 | - | 4 | LSB | 12-bit resolution |
| Offset Error [1] | $EA_{OFF}$ CC | -6 | - | 6 | LSB | 12-bit Resolution; $T_J$ > 150 °C |
| | | -5 | - | 5 | LSB | 12-bit Resolution; $T_J$ ≤ 150 °C |
| Total capacitance of an analog input | $C_{AINT}$ CC | - | - | 30 | pF | |
| Switched capacitance of an analog input | $C_{AINS}$ CC | 2 | 4 | 7 | pF | |
| Resistance of the analog input path | $R_{AIN}$ CC | - | - | 4.5 | kOhm | |
| Switched capacitance of a reference input | $C_{AREFS}$ CC | - | - | 30 | pF | |
| RMS Noise [7] | $EN_{RMS}$ CC | - | - | 1.7 [6][8] | LSB | |
| Positive reference $V_{AREFx}$ pin leakage | $I_{OZ2}$ CC | -6 | - | 6 | µA | $V_{AREFx} = V_{AREF2}$; $V_{AREF} > V_{DDM}$V; $T_J$>150°C |
| | | -3.5 | - | 3.5 | µA | $V_{AREFx} = V_{AREF2}$; $V_{AREF} > V_{DDM}$V; $T_J$≤150°C |
| | | -2 | - | 2.5 | µA | $V_{AREFx} = V_{AREF2}$; $V_{AREF} ≤ V_{DDM}$V; $T_J$>150°C |
| | | -1 | - | 1 | µA | $V_{AREFx} = V_{AREF2}$; $V_{AREF} ≤ V_{DDM}$V; $T_J$≤150°C |
| Negative reference $V_{AGNDx}$ pin leakage | $I_{OZ3}$ CC | -12 | - | 12 | µA | $V_{AGNDx} = V_{AGND2}$; $V_{AGND} < V_{SSM}$V; $T_J$>150°C |
| | | -6.5 | - | 6.5 | µA | $V_{AGNDx} = V_{AGND2}$; $V_{AGND} < V_{SSM}$V; $T_J$≤150°C |
| | | -2.2 | - | 2 | µA | $V_{AGNDx} = V_{AGND2}$; $V_{AREF} ≤ V_{DDM}$V; $T_J$>150°C |
| | | -1 | - | 1 | µA | $V_{AGNDx} = V_{AGND2}$; $V_{AREF} ≤ V_{DDM}$V; $T_J$≤150°C |
| Resistance of the reference input path | $R_{AREF}$ CC | - | - | 3 | kOhm | |
| CSD resistance [9] | $R_{CSD}$ CC | - | - | 28 | kOhm | |

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**Table 3-28 VADC_33V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Resistance of the multiplexer diagnostics pull-down device | $R_{MDD}$ CC | $25 + 3*V_{IN}$ | - | $40 + 12*V_{IN}$ | kOhm | $0\ V \le V_{IN} \le 1.667\ V$ |
| | | $0 + 18*V_{IN}$ | - | $0 + 18*V_{IN}$ | kOhm | $1.667\ V \le V_{IN} \le V_{DDM}$ |
| Resistance of the multiplexer diagnostics pull-up device | $R_{MDU}$ CC | $60 - 12*V_{IN}$ | - | $120 - 30*V_{IN}$ | kOhm | $0\ V \le V_{IN} \le 1.667\ V$ |
| | | $55 - 9*V_{IN}$ | - | $95 - 15*V_{IN}$ | kOhm | $1.667\ V \le V_{IN} \le V_{DDM}$ |
| Resistance of the pull-down test device [10] | $R_{PDD}$ CC | - | - | 0.9 | kOhm | |
| CSD voltage accuracy [11] [12] | $dVCSD$ CC | - | - | 10 | % | |
| Wakeup time | $t_{WU}$ CC | - | - | 12 | µs | |

1) If the reference voltage is reduced by the factor k (k < 1), TUE,DNL,INL,Gain, and Offset errors increase also by the factor 1/k. $V_{AREF}$ must be decoupled with an external capacitor.
2) For QCONV = X pC and a conversion time of 1 µs a rms value of X µA results for $I_{AREFx}$.
3) For the details of the mapping for a VADC group to pin $V_{AREFx}$ please see the User's Manual.
4) The broken wire detection delay against $V_{AGND}$ is measured in numbers of consecutive precharge cycles at a conversion rate higher than 1 conversion per 500 ms.
5) The broken wire detection delay against $V_{AREF}$ is measured in numbers of consecutive precharge cycles at a conversion rate higher than 1 conversion per 10 ms. This function is influenced by leakage current, in particular at high temperature.
6) Resulting worst case combined error is arithmetic combination of TUE and $EN_{RMS}$.
7) This parameter is valid for soldered devices and requires careful analog board design.
8) Value is defined for one sigma Gauss distribution.
9) In order to avoid an additional error due to incomplete sampling, the sampling time shall be set greater than 5 * $R_{CSD}$ * $C_{AINS}$.
10) The pull-down resistor $R_{PDD}$ is connected between the input pad and the analog multiplexer. The input pad itself adds another 200-Ohm series resistance, when measuring through the pin.
11) CSD: Converter Self Diagnostics, for details please consult the User's Manual.
12) Note, that in case CSD voltage is chosen to nom. 1/3 or 2/3 of $V_{AREF}$ voltage, the reference voltage is loaded with a current of max. $V_{AREF}$ / 45 kOhm.

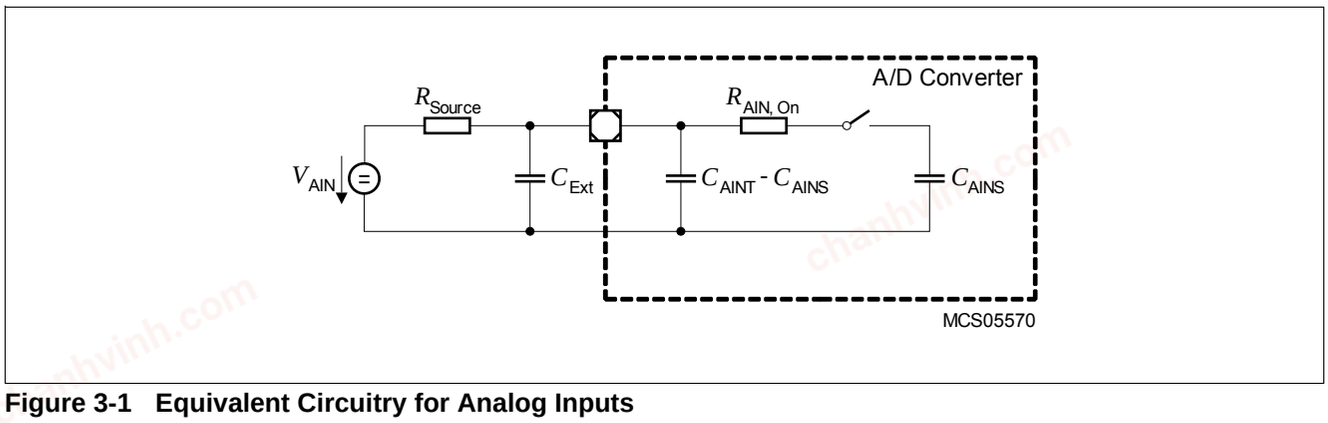



**Figure 3-1 Equivalent Circuitry for Analog Inputs**

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## 3.10 DSADC Parameters

The following DSADC parameter are valid for $V_{DDM}$ = 4.5 V to 5.5 V.

**Table 3-29 DSADC**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Analog input voltage range [1] | $V_{DSIN}$ SR | 0 | - | 5 | V | single ended |
| | | 0 | - | 10 | V | differential;$V_{DSxP}$ - $V_{DSxN}$ |
| Reference load current | $I_{REF}$ SR | - | 4.5 | 6.3 | µA | per twin-modulator (1 or 2 channels) |
| Modulator clock frequency [2] | $f_{MOD}$ SR | 10 | - | 20 | MHz | |
| Gain error | $ED_{GAIN}$ CC | -1 | - | 1 [3] | % | Calibrated once |
| | | -3.5 [4] | - | 3.5 [4] | % | Uncalibrated |
| | | -0.2 | - | 0.2 [5] | % | calibrated; GAIN = 1; MODCFG.INCFGx=01 |
| DC offset error | $ED_{OFF}$ CC | -5 | - | 5 [5] | mV | calibrated |
| | | -50 | - | 50 | mV | calibrated once |
| | | -100 [4] | 0[4] | 100 [4] | mV | gain = 1; uncalibrated |
| Common Mode Rejection Ratio | $ED_{CM}$ CC | 200 | 500 | - | | |
| Input impedance [6] | $R_{DAIN}$ CC | 100 | 130 | 170 | kOhm | Exact value (±1%) available in UCB |
| Signal-Noise Ratio [7] [8] [9] [10] | $SNR$ CC | 80 | - | - | dB | $f_{PB}$ = 30 kHz; $V_{DDM}$ = ±5%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| | | 78 | - | - | dB | $f_{PB}$ = 50 kHz; $V_{DDM}$ = ±5%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| | | 70 | - | - | dB | $f_{PB}$ = 100 kHz; $V_{DDM}$ = ±10%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| | | 74 | - | - | dB | $f_{PB}$ = 100 kHz; $V_{DDM}$ = ±5%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| | | 76 | - | - | dB | $f_{PB}$ = 30 kHz; $V_{DDM}$ = ±10%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| | | 74 | - | - | dB | $f_{PB}$ = 50 kHz; $V_{DDM}$ = ±10%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| Pass band | $f_{PB}$ CC | 10 [11] | - | 100 | kHz | Output data rate $f_D$ = $f_{PB}$ * 3 |
| Pass band ripple [8] | $df_{PB}$ CC | -1 | - | 1 | % | |
| Output sampling rate | $f_D$ CC | 30 | - | 330 | kHz | |

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**Table 3-29 DSADC** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DC compensation factor | $DCF$ CC | -3 | - | - | dB | $10^{-5}$ $f_D$ |
| Positive reference $V_{AREF1}$ pin leakage | $I_{OZ5}$ CC | -2 | - | 2 | µA | all ADCs disabled |
| Negative reference $V_{AGND1}$ pin leakage | $I_{OZ6}$ CC | -2 | - | 2 | µA | all ADCs disabled |
| Stop band attenuation [8] | $SBA$ CC | 40 | - | - | dB | 0.5 ... 1 $f_D$ |
| | | 45 | - | - | dB | 1 ... 1.5 $f_D$ |
| | | 50 | - | - | dB | 1.5 ... 2 $f_D$ |
| | | 55 | - | - | dB | 2 ... 2.5 $f_D$ |
| | | 60 | - | - | dB | 2.5 ... OSR/2 $f_D$ |
| Reference ground voltage | $V_{AGND}$ SR | $V_{SSM}$ - 0.05 | - | $V_{SSM}$ + 0.05 | V | |
| Positive reference voltage | $V_{AREF}$ SR | $V_{DDMnom}$ * 0.9 | - | $V_{DDM}$ + 0.05 | V | |
| Common mode voltage accuracy | $dV_{CM}$ CC | -100 | - | 100 | mV | from selected voltage |
| Common mode hold voltage deviation [12] | $dV_{CMH}$ CC | -200 | - | 200 | mV | From common mode voltage |
| Analog filter settling time | $t_{AFSET}$ CC | - | 2 | 4 | µs | If enabled |
| Modulator recovery time | $t_{MREC}$ CC | - | 3.5 | 5.5 | µs | After leaving overdrive state |
| Modulator settling time [13] | $t_{MSET}$ CC | - | 1 | - | µs | After switching on, voltage regulator already running |
| Spurious Free Dynamic Range [7][14] | SFDR CC | 60 | - | - | dB | $V_{CM}$ = 2.2 V, DC coupled; $V_{DDM}$ = ±10% |

1) The maximum input range for symmetrical signals (e.g. AC-coupled inputs) depends on the selected internal/external common mode voltage. In this case the Amplitude is limited to $V_{CM}$ * 2.
2) All modulators must run on the same frequency.
3) The calibration sequence must be executed once after an Application Reset
4) The total DC error for the uncalibrated case can be calculated by the geometric addition of $ED_{GAIN}$ and $ED_{OFF}$
5) Recalibration needed in case of a temperature change > 20ºC
6) The variation of the impedance between different channels is < 1.5%.
7) Derating factors:
   -2 dB in standard-performance mode.
   -3 dB for CMV = $10_B$, i.e. $V_{CM}$ = ($V_{AREF}$±2%) / 2.0.
8) CIC3, FIR0, FIR1 filters enabled.
9) Single-ended mode reduces the SNR by 6 dB if the unused input is grounded, by 3 dB if the unused input connects to $V_{CM}$ (GAIN = 2).
10) The defined limits are only valid if the following condition is not applicable: $T_J$ > 150°C and $V_{VAREF}$ > $V_{DDM}$.
11) 10 kHz only reachable with 10 MHz modulator clock frequency.
12) Voltage $V_{CM}$ is proportional to $V_{AREF}$, voltage $V_{CMH}$ is proportional to $V_{DDM}$.
13) The modulator needs to settle after being switched on and after leaving the overdrive state.
14) SFDR = 20 * log(INL / $2^N$); N = amount of bits

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The following DSADC parameter are valid for $V_{DDM}$ = 2.97 V to 3.63 V.

**Table 3-30 DSADC_33V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Analog input voltage range [1] | $V_{DSIN}$ SR | 0 | - | 3.3 | V | single ended |
| | | 0 | - | 6.6 | V | differential;$V_{DSxP}$ - $V_{DSxN}$ |
| Reference load current | $I_{REF}$ SR | - | 4.5 | 5.8 | µA | per twin-modulator (1 or 2 channels) |
| Modulator clock frequency [2] | $f_{MOD}$ SR | 10 | - | 20 | MHz | |
| Gain error | $ED_{GAIN}$ CC | -1.5 | - | 1.5 [3] | % | Calibrated once |
| | | -10 [4] | - | 10 [4] | % | Uncalibrated |
| | | -0.3 | - | 0.3 [5] | % | calibrated; GAIN = 1; MODCFG.INCFGx=01 |
| DC offset error | $ED_{OFF}$ CC | -5 | - | 5 [5] | mV | calibrated |
| | | -50 | - | 50 | mV | calibrated once |
| | | -100 [4] | - | 100 [4] | mV | gain = 1; uncalibrated |
| | | - | 0[4] | - | mV | gain = 1; uncalibrated; uncalibrated |
| Common Mode Rejection Ratio | $ED_{CM}$ CC | 200 | 500 | - | | |
| Input impedance [6] | $R_{DAIN}$ CC | 100 | 130 | 170 | kOhm | Exact value (±1%) available in UCB |
| Signal-Noise Ratio [7] [8] [9] [10] | $SNR$ CC | 45 | 63 | - | dB | $f_{PB}$ = 100kHz; $V_{DDM}$ = ±10%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| | | 60 | 69 | - | dB | $f_{PB}$ = 100kHz; $V_{DDM}$ = ±5%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| | | 60 | 68 | - | dB | $f_{PB}$ = 30kHz; $V_{DDM}$ = ±10%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| | | 69 | 74 | - | dB | $f_{PB}$ = 30kHz; $V_{DDM}$ = ±5%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| | | 55 | 66 | - | dB | $f_{PB}$ = 50kHz; $V_{DDM}$ = ±10%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| | | 65 | 72 | - | dB | $f_{PB}$ = 50kHz; $V_{DDM}$ = ±5%; $f_{MOD}$ = 20 MHz; GAIN = 1 |
| Pass band | $f_{PB}$ CC | 10 [11] | - | 100 | kHz | Output data rate $f_D$ = $f_{PB}$ * 3 |
| Pass band ripple [8] | $df_{PB}$ CC | -1 | - | 1 | % | |

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**Table 3-30 DSADC_33V** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output sampling rate | $f_D$ CC | 30 | - | 330 | kHz | |
| DC compensation factor | $DCF$ CC | -3 | - | - | dB | $10^{-5}$ $f_D$ |
| Positive reference $V_{AREF1}$ pin leakage | $I_{OZ5}$ CC | -2 | - | 2 | µA | |
| Negative reference $V_{AGND1}$ pin leakage | $I_{OZ6}$ CC | -2 | - | 2 | µA | |
| Stop band attenuation [8] | $SBA$ CC | 40 | - | - | dB | 0.5 ... 1 $f_D$ |
| | | 45 | - | - | dB | 1 ... 1.5 $f_D$ |
| | | 50 | - | - | dB | 1.5 ... 2 $f_D$ |
| | | 55 | - | - | dB | 2 ... 2.5 $f_D$ |
| | | 60 | - | - | dB | 2.5 ... OSR/2 $f_D$ |
| Reference ground voltage | $V_{AGND}$ SR | $V_{SSM}$ - 0.05 | - | $V_{SSM}$ + 0.05 | V | |
| Positive reference voltage | $V_{AREF}$ SR | $V_{DDMnom}$ * 0.9 | - | $V_{DDM}$ + 0.05 | V | |
| Common mode voltage accuracy | $dV_{CM}$ CC | -100 | - | 100 | mV | from selected voltage |
| Common mode hold voltage deviation [12] | $dV_{CMH}$ CC | -200 | - | 200 | mV | From common mode voltage |
| Analog filter settling time | $t_{AFSET}$ CC | - | 2 | 4 | µs | If enabled |
| Modulator recovery time | $t_{MREC}$ CC | - | 3.5 | - | µs | After leaving overdrive state |
| Modulator settling time [13] | $t_{MSET}$ CC | - | 1 | - | µs | After switching on, voltage regulator already running |
| Spurious Free Dynamic Range [7][14] | SFDR CC | 52 | - | - | dB | $V_{CM}$ = 2.2 V, DC coupled; $V_{DDM}$ = ±10% |
| | | 60 | - | - | dB | $V_{CM}$ = 2.2 V, DC coupled; $V_{DDM}$ = ±5% |

1) The maximum input range for symmetrical signals (e.g. AC-coupled inputs) depends on the selected internal/external common mode voltage. In this case the Amplitude is limited to $V_{CM}$ * 2.
2) All modulators must run on the same frequency.
3) The calibration sequence must be executed once after an Application Reset
4) The total DC error for the uncalibrated case can be calculated by the geometric addition of $ED_{GAIN}$ and $ED_{OFF}$
5) Recalibration needed in case of a temperature change > 20ºC.
6) The variation of the impedance between different channels is < 1.5%.
7) Derating factors:
-2 dB in standard-performance mode.
-3 dB for CMV = $10_B$, i.e. $V_{CM}$ = ($V_{AREF}$±2%) / 2.0.
8) CIC3, FIR0, FIR1 filters enabled.
9) Single-ended mode reduces the SNR by 6 dB if the unused input is grounded, by 3 dB if the unused input connects to $V_{CM}$ (GAIN = 2).
10) The defined limits are only valid if the following condition is not applicable: $T_J$ > 150°C and $V_{VAREF}$ > $V_{DDM}$.

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11) 10 kHz bandwidth only with 10Mhz modulator clock frequency  reachable
12) Voltage $V_{CM}$ is proportional to $V_{AREF}$, voltage $V_{CMH}$ is proportional to $V_{DDM}$.
13) The modulator needs to settle after being switched on and after leaving the overdrive state.
14) SFDR = 20 * log(INL / $2^N$); N = amount of bits

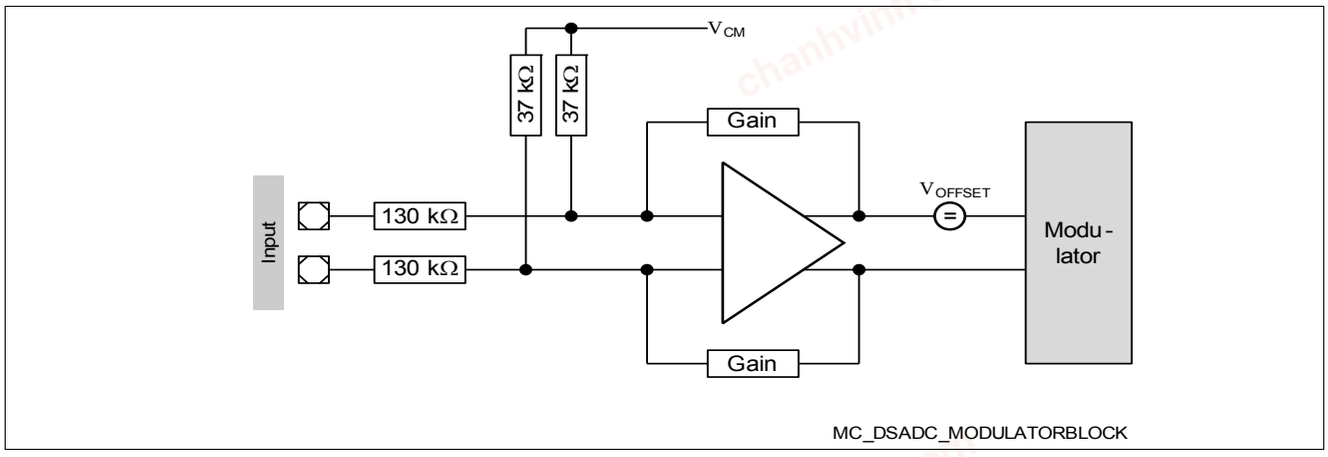



**Figure 3-2 DSADC Analog Inputs**

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## 3.11 MHz Oscillator

OSC_XTAL is used as accurate and exact clock source. OSC_XTAL supports 8 MHz to 40 MHz crystals external outside of the device. Support of ceramic resonators is also provided.

**Table 3-31 OSC_XTAL**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input current at XTAL1 | $I_{IX1}$ CC | -25 | - | 25 | µA | $V_{IN}$>0V ; $V_{IN}$<$V_{DDP3}$V |
| Oscillator frequency | $f_{OSC}$ SR | 4 | - | 40 | MHz | Direct Input Mode selected |
| | | 8 | - | 40 | MHz | External Crystal Mode selected |
| Oscillator start-up time [1] | $t_{OSCS}$ CC | - | - | 5 [2] | ms | |
| Input high voltage at XTAL1 | $V_{IHBX}$ SR | 0.8 | - | $V_{DDP3}$ + 0.5 | V | If shaper is bypassed |
| Input low voltage at XTAL1 | $V_{ILBX}$ SR | -0.5 | - | 0.4 | V | If shaper is bypassed |
| Input voltage at XTAL1 | $V_{IX}$ SR | -0.5 | - | $V_{DDP3}$ + 0.5 | V | If shaper is not bypassed |
| Input amplitude (peak to peak) at XTAL1 | $V_{PPX}$ SR | 0.3 * $V_{DDP3}$ | - | $V_{DDP3}$ + 1.0 | V | If shaper is not bypassed; $f_{OSC}$ > 25MHz |
| | | 0.4 * $V_{DDP3}$ | - | $V_{DDP3}$ + 1.0 | V | If shaper is not bypassed; $f_{OSC}$ ≤ 25MHz |
| Internal load capacitor | $C_{L0}$ CC | 2 | 2.35 | 2.7 | pF | |
| Internal load capacitor | $C_{L1}$ CC | 2 | 2.35 | 2.7 | pF | |
| Internal load capacitor | $C_{L2}$ CC | 3 | 3.5 | 4 | pF | |
| Internal load capacitor | $C_{L3}$ CC | 5.1 | 5.9 | 6.6 | pF | |

1) $t_{OSCS}$ is defined from the moment when $V_{DDP3}$ = 3.13V until the oscillations reach an amplitude at XTAL1 of 0.3 * $V_{DDP3}$. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.

2) This value depends on the frequency of the used external crystal. For faster crystal frequencies this value decrease.

*Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

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## 3.12 Back-up Clock

The back-up clock provides an alternative clock source.

**Table 3-32 Back-up Clock**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Back-up clock before trimming | $f_{BACKUT}$ CC | 75 | 100 | 125 | MHz | $V_{EXT}$≥2.97V |
| Back-up clock after trimming | $f_{BACKT}$ CC | 97.5 | 100 | 102.5 | MHz | $V_{EXT}$≥2.97V |

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## 3.13 Temperature Sensor

**Table 3-33 DTS**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Measurement time | $t_M$ CC | - | - | 100 | µs | |
| Calibration reference accuracy | $T_{CALACC}$ CC | -1 | - | 1 | °C | calibration points @ $T_J$=-40°C and $T_J$=127°C |
| Non-linearity accuracy over temperature range | $T_{NL}$ CC | -2 | - | 2 | °C | |
| Temperature sensor range | $T_{SR}$ SR | -40 | - | 170 | °C | |
| Start-up time after resets inactive | $t_{TSST}$ SR | - | - | 20 | µs | |

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

(3.1)

$$Tj = \frac{DTSSTATRESULT - (607)}{2,13}$$

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## 3.14 Power Supply Current

The total power supply current defined below consists of leakage and switching component.

Application relevant values are typically lower than those given in the following table and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:

The real (realisic) power pattern defines the following conditions:

- $T_J$ = 150 °C
- $f_{SRI} = f_{MAX} = f_{CPU0}$ = 200 MHz
- $f_{SPB} = f_{STM} = f_{GTM} = f_{BAUD1} = f_{BAUD2} = f_{ASCLIN}$ = 40 MHz
- $V_{DD}$ = 1.326 V
- $V_{DDP3}$ = 3.366 V
- $V_{EXT / FLEX} = V_{DDM}$ = 5.1 V
- all cores are active including one lockstep core
- the following peripherals are inactive: HSM, HSCT, Ethernet, PSI5, I2C, FCE, MTU, and 50% of the DSADC channels

The max power pattern defines the following conditions:

- $T_J$ = 150 °C
- $f_{SRI} = f_{MAX} = f_{CPU0}$ = 200 MHz
- $f_{SPB} = f_{STM} = f_{GTM} = f_{BAUD1} = f_{BAUD2} = f_{ASCLIN}$ = 100 MHz
- $V_{DD}$ = 1.43 V
- $V_{DDP3}$ = 3.63 V
- $V_{EXT / FLEX} = V_{DDM}$ = 5.5 V
- all cores and lockstep cores are active
- all peripherals are active

**Table 3-34 Power Supply**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ∑ Sum of $I_{DD}$ 1.3 V core and peripheral supply currents | $I_{DD}$ CC | - | - | 550 | mA | max power pattern |
| | | - | - | 350 | mA | real power pattern |
| $I_{DD}$ core current during active power-on reset (PORST held low) | $I_{DDPORST}$ CC | - | - | 80 | mA | $T_J$=125°C |
| | | - | - | 160 | mA | $T_J$=150°C |
| | | - | - | 215 | mA | $T_J$=165°C |
| $I_{DD}$ core current of CPU0 lockstep core active | $I_{DDC01}$ CC | - | - | 36 | mA | real power pattern |
| $I_{DD}$ core current of CPU1 main core with CPU1 lockstep core inactive | $I_{DDC10}$ CC | - | - | 43 | mA | real power pattern |
| $I_{DD}$ core current of CPU1 main core with lockstep core active | $I_{DDC11}$ CC | - | - | $I_{DDC10}$ + 36 | mA | real power pattern |
| $I_{DD}$ core current of CPU2 main core | $I_{DDC20}$ CC | - | - | 37 | mA | real power pattern |

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**Table 3-34 Power Supply** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $I_{DD}$ core current added by HSM | $I_{DDHSM}$ CC | - | - | 20 | mA | HSM running at 100MHz. |
| ∑ Sum of 3.3 V supply currents without pad activity | $I_{DDx3RAIL}$ CC | - | - | 57 | mA | real power pattern |
| $I_{DDFL3}$ Flash memory current | $I_{DDFL3}$ CC | - | - | 42 [1] | mA | flash read current |
| | | - | - | 42 [2] | mA | flash read current while programming Dflash |
| $I_{DDP3}$ supply current without pad activity | $I_{DDP3}$ CC | - | - | 15 [1] | mA | real power pattern; incl. OSC current & flash read current |
| | | - | - | 37 [3] | mA | incl. OSC current and flash 3.3V programming current when using external 5V supply |
| | | - | - | 39 [2] | mA | incl. OSC current and flash programming current at 3.3V |
| $I_{DDP3}$ supply current for LVDSH pads in LVDS mode | $I_{DDP3LVDSH}$ CC | - | - | 16 | mA | |
| Σ Sum of external and ADC supply currents (incl. $I_{EXTFLEX}$+$I_{DDM}$+$I_{EXTLVDSM}$) | $I_{EXTRAIL}$ CC | - | - | 62 | mA | real power pattern |
| Sum of $I_{EXT}$ and $I_{FLEX}$ supply current without pad activity | $I_{EXT/FLEX}$ CC | - | - | 4 | mA | real power pattern; PORST output inactive. |
| $I_{EXT}$ supply current for LVDSM pads in LVDS mode | $I_{EXTLVDSM}$ CC | - | - | 14 [4] | mA | real power pattern |

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**Table 3-34 Power Supply** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $I_{DDM}$ supply current | $I_{DDM}$ CC | - | - | 44 | mA | real power pattern; sum of currents of DSADC and VADC modules |
| | | - | - | 30 | mA | current for DSADC module only; 50% DSADC channels active. |
| | | - | - | 14 | mA | real pattern; current for VADC only |
| | | - | - | 59 5) | mA | max power pattern; All DSADC channels active 100% time. |
| | | - | - | 17 6) | mA | max power pattern; All VADC converters are active 100% time |
| Σ Sum of all currents (incl. $I_{EXTRAIL}$+$I_{DDx3RAIL}$+$I_{DD}$) | $I_{DDTOT}$ CC | - | - | 469 | mA | real power pattern |
| Σ Sum of all currents with DC-DC EVR13 regulator active 7) | $I_{DDTOTDC3}$ CC | - | - | 302 | mA | real power pattern; $V_{EXT}$ = 3.3$V$ |
| Σ Sum of all currents with DC-DC EVR13 regulator active 7) | $I_{DDTOTDC5}$ CC | - | - | 240 | mA | real power pattern; $V_{EXT}$ = 5$V$ |
| ∑ Sum of all currents (STANDBY mode) | $I_{EVRSB}$ CC | - | - | 150 8) | µA | Standby RAM is active. Power to remaining domains switched off. $T_J$ = 25°$C$; $V_{EVRSB}$ = 5$V$ |
| ∑ Sum of all currents (SLEEP mode) | $I_{SLEEP}$ CC | - | - | 15 | mA | All CPUs in idle, All peripherals in sleep, $f_{SRI/SPB}$ = 1 $MHz$ via LPDIV divider; $T_J$ = 25°$C$ |
| Maximum power dissipation | $PD$ CC | - | - | 1480 | mW | max power pattern |
| | | - | - | 1014 | mW | real power pattern |

1) Realistic Pflash read pattern with 70% Pflash bandwidth utlilization and a code mix of 50% 0s and 50% 1s. A common decoupling capacitor of atleast 100nF for ($V_{DDFL3}$+$V_{DDP3}$) is used. Dflash read current is also included. Flash read current is predominantly drawn from $V_{DDFL3}$ pin and a minor part drawn from the neighbouring $V_{DDP3}$ pin.

2) Continuous Dflash programming in burst mode with 3.3 V supply and realistic Pflash read access in parallel. Erase currents of the corresponding flash modules are less than the respective programming currents at $V_{DDP3}$ pin. Programming and erasing flash may generate transient current spikes of up to x mA for maximum x us which is handled by the decoupling and buffer capacitors. This parameter is relevant for external power supply dimensioning and not for thermal considerations.

3) In addition to the current specified, upto 4 mA is additionally drawn at $V_{EXT}$ supply in burst programming mode with 5V external supply. Erase currents of the corresponding flash modules are less than the respective programming currents at $V_{DDP3}$ supply. This parameter is relevant for external power supply dimensioning and not for thermal considerations.

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4) The current consumption is for 2 pairs of LVDSM differential pads (8 pins). A single pair of LVDSM differential pads (4 pins) consumes 7 mA.
5) The current consumption is for 6 DS channels with standard performance (MCFG=11b). A single DS channel instance consumes 6-8 mA.
6) A single converter instance of VADC unit consumes 2 mA.
7) The total current drawn from external regulator is estimated with 72% EVR13 SMPS regulator Efficiency. $I_{DDTOTDC}$x is calculated from $I_{DDTOT}$ using the scaled core current [($I_{DD}$ x $V_{DD}$)/(VinxEfficiency)] and constitutes all other rail currents and $I_{DDM}$.
8) Current at $V_{EVRSB}$ supply pin during normal RUN mode is less than 5 mA at Tj =150 degC. The transition between RUN mode to STANDBY mode has a duration of less than 100us during which the current is higher but is less than 8 mA at Tj =150 degC. Once STANDBY mode is entered with only Standby RAM active the current is less than 5mA at Tj = 150 degC. It is recommended to have atleast 100 nF decoupling capacitor at this pin.

### 3.14.1 Calculating the 1.3 V Current Consumption

The current consumption of the 1.3 V rail compose out of two parts:

- Static current consumption
- Dynamic current consumption

The static current consumption is related to the device temperature $T_J$ and the dynamic current consumption depends of the configured clocking frequencies and the software application executed. These two parts needs to be added in order to get the rail current consumption.

(3.2)

$$I_0 = 1,135\left[\frac{mA}{C}\right] \times e^{0,02689 \times T_J[C]}$$

(3.3)

$$I_0 = 3,264\left[\frac{mA}{C}\right] \times e^{0,0259 \times T_J[C]}$$

Function 2 defines the typical static current consumption and Function 3 defines the maximum static current consumption. Both functions are valid for $V_{DD}$ = 1.326 V.

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## 3.15 Power-up and Power-down

### 3.15.1 External Supply Mode

5 V & 1.3 V supplies are externally supplied. 3.3V is generated internally by EVR33.

- External supplies VEXT and VDD may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s). Voltage Ramp-up from a residual threshold (Eg : up to 1 V) should also lead to a normal startup of the device.
- The rate at which current is drawn from the external regulator (dIEXT /dt or dIDD /dt) is limited in the Start-up phase to a maximum of 50 mA/100 us.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when atleast one among the three supply domains (1.3 V, 3.3 V or 5 V) violate their primary under-voltage reset thresholds.The PORST (output) is deasserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available.
- The power sequence as shown in **Figure 3-3** is enumerated below
  - T1 refers to the point in time when basic supply and clock infrastructure is available as the external supplies ramp up. The supply mode is evaluated based on the HWCFG [0:2] pins and consequently a soft start of EVR33 regulator is initiated.
  - T2 refers to the point in time when all supplies are above their primary reset thresholds. EVR33 regulator has ramped up. PORST (output) is deasserted and HWCFG [0:7] pins are latched on PORST rising edge. Firmware execution is initiated.
  - T3 refers to the point in time when Firmware execution is completed. User code execution starts with a default frequency of 100 MHz.
  - T4 refers to the point in time during the Ramp-down phase when atleast one of the externally provided or generated supplies (1.3 V, 3.3 V or 5 V) drop below their respective primary under-voltage reset thresholds.

Please note that there is no special requirements for $\overline{\text{PORST}}$ slew rates.

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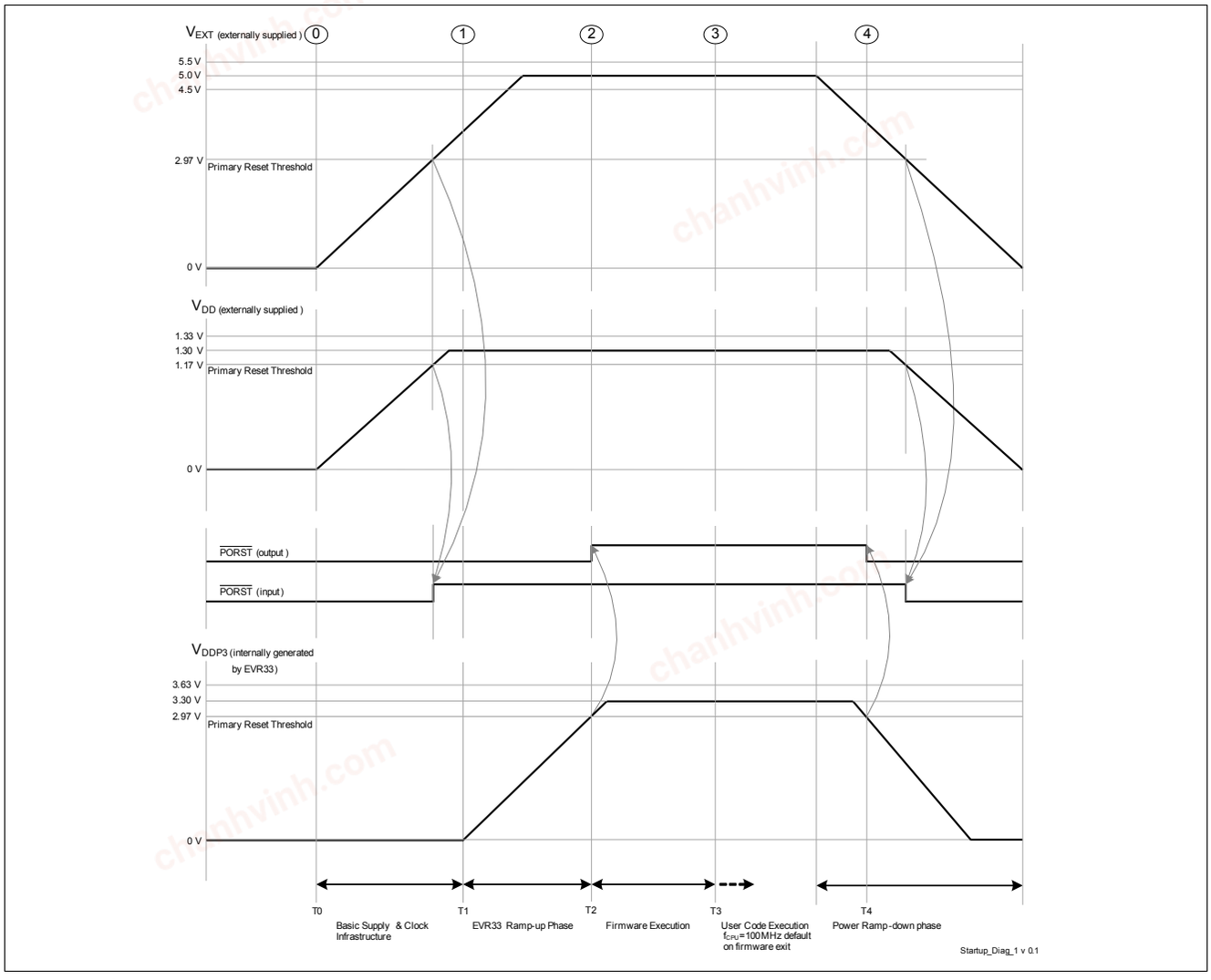



**Figure 3-3 External Supply Mode - 5 V and 1.3 V externally supplied**

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### 3.15.2 Single Supply Mode

5 V single supply mode. 1.3 V & 3.3 V are generated internally by EVR13 & EVR33.

- The rate at which current is drawn from the external regulator (dIEXT /dt) is limited in the Start-up phase to a maximum of 50 mA/100 us.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when atleast one among the three supply domains (1.3 V, 3.3 V or 5 V) violate their primary under-voltage reset thresholds.The PORST (output) is deasserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available.
- The power sequence as shown in **Figure 3-4** is enumerated below
  - T1 refers to the point in time when basic supply and clock infrastructure is available as the external supply ramps up. The supply mode is evaluated based on the HWCFG [0:2] pins and consequently a soft start of EVR13 and EVR33 regulators are initiated.
  - T2 refers to the point in time when all supplies are above their primary reset thresholds. EVR13 and EVR33 regulators have ramped up. PORST (output) is deasserted and HWCFG [0:7] pins are latched on PORST rising edge. Firmware execution is initiated.
  - T3 refers to the point in time when Firmware execution is completed. User code execution starts with a default frequency of 100 MHz.
  - T4 refers to the point in time during the Ramp-down phase when atleast one of the externally provided or generated supplies (1.3 V, 3.3 V or 5 V) drop below their respective primary under-voltage reset thresholds.

Please note that there is no special requirements for $\overline{\text{PORST}}$ slew rates.

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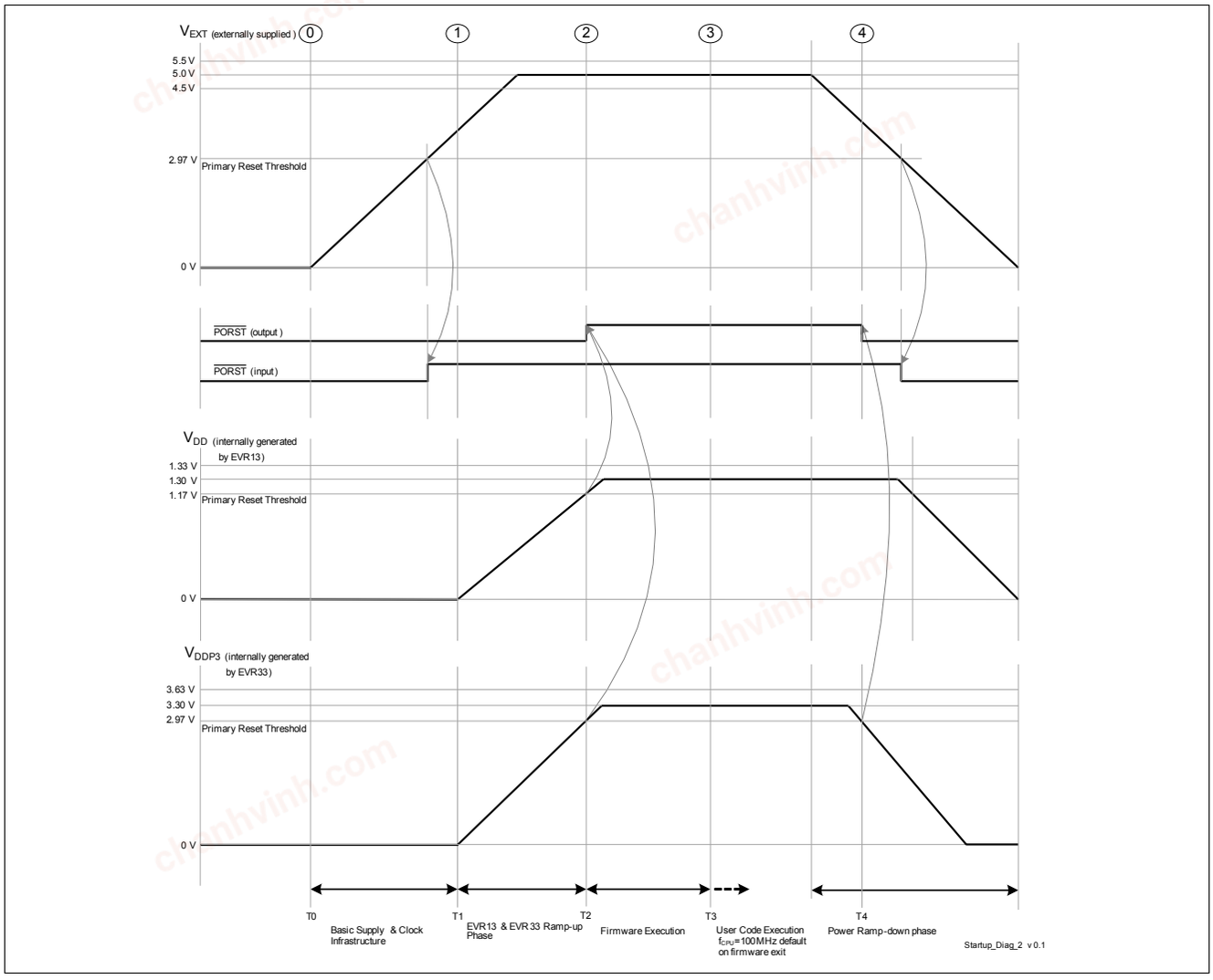



**Figure 3-4 Single Supply Mode - 5 V single supply**

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### 3.15.3 External Supply Mode

All supplies, namely 5 V, 3.3 V & 1.3 V, are externally supplied.

- External supplies VEXT ,, VDDP3 & VDD may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s).
- The rate at which current is drawn from the external regulator (dIEXT /dt, dIDD /dt or dIDDP3 /dt) is limited in the Start-up phase to a maximum of 50 mA/100 us.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when atleast one among the three supply domains (1.3 V, 3.3 V or 5 V) violate their primary under-voltage reset thresholds.The PORST (output) is deasserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available.
- The power sequence as shown in **Figure 3-5** is enumerated below
  - T1 refers to the point in time when all supplies are above their primary reset thresholds and basic clock infrastructure is available. The supply mode is evaluated based on the HWCFG [0:2] pins. PORST (output) is deasserted and HWCFG [0:7] pins are latched on PORST rising edge. Firmware execution is initiated.
  - T2 refers to the point in time when Firmware execution is completed. User code execution starts with a default frequency of 100 MHz.
  - T3 refers to the point in time during the Ramp-down phase when atleast one of the externally provided supplies (1.3 V, 3.3 V or 5 V) drop below their respective primary under-voltage reset thresholds.

Please note that there is no special requirements for $\overline{\text{PORST}}$ slew rates.

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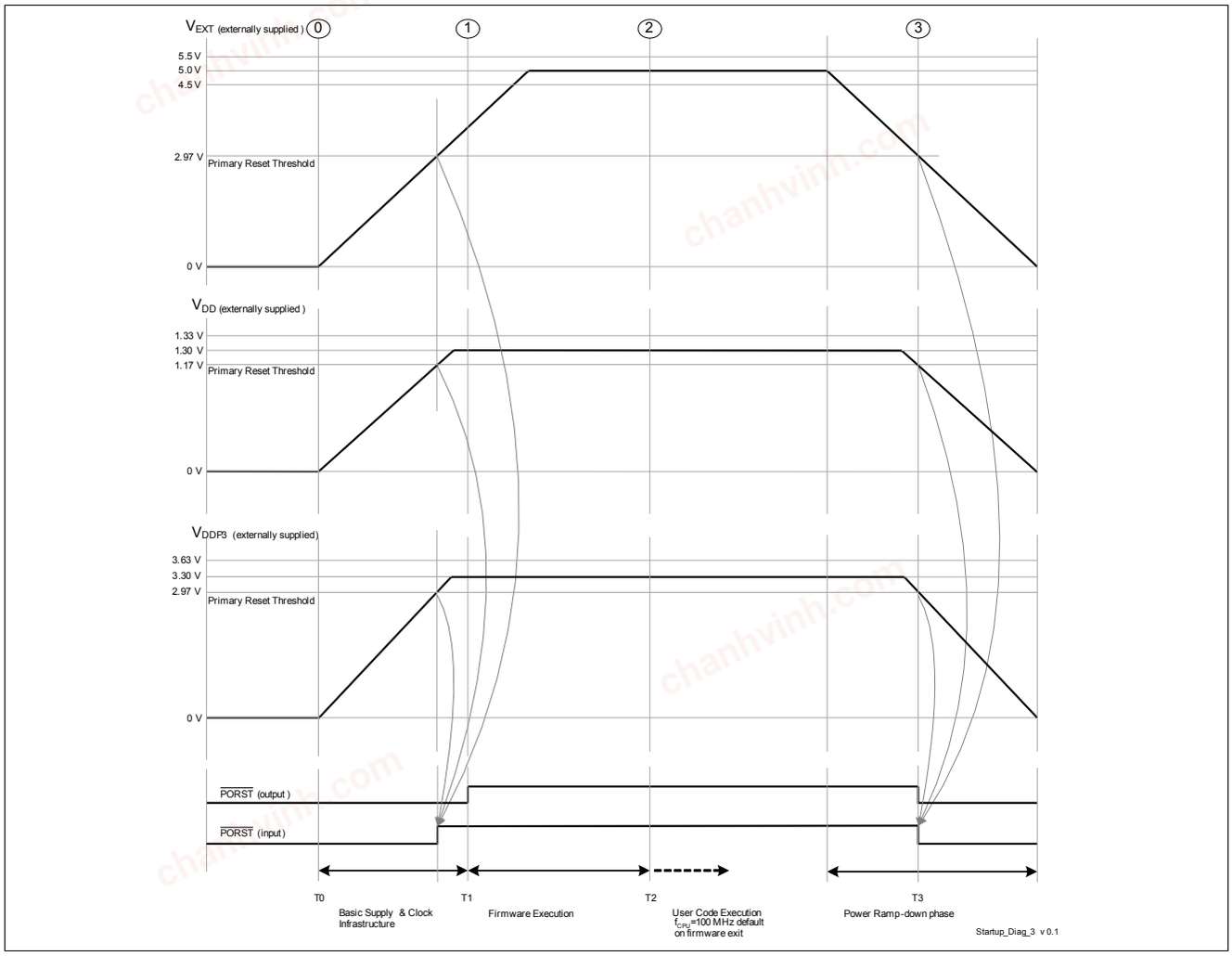



**Figure 3-5 External Supply Mode - 5 V, 3.3 V & 1.3 V externally supplied**

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### 3.15.4 Single Supply Mode

3.3 V single supply mode. 1.3 V is generated internally by EVR13.

- The rate at which current is drawn from the external regulator (dIEXT /dt) is limited in the Start-up phase to a maximum of 50 mA/100 us.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when atleast one among the three supply domains (1.3 V or 3.3 V) violate their primary under-voltage reset thresholds.The PORST (output) is deasserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available.
- The power sequence as shown in **Figure 3-6** is enumerated below
  - T1 refers to the point in time when basic supply and clock infrastructure is available as the external supply ramps up. The supply mode is evaluated based on the HWCFG [0:2] pins and consequently a soft start of EVR13 regulator is initiated.
  - T2 refers to the point in time when all supplies are above their primary reset thresholds. EVR13 regulator has ramped up. PORST (output) is deasserted and HWCFG [0:7] pins are latched on PORST rising edge. Firmware execution is initiated.
  - T3 refers to the point in time when Firmware execution is completed. User code execution starts with a default frequency of 100 MHz.
  - T4 refers to the point in time during the Ramp-down phase when atleast one of the externally provided or generated supplies (1.3 V or 3.3 V) drop below their respective primary under-voltage reset thresholds.

Please note that there is no special requirements for $\overline{\text{PORST}}$ slew rates.

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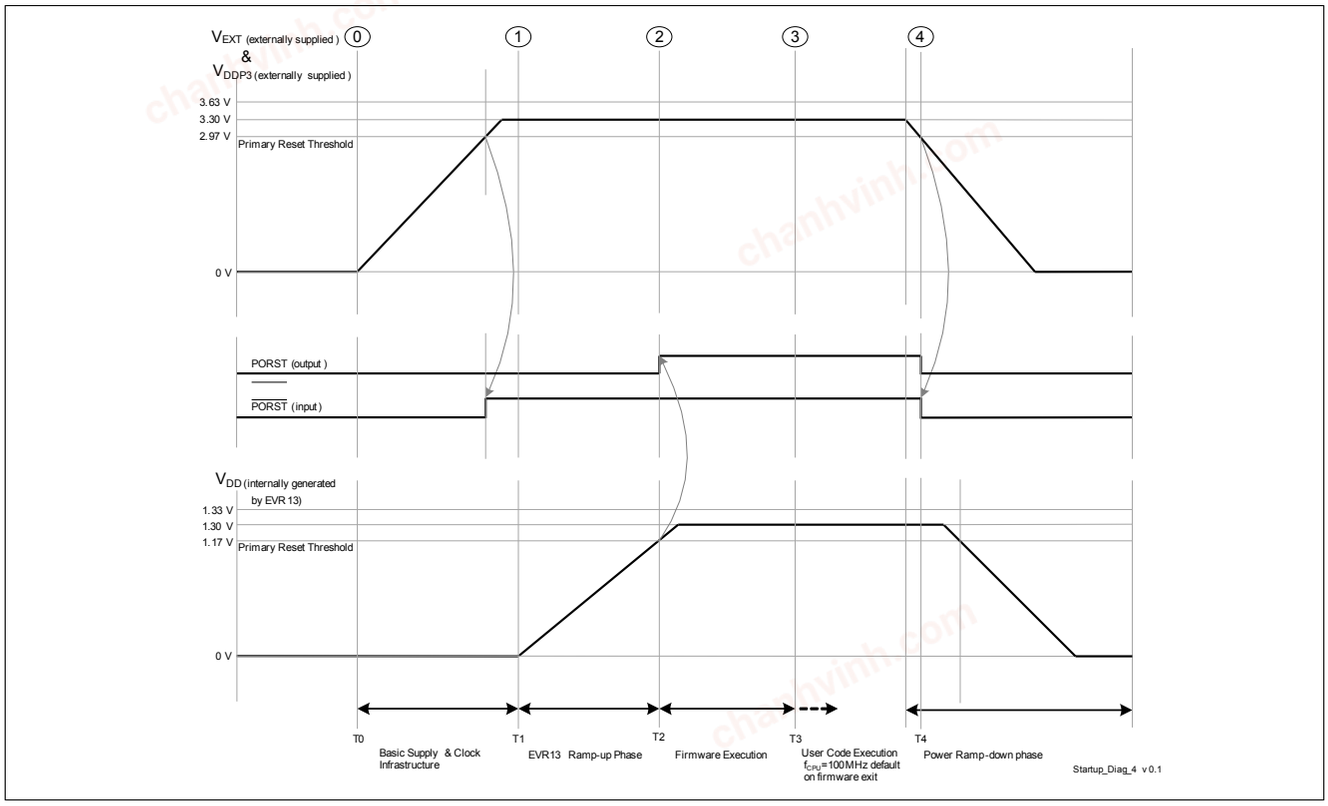



**Figure 3-6 Single Supply Mode - 3.3 V single supply**

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## 3.16 Reset Timing

**Table 3-35 Reset Timings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Application Reset Boot Time [1] | $t_B$ CC | - | - | 350 [2] | µs | operating with max. frequencies. |
| System Reset Boot Time | $t_{BS}$ CC | - | - | 1 | ms | |
| Power on Reset Boot Time [3] | $t_{BP}$ CC | - | - | 2.5 [2] | ms | $dV/dT$=1$V/ms$. including EVR ramp-up and Firmware execution time |
| | | - | - | 1.11 [2] | ms | Firmware execution time; without EVR operation (external supply only) |
| Minimum PORST hold time incase of power fail event issued by EVR primary monitor | $t_{EVRPOR}$ CC | 10 | - | - | µs | |
| EVR start-up or ramp-up time | $t_{EVRstartup}$ CC | - | - | 1 | ms | $dV/dT$=1$V/ms$. EVR13 and EVR33 active |
| Minimum PORST active hold time after power supplies are stable at operating levels [4] | $t_{POA}$ CC | 1 | - | - | ms | |
| Configurable PORST digital filter delay in addition to analog pad filter delay | $t_{PORSTDF}$ CC | 600 | - | 1200 | ns | |
| HWCFG pins hold time from ESR0 rising edge | $t_{HDH}$ CC | 16 / $f_{SPB}$ | - | - | ns | |
| HWCFG pins setup time to ESR0 rising edge | $t_{HDS}$ CC | 0 | - | - | ns | |
| Ports inactive after ESR0 reset active | $t_{PI}$ CC | - | - | 8/$f_{SPB}$ | ns | |
| Ports inactive after PORST reset active [5] | $t_{PIP}$ CC | - | - | 150 | ns | |
| Hold time from PORST rising edge | $t_{POH}$ SR | 150 | - | - | ns | |
| Setup time to PORST rising edge | $t_{POS}$ SR | 0 | - | - | ns | |

1) The duration of the boot time is defined between the rising edge of the internal application reset and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

2) The timing values assumes programmed BMI with ESR0CNT inactive.

3) The duration of the boot time is defined by all external supply voltages are inside there operation condictions and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

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4) The regulator that supplies $V_{EXT}$ should ensure that $V_{EXT}$ is in the operational region before PORST is externally released by the regulator. Incase of 5V nominal supply, it should be ensured that $V_{EXT}$ > 4V before PORST is released. Incase of 3.3V nominal supply , it should be ensured that $V_{EXT}$ > 3V before PORST is released. The additional minimum PORST hold time is required as an additional mechanism to avoid consecutive PORST toggling owing to slow supply slopes or residual supply ramp-ups. It is also required to activate external PORST atleast 100us before power-fail is recognised to avoid consecutive PORST toggling on a power fail event.
5) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.

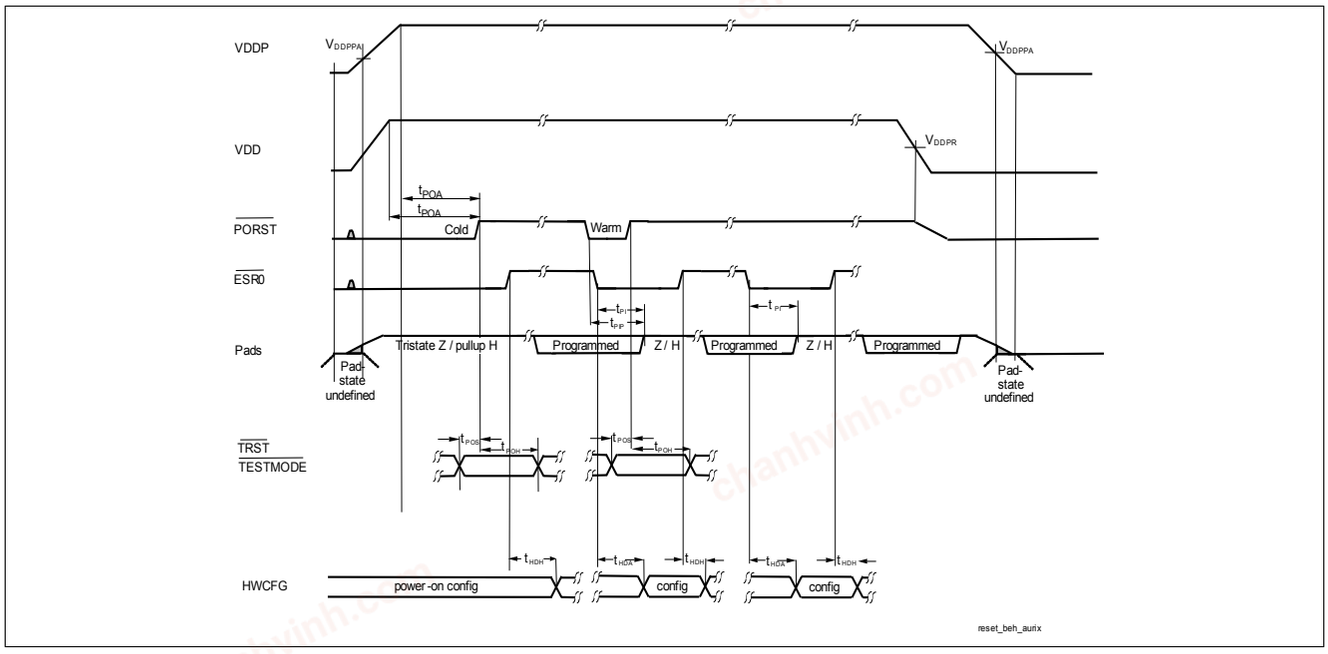



**Figure 3-7 Power, Pad and Reset Timing**

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## 3.17 EVR

**Table 3-36 3.3V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input voltage range [1] | $V_{IN}$ SR | 4 | - | 5.50 | V | pass device=on chip |
| Output voltage operational range including load/line regulation and aging incase of LDO regulator | $V_{OUT}$ CC | 2.97 | 3.3 | 3.63 | V | pass device=on chip |
| Output $V_{DDx3}$ static voltage accuracy after trimming and aging without dynamic load/line Regulation incase of LDO regulator. | $V_{OUTT}$ CC | 3.225 | 3.3 | 3.375 | V | pass device=on chip |
| Output buffer capacitance on $V_{OUT}$ [2] | $C_{OUT}$ CC | - | 1 | - | µF | pass device=on chip |
| Primary Undervoltage Reset threshold for $V_{DDx3}$ [3] | $V_{RST33}$ CC | - | - | 3.0 | V | by reset release before EVR trimming on supply ramp-up. |
| Startup time | $t_{STR}$ CC | - | - | 1000 | µs | Only EVR33 active. ; pass device=on chip |
| External $V_{IN}$ supply ramp [4] | *dVin/dT* SR | - | 1 | 50 | V/ms | pass device=on chip |
| Load step response | *dVout/dIout* CC | - | - | 240 | mV | *dI*=-70*mA*/20*ns*; *Tsettle*=20*us*; pass device=on chip |
| | | -240 | - | - | mV | *dI*=50*mA*/20*ns*; *Tsettle*=100*us*; pass device=on chip |
| Line step response | *dVout/dVin* CC | -20 | - | 20 | mV | *dV/dT*=1*V/ms*; pass device=on chip |

1) A maximum pass device dropout voltage of 700mV is included in the minimum input voltage to ensure optimal pass device operation.
2) It is recommended to select a capacitor with ESR less than 50 mOhm (0.5MHz - 10 MHz). It is also recommended that the resistance of the supply trace from the pin to the EVR output capacitor is less than 100 mOhm.
3) The reset release on supply ramp-up is delayed by a time duration 20-40 us after reaching undervoltage reset threshold. This serves as a time hysteresis to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. The reset limit of 2,97V at pin is for the case with 3.3V generated internally from EVR33. In case the 3.3V supply is provided externally, the bondwire drop will cause a reset at a higher voltage of 3.0V at the $V_{DDP3}$ pin.
4) EVR robust against residual voltage ramp-up starting between 0-1 V.

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**Table 3-37 1.3V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input voltage range [1] | $V_{IN}$ SR | 2.97 | - | 5.5 | V | pass device=off chip |
| Output voltage operational range including load/line regulation and aging incase of LDO regulator | $V_{OUT}$ CC | 1.17 | 1.3 | 1.43 | V | pass device=off chip |
| Output $V_{DD}$ static voltage accuracy after trimming without dynamic load/line regulation with aging incase of LDO regulator. | $V_{OUTT}$ CC | 1.275 | 1.3 | 1.325 | V | pass device=off chip |
| Output buffer capacitance on $V_{OUT}$ [2] | $C_{OUT}$ CC | 3 | 4.7 | 6.3 | µF | pass device=off chip |
| Primary undervoltage reset threshold for $V_{DD}$ [3] | $V_{RST13}$ CC | - | - | 1.17 | V | by reset release before EVR trimming on supply ramp-up. pass device=off chip |
| Startup time | $t_{STR}$ CC | - | - | 1000 | µs | pass device=off chip. Only EVR13 active. |
| External $V_{IN}$ supply ramp [4] | $dVin/dT$ SR | - | 1 | 50 | V/ms | pass device=off chip |
| Load step response | $dVout/dIout$ CC | - | - | 100 | mV | $dI$=-150$mA$; $Tsettle$=20$\mu s$; pass device=off chip |
| | | -100 | - | - | mV | $dI$=100$mA$; $Tsettle$=20$\mu s$; pass device=off chip |
| Line step response | $dVout/dVin$ CC | -10 | - | 10 | mV | $dV/dT$=1$V/ms$; pass device=off chip |

1) A maximum pass device dropout voltage of 700mV is included in the minimum input voltage to ensure optimal pass device operation.

2) It is recommended to select a capacitor with ESR less than 50 mOhm (0.5MHz - 10 MHz). It is also recommended that the resistance of the supply trace from the pin to the EVR output capacitor is less than 100 mOhm.

3) The reset release on supply ramp-up is delayed by a time duration 30-60 µs after reaching undervoltage reset threshold. This serves as a time hysteresis to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released.

4) EVR robust against residual voltage ramp-up starting between 0-1 V.

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**Table 3-38 Supply Monitoring**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{EXT}$ primary undervoltage monitor accuracy after trimming [1] | $V_{EXTPRIUV}$ SR | 2.86 | 2.92 | 2.97 | V | $V_{EXT}$ = Undervoltage Reset Threshold |
| $V_{DDP3}$ primary undervoltage monitor accuracy after trimming [1] | $V_{DDP3PRIUV}$ SR | 2.86 | 2.90 | 2.97 | V | $V_{DDP3}$ = Undervoltage Reset Threshold |
| $V_{DD}$ primary undervoltage monitor accuracy after trimming [1] | $V_{DDPRIUV}$ SR | 1.13 | 1.15 | 1.17 | V | $V_{DD}$ = Undervoltage Reset Threshold |
| $V_{EXT}$ secondary supply monitor accuracy | $V_{EXTMON}$ CC | 4.9 | 5.0 | 5.1 | V | SWDxxVAL $V_{EXT}$ monitoring threshold=5V=DBh |
| $V_{DDP3}$ secondary supply monitor accuracy | $V_{DDP3MON}$ CC | 3.23 | 3.30 | 3.37 | V | EVR33xxVAL $V_{DDP3}$ monitoring threshold=3.3V=91h |
| $V_{DD}$ secondary supply monitor accuracy | $V_{DDMON}$ CC | 1.27 | 1.30 | 1.33 | V | EVR13xxVAL $V_{DD}$ monitoring threshold=1.3V=E4h |
| EVR primary and secondary monitor measurement latency for a new supply value | $t_{EVRMON}$ CC | - | - | 1.8 | µs | after trimming |

1) The monitor tolerances constitute the inherent variation of the bandgap and ADC over process, voltage and temperature operational ranges. The xxxPRIUV parameters are device individually tested in production with ±1% tolerance about the min and max xxxPRIUV limits.

**Table 3-39 EVR13 SMPS External components**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| External output capacitor value [1] | $C_{OUTDC}$ SR | 15.4 | 22 | 29.7 | µF | $I_{DDDC}$=1A |
| | | 6.5 | 10 | 13.5 | µF | $I_{DDDC}$=400mA |
| External output capacitor ESR | $C_{DC_ESR}$ SR | - | - | 50 | mOhm | $f$≥0.5MHz ; $f$≤10MHz |
| | | - | - | 100 | Ohm | $f$=10Hz |
| External input capacitor value [1] | $C_{IN}$ SR | 6.5 | 10 | 13.5 | µF | $I_{DDDC}$=1A |
| | | 4.42 | 6.8 | 9.18 | µF | $I_{DDDC}$=400mA |
| External input capacitor ESR | $C_{IN_ESR}$ SR | - | - | 50 | mOhm | $f$≥0.5MHz ; $f$≤10MHz |
| | | - | - | 100 | Ohm | $f$=100Hz |
| External inductor value [2] | $L_{DC}$ SR | 2.31 | 3.3 | 4.29 | µH | $f_{DCDC}$=1.5MHz |
| | | 3.29 | 4.7 | 6.11 | µH | $f_{DCDC}$=1MHz |
| External inductor ESR | $L_{DC_ESR}$ SR | - | - | 0.2 | Ohm | |
| P + N-channel MOSFET logic level | $V_{LL}$ SR | - | - | 2.5 | V | |

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**Table 3-39 EVR13 SMPS External components** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| P + N-channel MOSFET drain source breakdown voltage | $\|V_{BR_DS}\|$ SR | - | - | 7 | V | |
| P + N-channel MOSFET drain source ON-state resistance | $R_{ON}$ SR | - | - | 150 | mOhm | $I_{DDDC}$=1A;$V_{GS}$=2.5$V$ ; $T_A$=25°$C$ |
| | | - | - | 200 | mOhm | $I_{DDDC}$=400mA;$V_{GS}$=2.5 $V$ ; $T_A$=25°$C$ |
| P + N-channel MOSFET Gate Charge | $Q_{ac}$ SR | - | 4 | - | nC | $I_{DDDC}$=1A; MOS-$V_{GS}$=5V |
| | | - | 8 | - | nC | $I_{DDDC}$=400mA; MOS-$V_{GS}$=5V |
| External MOSFET commutation time | $t_c$ SR | 10 | 30 | 40 | ns | configurable |
| N-channel MOSFET reverse diode forward voltage | $V_{RDN}$ SR | - | 0.8 | - | V | |

1) Capacitor min-max range represent typical ±35% tolerance including DC bias effect. The trace resistance from the capacitor to the supply or ground rail should be limited to 25 mOhm.

2) External inductor min-max range represent typical ±30% tolerance at a DC bias current of 100mA.

**Table 3-40 EVR13 SMPS**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input $V_{EXT}$ Voltage range | $V_{IN}$ SR | 2.97 | - | 5.5 | V | |
| SMPS regulator output voltage range including load/line regulation and aging [1] | $V_{DDDC}$ CC | 1.17 | - | 1.43 | V | $V_{DD}$≥2.97V ; $V_{DD}$≤5.5V ; $I_{DDDC}$≥1mA ; $I_{DDDC}$≤1A |
| SMPS regulator static voltage output accuracy after trimming without dynamic load/line Regulation with aging. [2] | $V_{DDDCT}$ CC | 1.275 | 1.3 | 1.325 | V | $V_{DD}$≥2.97V ; $V_{DD}$≤5.5V ; $I_{DDDC}$≥1mA ; $I_{DDDC}$≤1A |
| Programmable switching frequency | $f_{DCDC}$ CC | 0.4 | - | 2.0 | MHz | |
| Switching frequency modulation spread | $\Delta f_{DCSPR}$ CC | - | - | 2% | MHz | |
| Maximum ripple at $I_{MAX}$ (peak-to-peak) [3] | $\Delta V_{DDDC}$ CC | - | - | 15 | mV | $V_{DD}$≥2.97V ; $V_{DD}$≤5.5V ; $I_{DDDC}$≥300mA ; $I_{DDDC}$≤1A |
| No load current consumption of SMPS regulator | $I_{DCNL}$ CC | - | 5 | 10 | mA | $f_{DCDC}$=1$MHz$ |

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**Table 3-40 EVR13 SMPS** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SMPS regulator load transient response | *dVout/dIout* CC | -25 | - | 25 | mV | $dI$ < 200$mA$ ; $f_{DCDC}$=1$MHz$; $t_r$=0.1µs; $t_f$=0.1µs; $V_{DDDC}$=1.3V |
| | | -65 | - | 65 | mV | $dI$ < 400$mA$ ; $f_{DCDC}$=1$MHz$; $t_r$=0.1µs; $t_f$=0.1µs; $V_{DDDC}$=1.3V |
| | | -130 | - | 130 | mV | $dI$ < 700$mA$ ; $f_{DCDC}$=1$MHz$; $t_r$=0.1µs; $t_f$=0.1µs; $V_{DDDC}$=1.3V |
| Maximum output current of the regulator | $I_{MAX}$ SR | - | - | 1 | A | limited by thermal constraints and component choice |
| SMPS regulator efficiency | $n_{DC}$ CC | - | 85 | - | % | $V_{IN}$=3.3$V$; $I_{DDDC}$=300$mA$; $f_{DCDC}$=1$MHz$ |
| | | - | 75 | - | % | $V_{IN}$=5$V$; $I_{DDDC}$=400$mA$; $f_{DCDC}$=1.5$MHz$ |
| | | - | 80 | - | % | $V_{IN}$=5$V$; $I_{DDDC}$=400$mA$; $f_{DCDC}$=1$MHz$ |

1) Incase of SMPS mode, It shall be ensured that the $V_{DD}$ output pin shall be connected on PCB level to all other $V_{DD}$ Input pins.
2) Incase of $f_{SRI}$ running with max frequency, it shall be ensured that the $V_{DD}$ operating range is limited to 1.235V upto 1.430V. The DCDC may be configured in this case with a nominal voltage of 1.33V±7.5%. The static accuracy and regulation parameter ranges remain also valid for this case.
3) If frequency spreading (SDFREQSPRD = 1) is activated, an additional ripple of 1% need to be considered.

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## 3.18 Phase Locked Loop (PLL)

**Table 3-41 PLL**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| PLL base frequency | $f_{PLLBASE}$ CC | 80 | 150 | 360 | MHz | |
| VCO frequency range | $f_{VCO}$ SR | 400 | - | 800 | MHz | |
| VCO Input frequency range | $f_{REF}$ CC | 8 | - | 24 | MHz | |
| Modulation Amplitude | $MA$ CC | 0 | - | 2 | % | |
| Peak Period jitter | $DP$ CC | -200 | - | 200 | ps | |
| Peak Accumulated Jitter | $D_{PP}$ CC | -5 | - | 5 | ns | without modulation |
| Total long term jitter | $J_{TOT}$ CC | - | - | 11.5 | ns | including modulation; MA ≤ 1% |
| System frequency deviation | $f_{SYSD}$ CC | - | - | 0.01 | % | with active modulation |
| Modulation variation frequency | $f_{MV}$ CC | 2 | 3.6 | 5.4 | MHz | |
| PLL lock-in time | $t_L$ CC | 11.5 | - | 200 | µs | |

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L$ = 20 pF with the maximum driver and sharp edge.*

*Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of $V_{PP}$ = 100 mV for noise frequencies below 300 KHz and $V_{PP}$ = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.*

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## 3.19 ERAY Phase Locked Loop (ERAY_PLL)

**Table 3-42 PLL_ERAY**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| PLL Base Frequency of the ERAY PLL | $f_{PLLBASE_ERAY}$ CC | 50 | 200 | 320 | MHz | |
| VCO frequency range of the ERAY PLL | $f_{VCO_ERAY}$ SR | 400 | - | 480 | MHz | |
| VCO input frequency of the ERAY PLL | $f_{REF}$ SR | 16 | - | 24 | MHz | |
| Accumulated_Jitter | $D_P$ CC | -0.5 | - | 0.5 | ns | |
| Accumulated jitter at SYSCLK pin | $D_{PP}$ CC | -0.8 | - | 0.8 | ns | |
| PLL lock-in time | $t_L$ CC | 5.6 | - | 200 | µs | |

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L$ = 20 pF with the maximum driver and sharp edge.*

*Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of $V_{PP}$ = 100 mV for noise frequencies below 300 KHz and $V_{PP}$ = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.*

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## 3.20 AC Specifications

All AC parameters are specified for the complette operating range defined in **Chapter 3.4** unless otherwise noted in colum Note / test Condition.

Unless otherwise noted in the figures the timings are defined with the following guidelines:

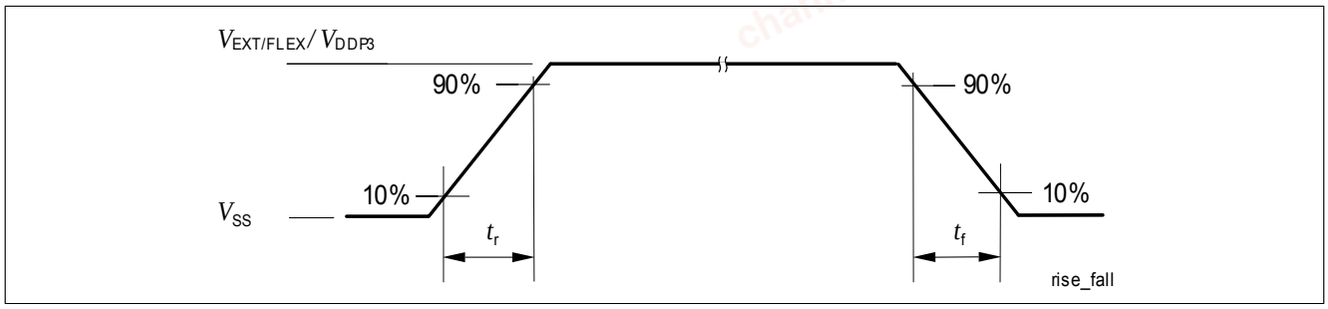



**Figure 3-8 Definition of rise / fall times**

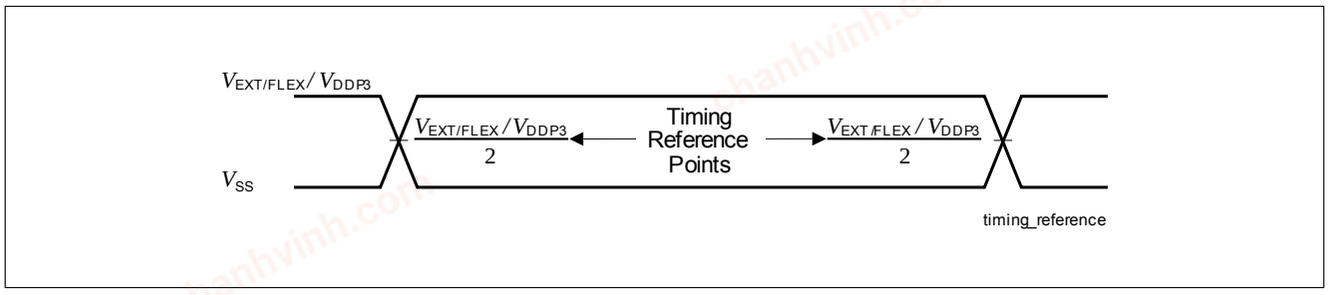



**Figure 3-9 Time Reference Point Definition**

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## 3.21 JTAG Parameters

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

**Table 3-43 JTAG**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TCK clock period | $t_1$ SR | 25 | - | - | ns | |
| TCK high time | $t_2$ SR | 10 | - | - | ns | |
| TCK low time | $t_3$ SR | 10 | - | - | ns | |
| TCK clock rise time | $t_4$ SR | - | - | 4 | ns | |
| TCK clock fall time | $t_5$ SR | - | - | 4 | ns | |
| TDI/TMS setup to TCK rising edge | $t_6$ SR | 6.0 | - | - | ns | |
| TDI/TMS hold after TCK rising edge | $t_7$ SR | 6.0 | - | - | ns | |
| TDO valid after TCK falling edge (propagation delay) [1] | $t_8$ CC | 3.0 | - | - | ns | $C_L$≤20pF |
| | | - | - | 16 | ns | $C_L$≤50pF |
| TDO hold after TCK falling edge [1] | $t_{18}$ CC | 2 | - | - | ns | |
| TDO high impedance to valid from TCK falling edge [1][2] | $t_9$ CC | - | - | 17.5 | ns | $C_L$≤50pF |
| TDO valid output to high impedance from TCK falling edge [1] | $t_{10}$ CC | - | - | 17 | ns | $C_L$≤50pF |

1) The falling edge on TCK is used to generate the TDO timing.
2) The setup time for TDO is given implicitly by the TCK cycle time.

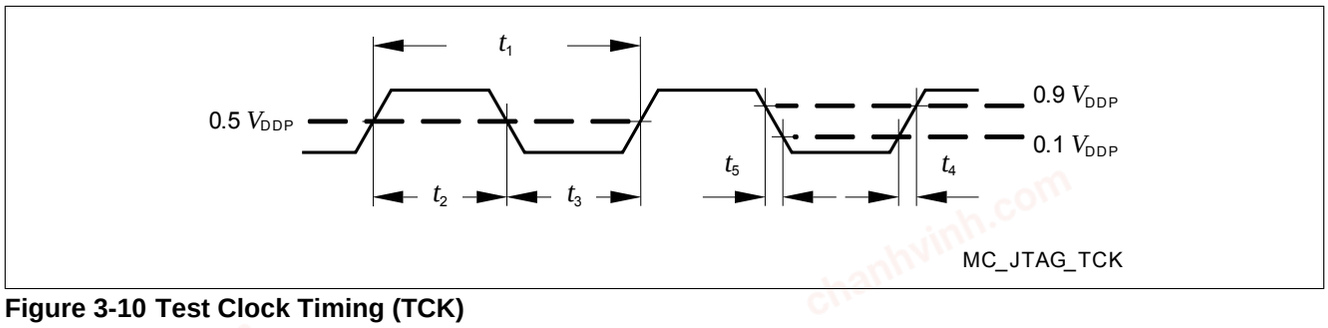



**Figure 3-10 Test Clock Timing (TCK)**

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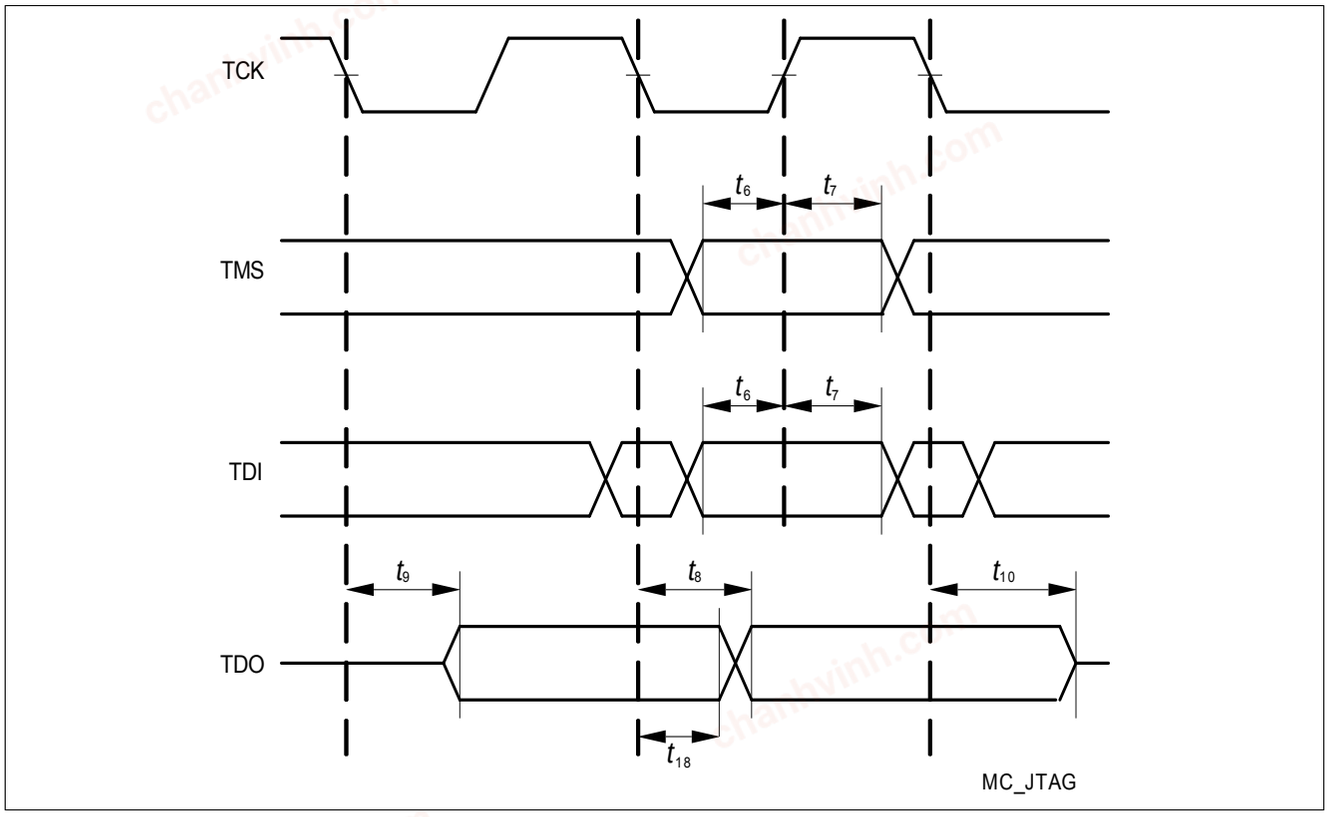



**Figure 3-11 JTAG Timing**

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## 3.22 DAP Parameters

The following parameters are applicable for communication through the DAP debug interface.

**Table 3-44 DAP**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DAP0 clock period | $t_{11}$ SR | 6.25 | - | - | ns | |
| DAP0 high time | $t_{12}$ SR | 2 | - | - | ns | |
| DAP0 low time | $t_{13}$ SR | 2 | - | - | ns | |
| DAP0 clock rise time | $t_{14}$ SR | - | - | 1 | ns | $f$=160MHz |
| | | - | - | 2 | ns | $f$=80MHz |
| DAP0 clock fall time | $t_{15}$ SR | - | - | 1 | ns | $f$=160MHz |
| | | - | - | 2 | ns | $f$=80MHz |
| DAP1 setup to DAP0 rising edge | $t_{16}$ SR | 4 | - | - | ns | |
| DAP1 hold after DAP0 rising edge | $t_{17}$ SR | 2 | - | - | ns | |
| DAP1 valid per DAP0 clock period [1] | $t_{19}$ CC | 3 | - | - | ns | $C_L$=20pF ; $f$=160MHz |
| | | 8 | - | - | ns | $C_L$=20pF ; $f$=80MHz |
| | | 10 | - | - | ns | $C_L$=50pF ; $f$=40MHz |

1) The Host has to find a suitable sampling point by analyzing the sync telegram response.

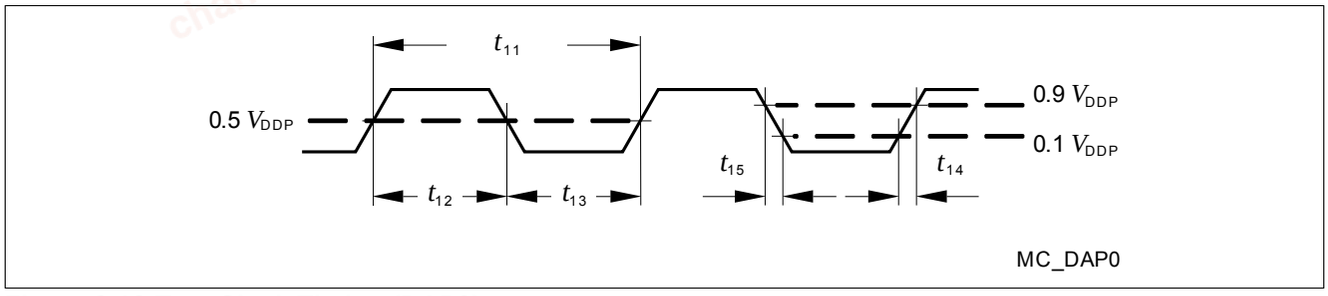



**Figure 3-12 Test Clock Timing (DAP0)**

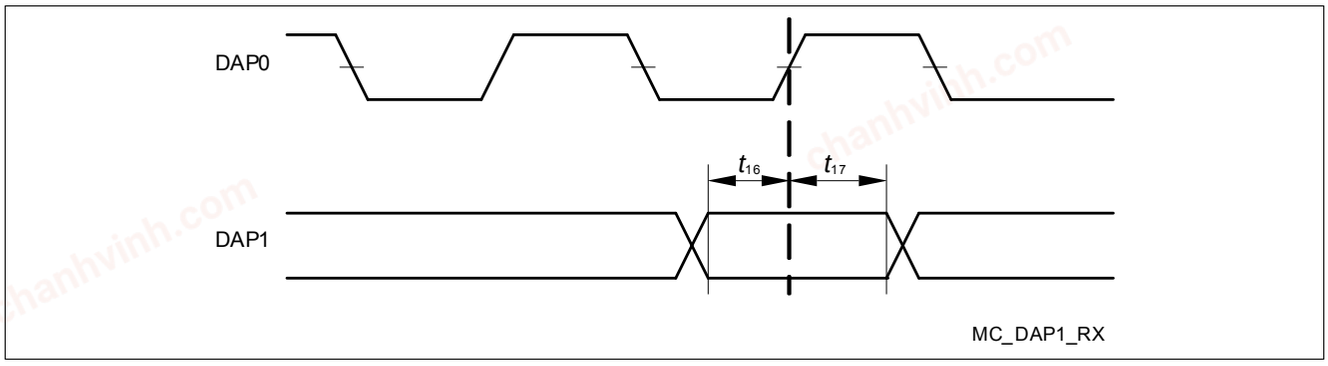



**Figure 3-13 DAP Timing Host to Device**

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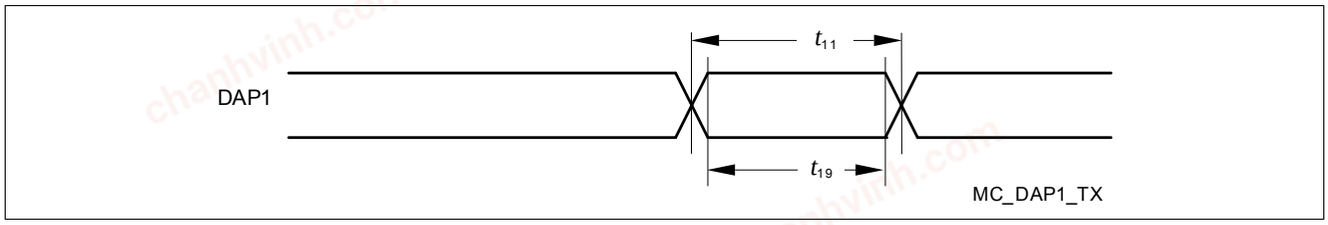



**Figure 3-14 DAP Timing Device to Host (DAP1 and DAP2 pins)**

*Note: The DAP1 and DAP2 device to host timing is individual for both pins. There is no guaranteed max. signal skew.*

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## 3.23 ASCLIN SPI Master Timing

This section defines the timings for the ASCLIN in the TC270 / TC275 / TC277, for 5V power supply.

*Note: Pad asymmetry is already included in the following timings.*

**Table 3-45 Master Mode MP+ss/MPRss output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 20 | - | - | ns | $C_L$=25pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -3 | - | 3 | ns | 0 < $C_L$ < 50pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -7 | - | 6 | ns | $C_L$=25pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | 5 | - | 35 | ns | $C_L$=25pF; pad used = LPm |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 28 | - | - | ns | $C_L$=25pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -6 | - | - | ns | $C_L$=25pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.

2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

**Table 3-46 Master Mode MP+sm/MPRsm output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 50 | - | - | ns | $C_L$=50pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -2 | - | 3+0.01 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -10 | - | 10 | ns | $C_L$=50pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | 5 | - | 35 | ns | $C_L$=50pF; pad used = LPm |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 50 | - | - | ns | $C_L$=50pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -10 | - | - | ns | $C_L$=50pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.

2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

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**Table 3-47 Master Mode MPss output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 20 | - | - | ns | $C_L$=25pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -2 | - | 3.5+0.035 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -7 | - | 6 | ns | $C_L$=25pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | -7 | - | 6 | ns | $C_L$=25pF |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 30 | - | - | ns | $C_L$=25pF, else |
| | | 33 [3] | - | - | ns | $C_L$=25pF, for P14.2, P14.4, and P15.1 |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -5 | - | - | ns | $C_L$=25pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
3) Please note that these pins didn't support the hystereses inactive feature.

**Table 3-48 Master Mode MPsm output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 100 | - | - | ns | $C_L$=50pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -3 | - | 4+0.04 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -11 | - | 10 | ns | $C_L$=50pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | -11 | - | 10 | ns | $C_L$=50pF |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 60 | - | - | ns | $C_L$=50pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -10 | - | - | ns | $C_L$=50pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

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**Table 3-49 Master Mode medium output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 200 | - | - | ns | $C_L$=50pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -8 | - | 4+0.04 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -20 | - | 15 | ns | $C_L$=50pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | -20 | - | 20 | ns | $C_L$=50pF |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 70 | - | - | ns | $C_L$=50pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -10 | - | - | ns | $C_L$=50pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

**Table 3-50 Master Mode weak output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 1000 | - | - | ns | $C_L$=50pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -30 | - | 30+0.15 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -75 | - | 75 | ns | $C_L$=50pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | -65 | - | 65 | ns | $C_L$=50pF |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 510 | - | - | ns | $C_L$=50pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -50 | - | - | ns | $C_L$=50pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

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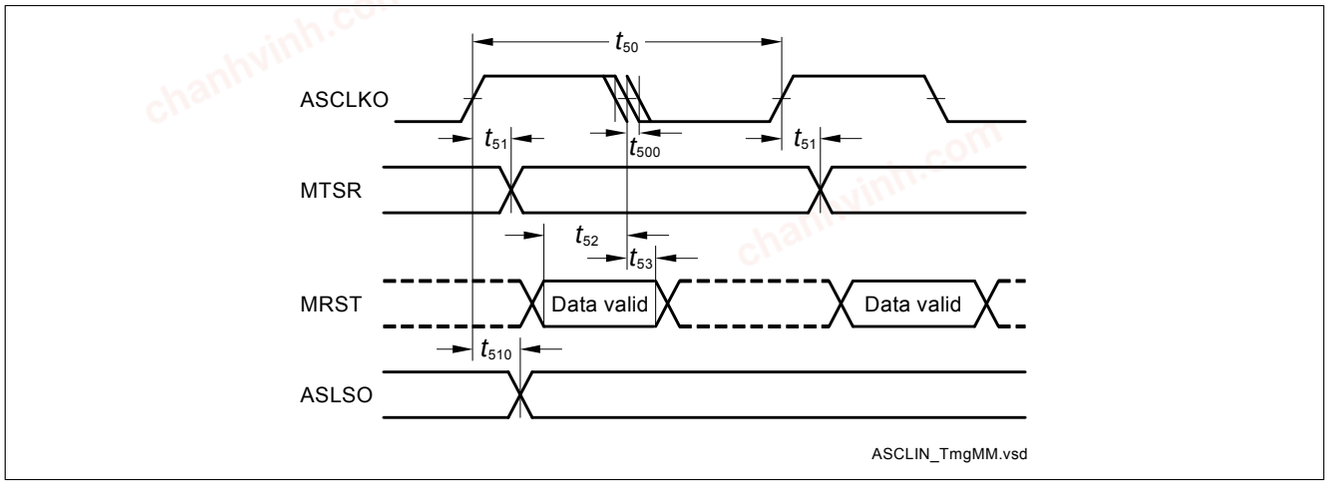



**Figure 3-15 ASCLIN SPI Master Timing**

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## 3.24 ASCLIN SPI Master Timing

This section defines the timings for the ASCLIN in the TC270 / TC275 / TC277, for 3.3V power supply, Medium Performance pads, strong sharp edge (MPss), $C_L$=25pF.

*Note: Pad asymmetry is already included in the following timings.*

**Table 3-51 Master Mode MP+ss/MPRss output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 40 | - | - | ns | $C_L$=25pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -5 | - | 5 | ns | 0 < $C_L$ < 50pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -12 | - | 12 | ns | $C_L$=25pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | 0 | - | 60 | ns | $C_L$=25pF; pad used = LPm |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 50 | - | - | ns | $C_L$=25pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -5 | - | - | ns | $C_L$=25pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.

2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

**Table 3-52 Master Mode MP+sm/MPRsm output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 100 | - | - | ns | $C_L$=50pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -3 | - | 7 | ns | 0 < $C_L$ < 200pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -17 | - | 17 | ns | $C_L$=50pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | 0 | - | 60 | ns | $C_L$=50pF; pad used = LPm |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 85 | - | - | ns | $C_L$=50pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -5 | - | - | ns | $C_L$=50pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.

2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

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**Table 3-53 Master Mode MPss output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 40 | - | - | ns | $C_L$=25pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -5 | - | 7+0.07 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -12 | - | 12 | ns | $C_L$=25pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | -12 | - | 12 | ns | $C_L$=25pF |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 50 | - | - | ns | $C_L$=25pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -5 | - | - | ns | $C_L$=25pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

**Table 3-54 Master Mode MPsm output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 200 | - | - | ns | $C_L$=50pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -5 | - | 9+0.06 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -19 | - | 17 | ns | $C_L$=50pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | -19 | - | 17 | ns | $C_L$=50pF |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 100 | - | - | ns | $C_L$=50pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -13 | - | - | ns | $C_L$=50pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

**Table 3-55 Master Mode medium output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 400 | - | - | ns | $C_L$=50pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -6-0.07 * $C_L$ | - | 6+0.07 * $C_L$ | ns | 0 < $C_L$ < 200pF |

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**Table 3-55 Master Mode medium output pads** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -33 | - | 25 | ns | $C_L$=50pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | -35 | - | 35 | ns | $C_L$=50pF |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 120 | - | - | ns | $C_L$=50pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -13 | - | - | ns | $C_L$=50pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.

2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

**Table 3-56 Master Mode weak output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 2000 | - | - | ns | $C_L$=50pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -110 | - | 150 | ns | 0 < $C_L$ < 200pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -170 | - | 170 | ns | $C_L$=50pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | -170 | - | 170 | ns | $C_L$=50pF |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 510 | - | - | ns | $C_L$=50pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | -40 | - | - | ns | $C_L$=50pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.

2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

**Table 3-57 Master Mode A2ss output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period [1] | $t_{50}$ CC | 20 | - | - | ns | $C_L$=50pF |
| Deviation from ideal duty cycle [2] | $t_{500}$ CC | -3 | - | 3 | ns | $C_L$=50pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -4 | - | 4 | ns | $C_L$=50pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | -5 | - | 4 | ns | $C_L$=50pF |

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**Table 3-57 Master Mode A2ss output pads** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 17 | - | - | ns | $C_L$=50pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | 0 | - | - | ns | $C_L$=50pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

**Table 3-58 Master Mode A2sm output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ASCLKO clock period 1) | $t_{50}$ CC | 40 | - | - | ns | $C_L$=50pF |
| Deviation from ideal duty cycle 2) | $t_{500}$ CC | -4 | - | 4 | ns | $C_L$=50pF |
| MTSR delay from ASCLKO shifting edge | $t_{51}$ CC | -8 | - | 6 | ns | $C_L$=50pF |
| ASLSOn delay from the first ASCLKO edge | $t_{510}$ CC | -8 | - | 9 | ns | $C_L$=50pF |
| MRST setup to ASCLKO latching edge | $t_{52}$ SR | 26 | - | - | ns | $C_L$=50pF |
| MRST hold from ASCLKO latching edge | $t_{53}$ SR | 0 | - | - | ns | $C_L$=50pF |

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

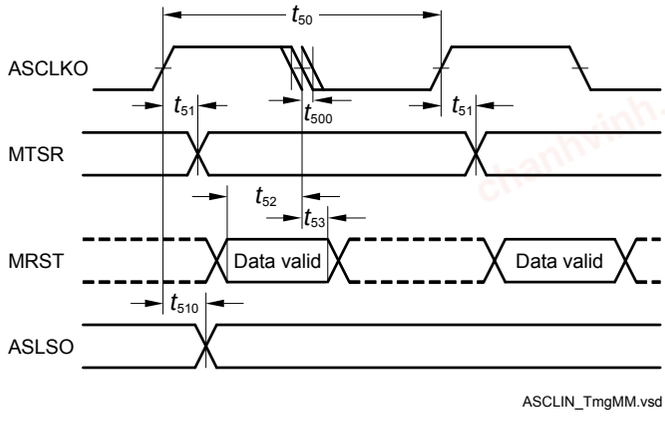



**Figure 3-16 ASCLIN SPI Master Timing**

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## 3.25 QSPI Timings, Master and Slave Mode

This section defines the timings for the QSPI in the TC270 / TC275 / TC277, for 5V pad power supply.
It is assumed that SCLKO, MTSR, and SLSO pads have the same pad settings:

- LVDSM output pads,LVDSH input pad, master mode, $C_L$=25pF
- Medium Performance Plus Pads (MP+):
  - strong sharp edge (MP+ss), $C_L$=25pF
  - strong medium edge (MP+sm), $C_L$=50pF
  - medium edge (MP+m), $C_L$=50pF
  - weak edge (MP+w), $C_L$=50pF
- Medium Performance Pads (MP):
  - strong sharp edge (MPss), $C_L$=25pF
  - strong medium edge (MPsm), $C_L$=50pF
- Medium and Low Performance Pads (MP/LP), the identical output strength settings:
  - medium edge (LP/MPm), $C_L$=50pF
  - weak edge (MPw), $C_L$=50pF

*Note: Pad asymmetry is already included in the following timings.*

**Table 3-59 Master Mode Timing, LVDSM output pads for data and clock**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 20 [2] | - | - | ns | $C_L$=25pF |
| Deviation from the ideal duty cycle [3] [4] | $t_{500}$ CC | -1 | - | 1 | ns | $C_L$=25pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -3 | - | 3 | ns | $C_L$=25pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | 0 | - | 30 | ns | $C_L$=25pF; MPsm |
| | | -5 | - | 7 | ns | $C_L$=25pF; MPss |
| | | -4 | - | 7 | ns | MP+ss; $C_L$=25pF |
| | | -1 | - | 15 | ns | MP+sm; $C_L$=25pF |
| MRST setup to SCLK latching edge [5] | $t_{52}$ SR | 19 [5] | - | - | ns | $C_L$=25pF; LVDSM 5V output and LVDSH 3.3V input |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -6 [5] | - | - | ns | $C_L$=25pF; LVDSM 5V output and LVDSH 3.3V input |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The capacitive load on the LVDS pins is differential, the capacitive load on the CMOS pins is single ended.
3) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
4) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
5) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

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**Table 3-60 Master Mode MP+ss/MPRss output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 20 | - | - | ns | $C_L$=25pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -3 | - | 3 | ns | 0 < $C_L$ < 50pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -7 | - | 6 | ns | $C_L$=25pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -7 | - | 6 | ns | $C_L$=25pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 27 [4][5] | - | - | ns | $C_L$=25pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -6 [4][5] | - | - | ns | $C_L$=25pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

**Table 3-61 Master Mode MP+sm/MPRsm output pads for data and clock**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 50 | - | - | ns | $C_L$=50pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -2 | - | 3+0.01 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -10 | - | 10 | ns | $C_L$=50pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -10 | - | 10 | ns | MP+sm; $C_L$=50pF |
| | | -13 | - | 1 | ns | MPss; $C_L$=50pF |
| | | 0 | - | 40 | ns | MP+m, MPm, LPm; $C_L$=50pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 50 [4][5] | - | - | ns | $C_L$=50pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -10 [4][5] | - | - | ns | $C_L$=50pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

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4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

**Table 3-62 Master Mode timing MPsm output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 100 | - | - | ns | $C_L$=50pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -3 | - | 4+0.04 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -11 | - | 10 | ns | $C_L$=50pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -11 | - | 10 | ns | $C_L$=50pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 60 [4][5] | - | - | ns | $C_L$=50pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -10 [4][5] | - | - | ns | $C_L$=50pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

**Table 3-63 Master Mode timing MPRm/MP+m/MPm/LPm output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 200 | - | - | ns | $C_L$=50pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -10 | - | 10+0.04 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -15 | - | 19 | ns | $C_L$=50pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -20 | - | 20 | ns | $C_L$=50pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 70 [4][5] | - | - | ns | $C_L$=50pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -10 [4][5] | - | - | ns | $C_L$=50pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

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4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

**Table 3-64 Master Mode Weak output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 1000 | - | - | ns | $C_L$=50pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -30 | - | 30+0.15 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -65 | - | 65 | ns | $C_L$=50pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -70 | - | 65 | ns | $C_L$=50pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 300 [4][5] | - | - | ns | $C_L$=50pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -40 [4][5] | - | - | ns | $C_L$=50pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

**Table 3-65 Slave mode timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLK clock period | $t_{54}$ SR | 4 x $T_{MAX}$ | - | - | ns | |
| SCLK duty cycle | $t_{55/t54}$ SR | 40 | - | 60 | % | |
| MTSR setup to SCLK latching edge | $t_{56}$ SR | 4 [1] | - | - | ns | Hystheresis Inactive |
| | | 5 [1] | - | - | ns | Input Level AL |
| | | 5 [1] | - | - | ns | Input Level TTL |
| MTSR hold from SCLK latching edge | $t_{57}$ SR | 3 [1] | - | - | ns | Hystheresis Inactive |
| | | 6 [1] | - | - | ns | Input Level AL |
| | | 9 [1] | - | - | ns | Input Level TTL |
| SLSI setup to first SCLK shift edge | $t_{58}$ SR | 5 [1] | - | - | ns | Hystheresis Inactive |
| | | 4 [1] | - | - | ns | Input Level AL |
| | | 8 [1] | - | - | ns | Input Level TTL |
| | | 6 | - | - | ns | Only for pin 15.1, AL |

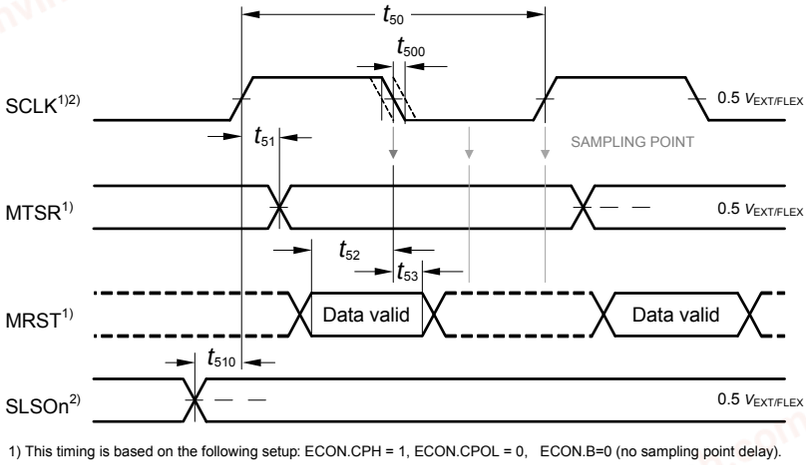
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**Table 3-65 Slave mode timing** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SLSI hold from last SCLK latching edge | $t_{59}$ SR | 3 [1] | - | - | ns | Hystheresis Inactive |
| | | 4 [1] | - | - | ns | Input Level AL |
| | | 8 [1] | - | - | ns | Input Level TTL |
| MRST delay from SCLK shift edge | $t_{60}$ CC | 10 | - | 70 | ns | MP+m/MPRm; $C_L$=50pF |
| | | 10 | - | 50 | ns | MP+sm/MPRsm; $C_L$=50pF |
| | | 5 | - | 30 | ns | MP+ss/MPRss; $C_L$=25pF |
| | | 40 | - | 300 | ns | MP+w/MPRw; $C_L$=50pF |
| | | 10 | - | 70 | ns | MPm/LPm; $C_L$=50pF |
| | | 10 | - | 55 | ns | MPsm; $C_L$=50pF |
| | | 5 | - | 30 | ns | MPss; $C_L$=25pF |
| | | 40 | - | 300 | ns | MPw/LPw; $C_L$=50pF |
| SLSI to valid data on MRST | $t_{61}$ SR | - | - | 5 | ns | |

1) Except pin P15.1.




1) This timing is based on the following setup: ECON.CPH = 1, ECON.CPOL = 0, ECON.B=0 (no sampling point delay).

2) t510 is the deviation from the ideal position configured with the leading delay, BACON.LPRE and BACON.LEAD > 0.

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**Figure 3-17 Master Mode Timing**

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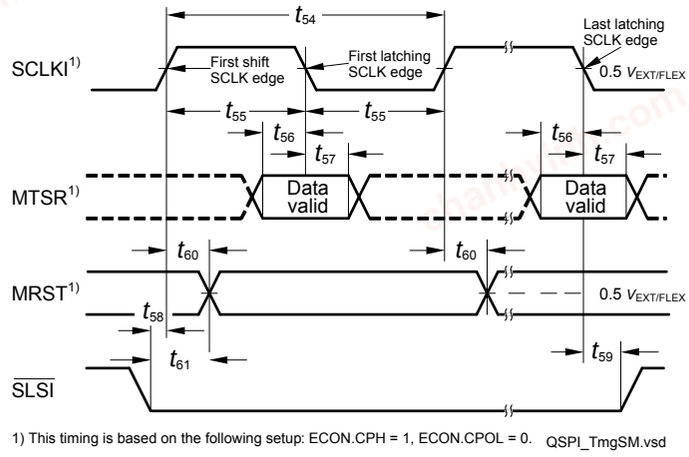



**Figure 3-18 Slave Mode Timing**

## 3.26 QSPI Timings, Master and Slave Mode

This section defines the timings for the QSPI in the TC270 / TC275 / TC277, for 3.3V pad power supply.
It is assumed that SCLKO, MTSR, and SLSO pads have the same pad settings:

- LVDSM output pads, LVDSH input pad, master mode, $C_L$=25pF
- Medium Performance Plus Pads (MP+):
  - strong sharp edge (MP+ss), $C_L$=25pF
  - strong medium edge (MP+sm), $C_L$=50pF
  - medium edge (MP+m), $C_L$=50pF
  - weak edge (MP+w), $C_L$=50pF
- Medium Performance Pads (MP):
  - strong sharp edge (MPss), $C_L$=25pF
  - strong medium edge (MPsm), $C_L$=50pF
- Medium and Low Performance Pads (MP/LP), the identical output strength settings:
  - medium edge (LP/MPm), $C_L$=50pF
  - weak edge (MPw), $C_L$=50pF

*Note: Pad asymmetry is already included in the following timings.*

**Table 3-66 Master Mode Timing, LVDSM output pads for data and clock**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1)] | $t_{50}$ CC | 20 | - | - | ns | $C_L$=25pF |
| Deviation from the ideal duty cycle [2) 3)] | $t_{500}$ CC | -2 | - | 2 | ns | $C_L$=25pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -5 | - | 5 | ns | $C_L$=25pF |

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**Table 3-66 Master Mode Timing, LVDSM output pads for data and clock** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -2 | - | 55 | ns | $C_L$=25pF; MPsm |
| | | -9 | - | 12 | ns | $C_L$=25pF; MPss |
| | | -7 | - | 12 | ns | MP+ss; $C_L$=25pF |
| | | -2 | - | 26 | ns | MP+sm; $C_L$=25pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 20 | - | - | ns | $C_L$=25pF; LVDSM 5V output and LVDSH 3.3V input |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -6 | - | - | ns | $C_L$=25pF; LVDSM 5V output and LVDSH 3.3V input |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

**Table 3-67 Master Mode MP+ss/MPRss output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 40 | - | - | ns | $C_L$=25pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -5 | - | 5 | ns | 0 < $C_L$ < 50pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -12 | - | 12 | ns | $C_L$=25pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -12 | - | 12 | ns | $C_L$=25pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 50 [4][5] | - | - | ns | $C_L$=25pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -6 [4][5] | - | - | ns | $C_L$=25pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

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**Table 3-68 Master Mode MP+sm/MPRsm output pads for data and clock**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 100 | - | - | ns | $C_L$=50pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -3 | - | 7 | ns | 0 < $C_L$ < 200pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -17 | - | 17 | ns | $C_L$=50pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -17 | - | 17 | ns | MP+sm; $C_L$=50pF |
| | | -22 | - | 2 | ns | MPss; $C_L$=50pF |
| | | 0 | - | 70 | ns | MP+m; MPm; LPm; $C_L$=50pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 85 [4][5] | - | - | ns | $C_L$=50pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -10 [4][5] | - | - | ns | $C_L$=50pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

**Table 3-69 Master Mode timing MPss output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 40 | - | - | ns | $C_L$=25pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -5 | - | 7+0.07 * $C_L$ | ns | $C_L$=25pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -10 | - | 10 | ns | $C_L$=25pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -10 | - | 10 | ns | $C_L$=25pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 50 [4][5] | - | - | ns | $C_L$=25pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -6 [4][5] | - | - | ns | $C_L$=25pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

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4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

**Table 3-70 Master Mode timing MPsm output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 200 | - | - | ns | $C_L$=50pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -5 | - | 9+0.06 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -19 | - | 19 | ns | $C_L$=50pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -19 | - | 17 | ns | $C_L$=50pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 100 [4][5] | - | - | ns | $C_L$=50pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -13 [4][5] | - | - | ns | $C_L$=50pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

**Table 3-71 Master Mode timing MPRm/MP+m/MPm/LPm output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 400 | - | - | ns | $C_L$=50pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -6-0.07 * $C_L$ | - | 6+0.07 * $C_L$ | ns | 0 < $C_L$ < 200pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -25 | - | 33 | ns | $C_L$=50pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -35 | - | 35 | ns | $C_L$=50pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 120 [4][5] | - | - | ns | $C_L$=50pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -13 [4][5] | - | - | ns | $C_L$=50pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

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4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

**Table 3-72 Master Mode Weak output pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLKO clock period [1] | $t_{50}$ CC | 2000 | - | - | ns | $C_L$=50pF |
| Deviation from the ideal duty cycle [2] [3] | $t_{500}$ CC | -110 | - | 110 | ns | 0 < $C_L$ < 200pF |
| MTSR delay from SCLKO shifting edge | $t_{51}$ CC | -170 | - | 170 | ns | $C_L$=50pF |
| SLSOn deviation from the ideal programmed position | $t_{510}$ CC | -170 | - | 170 | ns | $C_L$=50pF |
| MRST setup to SCLK latching edge [4] | $t_{52}$ SR | 510 [4][5] | - | - | ns | $C_L$=50pF |
| MRST hold from SCLK latching edge | $t_{53}$ SR | -40 [4][5] | - | - | ns | $C_L$=50pF |

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX}$ = 1 / $f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

**Table 3-73 Slave mode timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLK clock period | $t_{54}$ SR | 4 x $T_{MAX}$ | - | - | ns | |
| SCLK duty cycle | $t_{55/t54}$ SR | 40 | - | 60 | % | |
| MTSR setup to SCLK latching edge | $t_{56}$ SR | 7 [1] | - | - | ns | Hystheresis inactive |
| | | 9 [1] | - | - | ns | Input Level AL |
| | | 7 [1] | - | - | ns | Input Level TTL |
| MTSR hold from SCLK latching edge | $t_{57}$ SR | 5 [1] | - | - | ns | Hystheresis inactive |
| | | 11 [1] | - | - | ns | Input Level AL |
| | | 16 [1] | - | - | ns | Input Level TTL |
| SLSI setup to first SCLK shift edge | $t_{58}$ SR | 7 [1] | - | - | ns | Hystheresis inactive |
| | | 7 [1] | - | - | ns | Input Level AL |
| | | 14 [1] | - | - | ns | Input Level TTL |
| | | 11 | - | - | ns | Only for pin P15.1, AL |

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**Table 3-73 Slave mode timing** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SLSI hold from last SCLK latching edge | $t_{59}$ SR | 5 [1] | - | - | ns | Hystheresis inactive |
| | | 7 [1] | - | - | ns | Input Level AL |
| | | 14 [1] | - | - | ns | Input Level TTL |
| MRST delay from SCLK shift edge | $t_{60}$ CC | 13 | - | 120 | ns | MP+m/MPRm; $C_L$=50pF |
| | | 13 | - | 85 | ns | MP+sm/MPRsm; $C_L$=50pF |
| | | 6 | - | 50 | ns | MP+ss/MPRss; $C_L$=25pF |
| | | 70 | - | 500 | ns | MP+w/MPRw; $C_L$=50pF |
| | | 13 | - | 120 | ns | MPm/LPm; $C_L$=50pF |
| | | 13 | - | 100 | ns | MPsm; $C_L$=50pF |
| | | 6 | - | 52 | ns | MPss; $C_L$=25pF |
| | | 70 | - | 500 | ns | MPw/LPw; $C_L$=50pF |
| SLSI to valid data on MRST | $t_{61}$ SR | - | - | 9 | ns | |

1) Except pin P15.1

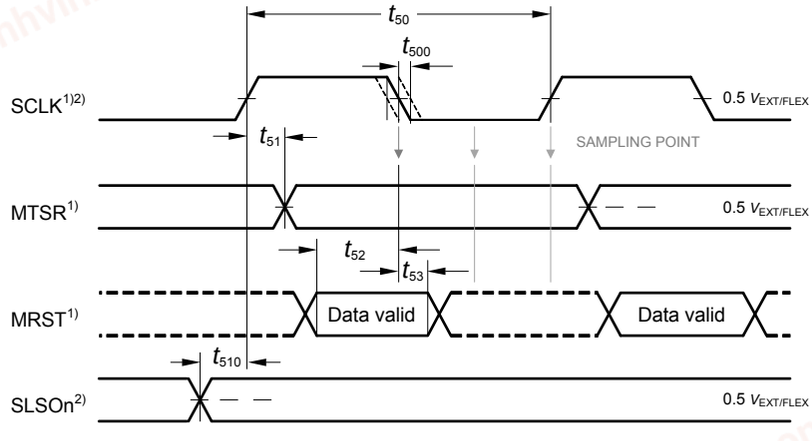
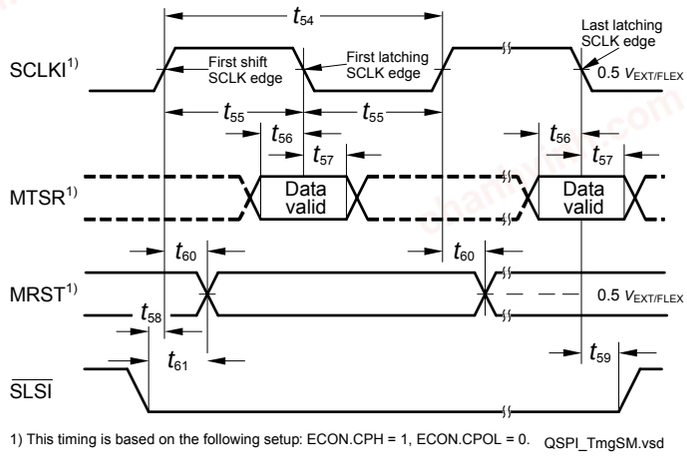



**Figure 3-19 Master Mode Timing**

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1) This timing is based on the following setup: ECON.CPH = 1, ECON.CPOL = 0. QSPI_TmgSM.vsd

**Figure 3-20 Slave Mode Timing**

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## 3.27 MSC Timing 5 V Operation

The following section defines the timings for 5V pad power supply.

*Note: Pad asymmetry is already included in the following timings.*

*Note: Load for LVDS pads are defined as differential loads in the following timings.*

**Table 3-74 LVDS clock/data (LVDS pads in LVDS mode)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLPx clock period [1] | $t_{40}$ CC | 2 * $T_A$ [2] [3] | - | - | ns | LVDSM; $C_L$=50pF |
| Deviation from ideal duty cycle [4] [5] | $t_{400}$ CC | -1 | - | 1 | ns | LVDSM; 0 < $C_L$ < 50pF |
| SOPx output delay [6] | $t_{44}$ CC | -3 | - | 4 | ns | LVDSM; $C_L$=50pF; option EN01 |
| | | -4 | - | 4.5 | ns | LVDSM; $C_L$=50pF; option EN01D |
| ENx output delay [6] | $t_{45}$ CC | -4 | - | 5 | ns | MP+ss/MPRss; option EN01; $C_L$=25pF |
| | | -3 | - | 7 | ns | MP+ss/MPRss; option EN01; $C_L$=50pF |
| | | -3 | - | 11 | ns | MP+sm/MPRsm; option EN01D; $C_L$=50pF |
| | | -2 | - | 9 | ns | MP+ss/MPRss; option EN23; $C_L$=25pF |
| | | -2 | - | 11 | ns | MP+ss/MPRss; option EN23; $C_L$=50pF |
| | | -3 | - | 11 | ns | MPss; option EN01; $C_L$=50pF |
| | | -7 | - | 2 | ns | MP+ss/MPRss; option EN01; $C_L$=0pF |
| | | -5 | - | 3 | ns | MP+sm/MPRsm; option EN01D; $C_L$=0pF |
| | | -4 | - | 5 | ns | MP+ss/MPRss; option EN23; $C_L$=0pF |
| | | -7 | - | 4 | ns | MPss; option EN01; $C_L$=0pF |
| SDI bit time | $t_{46}$ CC | 8 * $t_{MSC}$ | - | - | ns | Upstream Timing |
| SDI rise time [7] | $t_{48}$ SR | - | - | 200 | ns | Upstream Timing |
| SDI fall time [7] | $t_{49}$ SR | - | - | 200 | ns | Upstream Timing |

1) FCLP signal rise/fall times are the rise/fall times of the LVDSM pads, and the high/low times are min 1 * $T_A$.

2) $T_A$ depends on the clock source selected for baud rate generation in the ABRA block of the MSC.

3) The capacitive load on the LVDS pins is differential, the capacitive load on the CMOS pins is single ended.

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4) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted if the ABRA block is used.
5) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
6) From FCLP rising edge.
7) When using slow and asymmetrical edges, like in case of open drain upstream connection, the application must take care that the bit is long enough (the baud rate is low enough) so that under worst case conditions the three sampling points in the middle of the bit are not violated.

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### Timing Options for $t_{45}$

The wiring shown in the **Figure 3-21** provides three useful timing options for $t_{45}$. depending on the signals selected with the alternate output lines (ALT1 to ALT7) in the ports:

- EN01 - FCLN, SON, EN0, EN1 - $t_{45}$ reference timing
- EN01D - FCLND, SOND, EN0, EN1 - $t_{45}$ window shifted to the left
- EN23 - FCLN, SON, EN2, EN3 - $t_{45}$ window shifted to the right

The timings corresponding to EN01, EN01D, and EN23 are defined in the LVDS. In order to use the EN23 timings, the application should use the EN2 and EN3 outputs of the MSC module.

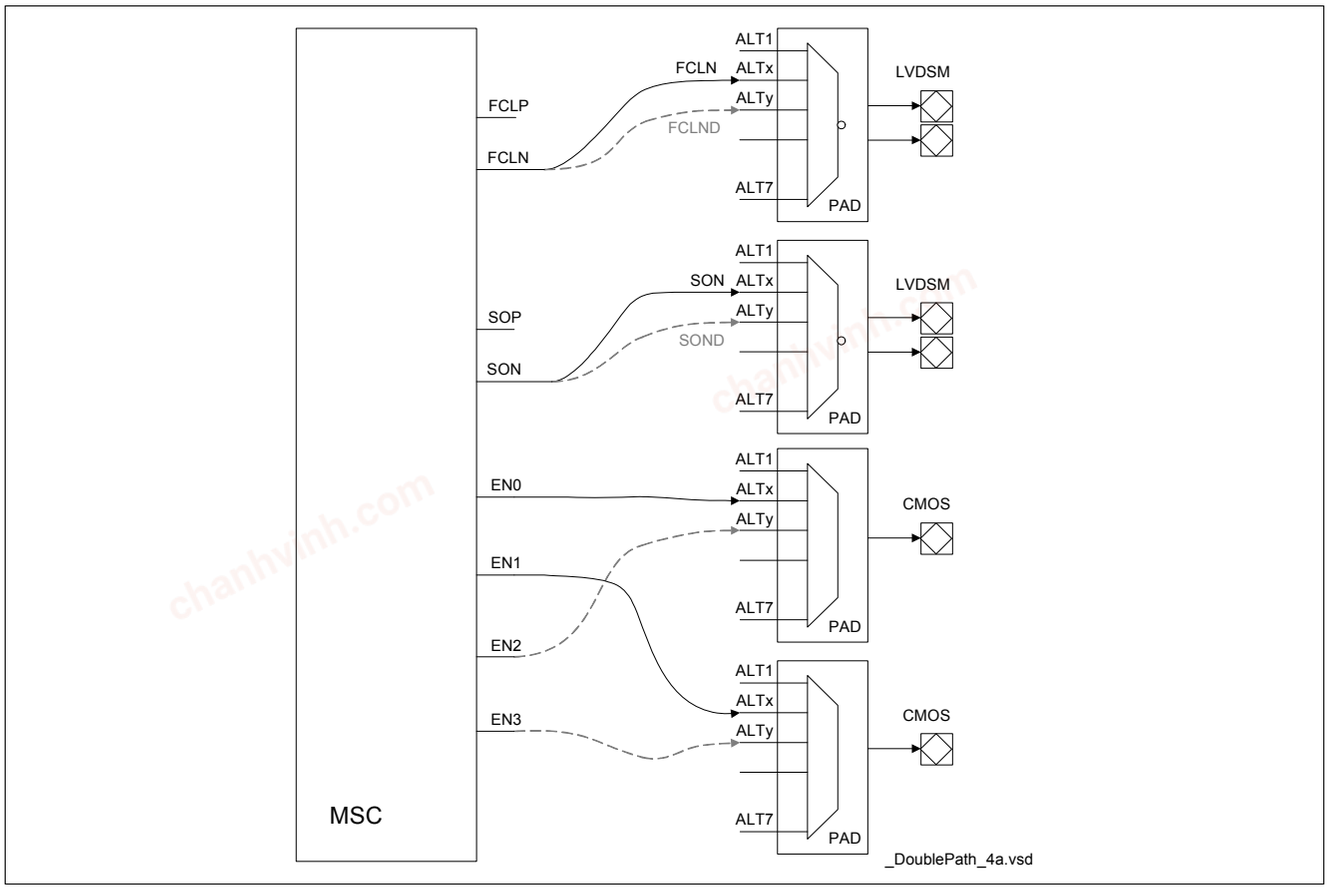



**Figure 3-21 Timing Options for $t_{45}$**

**Table 3-75 MPss clock/data (LVDS pads in CMOS mode, option EN01)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLPx clock period [1] | $t_{40}$ CC | 2 * $T_A$ [2] [3] | - | - | ns | MPss; $C_L$=50pF |
| Deviation from ideal duty cycle [4] [5] | $t_{400}$ CC | -2 | - | 6+0.035 * $C_L$ | ns | MPss; 0 < $C_L$ < 100pF |
| SOPx output delay [6] | $t_{44}$ CC | -4 | - | 7 | ns | MPss; $C_L$=50pF |

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**Table 3-75 MPss clock/data (LVDS pads in CMOS mode, option EN01)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ENx output delay [6] | $t_{45}$ CC | -5 | - | 7 | ns | MP+ss/MPRss; $C_L$=50pF |
| | | -2 | - | 15 | ns | MP+sm/MPRsm; $C_L$=50pF |
| | | -4 | - | 10 | ns | MPss; $C_L$=50pF |
| | | 0 | - | 30 | ns | MPsm; $C_L$=50pF; except pin P13.0 |
| | | 0 | - | 31 | ns | MPsm; $C_L$=50pF; pin P13.0 |
| | | 6 | - | 45 | ns | MPm/MP+m/MPRm; $C_L$=50pF |
| | | -11 | - | 2 | ns | MP+ss/MPRss; $C_L$=0pF |
| | | -4 | - | 7 | ns | MP+sm/MPRsm; $C_L$=0pF |
| | | -10 | - | 2 | ns | MPss; $C_L$=0pF |
| | | -1 | - | 16 | ns | MPsm; $C_L$=0pF |
| | | -2 | - | 18 | ns | MP+m/MPm/MPRm; $C_L$=0pF |
| SDI bit time | $t_{46}$ CC | 8 * $t_{MSC}$ | - | - | ns | Upstream Timing |
| SDI rise time [7] | $t_{48}$ SR | - | - | 200 | ns | Upstream Timing |
| SDI fall time [7] | $t_{49}$ SR | - | - | 200 | ns | Upstream Timing |

1) FCLP signal rise/fall times are the rise/fall times of the LVDSM pads, and the high/low times are min 1 * $T_A$.
2) $T_A$ depends on the clock source selected for baud rate generation in the ABRA block of the MSC.
3) FCLP signal high and low can be minimum 1 * $T_{MSC}$.
4) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted if the ABRA block is used.
5) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
6) From FCLP rising edge.
7) When using slow and asymmetrical edges, like in case of open drain upstream connection, the application must take care that the bit is long enough (the baud rate is low enough) so that under worst case conditions the three sampling points in the middle of the bit are not violated.

**Table 3-76 MP+sm/MPRsm clock/data**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLPx clock period [1] | $t_{40}$ CC | 2 * $T_A$ | - | - | ns | MP+sm/MPRsm; $C_L$=50pF |
| Deviation from ideal duty cycle [2] [3] | $t_{400}$ CC | -2 | - | 3+0.01 * $C_L$ | ns | MP+sm/MPRsm; 0 < $C_L$ < 200pF |
| SOPx output delay [4] | $t_{44}$ CC | -5 | - | 7 | ns | MP+sm; $C_L$=50pF |

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**Table 3-76 MP+sm/MPRsm clock/data** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ENx output delay 4) | $t_{45}$ CC | -13 | - | 2 5) | ns | MPss; $C_L$=50pF |
| | | -5 | - | 11 | ns | MP+sm/MPRsm; $C_L$=50pF |
| | | 1 | - | 24 | ns | MPsm; $C_L$=50pF |
| | | 4 | - | 37 | ns | MP+m/MPm/MPRm; $C_L$=50pF |
| | | -19 | - | -1 | ns | MPss; $C_L$=0pF |
| | | -13 | - | 2 | ns | MP+sm; $C_L$=0pF |
| | | -5 | - | 8 | ns | MPsm; $C_L$=0pF |
| | | -5 | - | 10 | ns | MPm/MP+m/MPRm; $C_L$=0pF |

1) FCLP signal rise/fall times are the rise/fall times of the LVDSM pads, and the high/low times are min 1 * $T_A$.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted if the ABRA block is used.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) From FCLP rising edge.
5) If EN1 is configured to P13.0 the max limt is increased by 0.5ns to 2.5ns.

**Table 3-77 MPm/MP+m/MPRm clock/data**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLPx clock period 1) | $t_{40}$ CC | 2 * $T_A$ | - | - | ns | MPm/MP+m/MPRm; $C_L$=50pF |
| Deviation from ideal duty cycle 2) 3) | $t_{400}$ CC | -8 | - | 15+0.04 * $C_L$ | ns | MPm/MP+m; 0 < $C_L$ < 200pF |
| SOPx output delay 4) | $t_{44}$ CC | -11 | - | 9 | ns | MPm/MP+m; $C_L$=50pF |
| ENx output delay 4) | $t_{45}$ CC | -15 | - | 11 | ns | MPm/MP+m/MPRm; $C_L$=50pF |
| | | -33 | - | -4 | ns | MPm/MP+m/MPRm; $C_L$=0pF |

1) FCLP signal rise/fall times are the rise/fall times of the LVDSM pads, and the high/low times are min 1 * $T_A$.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted if the ABRA block is used.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) From FCLP rising edge.

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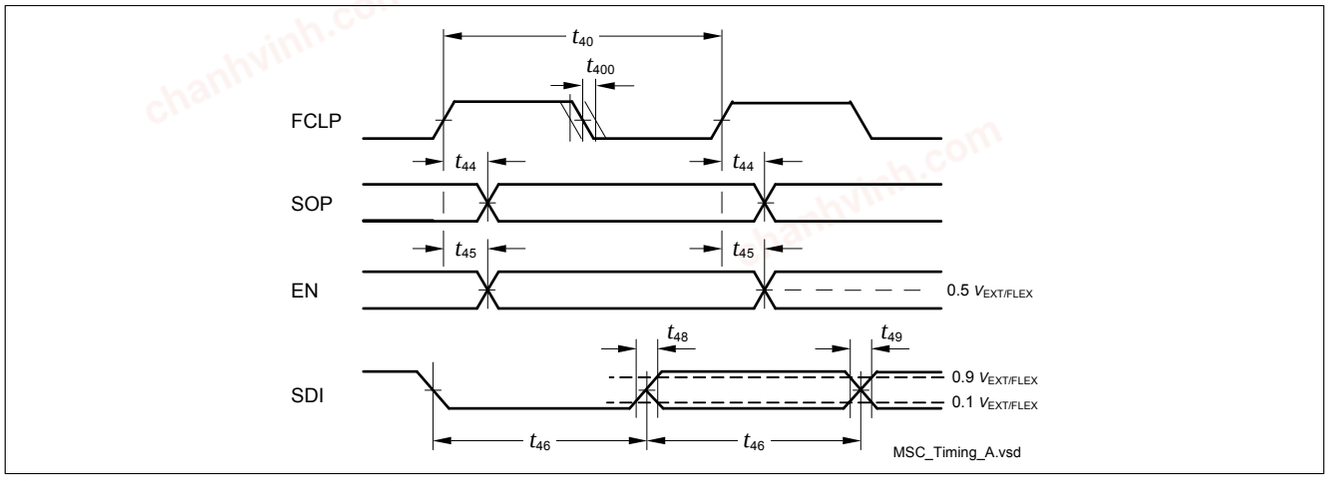



**Figure 3-22 MSC Interface Timing**

*Note: The SOP data signal is sampled with the falling edge of FCLP in the target device.*

## 3.28 MSC Timing 3.3 V Operation

The following section defines the timings for 3.3V pad power supply.

*Note: Pad asymmetry is already included in the following timings.*

*Note: Load for LVDS pads are defined as differential loads in the following timings.*

### Mapping A, Combo Pads in LVDS Mode or CMOS Mode

The timing applies for the LVDS pads in LVDS operating mode:

- The LVDSM output pads for clock and data signals set in LVDS mode
- The CMOS MP pads for enable signals, with strong driver sharp edge (MPss) or strong driver medium edge (MPsm).

**Table 3-78 LVDS clock/data (LVDS pads in LVDS mode)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLPx clock period [1] | $t_{40}$ CC | 2 * $T_A$ [2] [3] | - | - | ns | LVDSM; $C_L$=50pF |
| Deviation from ideal duty cycle [4] [5] | $t_{400}$ CC | -2 | - | 2 | ns | LVDSM; 0 < $C_L$ < 50pF |
| SOPx output delay [6] | $t_{44}$ CC | -5 | - | 5 | ns | LVDSM; $C_L$=50pF; option EN01 |
| | | -7 | - | 7 | ns | LVDSM; $C_L$=50pF; option EN01D |

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**Table 3-78 LVDS clock/data (LVDS pads in LVDS mode)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ENx output delay [6] | $t_{45}$ CC | -7 | - | 10 | ns | MP+ss/MPRss; option EN01; $C_L$=25pF |
| | | -5 | - | 13 | ns | MP+ss/MPRss; option EN01; $C_L$=50pF |
| | | -5 | - | 26 | ns | MP+sm/MPRsm; option EN01D; $C_L$=50pF |
| | | -4 | - | 16 | ns | MP+ss/MPRss; option EN23; $C_L$=25pF |
| | | -4 | - | 17 | ns | MP+ss/MPRss; option EN23; $C_L$=50pF |
| | | -5 | - | 19 | ns | MPss; option EN01; $C_L$=50pF |
| | | -12 | - | 4 | ns | MP+ss/MPRss; option EN01; $C_L$=0pF |
| | | -9 | - | 11 | ns | MP+sm/MPRsm; option EN01D; $C_L$=0pF |
| | | -7 | - | 9 | ns | MP+ss/MPRss; option EN23; $C_L$=0pF |
| | | -12 | - | 7 | ns | MPss; option EN01; $C_L$=0pF |
| SDI bit time | $t_{46}$ CC | 8 * $t_{MSC}$ | - | - | ns | Upstream Timing |
| SDI rise time [7] | $t_{48}$ SR | - | - | 200 | ns | Upstream Timing |
| SDI fall time [7] | $t_{49}$ SR | - | - | 200 | ns | Upstream Timing |

1) FCLP signal rise/fall times are the rise/fall times of the LVDSM pads, and the high/low times are min 1 * $T_A$.
2) $T_{Amin}$ = $T_{MAX}$. When $T_{MAX}$ = 100 MHz,$t_{40}$ = 20 ns
3) The capacitive load on the LVDS pins is differential, the capacitive load on the CMOS pins is single ended.
4) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted if the ABRA block is used.
5) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
6) From FCLP rising edge.
7) When using slow and asymmetrical edges, like in case of open drain upstream connection, the application must take care that the bit is long enough (the baud rate is low enough) so that under worst case conditions the three sampling points in the middle of the bit are not violated.

**Table 3-79 MPss clock/data (LVDS pads in CMOS mode, option EN01)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLPx clock period [1] | $t_{40}$ CC | 2 * $T_A$ [2] [3] | - | - | ns | MPss; $C_L$=50pF |
| Deviation from ideal duty cycle [4] [5] | $t_{400}$ CC | -5 | - | 7+0.07 * $C_L$ | ns | MPss; 0 < $C_L$ < 100pF |

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**Table 3-79 MPss clock/data (LVDS pads in CMOS mode, option EN01)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SOPx output delay [6] | $t_{44}$ CC | -7 | - | 12 | ns | MPss; $C_L$=50pF |
| ENx output delay [6] | $t_{45}$ CC | -9 | - | 12 | ns | MP+ss/MPRss; $C_L$=50pF |
| | | -4 | - | 26 | ns | MP+sm/MPRsm; $C_L$=50pF |
| | | -7 | - | 17 | ns | MPss; $C_L$=50pF |
| | | 0 | - | 54 | ns | MPsm; $C_L$=50pF; except pin P13.0 |
| | | 0 | - | 58 | ns | MPsm; $C_L$=50pF; pin P13.0 |
| | | 4 | - | 77 | ns | MPm/MP+m/MPRm; $C_L$=50pF |
| | | -19 | - | 4 | ns | MP+ss/MPRss; $C_L$=0pF |
| | | -7 | - | 12 | ns | MP+sm/MPRsm; $C_L$=0pF |
| | | -17 | - | 4 | ns | MPss; $C_L$=0pF |
| | | -2 | - | 28 | ns | MPsm; $C_L$=0pF |
| | | -4 | - | 31 | ns | MP+m/MPm/MPRm; $C_L$=0pF |
| SDI bit time | $t_{46}$ CC | 8 * $t_{MSC}$ | - | - | ns | Upstream Timing |
| SDI rise time [7] | $t_{48}$ SR | - | - | 200 | ns | Upstream Timing |
| SDI fall time [7] | $t_{49}$ SR | - | - | 200 | ns | Upstream Timing |

1) FCLP signal rise/fall times are the rise/fall times of the LVDSM pads, and the high/low times are min 1 * $T_A$.
2) $T_{Amin}$ = $T_{MAX}$. When $T_{MAX}$ = 100 MHz,$t_{40}$ = 20 ns
3) FCLP signal high and low can be minimum 1 * $T_{MSC}$.
4) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted if the ABRA block is used.
5) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
6) From FCLP rising edge.
7) When using slow and asymmetrical edges, like in case of open drain upstream connection, the application must take care that the bit is long enough (the baud rate is low enough) so that under worst case conditions the three sampling points in the middle of the bit are not violated.

### Mapping B, CMOS MP Pads

This timing applies for the dedicated CMOS pads, pin Mapping B:

- MP strong sharp (MPss) output pads for the clock and the data signals
- MP strong sharp or strong medium (MPss or MPsm) output pads for enable signals

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**Table 3-80 MP+sm/MPRsm clock/data**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLPx clock period [1] | $t_{40}$ CC | 2 * $T_A$ | - | - | ns | MP+sm/MPRsm; $C_L$=50pF |
| Deviation from ideal duty cycle [2] [3] | $t_{400}$ CC | -3 | - | 7 | ns | MP+sm/MPRsm; 0 < $C_L$ < 200pF |
| SOPx output delay [4] | $t_{44}$ CC | -9 | - | 12 | ns | MP+sm; $C_L$=50pF |
| ENx output delay [4] | $t_{45}$ CC | -20 | - | 4 | ns | MPss; $C_L$=50pF |
| | | -9 | - | 19 | ns | MP+sm/MPRsm; $C_L$=50pF |
| | | 0 | - | 44 | ns | MPsm; $C_L$=50pF |
| | | 0 | - | 63 | ns | MP+m/MPm/MPRm; $C_L$=50pF |
| | | -33 | - | 0 | ns | MPss; $C_L$=0pF |
| | | -23 | - | 4 | ns | MP+sm/MPRsm; $C_L$=0pF |
| | | -9 | - | 14 | ns | MPsm; $C_L$=0pF |
| | | -9 | - | 17 | ns | MPm/MP+m/MPRm; $C_L$=0pF |

1) FCLP signal rise/fall times are the rise/fall times of the LVDSM pads, and the high/low times are min 1 * $T_A$.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted if the ABRA block is used.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) From FCLP rising edge.

**Table 3-81 MPm/MP+m/MPRm clock/data**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLPx clock period [1] | $t_{40}$ CC | 2 * $T_A$ | - | - | ns | MPm/MP+m/MPRm; $C_L$=50pF |
| Deviation from ideal duty cycle [2] [3] | $t_{400}$ CC | -6-0.07 * $C_L$ | - | 6+0.07 * $C_L$ | ns | MPm/MP+m/MPRm; 0 < $C_L$ < 200pF |
| SOPx output delay [4] | $t_{44}$ CC | -19 | - | 17 | ns | MPm/MP+m; $C_L$=50pF |
| ENx output delay [4] | $t_{45}$ CC | -19 | - | 20 | ns | MPm/MP+m/MPRm; $C_L$=50pF |
| | | -57 | - | 0 | ns | MPm/MP+m/MPRm; $C_L$=0pF |

1) FCLP signal rise/fall times are the rise/fall times of the LVDSM pads, and the high/low times are min 1 * $T_A$.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted if the ABRA block is used.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

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4) From FCLP rising edge.

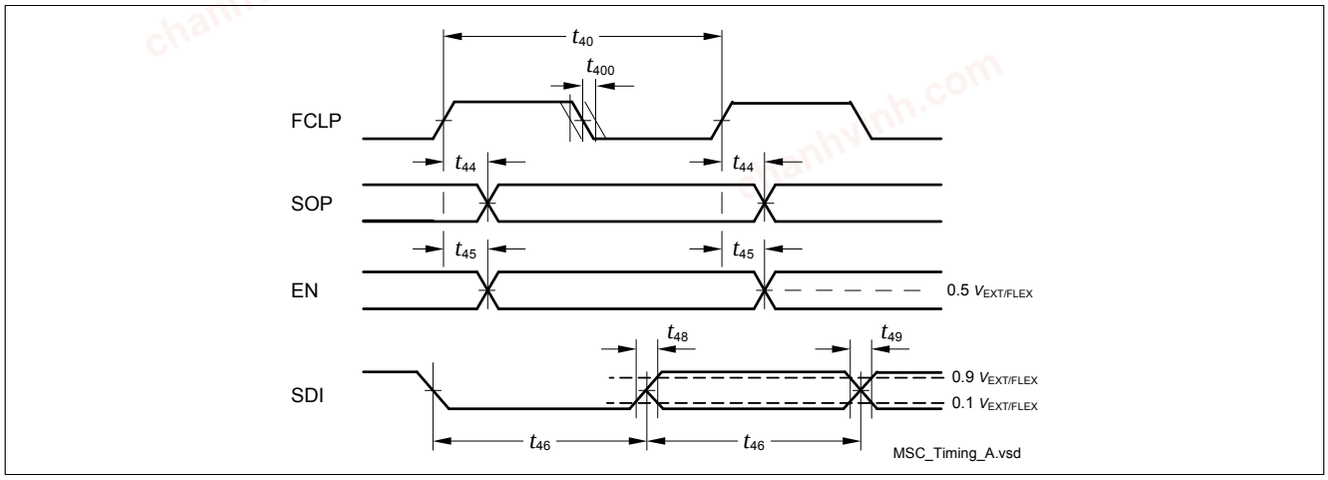



**Figure 3-23 MSC Interface Timing**

*Note: The SOP data signal is sampled with the falling edge of FCLP in the target device.*

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## 3.29 Ethernet Interface (ETH) Characteristics

### 3.29.1 ETH Measurement Reference Points

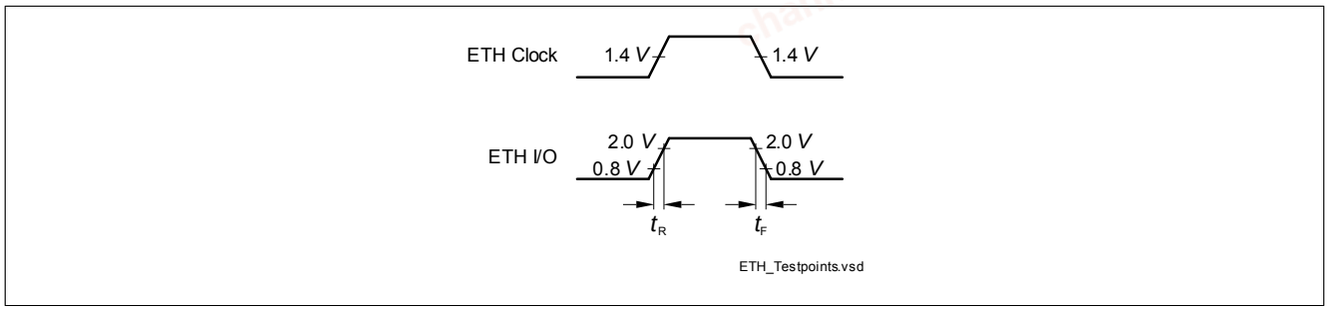



**Figure 3-24 ETH Measurement Reference Points**

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## 3.29.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

**Table 3-82 ETH Management Signal Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ETH_MDC period | $t_1$ CC | 400 | - | - | ns | $C_L$=25pF |
| ETH_MDC high time | $t_2$ CC | 160 | - | - | ns | $C_L$=25pF |
| ETH_MDC low time | $t_3$ CC | 160 | - | - | ns | $C_L$=25pF |
| ETH_MDIO setup time (output) | $t_4$ CC | 10 | - | - | ns | $C_L$=25pF |
| ETH_MDIO hold time (output) | $t_5$ CC | 10 | - | - | ns | $C_L$=25pF |
| ETH_MDIO data valid (input) | $t_6$ SR | 0 | - | 300 | ns | $C_L$=25pF |

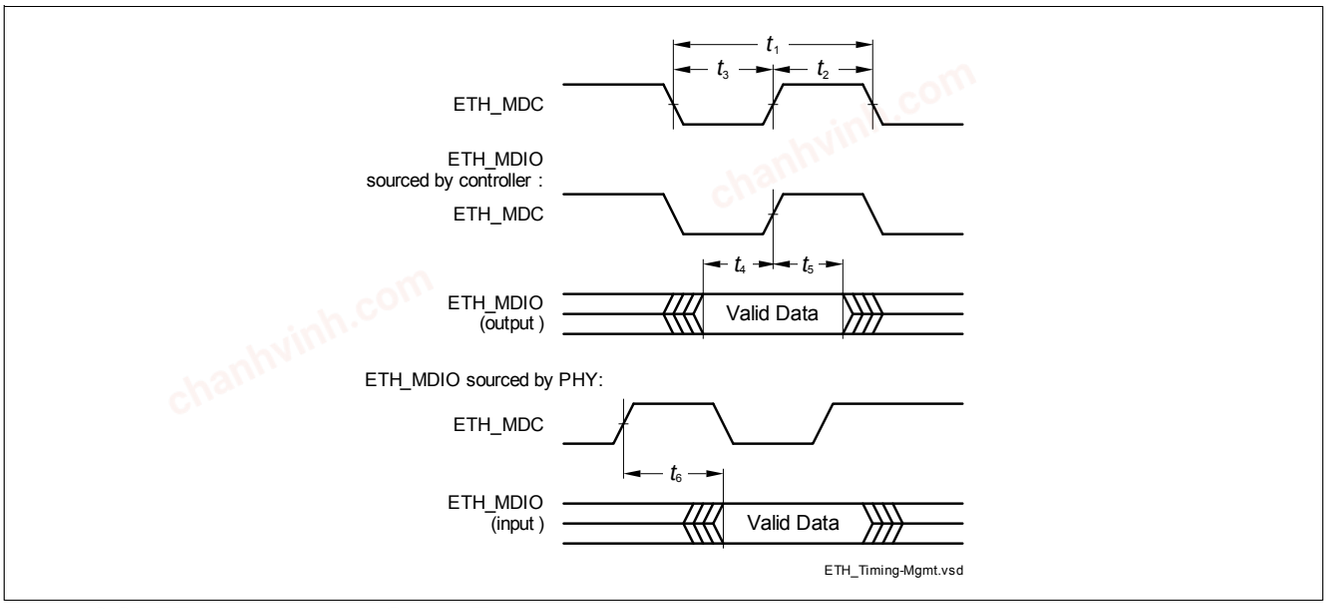



**Figure 3-25 ETH Management Signal Timing**

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### 3.29.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

**Table 3-83 ETH MII Signal Timing Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_7$ SR | 40 | - | - | ns | $C_L$=25pF; baudrate=100Mbps |
| | | 400 | - | - | ns | $C_L$=25pF; baudrate=10Mbps |
| Clock high time | $t_8$ SR | 14 | - | 26 | ns | $C_L$=25pF; baudrate=100Mbps |
| | | 140 [1] | - | 260 [2] | ns | $C_L$=25pF; baudrate=10Mbps |
| Clock low time | $t_9$ SR | 14 | - | 26 | ns | $C_L$=25pF; baudrate=100Mbps |
| | | 140 [1] | - | 260 [2] | ns | $C_L$=25pF; baudrate=10Mbps |
| Input setup time | $t_{10}$ SR | 10 | - | - | ns | $C_L$=25pF |
| Input hold time | $t_{11}$ SR | 10 | - | - | ns | $C_L$=25pF |
| Output valid time | $t_{12}$ CC | 0 | - | 25 | ns | $C_L$=25pF |

1) Defined by 35% of clock period.
2) Defined by 65% of clock period.

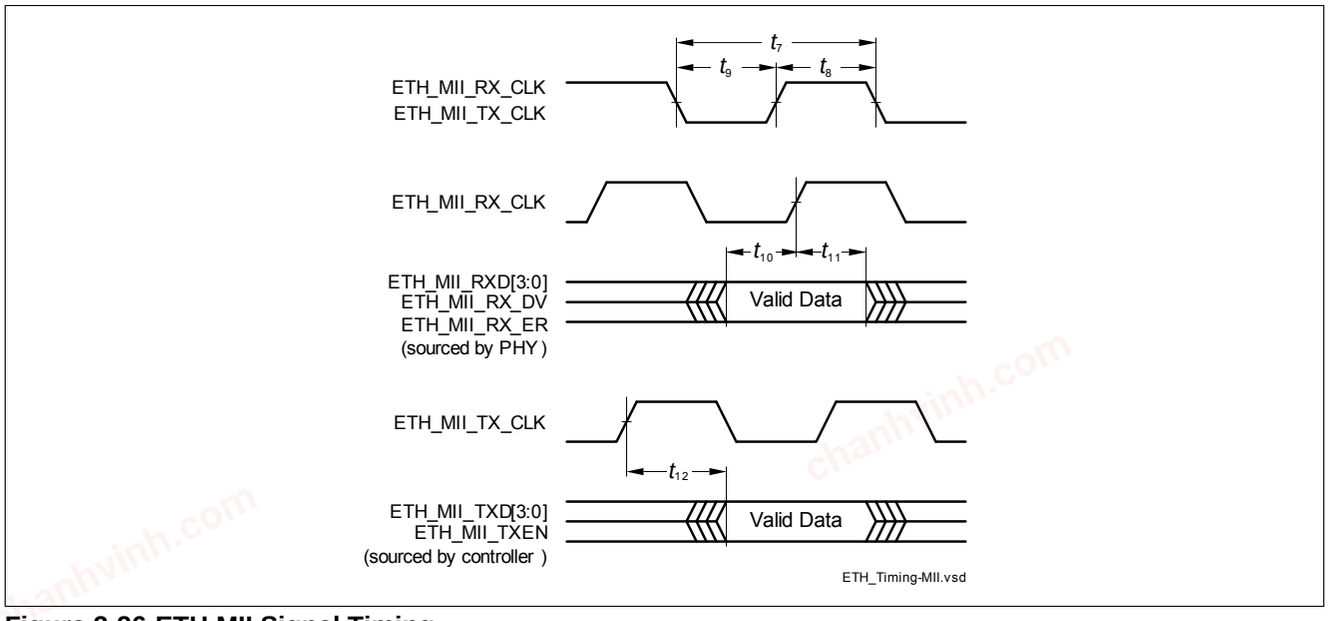



**Figure 3-26 ETH MII Signal Timing**

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### 3.29.4 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

**Table 3-84 ETH RMII Signal Timing Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ETH_RMII_REF_CL clock period | $t_{13}$ CC | 20 | - | - | ns | $C_L$=25pF; 50ppm |
| ETH_RMII_REF_CL clock high time | $t_{14}$ CC | 7 [1] | - | 13 [2] | ns | $C_L$=25pF |
| ETH_RMII_REF_CL clock low time | $t_{15}$ CC | 7 [1] | - | 13 [2] | ns | $C_L$=25pF |
| ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV, ETHRXER; setup time | $t_{16}$ CC | 4 | - | - | ns | $C_L$=25pF |
| ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV, ETHRXER; hold time | $t_{17}$ CC | 2 | - | - | ns | $C_L$=25pF |

1) Defined by 35% of clock period.
2) Defined by 65% of clock period.

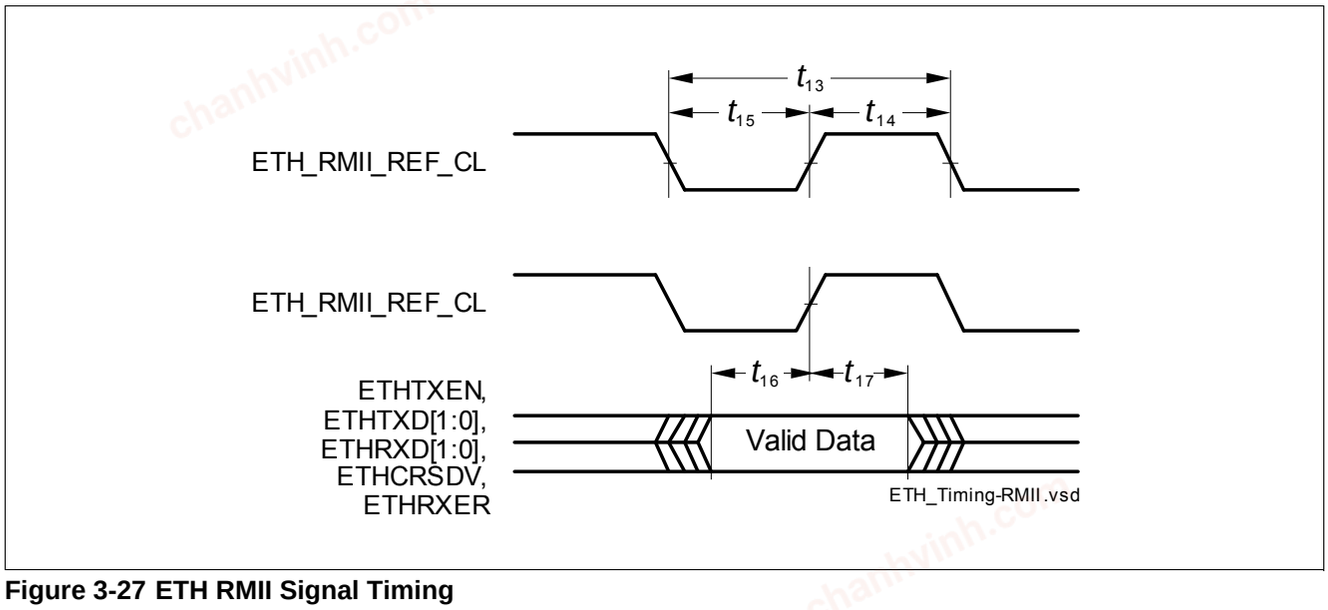



**Figure 3-27 ETH RMII Signal Timing**

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## 3.30 E-Ray Parameters

The timings of this section are valid for the strong driver and either sharp edge settings of the output drivers with $C_L$ = 25 pF. For the inputs the hysteresis has to be configured to inactive.

**Table 3-85 Transmit Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Rise time of TxEN | $t_{dCCTxENRise25}$ CC | - | - | 9 | ns | $C_L$=25pF |
| Fall time of TxEN | $t_{dCCTxENFall25}$ CC | - | - | 9 | ns | $C_L$=25pF |
| Sum of rise and fall time | $t_{dCCTxRise25+dCCTxFall25}$ CC | - | - | 9 | ns | 20% - 80%; $C_L$=25pF |
| Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN | $t_{dCCTxEN01}$ CC | - | - | 25 | ns | |
| Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN | $t_{dCCTxEN10}$ CC | - | - | 25 | ns | |
| Asymmetry of sending | $t_{tx_asym}$ CC | -2.45 | - | 2.45 | ns | $C_L$=25pF |
| Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD | $t_{dCCTxD01}$ CC | - | - | 25 | ns | |
| Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD | $t_{dCCTxD10}$ CC | - | - | 25 | ns | |
| TxD signal sum of rise and fall time at TP1_BD | $t_{txd_sum}$ CC | - | - | 9 | ns | |

**Table 3-86 Receive Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Acceptance of asymmetry at receiving part | $t_{dCCTxAsymAccept25}$ SR | -30.5 | - | 43.0 | ns | $C_L$=25pF |
| Acceptance of asymmetry at receiving part | $t_{dCCTxAsymAccept15}$ SR | -31.5 | - | 44.0 | ns | $C_L$=15pF |
| Threshold for detecting logical high | $T_{uCCLogic1}$ SR | 35 | - | 70 | % | |
| Threshold for detecting logical low | $T_{uCCLogic0}$ SR | 30 | - | 65 | % | |

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**Table 3-86 Receive Parameters** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD | $t_{dCCRxD01}$ CC | - | - | 10 | ns | |
| Sum of delay between TP1_CC and TP1_CC and delays derived from TP4_FFi, falling edge of RxD | $t_{dCCRxD10}$ CC | - | - | 10 | ns | |

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## 3.31 HSCT Parameters

**Table 3-87 HSCT - Rx/Tx setup timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| RX o/p duty cycle | *DCrx* CC | 40 | - | 60 | % | |
| Bias startup time | $t_{bias}$ CC | - | 5 | 10 | µs | Bias distributor waking up from power down and provide stable Bias. |
| RX startup time | $t_{rxi}$ CC | - | 5 | - | µs | Wake-up RX from power down. |
| TX startup time | $t_{tx}$ CC | - | 5 | - | µs | Wake-up TX from power down. |

**Table 3-88 HSCT - Rx parasitics and loads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Capacitance total budget | $C_{total}$ CC | - | 3.5 | 5 | pF | Total Budget for complete receiver including silicon, package, pins and bond wire |
| Parasitic inductance budget | *Htotal* CC | - | 5 | - | nH | |

**Table 3-89 LVDSH - Reduced TX and RX (RED)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output differential voltage | $V_{OD}$ CC | 150 | 200 | 285 | mV | Rt = 100 Ohm ±20% @2pF |
| Output voltage high | $V_{OH}$ CC | - | - | 1463 | mV | Rt = 100 Ohm ±20% |
| Output voltage low | $V_{OL}$ CC | 937 | - | - | mV | Rt = 100 Ohm ±20% |
| Output offset (Common mode) voltage | $V_{OS}$ CC | 1.08 | 1.2 | 1.32 | V | Rt = 100 Ohm ±20% @2pF |
| Input voltage range | $V_I$ SR | - | - | 1.6 | V | Absolute max = 1.6 V + (285mV/2) = 1.743 |
| | | 0.15 | - | - | V | Absolute min = 0.15 V - (285 mV /2) = 0 V |
| Input differential threshold | $V_{idth}$ SR | -100 | - | 100 | mV | 100 mV for 55% of bit period; Note Absolute Value (Vidth - Vidthl) |
| Data frequency | *DR* CC | 5 | - | 320 | Mbps | |

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**Table 3-89 LVDSH - Reduced TX and RX (RED)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Receiver differential input impedance | $R_{in}$ CC | 90 | 100 | 110 | Ohm | 0 V < $V_I$ < 1.6V |
| | | 80 | 100 | 120 | Ohm | 1.6 V < $V_I$ < 2.0V |
| Slew rate | $SRtx$ CC | - | - | 2 | V/ns | |
| Change in VOS between 0 and 1 | $dVOS$ CC | - | - | 50 | mV | Peak to peak (including DC transients). |
| Change in Vod between 0 and 1 | $dVod$ CC | - | - | 50 | mV | Peak to peak (including DC transients) |
| Fall time [1] | $t_{fall}$ CC | 0.26 | - | 1.2 | ns | Rt = 100 Ohm ±20% @2pF |
| Rise time [1] | $t_{rise}$ CC | 0.26 | - | 1.2 | ns | Rt = 100 Ohm ±20% @2pF |

1) Rise / fall times are defined for 10% - 90% of $V_{OD}$

**Table 3-90 HSCT PLL**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| PLL frequency range | $f_{PLL}$ CC | 12.5 | 320 | 320 | MHz | |
| PLL input frequency | $f_{REF}$ CC | 10 | - | 20 | MHz | |
| PLL lock-in time | $t_{LOCK}$ CC | - | - | 50 | µs | |
| Bit Error Rate based on 10 MHz reference clock at Slave PLL side | $BER_{10}$ CC | - | - | 10EXP-9 | - | Bit Error Rate based on Slave interface reference clock at 10 MHz |
| Bit Error Rate based on 20 MHz reference clock at Slave PLL side | $BER_{20}$ CC | - | - | 10EXP-12 | - | Bit Error Rate based on Slave interface reference clock at 20 MHz |
| Absolute RMS Jitter (TX out) | $J_{ABS10}$ CC | -125 | - | 125 | ps | Measured at link TX out; valid for Reference frequency at 10 MHz |
| Absolute RMS Jitter (TX out) | $J_{ABS20}$ CC | -85 | - | 85 | ps | Measured at link TX out; valid for Reference frequency at 20 MHz |

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**Table 3-90 HSCT PLL** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Accumulated RMS Jitter (RX side) | $J_{ACC10}$ CC | - | - | 145 | ps | Measured at link RX input, based on 5000 measures, each 300 clock cycles; valid for Reference frequency at 10 MHz |
| Accumulated RMS Jitter (link RX side) | $J_{ACC20}$ CC | - | - | 115 | ps | Measured at link RX input, based on 5000 measures, each 300 clock cycles; valid for Reference frequency at 20 MHz |
| Total Jitter peak to peak | $TJ_{pp}$ CC | - | - | 2083 | ps | Total Jitter as sum of deterministic jitter and random jitter |

**Table 3-91 HSCT Sysclk**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Frequency | $f_{SYSCLK}$ CC | 10 | - | 20 | MHz | |
| Frequency error | $dfERR$ CC | -1 | - | 1 | % | |
| Duty Cycle | $DCsys$ CC | 45 | - | 55 | % | |
| Load impedance | $R_{LOAD}$ CC | 10 | - | - | kOhm | |
| Load capacitance | $C_{LOAD}$ CC | - | - | 10 | pF | |
| Integrated phase noise | $I_{PN}$ CC | - | - | -58 | dB | single sideband phase noise in 10 kHz to 10 Mhz at 20 MHz SysClk |

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## 3.32 Inter-IC (I2C) Interface Timing

This section defines the timings for I2C in the TC270 / TC275 / TC277.

All I2C timing parameter are SR for Master Mode and CC for Slave Mode.

**Table 3-92 I2C Standard Mode Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Fall time of both SDA and SCL | $t_1$ | - | - | 300 | ns | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Capacitive load for each bus line | $C_b$ SR | - | - | 400 | pF | |
| Bus free time between a STOP and ATART condition | $t_{10}$ | 4.7 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Rise time of both SDA and SCL | $t_2$ | - | - | 1000 | ns | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Data hold time | $t_3$ | 0 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Data set-up time | $t_4$ | 250 | - | - | ns | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Low period of SCL clock | $t_5$ | 4.7 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| High period of SCL clock | $t_6$ | 4 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Hold time for the (repeated) START condition | $t_7$ | 4 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |

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**Table 3-92 I2C Standard Mode Timing** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Set-up time for (repeated) START condition | $t_8$ | 4.7 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Set-up time for STOP condition | $t_9$ | 4 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |

**Table 3-93 I2C Fast Mode Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Fall time of both SDA and SCL | $t_1$ | $20+0.1*C_b$ | - | 300 | ns | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Capacitive load for each bus line | $C_b$ SR | - | - | 400 | pF | |
| Bus free time between a STOP and ATART condition | $t_{10}$ | 1.3 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Rise time of both SDA and SCL | $t_2$ | $20+0.1*C_b$ | - | 300 | ns | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Data hold time | $t_3$ | 0 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Data set-up time | $t_4$ | 100 | - | - | ns | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Low period of SCL clock | $t_5$ | 1.3 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| High period of SCL clock | $t_6$ | 0.6 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |

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**Table 3-93 I2C Fast Mode Timing** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Hold time for the (repeated) START condition | $t_7$ | 0.6 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Set-up time for (repeated) START condition | $t_8$ | 0.6 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |
| Set-up time for STOP condition | $t_9$ | 0.6 | - | - | µs | Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line |

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## 3.33 Flash Target Parameters

Program Flash program and erase operation is only allowed up the $T_J$ = 150°C.

**Table 3-94 FLASH**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Program Flash Erase Time per logical sector | $t_{ERP}$ CC | - | - | 1 | s | cycle count < 1000 |
| | | - | 0.207 + 0.003 * ($S$ [KByte]) / ($f_{FSI}$ [MHz])[1)] | - | s | cycle count < 1000, for sector of size S |
| Program Flash Erase Time per Multi-Sector Command | $t_{MERP}$ CC | - | - | 1 | s | For consecutive logical sectors in a physical sector, cycle count < 1000 |
| | | - | 0.207 + 0.003 * ($S$ [KByte]) / ($f_{FSI}$ [MHz])[1)] | - | s | For consecutive logical sector range of size S in a physical sector, cycle count < 1000 |
| Program Flash program time per page in 5 V mode | $t_{PRP5}$ CC | - | - | 50 + 3000/($f_{FSI}$ [MHz]) | µs | 32 Byte |
| Program Flash program time per page in 3.3 V mode | $t_{PRP3}$ CC | - | - | 81 + 3400/($f_{FSI}$ [MHz]) | µs | 32 Byte |
| Program Flash program time per burst in 5 V mode | $t_{PRPB5}$ CC | - | - | 125 + 9500/($f_{FSI}$ [MHz]) | µs | 256 Byte |
| Program Flash program time per burst in 3.3 V mode | $t_{PRPB3}$ CC | - | - | 410 + 12000/($f_{FSI}$ [MHz]) | µs | 256 Byte |
| Program Flash program time for 1 MByte with burst programming in 3 V mode excluding communication | $t_{PRPB3_1MB}$ CC | - | - | 2.2 | s | Derived value for documentation purpose, valid for $f_{FSI}$ = 100MHz |
| Program Flash program time for 1 MByte with burst programming in 5 V mode excluding communication | $t_{PRPB5_1MB}$ CC | - | - | 0.9 | s | Derived value for documentation purpose, valid for $f_{FSI}$ = 100MHz |
| Program Flash program time for complete PFlash with burst programming in 5 V mode excluding communication | $t_{PRPB5_PF}$ CC | - | - | 3.6 | s | Derived value for documentation purpose, valid for $f_{FSI}$ = 100MHz |

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**Table 3-94 FLASH** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Write Page Once adder | $t_{ADD}$ CC | - | - | 15 + 500/($f_{FSI}$ [MHz]) | µs | Adder to Program Time when using Write Page Once |
| Program Flash suspend to read latency | $t_{SPNDP}$ CC | - | - | 12000/($f_{FSI}$ [MHz]) | µs | For Write Burst, Verify Erased and for multi-(logical) sector erase commands |
| Data Flash Erase Time per Sector [2] | $t_{ERD}$ CC | - | 0.12 + 0.08/($f_{FSI}$ [MHz])[1] | - | s | cycle count < 1000 |
| | | - | 0.57 + 0.15/($f_{FSI}$ [MHz])[1] | 0.928 + 0.15/($f_{FSI}$ [MHz]) | s | cycle count < 125000 |
| Data Flash Erase Time per Multi-Sector Command [2] | $t_{MERD}$ CC | - | 0.12 + 0.01 * ($S$ [KByte]) / ($f_{FSI}$ [MHz])[1] | - | s | For consecutive logical sector range of size S, cycle count < 1000 |
| | | - | 0.57 + 0.019 * ($S$ [KByte]) / ($f_{FSI}$ [MHz])[1] | 0.928 + 0.019 * ($S$ [KByte]) / ($f_{FSI}$ [MHz]) | s | For consecutive logical sector range of size S, cycle count < 125000 |
| Data Flash erase disturb limit | $N_{DFD}$ CC | - | - | 50 | cycles | |
| Program time data flash per page [3] | $t_{PRD}$ CC | - | - | 50 + 2500/($f_{FSI}$ [MHz]) [3] | µs | 8 Byte |
| Complete Device Flash Erase Time PFlash and DFlash [4] | $t_{ER_Dev}$ CC | - | - | 9 | s | Derived value for documentation purpose (excl. UCBs and HSMs), valid for $f_{FSI}$ = 100MHz |
| Data Flash program time per burst [3] | $t_{PRDB}$ CC | - | - | 96 + 4400/($f_{FSI}$ [MHz]) [3] | µs | 32 Bytes |
| Data Flash suspend to read latency | $t_{SPNDD}$ CC | - | - | 12000/($f_{FSI}$ [MHz]) | µs | |
| Wait time after margin change | $t_{FL_MarginDel}$ CC | - | - | 10 | µs | |
| Program Flash Retention Time, Sector | $t_{RET}$ CC | 20 | - | - | years | Max. 1000 erase/program cycles |
| Data Flash Endurance per EEPROMx sector [5] | $N_{E_EEP10}$ CC | 125000 | - | - | cycles | Max. data retention time 10 years |

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**Table 3-94 FLASH** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Data Flash Endurance per HSMx sector [5] | $N_{E_HSM}$ CC | 125000 | - | - | cycles | Max. data retention time 10 years |
| UCB Retention Time | $t_{RTU}$ CC | 20 | - | - | years | Max. 100 erase/program cycles per UCB, max 400 erase/program cycles in total |
| Data Flash access delay | $t_{DF}$ CC | - | - | 100 | ns | see PMU_FCON.WSDFLASH |
| Data Flash ECC Delay | $t_{DFECC}$ CC | - | - | 20 | ns | see PMU_FCON.WSECDF |
| Program Flash access delay | $t_{PF}$ CC | - | - | 30 | ns | see PMU_FCON.WSPFLASH |
| Program Flash ECC delay | $t_{PFECC}$ CC | - | - | 10 | ns | see PMU_FCON.WSECPF |
| Number of erase operations on DF0 over lifetime | $N_{ERD0}$ CC | - | - | 750000 | cycles | |
| Number of erase operations on DF1 over lifetime | $N_{ERD1}$ CC | - | - | 500000 | cycles | |
| Junction temperature limit for PFlash program/erase operations | $T_{JPFlash}$ SR | - | - | 150 | °C | |

1) All typical values were characterised, but are not tested. Typical values are safe median values at room temperature
2) Under out-of-spec conditions (e.g. over-cycling) or in case of activation of WL oriented defects, the duration of erase processes may be increased by up to 50%.
3) Time is not dependent on program mode (5V or 3.3V).
4) Using 512 KByte erase commands.
5) Only valid when a robust EEPROM emulation algorithm is used. For more details see the Users Manual.

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## 3.34 Package Outline

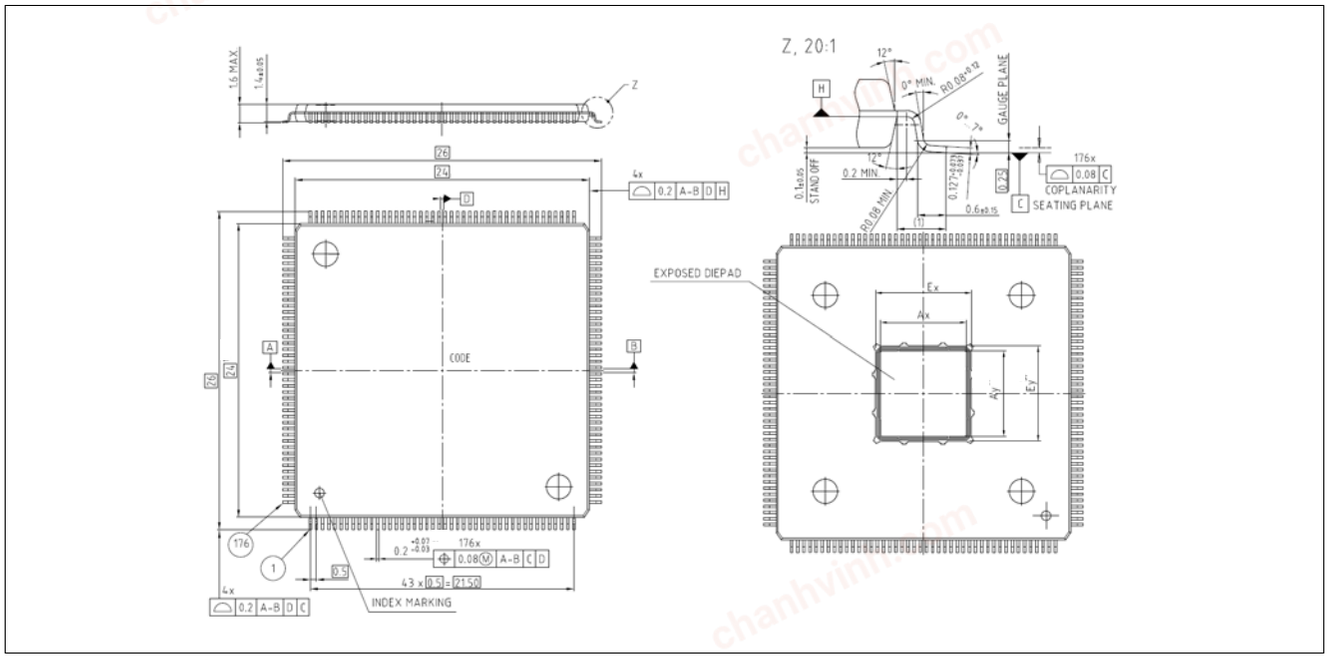



**Figure 3-28 Package Outlines PG-LQFP-176-22**

**Table 3-95 Exposed Pad Dimensions**

| | |
|---|---|
| **Ax (nominal EPad size)** | **7.9 mm ± 50 µm** |
| **Ay (nominal EPad size)** | **7.9 mm ± 50 µm** |
| **Ex (solder able EPad size)** | **8.7 mm ± 50 µm** |
| **Ey (solder able EPad size)** | **8.7 mm ± 50 µm** |

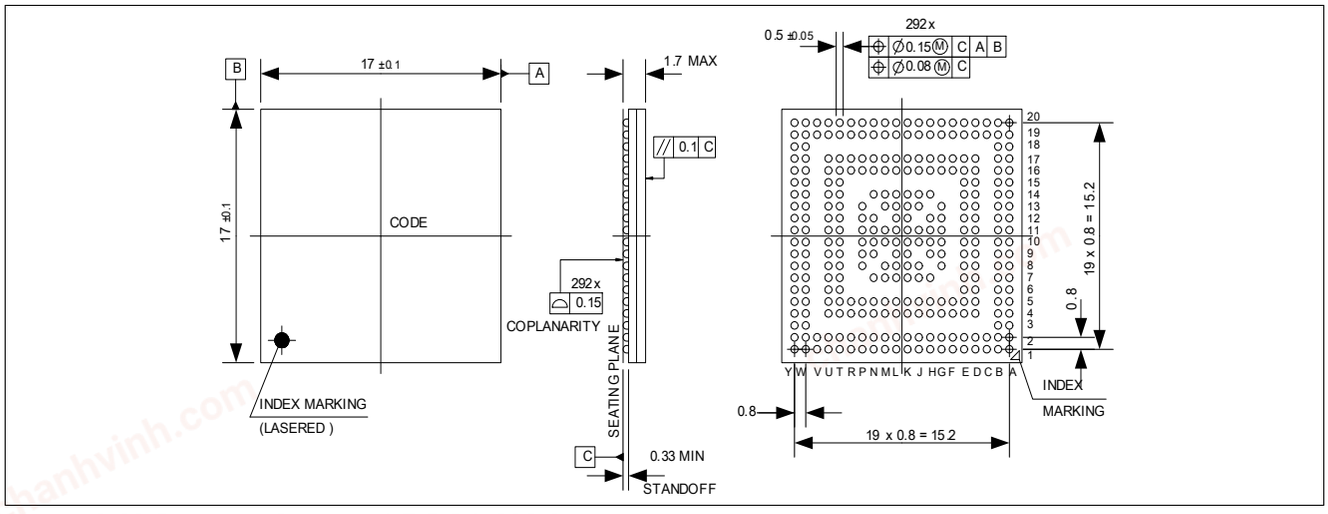



**Figure 3-29 Package Outlines LF-BGA-292-6**

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

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### 3.34.1 Package Parameters

**Table 3-96 Thermal Characteristics of the Package**

| Device | Package | RQJCT[1)] | RQJCB[1)] | RQJA | Unit | Note |
|---|---|---|---|---|---|---|
| TC275 | PG-LQFP-176-22 | 9,6 | 1,25 | 14,7[2)] | K/W | with soldered exposed pad |
| TC277 | LF-BGA-292-6 | 5,1 | 7,2 | 15,8[3)] | K/W | |

1) The top and bottom thermal resistances between the case and the ambient ($R_{TCAT}$, $R_{TCAB}$) are to be combined with the thermal resistances between the junction and the case given above ($R_{TJCT}$, $R_{TJCB}$), in order to calculate the total thermal resistance between the junction and the ambient ($R_{TJA}$). The thermal resistances between the case and the ambient ($R_{TCAT}$, $R_{TCAB}$) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} * P_D$, where the $R_{TJA}$ is the total thermal resistance between the junction and the ambient. This total junction ambient resistance $R_{TJA}$ can be obtained from the upper four partial thermal resistances.
Thermal resistances as measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1).
2) Value is defined in accordance with JEDEC JESD51-3, JESD51-5, and JESD51-7.
3) Value is defined in accordance with JEDEC JESD51-1.

### 3.34.2 TC270 Carrier Tape

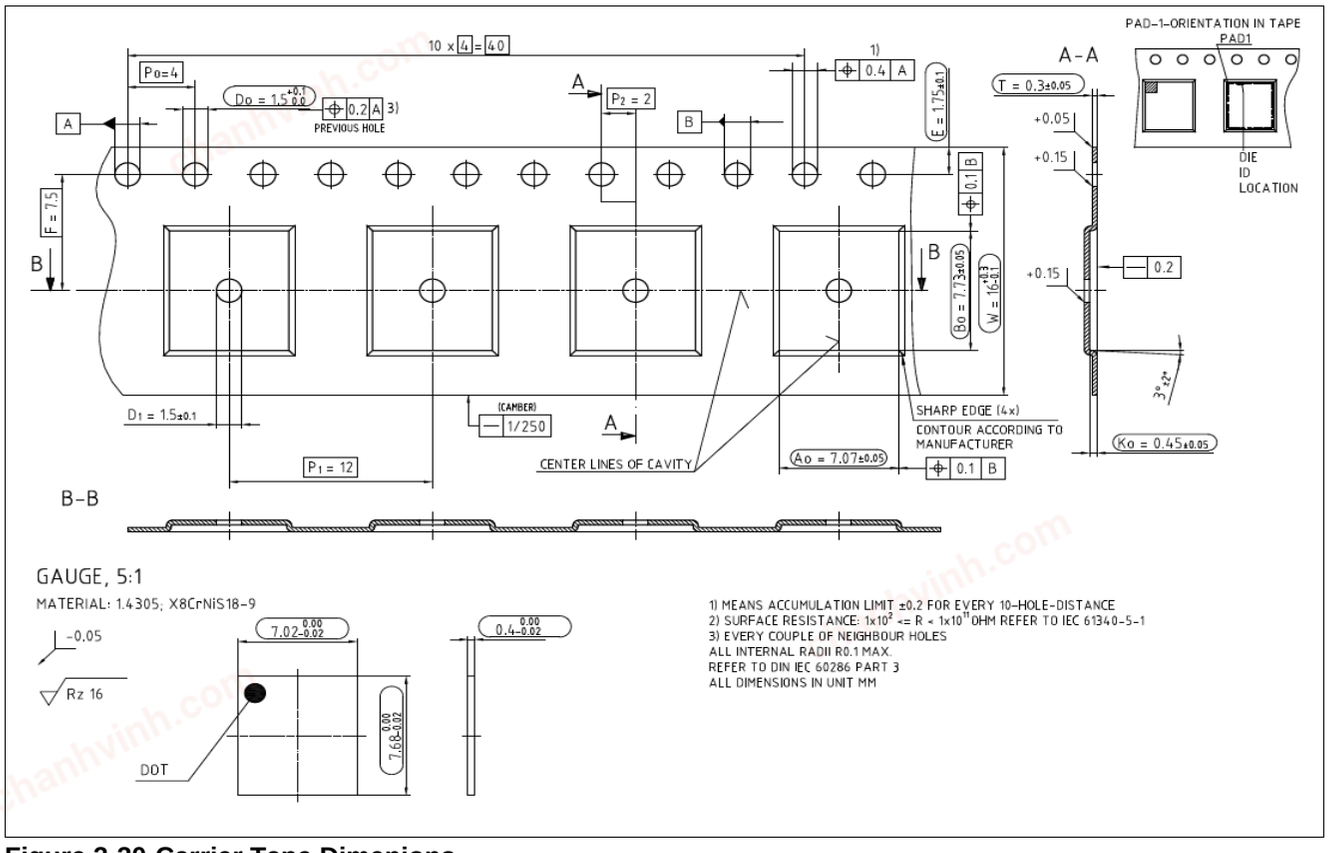



**Figure 3-30 Carrier Tape Dimenions**

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**Table 3-97 TC270 Chip Dimenions**

| Device | A | B | T |
|---|---|---|---|
| TC270 | 7,590 mm | 6,930 mm | 0,3 mm |

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## 3.35 Quality Declarations

**Table 3-98 Quality Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operation Lifetime | $t_{OP}$ | - | - | 24500 | hour | |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ | - | - | 2000 | V | Conforming to JESD22-A114-B |
| ESD susceptibility of the LVDS pins | $V_{HBM1}$ | - | - | 500 | V | |
| ESD susceptibility according to Charged Device Model (CDM) | $V_{CDM}$ | - | - | 500 | V | for all other balls/pins; conforming to JESD22-C101-C |
| | | - | - | 750 | V | for corner balls/pins; conforming to JESD22-C101-C |
| Moisture Sensitivity Level | $MSL$ | - | - | 3 | | Conforming to Jedec J-STD--020C for 240C |

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# 4 History

## 4.1 Changes from TC27xDB_v10 to 1.0

- Replace PG-LQFP-176-18 with correct package LF-BGA-292-6 in table 1
- VADC
  - Add parameter $t_{WU}$
  - Add parameter $R_{MDU}$
  - Add parameter $R_{MDD}$

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