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65 mΩ active-bridge daughter card

Line rectifier module featuring 600 V CoolMOS™ S7, integrated IR11688S controller and 2EDF7275F driver in an ultra-compact design

Order code

KIT_ACT_BRD_60R040S7

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Scope and purpose

This document describes the design and operation of a complete Infineon Technologies AG system solution for active line rectification based on a 600 V CoolMOS™ S7, aiming to replace the diode bridge in standard Power Factor Correction (PFC) converters.

Use of the 600 V CoolMOS™ S7 active-bridge daughter card boosts the PFC efficiency by more than 1 percent at low-line levels (115 V AC) and up to 0.7 percent at high-line (230 V AC) without any impact on system design.

The active-bridge daughter cards are available in the following variants:

- KIT_ACT_BRD_60R022S7, mounting 22 mΩ CoolMOS™ S7
- KIT_ACT_BRD_60R040S7, mounting 40 mΩ CoolMOS™ S7
- KIT_ACT_BRD_60R065S7, mounting 65 mΩ CoolMOS™ S7

The main Infineon components used in the **KIT_ACT_BRD_60R065S7** are described in the following.

Kit components:

- Synchronous Rectifier (SR) controller (IR11688S)
- 600 V CoolMOS™ S7 SJ MOSFET (IPT60R065S7)
- Fast dual-channel functional isolated gate driver (2EDF7275F)

Kit specifications:

- Input voltage: from 85 to 265 V AC
- CoolMOS™ S7 $R_{DS(on)}$: 65 mΩ
- Control and driver supply voltage: 12 V

Intended audience

Power supply design engineers

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Table of contents

Table of contents **2**
1 Introduction **3**
2 Kit overview **5**
2.1 Hardware description 5
2.2 Active-bridge control method 6
2.2.1 Turn-on blanking time 8
2.2.2 Minimum on-time 8
2.2.3 Regulation phase 8
2.2.4 Turn-off and reset 9
2.3 Board specification 10
3 Experimental results **11**
3.1 Steady-state waveforms 11
3.1 Control parameters optimization 12
3.2 Start-up waveforms 13
3.3 Efficiency measurements 13
3.4 Temperature measurements 14
4 Summary **16**
5 Schematics **17**
6 PCB layout **18**
7 Bill of Materials (BOM) **19**
8 References **20**
Revision history **21**

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1 Introduction

In recent years, the trend for SMPS has been toward increasing both efficiency and power density with optimized cost.

A variety of efficiency requirements, such as 80 PLUS or EuP, are defined for various SMPS. In the Platinum class the PSU must have a peak efficiency above 94 percent at high-line and 92 percent at low-line, while for a Titanium design these values increase to 96 percent and 94 percent, respectively. In addition, some customers may define stricter efficiency requirements based on system operating conditions.

It is obvious that the overall efficiency of the PSU depends on both efficiency levels of the PFC and of the DC-DC stages. For a fixed efficiency target of the PSU, if we are able to increase PFC performance than we can relax the requirements of the DC-DC converter, and vice-versa. Of course, this will impact the overall cost of the system. The question for every PSU manufacturer would be: what is the optimum balance between the two stages?

An easy and effective way of improving the PFC efficiency performance across the whole load and voltage range, without affecting the design, complexity and PFC cost too much, is to simply replace the classic diode bridge with an active bridge made with the 600 V CoolMOS™ S7.

Figure 1 shows a comparison between the active-bridge daughter card and a standard diode bridge. In terms of form factor the two solutions are comparable, while the active bridge needs one extra pin connection for the bias supply. More details about the board are discussed in the next chapter.

In Figure 2 the efficiency benefit of the **KIT_ACT_BRD_60R065S7** employed in a standard Continuous Conduction Mode (CCM) PFC is presented both at low-line (115 V AC) and high-line (230 V AC) in terms of delta efficiency comparison with the diode bridge solution. The measurement is done by plugging the 22 mΩ daughter card into the Infineon active-bridge PFC demo board **EVAL_2K4W_ACT_BRD_S7** [1]. The maximum output power is around 1200 W at low-line and 2400 W at high-line. An efficiency delta improvement of 1.1 percent and 0.5 percent can be seen at low-line and at high-line respectively under light-load condition. The delta efficiency is halved at 50 percent of the output power.

The 65 mΩ active bridge gives an improvement above 0.4 percent at both low-line and high-line when the output power is below 700 W, as shown by the red shaded zone in Figure 2.

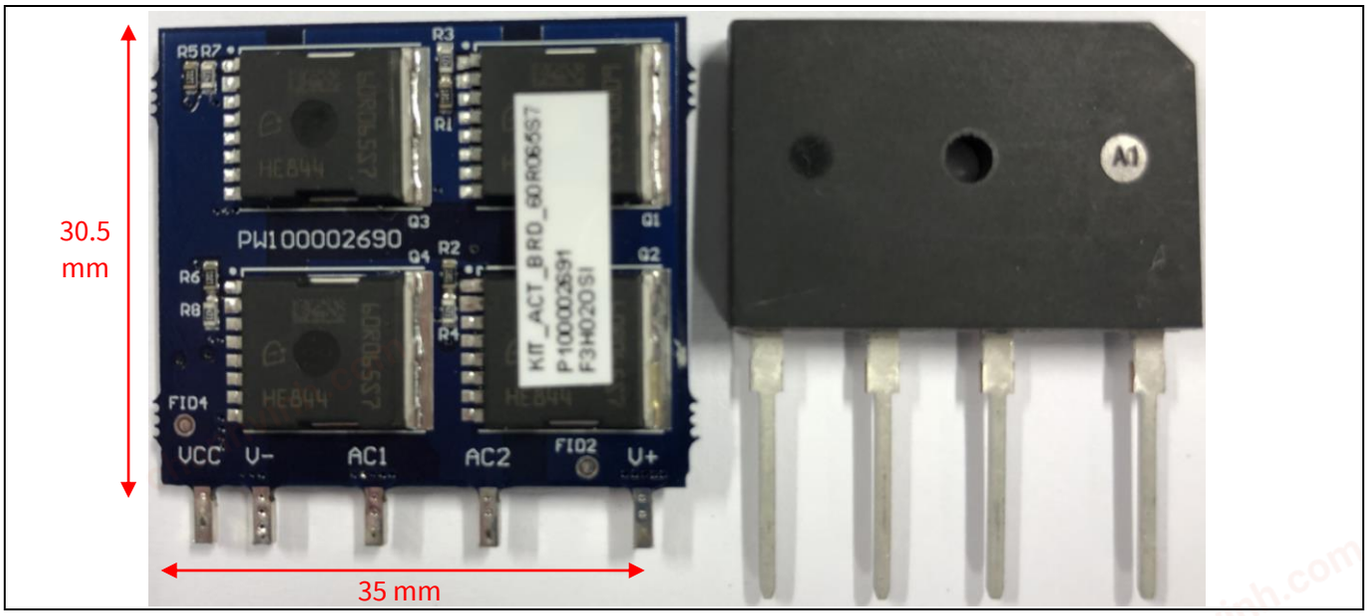


Figure 1 Active-bridge daughter card (left) compared with a standard diode bridge (right)

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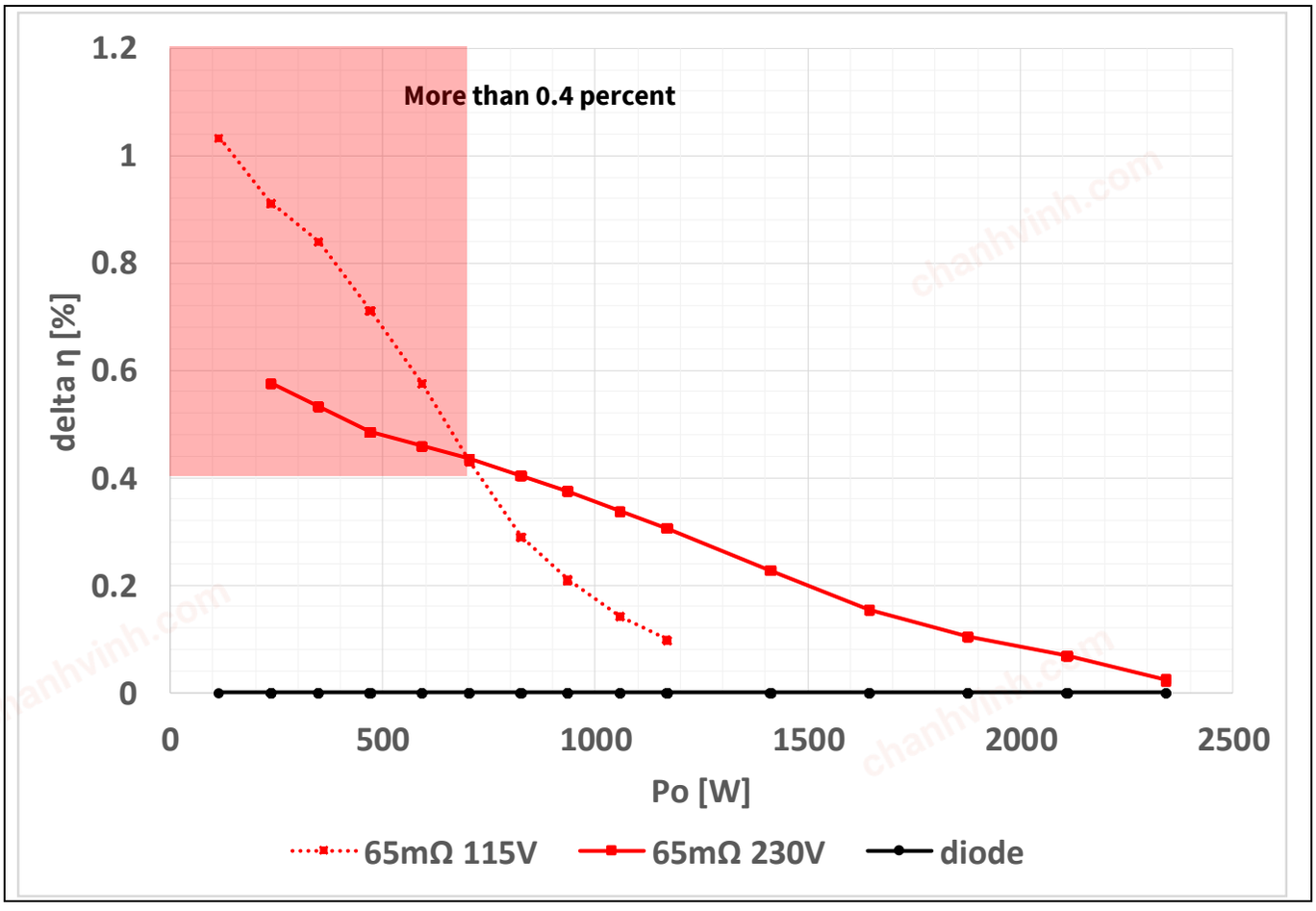


Figure 2 Efficiency improvement in CCM PFC with KIT_ACT_BRD_60R065S7

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2 Kit overview

2.1 Hardware description

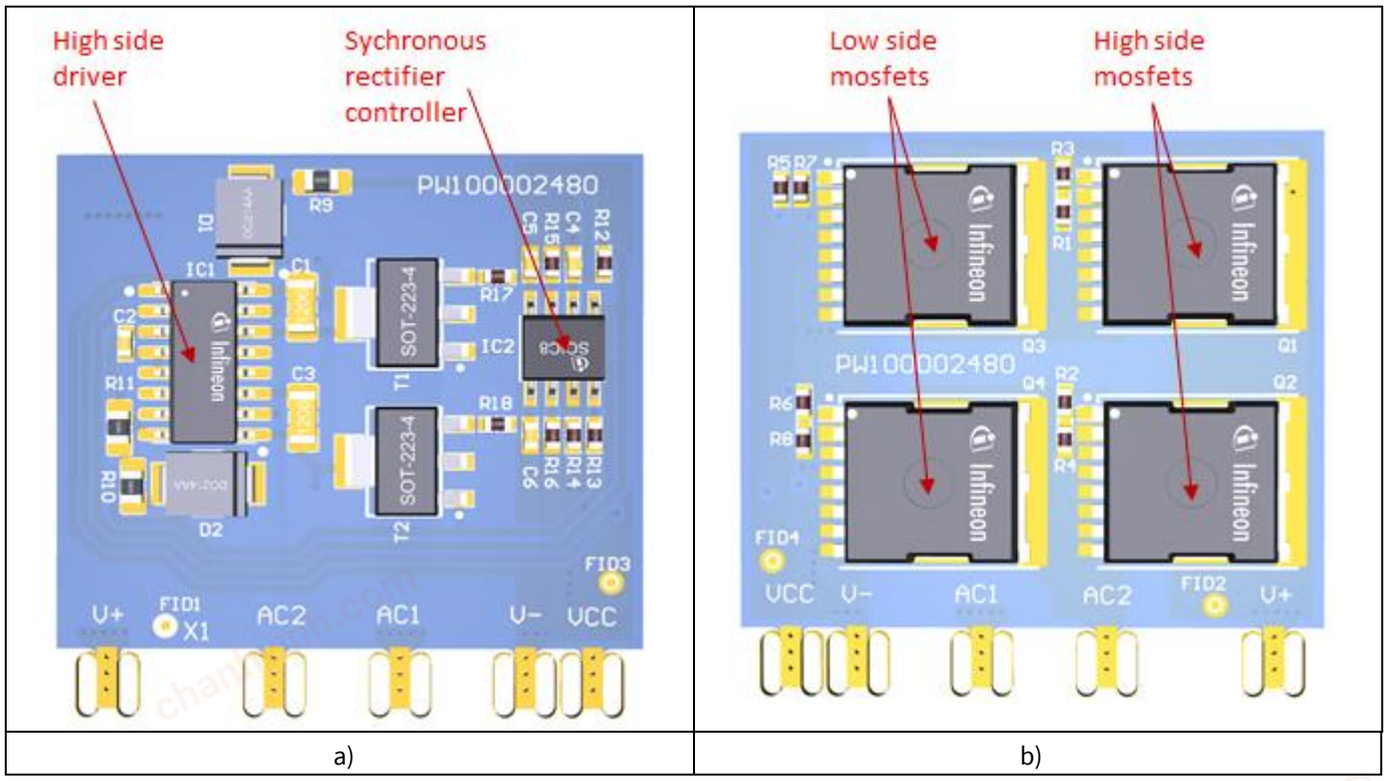
The active-bridge daughter board is shown in Figure 3. The board is 35 mm long, with a width of 6 mm and a height of 30.5 mm, comparable to the size of a standard diode bridge rectifier (20 mm x 30 mm x 4.6 mm).

The daughter board has five pins:

- Line (AC1) and neutral (AC2) alternate inputs
- Positive (V+) and negative (V-) rectified outputs
- Bias supply input (V_{CC})

The bias supply voltage of 12 V is provided by the PFC main board or by the application, and the same V_{CC} is also used to supply PFC control and driving stages.

The daughter card integrates both power devices and control/driving components, thus enabling a high power density design. The power devices in TO-leadless (TOLL) packages are placed on the bottom side together with the gate resistors, as shown in Figure 3b. On the top side, the controller (IR11688S) and the high-side MOSFET driver (2EDF7275F) are placed as shown in Figure 3a. Additional components are: bootstrap R-C-D networks for high-side MOSFET driving and small-signal transistor in SOT-223 to extend the voltage capability of the controller. In fact, without any extra transistors, the IR11688S drain voltage sense capability would be limited to only 200 V. More details about the control of the active bridge are discussed in the next section.



a) b)

Figure 3 Placement of the different components in the active-bridge daughter card with Infineon 600 V CoolMOS™ S7 MOSFET: a) top view and b) bottom view

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2.2 Active-bridge control method

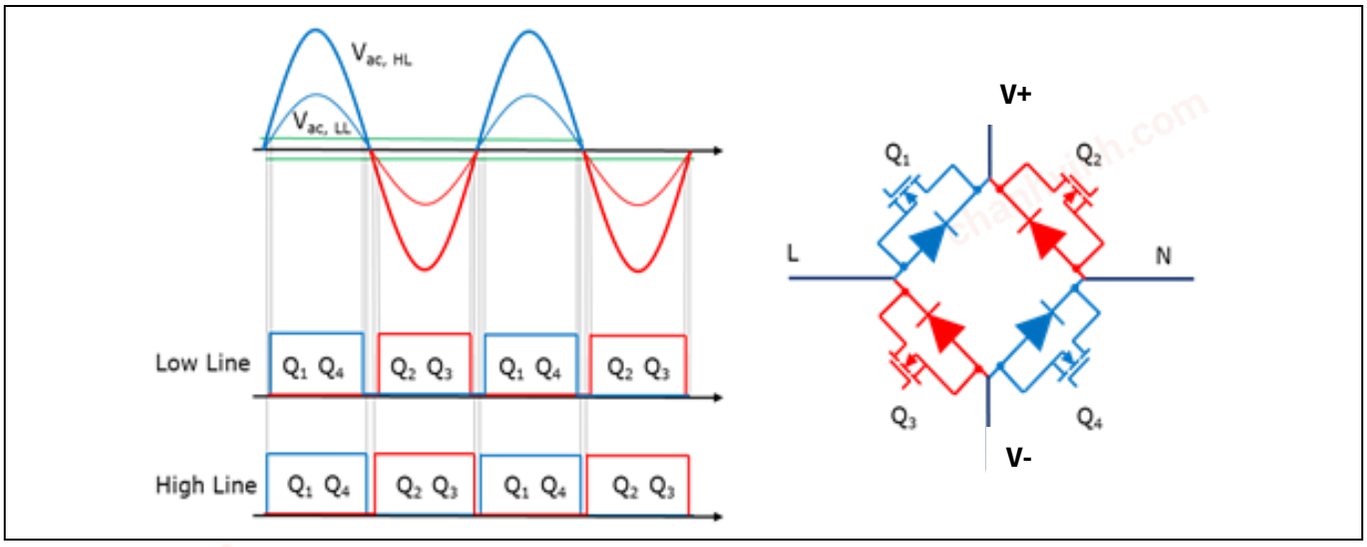


Figure 4 Control concept of the active-bridge line rectification

Control of an active bridge for line rectification is intuitive. As shown in Figure 4, during the positive half-cycle of the mains, Q1 and Q4 are supposed to be switched on, while the others are kept off. Instead, during the negative half-cycle of the AC-grid, Q3 and Q2 are supposed to conduct, while the others are off.

It's important to highlight that all the MOSFETs are always conducting in the so-called "reverse mode" or "diode mode", with a positive current flowing from the source to the drain. In fact, the active bridge's purpose is to take over the conduction of the diode in order to achieve better efficiency, since MOSFET conduction losses are lower than those from diodes.

There are two possible ways of controlling the active bridge switches:

1. By measuring the input voltage V AC
2. By sensing the voltage drop across the MOSFET V_{DS}

In the *first method*, the control signal for each MOSFET of the active bridge is obtained by comparing the instantaneous input voltage (properly scaled down through a resistive divider) with a fixed reference voltage threshold. The voltage divider resistance should be high enough to minimize the quiescent loss, especially at high-line input. With this method, the on-time of the control signal at each cycle strongly depends on the input voltage level. This means that a shorter on-time is obtained at low-line input and vice versa.

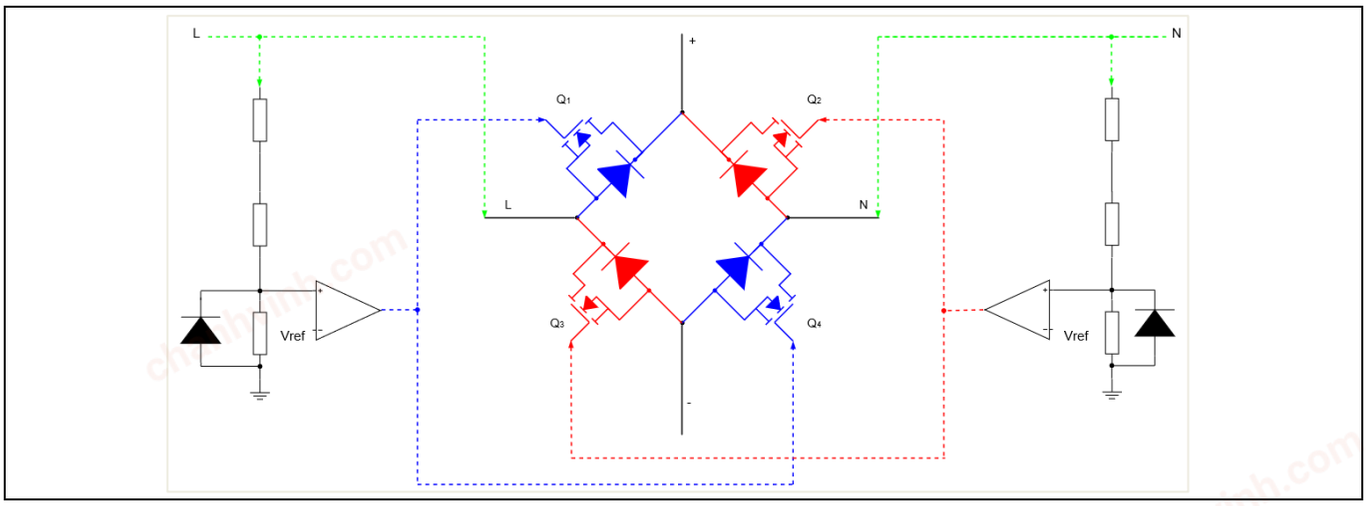


Figure 5 First control method based on measuring the input voltage

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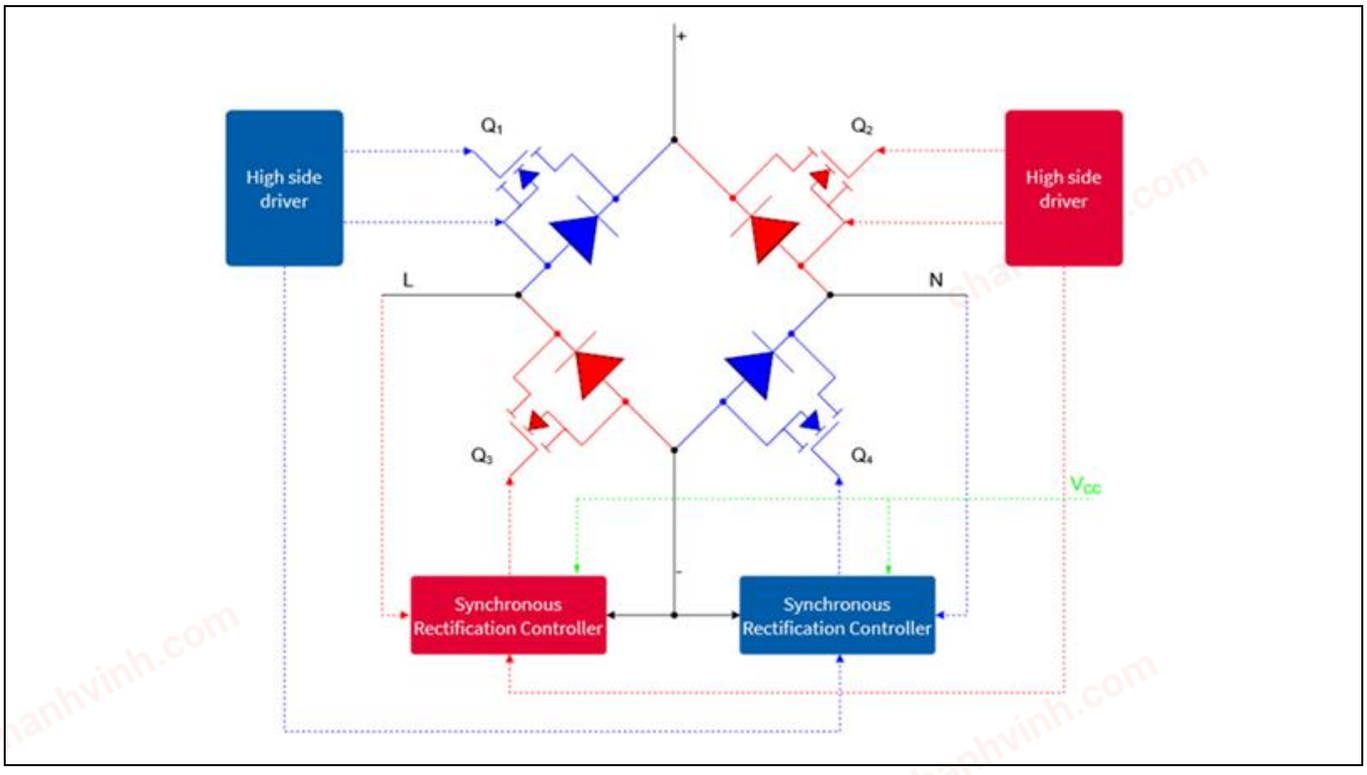


Figure 6 Second approach based on the SR controller

The *second approach* exploits the information of the current flowing through each low-side MOSFET by sensing the V_{DS} across the MOSFETs, as shown in Figure 6. This method is commonly used in the secondary-side SR controllers. Such a solution is already available in the market and is widely used in high-efficiency step-down DC-DC converters, for example for driving the SR of an LLC resonant converter.

This second method is the one employed in the proposed active-bridge daughter card by using Infineon controller IR11688S, as shown in Figure 7.

The IR11688S is a dual smart secondary-side controller IC optimized to drive two N-channel power MOSFETs configured for SR in resonant converter applications, with drain voltage sensing capability up to 200 V. Small-signal transistors T1 and T2 of Figure 7 are added to further extend the voltage capability of the controller, matching the high-line PFC application.

The drain-to-source voltage of the low-voltage side MOSFET (Q3, Q4) of the active bridge is sensed through the VD1 and VD2 pins to determine the source-to-drain current and consequently turn on/off each gate rapidly at the start/ending of each conduction cycle. The drain-to-source voltages are compared to different thresholds to precisely control the gates, as shown in Figure 8a.

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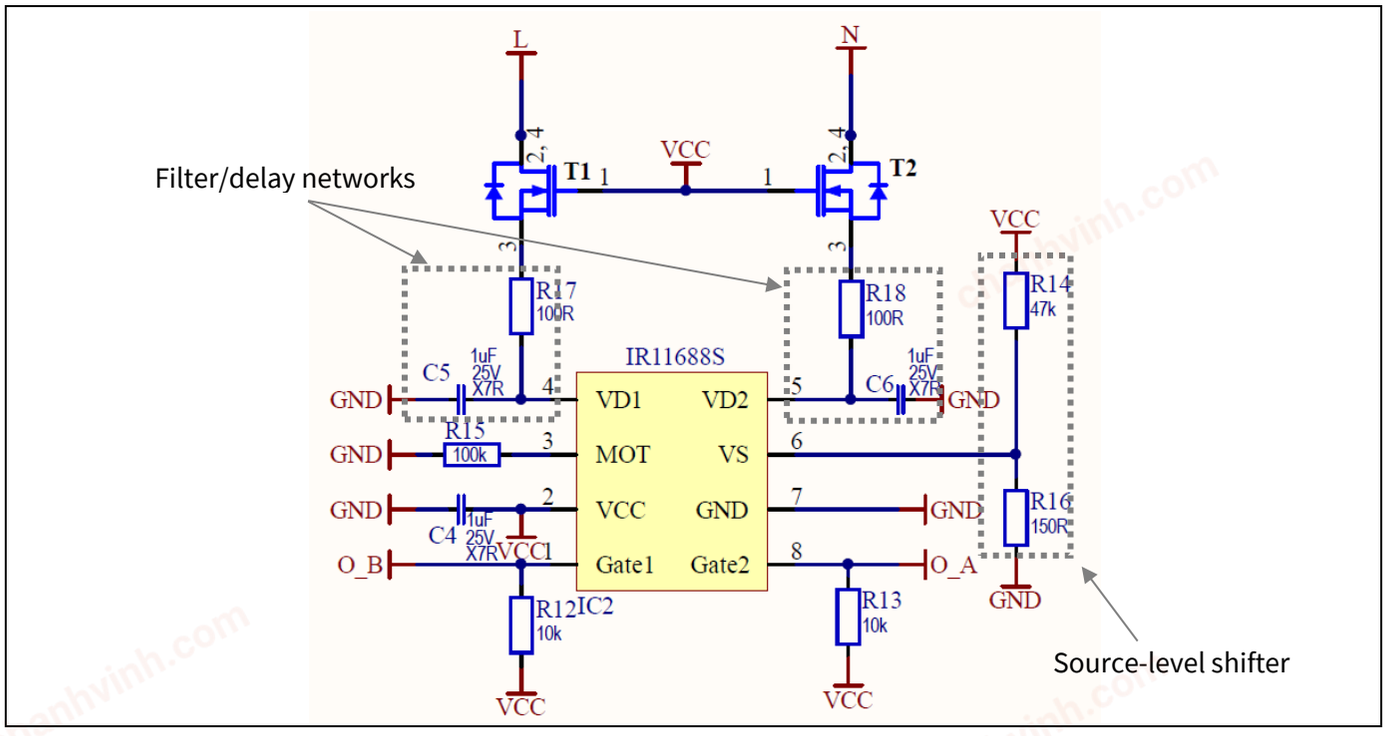


Figure 7 Adaptation of IR11688S for active line rectification

2.2.1 Turn-on blanking time

When the conduction phase of each active full-bridge MOSFET begins, the active MOSFET is still off, and therefore the current starts to flow through the body diode producing a negative V_{DS} voltage across it, as shown by the blue line of Figure 8b. The body diode high-voltage drop is sufficient to trigger the turn-on threshold V_{TH2} (≈-230 mV). If V_{DS} remains below V_{TH2} for more than T_{Don} (≈150 ns), the gate of the corresponding active MOSFET is driven high, which causes V_{DS} to reduce rapidly to $I_D * R_{DS_{ON}}$. The internal delay timer will be reset if V_{DS} rises above V_{TH2} before T_{Don} times out. This turn-on blanking time represents the body diode conduction time and helps to avoid misfiring that could be triggered by high-frequency ringing in Discontinuous Conduction Mode (DCM) operation. For fixed-frequency 50/60 Hz PFC applications this means very high duty cycle for the active bridge, regardless of working at low-line or high-line.

2.2.2 Minimum on-time

The voltage drop at the gate turn-on is usually accompanied by some amount of ringing, which could potentially trigger the input comparator to turn off the gate drive very quickly. However, the Minimum On-Time (MOT) blanking period prevents this. For fixed-frequency 50/60 Hz PFC applications the MOT is to be set to the highest possible value, as the value of R15 of Figure 7. In fact, $T_{MOT} = R_{MOT} * 2 * 10^{-11} + 20ns \approx 2us$.

2.2.3 Regulation phase

At the end of the MOT, the gate output is no longer driven high and reverts to a high impedance state. When V_{DS} is below the regulation threshold V_{THR} (≈-40 mV), a weak pull-down gradually discharges the gate voltage held by the active-bridge MOSFET input capacitance. As the gate voltage drops, the MOSFET channel resistance increases as it enters the linear region. This causes V_{DS} to once again exceed V_{THR} so that weak pull-down will cease until the conduction current falls to the point where V_{DS} again drops below V_{THR}.

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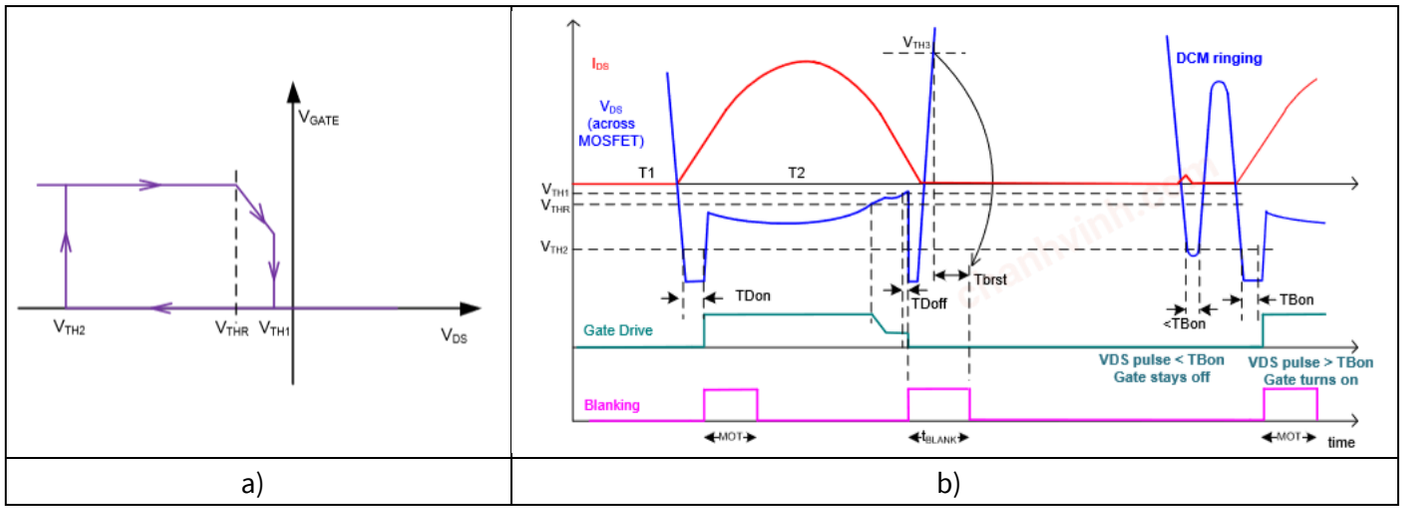


Figure 8 Behavior of IR11688S: a) input comparator thresholds and b) example of waveforms

This regulating process continues so that the conduction period is extended until the current has fallen to a very low level. In this way premature turn-off, which can arise due to parasitic inductances in PCB traces and the MOSFET package, is prevented. This period of conduction through the SR MOSFET body diodes is thereby reduced to a minimum, improving overall system efficiency.

2.2.4 Turn-off and reset

At the end of the switching cycle the conduction rectifier current reduces to zero so the V_{DS} voltage will cross the turn-off threshold V_{TH1} (≈-4 mV). When this happens the gate is driven low to switch off the SR MOSFET. Any residual current will again start flowing through the body diode, causing a negative step in V_{DS}. When this occurs V_{DS} could potentially trigger turn-on once again by crossing V_{TH2}. To prevent this possibility, turn-on is blanked for a time period t_{DBLANK} (≈15 µs) after turn-off has occurred. The blanking time is internally set and can be reset only when V_{DS} crosses the positive threshold V_{TH3} (≈1.18 V). Reset occurs only when V_{DS} remains higher than V_{TH3} for more than the reset blanking time, t_{BRST} (≈400 ns). This protects against false triggering due to ringing after the turn-off phase. Once reset the IR11688S is re-armed so that turn-on may be triggered for the next conduction cycle.

Reset V_{TH3} and regulation V_{THR} thresholds are referenced to GND (see Figure 7), and therefore they cannot be changed by any circuit modification. On the other hand, turn-on V_{TH2} and turn-off V_{TH1} thresholds are referenced to V_S, thus giving the designer freedom to change them by adapting the resistor-divider (named as source-level shifter in Figure 7). In our example we are shifting the V_S voltage of around 40 mV. This V_S offset must be adapted depending on the MOSFET $R_{DS(on)}$ and the application.

The IR11688S also has very low quiescent current when the gate drives are not switching to offer minimal power consumption in standby mode (less than 500 µA).

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2.3 Board specification

Table 1 presents the specification of the active-bridge board developed using the 600 V CoolMOS™ S7 in a TOLL package.

Table 1 Summary of specifications and test conditions for the active-bridge daughter card

Parameter	Specification
Input voltage range	85 to 265 Vrms
Nominal input voltage at low-line	115 Vrms
Nominal input voltage at high-line	230 Vrms
AC-line frequency range	45 to 65 Hz
Max. ambient temperature	40°C
Max. output power	2400 W (referenced to PFC board)
Bias voltage	12 V

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3 Experimental results

3.1 Steady-state waveforms

Steady-state behavior of the active-bridge daughter card is first tested in a standalone set-up with the AC generator directly connected to the board pins AC1 and AC2 of Figure 3, and a resistive load of around 160 Ω attached to the output pins V+ and V-.

Figure 9 shows the steady-state waveforms of active-bridge low-side complementary driving signals during PFC operation at high-line.

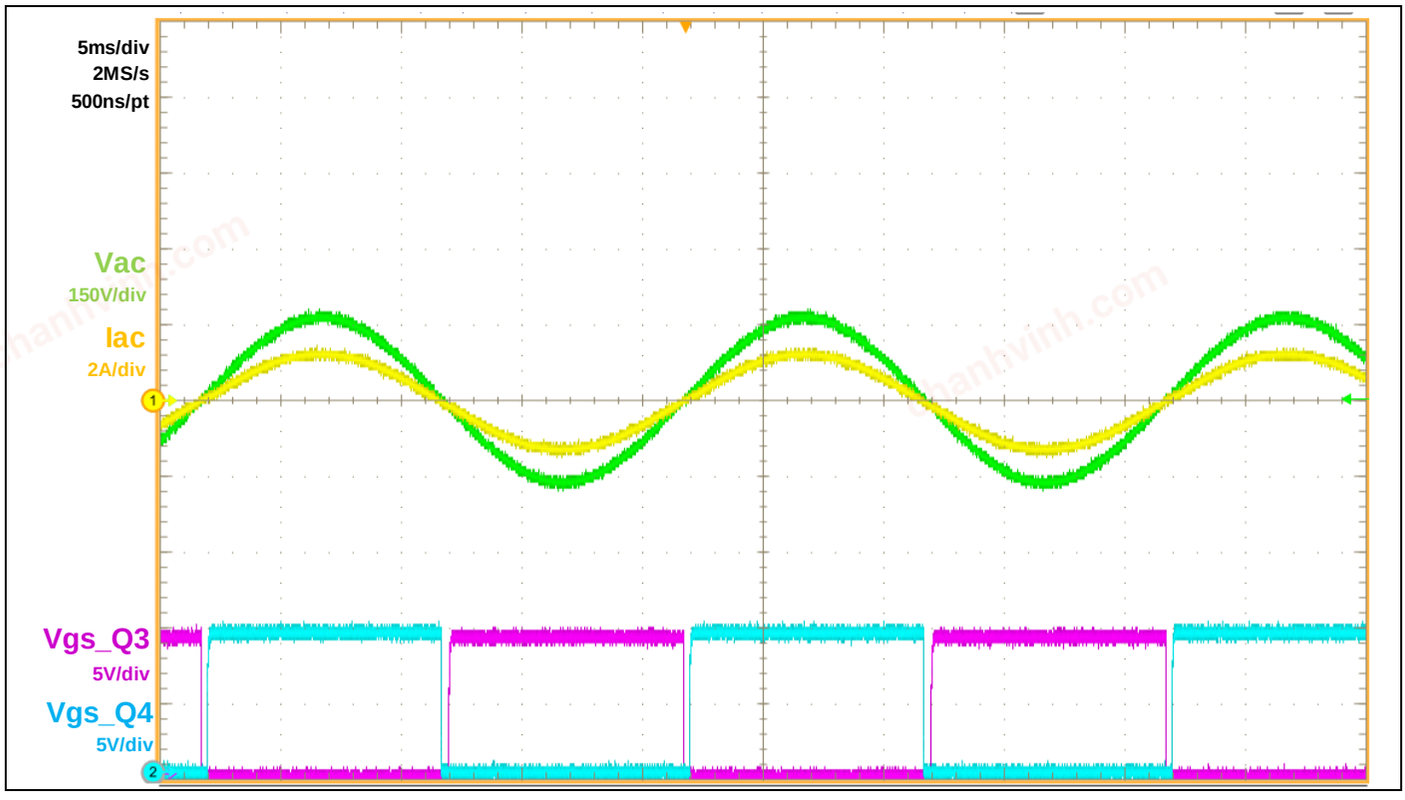


Figure 9 **Steady-state waveforms of active-bridge low-side complementary driving signals (magenta and light blue lines), input current and voltage (yellow and green lines) and PFC output voltage (light blue line) at 115 V AC**

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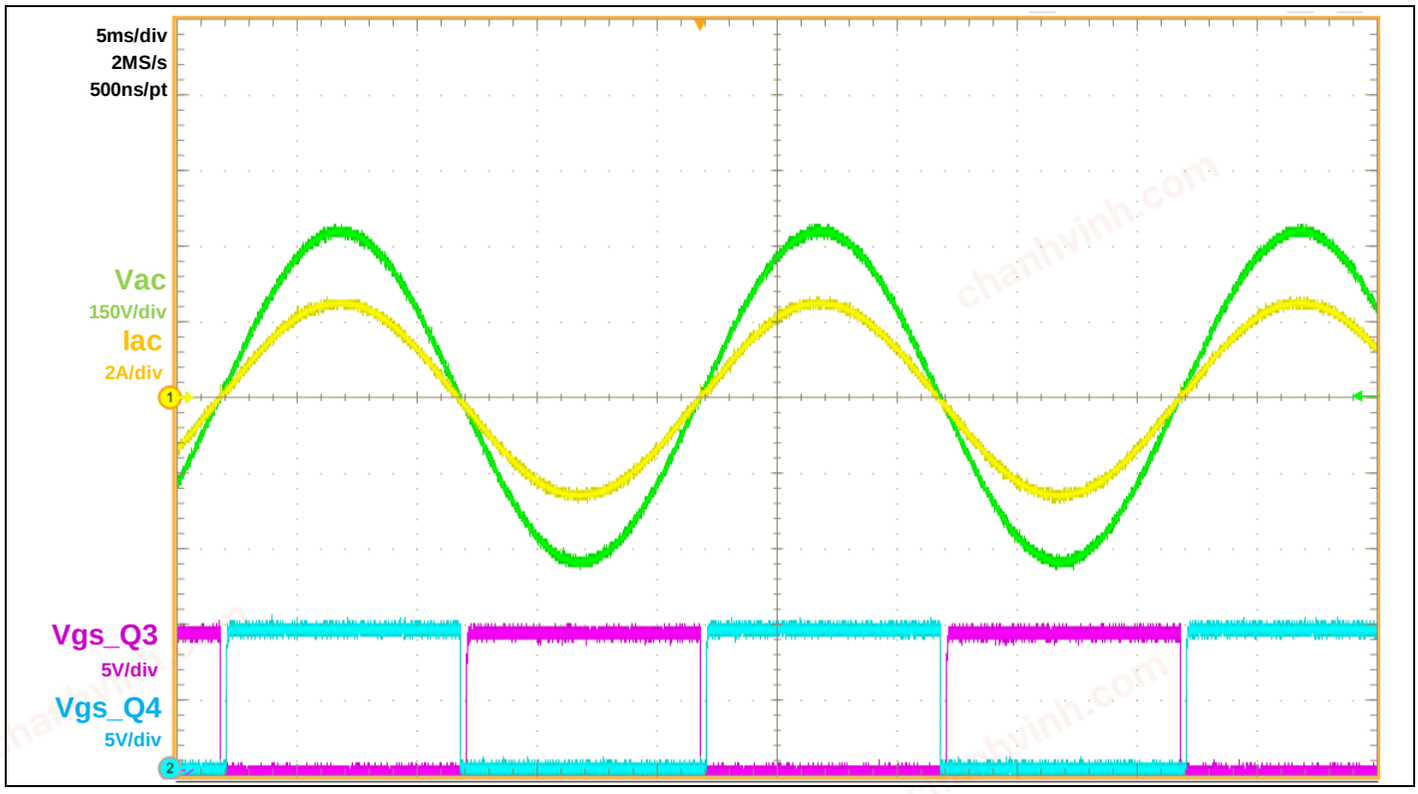
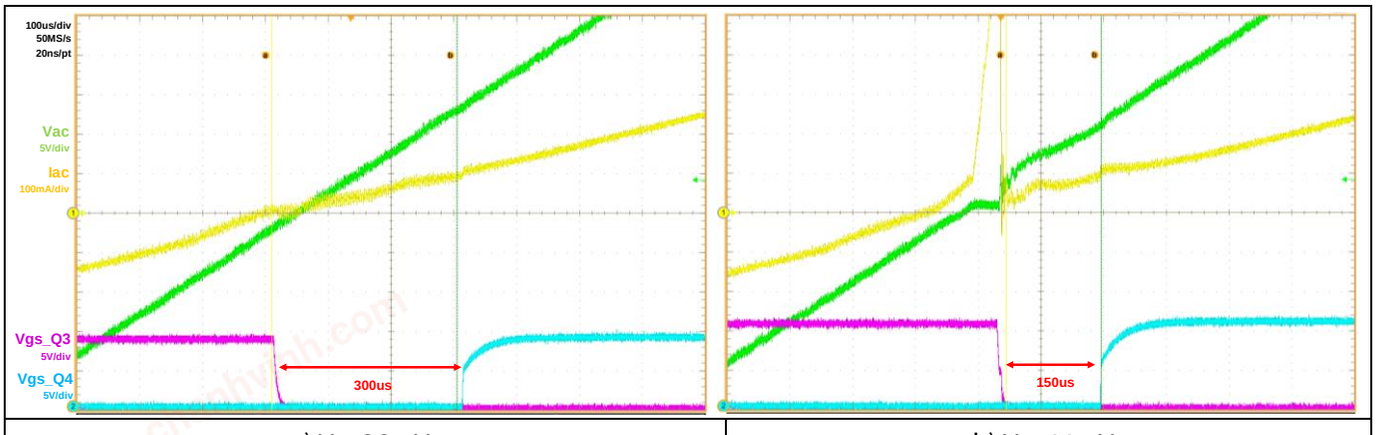


Figure 10 **Steady-state waveforms of active-bridge low-side complementary driving signals (magenta and light blue lines), input current and voltage (yellow and green lines) and PFC output voltage (light blue line) at 230 V AC**

3.1 Control parameters optimization

As mentioned in the discussion of the control method, the source voltage level shifter can be used to anticipate/postpone the the turn-on/off of the active-bridge MOSFETs.

In the experiment in Figure 11, the V_S level is changed by adjusting the V_{CC} voltage since the V_S depends on the bias voltage. In Figure 11a the V_S is 36 mV corresponding to a V_{CC} equal to 11.5 V. In this case the Q3 MOSFET is turning off near the zero crossing of the current.



a) Vs=36mV | b) Vs=44mV

Figure 11 **Zero crossing comparison using two different voltage values of the source-level shifter in the SR controller**

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The complementary MOSFET Q4 is switched on after 300 µs. During this sort of “dead-time” the body diode is conducting.

By increasing the V_S value, the MOSFET Q3 turn-off is postponed as shown in Figure 11b, where V_S is 44 mV corresponding to a V_{CC} equal to 14 V. The complementary MOSFET Q4 turn-on is then anticipated with a dead-time reduced to 150 µs.

3.2 Start-up waveforms

Active-bridge behavior during PFC start-up is checked by mounting the **KIT_ACT_BRD_60R065S7** on the 2400 W CCM PFC demo board **EVAL_2K4W_ACT_BRD_S7**. The test is perfomed at light load. As shown in Figure 12 the active bridge is activated only when the PFC starts boosting the current in order to reach the target output voltage. After that, since the load is very low, the active bridge is not triggered.

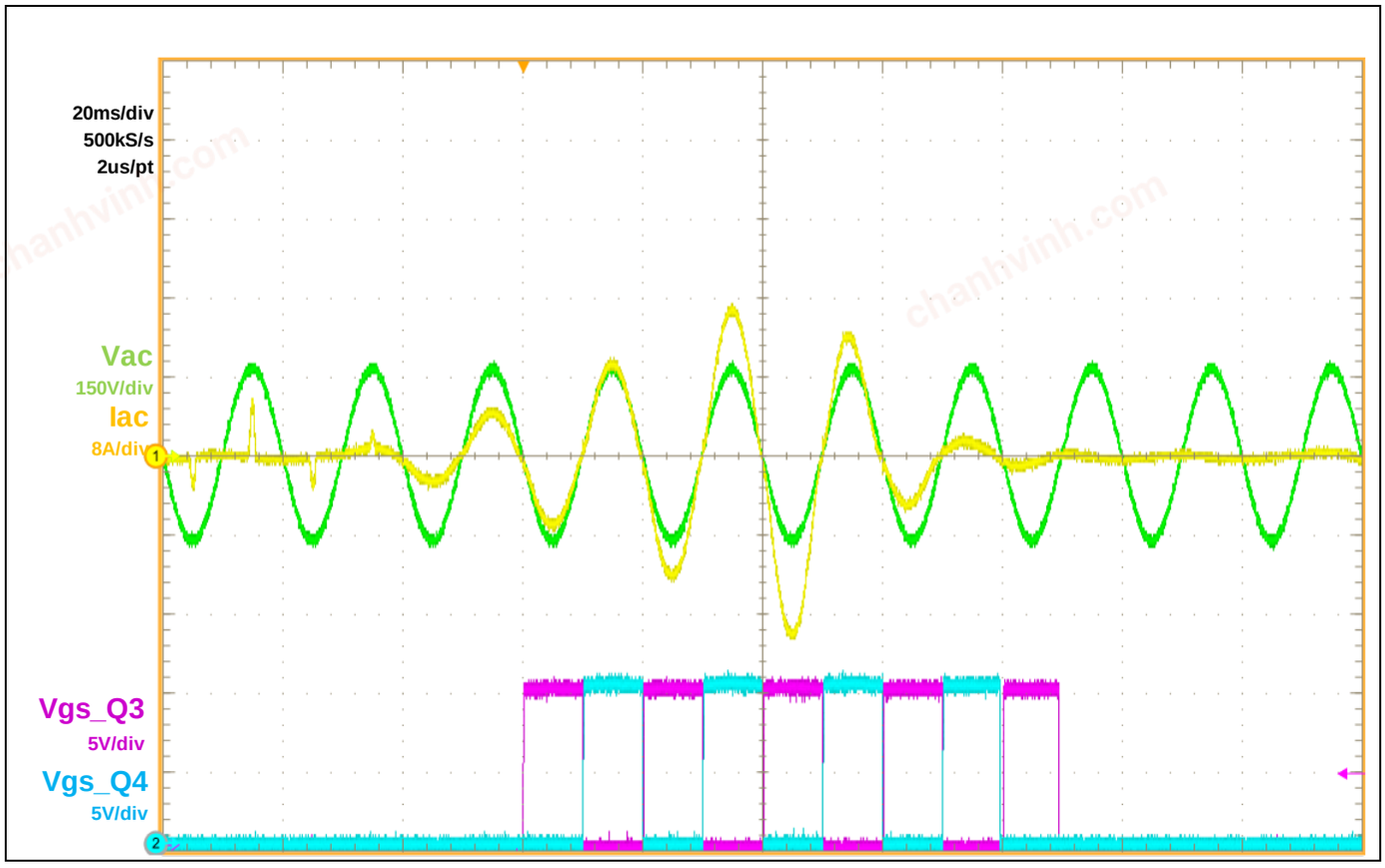


Figure 12 PFC start-up waveforms of active-bridge low-side complementary driving signals (magenta and light blue lines), input current and voltage (yellow and green lines) and PFC output voltage (light blue line) at 115 V AC and V_{out} = 390 V

3.3 Efficiency measurements

The efficiency measurements are performed by mounting the **KIT_ACT_BRD_60R065S7** on the 2400 W CCM PFC demo board **EVAL_2K4W_ACT_BRD_S7**. Load is changed through a DC electronic load and the output voltage is kept constant by the PFC at around 390 V DC.

Results at nominal low-line (115 V AC) and high-line (230 V AC) are shown in Figure 13, making a comparison with the standard diode bridge case. The fan consumption is included in the efficiency calculation.

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A peak efficiency of 98.4 percent is reached with the 65 Ω active bridge at around 50 percent of the output power.

A peak efficiency of 97 percent is reached with the 65 mΩ active bridge at around 50 percent of the output power.

From Figure 13 it is also evident that the PFC efficiency with the **KIT_ACT_BRD_60R065S7** is above 98 percent in almost all the load conditions, reaching the diode bridge performance only when the output power is around 2400 W.

The 65 mΩ active bridge's major benefit is given below 50 percent of the output power, especially at low-line.

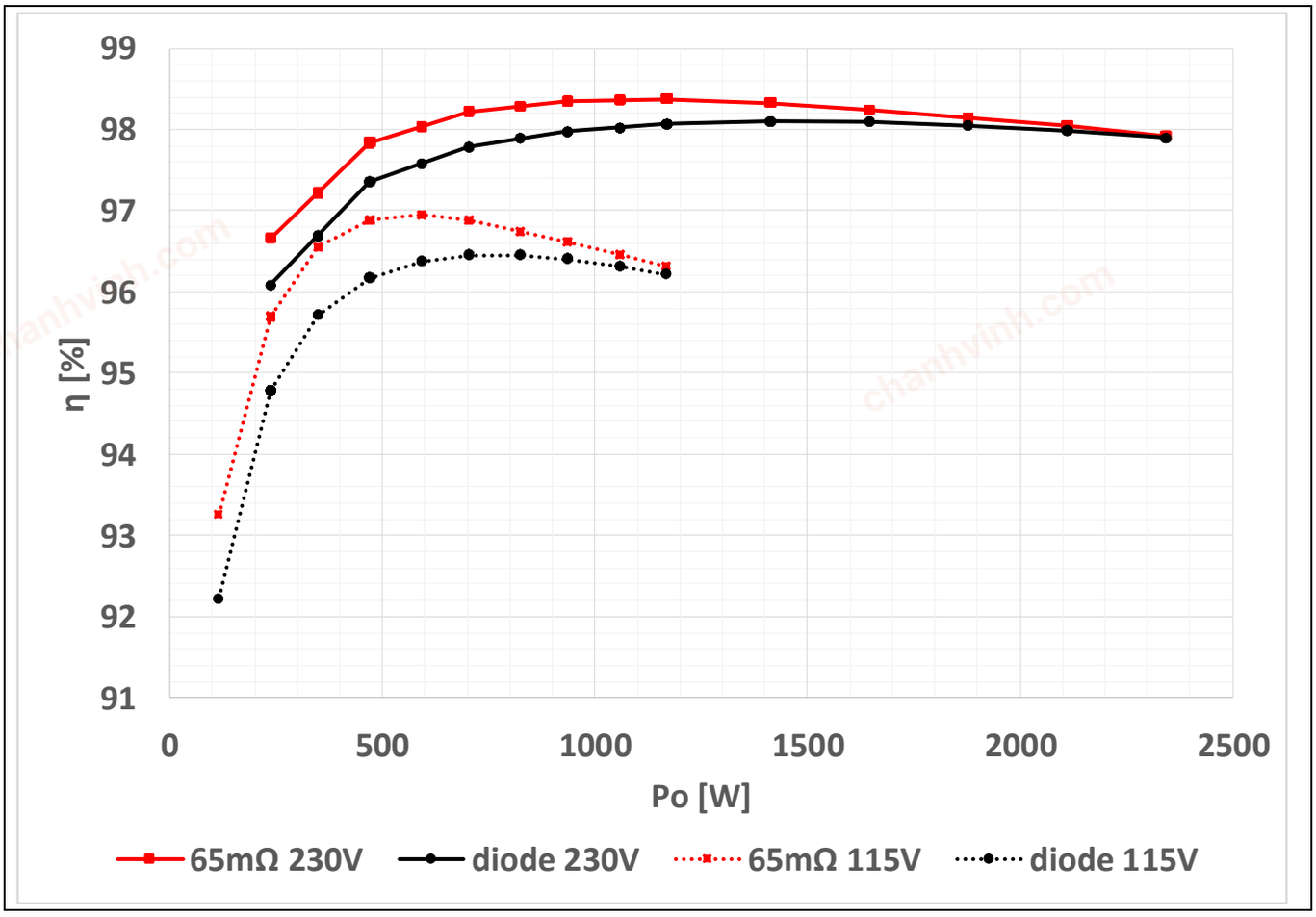


Figure 13 Efficiency test result of EVAL_2K4W_ACT_BRD_S7 with and without KIT_ACT_BRD_60R065S7 at both low-line (115 V AC) and high-line (230 V AC)

3.4 Temperature measurements

A long-run test has been performed with thermocouples attached to the main devices of the **EVAL_2K4W_ACT_BRD_S7** board, such as the active bridge (**KIT_ACT_BRD_60R065S7**) and the standard diode bridge. The test has been run for nominal input voltage (230 V AC) as well as the minimum input voltage (90 V AC), which is the worst case for PFC operation. The tested unit was enclosed and the fan was controlled by the bias Flyback supplied from the output voltage of the PFC. Therefore, the results presented in this section provide the thermal performance of the 2400 W active-bridge PFC with Infineon semiconductors introduced in this document at room temperature.

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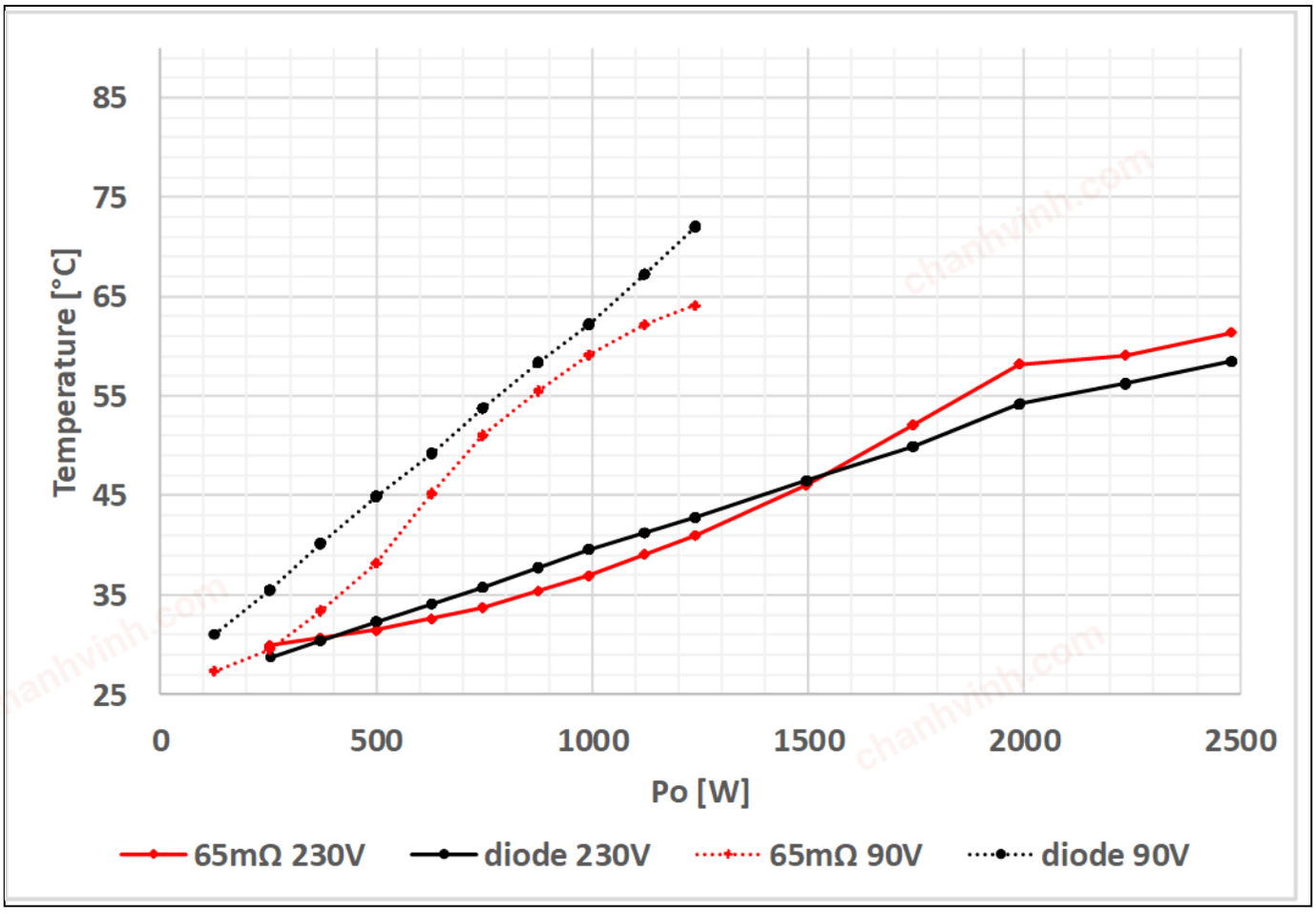


Figure 14 Bridge temperature result of EVAL_2K4W_ACT_BRD_S7 with and without KIT_ACT_BRD_60R065S7 at both low-line (115 V AC) and high-line (230 V AC)

Figure 14 shows the temperature evolution of the bridge (passive or active) from 10 percent to 100 percent of the output power at high-line (230 V AC) and from 5 percent to 50 percent at the minimum low-line (90 V AC).

The active bridge temperature reaches a maximum of 64°C at 1200 W/90 V with a delta of -9°C compared to the passive bridge case. On the other hand, at high-line Figure 14 shows that a maximum temperature of 63°C is reached by the active bridge with a delta of +2°C compared to the passive bridge case, with a break-even point at around 1500 W.

Please note that in the **EVAL_2K4W_ACT_BRD_S7** the diode bridge is always present for surge protection purposes.

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4 Summary

Active-bridge line rectification is a circuit which can improve efficiency within entire power ranges for high efficiency and high power density in SMPS. It demonstrates a flexible design with different daughter board MOSFET $R_{DS(on)}$ for various efficiency requirements of different applications without any other circuit modification.

Steady-state waveforms are documented, as well as indication of how to tune some control parameters depending on the application.

Start-up waveforms and efficiency improvement results with active-bridge line rectification are demonstrated in a 2400 W PFC.

A schematic of a reference circuit is provided in this application note, so that readers can design and manufacture an active-bridge line rectification board following the concept.

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5 Schematics

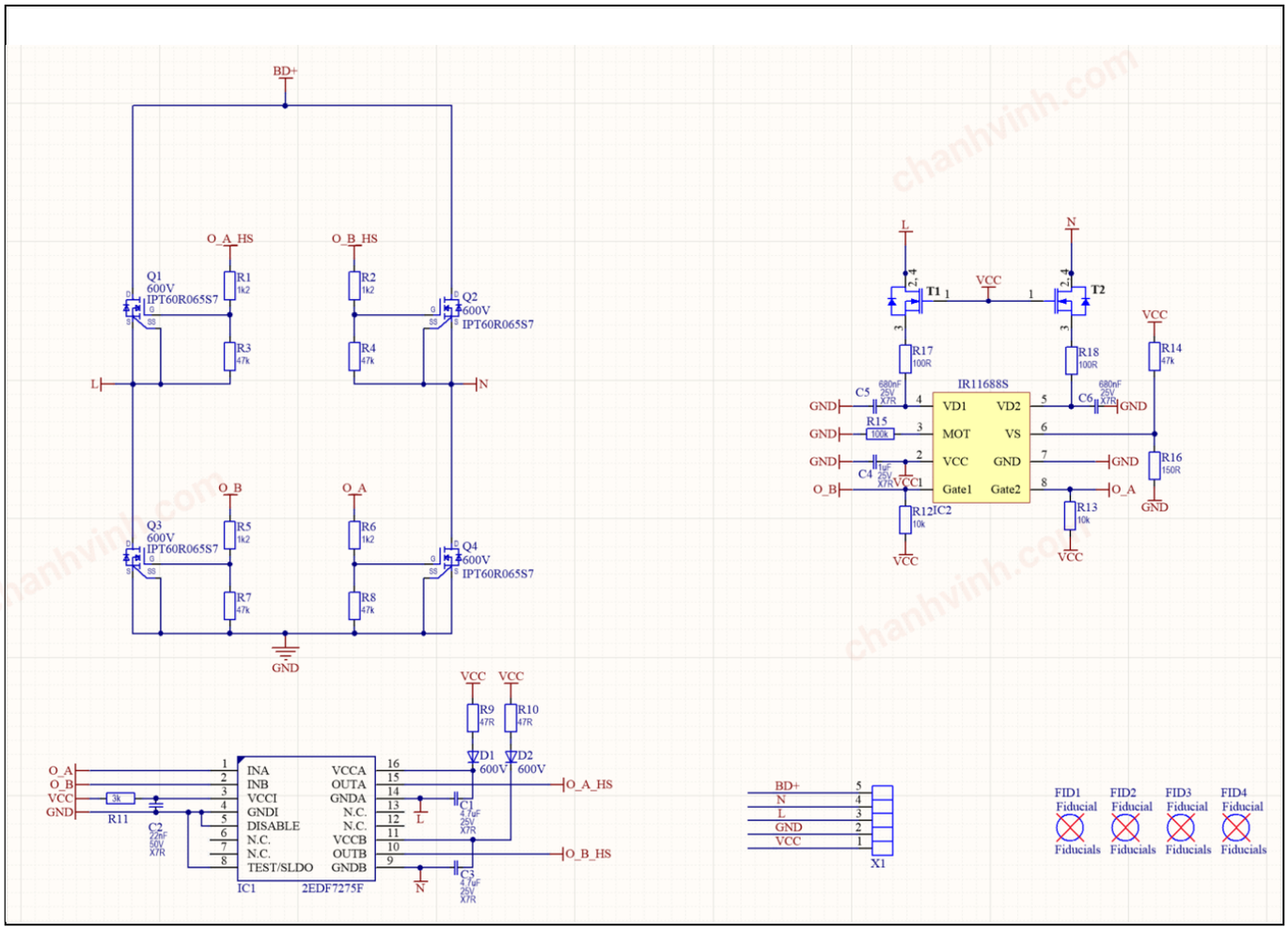


Figure 15 Active-bridge daughter card schematic

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6 PCB layout

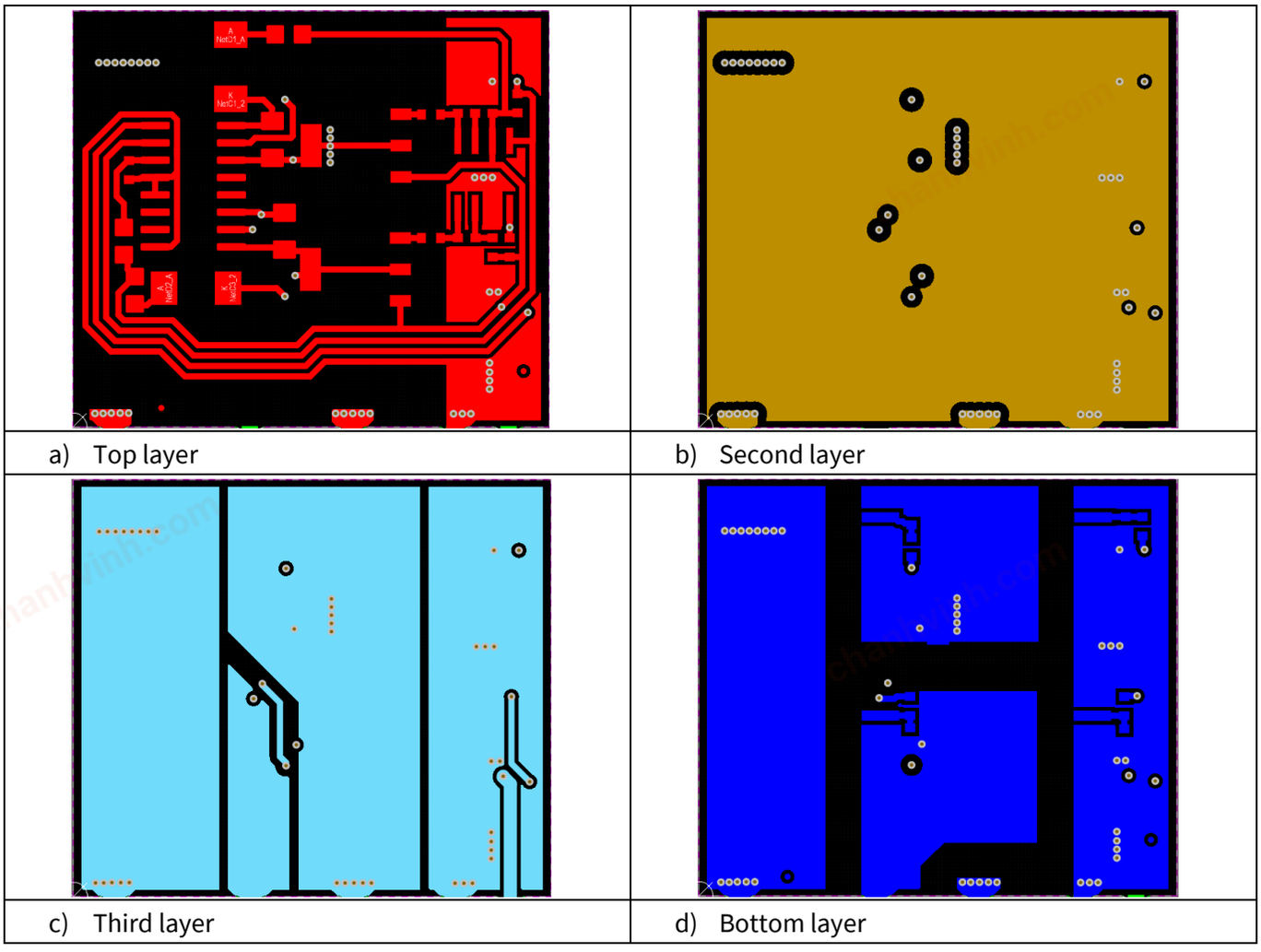


Figure 16 Active-bridge daughter card PCB layout: a) top, b) second, c) third and d) bottom layers

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7 Bill of Materials (BOM)

Table 2 Active-bridge daughter card components

Designator	Comment	Value	Tolerance	Voltage	Description
C1, C3	SMD	4.7 µF	X7R	25 V	Ceramic capacitor
C2	SMD	22 nF	X7R	50 V	Ceramic capacitor
C4	SMD	1 µF	X7R	25 V	Ceramic capacitor
C5, C6	SMD	680 nF	X7R	25 V	Ceramic capacitor
D1, D2	SMD	MURS360BT3G		600 V	Standard diode
IC1	SMD	2EDF7275F			Integrated circuit
IC2	SMD	IR11688S			Integrated circuit
Q1, Q2, Q3, Q4	SMD	IPT60R065S7		600 V	N-channel MOSFET
R1, R2, R5, R6	SMD	1k2	1 percent		Resistor
R12, R13	SMD	10 k	1 percent		Resistor
R3, R4, R7, R8, R14	SMD	47 k	1 percent		Resistor
R9, R10	SMD	47 R	1 percent		Resistor
R11	SMD	3 k	1 percent		Resistor
R15	SMD	100 k	1 percent		Resistor
R16	SMD	150 R	1 percent		Resistor
R17, R18	SMD	100 R	1 percent		Resistor
T1, T2	SMD	BSP300H6327XUSA1		800 V	N-channel MOSFET

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8 References

[1] “CCM PFC demo board with CoolMOS™ S7 for active line rectification and inrush current control” AN_1912_PL52_2002_103313.

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Revision history

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