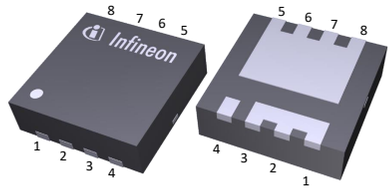
chanhvinh.com



# MOSFET

## OptiMOS™5 Power-Transistor, 100 V

PG-TSDSON-8 FL

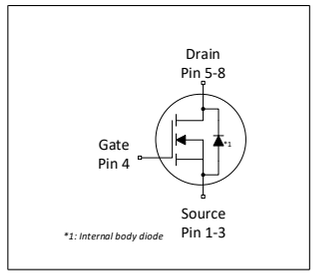



### Features

- Ideal for high-frequency switching
- Optimized for chargers
- 100% avalanche tested
- Superior thermal resistance
- N-channel, logic level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

### Product validation

Qualified according to JEDEC Standard




### Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 100 | V |
| $R_{DS(on),max}$ | 16.9 | mΩ |
| $I_D$ | 37 | A |
| $Q_{oss}$ | 16 | nC |
| $Q_G$(0V..4.5V) | 6 | nC |

| Type / Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| ISZ0803NLS | PG-TSDSON-8 FL | 0803NL | - |

chanhvinh.com



## Table of Contents

Description . . . . . 1
Maximum ratings . . . . . 3
Thermal characteristics . . . . . 3
Electrical characteristics . . . . . 4
Electrical characteristics diagrams . . . . . 6
Package Outlines . . . . . 10
Revision History . . . . . 11
Trademarks . . . . . 11
Disclaimer . . . . . 11

chanhvinh.com



# 1 Maximum ratings

at $T_A$=25 °C, unless otherwise specified

**Table 2 Maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current[1] | $I_D$ | -<br>-<br>- | -<br>-<br>- | 37<br>23<br>7.7 | A | $V_{GS}$=10 V, $T_C$=25 °C<br>$V_{GS}$=10 V, $T_C$=100 °C<br>$V_{GS}$=10 V, $T_A$=25 °C, $R_{thJA}$=60 °C/W[2] |
| Pulsed drain current[3] | $I_{D,pulse}$ | - | - | 148 | A | $T_A$=25 °C |
| Avalanche energy, single pulse[4] | $E_{AS}$ | - | - | 25 | mJ | $I_D$=20 A, $R_{GS}$=25 Ω |
| Gate source voltage | $V_{GS}$ | -20 | - | 20 | V | - |
| Power dissipation | $P_{tot}$ | -<br>- | -<br>- | 43<br>2.1 | W | $T_C$=25 °C<br>$T_A$=25 °C, $R_{thJA}$=60 °C/W[2] |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | - | 150 | °C | IEC climatic category; DIN IEC 68-1: 55/150/56 |

# 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case, bottom | $R_{thJC}$ | - | 1.7 | 2.9 | °C/W | - |
| Thermal resistance, junction - case, top | $R_{thJC}$ | - | - | 20 | °C/W | - |
| Device on PCB, 6 cm² cooling area [2] | $R_{thJA}$ | - | - | 60 | °C/W | - |

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

chanhvinh.com



# 3 Electrical characteristics

at $T_j$=25 °C, unless otherwise specified

## Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 100 | - | - | V | $V_{GS}$=0 V, $I_D$=1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 1.1 | 1.6 | 2.3 | V | $V_{DS}$=$V_{GS}$, $I_D$=18 µA |
| Zero gate voltage drain current | $I_{DSS}$ | -<br>- | 0.1<br>10 | 1<br>100 | µA | $V_{DS}$=100 V, $V_{GS}$=0 V, $T_j$=25 °C<br>$V_{DS}$=100 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 10 | 100 | nA | $V_{GS}$=20 V, $V_{DS}$=0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | -<br>- | 15.5<br>20.1 | 16.9<br>21.9 | mΩ | $V_{GS}$=10 V, $I_D$=20 A<br>$V_{GS}$=4.5 V, $I_D$=10 A |
| Gate resistance[1)] | $R_G$ | - | 1.0 | - | Ω | - |
| Transconductance | $g_{fs}$ | - | 32 | - | S | $\lvert V_{DS}\rvert \geq 2 \lvert I_D\rvert R_{DS(on)max}$, $I_D$=20 A |

## Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance[1)] | $C_{iss}$ | - | 790 | 1000 | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=1 MHz |
| Output capacitance[1)] | $C_{oss}$ | - | 140 | 180 | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=1 MHz |
| Reverse transfer capacitance[1)] | $C_{rss}$ | - | 7.1 | 12 | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=1 MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 5.6 | - | ns | $V_{DD}$=50 V, $V_{GS}$=4.5 V, $I_D$=20 A, $R_{G,ext}$=3 Ω |
| Rise time | $t_r$ | - | 4.0 | - | ns | $V_{DD}$=50 V, $V_{GS}$=4.5 V, $I_D$=20 A, $R_{G,ext}$=3 Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 10 | - | ns | $V_{DD}$=50 V, $V_{GS}$=4.5 V, $I_D$=20 A, $R_{G,ext}$=3 Ω |
| Fall time | $t_f$ | - | 2.2 | - | ns | $V_{DD}$=50 V, $V_{GS}$=4.5 V, $I_D$=20 A, $R_{G,ext}$=3 Ω |

## Table 6 Gate charge characteristics[2)]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 2.6 | - | nC | $V_{DD}$=50 V, $I_D$=20 A, $V_{GS}$=0 to 4.5 V |
| Gate charge at threshold | $Q_{g(th)}$ | - | 1.3 | - | nC | $V_{DD}$=50 V, $I_D$=20 A, $V_{GS}$=0 to 4.5 V |
| Gate to drain charge | $Q_{gd}$ | - | 2.2 | - | nC | $V_{DD}$=50 V, $I_D$=20 A, $V_{GS}$=0 to 4.5 V |
| Switching charge | $Q_{sw}$ | - | 3.5 | - | nC | $V_{DD}$=50 V, $I_D$=20 A, $V_{GS}$=0 to 4.5 V |
| Gate charge total[1)] | $Q_g$ | - | 6.0 | 7 | nC | $V_{DD}$=50 V, $I_D$=20 A, $V_{GS}$=0 to 4.5 V |
| Gate plateau voltage | $V_{plateau}$ | - | 3.3 | - | V | $V_{DD}$=50 V, $I_D$=20 A, $V_{GS}$=0 to 4.5 V |
| Gate charge total[1)] | $Q_g$ | - | 11 | 15 | nC | $V_{DD}$=50 V, $I_D$=20 A, $V_{GS}$=0 to 10 V |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | - | 10 | - | nC | $V_{DS}$=0.1 V, $V_{GS}$=0 to 10 V |
| Output charge | $Q_{oss}$ | - | 16 | - | nC | $V_{DS}$=50 V, $V_{GS}$=0 V |

[1)] Defined by design. Not subject to production test.
[2)] See "Gate charge waveforms" for parameter definition

chanhvinh.com



## Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | $I_S$ | - | - | 37 | A | $T_C$=25 °C |
| Diode pulse current | $I_{S,pulse}$ | - | - | 148 | A | $T_C$=25 °C |
| Diode forward voltage | $V_{SD}$ | - | 0.89 | 1.0 | V | $V_{GS}$=0 V, $I_F$=20 A, $T_j$=25 °C |
| Reverse recovery time[1)] | $t_{rr}$ | - | 31 | - | ns | $V_R$=50 V, $I_F$=20 A, d$i_F$/d$t$=100 A/µs |
| Reverse recovery charge[1)] | $Q_{rr}$ | - | 25 | - | nC | $V_R$=50 V, $I_F$=20 A, d$i_F$/d$t$=100 A/µs |

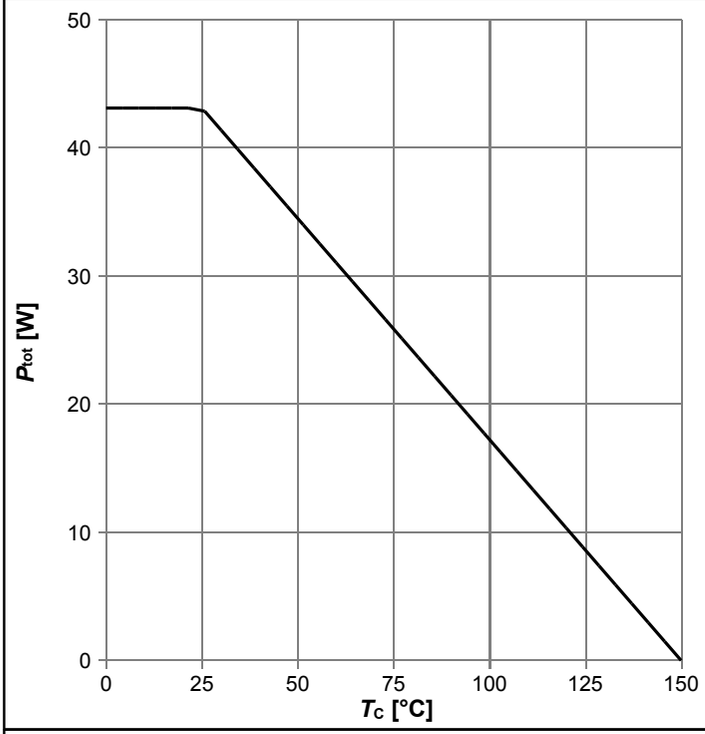
[1)] Defined by design. Not subject to production test.

chanhvinh.com



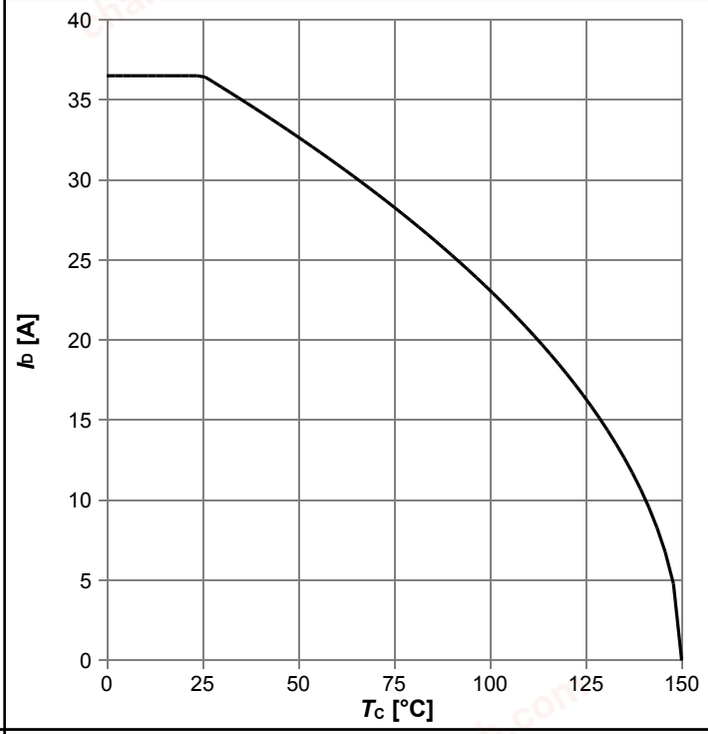
# 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



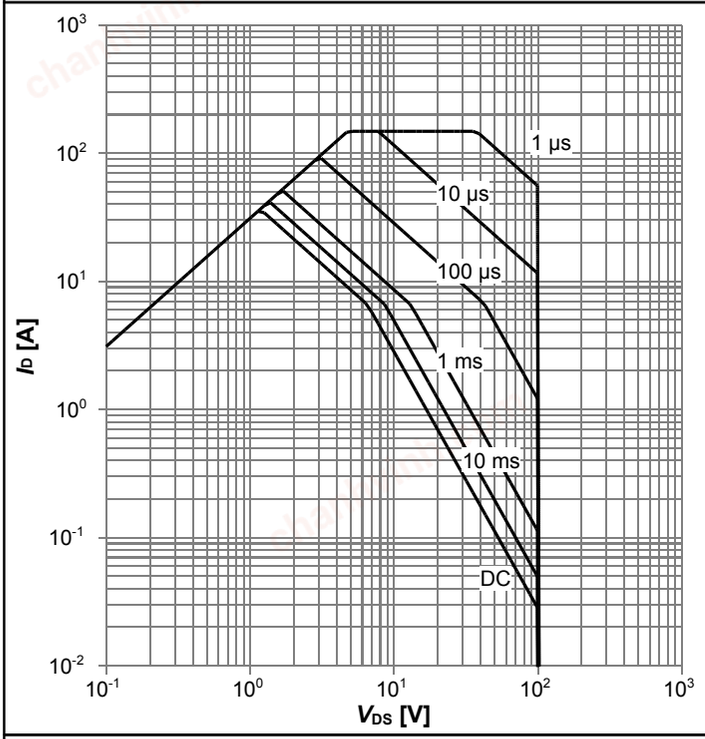

$P_{tot}=f(T_C)$

**Diagram 2: Drain current**



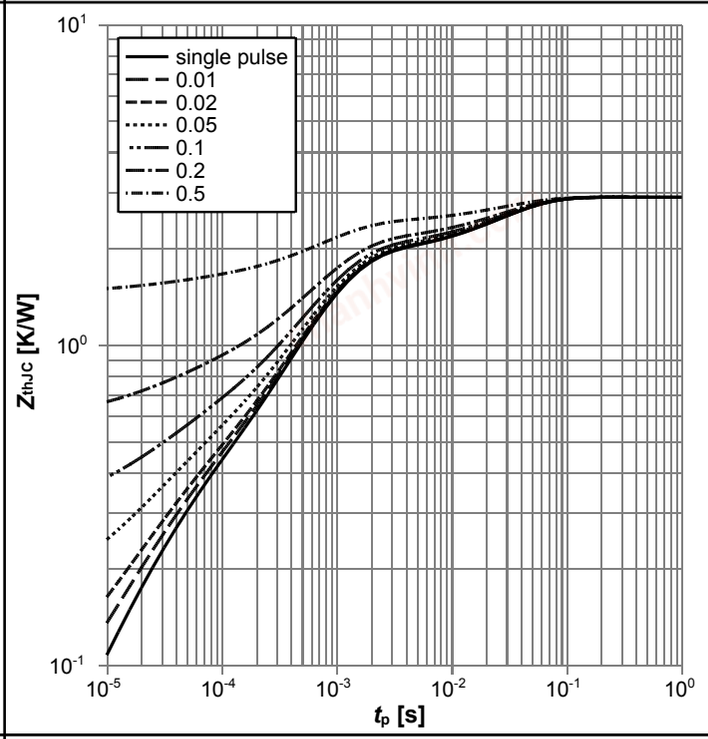

$I_D=f(T_C)$; $V_{GS}\geq 10$ V

**Diagram 3: Safe operating area**




$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**

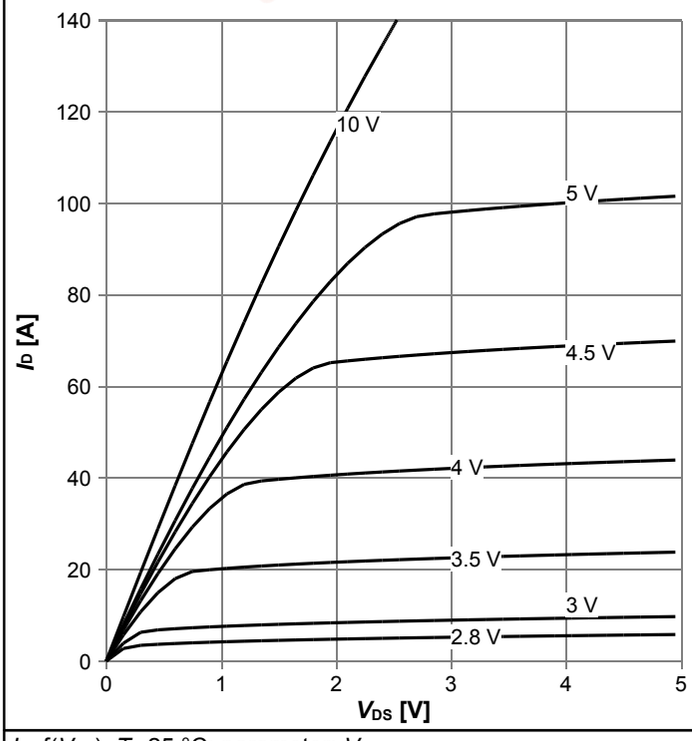



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

chanhvinh.com

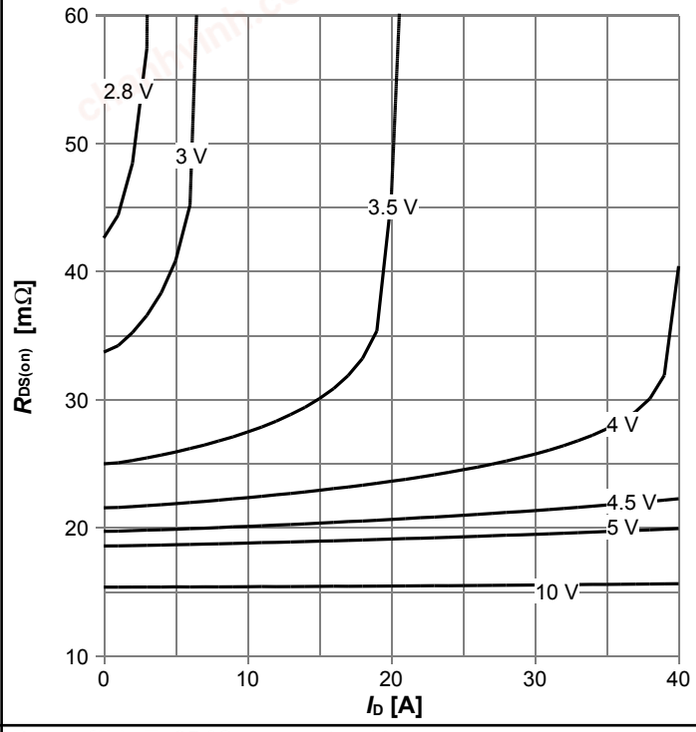


**Diagram 5: Typ. output characteristics**



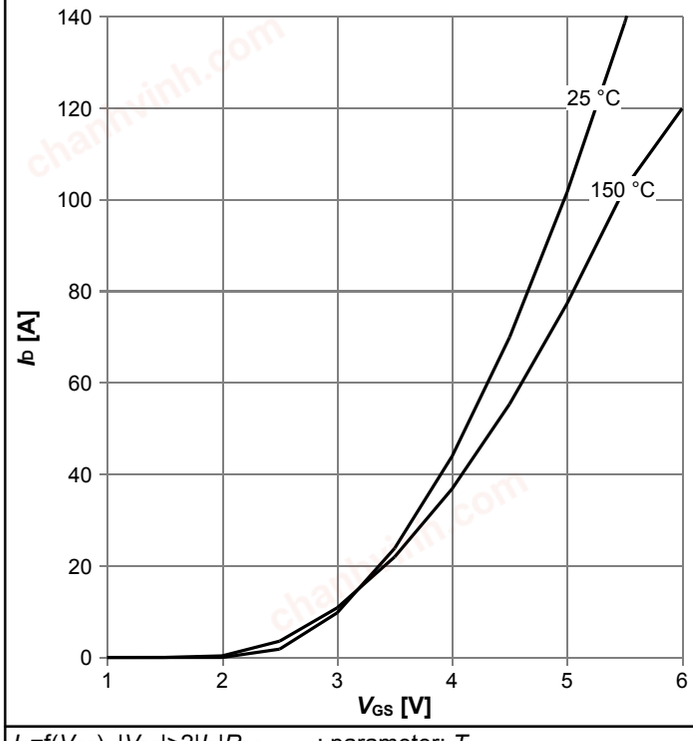

$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



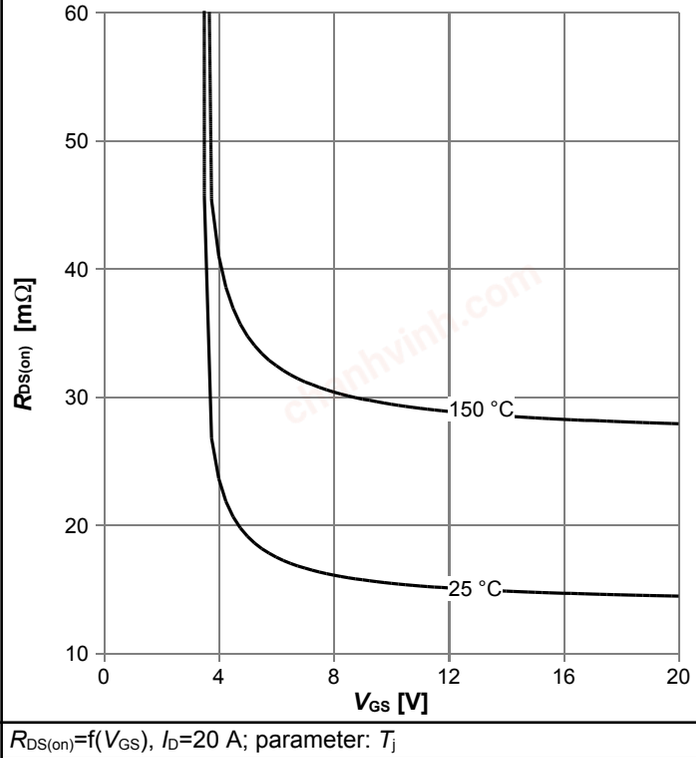

$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: $V_{GS}$

**Diagram 7: Typ. transfer characteristics**




$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: $T_j$

**Diagram 8: Typ. drain-source on resistance**

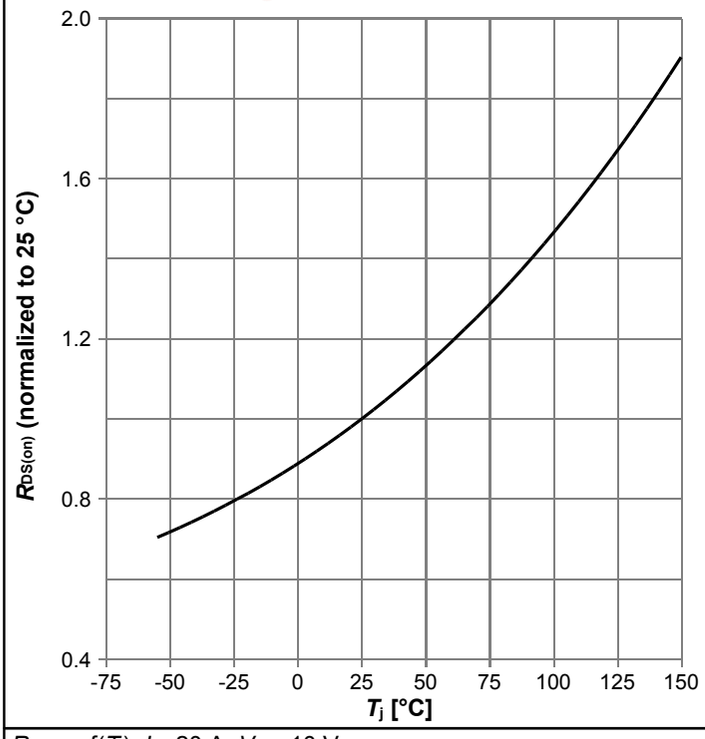



$R_{DS(on)}=f(V_{GS})$, $I_D=20$ A; parameter: $T_j$

chanhvinh.com

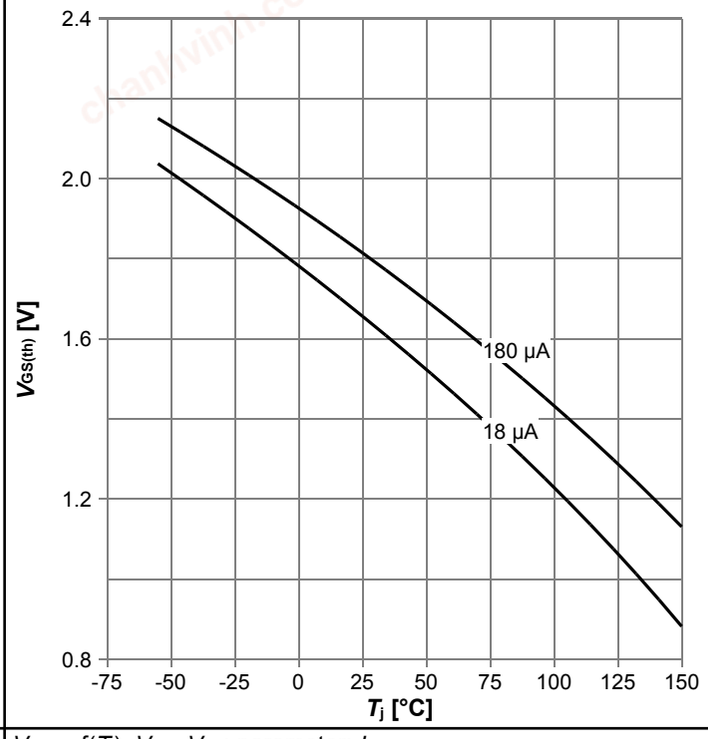


**Diagram 9: Normalized drain-source on resistance**



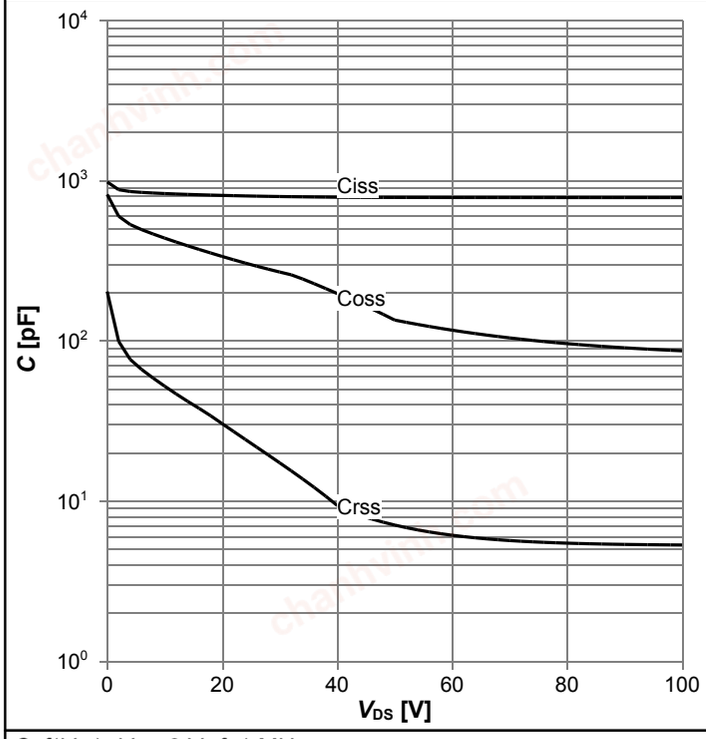

$R_{DS(on)}$=f($T_j$), $I_D$=20 A, $V_{GS}$=10 V

**Diagram 10: Typ. gate threshold voltage**



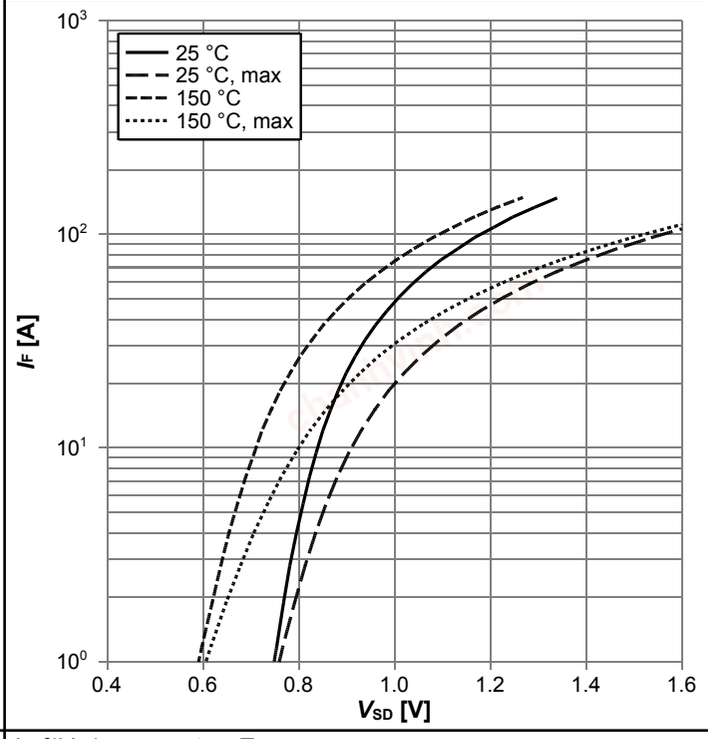

$V_{GS(th}$=f($T_j$), $V_{GS}$=$V_{DS}$; parameter: $I_D$

**Diagram 11: Typ. capacitances**




$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

**Diagram 12: Forward characteristics of reverse diode**

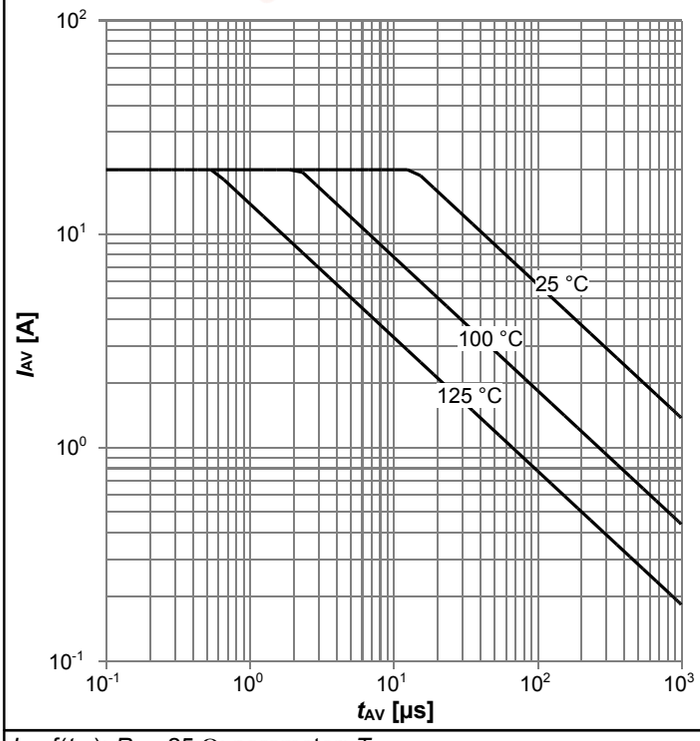



$I_F$=f($V_{SD}$); parameter: $T_j$

chanhvinh.com

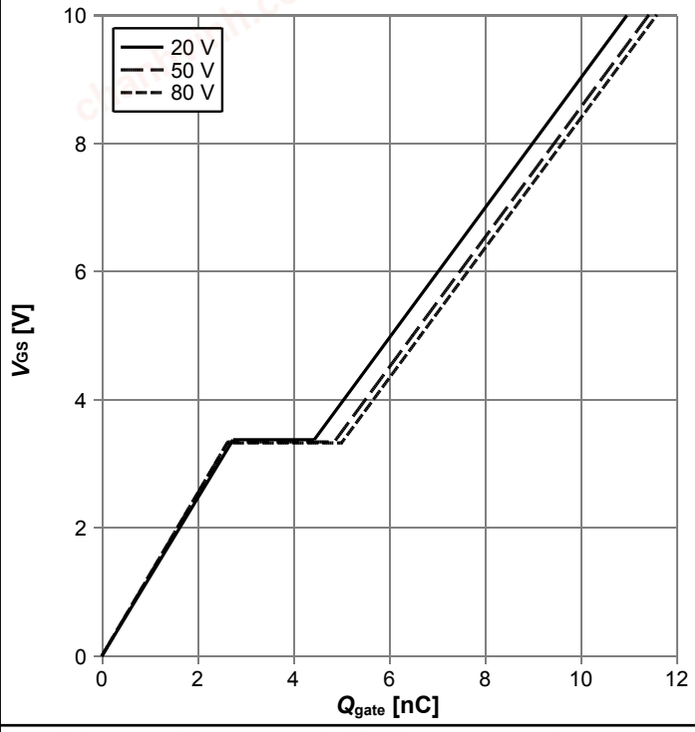


**Diagram 13: Avalanche characteristics**



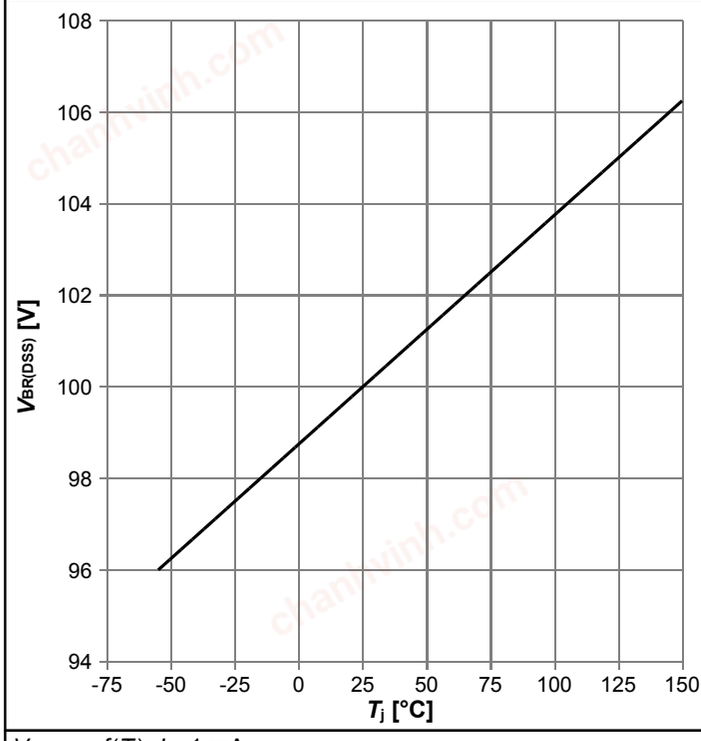

$I_{AS}$=f($t_{AV}$); $R_{GS}$=25 Ω; parameter: $T_{j,start}$

**Diagram 14: Typ. gate charge**



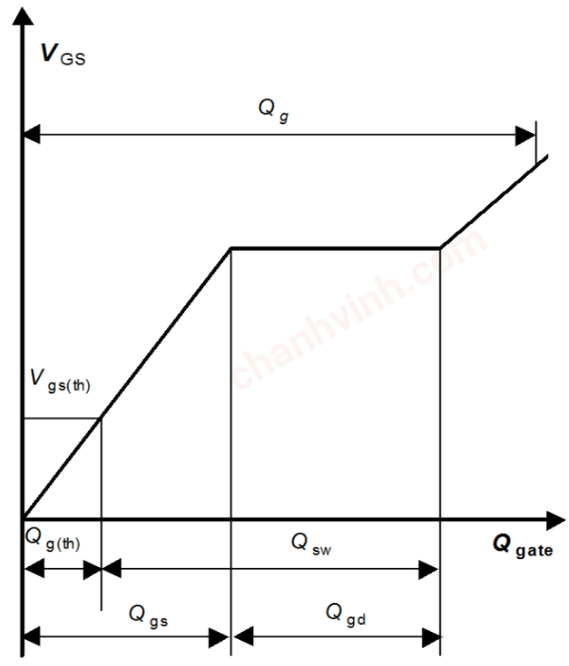

$V_{GS}$=f($Q_{gate}$), $I_D$=20 A pulsed, $T_j$=25 °C; parameter: $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**




$V_{BR(DSS)}$=f($T_j$); $I_D$=1 mA

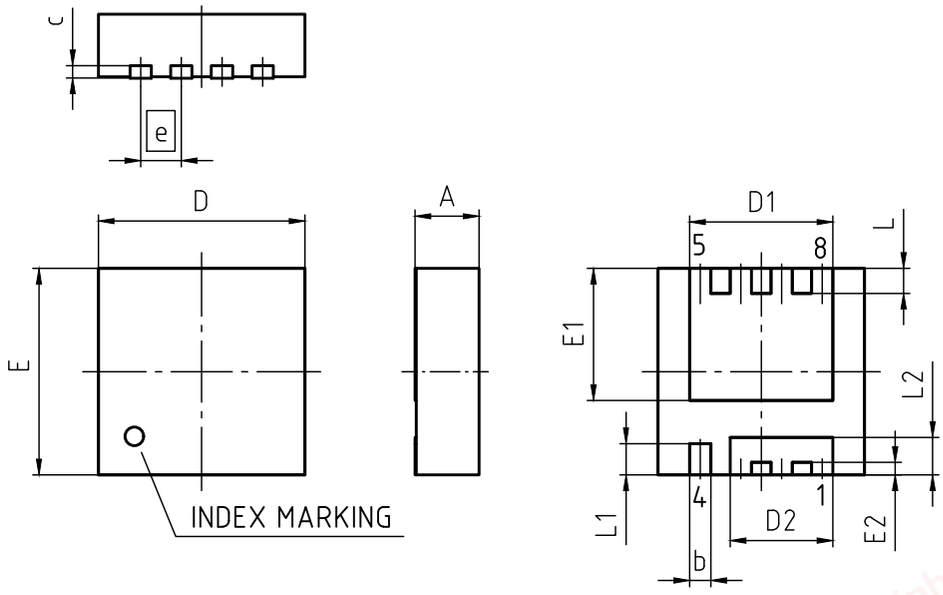
**Diagram Gate charge waveforms**



chanhvinh.com



# 5 Package Outlines




| PACKAGE - GROUP NUMBER: | PG-TSDSON-8-U03 | |
|---|---|---|
| REVISION: 03 | DATE: 20.10.2020 | |
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 0.90 | 1.10 |
| b | 0.24 | 0.44 |
| c | (0.20) | |
| D | 3.20 | 3.40 |
| D1 | 2.19 | 2.39 |
| D2 | 1.54 | 1.74 |
| E | 3.20 | 3.40 |
| E1 | 2.01 | 2.21 |
| E2 | 0.10 | 0.30 |
| e | 0.65 | |
| L | 0.30 | 0.50 |
| L1 | 0.40 | 0.60 |
| L2 | 0.50 | 0.70 |
| aaa | 0.06 | |

**Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm**

chanhvinh.com



## Revision History

ISZ0803NLS

**Revision: 2021-04-01, Rev. 2.1**

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 2.0 | 2021-03-22 | Release of final version |
| 2.1 | 2021-04-01 | Update of features list |

**Trademarks**
All referenced product or service names and trademarks are the property of their respective owners.

**We Listen to Your Comments**
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
**erratum@infineon.com**

**Published by**
**Infineon Technologies AG**
**81726 München, Germany**
**© 2020 Infineon Technologies AG**
**All Rights Reserved.**

**Legal Disclaimer**
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”) .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.
In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.
The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

**Information**
For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

**Warnings**
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.