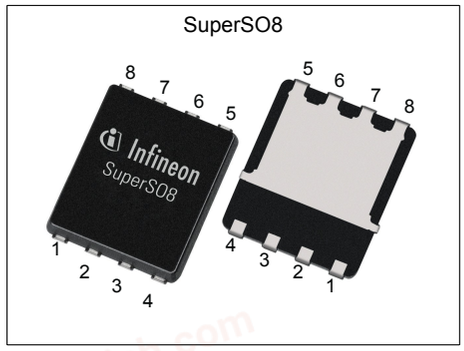
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MOSFET

OptiMOS™ Power Transistor, -60 V



Features

- P-Channel
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=-4.5 V
- 100% avalanche tested
- Logic Level
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

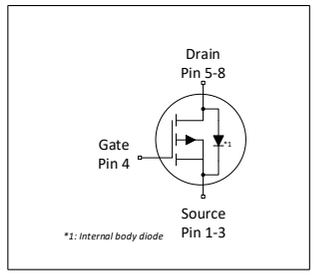


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-60	V
$R_{DS(on),max}$	24	mΩ
I_D	-59	A

Type / Ordering Code	Package	Marking	Related Links
ISC240P06LM	PG-TDSON-8	240P06LM	-

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - -	- - - -	-59 -41 -51 -36	A	V_{GS}=-10 V, T_C=25 °C V_{GS}=-10 V, T_C=100 °C V_{GS}=-4.5 V, T_C=25 °C V_{GS}=-4.5 V, T_C=100 °C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	-236	A	T_A=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	770	mJ	I_D=-46 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	188	W	T_A=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	0.8	°C/W	-
Device on PCB, 6 cm² cooling area[4]	R_{thJA}	-	-	50	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information
[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

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3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	-1	-1.5	-2	V	V_{DS}=V_{GS}, I_D=-2340 µA
Zero gate voltage drain current	I_{DSS}	- -	-0.1 -10	-1 -100	µA	V_{DS}=-60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=-60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	V_{GS}=-20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	20 24	24 32	mΩ	V_{GS}=-10 V, I_D=-40 A V_{GS}=-4.5 V, I_D=-32 A
Gate resistance	R_G	-	5	-	Ω	-
Transconductance	g_{fs}	-	62	-	S	|V_{DS}|≥2|I_D|$R_{DS(on)max}$, I_D=-40 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	3400	4400	pF	V_{GS}=0 V, V_{DS}=-30 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	480	620	pF	V_{GS}=0 V, V_{DS}=-30 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	110	190	pF	V_{GS}=0 V, V_{DS}=-30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	5	-	ns	V_{DD}=-30 V, V_{GS}=-10 V, I_D=-40 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	3	-	ns	V_{DD}=-30 V, V_{GS}=-10 V, I_D=-40 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	109	-	ns	V_{DD}=-30 V, V_{GS}=-10 V, I_D=-40 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	49	-	ns	V_{DD}=-30 V, V_{GS}=-10 V, I_D=-40 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-12	-	nC	V_{DD}=-30 V, I_D=-40 A, V_{GS}=0 to -4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	-5	-	nC	V_{DD}=-30 V, I_D=-40 A, V_{GS}=0 to -4.5 V
Gate to drain charge[1)]	Q_{gd}	-	-30	-45	nC	V_{DD}=-30 V, I_D=-40 A, V_{GS}=0 to -4.5 V
Switching charge	Q_{sw}	-	-37	-	nC	V_{DD}=-30 V, I_D=-40 A, V_{GS}=0 to -4.5 V
Gate charge total[1)]	Q_g	-	-51	-64	nC	V_{DD}=-30 V, I_D=-40 A, V_{GS}=0 to -4.5 V
Gate plateau voltage	$V_{plateau}$	-	-3.5	-	V	V_{DD}=-30 V, I_D=-40 A, V_{GS}=0 to -4.5 V
Gate charge total[1)]	Q_g	-	-102	-136	nC	V_{DD}=-30 V, I_D=-40 A, V_{GS}=0 to -10 V
Output charge[1)]	Q_{oss}	-	-36	-48	nC	V_{DD}=-30 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test
[2)] See diagram ,Gate charge waverforms, for gate charge parameter definition

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Table 7 Reverse diode

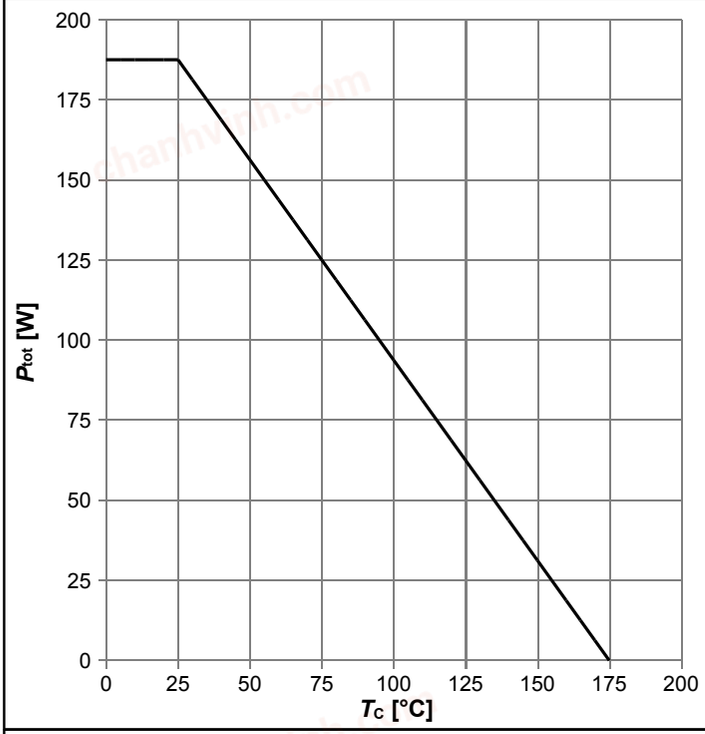
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-59	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	-236	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	-0.86	-1.2	V	V_{GS}=0 V, I_F=-40 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	75	150	ns	V_R=-30 V, I_F=-40 A, di_F/dt=-100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	-164	-328	nC	V_R=-30 V, I_F=-40 A, di_F/dt=-100 A/µs

[1)] Defined by design. Not subject to production test

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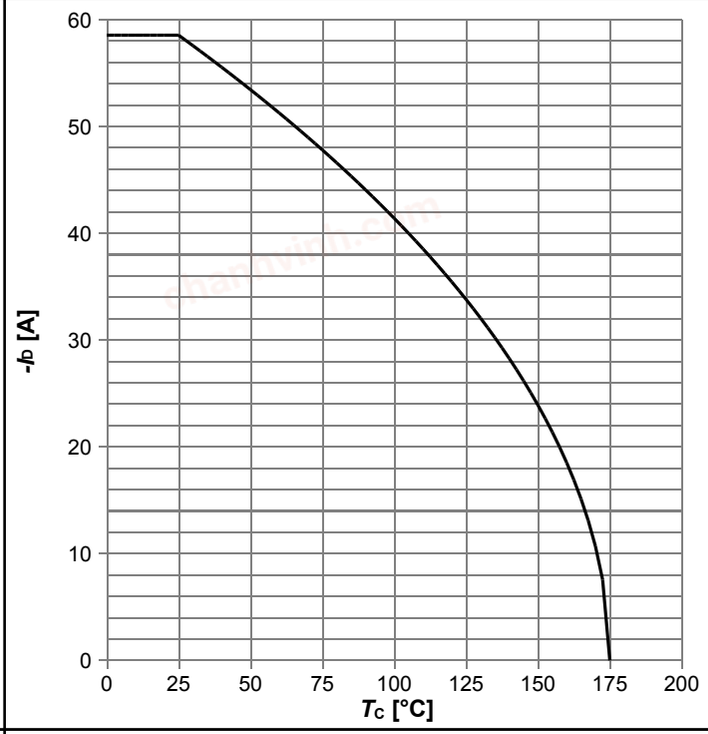
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



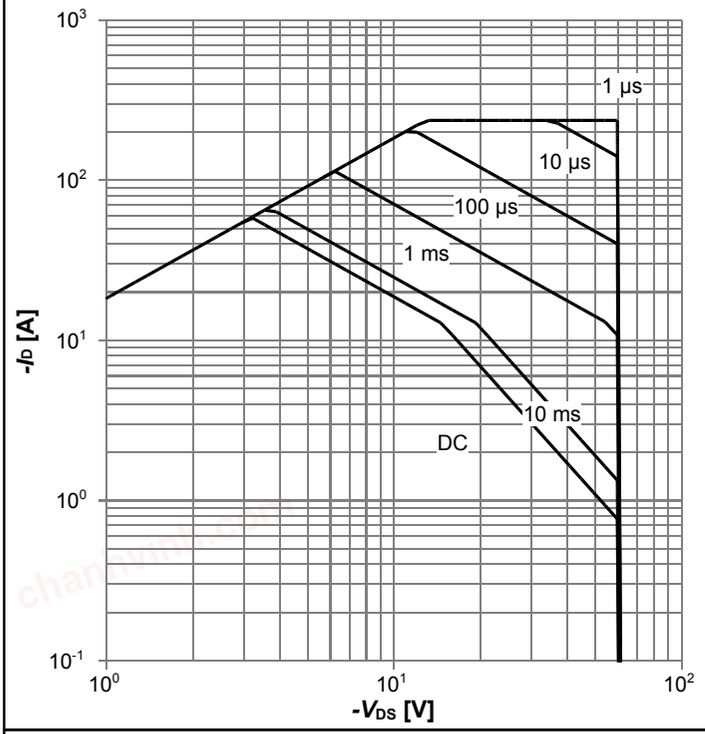
$P_{tot}=f(T_C)$

Diagram 2: Drain current



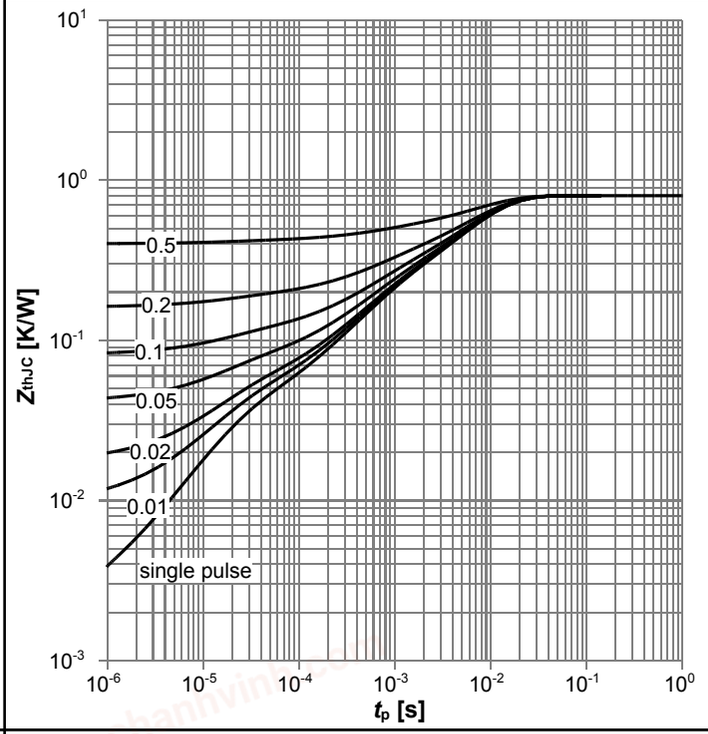
$I_D=f(T_C)$; $|V_{GS}|\geq 10$ V

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

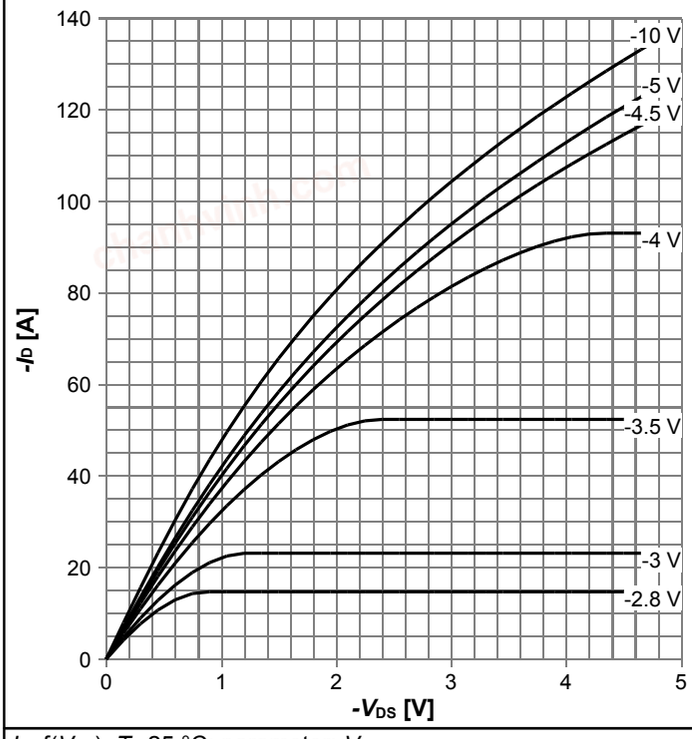
Diagram 4: Max. transient thermal impedance



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

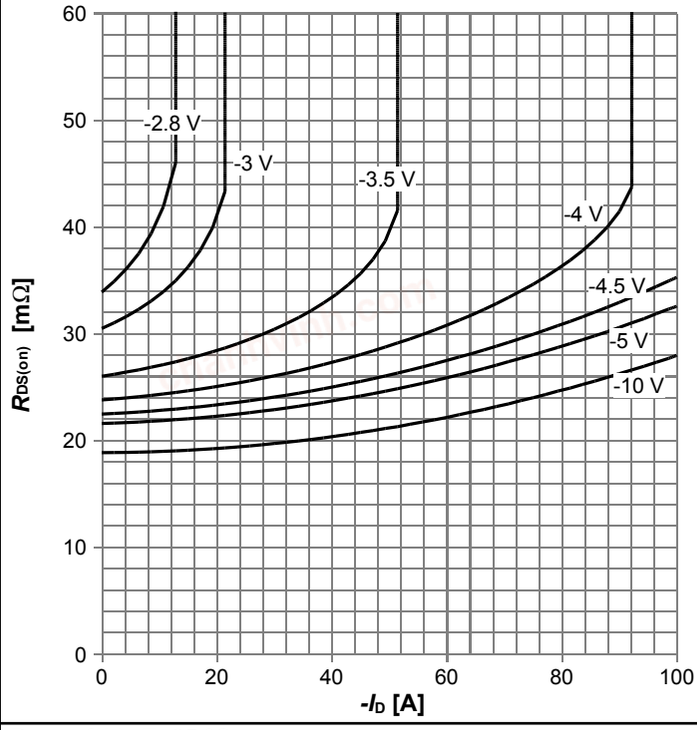
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Diagram 5: Typ. output characteristics



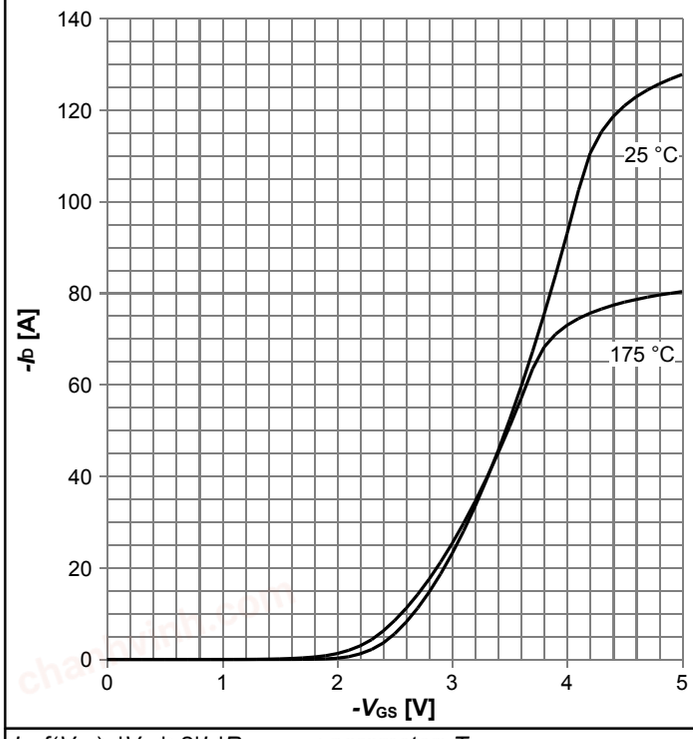
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



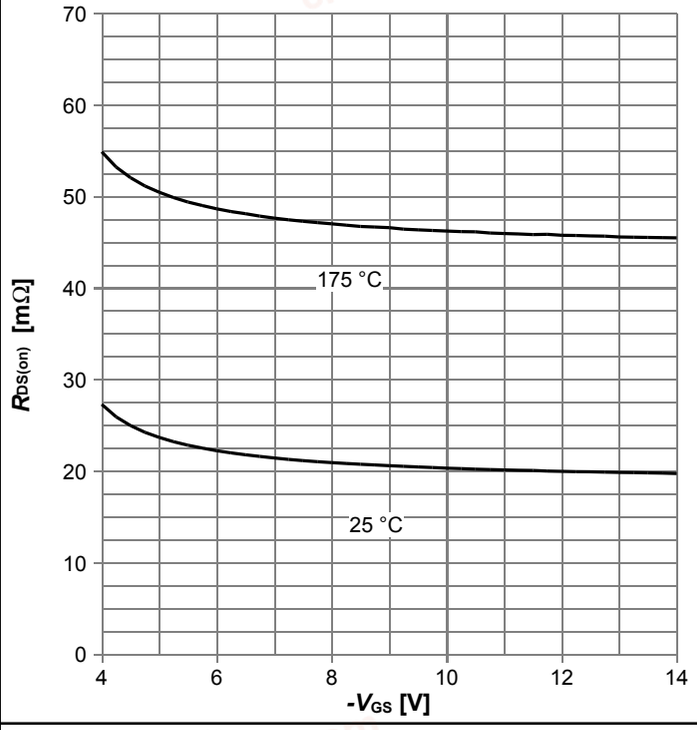
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

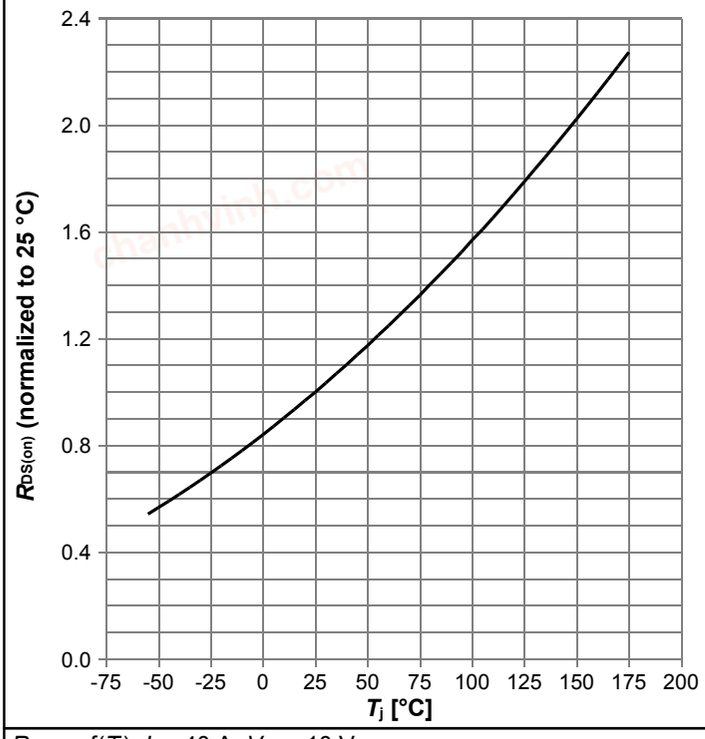
Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=-40 A; parameter: T_j

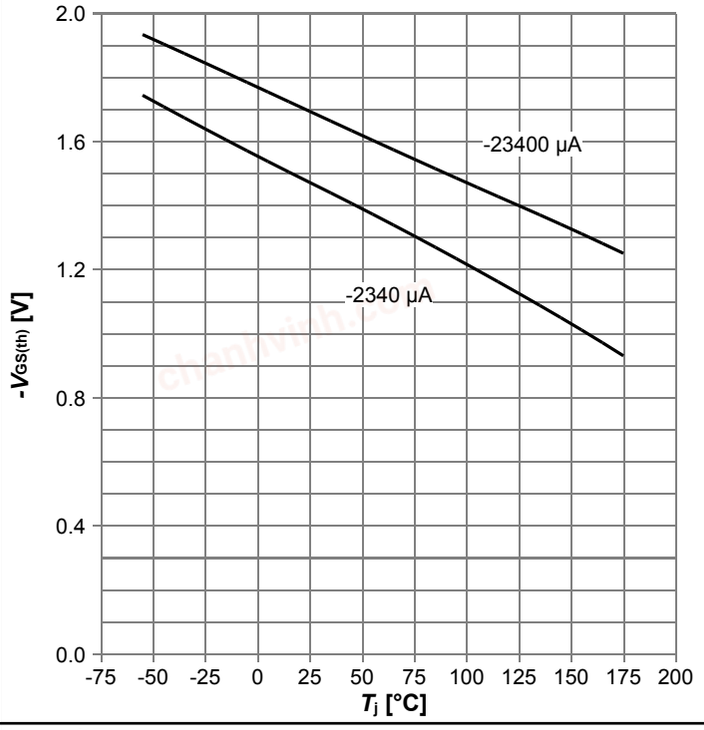
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Diagram 9: Normalized drain-source on resistance



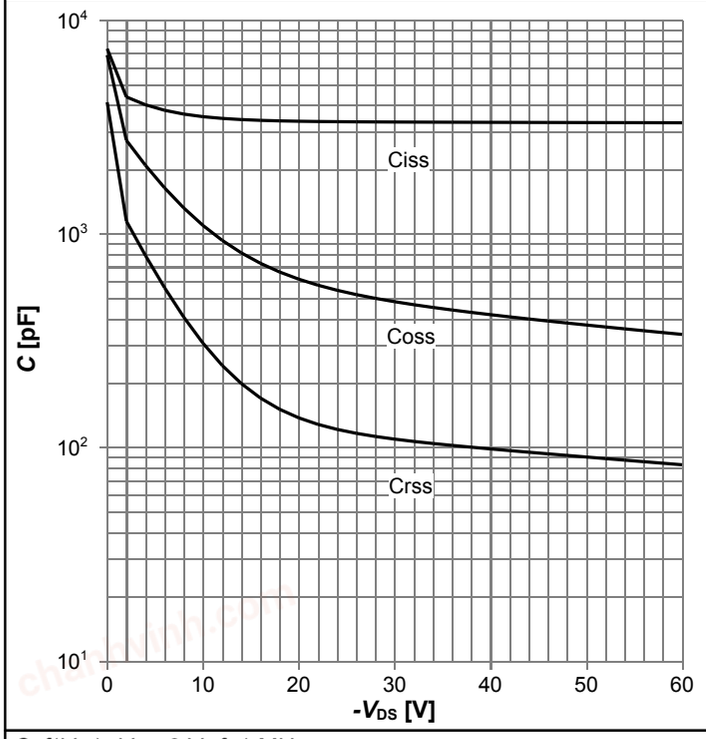
$R_{DS(on)}$=f(T_j), I_D=-40 A, V_{GS}=-10 V

Diagram 10: Typ. gate threshold voltage



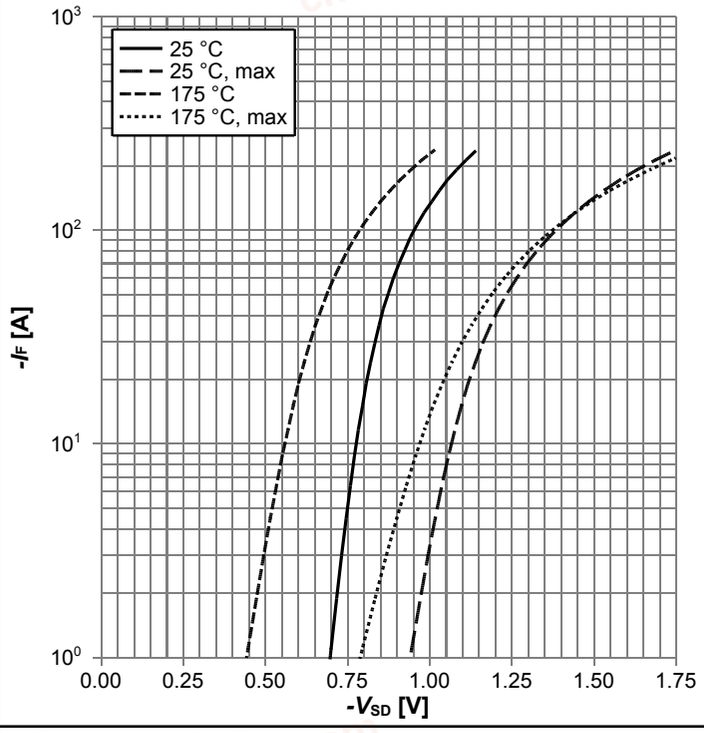
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

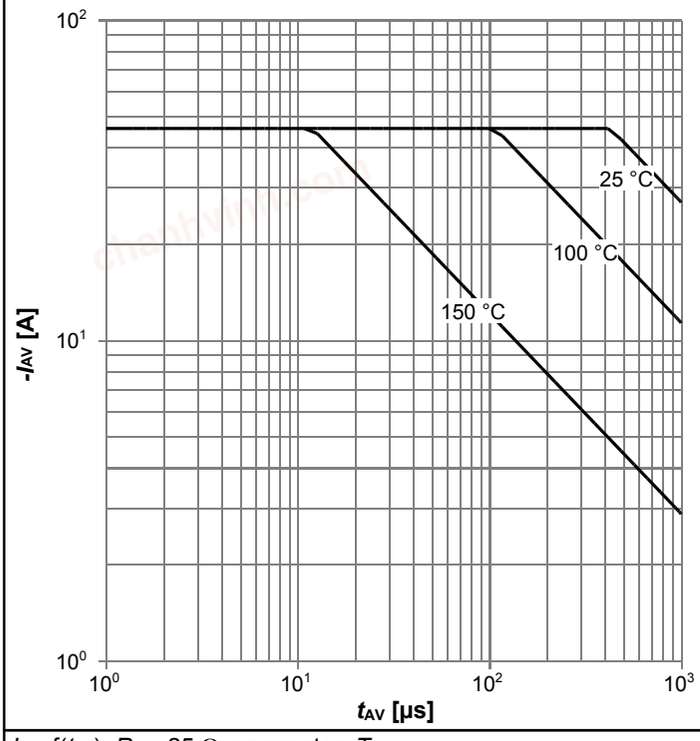
Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

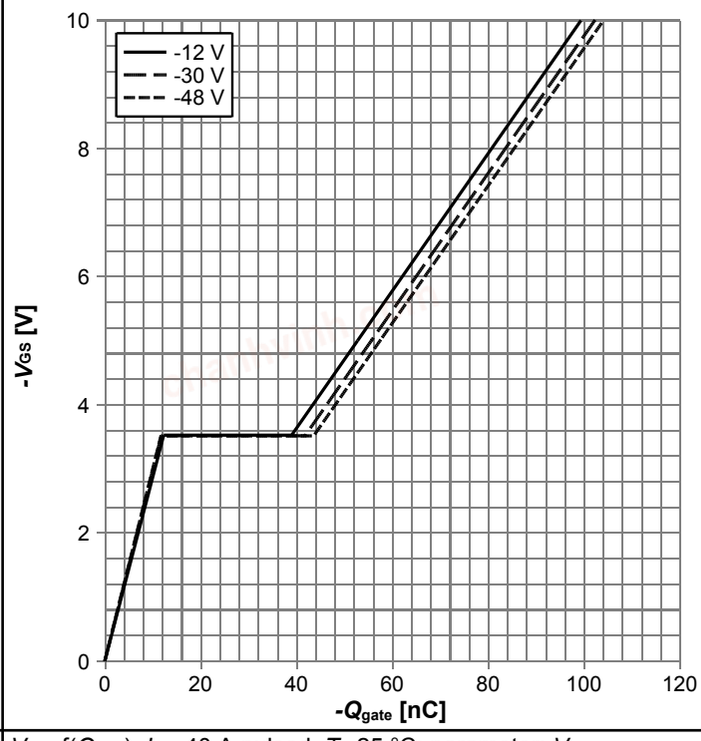
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Diagram 13: Avalanche characteristics



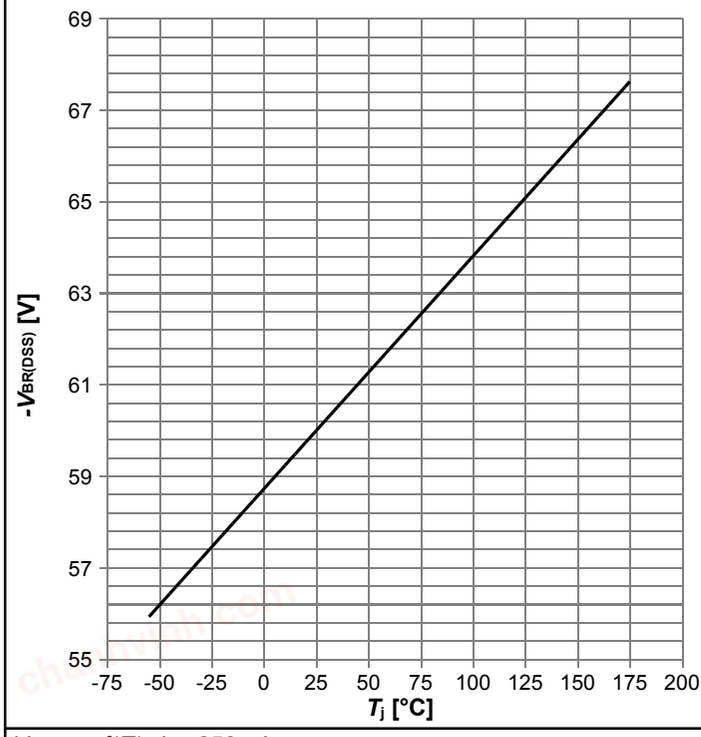
I_{AV}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



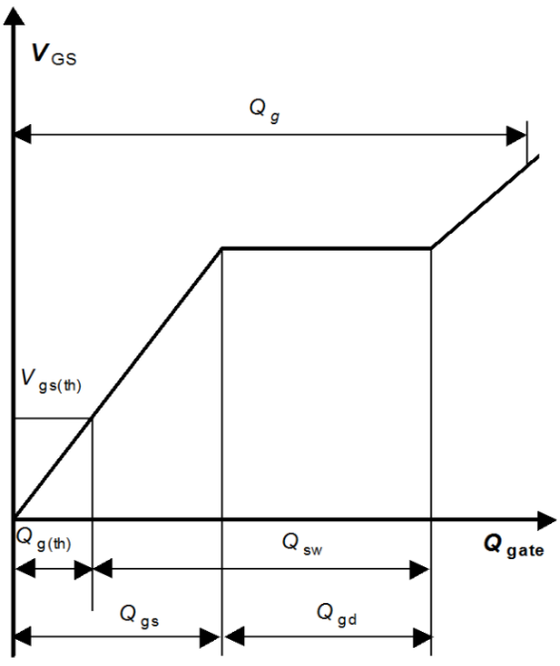
V_{GS}=f(Q_{gate}), I_D=-40 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



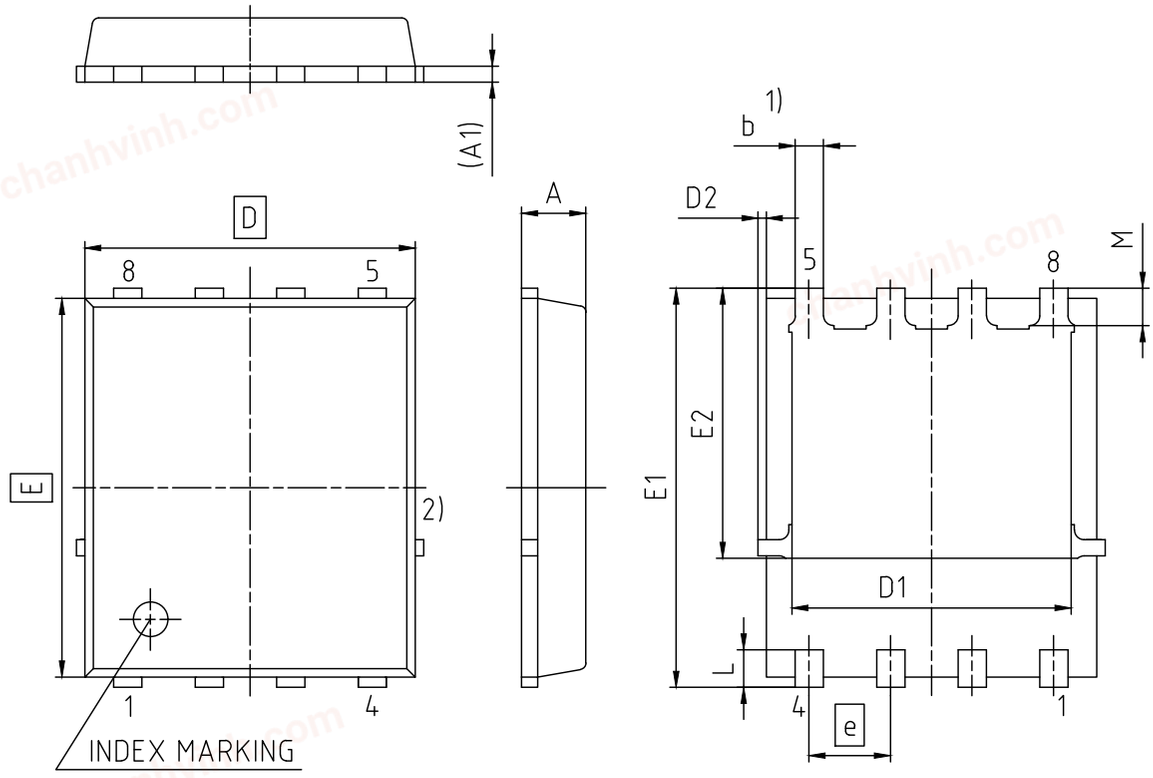
$V_{BR(DSS)}$=f(T_j); I_D=-250 µA

Diagram Gate charge waveforms



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5 Package Outlines



1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

DOCUMENT NO. Z8B00003332
REVISION 08
SCALE 10:1 0 1 2 3mm
EUROPEAN PROJECTION
ISSUE DATE 05.11.2019

Figure 1 Outline PG-TDSON-8, dimensions in mm

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Revision History

ISC240P06LM

Revision: 2022-10-10, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-10-10	Release of final version

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