chanhvinh.com

International
IOR Rectifier

PD - 95490A

IRF2204PbF

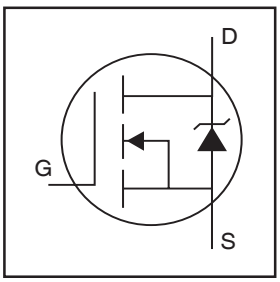
HEXFET® Power MOSFET

Typical Applications

- Industrial Motor Drive

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free



V_{DSS} = 40V

$R_{DS(on)}$ = 3.6mΩ

I_D = 210A⑥



TO-220AB

Description

This HEXFET® Power MOSFET utilizes the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	210⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	150⑥	
I_{DM}	Pulsed Drain Current ①	850	
P_D @T_C = 25°C	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	460	mJ
I_{AR}	Avalanche Current①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

chanhvinh.com

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.041	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.0	3.6	mΩ	V_{GS} = 10V, I_D = 130A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = 10V, I_D = 250μA
g_{fs}	Forward Transconductance	120	—	—	S	V_{DS} = 10V, I_D = 130A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V_{DS} = 40V, V_{GS} = 0V
		—	—	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	130	200	nC	I_D = 130A
Q_{gs}	Gate-to-Source Charge	—	35	52		V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	39	59		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	V_{DD} = 20V
t_r	Rise Time	—	140	—		I_D = 130A
$t_{d(off)}$	Turn-Off Delay Time	—	62	—		R_G = 2.5Ω
t_f	Fall Time	—	110	—		V_{GS} = 10V ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	5890	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1570	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	130	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	8000	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	1370	—		V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	2380	—		V_{GS} = 0V, V_{DS} = 0V to 32V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	210⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	850		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 130A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	68	100	ns	T_J = 25°C, I_F = 130A
Q_{rr}	Reverse RecoveryCharge	—	120	180	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

chanhvinh.com

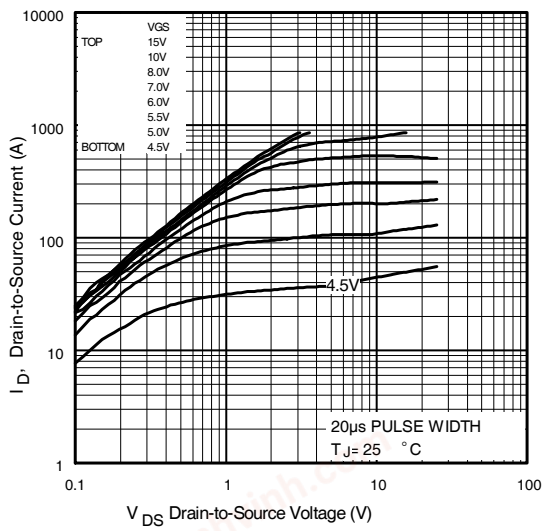


Fig 1. Typical Output Characteristics

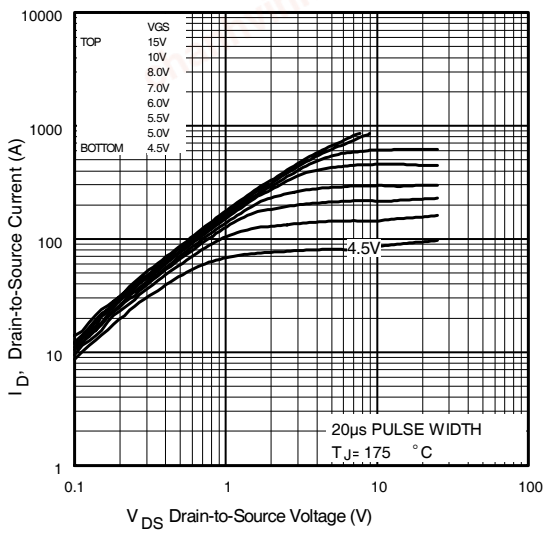


Fig 2. Typical Output Characteristics

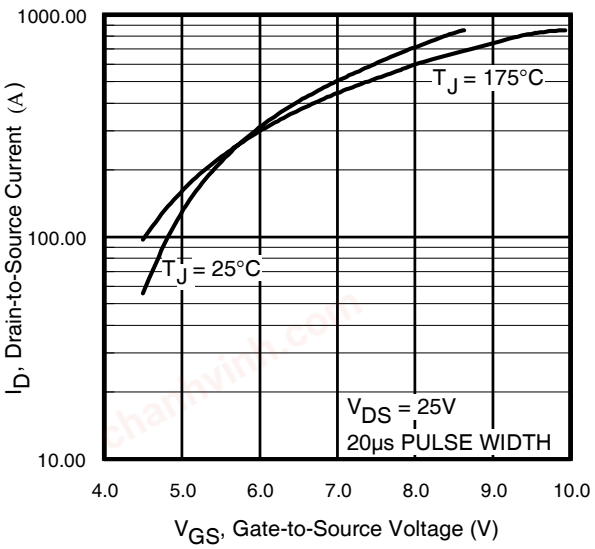


Fig 3. Typical Transfer Characteristics

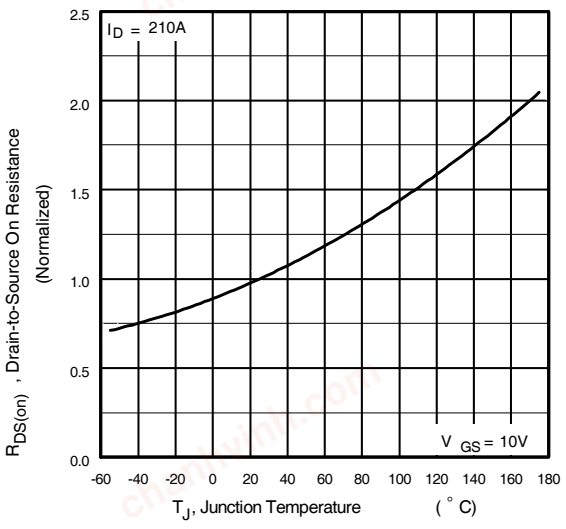


Fig 4. Normalized On-Resistance Vs. Temperature

chanhvinh.com

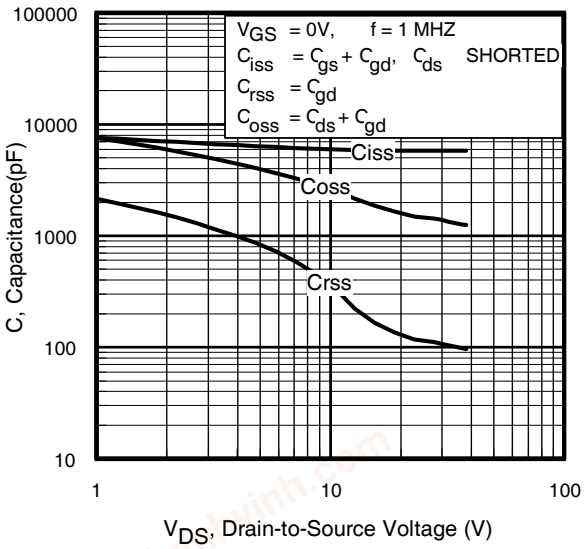


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

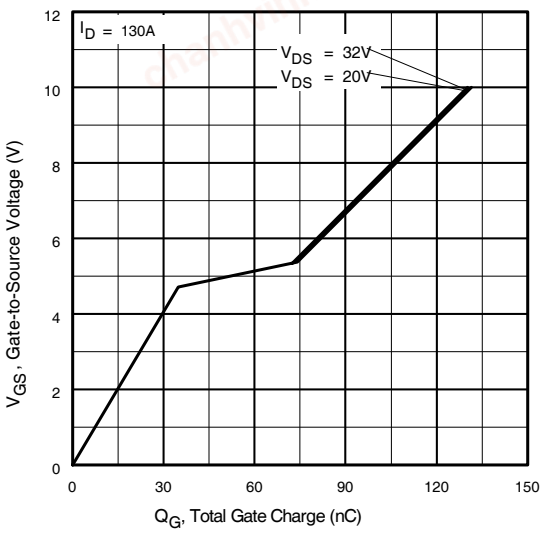


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

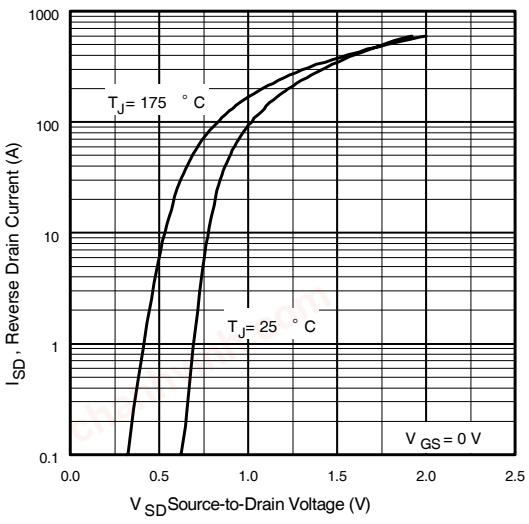


Fig 7. Typical Source-Drain Diode Forward Voltage

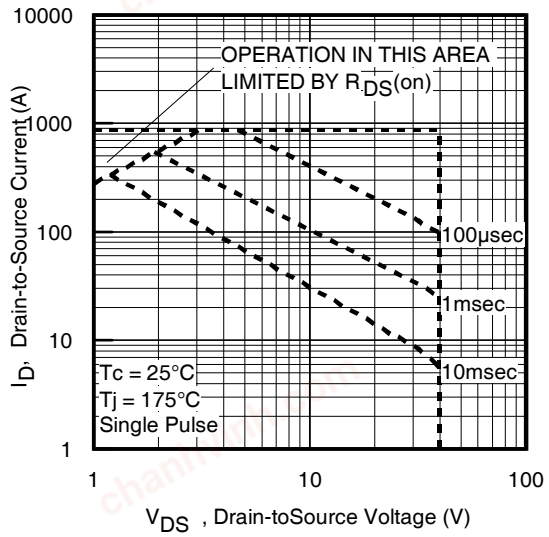


Fig 8. Maximum Safe Operating Area

chanhvinh.com

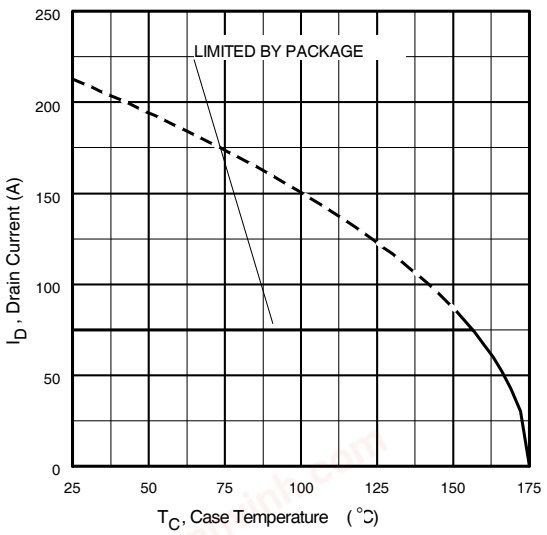


Fig 9. Maximum Drain Current Vs. Case Temperature

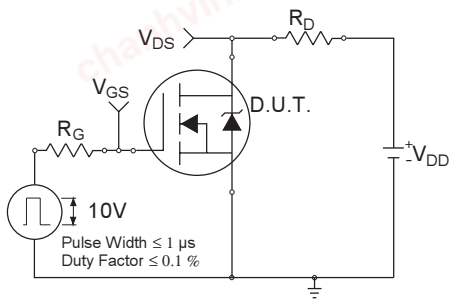


Fig 10a. Switching Time Test Circuit

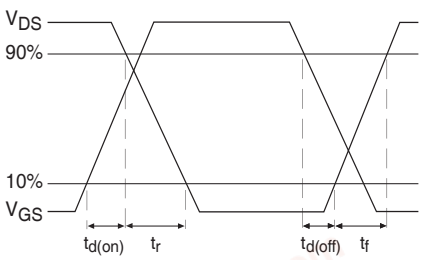


Fig 10b. Switching Time Waveforms

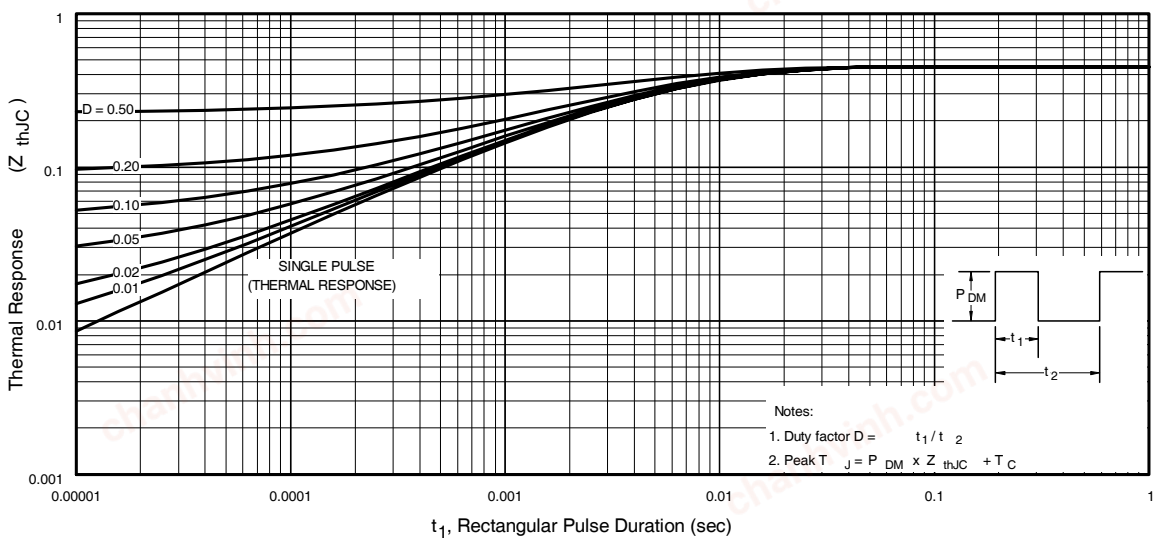


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

chanhvinh.com

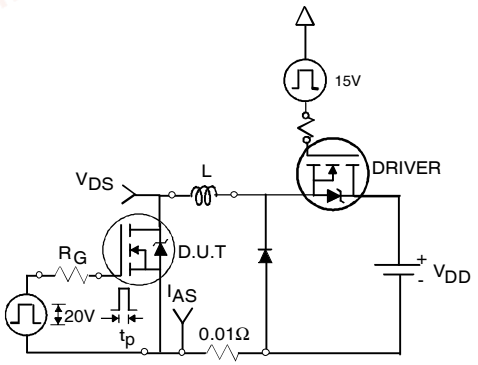


Fig 12a. Unclamped Inductive Test Circuit

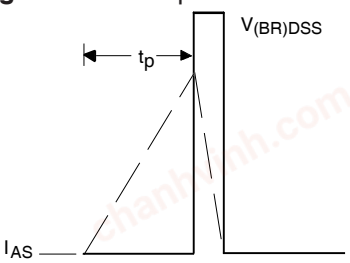


Fig 12b. Unclamped Inductive Waveforms

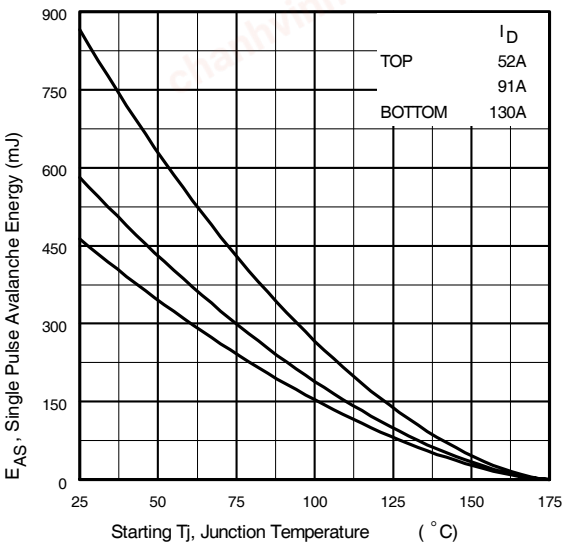


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

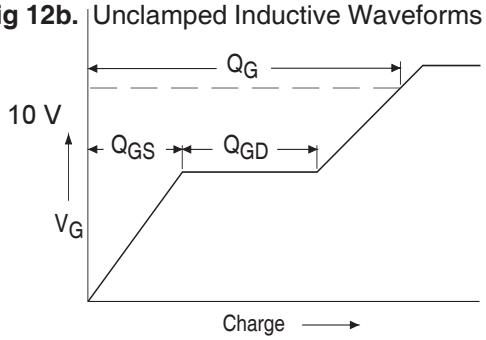


Fig 13a. Basic Gate Charge Waveform

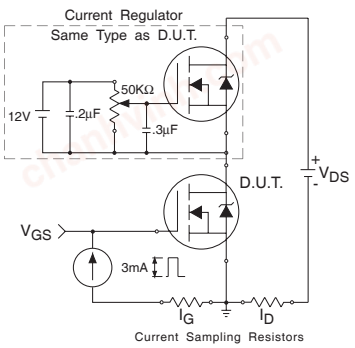


Fig 13b. Gate Charge Test Circuit

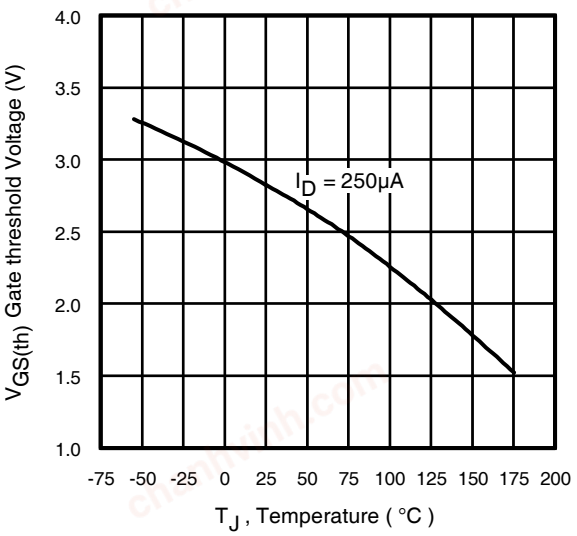


Fig 14. Threshold Voltage Vs. Temperature

chanhvinh.com

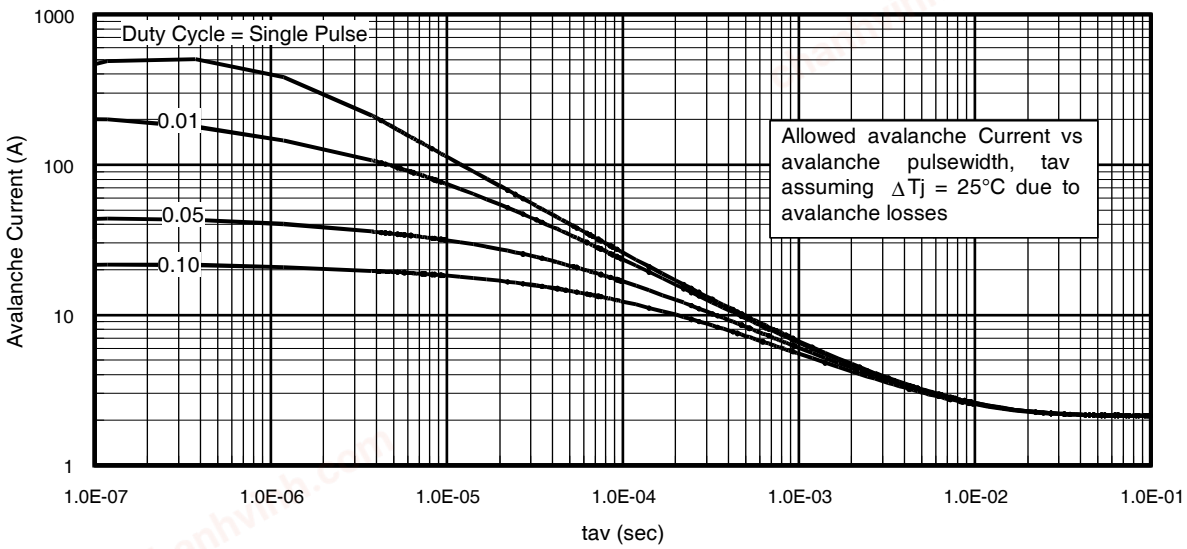


Fig 15. Typical Avalanche Current Vs.Pulsewidth

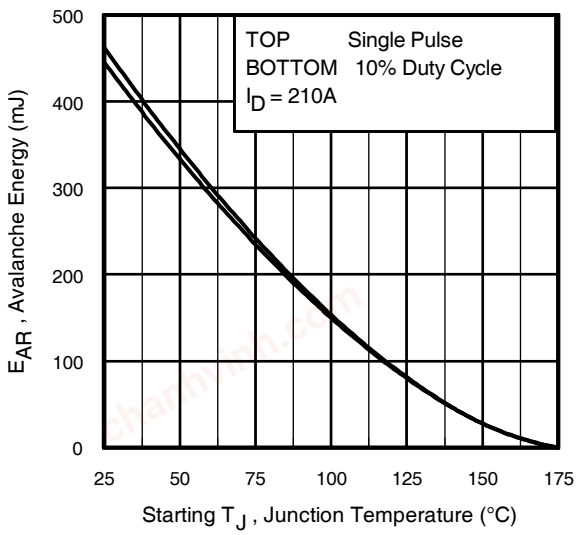


Fig 16. Maximum Avalanche Energy Vs. Temperature

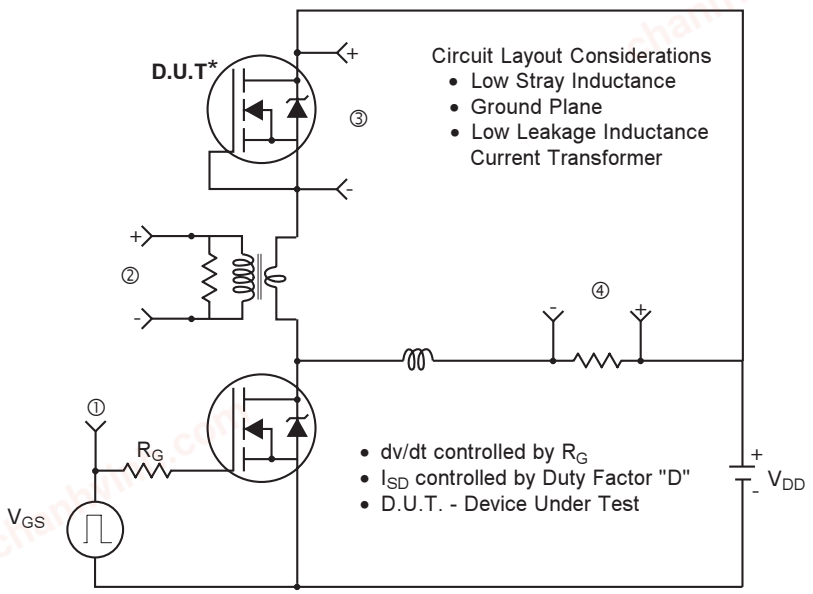
Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

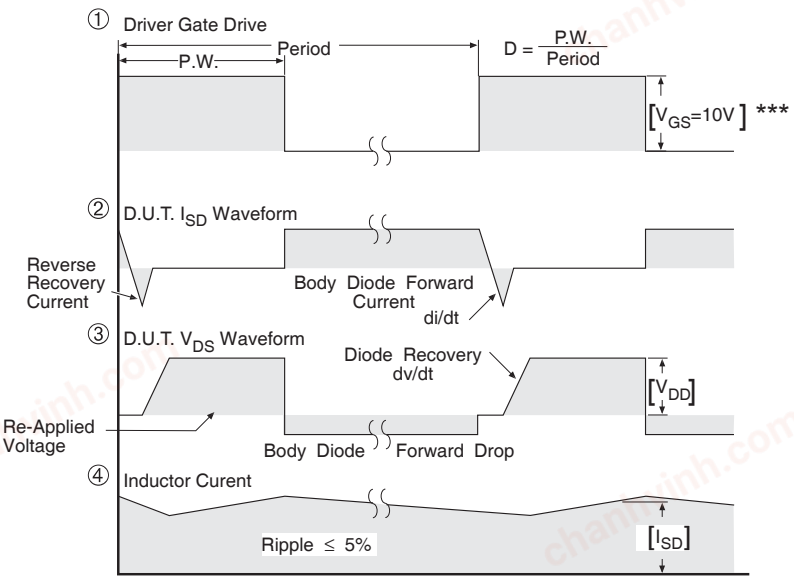
$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

chanhvinh.com

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

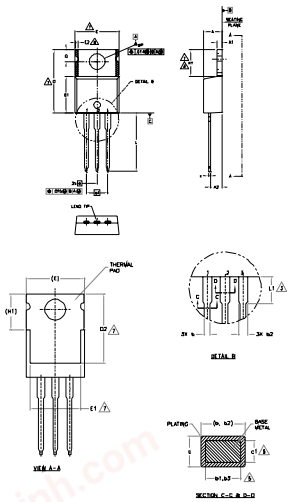


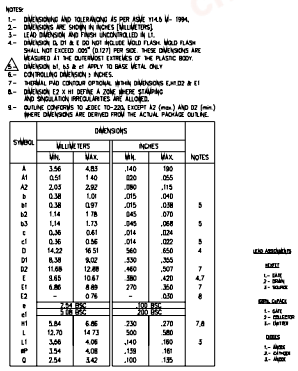
*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

chanhvinh.com

TO-220AB Package Outline(Dimensions are shown in millimeters (inches))





SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE

IGBT & CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER

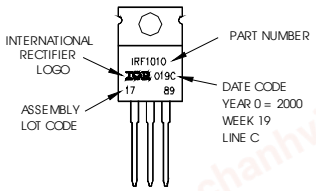
DIODES

1.- ANODE
2.- CATHODE
3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB package is not recommended for Surface Mount Application.

Notes:

1. For an Automotive Qualified version of this part please see http://www.irf.com/product-info/auto/

2. For the most current drawing please refer to IR website at http://www.irf.com/package/

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.06mH R_G = 25Ω, I_{AS} = 130A. (See Figure 12).

③ $I_{SD} \leq$ 130A, di/dt ≤ 170A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.07/2010

chanhvinh.com

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”) .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.