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OptiMOS™ Power-Transistor

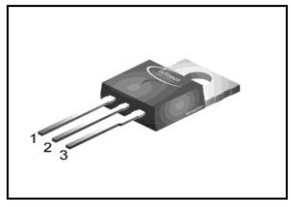
Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

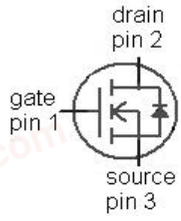
V_{DS}	60	V
$R_{DS(on),max}$	4.0	mΩ
I_D	80	A
Q_{OSS}	44	nC
Q_G(0V..10V)	38	nC

PG-TO220-3



RoHS Halogen-Free Pb-Free

Type	Package	Marking
IPP040N06N	PG-TO220-3	040N06N



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	80	A
		V_{GS}=10 V, T_C=100 °C	80	
		V_{GS}=10 V, T_C=25 °C, R_{thJA} =50K/W	20	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	320	
Avalanche energy, single pulse[3]	E_{AS}	I_D=80 A, R_{GS}=25 Ω	70	mJ
Gate source voltage	V_{GS}		±20	V

[1] J-STD20 and JESD22

[2] See figure 3 for more detailed information

[3] See figure 13 for more detailed information

[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

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Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	107	W
		T_A=25 °C, R_{thJA}=50 K/W	3.0	
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.4	K/W
Device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm² cooling area[4)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=50 µA	2.1	2.8	3.3	
Zero gate voltage drain current	I_{DSS}	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C	-	0.5	1	µA
		V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=80 A	-	3.6	4.0	mΩ
		V_{GS}=6 V, I_D=20 A	-	4.7	6.0	
Gate resistance	R_G		-	1.3	1.95	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=80 A	60	120	-	S

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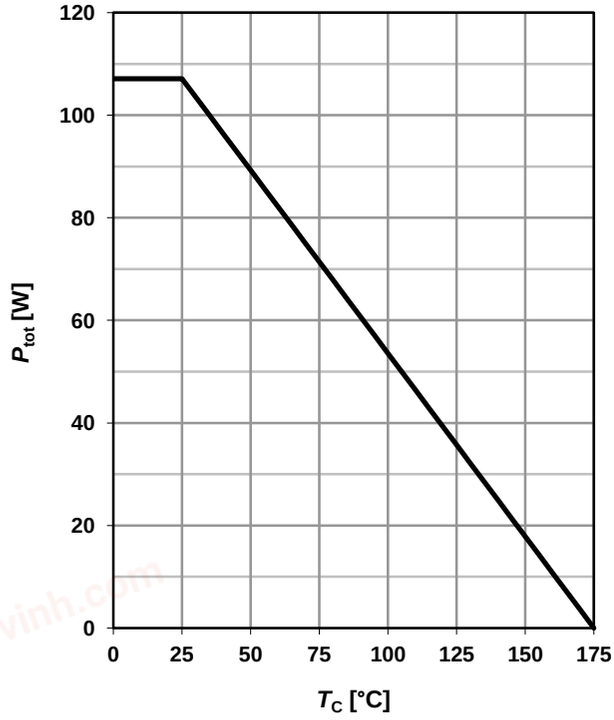
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz	-	2700	3375	pF
Output capacitance	C_{oss}		-	670	838	
Reverse transfer capacitance	C_{rss}		-	28	56	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=80 A, $R_{G,ext}$=3 Ω	-	19	-	ns
Rise time	t_r		-	16	-	
Turn-off delay time	$t_{d(off)}$		-	30	-	
Fall time	t_f		-	9	-	
Gate Charge Characteristics[5)]						
Gate to source charge	Q_{gs}	V_{DD}=30 V, I_D=80 A, V_{GS}=0 to 10 V	-	13	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	8	-	
Gate to drain charge	Q_{gd}		-	7	9	
Switching charge	Q_{sw}		-	13	-	
Gate charge total	Q_g		-	38	44	
Gate plateau voltage	$V_{plateau}$		-	4.9	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 10 V	-	33	-	nC
Output charge	Q_{oss}	V_{DD}=30 V, V_{GS}=0 V	-	44	-	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	80	A
Diode pulse current	$I_{S,pulse}$		-	-	320	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=80 A, T_j=25 °C	-	1.0	1.2	V
Reverse recovery time	t_{rr}	V_R=30 V, I_F=80 A, di_F/dt=100 A/µs	-	34	54	ns
Reverse recovery charge	Q_{rr}		-	34	-	nC

[5)] See figure 16 for gate charge parameter definition

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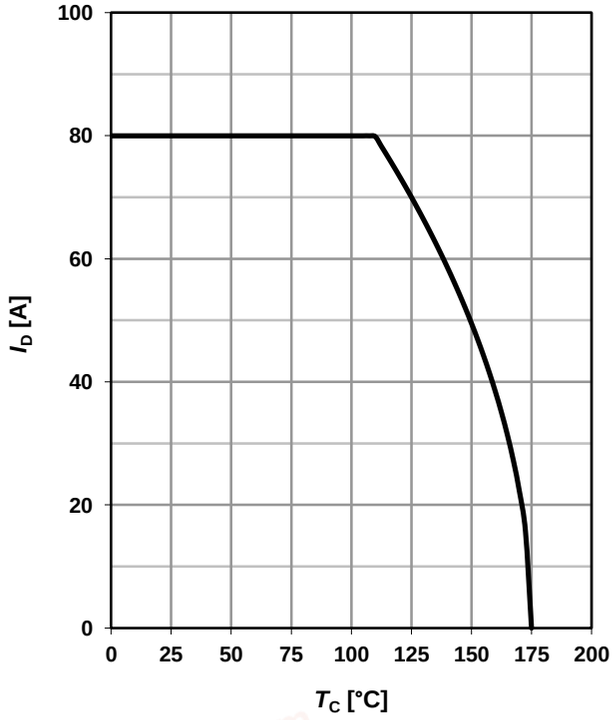
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

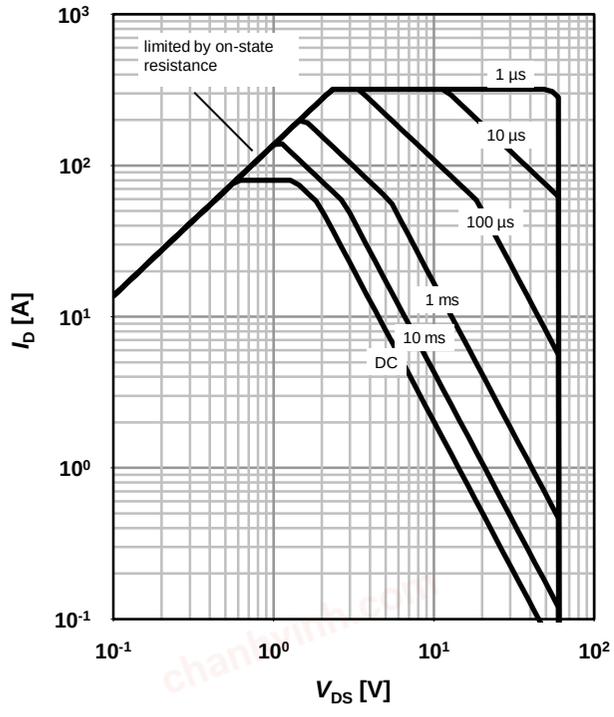
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

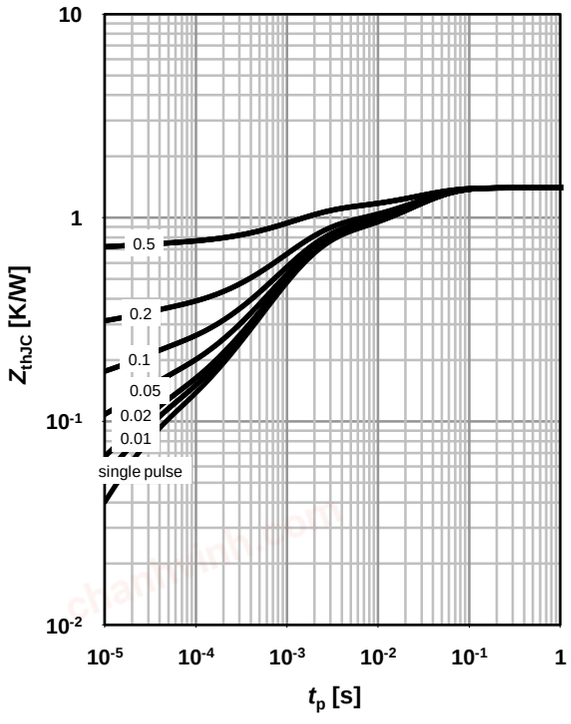
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

parameter: $D=t_p/T$

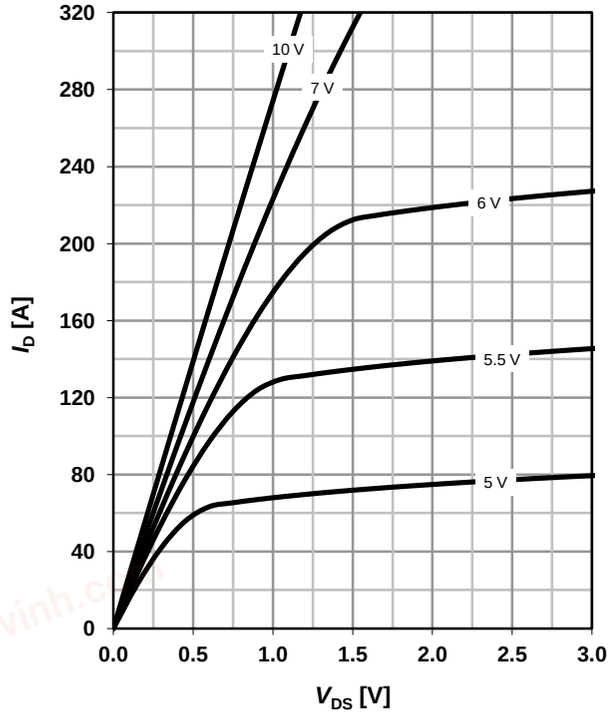


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5 Typ. output characteristics

$I_D=f(V_{DS})$; T_j=25 °C

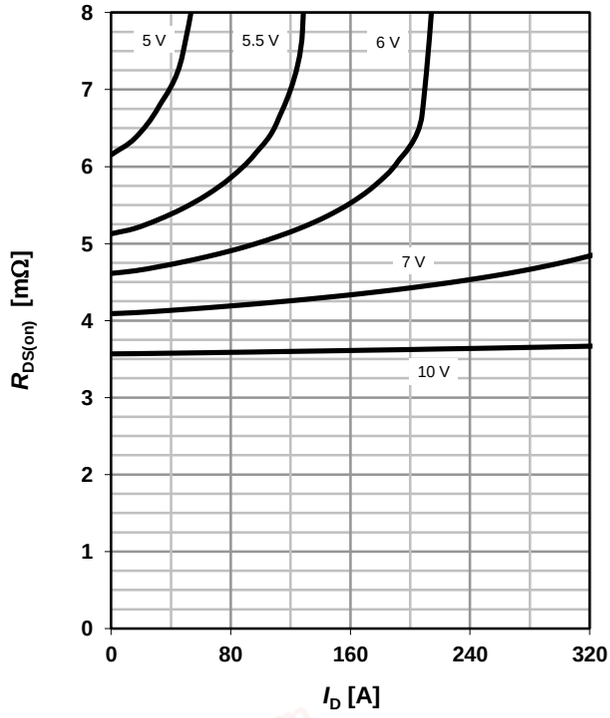
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; T_j=25 °C

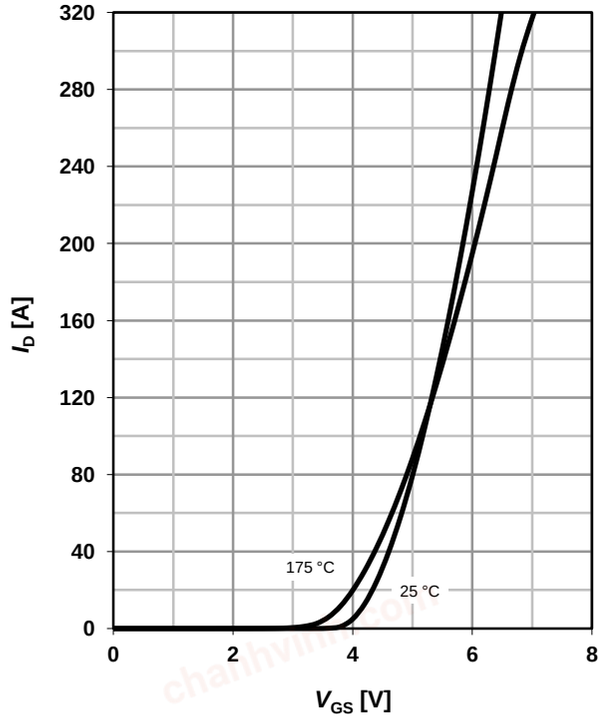
parameter: V_{GS}



7 Typ. transfer characteristics

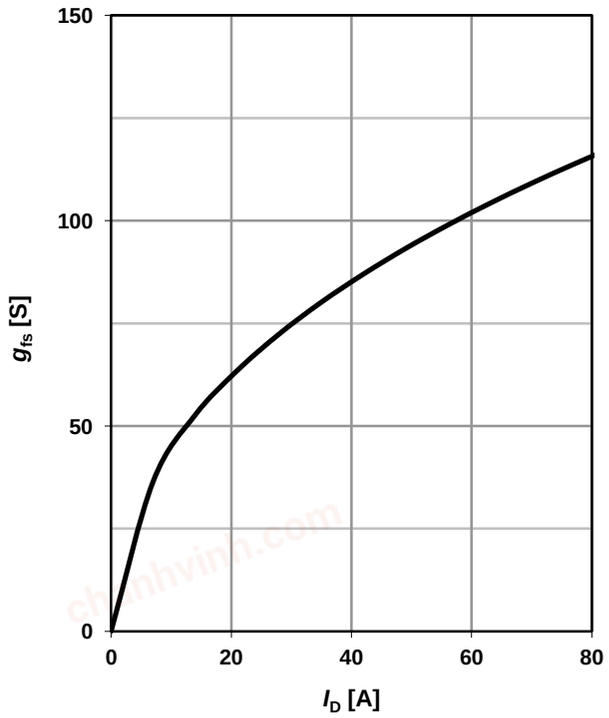
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



8 Typ. forward transconductance

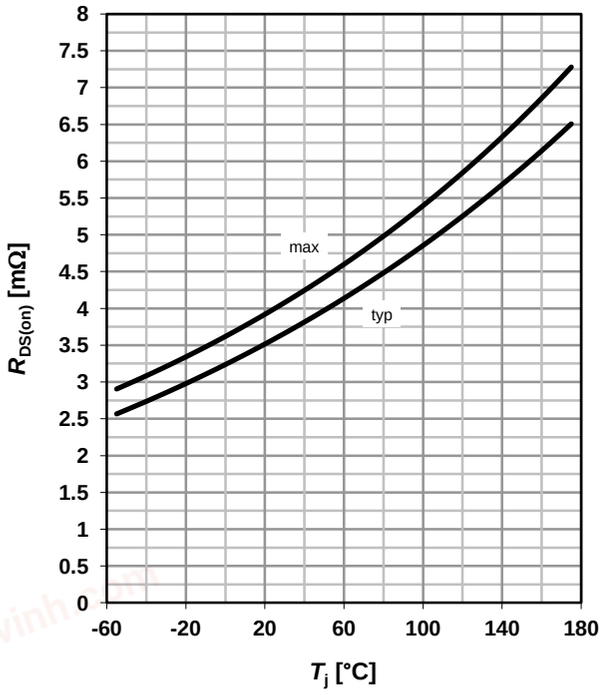
$g_{fs}=f(I_D)$; T_j=25 °C



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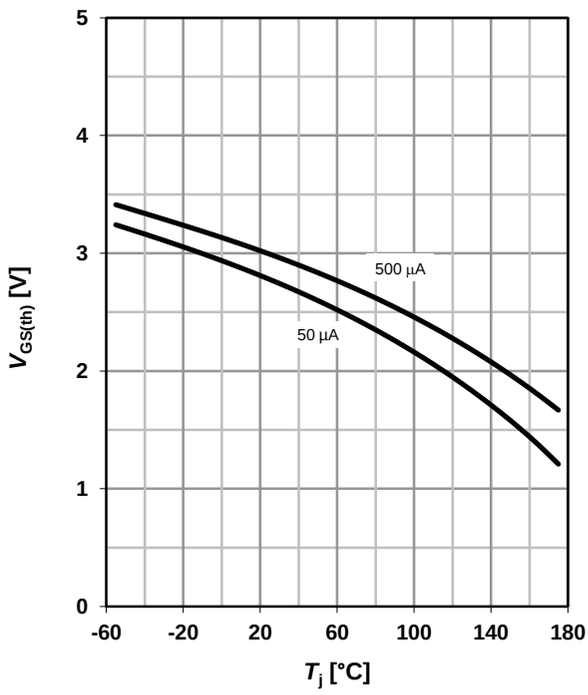
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=80 A; V_{GS}=10 V



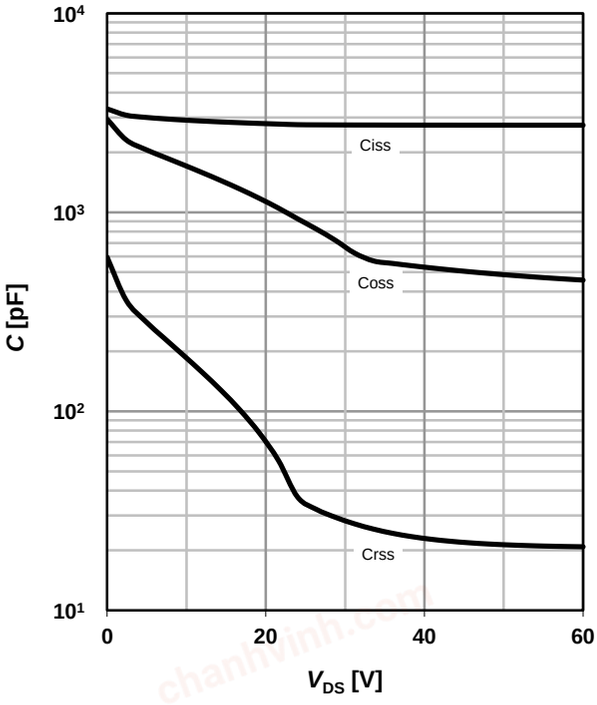
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}



11 Typ. capacitances

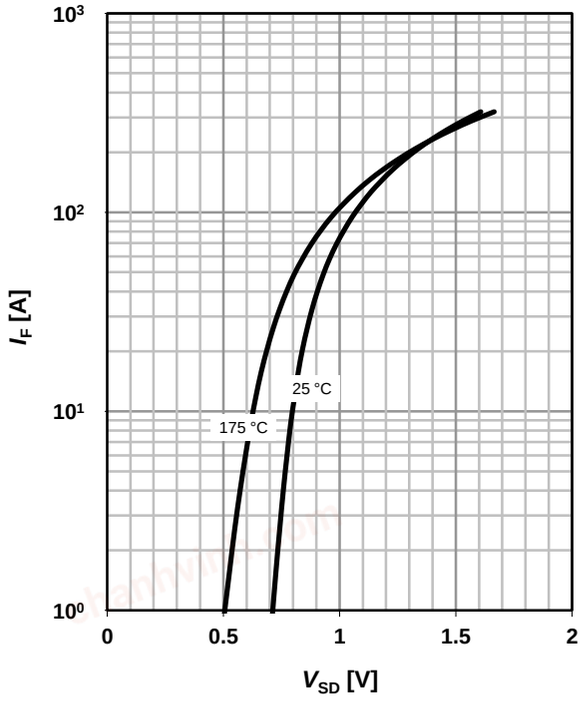
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

parameter: T_j

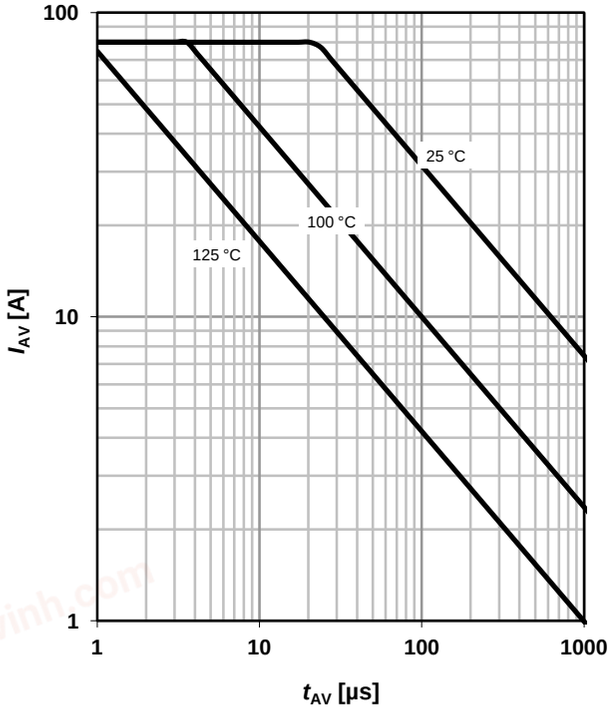


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13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

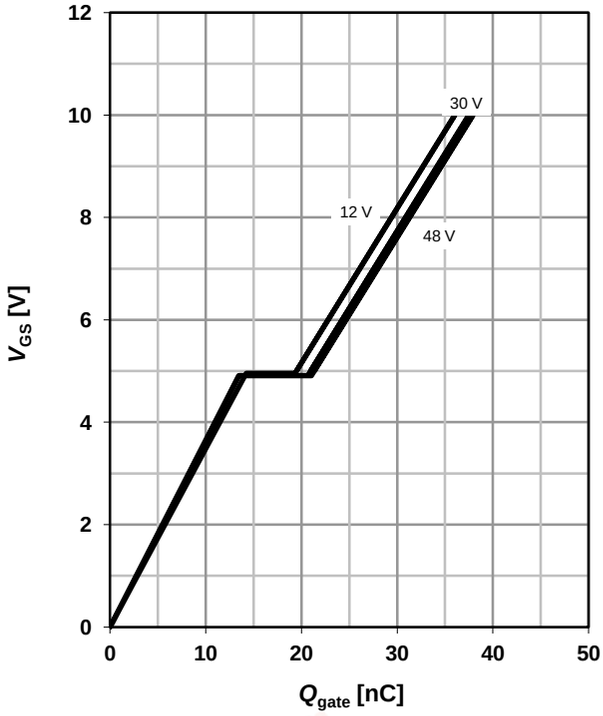
parameter: $T_{j(start)}$



14 Typ. gate charge

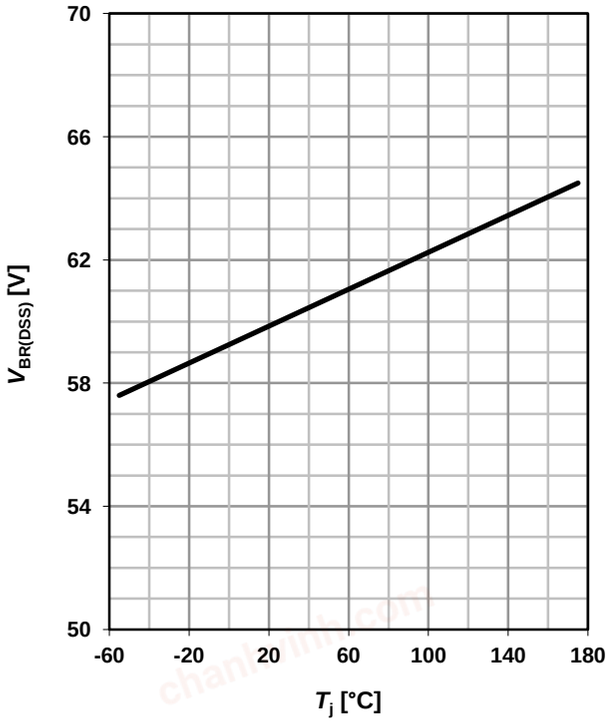
V_{GS}=f(Q_{gate}); I_D=80 A pulsed

parameter: V_{DD}

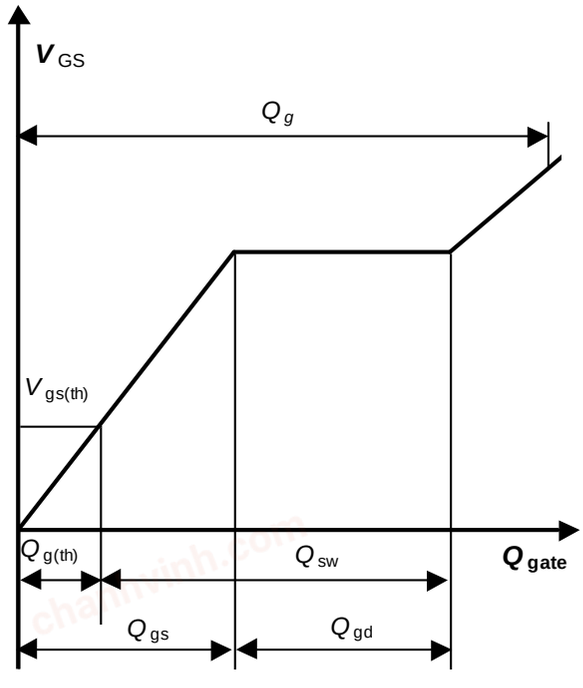


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

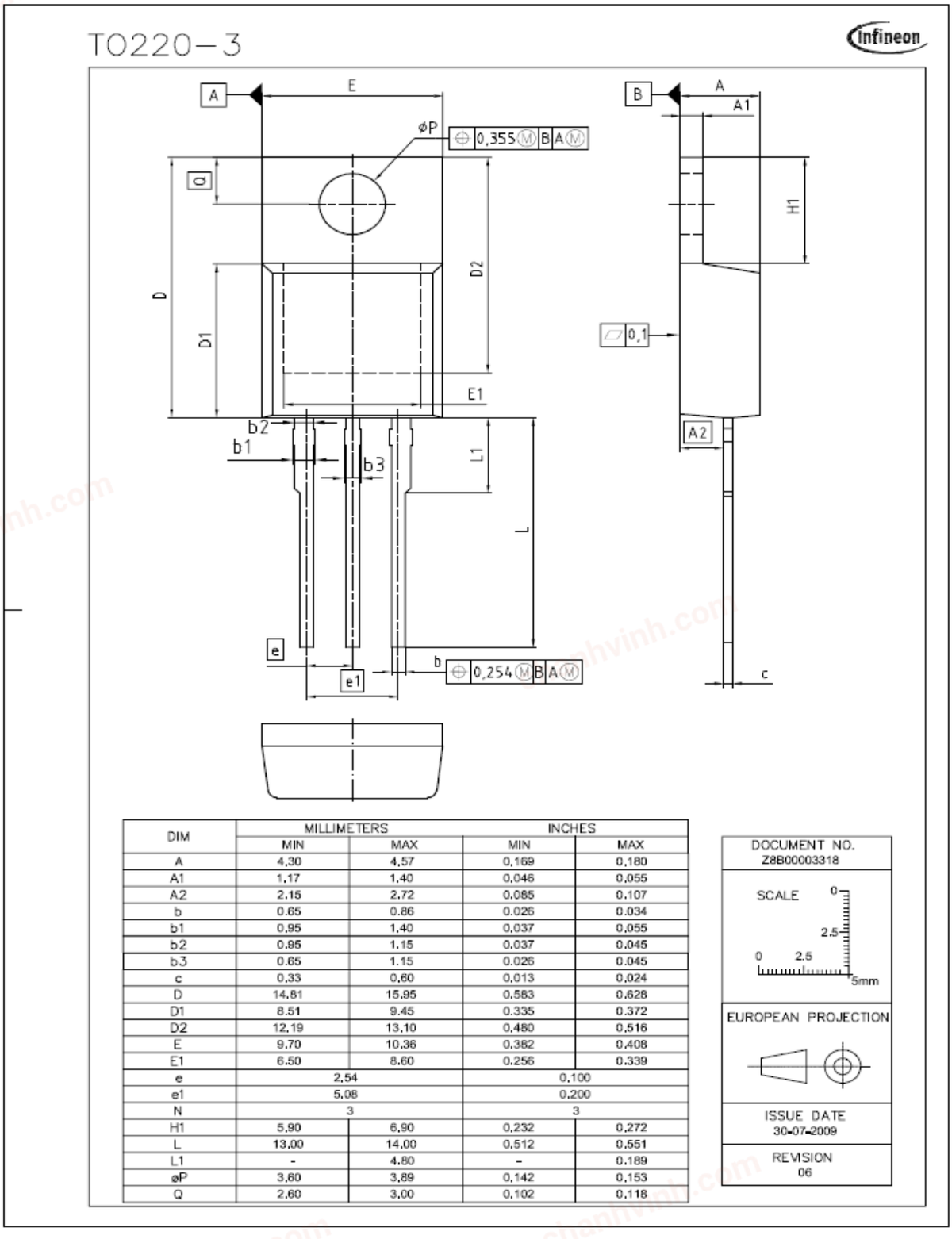


16 Gate charge waveforms



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Package Outline **PG-TO220-3**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4,30	4,57	0,169	0,180
A1	1,17	1,40	0,046	0,055
A2	2,15	2,72	0,085	0,107
b	0,65	0,86	0,026	0,034
b1	0,95	1,40	0,037	0,055
b2	0,95	1,15	0,037	0,045
b3	0,65	1,15	0,026	0,045
c	0,33	0,60	0,013	0,024
D	14,81	15,95	0,583	0,628
D1	8,51	9,45	0,335	0,372
D2	12,19	13,10	0,480	0,516
E	9,70	10,36	0,382	0,408
E1	6,50	8,60	0,256	0,339
e	2,54		0,100	
e1	5,08		0,200	
N	3		3	
H1	5,90	6,90	0,232	0,272
L	13,00	14,00	0,512	0,551
L1	-	4,80	-	0,189
øP	3,60	3,89	0,142	0,153
Q	2,60	3,00	0,102	0,118

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