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MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C6 600V

600V CoolMOS™ C6 Power Transistor
IPx60R950C6

Data Sheet

Rev. 2.5
Final

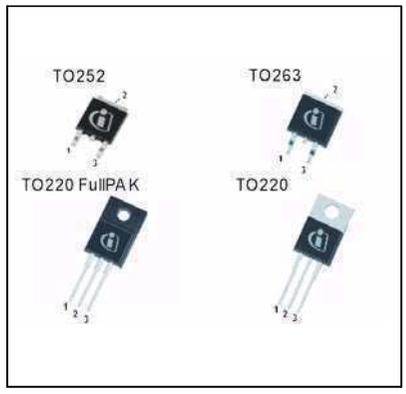
Power Management & Multimarket

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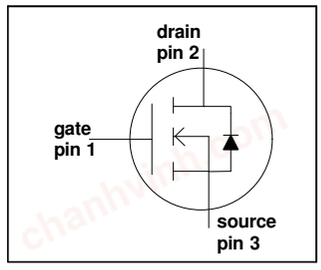
600V CoolMOS™ C6 Power Transistor

IPD60R950C6, IPB60R950C6
IPP60R950C6, IPA60R950C6

1 Description



CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ C6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter, and cooler.



Features

- Extremely low losses due to very low FOM R_{dson}*Q_g and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Fully qualified according to JEDEC for Industrial Applications
- Pb-free plating, Halogen free mold compound

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	0.95	Ω
$Q_{g,typ}$	13	nC
$I_{D,pulse}$	12	A
E_{oss} @ 400V	1.3	µJ
Body diode d*i*/d*t*	500	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPD60R950C6	PG-TO252	6R950C6	IFX C6 Product Brief
IPB60R950C6	PG-TO263		IFX C6 Portfolio
IPP60R950C6	PG-TO220		IFX CoolMOS Webpage
IPA60R950C6	PG-TO220 FullPAK		IFX Design tools

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2 Maximum Ratings

at T_j = 25 °C, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	-	-	4.4	A	T_C= 25 °C
				2.8		T_C= 100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	12	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	46	mJ	I_D=0.8 A, V_{DD}=50 V (see table 21)
Avalanche energy, repetitive	E_{AR}	-	-	0.13		I_D=0.8 A, V_{DD}=50 V
Avalanche current, repetitive	I_{AR}	-	-	0.8	A	
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS}=0...480 V
Gate source voltage	V_{GS}	-20	-	20	V	static
		-30		30		AC (f>1 Hz)
Power dissipation for TO-220, TO-252, TO-263	P_{tot}	-	-	37	W	T_C=25 °C
Power dissipation for TO-220 FullPAK	P_{tot}	-	-	26	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	
Mounting torque TO-220		-	-	60	Ncm	M3 and M3.5 screws
TO-220FP				50		M2.5 screws
Continuous diode forward current	I_S	-	-	3.9	A	T_C=25 °C
Diode pulse current[2]	$I_{S,pulse}$	-	-	12	A	T_C=25 °C
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS}=0...480 V, $I_{SD} \leq I_D$, T_j=125 °C
Maximum diode commutation speed[3]	di_f/dt			500	A/µs	(see table 22)

1) Limited by $T_{j,max.}$ Maximum duty cycle D=0.75
2) Pulse width t_p limited by $T_{j,max}$
3) Identical low side and high side switch with identical R_G

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3 Thermal characteristics

Table 3 Thermal characteristics TO-220 (IPP60R950C6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.41	°C/W	
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 4 Thermal characteristics TO-220FullPAK (IPA60R950C6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.9	°C/W	
Thermal resistance, junction - ambient	R_{thJA}	-	-	80		leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 5 Thermal characteristics TO-263 (IPB60R950C6),TO-252 (IPD60R950C6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.41	°C/W	
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm^2 cooling area[1)]
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

1) Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm^2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical without air stream cooling

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4 Electrical characteristics

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0 V, I_D=0.25 mA
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5		V_{DS}=V_{GS}, I_D=0.13 mA
Zero gate voltage drain current	I_{DSS}	-	-	1	µA	V_{DS}=600 V, V_{GS}=0 V, T_j=25 °C
		-	10	-		V_{DS}=600 V, V_{GS}=0 V, T_j=150 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.86	0.95	Ω	V_{GS}=10 V, I_D=1.5 A, T_j=25 °C
		-	2.22	-		V_{GS}=10 V, I_D=1.5 A, T_j=150 °C
Gate resistance	R_G	-	16	-	Ω	f=1 MHz, open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	280	-	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Output capacitance	C_{oss}	-	21	-		
Effective output capacitance, energy related[1)]	$C_{o(er)}$	-	14	-		V_{GS}=0 V, V_{DS}=0...480 V
Effective output capacitance, time related[2)]	$C_{o(tr)}$	-	57	-		I_D=constant, V_{GS}=0 V V_{DS}=0...480V
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	V_{DD}=400 V, V_{GS}=10 V, I_D=1.9A, R_G= 12.2 Ω (see table 20)
Rise time	t_r	-	8	-		
Turn-off delay time	$t_{d(off)}$	-	60	-		
Fall time	t_f	-	13	-		

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

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Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
IGate to source charge	Q_{gs}	-	1.5	-	nC	V_{DD}=480 V, I_D=1.9 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	6.5	-		
Gate charge total	Q_g	-	13	-		
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0 V, I_F=1.9 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	220	-	ns	V_R=400 V, I_F=1.9 A, di_F/dt=100 A/µs (see table 22)
Reverse recovery charge	Q_{rr}	-	1.5	-	µC	
Peak reverse recovery current	I_{rrm}	-	12	-	A	

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5 Electrical characteristics diagrams

Table 10

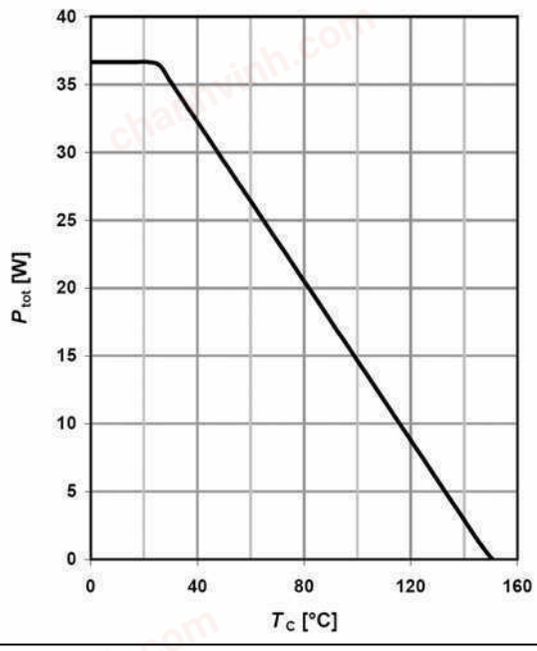
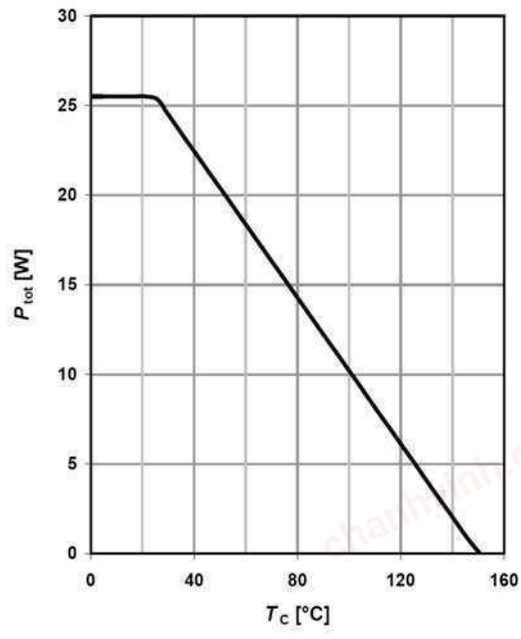
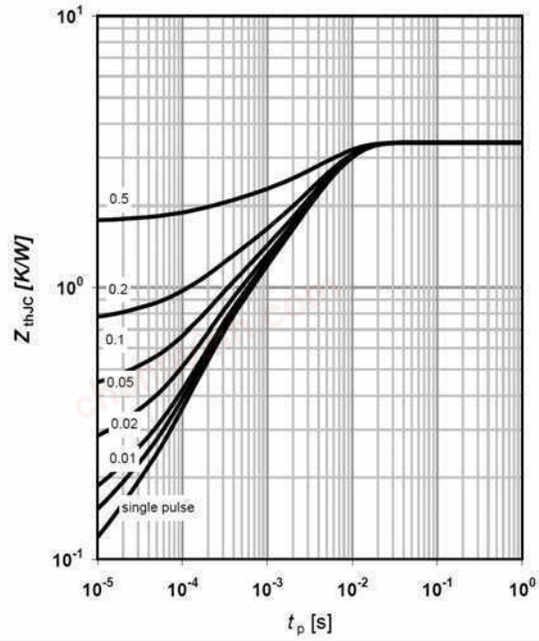
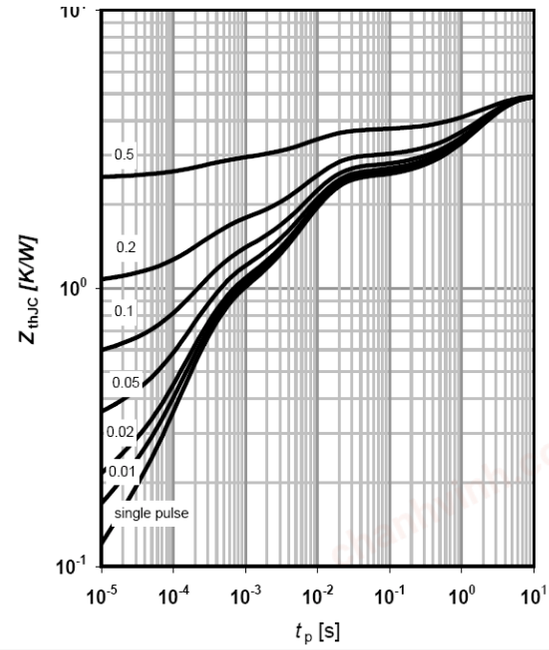
Power dissipation TO-220, TO-252, TO-263	Power dissipation TO-220 FullPAK
	
$P_{tot} = f(T_C)$	$P_{tot} = f(T_C)$

Table 11

Max. transient thermal impedance TO-220, TO-252, TO-263	Max. transient thermal impedance TO-220 FullPAK
	
$Z_{(thJC)}$=f(tp); parameter: D=t_p/T	$Z_{(thJC)}$=f(tp); parameter: D=t_p/T

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Table 12

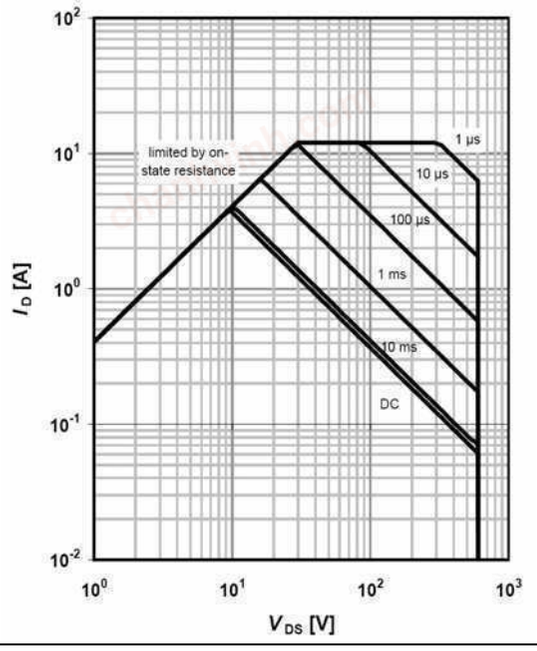
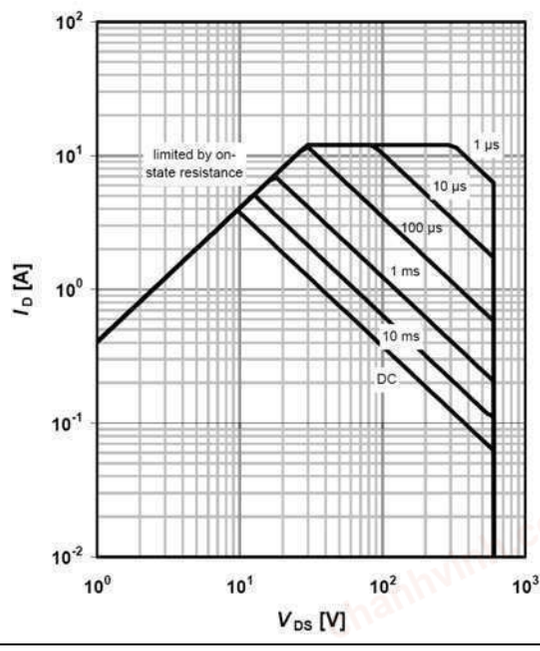
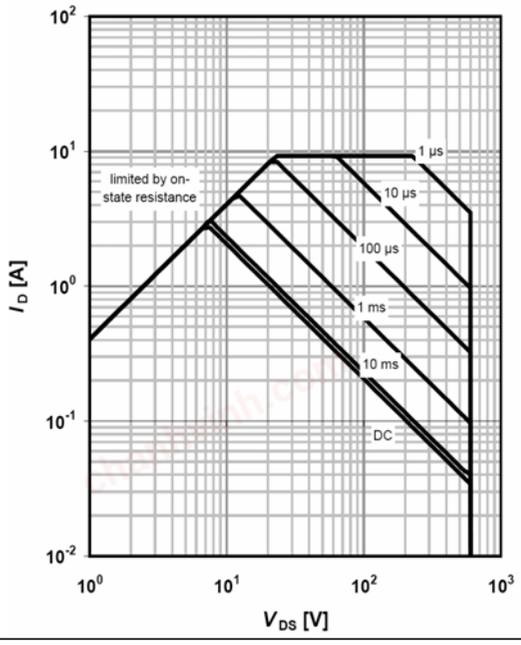
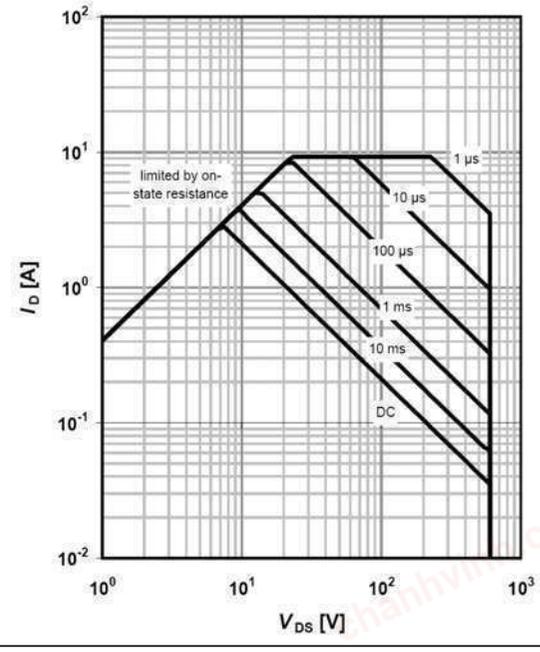
Safe operating area T_C=25 °C TO-220, TO-252, TO-263	Safe operating area T_C=25 °C TO-220 FullPAK
	
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter t_p	I_D=f(V_{DS}); T_C=25 °C; D=0; parameter t_p

Table 13

Safe operating area T_C=80 °C TO-220, TO-252, TO-263	Safe operating area T_C=80 °C TO-220 FullPAK
	
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter t_p	I_D=f(V_{DS}); T_C=80 °C; D=0; parameter t_p

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Table 14

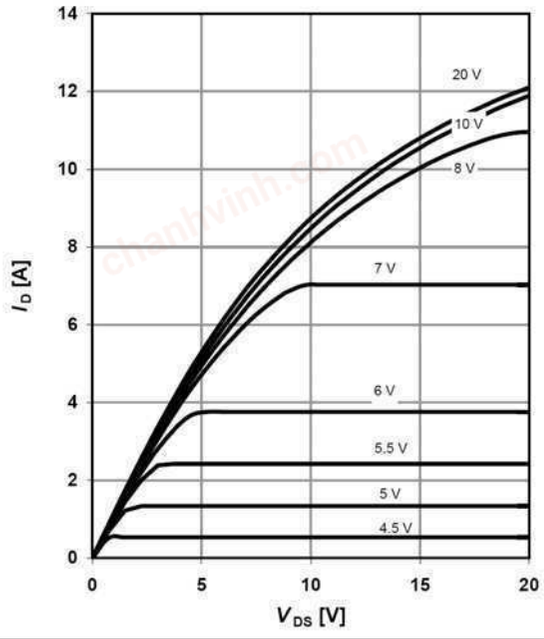
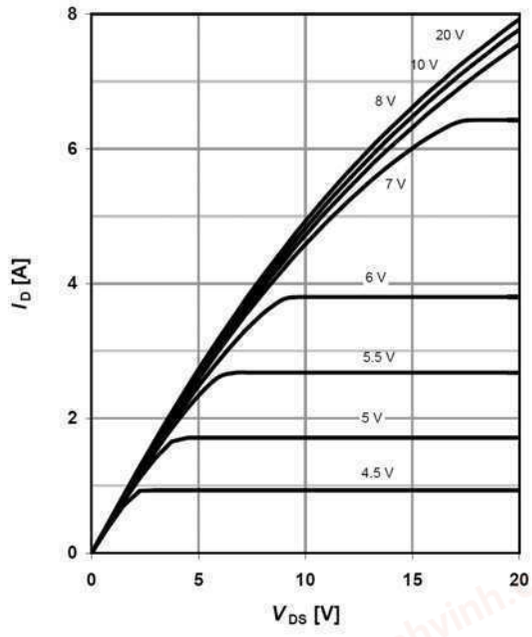
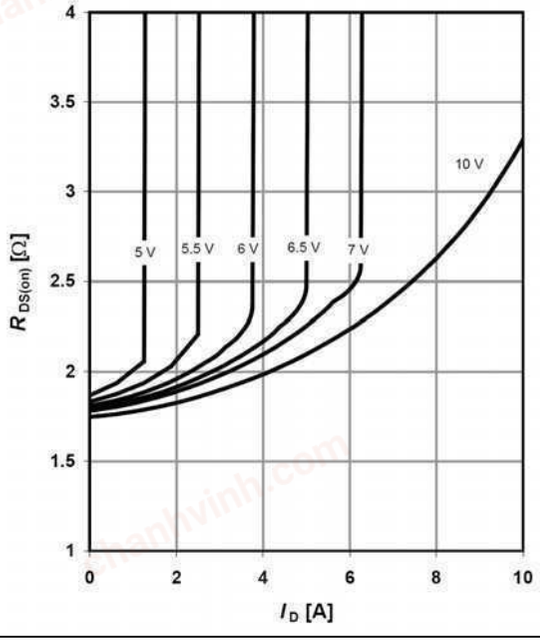
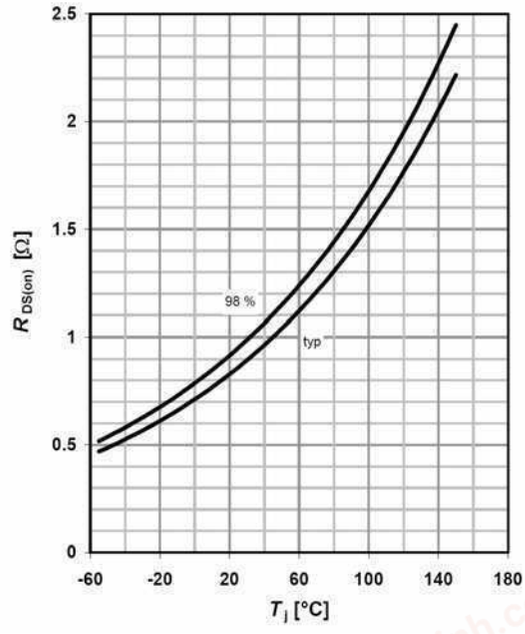
Typ. output characteristics T_j=25 °C	Typ. output characteristics T_j=125 °C
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Table 15

Typ. drain-source on-state resistance	Drain-source on-state resistance
	
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}	$R_{DS(on)}$=f(T_j); I_D=1.5A; V_{GS}=10 V

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Table 16

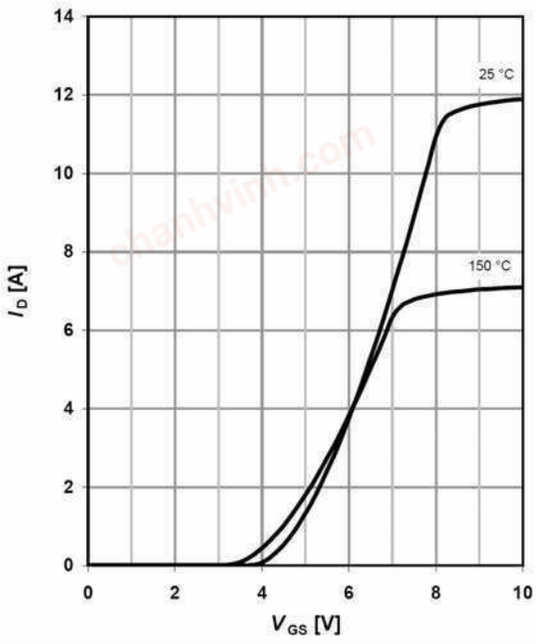
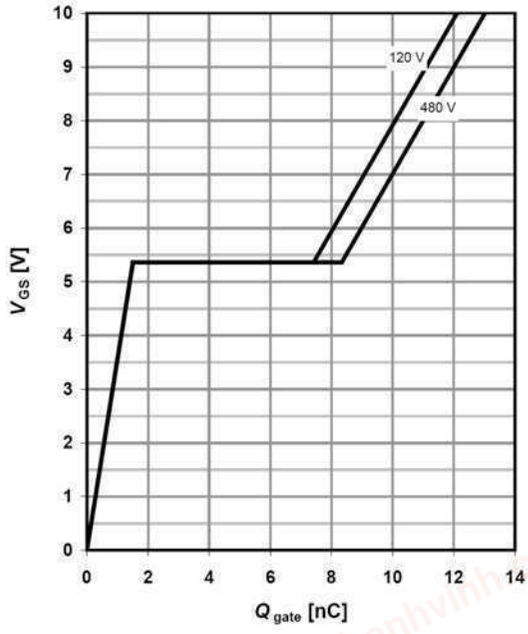
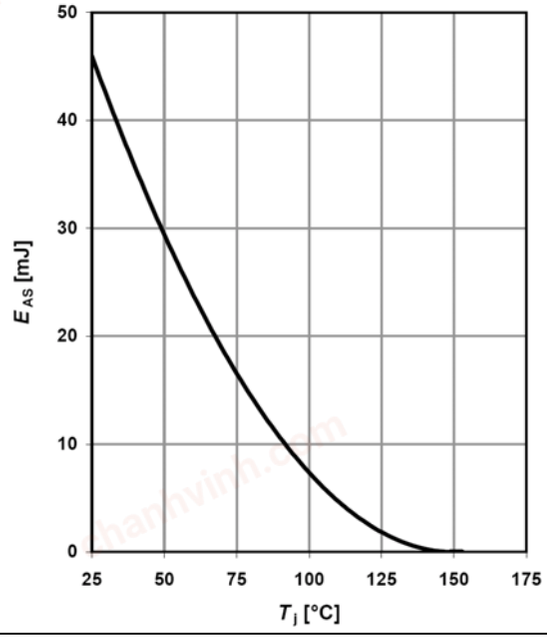
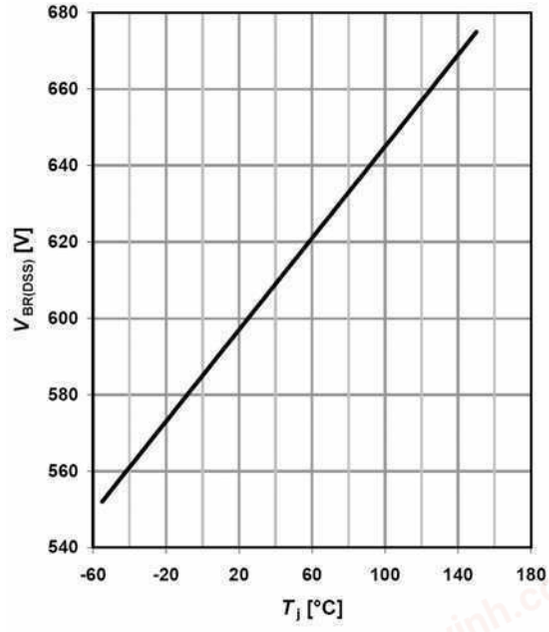
Typ. transfer characteristics	Typ. gate charge
	
I_D=f(V_{GS}); V_{DS}=20V	V_{GS}=f(Q_{gate}), I_D=1.9A pulsed

Table 17

Avalanche energy	Drain-source breakdown voltage
	
E_{AS}=f(T_j); I_D=0.8A; V_{DD}=50 V	$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA

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Table 18

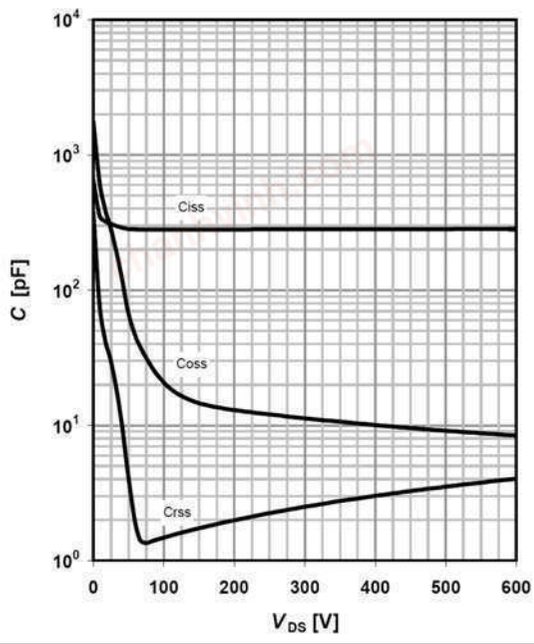
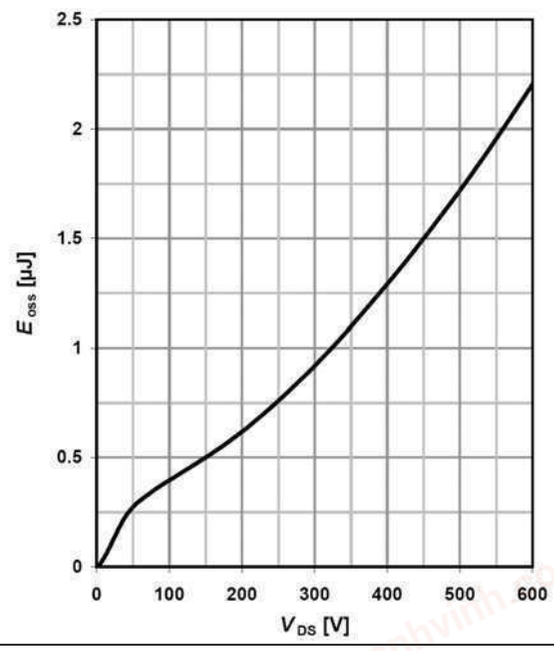
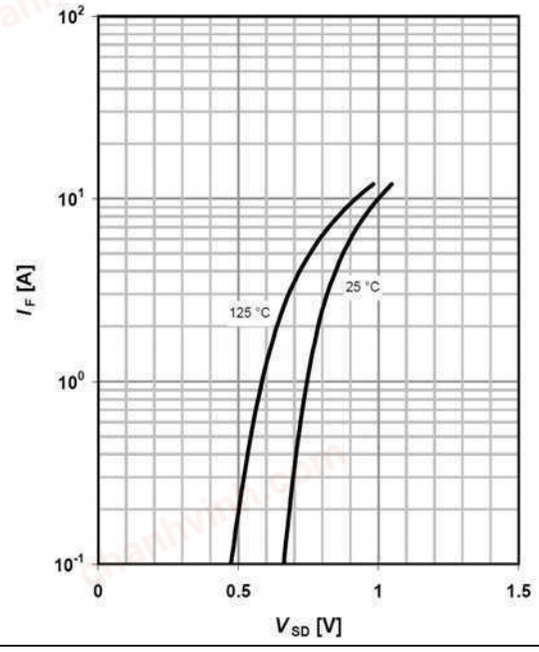
Typ. capacitances	Typ. C_{oss} stored energy
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	E_{oss}=f(V_{DS})

Table 19

Forward characteristics of reverse diode

I_F=f(V_{SD}); parameter: T_j

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6 Test circuits

Table 20 Switching times test circuit and waveform for inductive load

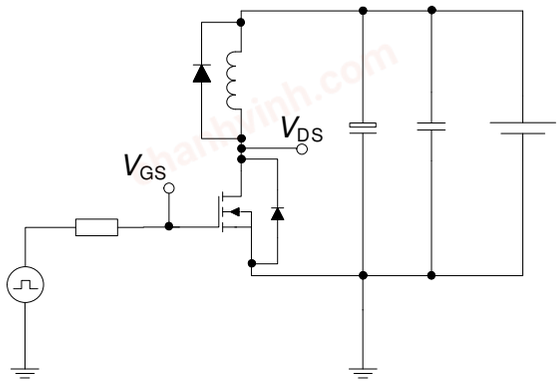
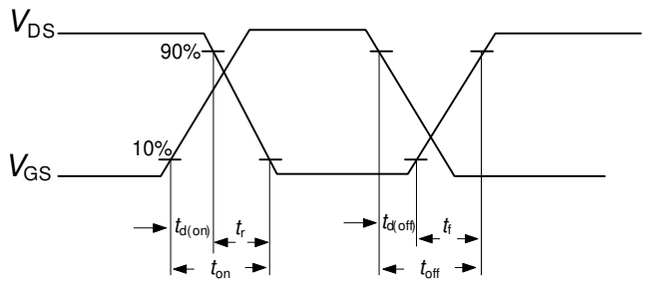
Switching times test circuit for inductive load	Switching time waveform
	

Table 21 Unclamped inductive load test circuit and waveform

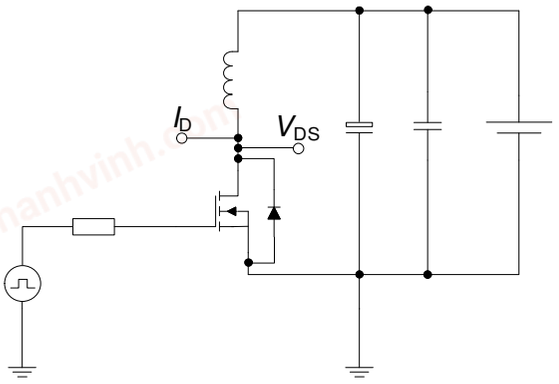
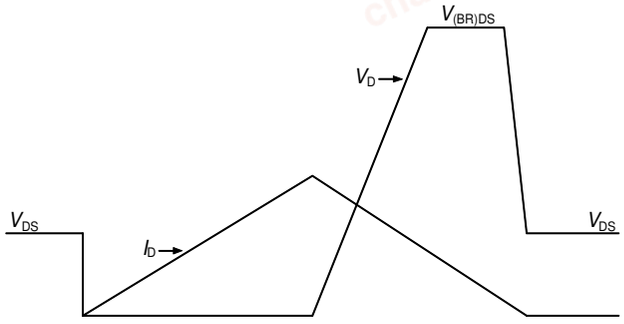
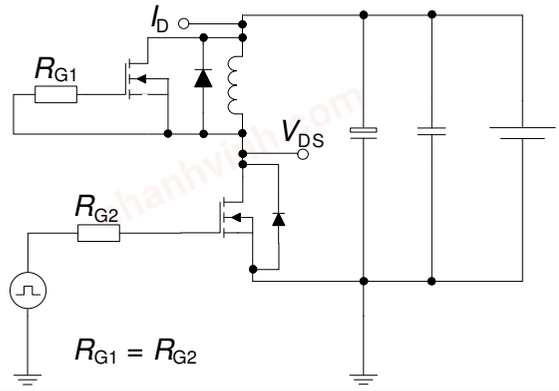
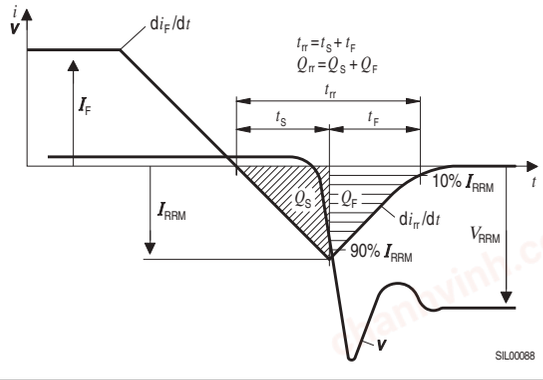
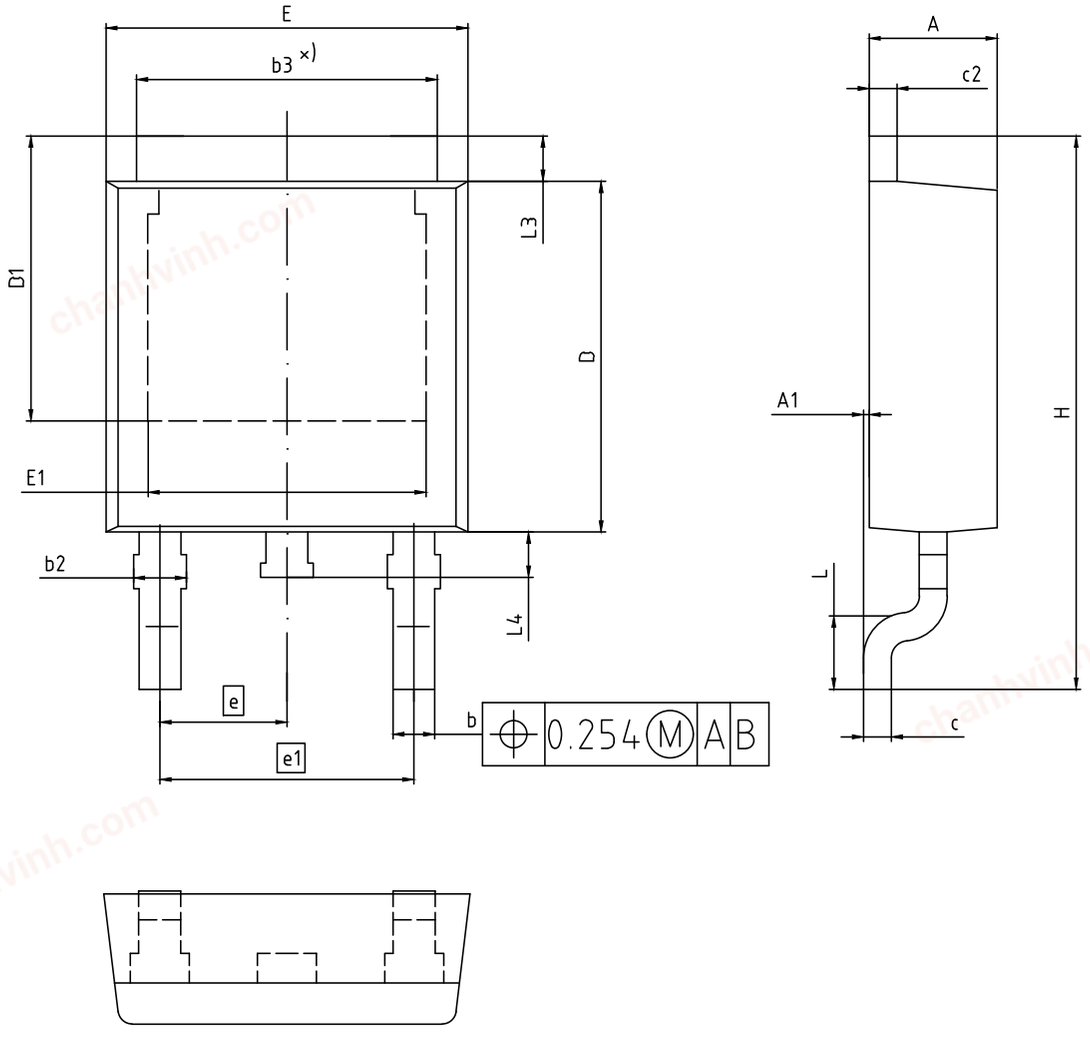
Unclamped inductive load test circuit	Unclamped inductive waveform
	

Table 22 Test circuit and waveform for diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
	

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7 Package outlines



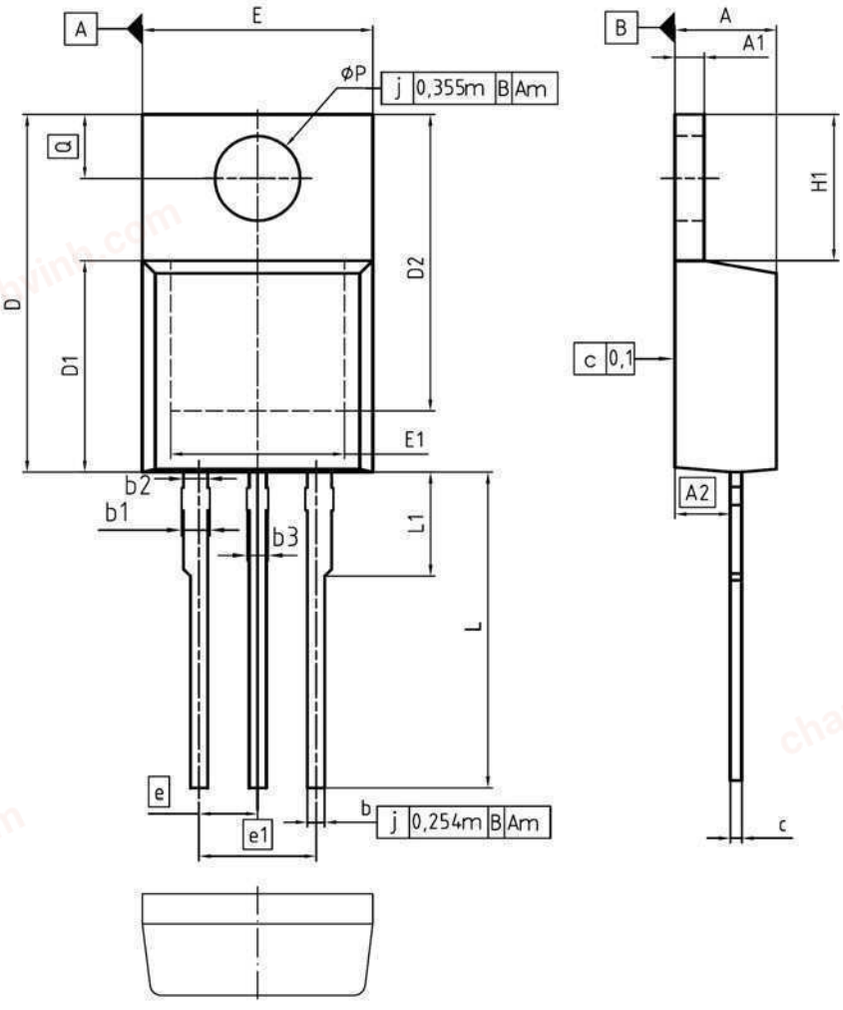
ALL DIMENSIONS REFER TO JEDEC
STANDARD TO-252 AND DO NOT INCLUDE MOLD
FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4,95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

DOCUMENT NO. Z8B00003328
REVISION 07
SCALE: 10:1 0 1 2mm
EUROPEAN PROJECTION
ISSUE DATE 01.04.2020

Figure 1 Outlines TO-252, dimensions in mm

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DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

SCALE 0 2.5 0 2.5 5mm

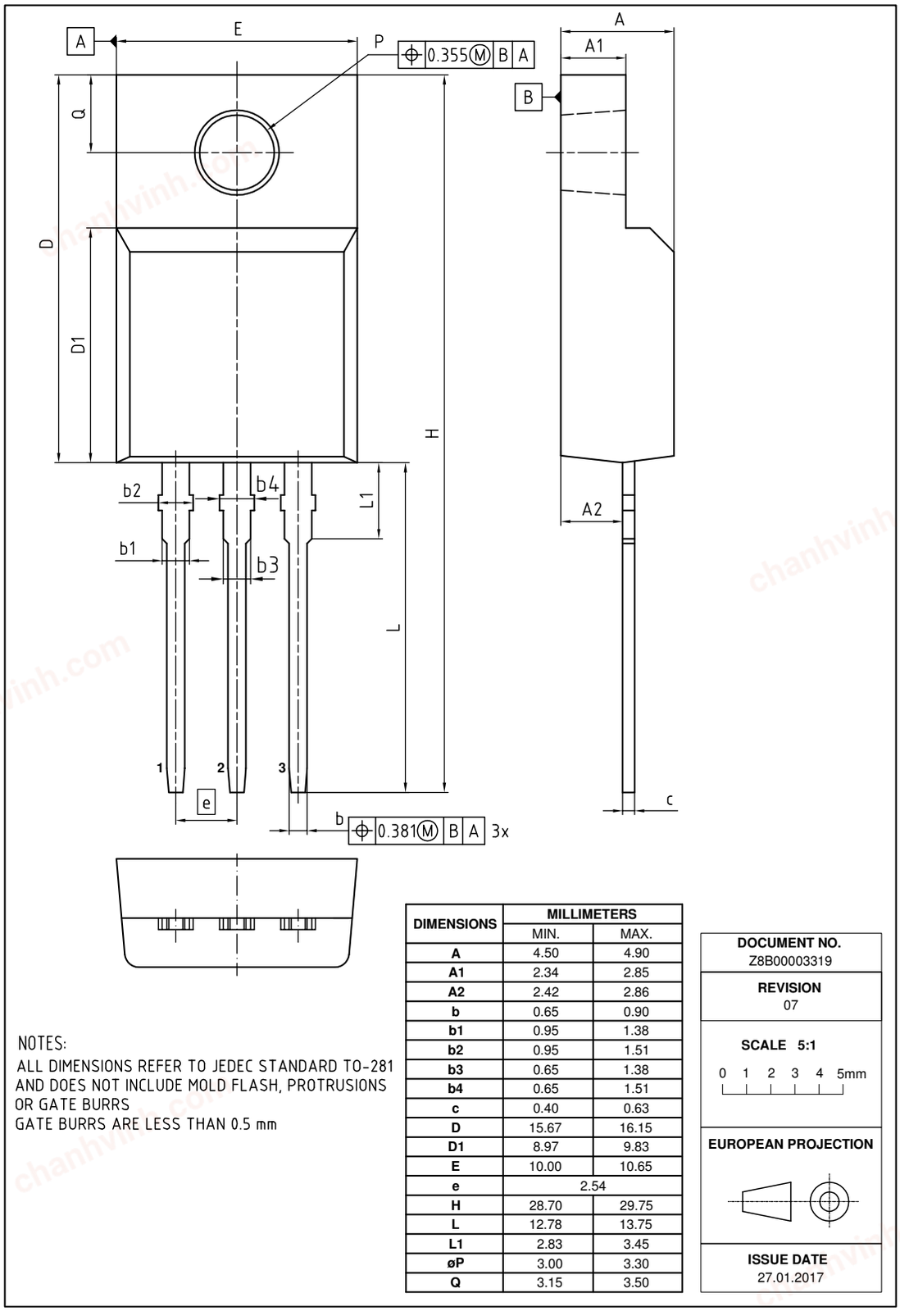
EUROPEAN PROJECTION

ISSUE DATE
23-08-2007

REVISION
05

Figure 2 Outlines TO-220, dimensions in mm/inches

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NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281 AND DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.30
Q	3.15	3.50

DOCUMENT NO.
Z8B00003319

REVISION
07

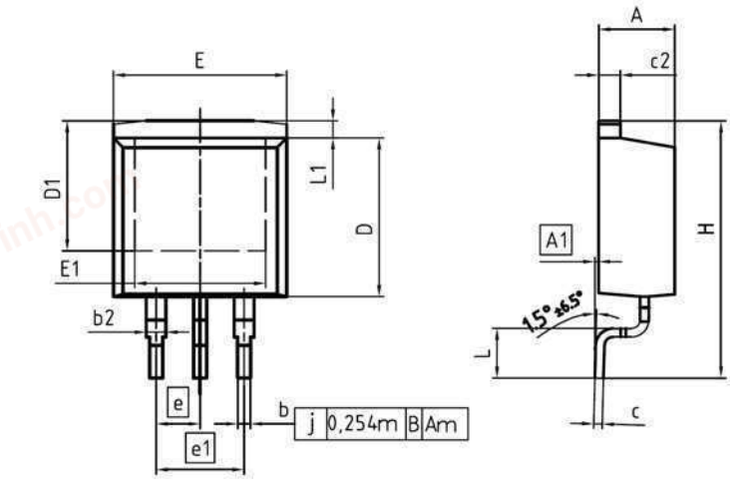
SCALE 5:1
0 1 2 3 4 5mm

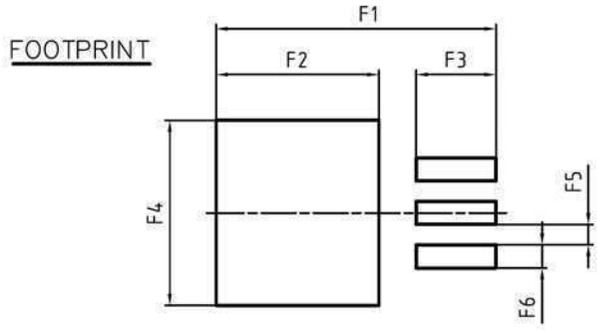
EUROPEAN PROJECTION

ISSUE DATE
27.01.2017

Figure 3 Outlines PG-TO-220 FullPAK,dimensions in mm

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DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	1.10	1.30	0.043	0.051
F6	1.25	1.45	0.049	0.057

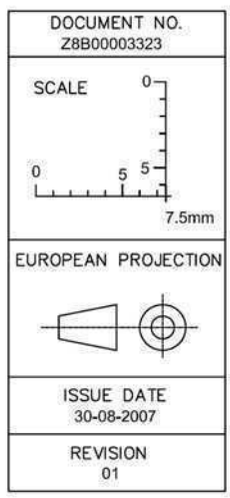


Figure 4 Outlines TO-263, dimensions in mm/inches

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Revision History

IPx60R950C6

Revision: 2020-05-20, Rev. 2.5

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2011-06-08	Release of final Data sheet
2.1	2011-09-14	-
2.2	2015-02-11	PG-TO220 FullPAK package outline update (creation:2014-12-10)
2.3	2015-11-19	Updated with Halogen free logo
2.4	2018-03-06	Outline PG-TO220 FullPAK update
2.5	2020-05-20	Update of the package outlines TO-252

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