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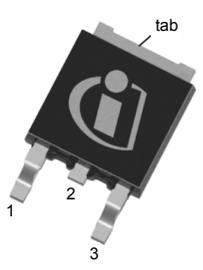
# MOSFET

## StrongIRFET™2 Power-Transistor

DPAK

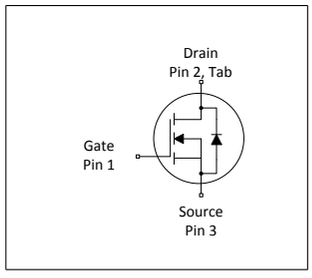



### Features

- Optimized for wide range of applications
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

### Product validation

Qualified according to JEDEC Standard




### Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 40 | V |
| $R_{DS(on),max}$ | 2.3 | mΩ |
| $I_D$ | 143 | A |
| $Q_{oss}$ | 76 | nC |
| $Q_G$ (0V..10V) | 68 | nC |

| Type / Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| IPD023N04NF2S | PG-TO252-3 | 023N04NS | - |

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# 1 Maximum ratings

at $T_A$=25 °C, unless otherwise specified

**Table 2 Maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current[1] | $I_D$ | -<br>-<br>- | -<br>-<br>- | 143<br>110<br>27 | A | $V_{GS}$=10 V, $T_C$=25 °C<br>$V_{GS}$=10 V, $T_C$=100 °C<br>$V_{GS}$=10 V, $T_A$=25 °C, $R_{THJA}$=50 °C/W[2] |
| Pulsed drain current[3] | $I_{D,pulse}$ | - | - | 572 | A | $T_A$=25 °C |
| Avalanche energy, single pulse[4] | $E_{AS}$ | - | - | 167 | mJ | $I_D$=70 A, $R_{GS}$=25 Ω |
| Gate source voltage | $V_{GS}$ | -20 | - | 20 | V | - |
| Power dissipation | $P_{tot}$ | -<br>- | -<br>- | 150<br>3.0 | W | $T_C$=25 °C<br>$T_A$=25 °C, $R_{THJA}$=50 °C/W[2] |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | - | 175 | °C | - |

# 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | 1.0 | °C/W | - |
| Thermal resistance, junction - ambient, 6 cm² cooling area[2] | $R_{thJA}$ | - | - | 50 | °C/W | - |
| Thermal resistance, junction - ambient, minimal footprint | $R_{thJA}$ | - | - | 75 | °C/W | - |

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

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# 3 Electrical characteristics

at $T_j$=25 °C, unless otherwise specified

## Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 40 | - | - | V | $V_{GS}$=0 V, $I_D$=1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 2.2 | 2.8 | 3.4 | V | $V_{DS}$=$V_{GS}$, $I_D$=81 µA |
| Zero gate voltage drain current | $I_{DSS}$ | -<br>- | 0.1<br>10 | 1<br>100 | µA | $V_{DS}$=40 V, $V_{GS}$=0 V, $T_j$=25 °C<br>$V_{DS}$=40 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 10 | 100 | nA | $V_{GS}$=20 V, $V_{DS}$=0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | -<br>- | 1.9<br>2.2 | 2.3<br>3.1 | mΩ | $V_{GS}$=10 V, $I_D$=70 A<br>$V_{GS}$=6 V, $I_D$=35 A |
| Gate resistance | $R_G$ | - | 3.0 | - | Ω | - |
| Transconductance[1)] | $g_{fs}$ | 125 | - | - | S | \|$V_{DS}$\|≥2\|$I_D$\|$R_{DS(on)max}$, $I_D$=70 A |

## Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 4800 | - | pF | $V_{GS}$=0 V, $V_{DS}$=20 V, $f$=1 MHz |
| Output capacitance | $C_{oss}$ | - | 1800 | - | pF | $V_{GS}$=0 V, $V_{DS}$=20 V, $f$=1 MHz |
| Reverse transfer capacitance | $C_{rss}$ | - | 98 | - | pF | $V_{GS}$=0 V, $V_{DS}$=20 V, $f$=1 MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 16 | - | ns | $V_{DD}$=20 V, $V_{GS}$=10 V, $I_D$=70 A, $R_{G,ext}$=1.6 Ω |
| Rise time | $t_r$ | - | 15 | - | ns | $V_{DD}$=20 V, $V_{GS}$=10 V, $I_D$=70 A, $R_{G,ext}$=1.6 Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 35 | - | ns | $V_{DD}$=20 V, $V_{GS}$=10 V, $I_D$=70 A, $R_{G,ext}$=1.6 Ω |
| Fall time | $t_f$ | - | 15 | - | ns | $V_{DD}$=20 V, $V_{GS}$=10 V, $I_D$=70 A, $R_{G,ext}$=1.6 Ω |

## Table 6 Gate charge characteristics[2)]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 21 | - | nC | $V_{DD}$=20 V, $I_D$=70 A, $V_{GS}$=0 to 10 V |
| Gate charge at threshold | $Q_{g(th)}$ | - | 13.5 | - | nC | $V_{DD}$=20 V, $I_D$=70 A, $V_{GS}$=0 to 10 V |
| Gate to drain charge | $Q_{gd}$ | - | 13 | - | nC | $V_{DD}$=20 V, $I_D$=70 A, $V_{GS}$=0 to 10 V |
| Switching charge | $Q_{sw}$ | - | 20 | - | nC | $V_{DD}$=20 V, $I_D$=70 A, $V_{GS}$=0 to 10 V |
| Gate charge total[1)] | $Q_g$ | - | 68 | 102 | nC | $V_{DD}$=20 V, $I_D$=70 A, $V_{GS}$=0 to 10 V |
| Gate plateau voltage | $V_{plateau}$ | - | 4.3 | - | V | $V_{DD}$=20 V, $I_D$=70 A, $V_{GS}$=0 to 10 V |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | - | 61 | - | nC | $V_{DS}$=0.1 V, $V_{GS}$=0 to 10 V |
| Output charge | $Q_{oss}$ | - | 76 | - | nC | $V_{DS}$=20 V, $V_{GS}$=0 V |

[1)] Defined by design. Not subject to production test.
[2)] See "Gate charge waveforms" for parameter definition

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## Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | $I_S$ | - | - | 106 | A | $T_C$=25 °C |
| Diode pulse current | $I_{S,pulse}$ | - | - | 572 | A | $T_C$=25 °C |
| Diode forward voltage | $V_{SD}$ | - | 0.87 | 1.1 | V | $V_{GS}$=0 V, $I_F$=70 A, $T_j$=25 °C |
| Reverse recovery time | $t_{rr}$ | - | 32 | - | ns | $V_R$=20 V, $I_F$=70 A, d$i_F$/d$t$=500 A/µs |
| Reverse recovery charge | $Q_{rr}$ | - | 125 | - | nC | $V_R$=20 V, $I_F$=70 A, d$i_F$/d$t$=500 A/µs |

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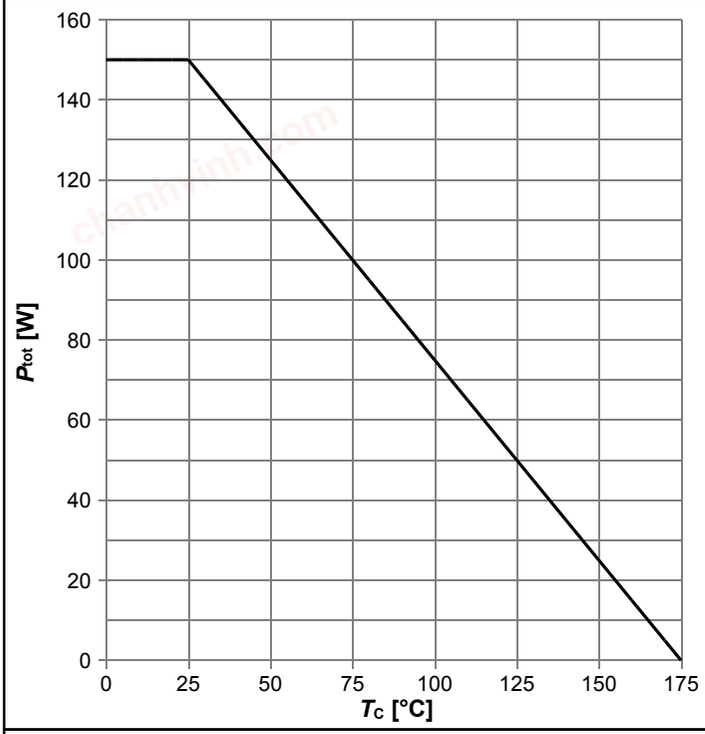
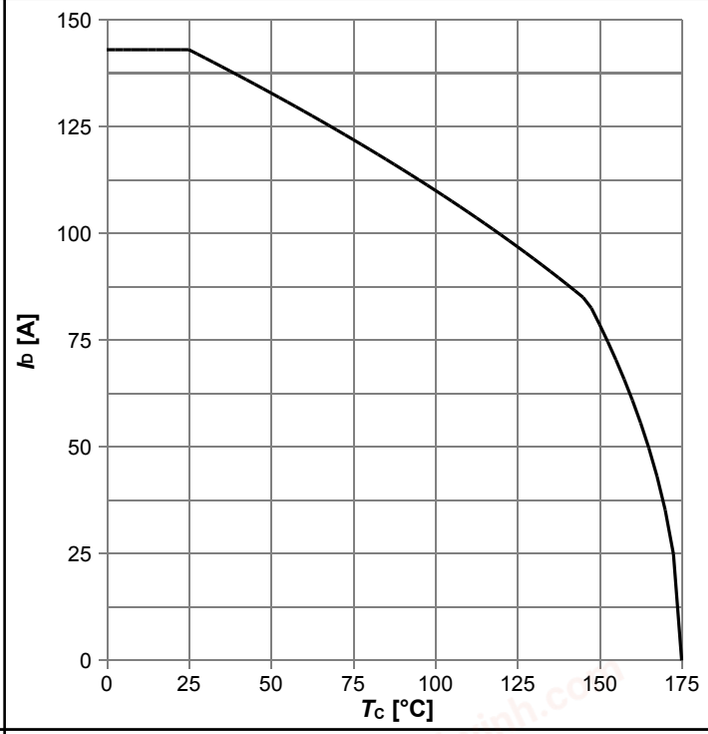
# 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



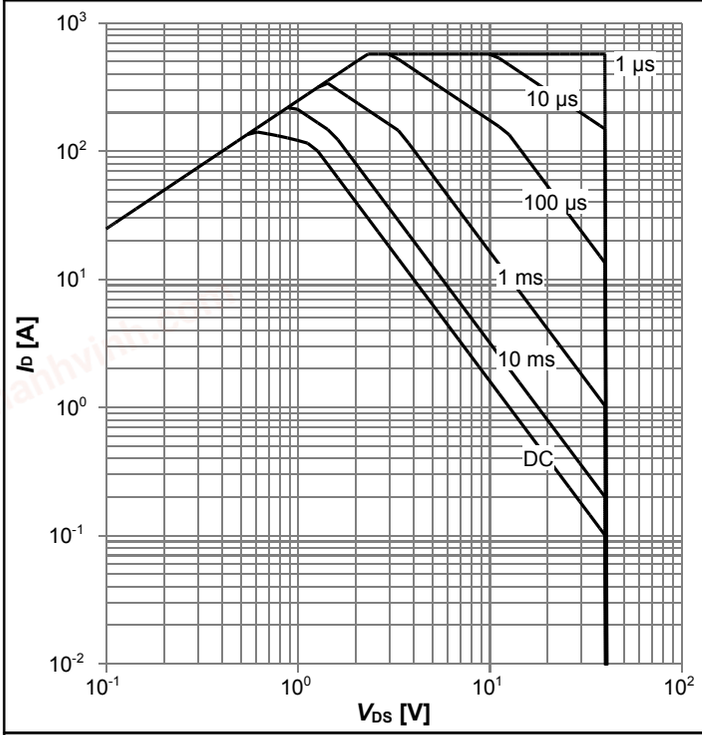

$P_{tot}=f(T_C)$

**Diagram 2: Drain current**



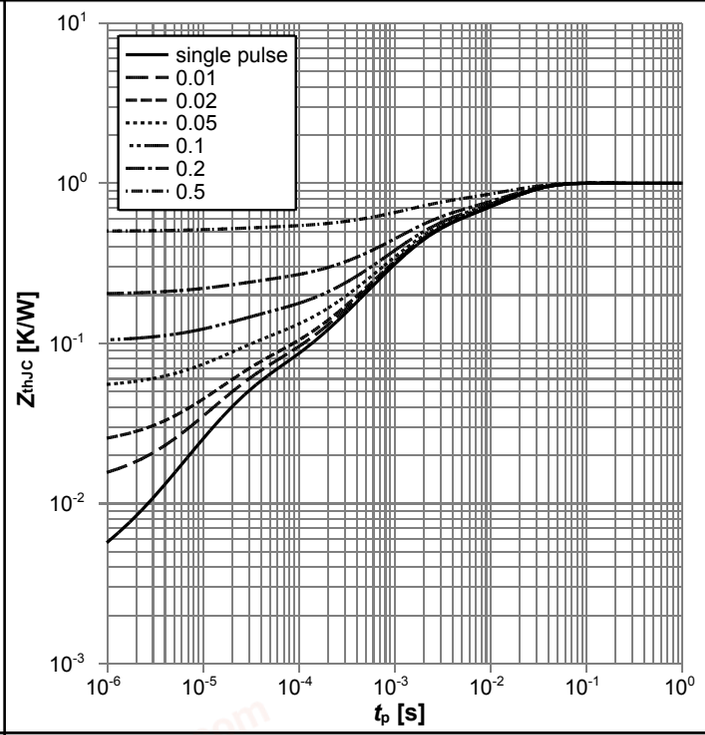

$I_D=f(T_C)$; $V_{GS}\geq 10$ V

**Diagram 3: Safe operating area**




$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**




$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

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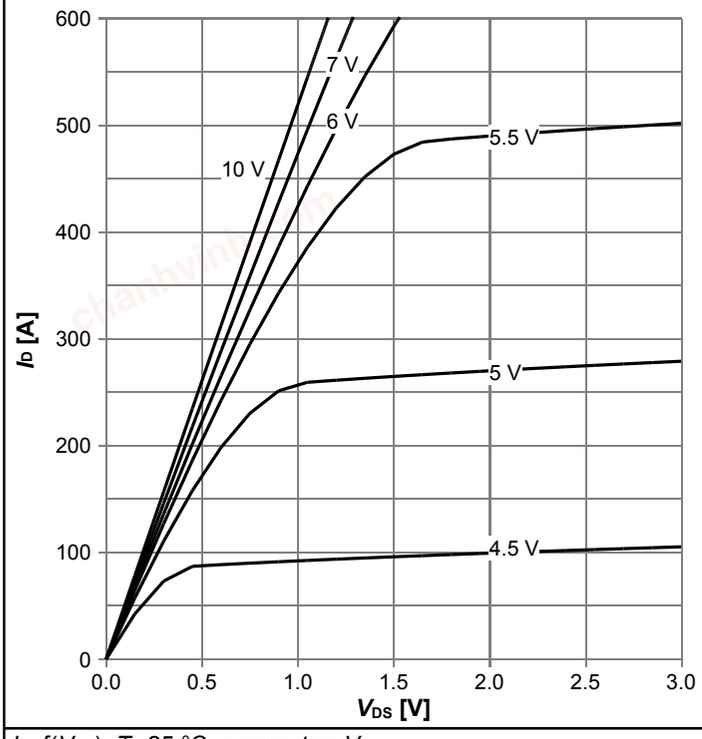
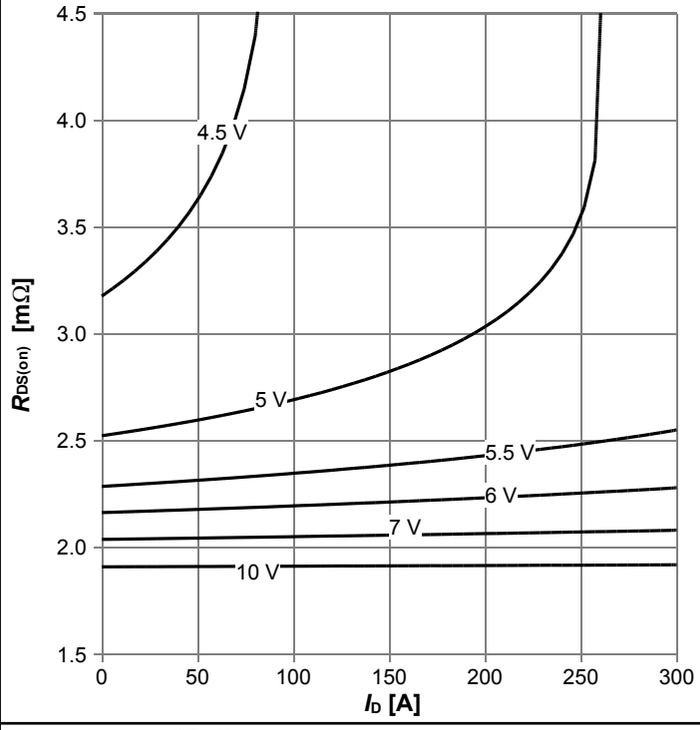
**Diagram 5: Typ. output characteristics**



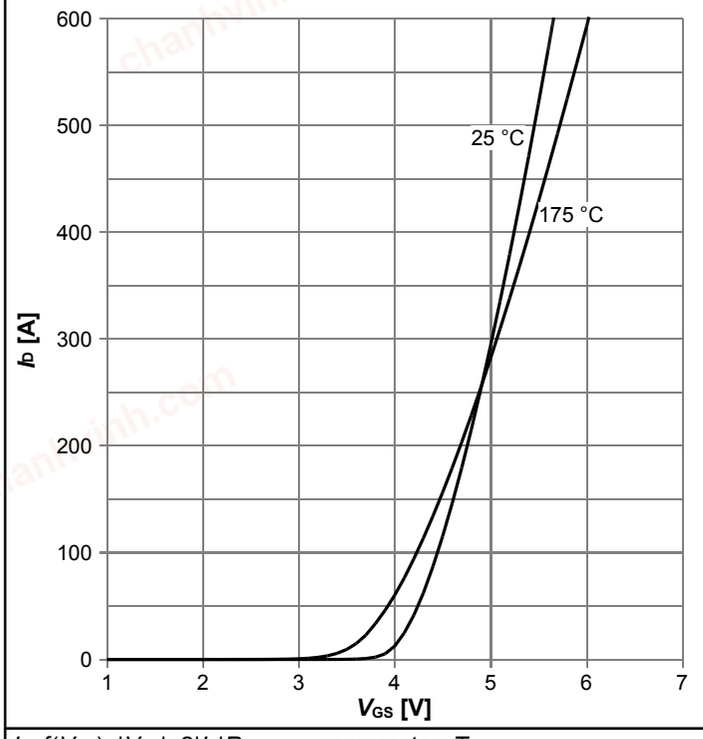

$I_D$=f($V_{DS}$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



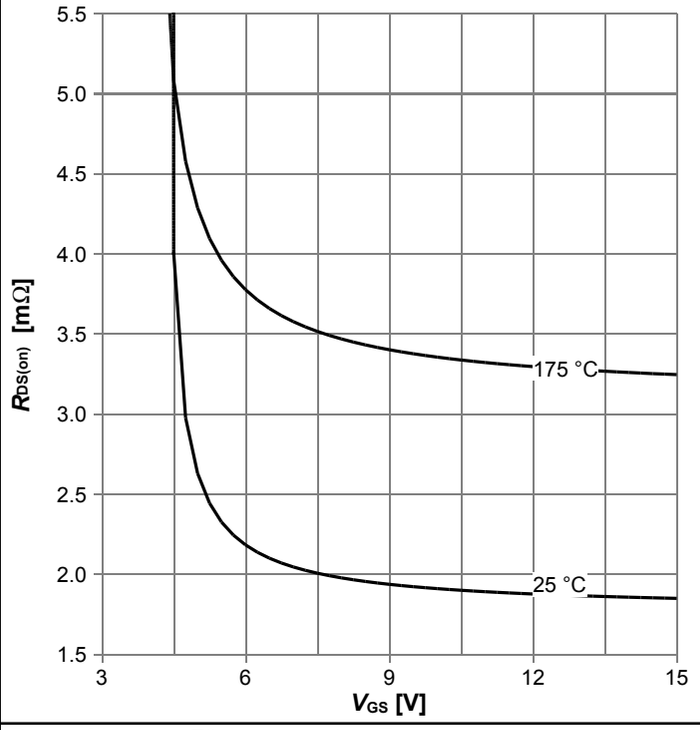

$R_{DS(on)}$=f($I_D$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 7: Typ. transfer characteristics**




$I_D$=f($V_{GS}$), |$V_{DS}$|>2|$I_D$|$R_{DS(on)max}$; parameter: $T_j$

**Diagram 8: Typ. drain-source on resistance**




$R_{DS(on)}$=f($V_{GS}$), $I_D$=70 A; parameter: $T_j$

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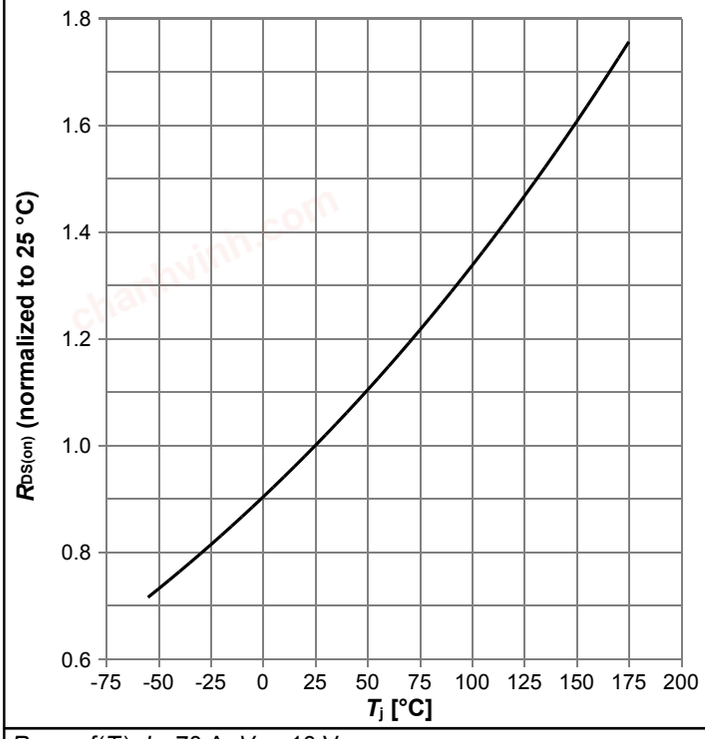
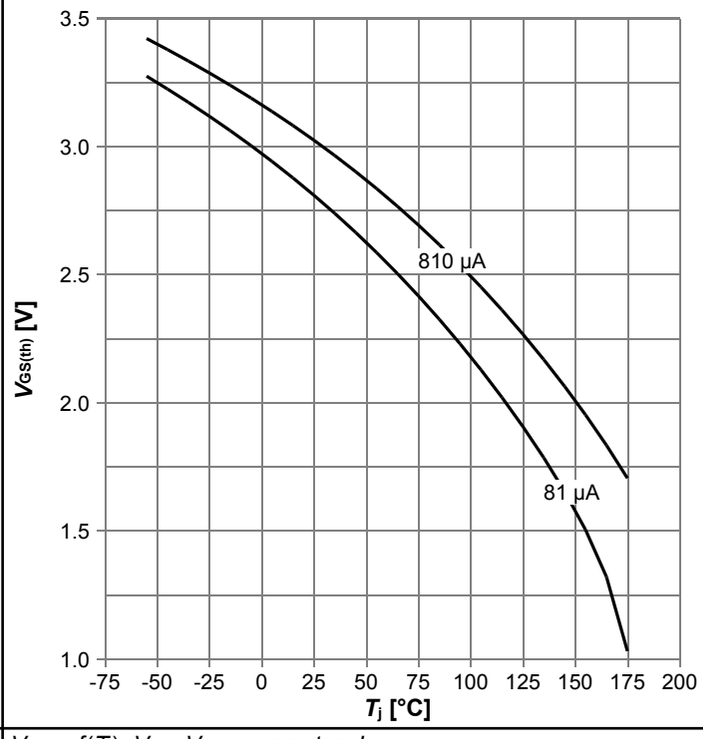
**Diagram 9: Normalized drain-source on resistance**



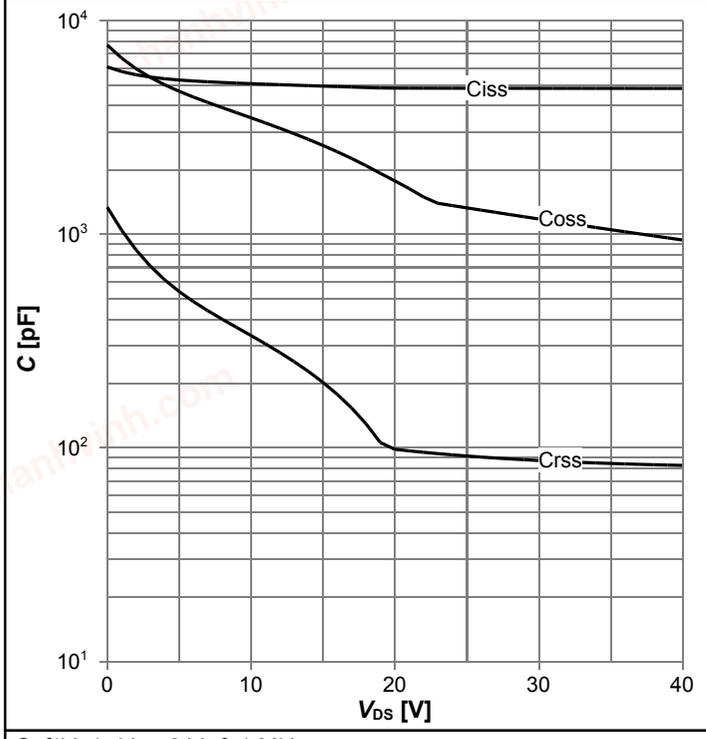

$R_{DS(on)}$=f($T_j$), $I_D$=70 A, $V_{GS}$=10 V

**Diagram 10: Typ. gate threshold voltage**



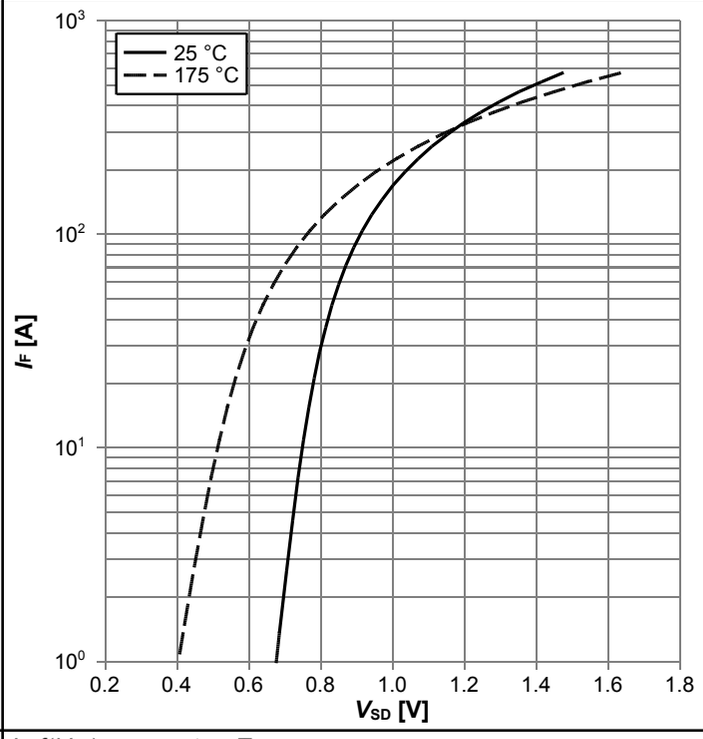

$V_{GS(th}$=f($T_j$), $V_{GS}$=$V_{DS}$; parameter: $I_D$

**Diagram 11: Typ. capacitances**




$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

**Diagram 12: Typ. forward characteristics of reverse diode**




$I_F$=f($V_{SD}$); parameter: $T_j$

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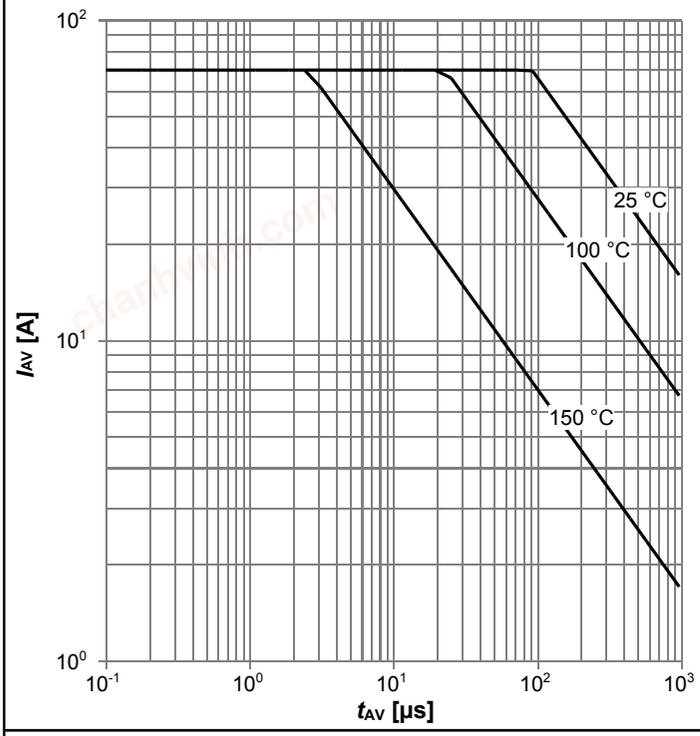
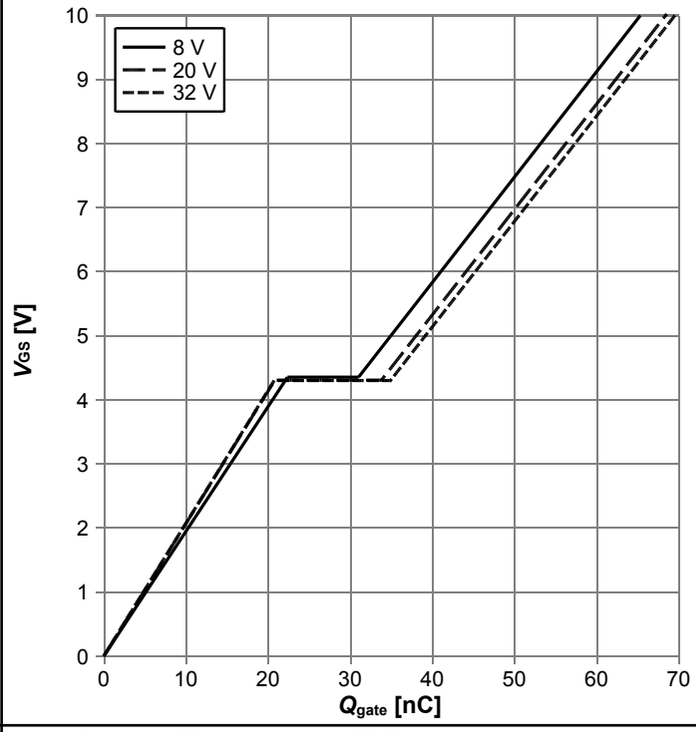
**Diagram 13: Avalanche characteristics**



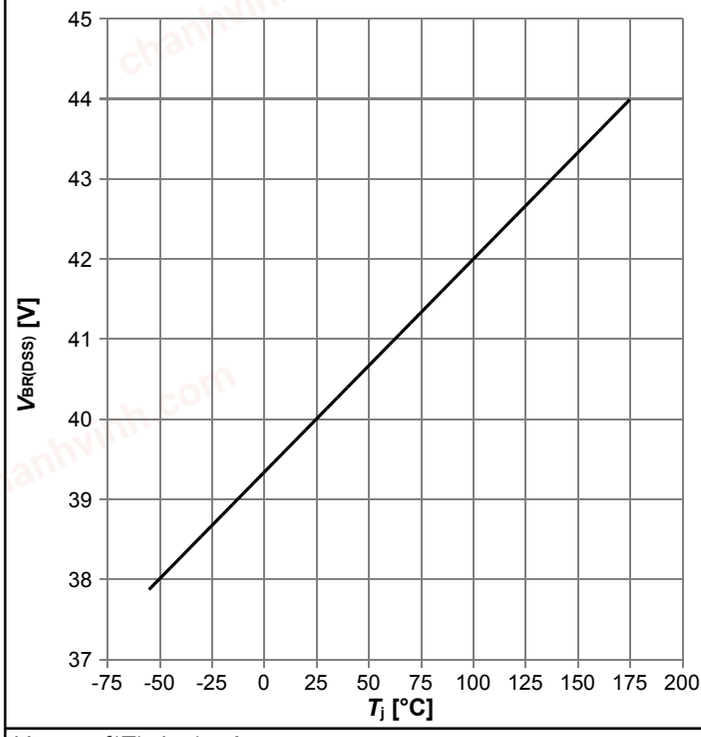

$I_{AS}$=f($t_{AV}$); $R_{GS}$=25 Ω; parameter: $T_{j,start}$

**Diagram 14: Typ. gate charge**



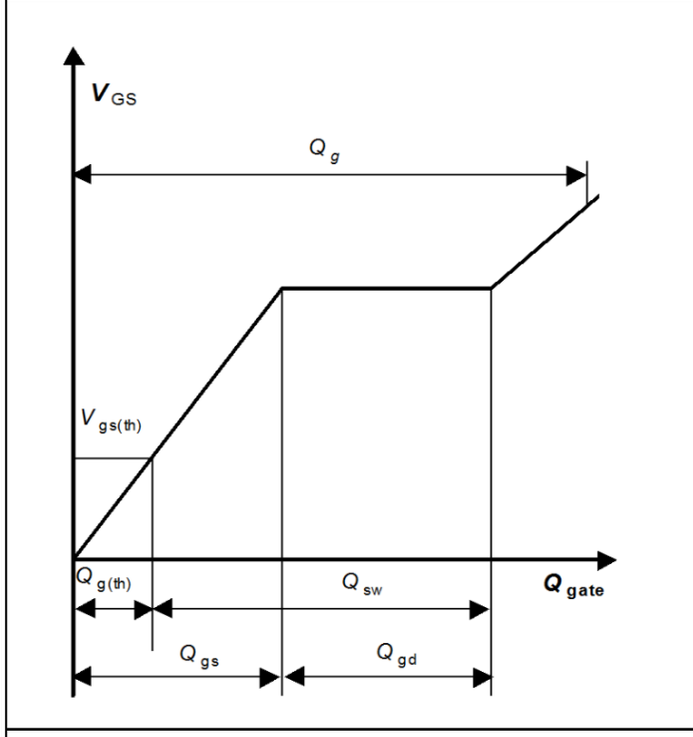

$V_{GS}$=f($Q_{gate}$), $I_D$=70 A pulsed, $T_j$=25 °C; parameter: $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**




$V_{BR(DSS)}$=f($T_j$); $I_D$=1 mA

**Diagram Gate charge waveforms**



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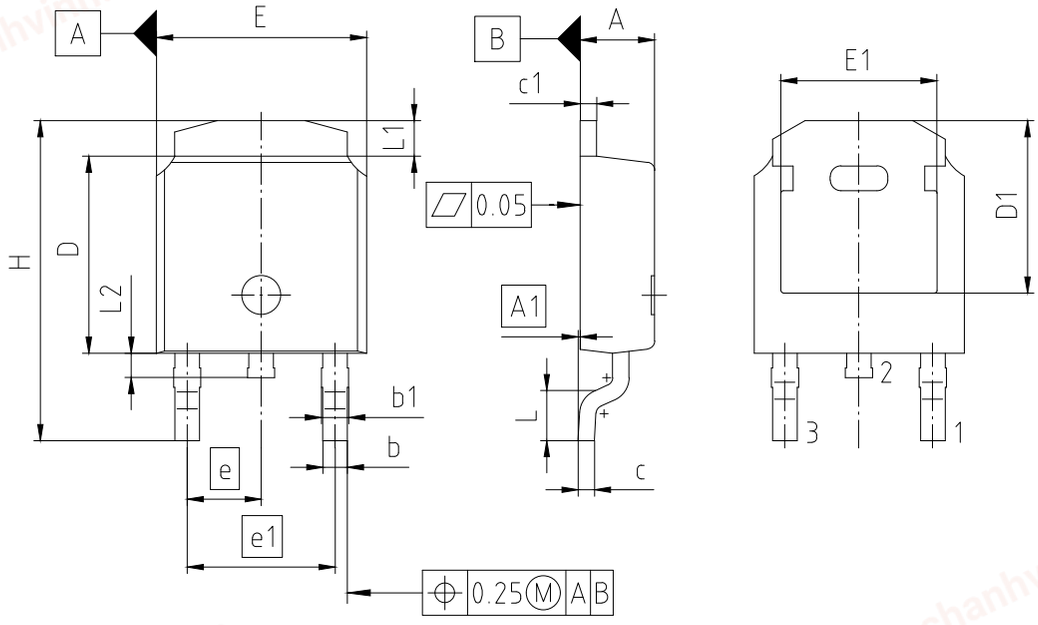
# 5 Package Outlines




| PACKAGE - GROUP NUMBER: | PG-TO252-3-U01 | |
|---|---|---|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 2.18 | 2.39 |
| A1 | 0.00 | 0.13 |
| b | 0.64 | 0.89 |
| b1 | 0.76 | 1.14 |
| c | 0.46 | 0.61 |
| c1 | 0.40 | 0.89 |
| D | 5.97 | 6.22 |
| D1 | 5.21 | --- |
| E | 6.35 | 6.73 |
| E1 | 4.32 | --- |
| e | 2.29 | |
| e1 | 4.58 | |
| N | 3 | |
| H | 9.40 | 10.41 |
| L | 1.40 | 1.78 |
| L1 | 0.89 | 1.27 |
| L2 | 0.50 | 1.02 |

**Figure 1 Outline PG-TO252-3, dimensions in mm**

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## Revision History

IPD023N04NF2S

**Revision: 2022-09-20, Rev. 2.1**

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 2.0 | 2022-07-13 | Release of final version |
| 2.1 | 2022-09-20 | updated Package outline drawing |

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**Infineon Technologies AG**
**81726 München, Germany**
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