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MOSFET

OptiMOS™ Power-Transistor, -150 V

D²PAK



Features

- P-channel
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- Logic level
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

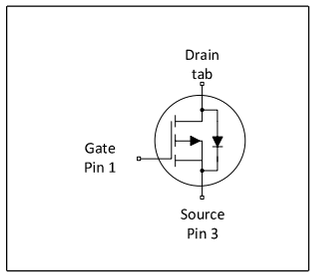


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-150	V
$R_{DS(on),max}$	72	mΩ
I_D	-41	A
Q_{oss}	-61	nC
Q_G	-224	nC

Type / Ordering Code	Package	Marking	Related Links
IPB720P15LM	PG-TO263-3	720P15LM	-

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - -	- - - -	-41 -29 -29 -4.6	A	V_{GS}=-10 V, T_C=25 °C V_{GS}=-10 V, T_C=100 °C V_{GS}=-4.5 V, T_C=100 °C V_{GS}=-4.5 V,T_A=25°C,R_{THJA}=40°C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	-164	A	T_A=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	2020	mJ	I_D=-37 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	300 3.8	W	T_C=25 °C T_A=25 °C, R_{THJA}=40 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.5	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area	R_{thJA}	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint[2]	R_{thJA}	-	-	62	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

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3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-150	-	-	V	V_{GS}=0 V, I_D=-1 mA
Gate threshold voltage	$V_{GS(th)}$	-1	-1.5	-2	V	V_{DS}=V_{GS}, I_D=-5550 µA
Zero gate voltage drain current	I_{DSS}	- -	-0.1 -10	-1 -100	µA	V_{DS}=-150 V, V_{GS}=0 V, T_j=25 °C V_{DS}=-150 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	V_{GS}=-20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	60.1 59.6	72 73	mΩ	V_{GS}=-10 V, I_D=-37 A V_{GS}=-4.5 V, I_D=-30 A
Gate resistance	R_G	-	5.3	-	Ω	-
Transconductance	g_{fs}	-	89	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=-37 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	8400	11000	pF	V_{GS}=0 V, V_{DS}=-75 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	340	440	pF	V_{GS}=0 V, V_{DS}=-75 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	63	110	pF	V_{GS}=0 V, V_{DS}=-75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	23.93	-	ns	V_{DD}=-75 V, V_{GS}=-4.5 V, I_D=-37 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	91.68	-	ns	V_{DD}=-75 V, V_{GS}=-4.5 V, I_D=-37 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	204.9	-	ns	V_{DD}=-75 V, V_{GS}=-4.5 V, I_D=-37 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	128.05	-	ns	V_{DD}=-75 V, V_{GS}=-4.5 V, I_D=-37 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-24	-	nC	V_{DD}=-75 V, I_D=-37 A, V_{GS}=0 to -4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	-12.6	-	nC	V_{DD}=-75 V, I_D=-37 A, V_{GS}=0 to -4.5 V
Gate to drain charge[1)]	Q_{gd}	-	-52	-78	nC	V_{DD}=-75 V, I_D=-37 A, V_{GS}=0 to -4.5 V
Switching charge	Q_{sw}	-	-64	-	nC	V_{DD}=-75 V, I_D=-37 A, V_{GS}=0 to -4.5 V
Gate charge total[1)]	Q_g	-	-110	-138	nC	V_{DD}=-75 V, I_D=-37 A, V_{GS}=0 to -4.5 V
Gate plateau voltage	$V_{plateau}$	-	-2.9	-	V	V_{DD}=-75 V, I_D=-37 A, V_{GS}=0 to -4.5 V
Gate charge total	Q_g	-	-224	-	nC	V_{DD}=-75 V, I_D=-37 A, V_{GS}=0 to -10 V
Output charge[1)]	Q_{oss}	-	-61	-81	nC	V_{DS}=-75 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test.
[2)] See "Gate charge waveforms" for parameter definition

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Table 7 Reverse diode

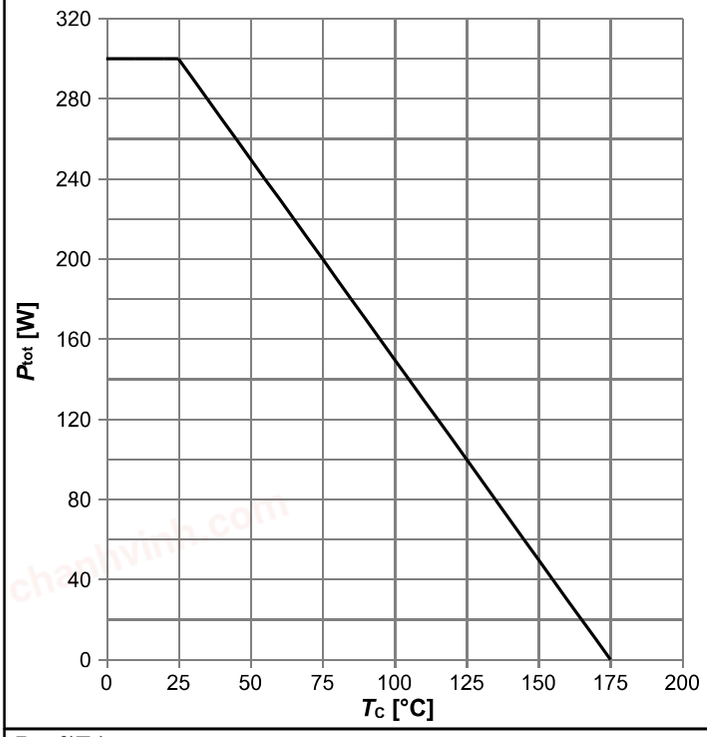
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-41	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	-164	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	-0.84	-1.2	V	V_{GS}=0 V, I_F=-37 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	118.8	237.6	ns	V_R=-75 V, I_F=-37 A, di_F/dt=-100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	671.02	1342.0	nC	V_R=-75 V, I_F=-37 A, di_F/dt=-100 A/µs

[1)] Defined by design. Not subject to production test.

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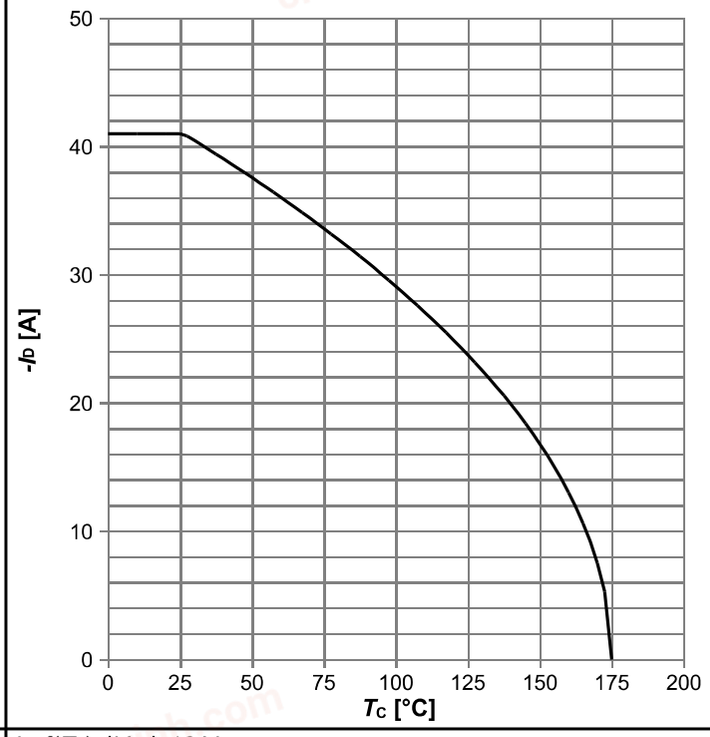
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



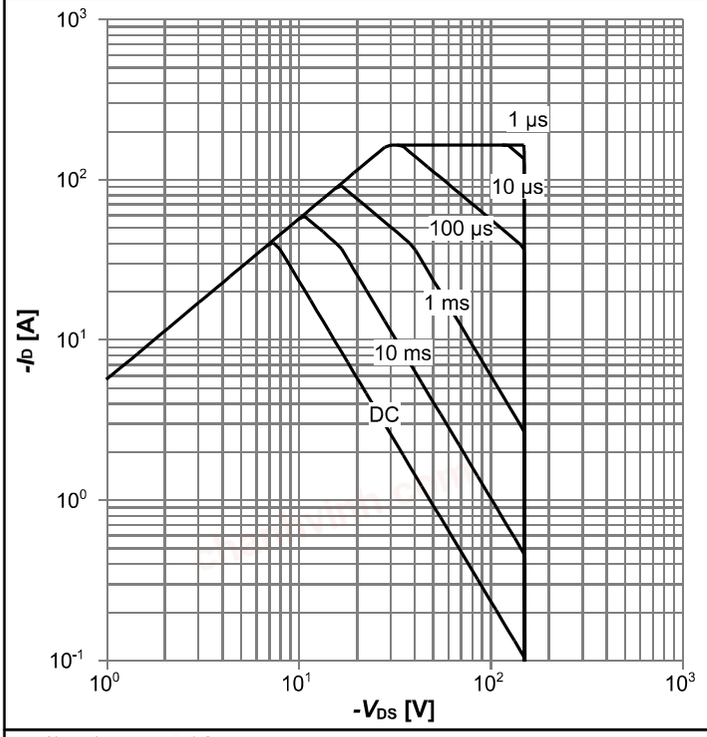
$P_{tot}=f(T_C)$

Diagram 2: Drain current



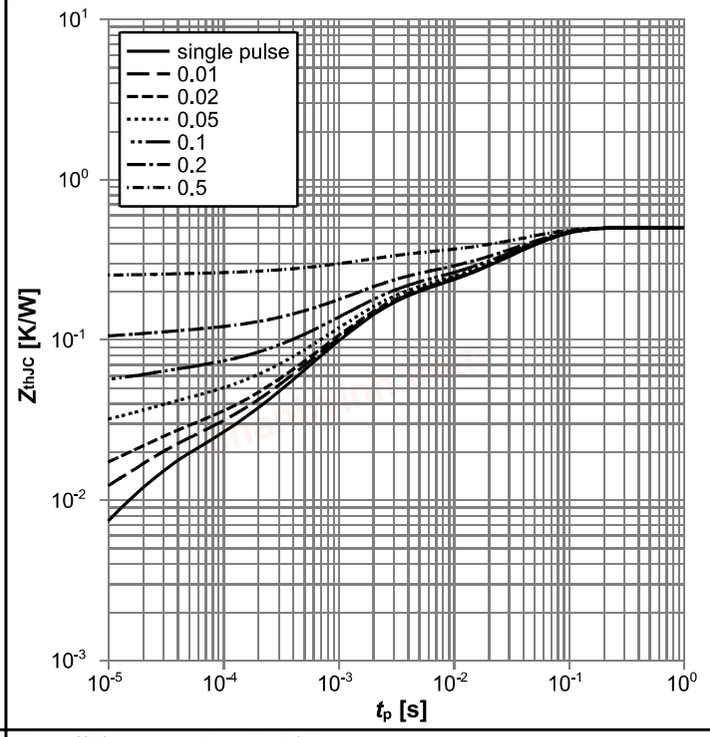
$I_D=f(T_C)$; $|V_{GS}|\geq 10$ V

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

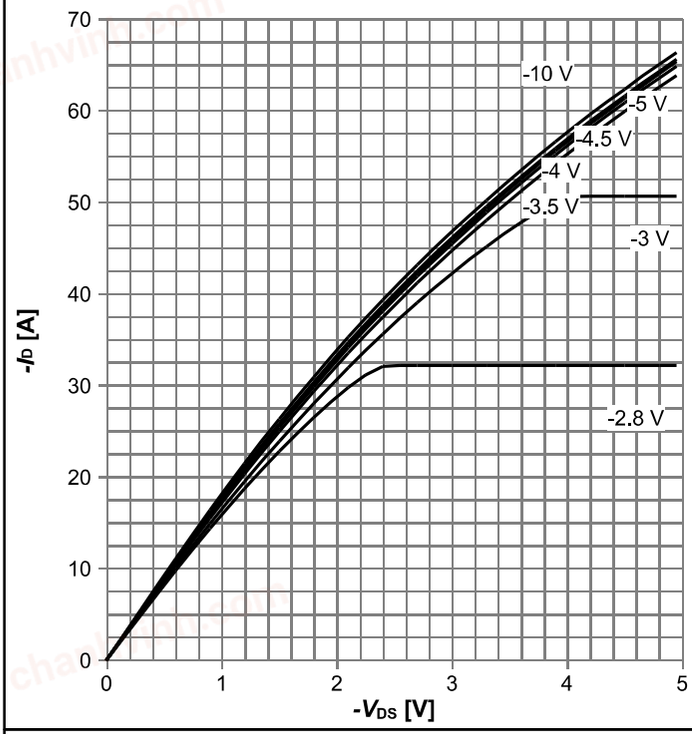
Diagram 4: Max. transient thermal impedance



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

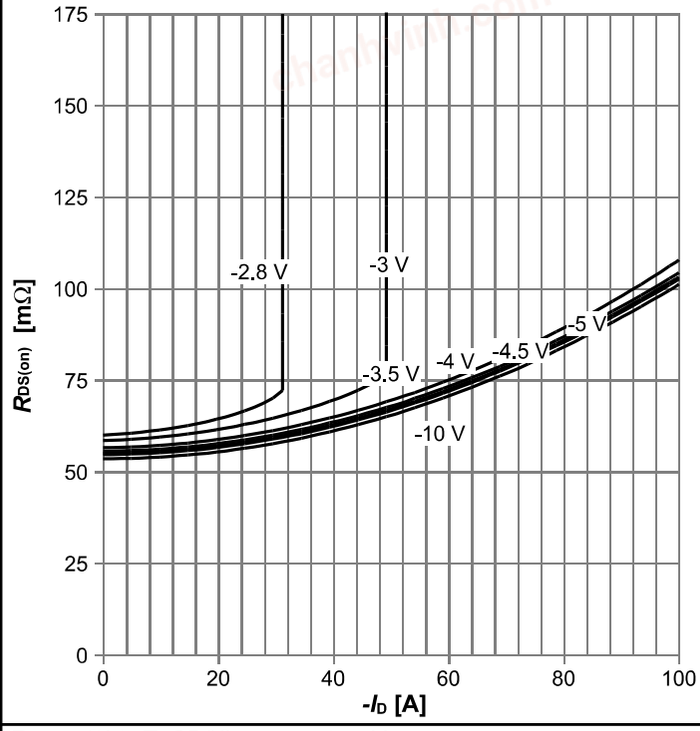
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Diagram 5: Typ. output characteristics



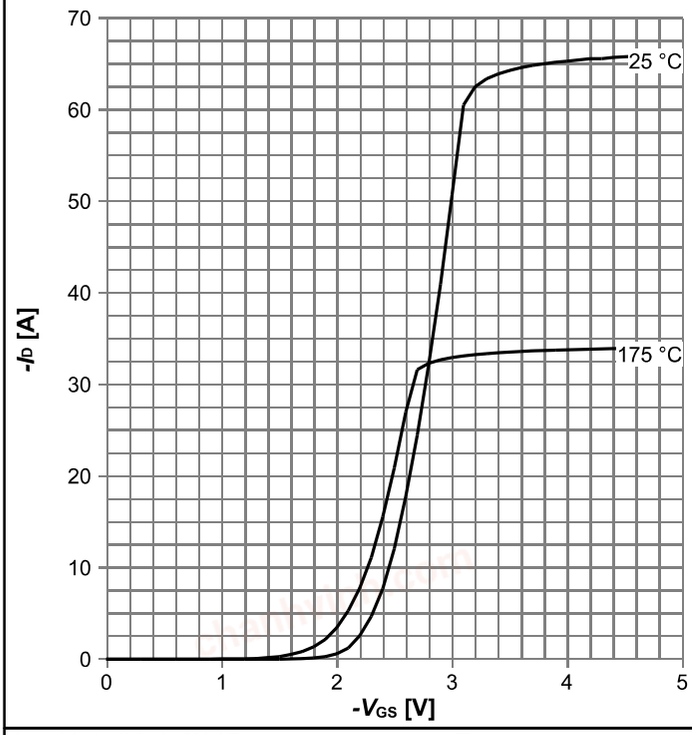
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



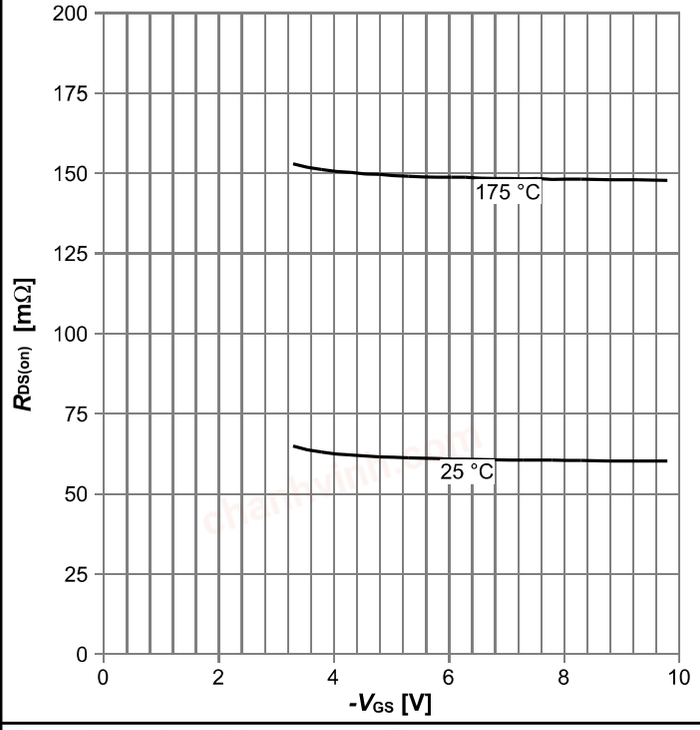
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

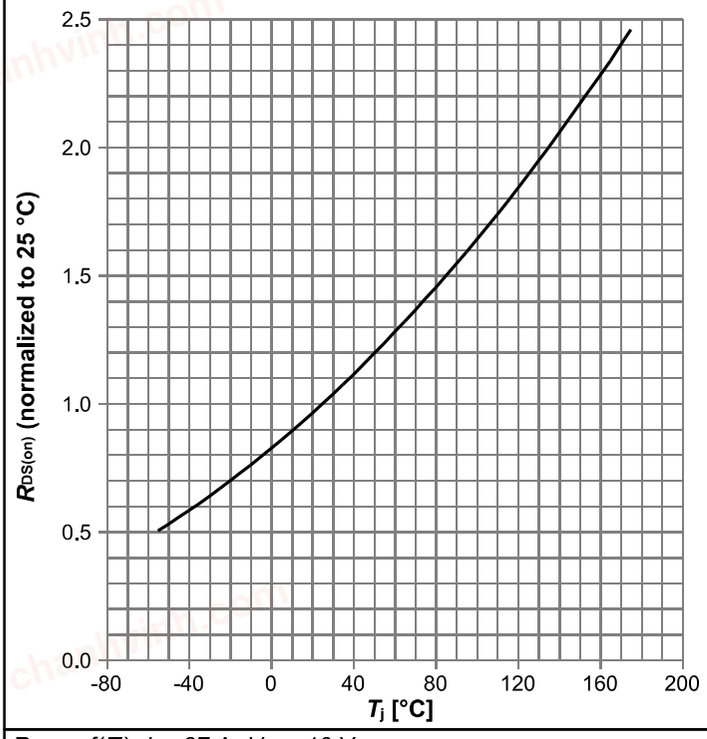
Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=-37 A; parameter: T_j

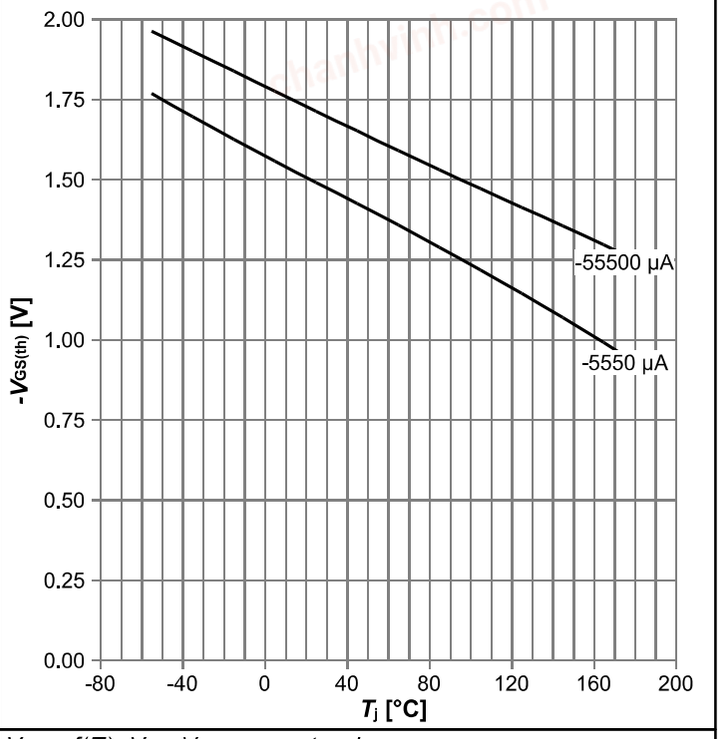
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Diagram 9: Normalized drain-source on resistance



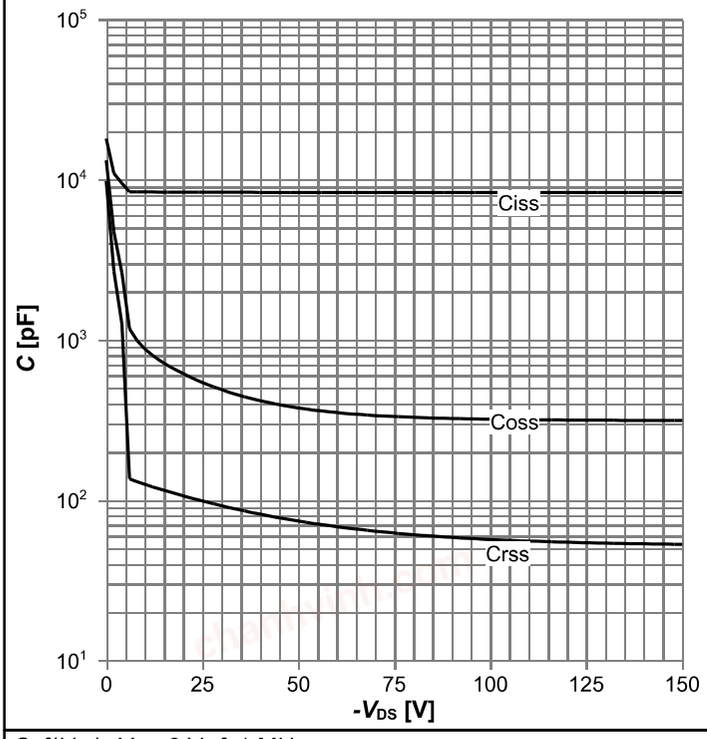
$R_{DS(on)}$=f(T_j), I_D=-37 A, V_{GS}=-10 V

Diagram 10: Typ. gate threshold voltage



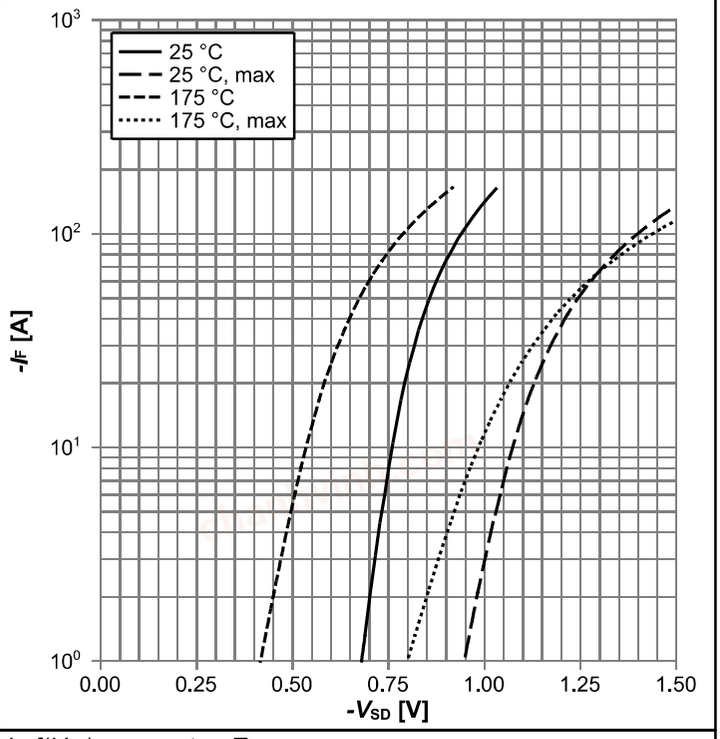
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

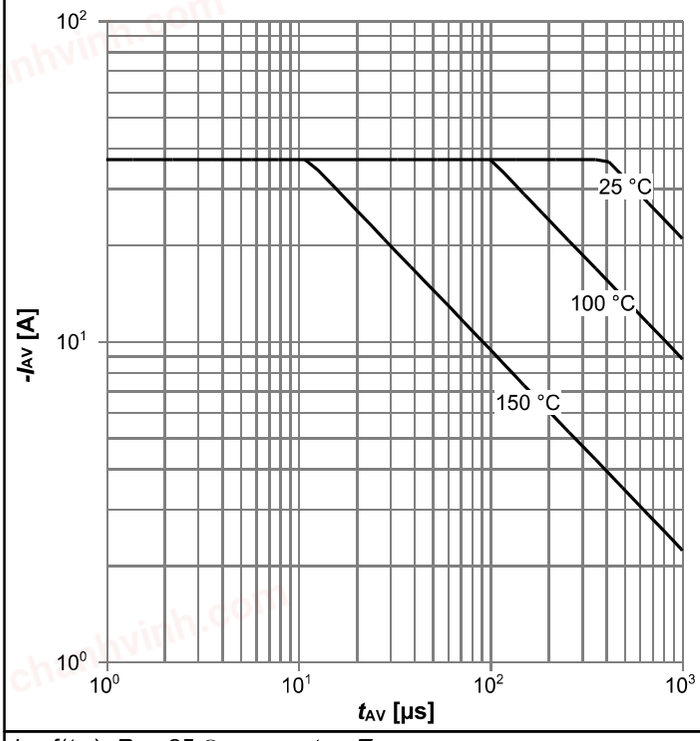
Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

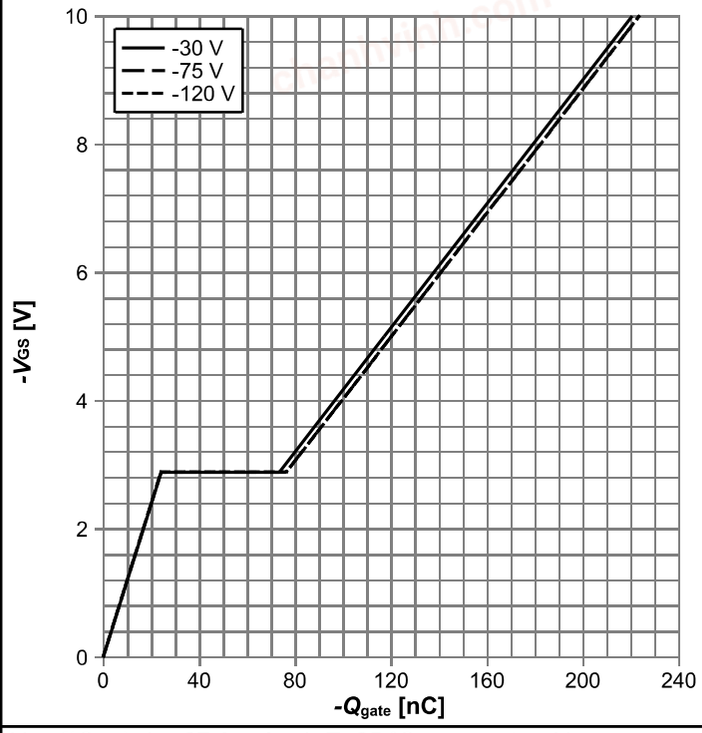
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Diagram 13: Avalanche characteristics



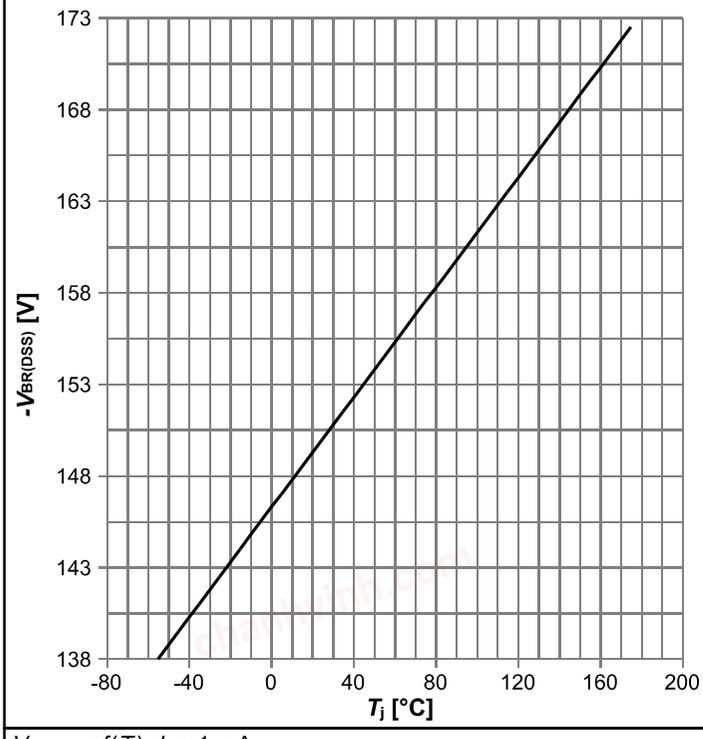
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



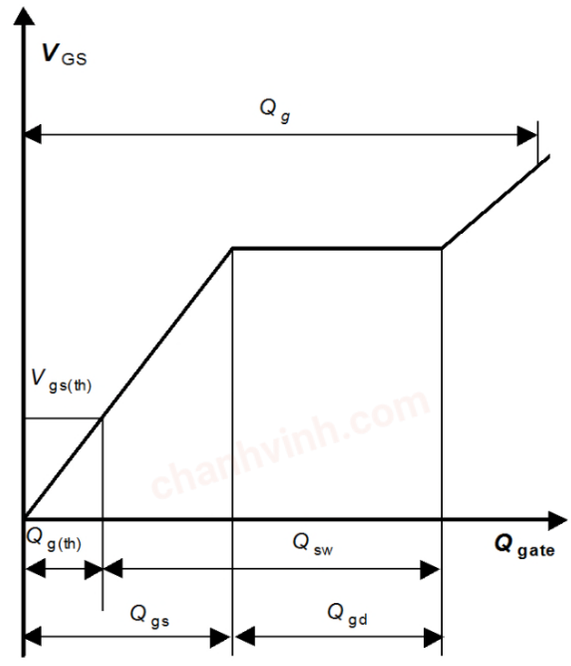
V_{GS}=f(Q_{gate}), I_D=-37 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



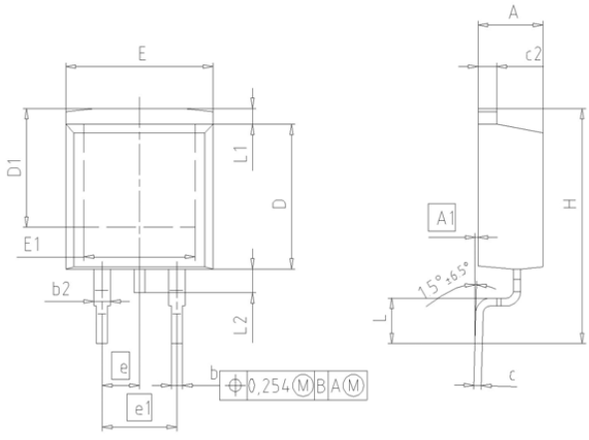
$V_{BR(DSS)}$=f(T_j); I_D=-1 mA

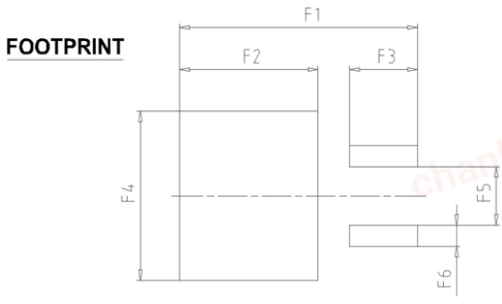
Diagram Gate charge waveforms



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5 Package Outlines



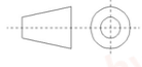


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

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Z8B00003324

SCALE 0 0 5 5 7.5mm

EUROPEAN PROJECTION



ISSUE DATE
30-08-2007

REVISION
01

Figure 1 Outline PG-TO263-3, dimensions in mm/inches

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Revision History

IPB720P15LM

Revision: 2021-05-10, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-05-10	Release of final version

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